

# SN74HCS74 シュミット・トリガ入力、デュアル D タイプ・ポジティブ・エッジ・トリガ・フリップ・フロップ、クリア/プリセット付き

## 1 特長

- 広い動作電圧範囲: 2V~6V
- シュミット・トリガ入力により低速の信号またはノイズの多い信号に対応
- 低消費電力
  - $I_{CC}$ : 100nA (標準値)
  - 入力リーク電流:  $\pm 100$ nA (標準値)
- 6V で  $\pm 7.8$ mA の出力駆動能力
- 広い周囲温度範囲:  $-40^{\circ}\text{C} \sim +125^{\circ}\text{C}$ ,  $T_A$

## 2 アプリケーション

- モメンタリ・スイッチからトグル・スイッチへの変換
- コントローラ・リセット時の信号保持
- 低速エッジレート信号の入力
- ノイズの多い環境での動作
- クロック信号の 2 分割

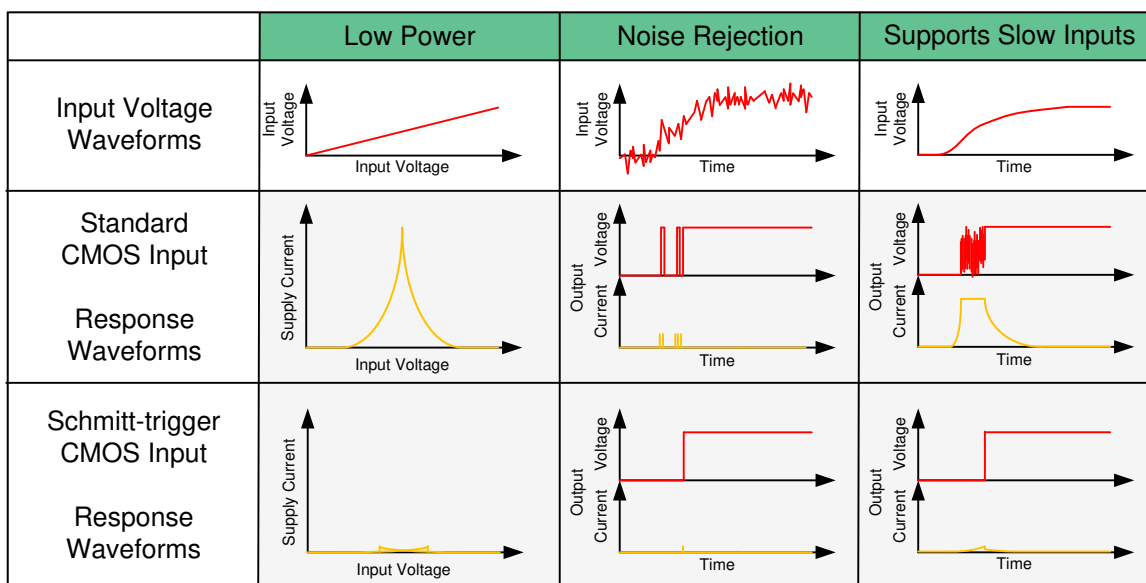
## 3 概要

このデバイスには、2 つの独立した D タイプ正エッジ・トリガのフリップ・フロップが含まれています。すべての入力はシュミット・トリガを備えているため、低速またはノイズの多い入力信号にも対応できます。プリセット ( $\overline{\text{PRE}}$ ) 入力が Low レベルのとき、出力は High になります。クリア ( $\overline{\text{CLR}}$ ) 入力が Low レベルのとき、出力は Low にリセットされます。プリセット機能とクリア機能は非同期であり、他方の入力レベルとは無関係です。 $\overline{\text{PRE}}$  と  $\overline{\text{CLR}}$  が非アクティブ (High) の場合、セットアップ時間の要件を満たすデータ (D) 入力のデータは、クロック (CLK) パルスの正方向エッジで出力 (Q,  $\overline{\text{Q}}$ ) に転送されます。クロックのトリガは電圧レベルで発生し、入力クロック (CLK) 信号の立ち上がり時間とは直接関係しません。ホールド時間が経過した後、データ (D) 入力のデータは、出力 (Q,  $\overline{\text{Q}}$ ) のレベルに影響を及ぼさずに変化させることができます。

### 製品情報

部品番号	パッケージ <sup>(1)</sup>	本体サイズ (公称)
SN74HCS74PW	TSSOP (14)	5.00mm × 4.40mm
SN74HCS74D	SOIC (14)	8.70mm × 3.90mm
SN74HCS74BQA	WQFN (14)	3.00mm × 2.50mm
SN74HCS74DYY	SOT-23-THIN (14)	2.00mm × 4.20mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



シュミット・トリガ入力の利点



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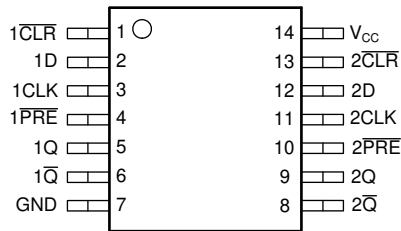
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## 4 Revision History

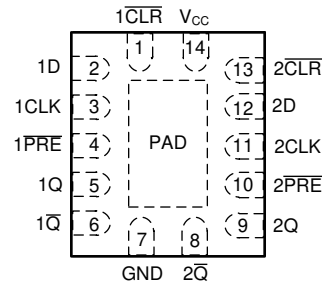
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (January 2021) to Revision D (December 2021)	Page
• 「製品情報」に DYY パッケージの情報を追加.....	1
• Added DYY package information to <i>Pin Configuration and Functions</i> .....	3
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Changes from Revision B (November 2020) to Revision C (January 2021)	Page
• BQA パッケージのステータスを「プレビュー」から「アクティブ」に変更.....	1
• データシートのステータスを「混合ステータス」から「量産データ」に変更.....	1
Changes from Revision A (May 2020) to Revision B (November 2020)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新.....	1
• 「製品情報」に BQA パッケージの情報を追加.....	1
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Changes from Revision * (November 2019) to Revision A (May 2020)	Page
• 「製品情報」に D パッケージの情報を追加.....	1
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## 5 Pin Configuration and Functions



**D, PW or DYY Package**  
**14-Pin SOIC, TSSOP or SOT**  
**Top View**



**BQA Package**  
**14-Pin WQFN**  
**Top View**

## Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
1 CLR	1	Input	Clear for channel 1, active low
1D	2	Input	Data for channel 1
1CLK	3	Input	Clock for channel 1, rising edge triggered
1 PRE	4	Input	Preset for channel 1, active low
1Q	5	Output	Output for channel 1
1 $\bar{Q}$	6	Output	Inverted output for channel 1
GND	7	—	Ground
2 $\bar{Q}$	8	Output	Inverted output for channel 2
2Q	9	Output	Output for channel 2
2 PRE	10	Input	Preset for channel 2, active low
2CLK	11	Input	Clock for channel 2, rising edge triggered
2D	12	Input	Data for channel 2
2 CLR	13	Input	Clear for channel 2, active low
V <sub>CC</sub>	14	—	Positive supply
Thermal Pad <sup>(1)</sup>		—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply

(1) BQA package only.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	-0.5	7	V
I <sub>IK</sub>	Input clamp current <sup>(2)</sup>	V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V		±20 mA
I <sub>OK</sub>	Output clamp current <sup>(2)</sup>	V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V		±20 mA
I <sub>O</sub>	Continuous output current	V <sub>O</sub> = 0 to V <sub>CC</sub>		±35 mA
	Continuous current through V <sub>CC</sub> or GND			±70 mA
T <sub>J</sub>	Junction temperature <sup>(3)</sup>			150 °C
T <sub>stg</sub>	Storage temperature	-65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) Assured by design.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/ JEDEC JS-001 <sup>(1)</sup>	±4000	V
		Charged-device model (CDM), per ANSI/ESDA/ JEDEC JS-002 <sup>(2)</sup>	±1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2	5	6	V
V <sub>I</sub>	Input voltage	0		V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0		V <sub>CC</sub>	V
T <sub>A</sub>	Ambient temperature	-40		125	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74HCS74				UNIT
		PW (TSSOP)	D (SOIC)	BQA (WQFN)	DYY (SOT)	
		14 PINS	14 PINS	14 PINS	14 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	151.7	133.6	109.7	236.5	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	79.4	89.0	111.0	143.2	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	94.7	89.5	77.9	146.0	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	25.2	45.5	20.2	29.5	°C/W

THERMAL METRIC <sup>(1)</sup>		SN74HCS74				UNIT
		PW (TSSOP)	D (SOIC)	BQA (WQFN)	DYY (SOT)	
		14 PINS	14 PINS	14 PINS	14 PINS	
$\Psi_{JB}$	Junction-to-board characterization parameter	94.1	89.1	77.8	145.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	56.6	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

over operating free-air temperature range; typical values measured at  $T_A = 25^\circ\text{C}$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS		$V_{CC}$	MIN	TYP	MAX	UNIT
$V_{T+}$	Positive switching threshold			2 V	0.7		1.5	V
				4.5 V	1.7		3.15	
				6 V	2.1		4.2	
$V_{T-}$	Negative switching threshold			2 V	0.3		1.0	V
				4.5 V	0.9		2.2	
				6 V	1.2		3.0	
$\Delta V_T$	Hysteresis ( $V_{T+} - V_{T-}$ ) <sup>(1)</sup>			2 V	0.2		1.0	V
				4.5 V	0.4		1.4	
				6 V	0.6		1.6	
$V_{OH}$	High-level output voltage	$V_I = V_{IH}$ or $V_{IL}$	$I_{OH} = -20\ \mu\text{A}$	2 V to 6 V	$V_{CC} - 0.1$	$V_{CC} - 0.002$		V
			$I_{OH} = -6\ \text{mA}$	4.5 V	4.0	4.3		
			$I_{OH} = -7.8\ \text{mA}$	6 V	5.4	5.75		
$V_{OL}$	Low-level output voltage	$V_I = V_{IH}$ or $V_{IL}$	$I_{OL} = 20\ \mu\text{A}$	2 V to 6 V		0.002	0.1	V
			$I_{OL} = 6\ \text{mA}$	4.5 V		0.18	0.30	
			$I_{OL} = 7.8\ \text{mA}$	6 V		0.22	0.33	
$I_I$	Input leakage current	$V_I = V_{CC}$ or 0		6 V		$\pm 100$	$\pm 1000$	nA
$I_{CC}$	Supply current	$V_I = V_{CC}$ or 0, $I_O = 0$		6 V		0.1	2	$\mu\text{A}$
$C_i$	Input capacitance			2 V to 6 V			5	pF
$C_{pd}$	Power dissipation capacitance per gate	No load		2 V to 6 V		10		pF

(1) Guaranteed by design.

## 6.6 Switching Characteristics

$C_L = 50\ \text{pF}$ ; over operating free-air temperature range; typical values measured at  $T_A = 25^\circ\text{C}$  (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER		FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	MIN	TYP	MAX	UNIT
$f_{max}$	Max switching frequency			2 V	18	31		MHz
				4.5 V	45	95		
				6 V	65	105		
$t_{pd}$	Propagation delay	PRE or $\overline{\text{CLR}}$	Q or $\overline{Q}$	2 V		19	42	ns
				4.5 V		8	19	
				6 V		7	15	
		CLK	Q or $\overline{Q}$	2 V		19	42	ns
				4.5 V		8	19	
				6 V		7	15	

**SN74HCS74**

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 $C_L = 50$  pF; over operating free-air temperature range; typical values measured at  $T_A = 25^\circ\text{C}$  (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER		FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	MIN	TYP	MAX	UNIT
$t_t$	Transition-time		Q or $\bar{Q}$	2 V	9	16	ns	
				4.5 V	5	9		
				6 V	4	8		

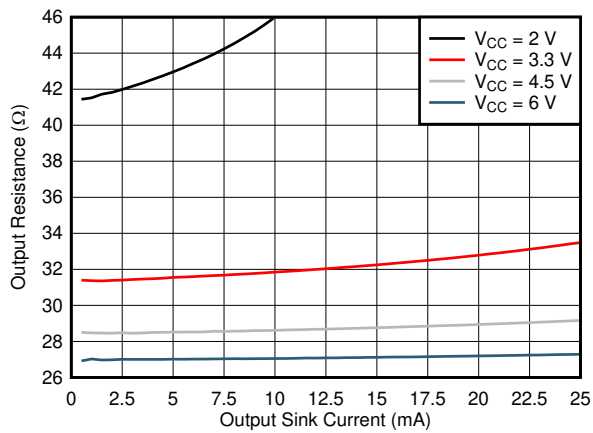
## 6.7 Timing Characteristics

 $C_L = 50$  pF; over operating free-air temperature range (unless otherwise noted). See *Parameter Measurement Information*.

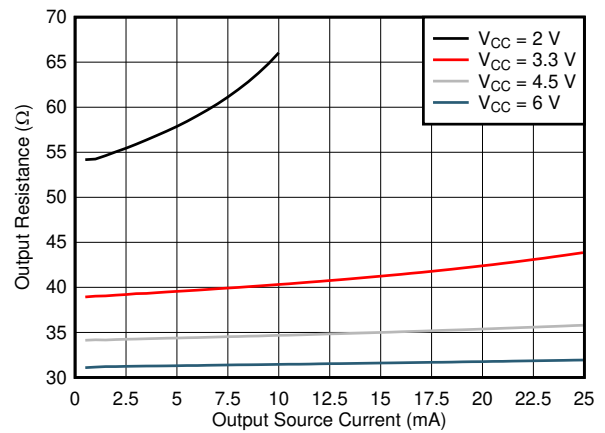
PARAMETER			$V_{CC}$	MIN	MAX	UNIT
$f_{\text{clock}}$	Clock frequency		2 V		18	MHz
			4.5 V		45	
			6 V		65	
$t_w$	Pulse duration	PRE or $\bar{\text{CLR}}$ low	2 V	11	ns	
			4.5 V	11		
			6 V	11		
		CLK high or low	2 V	14	ns	
			4.5 V	12		
			6 V	11		
$t_{su}$	Setup time before CLK high	Data	2 V	24	ns	
			4.5 V	9		
			6 V	6		
		PRE or $\bar{\text{CLR}}$ inactive	2 V	7	ns	
			4.5 V	5		
			6 V	5		
$t_h$	Hold time	Data after CLK $\uparrow$	2 V	0	ns	
			4.5 V	0		
			6 V	0		

## 6.8 Typical Characteristics

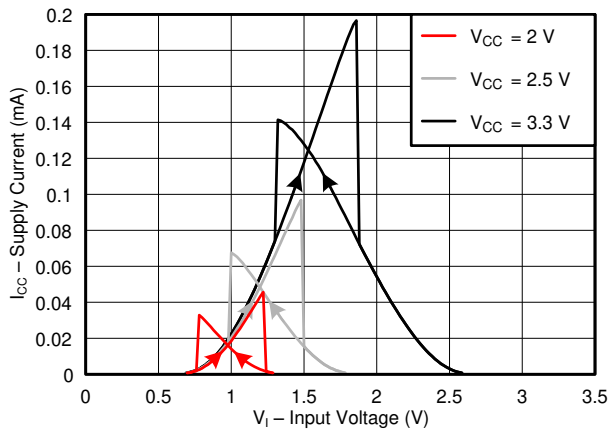
$T_A = 25^\circ\text{C}$



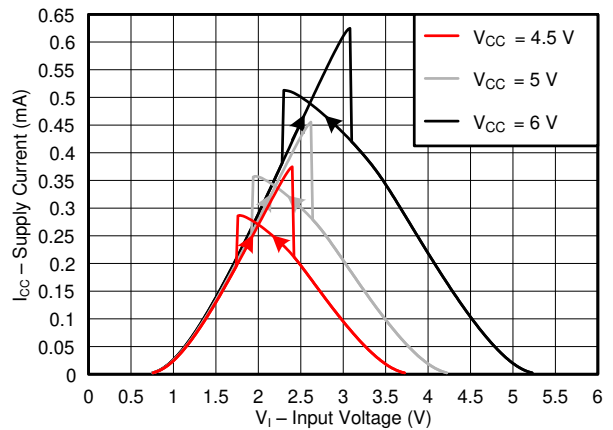
**6-1. Output Driver Resistance in LOW State**



**6-2. Output Driver Resistance in HIGH State**



**6-3. Supply Current Across Input Voltage, 2-, 2.5-, and 3.3-V Supply**



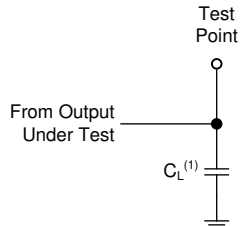
**6-4. Supply Current Across Input Voltage, 4.5-, 5-, and 6-V Supply**

## 7 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_t < 2.5 \text{ ns}$ .

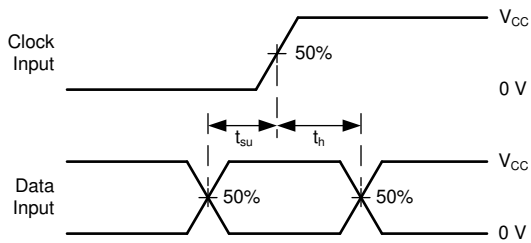
For clock inputs,  $f_{max}$  is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.

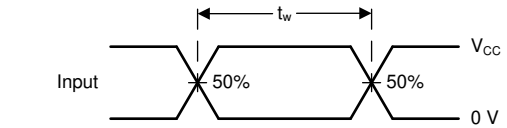


(1)  $C_L$  includes probe and test-fixture capacitance.

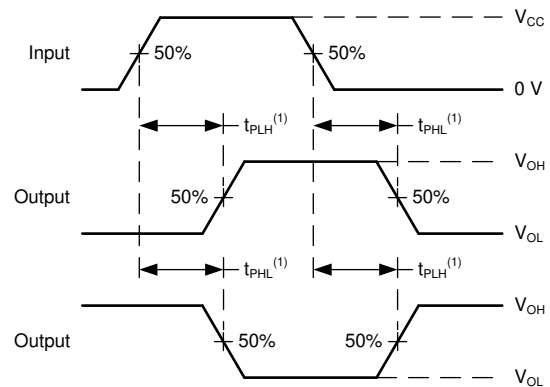
**7-1. Load Circuit for Push-Pull Outputs**



**7-3. Voltage Waveforms, Setup and Hold Times**

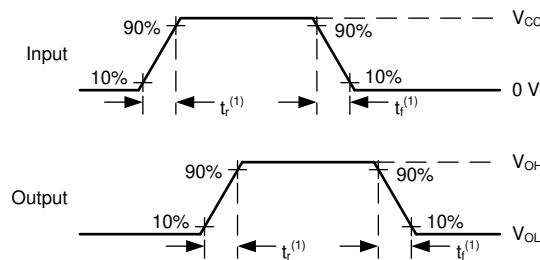


**7-2. Voltage Waveforms, Pulse Duration**



(1) The greater between  $t_{PLH}$  and  $t_{PHL}$  is the same as  $t_{pd}$ .

**7-4. Voltage Waveforms Propagation Delays**



(1) The greater between  $t_r$  and  $t_f$  is the same as  $t_t$ .

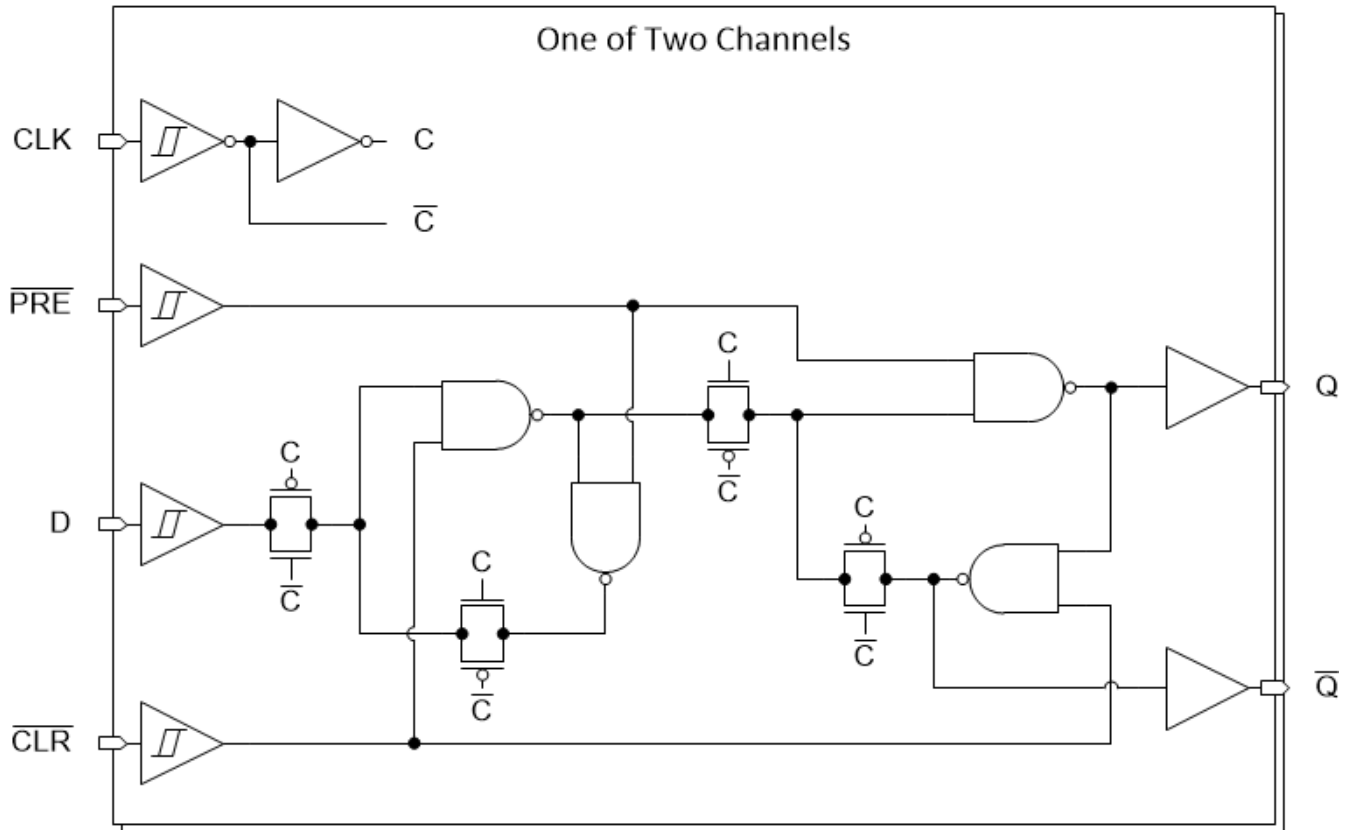
**7-5. Voltage Waveforms, Input and Output Transition Times**

## 8 Detailed Description

### 8.1 Overview

[Logic Diagram \(Positive Logic\) for one channel of SN74HCS74](#) describes the SN74HCS74. As the SN74HCS74 is a dual D-Type positive-edge-triggered flip-flop with clear and preset, the diagram below describes one of the two device flip-flops.

### 8.2 Functional Block Diagram



 8-1. Logic Diagram (Positive Logic) for one channel of SN74HCS74

### 8.3 Feature Description

#### 8.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term "balanced" indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs should be left disconnected.

#### 8.3.2 CMOS Schmitt-Trigger Inputs

This device includes inputs with the Schmitt-trigger architecture. These inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics* table from the input to ground. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings* table, and the maximum input leakage current, given in the *Electrical Characteristics* table, using Ohm's law ( $R = V \div I$ ).

The Schmitt-trigger input architecture provides hysteresis as defined by  $\Delta V_T$  in the *Electrical Characteristics* table, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs with slow transitioning signals will increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see [Understanding Schmitt Triggers](#).

### 8.3.3 Clamp Diode Structure

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in [Electrical Placement of Clamping Diodes for Each Input and Output](#).

**CAUTION**

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

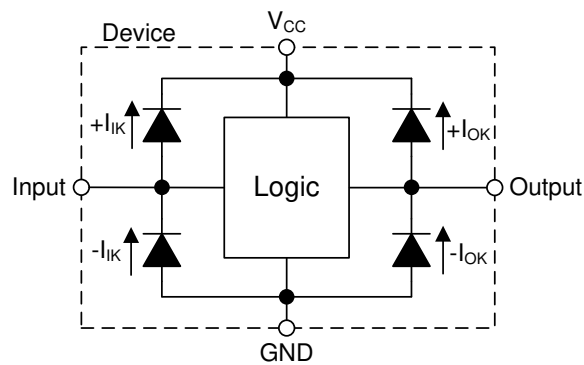


图 8-2. Electrical Placement of Clamping Diodes for Each Input and Output

## 8.4 Device Functional Modes

[Function Table](#) lists the functional modes of the SN74HCS74.

表 8-1. Function Table

INPUTS				OUTPUTS	
PRE	CLR	CLK	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H <sup>(1)</sup>	H <sup>(1)</sup>
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q <sub>0</sub>	Q̄ <sub>0</sub>

- (1) This configuration is nonstable; that is, it does not persist when PRE or CLR returns to its inactive (high) level.

## 9 Application and Implementation

### Note

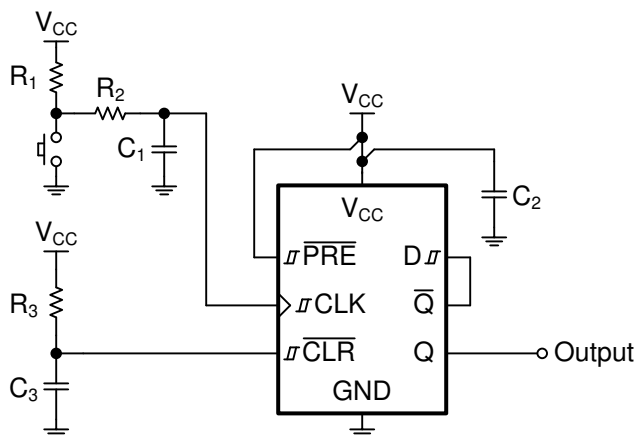
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### 9.1 Application Information

Toggle switches are typically large, mechanically complex and relatively expensive. It is desirable to use a momentary switch instead because they are small, mechanically simple and low cost. Some systems require a toggle switch's functionality but are space or cost constrained and must use a momentary switch instead. The SN74HCS74 has integrated Schmitt-trigger inputs that eliminate the need for a second IC for signal conditioning, reducing the required board space. This makes the SN74HCS74 an ideal device for converting a momentary switch into a toggle switch.

If the data input (D) of the SN74HCS74 is tied to the inverted output ( $\bar{Q}$ ), then each clock pulse will cause the value at the output (Q) to toggle. The momentary switch can be debounced and directly connected to the clock input (CLK) to toggle the output.

### 9.2 Typical Application



9-1. Device Power Button Circuit

#### 9.2.1 Design Requirements

##### 9.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics*.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74HCS74 plus the maximum static supply current,  $I_{CC}$ , listed in *Electrical Characteristics* and any transient current required for switching. The logic device can only source as much current as is provided by the positive supply source. Be sure not to exceed the maximum total current through  $V_{CC}$  listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74HCS74 plus the maximum supply current,  $I_{CC}$ , listed in *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current as can be sunk into its ground connection. Be sure not to exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74HCS74 can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed 50 pF.

The SN74HCS74 can drive a load with total resistance described by  $R_L \geq V_O / I_O$ , with the output voltage and current defined in the *Electrical Characteristics* table with  $V_{OH}$  and  $V_{OL}$ . When outputting in the high state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the  $V_{CC}$  pin.

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and Cpd Calculation](#).

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

#### CAUTION

The maximum junction temperature,  $T_{J(max)}$  listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

#### 9.2.1.2 Input Considerations

Input signals must cross  $V_{t-(min)}$  to be considered a logic LOW, and  $V_{t+(max)}$  to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either  $V_{CC}$  or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the SN74HCS74, as specified in the *Electrical Characteristics*, and the desired input transition rate. A 10-k $\Omega$  resistor value is often used due to these factors.

The SN74HCS74 has no input signal transition rate requirements because it has Schmitt-trigger inputs.

Another benefit to having Schmitt-trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the  $\Delta V_{T(min)}$  in the *Electrical Characteristics*. This hysteresis value will provide the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than  $V_{CC}$  or ground is plotted in the *Typical Characteristics*.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

#### 9.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the  $V_{OH}$  specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the  $V_{OL}$  specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to  $V_{CC}$  or ground.

Refer to *Feature Description* section for additional information regarding the outputs for this device.

### 9.2.2 Detailed Design Procedure

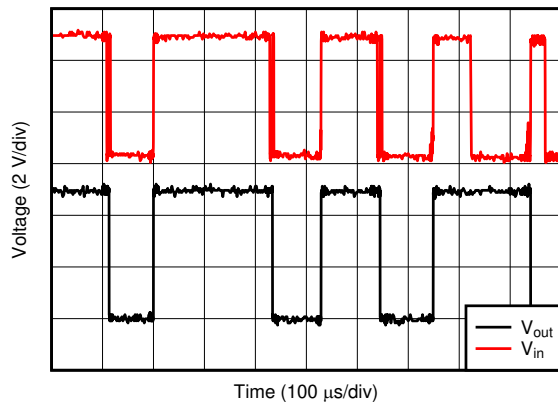
1. Add a decoupling capacitor from  $V_{CC}$  to GND. The capacitor needs to be placed physically close to the device and electrically close to both the  $V_{CC}$  and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is  $\leq 50$  pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74HCS74 to the receiving device(s).
3. Ensure the resistive load at the output is larger than  $(V_{CC} / I_{O(max)}) \Omega$ . This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in megaohms; much larger than the minimum calculated above.
4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#).

### 9.2.3 Application Curve


#### Circuit response without RC debounce

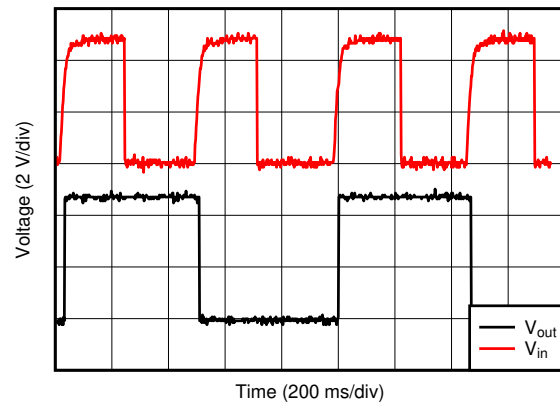
$V_{in} :=$  CLK input,  $V_{out} :=$  Q output illustrates an example of a single button press bouncing and causing the output to toggle multiple times. This will cause issues in the desired application. [Circuit response with RC debounce](#)

$V_{in} :=$  CLK input,  $V_{out} :=$  Q output illustrates 4 button presses with an added debounce circuit, fixing the unwanted toggling and allowing for proper toggle switch operation.



D001


**9-2. Circuit response without RC debounce**  
 $V_{in} :=$  CLK input,  $V_{out} :=$  Q output



D002


**9-3. Circuit response with RC debounce**  
 $V_{in} :=$  CLK input,  $V_{out} :=$  Q output

## 10 Power Supply Recommendations

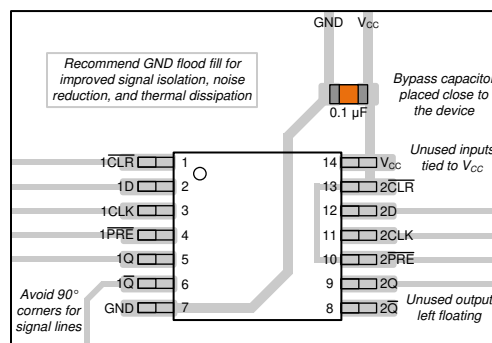
The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- $\mu\text{F}$  capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- $\mu\text{F}$  and 1- $\mu\text{F}$  capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in given example layout image.

## 11 Layout

### 11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

### 11.2 Layout Example



11-1. Layout Example of the SN74HCS74

## 12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [HCMOS Design Considerations application report \(SCLA007\)](#)
- Texas Instruments, [CMOS Power Consumption and  \$C\_{pd}\$  Calculation application report \(SDYA009\)](#)
- Texas Instruments, [Designing With Logic application report](#)

### 12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](#) のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 12.3 サポート・リソース

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### 12.4 Trademarks

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 12.6 用語集

[TI 用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74HCS74BQAR</a>	Active	Production	WQFN (BQA)   14	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	HCS74
SN74HCS74BQAR.A	Active	Production	WQFN (BQA)   14	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	HCS74
<a href="#">SN74HCS74DR</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	HCS74
SN74HCS74DR.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS74
<a href="#">SN74HCS74DYYR</a>	Active	Production	SOT-23-THIN (DYY)   14	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS74
SN74HCS74DYYR.A	Active	Production	SOT-23-THIN (DYY)   14	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS74
<a href="#">SN74HCS74PWR</a>	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	HCS74
SN74HCS74PWR.A	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS74

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74HCS74 :**

- Automotive : [SN74HCS74-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCS74BQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74HCS74DR	SOIC	D	14	2500	330.0	16.4	6.6	9.3	2.1	8.0	16.0	Q1
SN74HCS74DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HCS74DYYR	SOT-23-THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
SN74HCS74PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HCS74PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCS74BQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74HCS74DR	SOIC	D	14	2500	366.0	364.0	50.0
SN74HCS74DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74HCS74DYR	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8
SN74HCS74PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74HCS74PWR	TSSOP	PW	14	2000	356.0	356.0	35.0

D0014A



# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

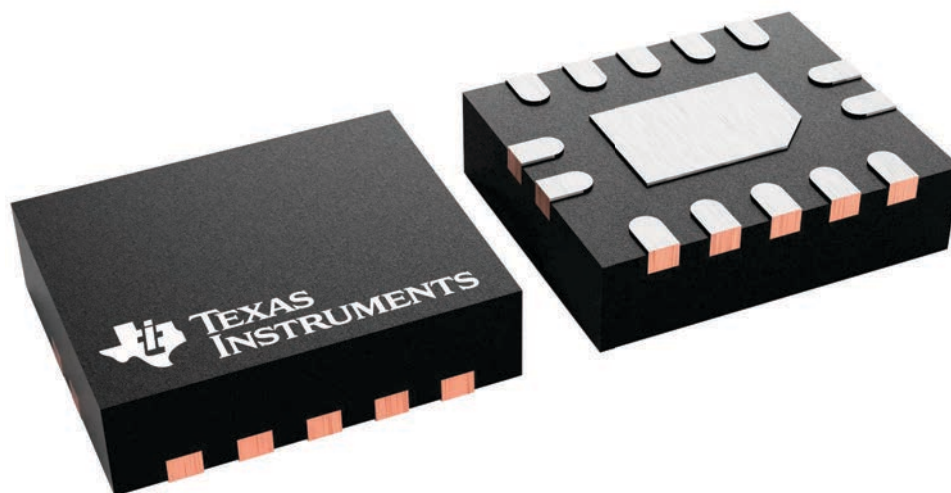
**BQA 14**

**WQFN - 0.8 mm max height**

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4227145/A



4224636/A 11/2018

**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

WQFN - 0.8 mm max height

BQA0014A

PLASTIC QUAD FLAT PACK-NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

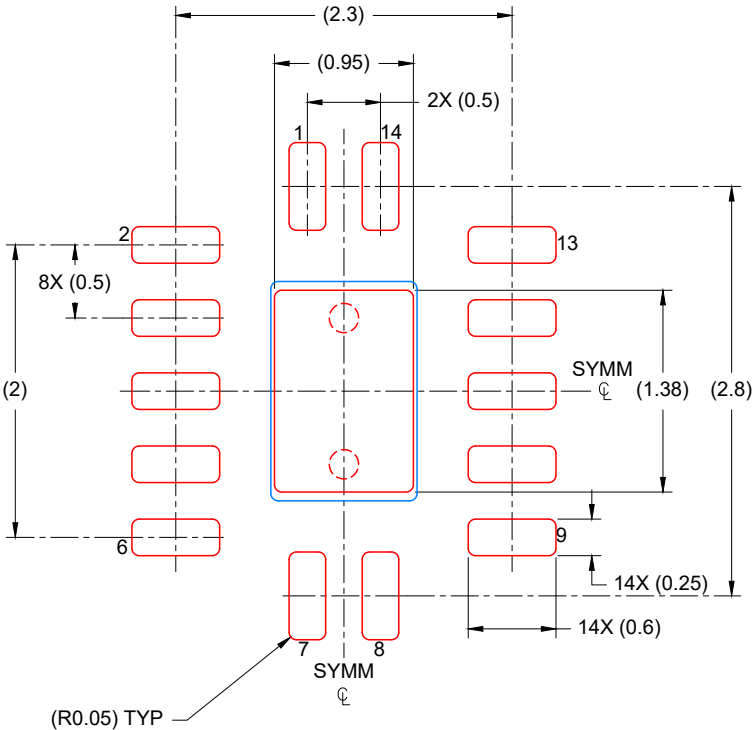
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

BQA0014A

WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



SOLDER PASTE EXAMPLE  
 BASED ON 0.125 mm THICK STENCIL

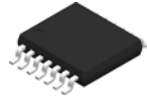
EXPOSED PAD  
 88% PRINTED COVERAGE BY AREA  
 SCALE: 20X

4224636/A 11/2018

NOTES: (continued)

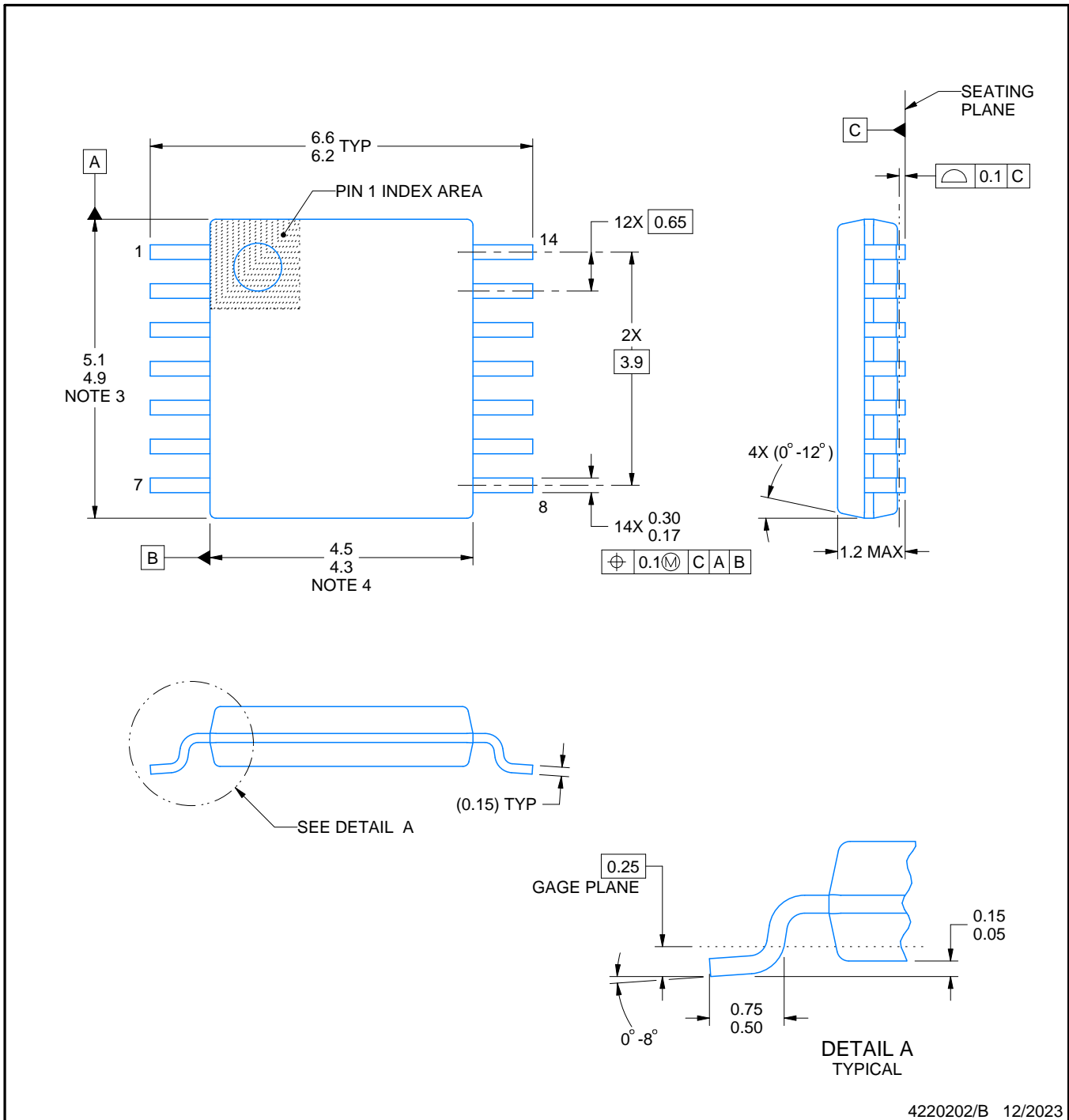
- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PW0014A



**PACKAGE OUTLINE**  
**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

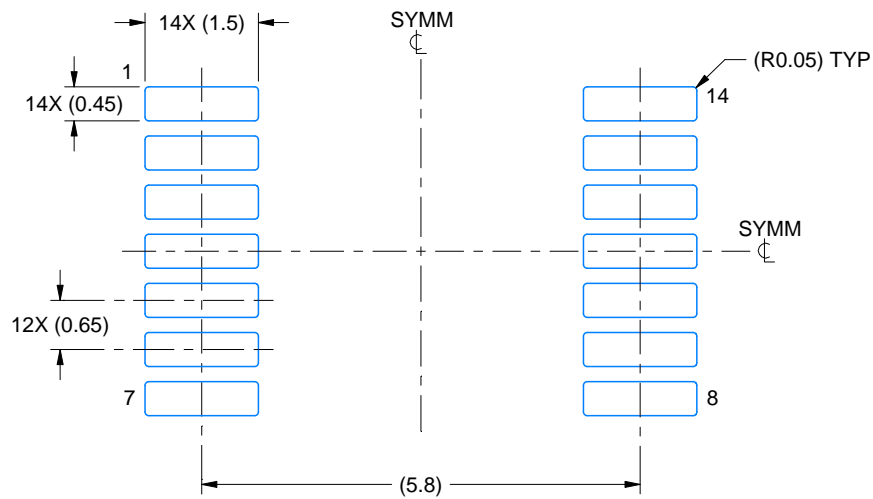
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

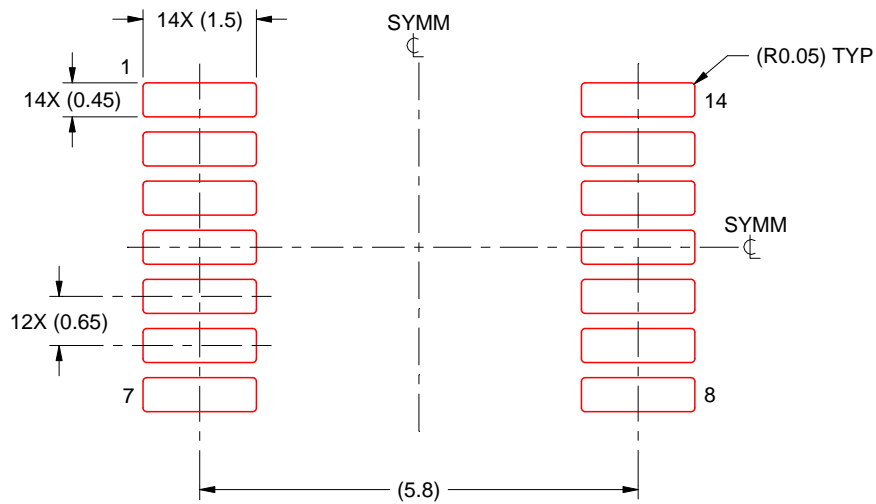
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

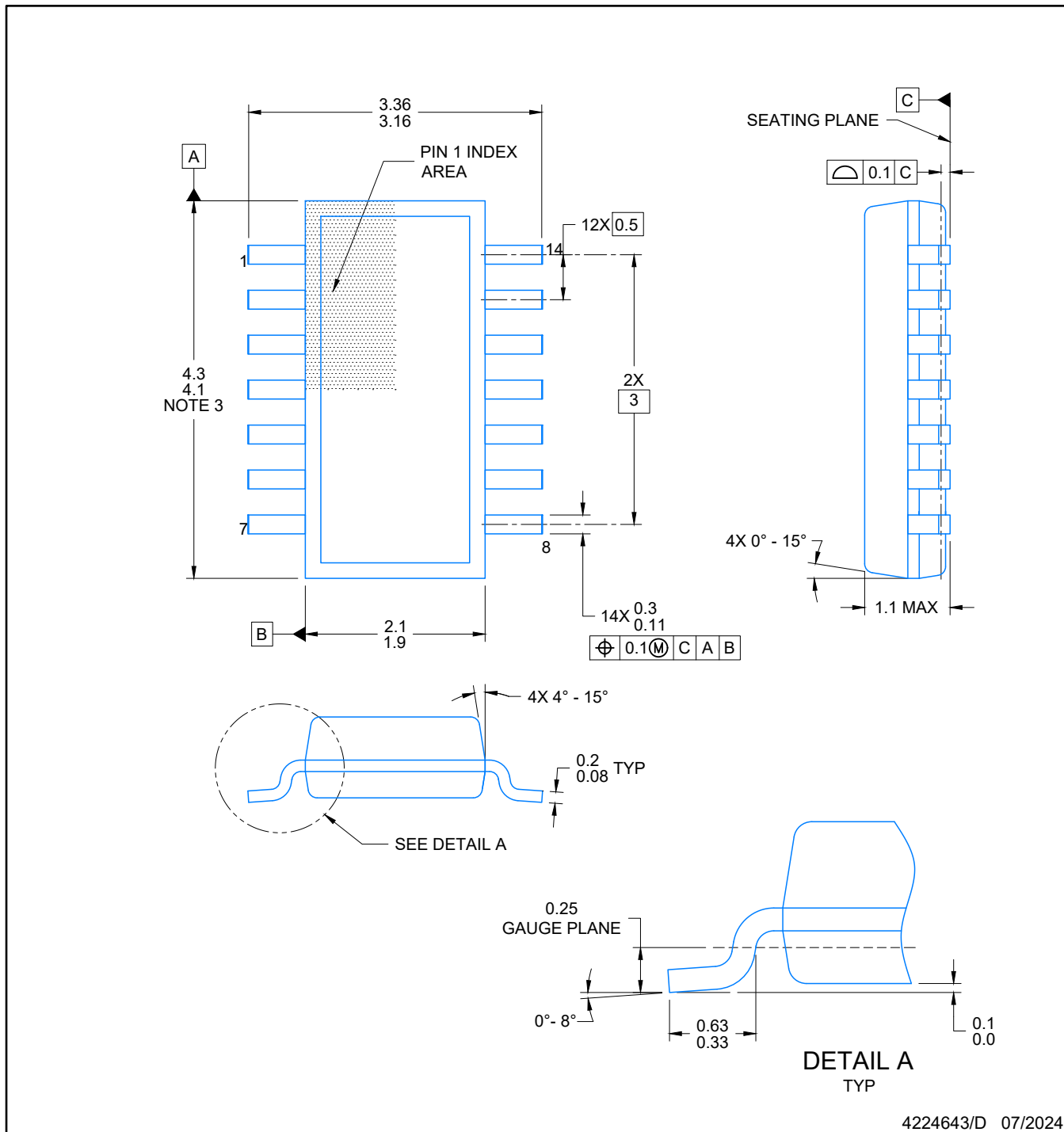


SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

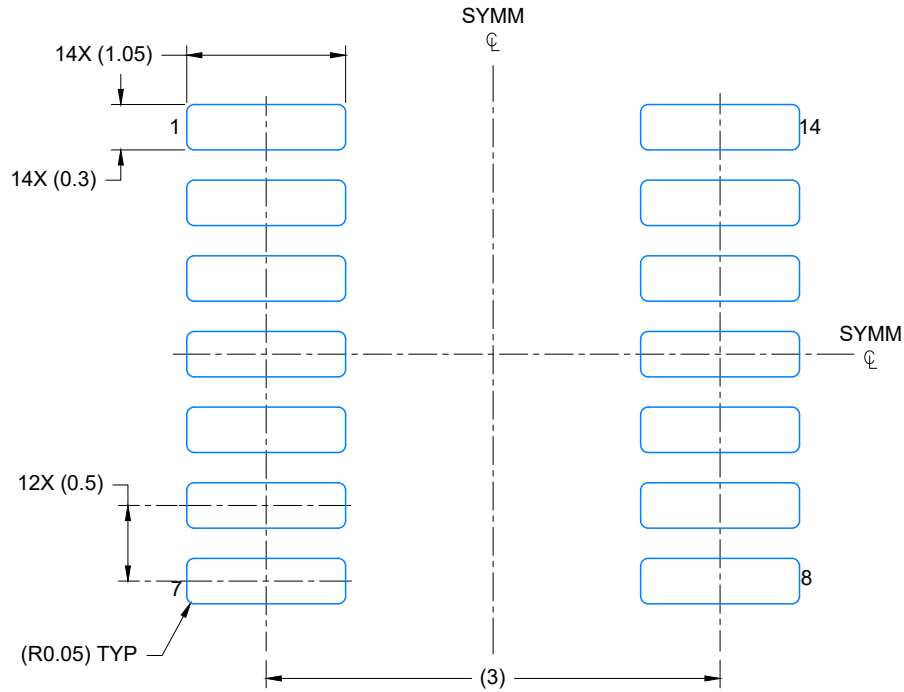
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



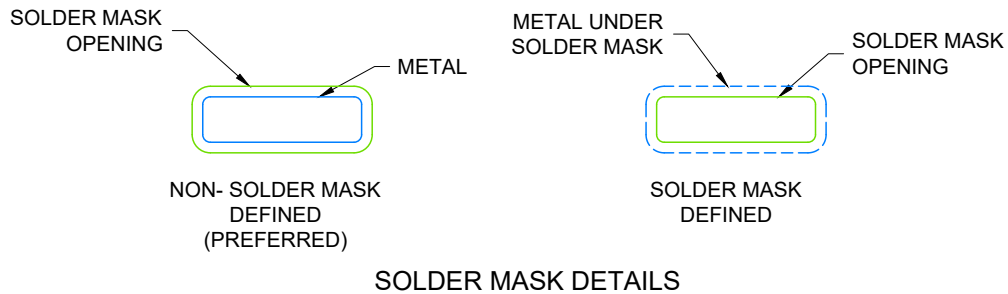
4224643/D 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



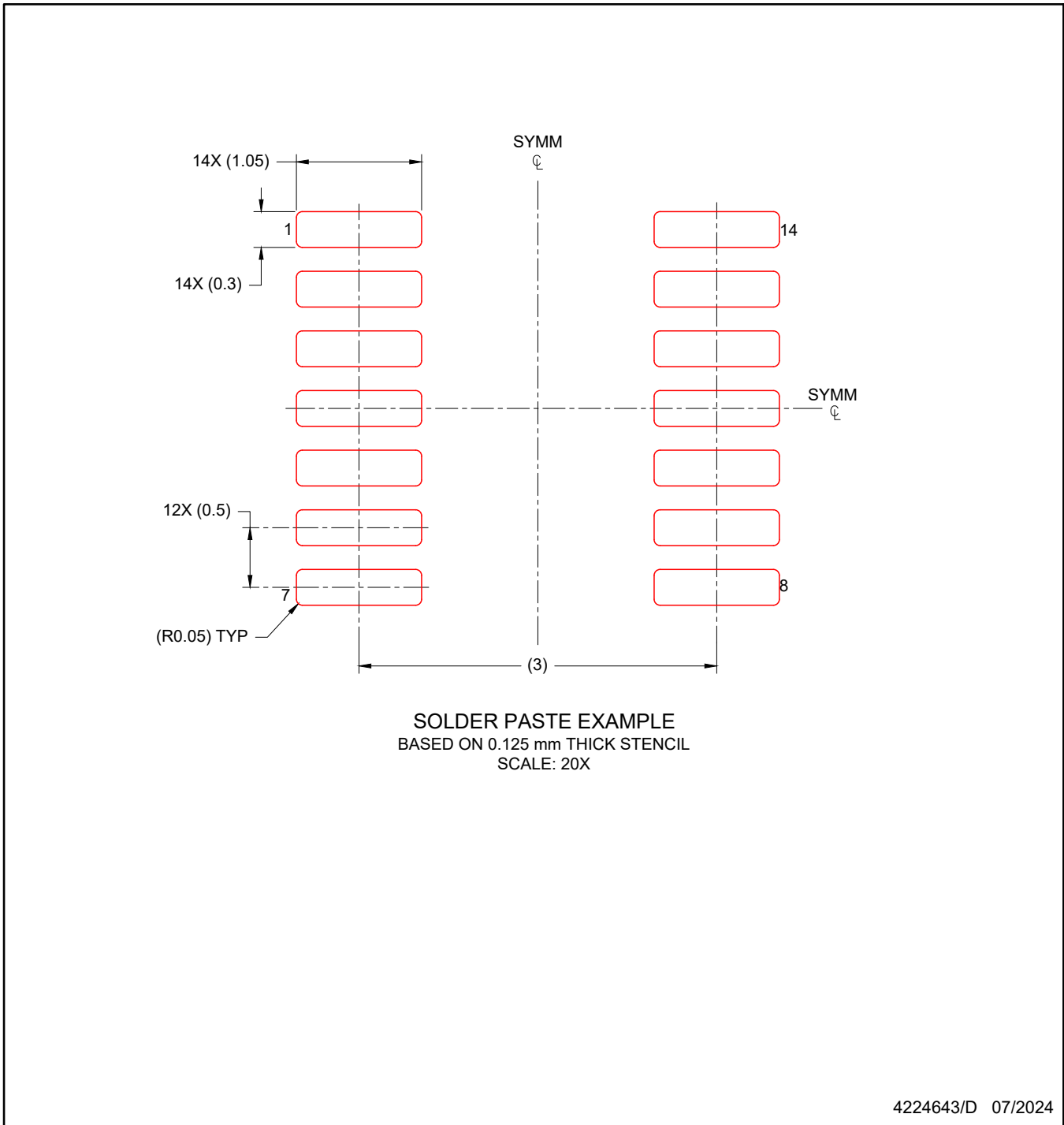
LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



4224643/D 07/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.

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