# SN74LV273A-Q1 クリア機能付きの車載用オクタル D タイプ・フリップ・フロップ

## 1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
  - デバイス温度グレード 1:
    - 40℃～+125℃、$T_A$
  - デバイス HBM ESD 分類レベル 2
  - デバイス CDM ESD 分類レベル C6
- ウェッタブル・フランク QFN (WRKS) パッケージで供給
- 2V～5.5V の $V_{CC}$ で動作
- 最大 $t_{pd}$ 10.5ns (5V 時)
- すべてのポートで混合モード電圧動作をサポート
- $I_{off}$ により部分的パワーダウン・モードでの動作をサポート
- JESD 17 準拠で 250mA 超のラッチアップ性能

## 2 アプリケーション

- デジタル信号のクロック同期
- 少ない入力による信号の監視
- スイッチからトグルへの変換

## 3 概要

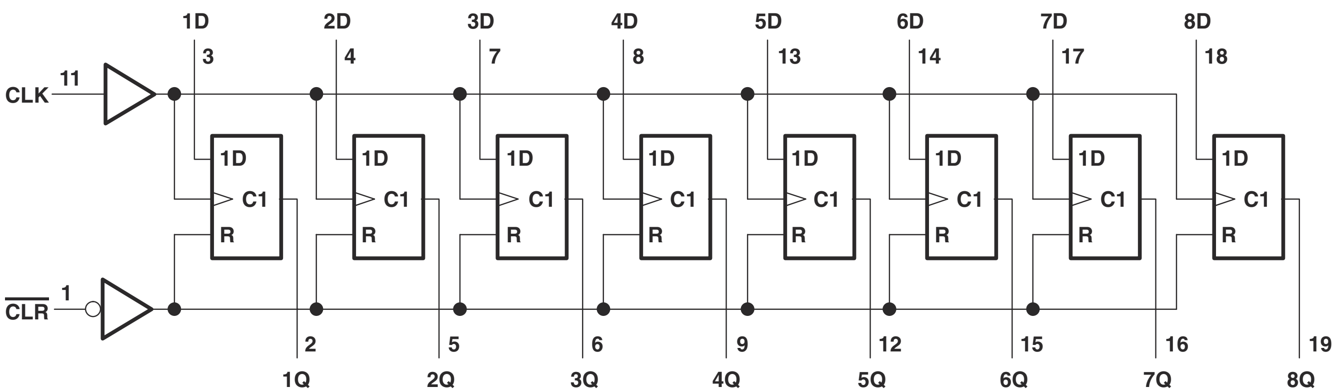
SN74LV273A-Q1 デバイスは、共有の直接アクティブ Low クリア ($\overline{CLR}$) 入力とクロック (CLK) を搭載した、オクタル・ポジティブ・エッジ・トリガの D タイプ・フリップ・フロップです。

セットアップ時間の要件を満たすデータ (D) 入力の情報は、クロック (CLK) パルスの立ち上がりエッジで (Q) 出力に転送されます。クロックのトリガは、特定の電圧レベルで発生し、立ち上がりパルスの遷移時間とは直接関係しません。CLK が High レベルまたは Low レベルのとき、または High レベルから Low レベルに遷移する途中のとき、D 入力は出力に影響を与えません。データ (Q) 出力の情報は、クリア ($\overline{CLR}$) ピンへの Low レベル入力によって非同期的にクリアできます。

**パッケージ情報** (1)

| 部品番号 | パッケージ | 本体サイズ (公称) |
|---|---|---|
| SN74LV273A-Q1 | WRKS (WQFN、20) | 4.50mm × 2.50mm |
| | DGS (VSSOP、20) | 5.10mm × 3.00mm |

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。




**論理図 (正論理)**

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## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| Changes from Revision A (October 2022) to Revision B (January 2023) | Page |
|---|---|
| • データシートに *DGS* パッケージ情報を追加 | 1 |

| Changes from Revision * (August 2022) to Revision A (October 2022) | Page |
|---|---|
| • データシートのステータスを「事前情報」から*「量産データ」に変更* | 1 |

## 5 Pin Configuration and Functions

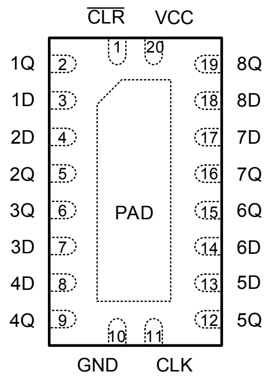



図 5-1. SN74LV273A-Q1 WRKS Package, 20-Pin WQFN (Top View)

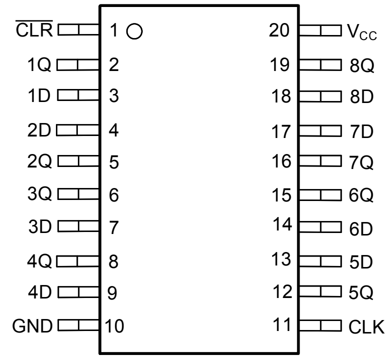



図 5-2. SN74LV273A-Q1 DGS Package, 20-Pin VSSOP (Top View)

表 5-1. Pin Functions

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| $\overline{CLR}$ | 1 | I | Clear for all channels, active low |
| 1Q | 2 | O | Output for channel 1 |
| 1D | 3 | I | Input for channel 1 |
| 2D | 4 | I | Input for channel 2 |
| 2Q | 5 | O | Output for channel 2 |
| 3Q | 6 | O | Output for channel 3 |
| 3D | 7 | I | Input for channel 3 |
| 4D | 8 | I | Input for channel 4 |
| 4Q | 9 | O | Output for channel 4 |
| GND | 10 | G | Ground |
| CLK | 11 | I | Clock for all channels, rising edge triggered |
| 5Q | 12 | O | Output for channel 5 |
| 5D | 13 | I | Input for channel 5 |
| 6D | 14 | I | Input for channel 6 |
| 6Q | 15 | O | Output for channel 6 |
| 7Q | 16 | O | Output for channel 7 |
| 7D | 17 | I | Input for channel 7 |
| 8D | 18 | I | Input for channel 8 |
| 8Q | 19 | O | Output for channel 8 |
| $V_{CC}$ | 20 | P | Positive supply |
| Thermal pad | | — | Thermal Pad(2) |

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.
(2) WRKS Package Only

# 6 Specifications

## 6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)[(1)]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | –0.5 | 7 | V |
| $V_I$ | Input voltage[(2)] | | –0.5 | 7 | V |
| $V_O$ | Voltage range applied to any output in the high-impedance or power-off state[(2)] | | –0.5 | 7 | V |
| $V_O$ | Output voltage [(2)] [(3)] | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I < 0$ | | –20 | mA |
| $I_{OK}$ | Output clamp current | $V_O < 0$ | | –50 | mA |
| $I_O$ | Continuous output current | $V_O$ = 0 to $V_{CC}$ | | ±25 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±50 | mA |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 5.5 V maximum.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2[(1)] | ±4000 | V |
| | | Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B | ±2000 | |

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[(1)]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | V |
| | | $V_{CC}$ = 2.3 V to 5.5 V | $V_{CC}$ × 0.7 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | V |
| | | $V_{CC}$ = 2.3 V to 5.5 V | | $V_{CC}$ × 0.3 | |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | μA |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | –2 | mA |
| | | $V_{CC}$ = 3 V to 3.6 V | | –6 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | –12 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | μA |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 2 | mA |
| | | $V_{CC}$ = 3 V to 3.6 V | | 6 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 12 | |
| Δt/Δv | Input transition rise or fall rate | $V_{CC}$ = 2.3 V to 2.7 V | | 200 | ns/V |
| | | $V_{CC}$ = 3 V to 3.6 V | | 100 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 20 | |
| $T_A$ | Operating free-air temperature | | –40 | 125 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs.*

### 6.4 Thermal Information

| THERMAL METRIC[(1)] | | SN74LV273A-Q1 | | UNIT |
|---|---|---|---|---|
| | | WRKS (WQFN) | DGS (VSSOP) | |
| | | 20 PINS | 20 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 75.8 | 125.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 80.3 | 80.0 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 50.5 | 63.8 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 16.0 | 8.4 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 50.4 | 79.9 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 32.3 | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics.*

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted).

| PARAMETER | | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High level output voltage | $I_{OH}$ = –50 mA | 2 V to 5.5 V | $V_{CC}$ – 0.1 | | | V |
| | | $I_{OH}$ = –2 mA | 2.3 V | 2 | | | |
| | | $I_{OH}$ = –6 mA | 3 V | 2.48 | | | |
| | | $I_{OH}$ = –12 mA | 4.5 V | 3.8 | | | |
| $V_{OL}$ | Low level output voltage | $I_{OL}$ = 50 mA | 2 V to 5.5 V | | | 0.1 | V |
| | | $I_{OL}$ = 2 mA | 2.3 V | | | 0.4 | |
| | | $I_{OL}$ = 6 mA | 3 V | | | 0.44 | |
| | | $I_{OL}$ = 12 mA | 4.5 V | | | 0.55 | |
| $I_I$ | Input leakage current | $V_I$ = 5.5 V or GND | 0 V to 5.5 V | | | ±1 | μA |
| $I_{CC}$ | Supply current | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 20 | μA |
| $I_{off}$ | Input/Output Power-Off Leakage Current | $V_I$ or $V_O$ = 0 to 5.5 V | 0 V | | | 5 | μA |
| $C_i$ | Input Capacitance | $V_I$ = $V_{CC}$ or GND | 3.3 V | | 2 | | pF |

## 6.6 Timing Requirements, $V_{CC}$ = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted) (see 図 7-1)

| PARAMETER | | TEST CONDITION | 25°C | | –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | $\overline{CLR}$ low | 6.5 | | 7.5 | | ns |
| | | CLK high or low | 7 | | 9 | | |
| $t_{su}$ | Setup time | Data before CLK↑ | 8.5 | | 12 | | ns |
| | | $\overline{CLR}$ inactive before CLK↑ | 4 | | 4.5 | | |
| $t_h$ | Hold time | Data after CLK↑ | 0.5 | | 2.5 | | ns |

## 6.7 Timing Requirements, $V_{CC}$ = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see 図 7-1)

| PARAMETER | | TEST CONDITION | 25°C | | –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | $\overline{CLR}$ low | 5 | | 6.5 | | ns |
| | | CLK high or low | 5 | | 7 | | |
| $t_{su}$ | Setup time | Data before CLK↑ | 5.5 | | 8 | | ns |
| | | $\overline{CLR}$ inactive before CLK↑ 2.5 | 2.5 | | 3 | | |
| $t_h$ | Hold time | Data after CLK↑ | 1 | | 2.5 | | ns |

## 6.8 Timing Requirements, $V_{CC}$ = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see 図 7-1)

| PARAMETER | | TEST CONDITION | 25°C | | –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | $\overline{CLR}$ low | 5 | | 5.5 | | ns |
| | | CLK high or low | 5 | | 5.5 | | |
| $t_{su}$ | Setup time | Data before CLK↑ | 4.5 | | 6 | | ns |
| | | $\overline{CLR}$ inactive before CLK↑ | 2 | | 2.5 | | |
| $t_h$ | Hold time | Data after CLK↑ | 1 | | 2 | | ns |

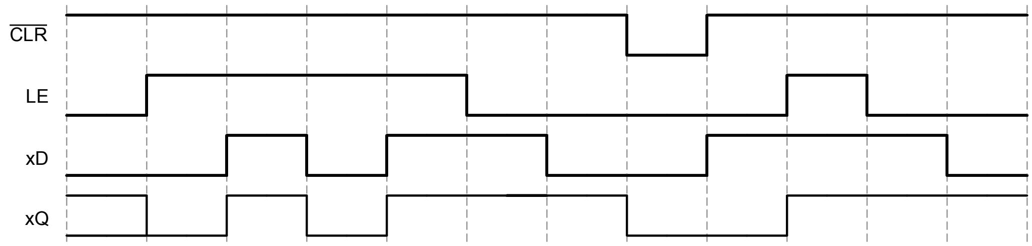



図 6-1. Typical Clock, Load, and Clear Sequences

## 6.9 Switching Characteristics, $V_{CC}$ = 2.5 V ± 0.2 V

over operating free-air temperature range (unless otherwise noted), (see 図 7-1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAP | 25°C MIN | 25°C TYP | 25°C MAX | –40°C to 125°C MIN | –40°C to 125°C TYP | –40°C to 125°C MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | | | $C_L$ = 15 pF | 55 | 95 | | 45 | | | MHz |
| | | | $C_L$ = 50 pF | 45 | 75 | | 40 | | | |
| $t_{pd}$ | CLK | Q | $C_L$ = 15 pF | | 10.4 | 18.3 | 1 | | 22.5 | ns |
| | $\overline{CLR}$ | | | | 10.3 | 19 | 1 | | 23 | |
| $t_{pd}$ | CLK | Q | $C_L$ = 50 pF | | 12.9 | 22.1 | 1 | | 27 | ns |
| | $\overline{CLR}$ | | | | 13.1 | 22.8 | 1 | | 27.5 | |
| $t_{sk(o)}$ | | | | | | 2 | | | 2 | |

## 6.10 Switching Characteristics, $V_{CC}$ = 3.3 V ± 0.3 V

over operating free-air temperature range (unless otherwise noted), (see 図 7-1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAP | 25°C MIN | 25°C TYP | 25°C MAX | –40°C to 125°C MIN | –40°C to 125°C TYP | –40°C to 125°C MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | | | $C_L$ = 15 pF | 75 | 140 | | 65 | | | MHz |
| | | | $C_L$ = 50 pF | 50 | 110 | | 45 | | | |
| $t_{pd}$ | CLK | Q | $C_L$ = 15 pF | | 7.1 | 13.6 | 1 | | 17.5 | ns |
| | $\overline{CLR}$ | | | | 6.9 | 13.6 | 1 | | 17.5 | |
| $t_{pd}$ | CLK | Q | $C_L$ = 50 pF | | 9.1 | 17.1 | 1 | | 21 | ns |
| | $\overline{CLR}$ | | | | 8.7 | 17.1 | 1 | | 21 | |
| $t_{sk(o)}$ | | | | | | 1.5 | | | 1.5 | |

## 6.11 Switching Characteristics, $V_{CC}$ = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted), (see 図 7-1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAP | 25°C MIN | 25°C TYP | 25°C MAX | –40°C to 125°C MIN | –40°C to 125°C TYP | –40°C to 125°C MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | | | $C_L$ = 15 pF | 120 | 205 | | 100 | | | MHz |
| | | | $C_L$ = 50 pF | 80 | 160 | | 70 | | | |
| $t_{pd}$ | CLK | Q | $C_L$ = 15 pF | | 4.8 | 9 | 1 | | 11.5 | ns |
| | $\overline{CLR}$ | | | | 4.7 | 8.5 | 1 | | 11 | |
| $t_{pd}$ | CLK | Q | $C_L$ = 50 pF | | 6.2 | 11 | 1 | | 14 | ns |
| | $\overline{CLR}$ | | | | 6 | 10.5 | 1 | | 13.5 | |
| $t_{sk(o)}$ | | | | | | 1 | | | 1 | |

## 6.12 Operating Characteristics

$T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | TYP | UNIT |
|---|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | $C_L$ = 50 pF | f = 10 MHz | 3.3 V | 15.9 | pF |
| | | | | 5 V | 17.1 | |

## 6.13 Noise Characteristics

$V_{CC}$ = 3.3 V, $C_L$ = 50 pF, $T_A$ = 25°C

| PARAMETER(1) | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.3 | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.3 | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 3 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2.31 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.99 | V |

(1) Characteristics for surface-mount packages only.

## 6.14 Typical Characteristics

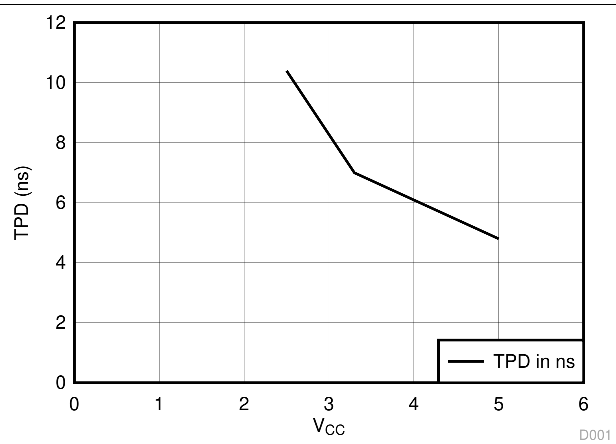



図 6-2. $T_{PD}$ vs $V_{cc}$ at 25°C

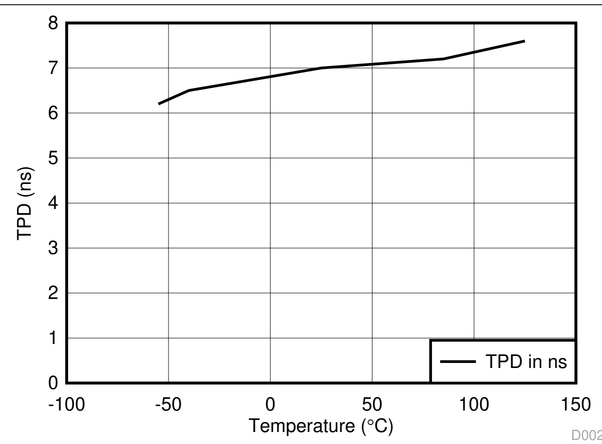
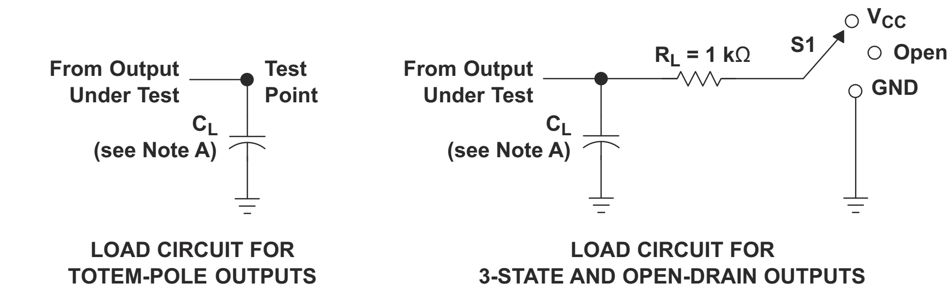
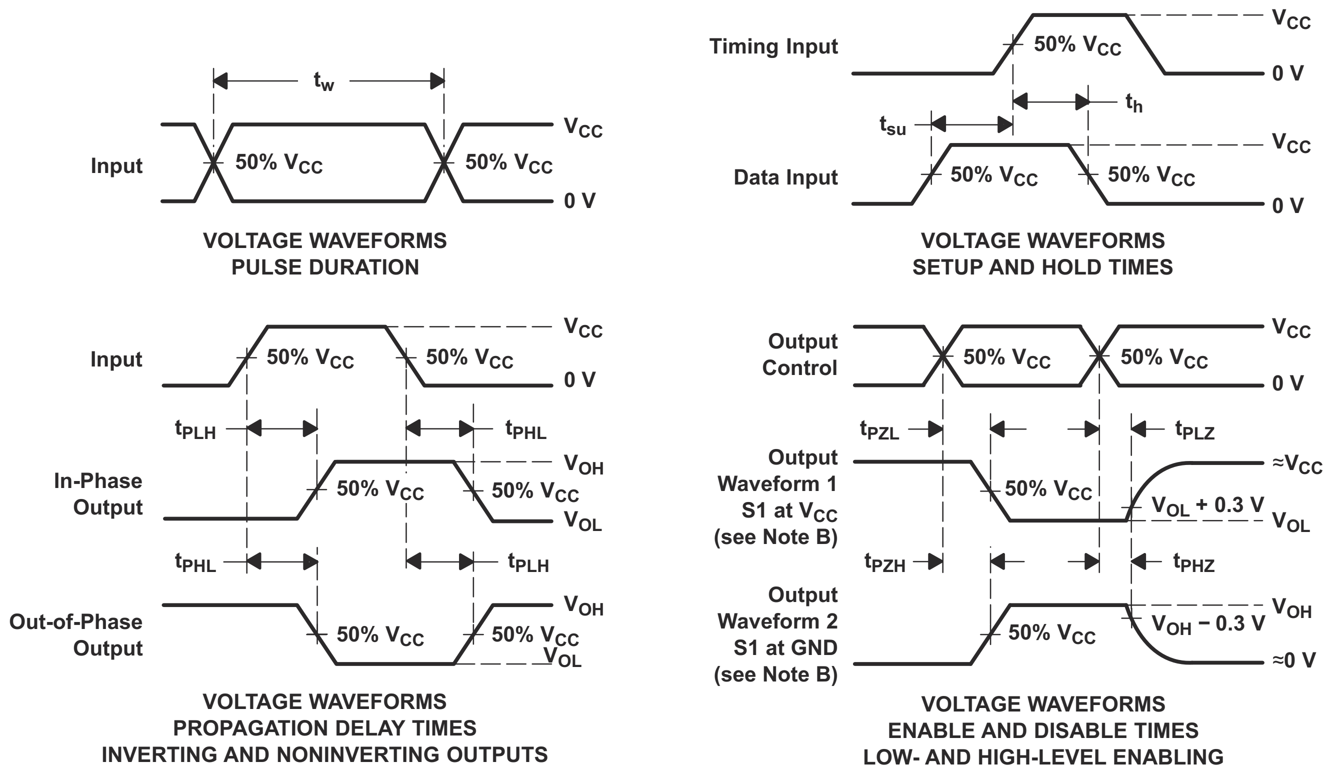



図 6-3. $T_{PD}$ vs Temperature

# 7 Parameter Measurement Information




| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |
| Open Drain | $V_{CC}$ |




A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 3 ns, and $t_f$ ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PHL}$ and $t_{PLH}$ are the same as $t_{pd}$.
H. All parameters and waveforms are not applicable to all devices.

**図 7-1. Load Circuit and Voltage Waveforms**

# 8 Detailed Description

## 8.1 Overview

The SN74LV273A-Q1 device is an octal positive-edge triggered D-type flip-flop with shared direct active low clear ($\overline{CLR}$) input and clock (CLK).

Information at the data (D) inputs meeting the setup time requirements is transferred to the (Q) outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not related directly to the transition time of the positive-going pulse. When CLK is at either the high or low level or transitioning from a high level to a low level, the D input has no effect at the output. Information at the data (Q) outputs can be asynchronously cleared with a low level input through the clear ($\overline{CLR}$) pin.

The SN74LV273A-Q1 is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

## 8.2 Functional Block Diagram

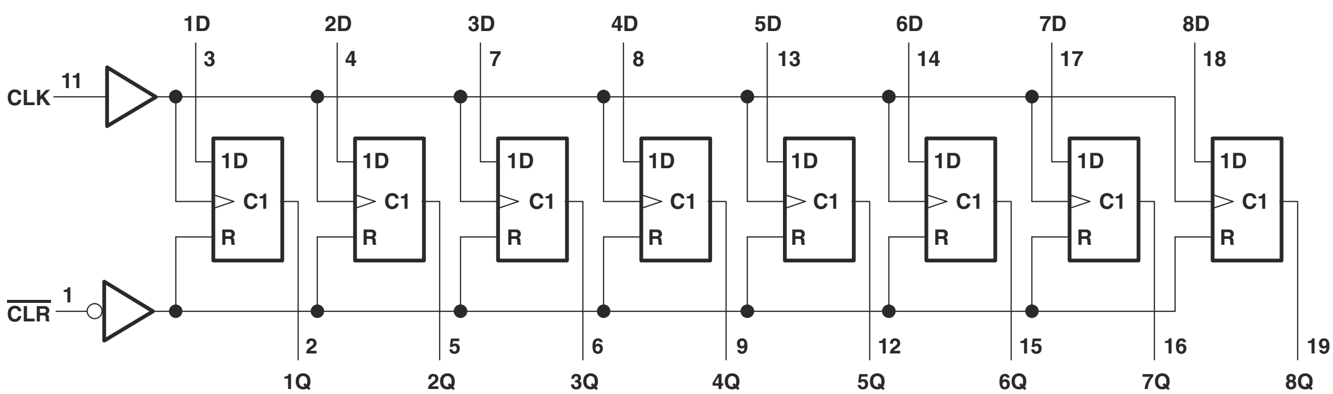



**図 8-1. Logic Diagram (Positive Logic)**

## 8.3 Feature Description

### 8.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs should be left disconnected.

### 8.3.2 Latching Logic

This device includes latching logic circuitry. Latching circuits commonly include D-type latches and D-type flip-flops, but include all logic circuits that act as volatile memory.

When the device is powered on, the state of each latch is unknown. There is no default state for each latch at start-up.

The output state of each latching logic circuit only remains stable as long as power is applied to the device within the supply voltage range specified in the *Recommended Operating Conditions* table.

### 8.3.3 Partial Power Down ($I_{off}$)

This device includes circuitry to disable all outputs when the supply pin is held at 0 V. When disabled, the outputs will neither source nor sink current, regardless of the input voltages applied. The amount of leakage current at each output is defined by the $I_{off}$ specification in the *Electrical Characteristics* table.

### 8.3.4 Wettable Flanks

This device includes wettable flanks for at least one package. See the *Features* section on the front page of the data sheet for which packages include this feature.

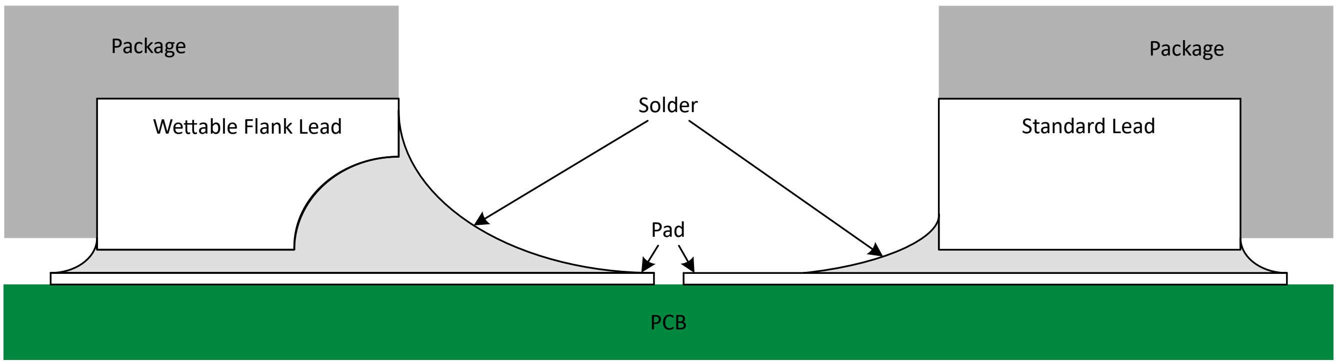



**図 8-2. Simplified Cutaway View of Wettable-Flank QFN Package and Standard QFN Package After Soldering**

Wettable flanks help improve side wetting after soldering, which makes QFN packages easier to inspect with automatic optical inspection (AOI). As shown in 図 8-2, a wettable flank can be dimpled or step-cut to provide additional surface area for solder adhesion which assists in reliably creating a side fillet. Please see the mechanical drawing for additional details.

### 8.3.5 Clamp Diode Structure

図 8-3 shows the inputs and outputs to this device have negative clamping diodes only.

> 注意
> Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

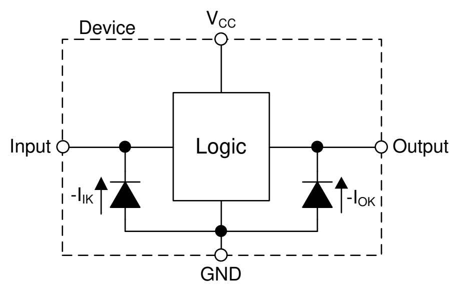



**図 8-3. Electrical Placement of Clamping Diodes for Each Input and Output**

## 8.4 Device Functional Modes

**表 8-1. Function Table**

| INPUTS(1) | | | OUTPUT(2) |
|---|---|---|---|
| $\overline{CLR}$ | CLK | D | Q |
| L | X | X | L |
| H | L, H, ↓ | X | $Q_0$ |
| H | ↑ | L | L |
| H | ↑ | H | H |

(1) L = input low, H = input high, ↑ = input transitioning from low to high, ↓ = input transitioning from high to low, X = do not care
(2) L = output low, H = output high, $Q_0$ = previous state

# 9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 9.1 Application Information

In this application, the SN74LV273A-Q1 is used to synchronize incoming data to the system clock on an 8-bit bus.

## 9.2 Typical Application

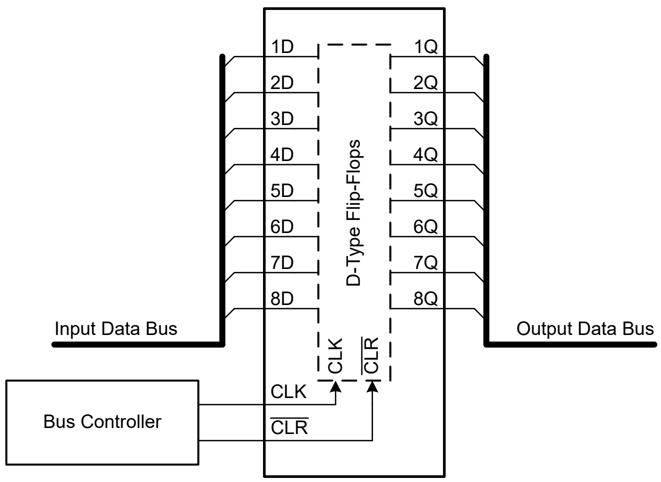



**図 9-1. Typical Application Diagram**

### 9.2.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LV273A-Q1 plus the maximum static supply current, $I_{CC}$, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Be sure to not exceed the maximum total current through $V_{CC}$ listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LV273A-Q1 plus the maximum supply current, $I_{CC}$, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Be sure to not exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74LV273A-Q1 can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50 pF.

The SN74LV273A-Q1 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with $V_{OH}$ and $V_{OL}$. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the $V_{CC}$ pin.

Total power consumption can be calculated using the information provided in *CMOS Power Consumption and Cpd Calculation*.

Thermal increase can be calculated using the information provided in *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices*.

> 注意
> The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

#### 9.2.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either $V_{CC}$ or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LV273A-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10-kΩ resistor value is often used due to these factors.

The SN74LV273A-Q1 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

#### 9.2.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the $V_{OH}$ specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the $V_{OL}$ specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to $V_{CC}$ or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

### 9.2.4 Detailed Design Procedure

1. Add a decoupling capacitor from $V_{CC}$ to GND. The capacitor needs to be placed physically close to the device and electrically close to both the $V_{CC}$ and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50 pF. This is not a hard limit; it will, however, ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74LV273A-Q1 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than ($V_{CC}$ / $I_{O(max)}$) Ω. This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*.

### 9.2.5 Application Curves

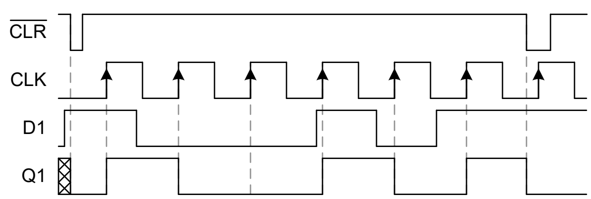



**図 9-2. Application Timing Diagram**

## 9.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Absolute Maximum Ratings* section. Each $V_{CC}$ terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1-μF capacitor; if there are multiple $V_{CC}$ terminals, then TI recommends a 0.01-μF or 0.022-μF capacitor for each power terminal. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. Frequencies of 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor must be installed as close as possible to the power terminal for best results.

## 9.4 Layout

### 9.4.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or $V_{CC}$, whichever makes more sense for the logic function or is more convenient.

### 9.4.2 Layout Example

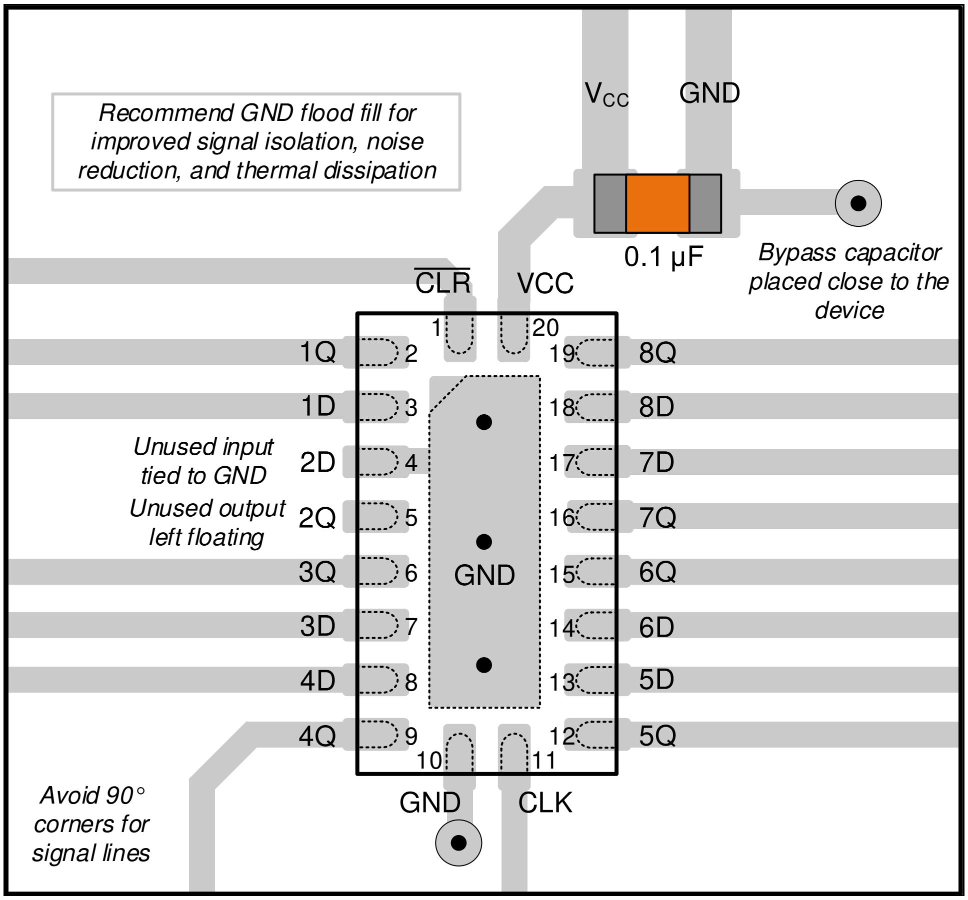



**図 9-3. Layout Example for the SN74LV273A-Q1 in the WRKS Package**

# 10 Device and Documentation Support

## 10.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Power-Up Behavior of Clocked Devices* application note
- Texas Instruments, *Introduction to Logic* application note

## 10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com. In the upper right-hand corner, click the *Alert me* button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

## 10.3 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

## 10.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

# 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SN74LV273AQDGSRQ1 | Active | Production | VSSOP (DGS) \| 20 | 5000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | L273Q |
| SN74LV273AQDGSRQ1.A | Active | Production | VSSOP (DGS) \| 20 | 5000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | L273Q |
| SN74LV273AQWRKSRQ1 | Active | Production | VQFN (RKS) \| 20 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV273AQ |
| SN74LV273AQWRKSRQ1.A | Active | Production | VQFN (RKS) \| 20 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV273AQ |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74LV273A-Q1 :**

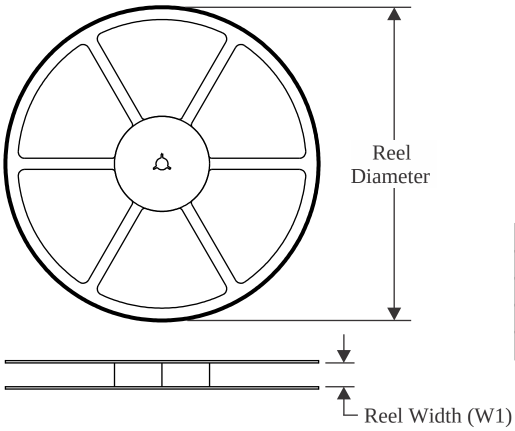
- Catalog : SN74LV273A

NOTE: Qualified Version Definitions:

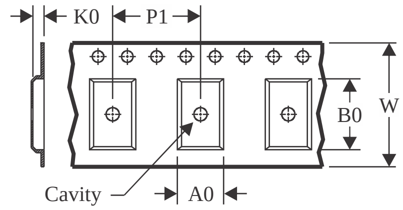
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

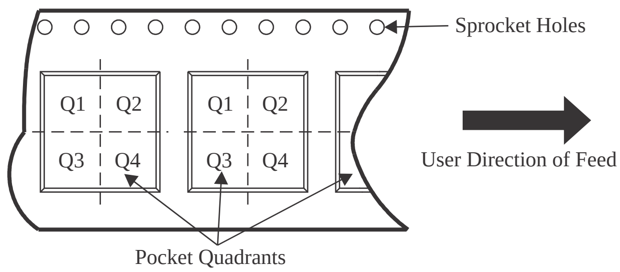



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

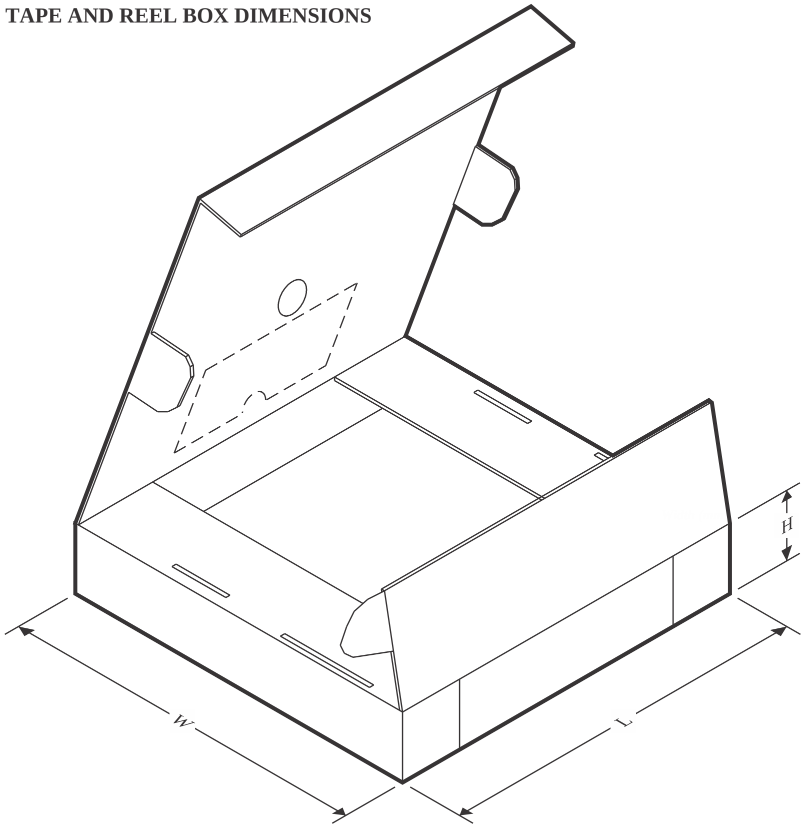
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

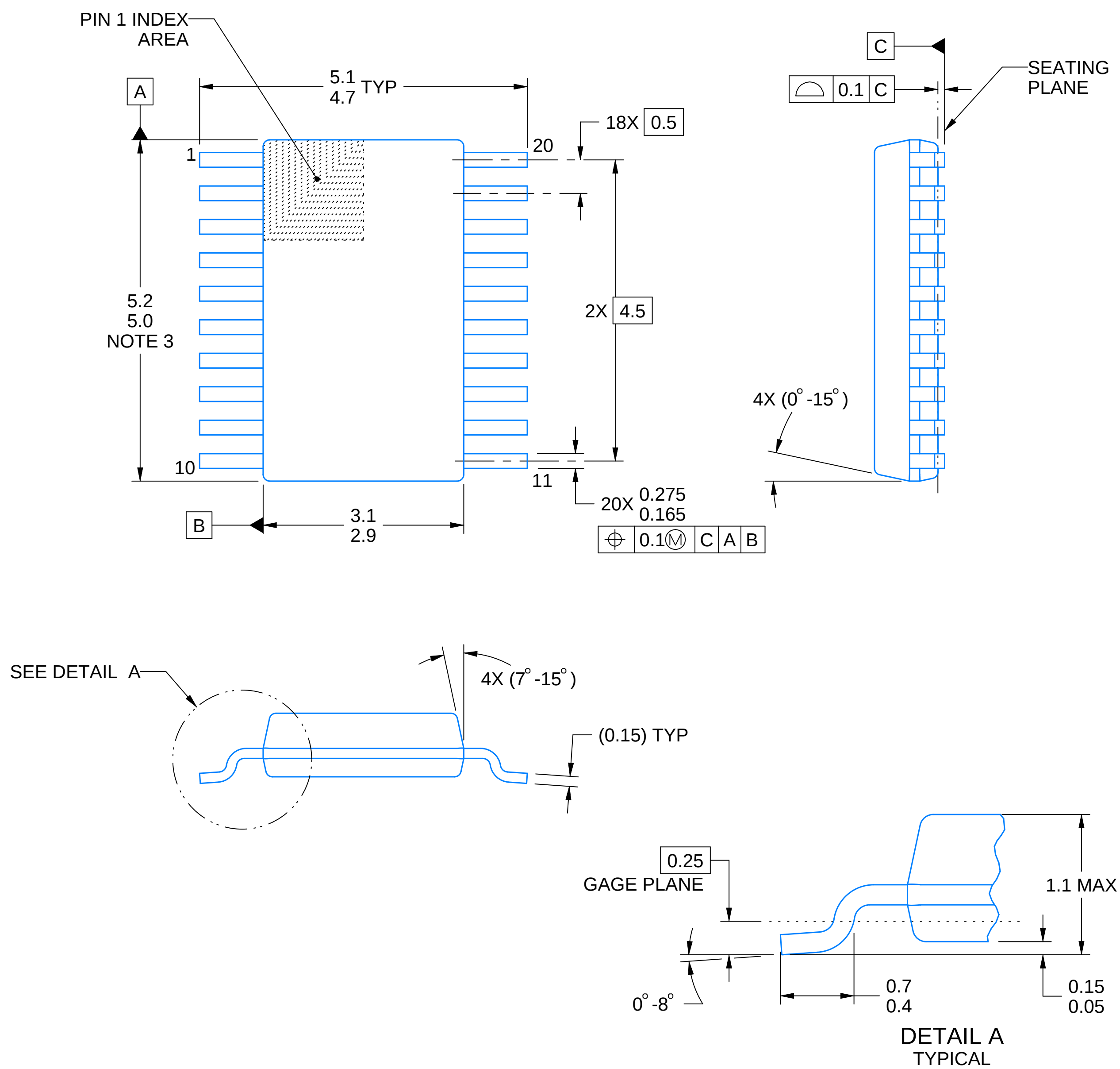
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LV273AQDGSRQ1 | VSSOP | DGS | 20 | 5000 | 330.0 | 16.4 | 5.4 | 5.4 | 1.45 | 8.0 | 16.0 | Q1 |
| SN74LV273AQWRKSRQ1 | VQFN | RKS | 20 | 3000 | 180.0 | 12.4 | 2.8 | 4.8 | 1.2 | 4.0 | 12.0 | Q1 |

## TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LV273AQDGSRQ1 | VSSOP | DGS | 20 | 5000 | 353.0 | 353.0 | 32.0 |
| SN74LV273AQWRKSRQ1 | VQFN | RKS | 20 | 3000 | 210.0 | 185.0 | 35.0 |

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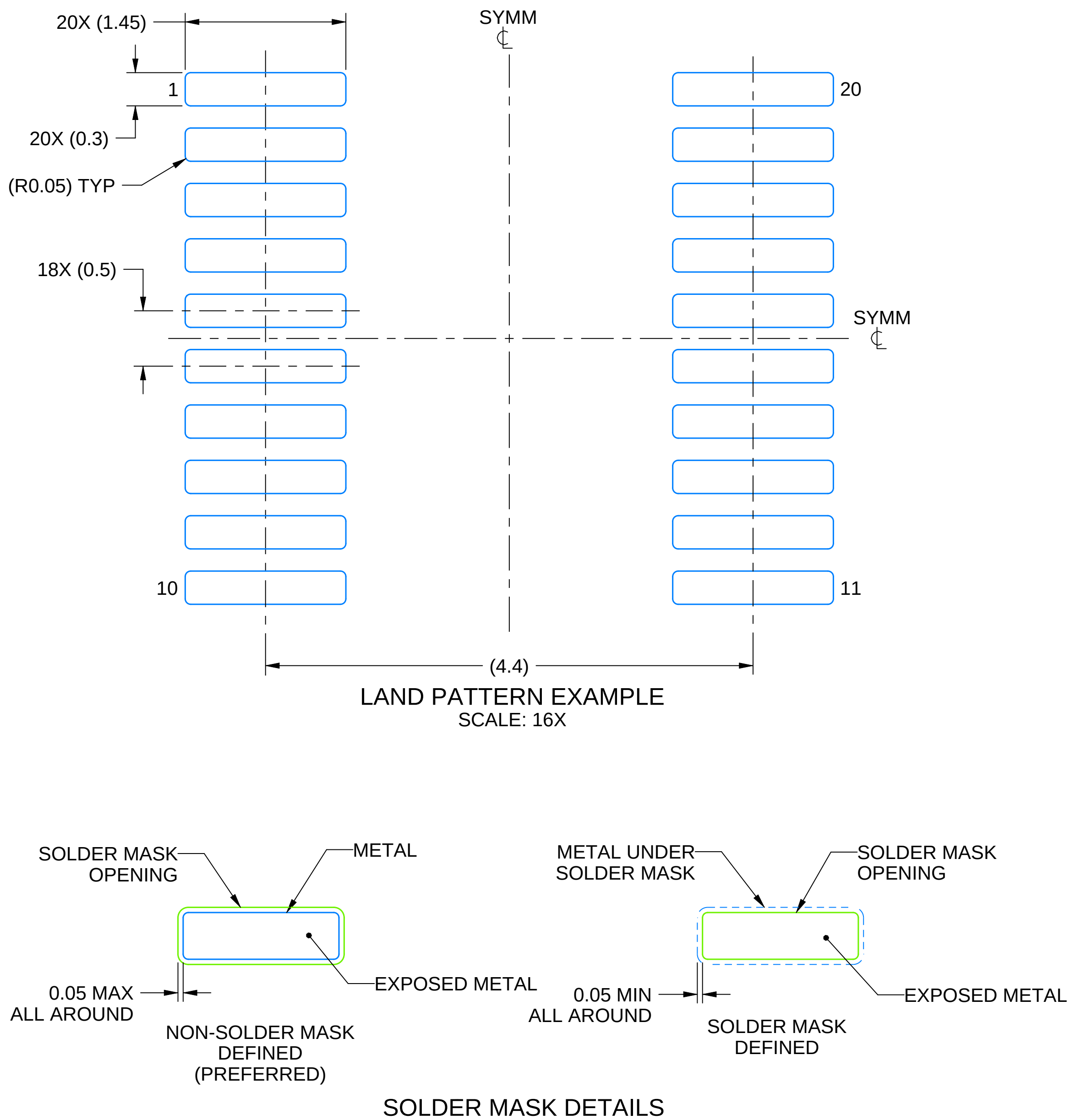
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.

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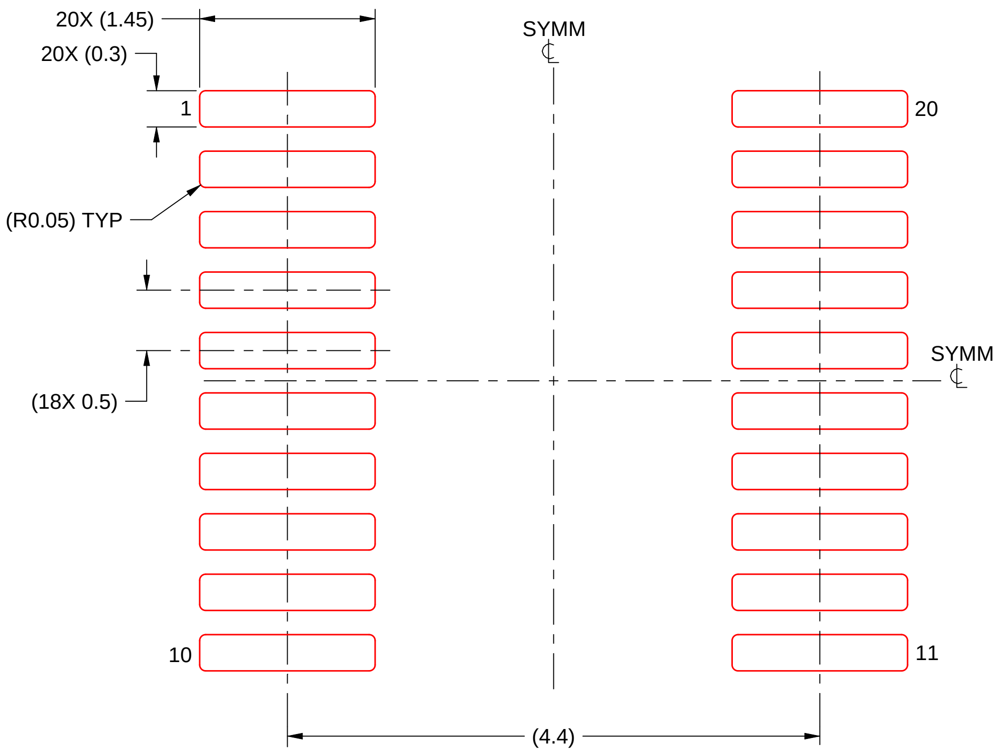
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 16X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

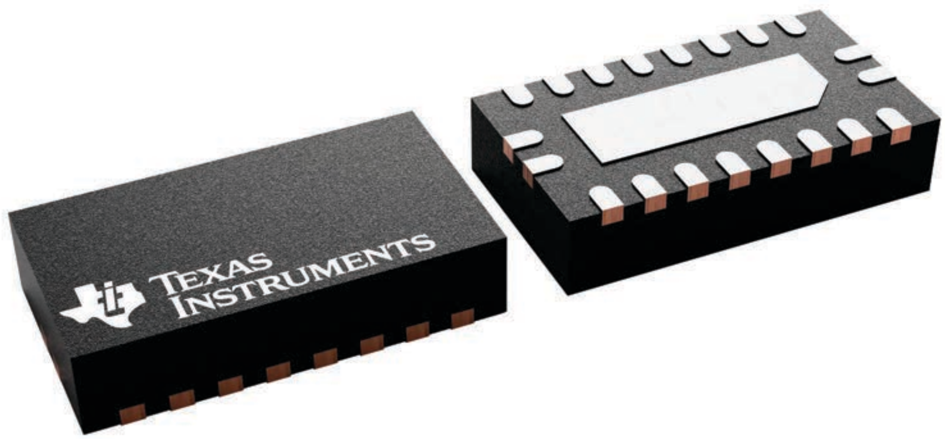
## RKS 20

**VQFN - 1 mm max height**

**2.5 x 4.5, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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最終更新日：2025 年 10 月