SN74LV4T125 単電源 4 バッファ・トランスレータ・ゲート、3 ステート出力 CMOS ロジック・レベル・シフタ付き

1 特長

- 5.0V、3.3V、2.5V、1.8V V_{CC} の単一電源電圧レベル・シフタ
- 動作範囲:1.8V～5.5V
- 昇圧変換
  - 1.8V V_{CC} で 1.2V(1) から 1.8V
  - 2.5V V_{CC} で 1.5V(1) から 2.5V
  - 3.3V V_{CC} で 1.8V(1) から 3.3V
  - 5.0V V_{CC} で 3.3V から 5.0V
- 降圧変換
  - 1.8V V_{CC} で 3.3V から 1.8V
  - 2.5V V_{CC} で 3.3V から 2.5V
  - 3.3V V_{CC} で 5.0V から 3.3V
- ロジック出力は V_{CC} を基準とする
- 3.3V V_{CC} で最大 50MHz での動作が規定
- 入力ピンの許容電圧:5.5V
- 動作温度範囲:-40℃～125℃
- 提供している鉛フリー・パッケージ:SC-70 (RGY)
  - 3.5 × 3.5 × 1 mm
- JESD 17 準拠で 250mA 超のラッチアップ性能
- 標準ロジック・ピン配置をサポート
- I_{off} により部分的パワーダウン・モードでの動作をサポート
- CMOS 出力 B は AUP125 および LVC125 と互換性あり。[1]

2 アプリケーション

- タブレット
- スマートフォン
- パーソナル・コンピュータ
- 産業用および車載用

3 概要

SN74LV4T125 は低電圧 CMOS バッファ・ゲートで、動作電圧範囲が広く、ポータブル、テレコム、産業用、車載の各アプリケーションに対応します。出力レベルは電源電圧を基準としており、1.8V、2.5V、3.3V、5V の CMOS レベルをサポートします。

入力は、低スレッショルド回路を使用して V_{CC} = 3.3V で 1.8V 入力ロジックと一致するように設計されており、1.8V から 3.3V へのレベル・アップ変換に使用できます。また、5V 許容の入力ピンにより、降圧変換 (例:V_{CC} = 2.5V で 3.3V 入力から 2.5V 出力) が可能です。V_{CC} の範囲が 1.8V～5.5V と広いため、目的の出力レベルを発生させて外部のコントローラまたはプロセッサに接続できます。

SN74LV4T125 デバイスは、8mA の電流駆動能力を持つように設計されており、高駆動出力によるラインの反射、オーバーシュート、アンダーシュートを低減します。

製品情報

部品番号(1)	パッケージ	本体サイズ (公称)
SN74LV4T125	PW (TSSOP) (14)	5.00mm × 4.40mm
	RGY (VQFN、14)	3.50mm×3.50mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。

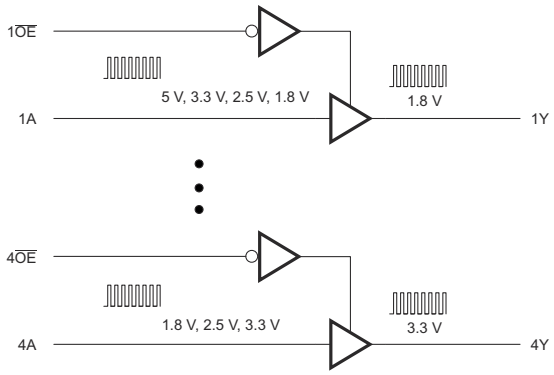

図 3-1. アプリケーション概略図

[1] より低い V_{CC} 条件については、V_{IH}/V_{IL} と出力駆動能力を参照してください。

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

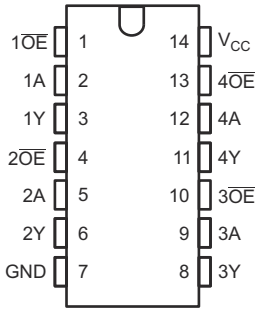
Changes from Revision B (March 2014) to Revision C (June 2022)	Page
• 「特長」に「I_{off} により部分的パワーダウン・モードでの動作をサポート」を追加。	1
• 文書全体にわたって表、図、相互参照の採番方法を更新	1
• 「ESD 定格」表、「ドキュメントの更新通知を受け取る方法」セクション、「サポート・リソース」セクションを追加。	1

Changes from Revision A (March 2014) to Revision B (September 2014)	Page
• 「特長」を更新	1
• Updated Pin Functions table.	3
• Added ESD Ratings table, Thermal Information table, Typical Characteristics section, Pin Configuration and Functions section, Detailed Description section, Power Supply Recommendations section, Layout section, Receiving Notification of Documentation Updates section, and Community Resources section	4
• Updated Detailed Design Procedure section.	13

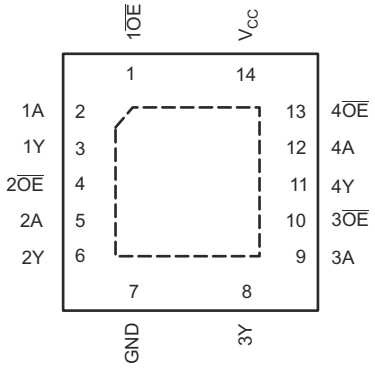
Changes from Revision * (February 2014) to Revision A (March 2014)	Page
• 1 ページのプレビュー・ドキュメントをフル・バージョンに更新。	1

5 Pin Configuration and Functions

PW Package
(TOP VIEW)



RGY Package
(Transparent TOP VIEW)



Pin Functions

PIN		TYPE [1]	DESCRIPTION
NO.	NAME		
1	1 $\overline{OE}$	I	Enable 1
2	1A	I	Input 1
3	1Y	O	Output 1
4	2 $\overline{OE}$	I	Enable 2
5	2A	I	Input 2
6	2Y	O	Output 2
7	GND	—	Ground Pin
8	3Y	O	Output 3
9	3A	I	Input 3
10	3 $\overline{OE}$	I	Enable 3
11	4Y	O	Output 4
12	4A	I	Input 4
13	4 $\overline{OE}$	I	Enable 4
14	V_{CC}	—	Power Pin

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7.0	V
V_I	Input voltage range(2)		–0.5	7.0	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	4.6	V
	Voltage range applied to any output in the high or low state(2)		–0.5	V_{CC} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–20	mA
I_{OK}	Output clamp current	V_O < 0 or V_O > V_{CC}		±50	mA
I_O	Continuous output current			±35	mA
	Continuous current through V_{CC} or GND			±70	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Machine Model (MM), per JEDEC specification	±200	
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.6	5.5	V
V_I	Input voltage		0	5.5	V
V_O	Output voltage	High or Low State	0	V_{CC}	V
		H-Z	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.8 V		–3	mA
		V_{CC} = 2.5 V		–5	
		V_{CC} = 3.3 V		–8	
		V_{CC} = 5.0 V		–16	
I_{OL}	Low-level output current	V_{CC} = 1.8 V		3	mA
		V_{CC} = 2.5 V		5	
		V_{CC} = 3.3 V		8	
		V_{CC} = 5.0 V		16	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 1.6 V to 2.0 V		20	ns/V
		V_{CC} = 2.3 V to 2.7 V		20	
		V_{CC} = 3 V or 3.6 V		20	
		V_{CC} = 4.5 V to 5.0 V		20	
T_A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

6.4 Thermal Information

THERMAL METRIC(1)		SN74LV4T125		UNIT
		PW	RGY	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	126.9	52.9	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	54.2	67.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	68.6	29.0	
ψ_{JT}	Junction-to-top characterization parameter	7.5	2.6	
ψ_{JB}	Junction-to-board characterization parameter	68.0	29.1	
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	—	9.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			T_A = –40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
V_{IH}	High-level input voltage		V_{CC} = 1.65 V to 1.9 V	0.95			1		V
			V_{CC} = 2.3 V to 2.7 V	1.1			1.2		
			V_{CC} = 3 V to 3.6 V	1.3			1.35		
			V_{CC} = 4.5 V to 5.0 V	2			2		
V_{IL}	Low-level input voltage		V_{CC} = 1.65 V to 1.9 V			0.55		0.5	V
			V_{CC} = 2.3 V to 2.77 V			0.7		0.6	
			V_{CC} = 3 V to 3.6 V			0.85		0.75	
			V_{CC} = 4.5 V to 5.5 V			0.9		0.85	
V_{OH}	High-level output voltage	I_{OH} = –50 µA	V_{CC} = 1.65 V to 5.5 V	V_{CC} – 0.1			V_{CC} – 0.1		V
		I_{OH} = –2 mA	V_{CC} = 1.65 V	1.4			1.35		V
		I_{OH} = –3 mA	V_{CC} = 2.3 V	2.05			2.0		V
		I_{OH} = –5 mA	V_{CC} = 3.0 V	2.7			2.6		V
		I_{OH} = –8 mA		2.6			2.5		
		I_{OH} = –8 mA	V_{CC} = 4.5 V	3.7			3.6		V
		I_{OH} = –16 mA		3.8			3.7		
		I_{OH} = –16 mA	V_{CC} = 5.0 V	4.4			4.3		V
V_{OL}	Low-level output voltage	I_{OL} = 50 µA	V_{CC} = 1.65 V to 5.5 V			0.1		0.1	V
		I_{OH} = 2 mA	V_{CC} = 1.65 V			0.1		0.1	V
			V_{CC} = 1.8 V			0.2		0.3	
		I_{OH} = 3 mA	V_{CC} = 2.3 V			0.2		0.3	V
			V_{CC} = 2.5 V			0.25		0.3	
		I_{OH} = 5 mA	V_{CC} = 3.0 V			0.35		0.4	V
		I_{OH} = 8 mA				0.4		0.45	
		I_{OH} = 8 mA	V_{CC} = 3.3 V			0.45		0.5	V
		I_{OH} = 8 mA	V_{CC} = 4.5 V			0.50		0.55	V
		I_{OH} = 16 mA				0.55		0.55	
		I_{OH} = 16 mA	V_{CC} = 5.0 V			0.55		0.55	V
I_I	Input leakage current	V_I =0 V or V_{CC}	V_{CC} = 0 V, 1.8 V, 2.5 V, 3.3 V, 5.5 V			±0.1		±1	µA
I_{CC}	Static supply current	V_I = 0 V or V_{CC}, I_O = 0; open on loading	V_{CC} = 5.0 V			2		20	µA
			V_{CC} = 3.3 V			2		20	
			V_{CC} = 2.5 V			2		20	
			V_{CC} = 1.8 V			2		20	
ΔI_{CC}	Additional static supply current	One input at 0.3 V or 3.4 V Other inputs at 0 or V_{CC}, I_O = 0	V_{CC} = 5.5 V			1.35		1.5	µA
		One input at 0.3 V or 1.1 V Other inputs at 0 or V_{CC}, I_O = 0	V_{CC} = 1.8 V						
I_{OZ}	Off-state (High Impedance State) Output Current	V_O = V_{CC} or GND	V_{CC} = 5.5 V			±0.25		±2.5	µA
I_{off}	Partial power down current	V_O or V_I = 0 to 5.5 V	V_{CC} = 0 V			0.5		5	µA
C_i	Input capacitance	V_I = V_{CC} or GND	V_{CC} = 3.3 V		1.6		1.6		pF
C_o	Output capacitance	V_O = V_{CC} or GND	V_{CC} = 3.3 V		4.8		4.8		pF

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted) (see 図 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	FREQUENCY (TYP)	V_{CC}	C_L	T_A = 25°C			T_A = –65°C to 125°C			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	Any In	Y	DC to 50 MHz	5.0 V	15 pF		2.8	3.2		3	3.5	ns
					30 pF		3	3.5		3	4.5	
				3.3 V	15 pF		4	4.5		5	5.5	
					30 pF		5	5.5		5.5	6.5	
			DC to 50 MHz	2.5 V	15 pF		5.5	6.5		7	7.5	ns
					30 pF		6.5	7		7.5	8.5	
			DC to 30 MHz	1.8 V	15 pF		10	11		11	12	ns
					30 pF		11	12		12.5	13	
t_{PZH}	$\overline{OE}$	Y	DC to 50 MHz	5.0 V	15 pF		3.5	4		3.5	4	ns
					30 pF		3.8	4.2		4	4.5	
				3.3 V	15 pF		5	5.8		5.8	6.1	
					30 pF		5.5	6		5.7	6.5	
			DC to 50 MHz	2.5 V	15 pF		7.5	8		8.5	9	ns
					30 pF		8	8.5		9	9.5	
			DC to 30 MHz	1.8 V	15 pF		14.5	15		15.5	16.5	ns
					30 pF		15.5	16		16	17	
t_{PZL}	$\overline{OE}$	Y	DC to 50 MHz	5.0 V	15 pF		3	3.5		3.5	4	ns
					30 pF		3.5	4		4	4.5	
				3.3 V	15 pF		5.3	5.6		6	6.2	
					30 pF		5.8	6.2		7	7.5	
			DC to 50 MHz	2.5 V	15 pF		8	8.5		9	9.5	ns
					30 pF		9	9.5		10.5	11	
			DC to 30 MHz	1.8 V	15 pF		17	17.5		18	18.5	ns
					30 pF		18	18.5		19	20	
t_{PHZ}	$\overline{OE}$	Y	DC to 50 MHz	5.0 V	15 pF		3	3.5		3.5	4	ns
					30 pF		3.5	4		4	4.5	
				3.3 V	15 pF		3.5	4		4.5	5	
					30 pF		5	6		6.5	7	
			DC to 50 MHz	2.5 V	15 pF		5.5	6		6	6.5	ns
					30 pF		7.5	8		8	9	
			DC to 30 MHz	1.8 V	15 pF		7.5	8		8	8.5	ns
					30 pF		11	12		12	13	
t_{PLZ}	$\overline{OE}$	Y	DC to 50 MHz	5.0 V	15 pF		2	2.5		2	2.7	ns
					30 pF		2	3		2	3.2	
				3.3 V	15 pF		2.3	2.8		2.5	3.2	
					30 pF		2.8	3.2		3.3	4	
			DC to 50 MHz	2.5 V	15 pF		3.3	3.8		3.8	4.2	ns
					30 pF		4	4.3		4.2	5	
			DC to 30 MHz	1.8 V	15 pF		5	5.5		5	5.7	ns
					30 pF		6.5	7		7	8.5	
t_{sk}	Any In	Y	DC to 50 MHz	5.0 V to 2.5 V	15 pF					1	1	ns
			DC to 30 MHz	1.8 V	15 pF							

6.7 Noise Characteristics

V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C(1)

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.4	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.3	–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		3		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

(1) Characteristics are for surface-mount packages only.

6.8 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 10 MHz	16	pF

6.9 Typical Characteristics

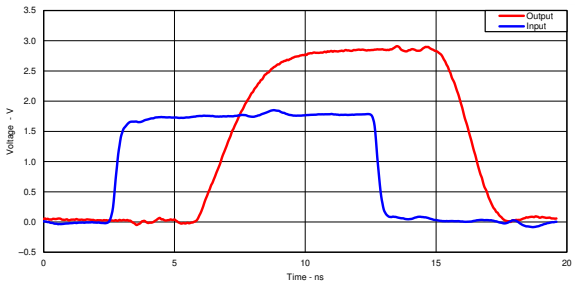
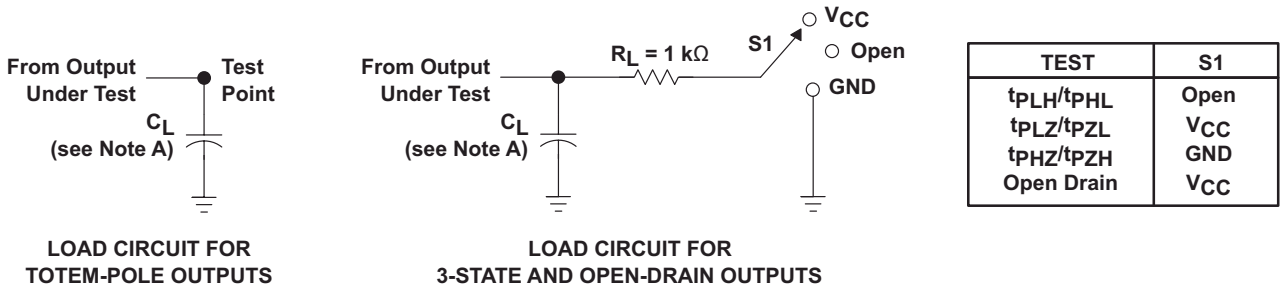


図 6-1. Switching Characteristics at 50 MHz Excellent Signal Integrity (1.8 V to 3.3 V at 3.3-V V_{CC})

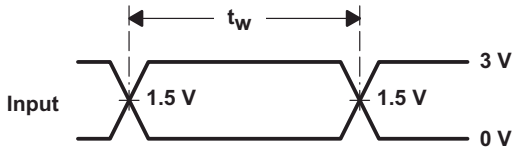
7 Parameter Measurement Information

7.1

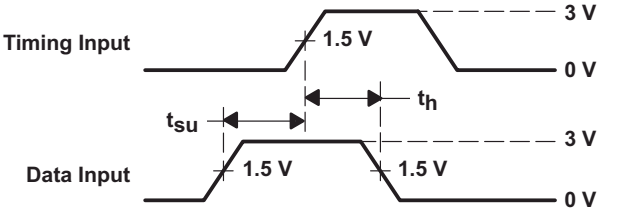


LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

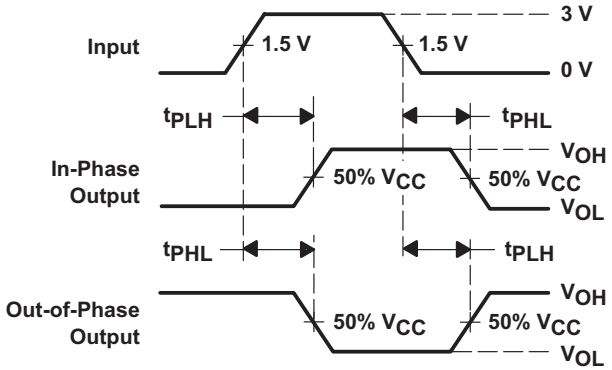
LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS



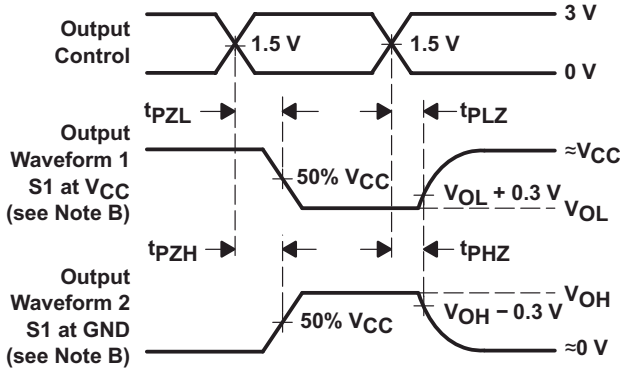
VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

図 7-1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74LVxTxx family was created to allow up- or down-voltage translation with only one power rail. The family has over-voltage tolerant inputs that allow down translation from up to 5.5 V to the V_{CC} level that can be as low as 1.8 V. The family SN74LVxTxx also has a lowered switching threshold that allows it to translate up to the V_{CC} level that can be as high as 5.5 V.

8.1.1 Translating Down

Using these parts to translate down is very simple. Because the inputs are tolerant to 5.5 V at any valid V_{CC}, they can be used to down translate. The input can be any level above V_{CC} up to 5.5 V and the output will equal the V_{CC} level, which can be as low as 1.8 V. One important advantage to down translating using this part is that the I_{CC} current will remain less than or equal to the specified value.

Down translation possibilities with SN74LVxTxx:

- With 1.8-V V_{CC} from 2.5 V, 3.3 V, or 5 V down to 1.8 V.
- With 2.5-V V_{CC} from 3.3 V or 5 V down to 2.5 V.
- With 3.3-V V_{CC} from 5 V down to 3.3 V.

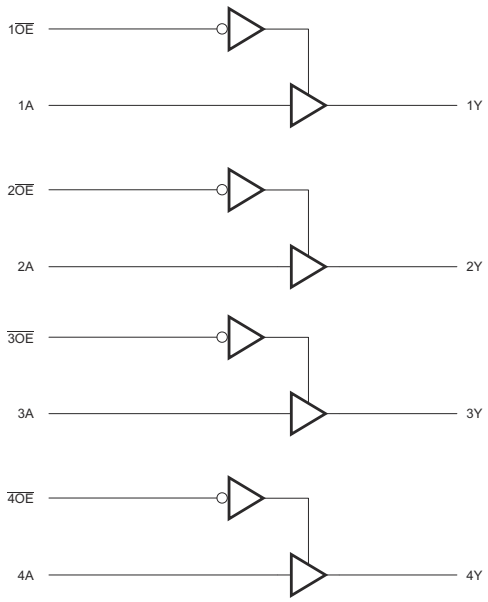
8.1.2 Translating Up

Using the SN74LVxTxx family to translate up is very simple. The input switching threshold is lowered so the high level of the input voltage can be much lower than a typical CMOS V_{IH}. For instance, If the V_{CC} is 3.3 V then the typical CMOS switching threshold would be V_{CC} / 2 or 1.65 V. This means the input high level must be at least V_{CC} × 0.7 or 2.31 V. On the LVxT devices the input threshold for 3.3-V V_{CC} is approximately 1 V. This allows a signal with a 1.8-V V_{IH} to be translated up to the V_{CC} level of 3.3 V.

Up translation possibilities with SN74LVxTxx:

- With 2.5-V V_{CC} from 1.8 V to 2.5 V.
- With 3.3-V V_{CC} from 1.8 V or 2.5 V to 3.3 V.
- With 5-V V_{CC} From 2.5 V or 3.3 V to 5 V.

8.2 Functional Block Diagram



8.3 Feature Description

This part is a single supply buffer that is capable up or down translation. The output will equal V_{CC} while the input can vary from 1.2 V to 5.5 V.

Up Translation Mode:

- 1.2 V to 1.8 V at 1.8-V V_{CC}
- 1.5 V to 2.5 V at 2.5-V V_{CC}
- 1.8 V to 3.3 V at 3.3-V V_{CC}
- 3.3 V to 5.0 V at 5.0-V V_{CC}

Down Translation Mode:

- 3.3 V to 1.8 V at 1.8-V V_{CC}
- 3.3 V to 2.5 V at 2.5-V V_{CC}
- 5.0 V to 3.3 V at 3.3-V V_{CC}

8.4 Device Functional Modes

This device performs the function of a buffer where input logic level equals the output logic level, while providing buffering and drive to the output. The SN74LV4T125 device will also translate voltages up or down while performing this function.

表 8-1. Function Table (Each Buffer)

INPUTS (1)		OUTPUT (2)
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

表 8-2. Supply V_{CC} = 3.3 V

INPUT b (Lower Level Input)		OUTPUT (V_{CC} CMOS)
A	B	Y
V_{IH}(min) = 1.35 V		V_{OH}(min) = 2.9 V
V_{IL}(max) = 0.8 V		V_{OL}(max) = 0.2 V

(1) H = High Voltage Level, L = Low Voltage Level, X = Do not Care, Z = High Impedance
(2) H = Driving High, L = Driving Low, Z = High Impedance State

9 Applications and Implementation

Note

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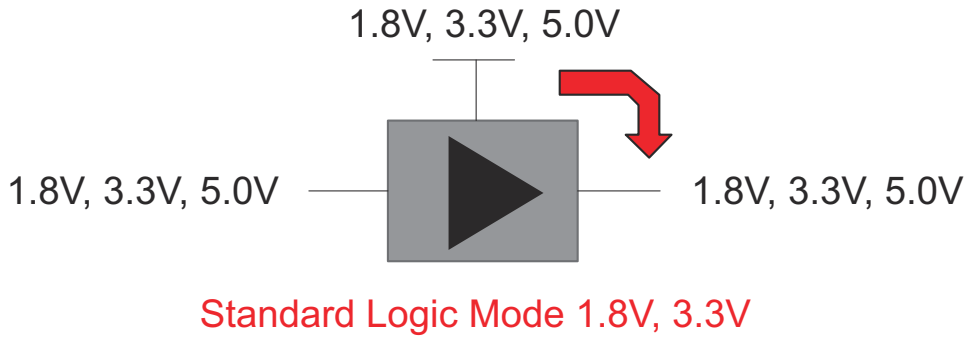
9.1 Application Information

Based upon the lower-threshold circuit design of the LVxT family, the LVxT family also supports level translation. For level translation up and down, the LVxT family requires only a single power supply.



9.2 Typical Application

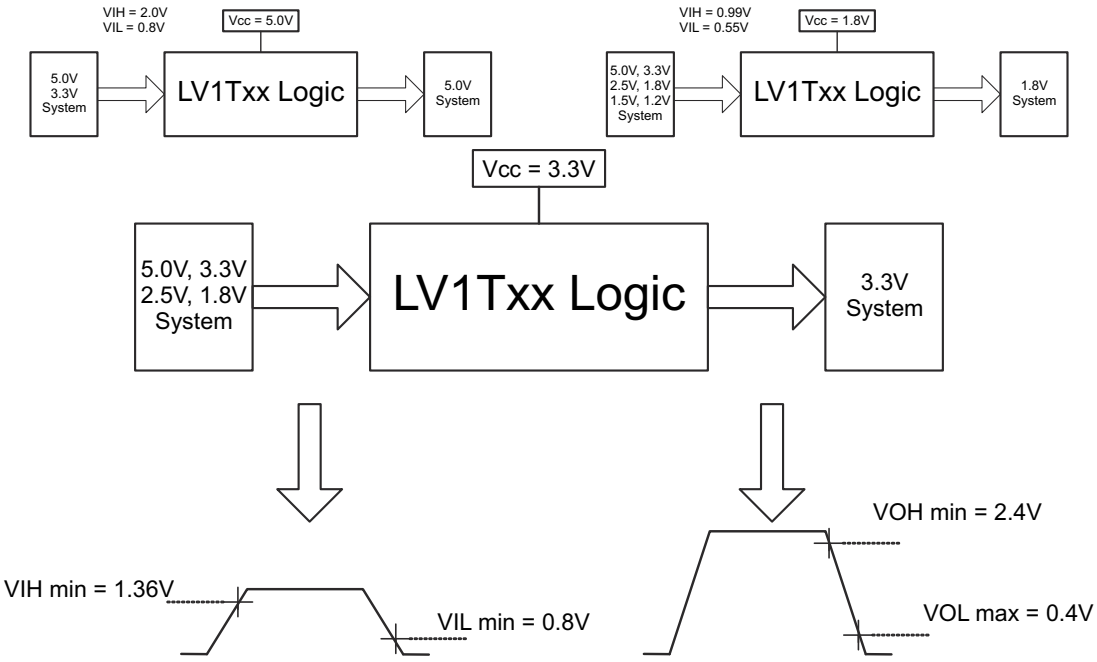


図 9-1. Switching Thresholds for 1.8 V to 3.3 V Translation

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. The input threshold levels are lowered to allow for up translation. At 5 V the device has equivalent TTL input levels.

9.2.2 Detailed Design Procedure

1. Recommended input conditions:
   - Rise time and fall time specifications. See (Δt/ΔV) in *Recommended Operating Conditions* table.
   - Specified high and low levels. See (V_{IH} and V_{IL}) in *Recommended Operating Conditions* table.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
2. Recommend output conditions:
   - Load currents should not exceed 35 mA per output and 70 mA total for the part.
   - Outputs should not be pulled above V_{CC}.

9.2.3 Application Curves

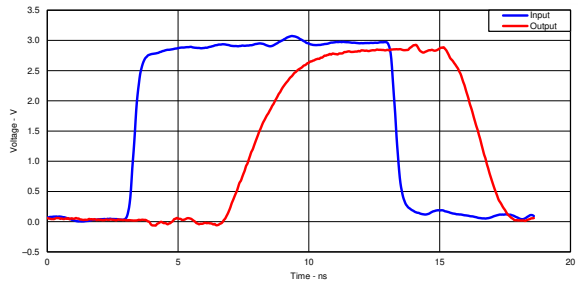


図 9-2. Switching Characteristics at 50 MHz Excellent Signal Integrity (3.3 V to 3.3 V at 3.3-V V_{CC})

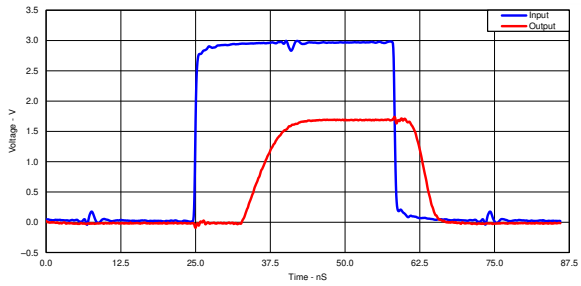


図 9-3. Switching Characteristics at 15 MHz Excellent Signal Integrity (3.3 V to 1.8 V at 1.8-V V_{CC})

10 Power Supply Recommendations

The power supply can be any voltage between the Min and Max supply voltage rating located in the *Recommended Operating Conditions*.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µF is recommended. If there are multiple V_{CC} pins, then 0.01 µF or 0.022 µF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in 図 11-1 are the rules that must be observed under all circumstances.

All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient.

It is generally acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the IOs so they also cannot float when disabled.

11.2 Layout Example

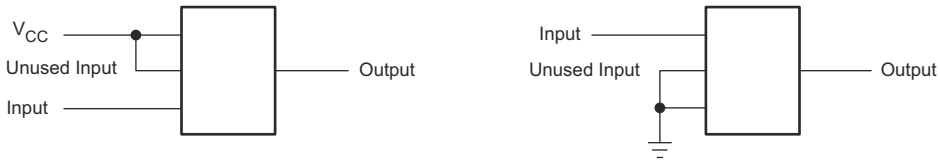


図 11-1. Layout Diagram

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Additional Product Selection

DEVICE	PACKAGE	DESCRIPTION
SN74LV1T00	DCK, DBV	2-Input Positive-NAND Gate
SN74LV1T02	DCK, DBV	2-Input Positive-NOR Gate
SN74LV1T04	DCK, DBV	Inverter Gate
SN74LV1T08	DCK, DBV	2-Input Positive-AND Gate
SN74LV1T34	DCK, DBV, DRL	Single Buffer Gate
SN74LV1T14	DCK, DBV	Single Schmitt-Trigger Inverter Gate
SN74LV1T32	DCK, DBV	2-Input Positive-OR Gate
SN74LV1T86	DCK, DBV	Single 2-Input Exclusive-Or Gate
SN74LV1T125	DCK, DBV, DRL	Single Buffer Gate with 3-state Output
SN74LV1T126	DCK, DBV, DRL	Single Buffer Gate with 3-state Output
SN74LV4T125	RGY, PW	Quadruple Bus Buffer Gate With 3-State Outputs

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 サポート・リソース

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12.4 Trademarks

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV4T125PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LV4T125	Samples
SN74LV4T125RGYR	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVT125	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN74LV4T125 :

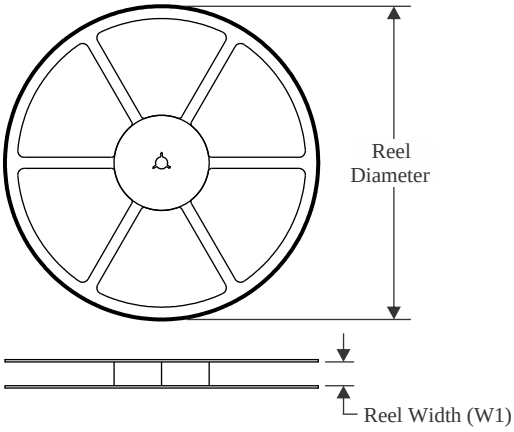
- Automotive : SN74LV4T125-Q1
- Enhanced Product : SN74LV4T125-EP

NOTE: Qualified Version Definitions:

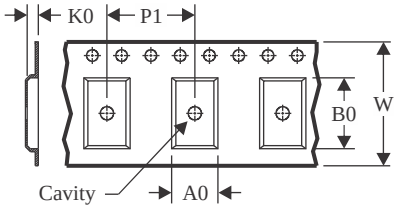
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

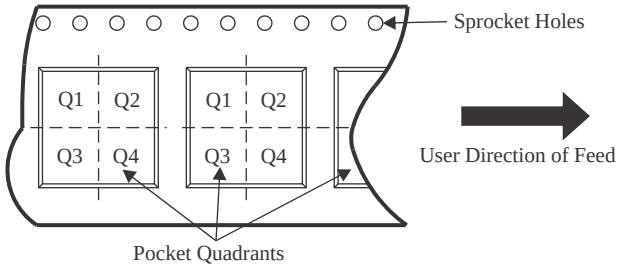


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

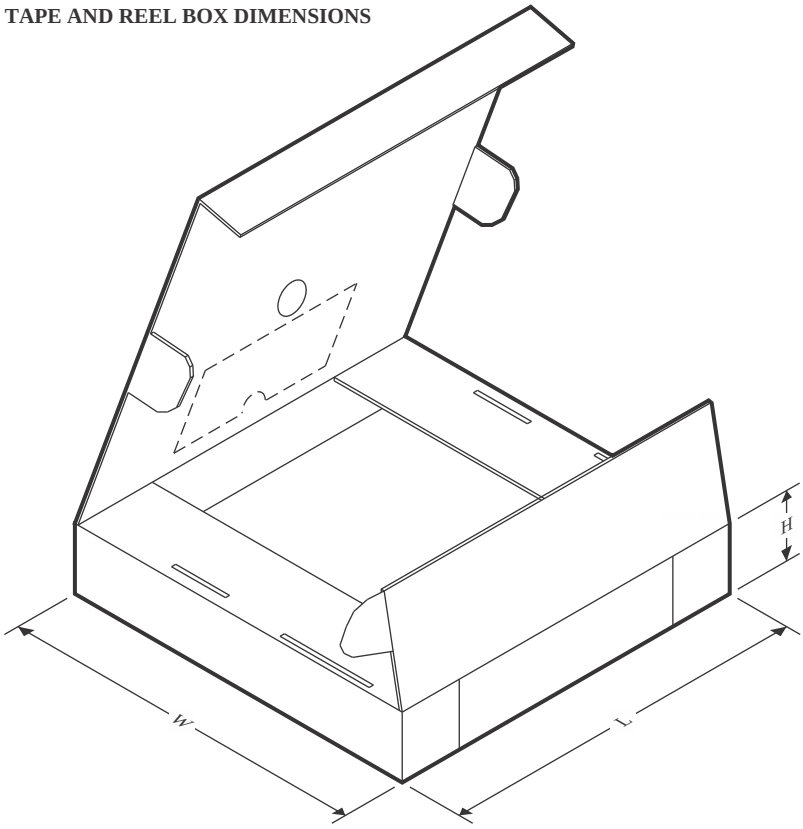
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV4T125PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV4T125PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV4T125RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

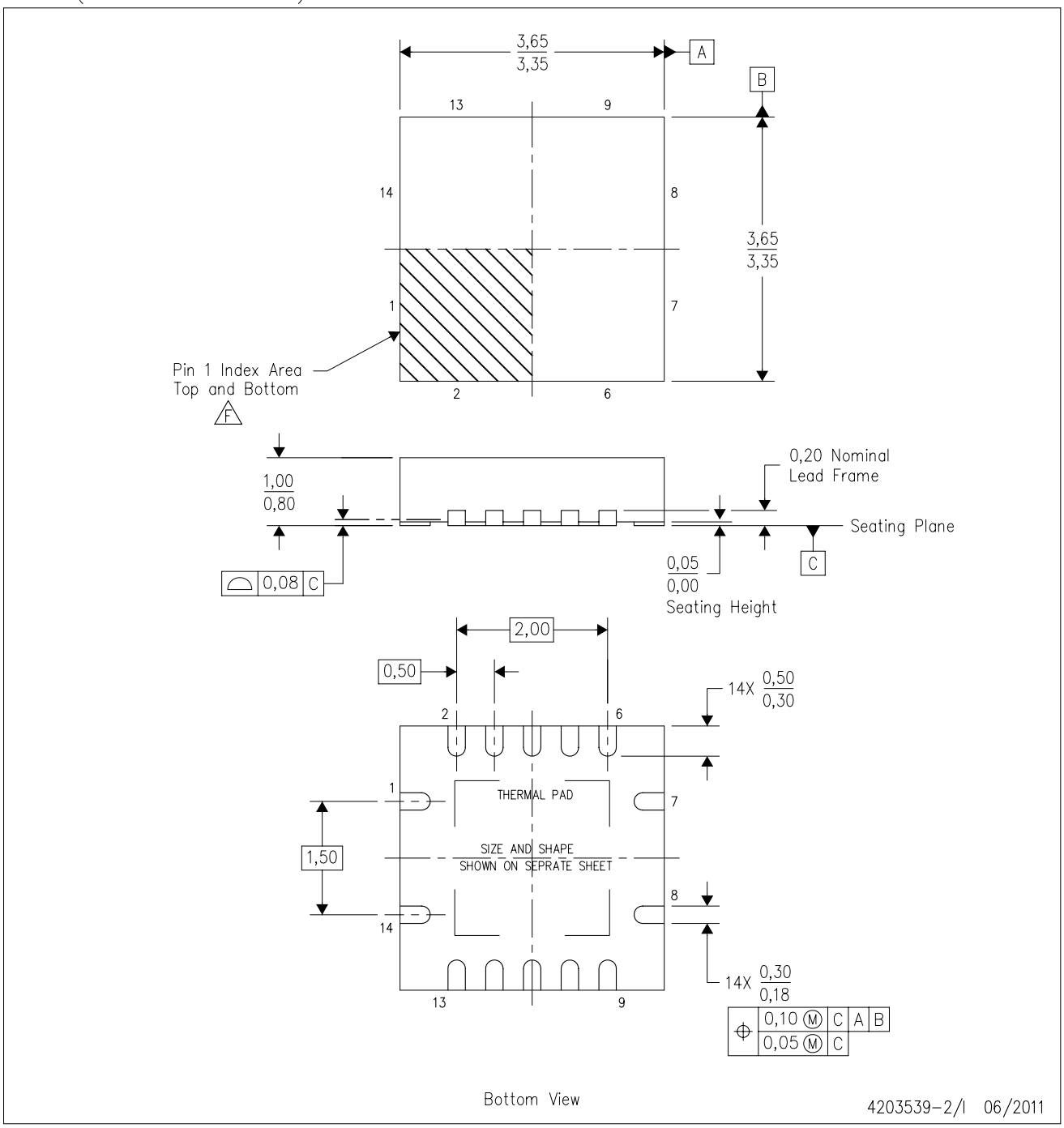
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

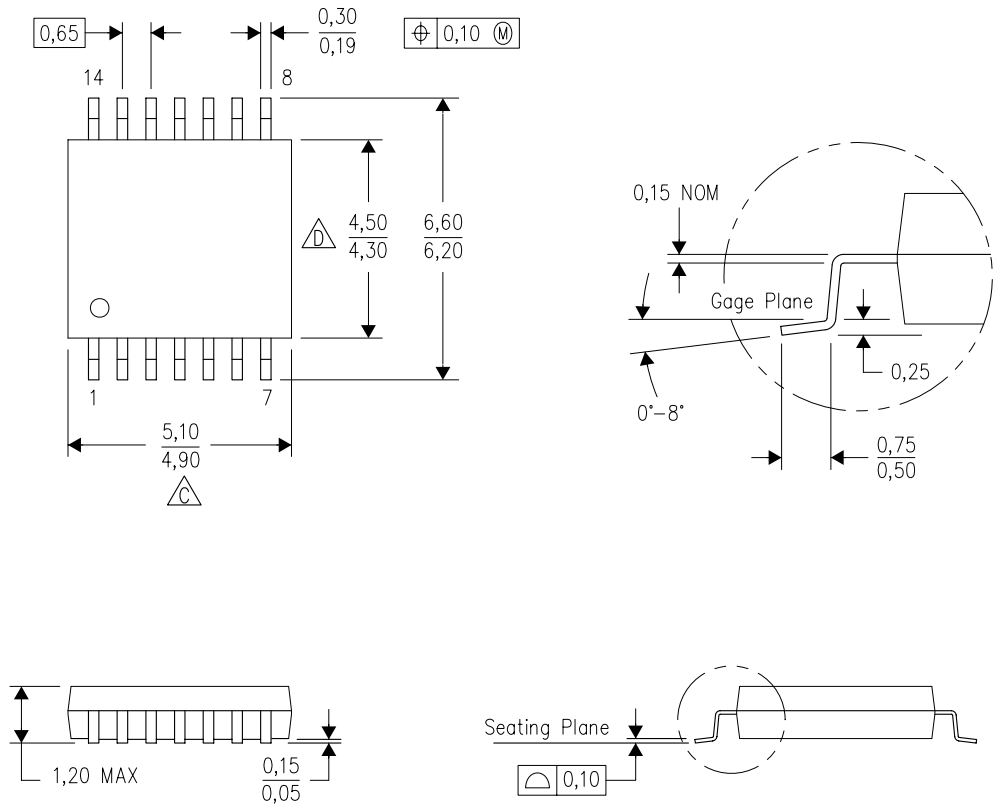
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV4T125PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74LV4T125PWR	TSSOP	PW	14	2000	364.0	364.0	27.0
SN74LV4T125RGYR	VQFN	RGY	14	3000	360.0	360.0	36.0

RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

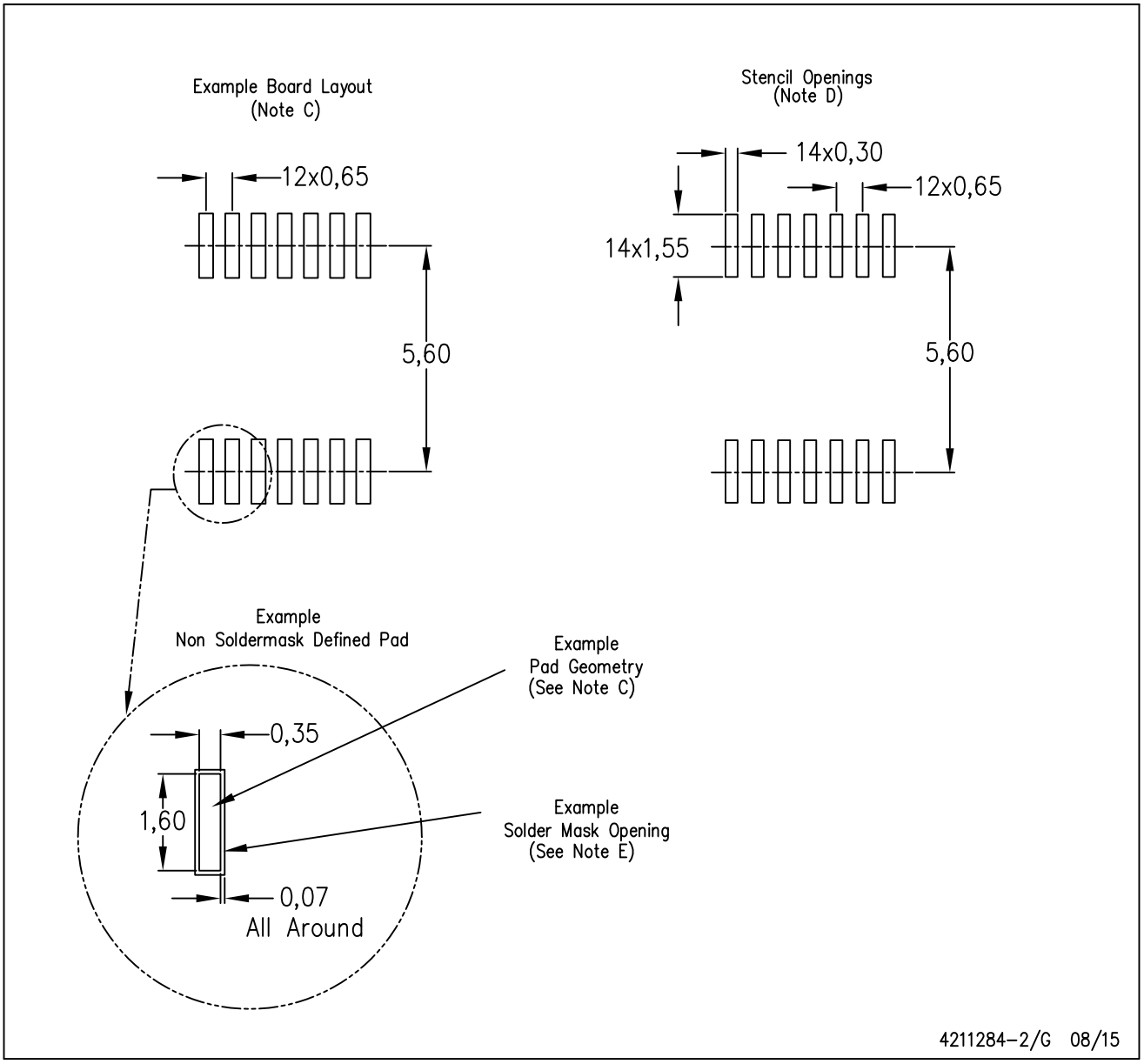
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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