

SN74LVC2G241 デュアル・バッファドライバ、3-state 出力

1 特長

- テキサス・インスツルメンツの NanoFree™ パッケージで供給
- 5V V_{CC} 動作をサポート
- 5.5V までの入力電圧に対応
- 最大 t_{pd} 4.1ns (3.3V 時)
- 低消費電力、最大 I_{CC} 10 μ A
- 3.3V において ± 24 mA の出力駆動能力
- 標準 V_{OLP} (出力グランド・バウンス) < 0.8V ($V_{CC} = 3.3V$, $T_A = 25^\circ C$)
- 標準 V_{OHV} (出力 V_{OH} アンダーシュート) > 2V ($V_{CC} = 3.3V$, $T_A = 25^\circ C$)
- I_{off} により活線挿抜、部分的パワーダウン・モード、バック・ドライブ保護をサポート
- 最高 5.5V の入力を V_{CC} レベルに変換する降圧トランスレータとして使用可能
- JESD 78, Class II 準拠で 100mA 超のラッチアップ性能
- JESD 22 を超える ESD 保護
 - 2000V、人体モデル (A114-A)
 - 200V、マシン・モデル (A115-A)
 - 1000V、荷電デバイス・モデル (C101)

2 アプリケーション

- AV レシーバ
- Blu-ray プレーヤおよびホーム・シアター
- DVD レコーダおよびプレーヤ
- デスクトップ PC または ノート PC
- デジタル・ラジオまたは インターネット・ラジオ・プレーヤ
- デジタル・ビデオ・カメラ (DVC)
- 組み込み用 PC
- GPS : パーソナル・ナビゲーション・デバイス
- モバイル・インターネット・デバイス
- ネットワーク・プロジェクトのフロントエンド
- 携帯用メディア・プレーヤ
- プロ用オーディオ・ミキサー

3 概要

このデュアル・バッファおよびライン・ドライバは、1.65V ~ 5.5V の V_{CC} で動作するように設計されています。

SN74LVC2G241 デバイスは、3-state メモリ・アドレス・ドライバ、クロック・ドライバ、バス用レシーバ/トランスミッタの性能と密度の両方を向上することに特化して設計されています。

NanoFree パッケージ技術は IC パッケージの概念における主要なブレイクスルーであり、ダイをパッケージとして使用します。

SN74LVC2G241 デバイスは、独立した出力イネーブル ($1\overline{OE}$ 、 $2OE$) 入力を備えた 2 つの 1ビット・ライン・ドライバで構成されています。 $1\overline{OE}$ が LOW、 $2OE$ が HIGH の場合、デバイスは A 入力からのデータを Y 出力に渡します。 $1\overline{OE}$ が HIGH、 $2OE$ が LOW の場合、出力は高インピーダンス状態になります。

電源オンまたは電源オフ時に高インピーダンス状態になるように、 \overline{OE} をプルダウン抵抗経路で V_{CC} に接続し、 OE をプルダウン抵抗経路で GND に接続する必要があります。この抵抗の最小値は、ドライバの電流シンクまたは電流ソース能力によって決まります。

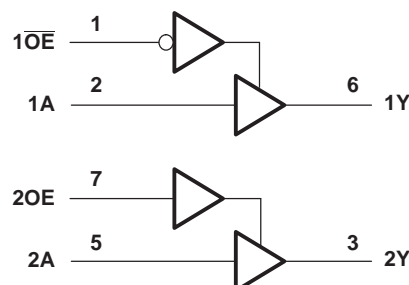
このデバイスは、 I_{off} を使用する部分的パワーダウン・アプリケーション用に完全に動作が規定されています。 I_{off} 回路が出力をディセーブルにするため、電源切断時にデバイスに電流が逆流して損傷に至ることを回避できます。

製品情報⁽¹⁾

型番	パッケージ	本体サイズ(公称)
SN74LVC2G241DCT	SM8 (8)	2.95mmx2.80mm
SN74LVC2G241DCU	VSOOP (8)	2.30mmx2.00mm
SN74LVC2G241YZP	DSBGA (8)	1.91mmx0.91mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

ロジック図 (正論理)



目次

1	特長	1	8.2	Functional Block Diagram	8
2	アプリケーション	1	8.3	Feature Description	8
3	概要	1	8.4	Device Functional Modes	8
4	改訂履歴	2	9	Application and Implementation	9
5	Pin Configuration and Functions	3	9.1	Application Information	9
6	Specifications	4	9.2	Typical Application	9
6.1	Absolute Maximum Ratings	4	10	Power Supply Recommendations	10
6.2	ESD Ratings	4	11	Layout	10
6.3	Recommended Operating Conditions	4	11.1	Layout Guidelines	10
6.4	Thermal Information	5	11.2	Layout Example	10
6.5	Electrical Characteristics	5	12	デバイスおよびドキュメントのサポート	11
6.6	Switching Characteristics	6	12.1	ドキュメントのサポート	11
6.7	Operating Characteristics	6	12.2	コミュニティ・リソース	11
6.8	Typical Characteristic	6	12.3	商標	11
7	Parameter Measurement Information	7	12.4	静電気放電に関する注意事項	11
8	Detailed Description	8	12.5	Glossary	11
8.1	Overview	8	13	メカニカル、パッケージ、および注文情報	11

4 改訂履歴

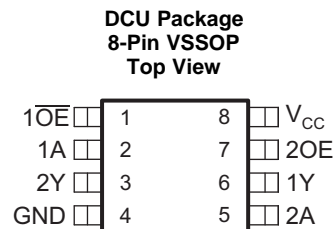
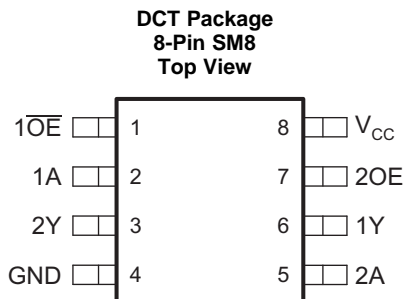
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision O (December 2015) から Revision P に変更	Page
• Changed Electrical Characteristics table format	5
• Changed Switching Characteristics tables format.	6

Revision N (November 2013) から Revision O に変更	Page
• 「アプリケーション」セクション、「製品情報」表、「ESD定格」表、「熱に関する情報」表、「代表的特性」セクション、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加	1

Revision M (February 2007) から Revision N に変更	Page
• ドキュメントを新しい TI データシートのフォーマットに更新	1
• 「注文情報」表を削除	1
• 「特長」を更新	1
• Updated operating temperature range.	4

5 Pin Configuration and Functions



YZP Package
8-Pin DSBGA
Bottom View



Pin Functions⁽¹⁾⁽²⁾

PIN		I/O	DESCRIPTION
NAME	NO.		
1A	2	I	Input
$\overline{1OE}$	1	I	Output enable (Active low)
1Y	6	O	Output
2A	5	I	Input
2Y	3	O	Output
2OE	7	I	Output enable (Active high)
GND	4	—	Ground
V _{CC}	8	—	Power pin

(1) N.C. – No internal connection

(2) See for dimensions

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		-0.5	6.5	V
V _I	Input voltage ⁽²⁾		-0.5	6.5	V
V _O	Voltage applied to any output in the high-impedance or power-off state ⁽²⁾		-0.5	6.5	V
V _O	Voltage applied to any output in the high or low state ⁽²⁾⁽³⁾		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
I _O	Continuous output current			±50	mA
	Continuous current through V _{CC} or GND			±100	mA
T _J	Maximum junction temperature			150	°C
T _{stg}	Storage temperature		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		
		V _{CC} = 3 V to 3.6 V	2		
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V		0.7	
		V _{CC} = 3 V to 3.6 V		0.8	
		V _{CC} = 4.5 V to 5.5 V		0.3 × V _{CC}	
V _I	Input voltage		0	5.5	V
V _O	Output voltage	High or low state	0	V _{CC}	V
		3-state	0	5.5	
I _{OH}	High-level output current	V _{CC} = 1.65 V		-4	mA
		V _{CC} = 2.3 V		-8	
		V _{CC} = 3 V		-16	
		V _{CC} = 4.5 V		-24	

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

Recommended Operating Conditions⁽¹⁾ (continued)

		MIN	MAX	UNIT
I _{OL}	Low-level output current	V _{CC} = 1.65 V	4	mA
		V _{CC} = 2.3 V	8	
		V _{CC} = 3 V	16	
			24	
V _{CC} = 4.5 V	32			
Δt/Δv	Input transition rise or fall rate	V _{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V	20	ns/V
		V _{CC} = 3.3 V ± 0.3 V	10	
		V _{CC} = 5 V ± 0.5 V	5	
T _A	Operating free-air temperature	-40	85	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	SN74LVC2G241			UNIT
	DCT (SM8)	DCU (VSSOP)	YZP (DSBGA)	
	8 PINS	8 PINS	8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance			°C/W
	220	227	102	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

over recommended operating free-air temperature range, T_A = -40°C to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	-40°C to 85°C			-40°C to 125°C (Recommended)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = -100 μA	1.65 V to 5.5 V	V _{CC} - 0.1			V _{CC} - 0.1			V
	I _{OH} = -4 mA	1.65 V	1.2			1.2			
	I _{OH} = -8 mA	2.3 V	1.9			1.9			
	I _{OH} = -16 mA	3 V	2.4			2.4			
	I _{OH} = -24 mA		2.3			2.3			
	I _{OH} = -32 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 100 μA	1.65 V to 5.5 V	0.1			0.1			V
	I _{OL} = 4 mA	1.65 V	0.45			0.45			
	I _{OL} = 8 mA	2.3 V	0.3			0.3			
	I _{OL} = 16 mA	3 V	0.4			0.4			
	I _{OL} = 24 mA		0.55			0.55			
	I _{OL} = 32 mA	4.5 V	0.55			0.75			
I _i	A or \overline{OE} inputs	V _I = 5.5 V or GND	0 to 5.5 V			±5			μA
I _{off}	V _I or V _O = 5.5 V	0	±10			±10			μA
I _{OZ}	V _O = 0 to 5.5 V	3.6 V	10			10			μA
I _{CC}	V _I = 5.5 V or GND, I _O = 0	1.65 V to 5.5 V	10			10			μA
ΔI _{CC}	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 5.5 V	500			500			μA
C _i	Data Inputs	V _I = V _{CC} or GND	3.5						pF
	Control Inputs		4						
C _o	V _O = V _{CC} or GND	3.3 V	6.5						pF

6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°C to 85°C								UNIT
			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	3.3	9.1	1.5	5.5	1.4	4.3	1.0	4.0	ns
t _{en}	\overline{OE}	Y	4.0	9.9	1.3	6.6	1.2	4.7	1.1	5.0	ns
t _{dis}	\overline{OE}	Y	1.5	11.6	1.0	5.7	1.4	4.6	0.5	4.2	ns

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°C to 125°C (Recommended)								UNIT
			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	3.3	10.1	1.5	5.6	1.4	5.3	1.0	4.2	ns
t _{en}	\overline{OE}	Y	4.0	10.9	1.3	6.6	1.2	5.7	1.2	4.3	ns
t _{dis}	\overline{OE}	Y	1.5	12.6	1.0	6.6	1.4	5.6	1.0	3.9	ns

6.7 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V _{CC}	TYP	UNIT	
C _{pd}	Power dissipation capacitance per buffer/driver	Outputs enabled	f = 10 MHz	V _{CC} = 1.8 V	19	pF
				V _{CC} = 2.5 V	19	
				V _{CC} = 3.3 V	20	
				V _{CC} = 5 V	22	
	Outputs disabled	V _{CC} = 1.8 V	2	pF		
		V _{CC} = 2.5 V	2			
		V _{CC} = 3.3 V	2			
		V _{CC} = 5 V	3			

6.8 Typical Characteristic

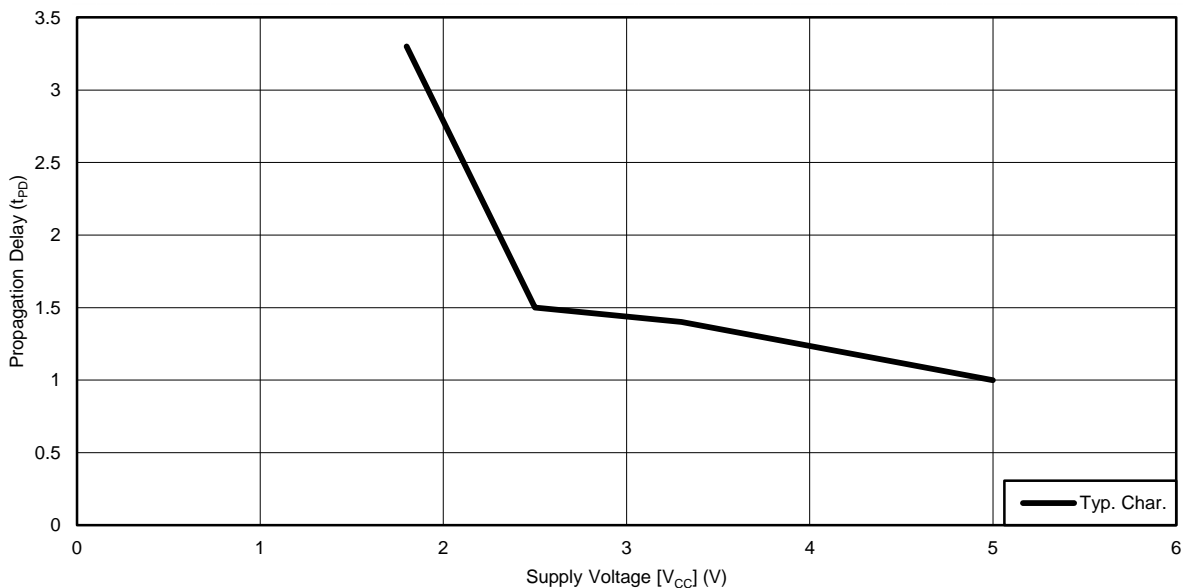
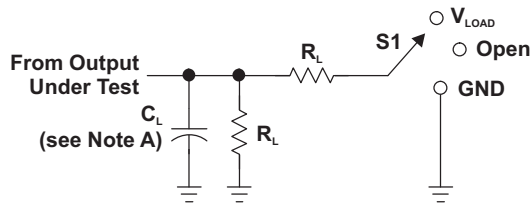


Figure 1. t_{pd} vs V_{CC} Over Full Temperature Range

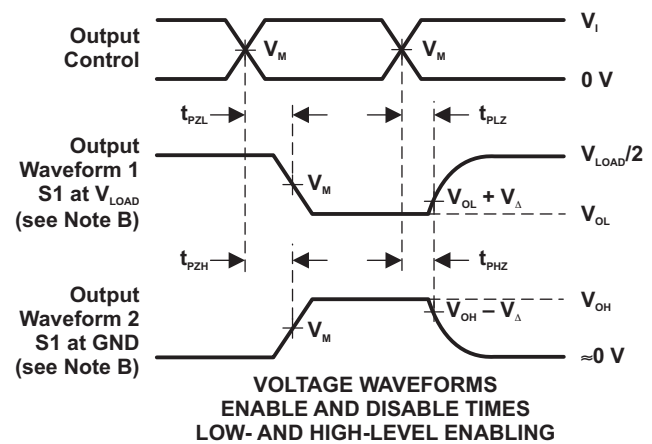
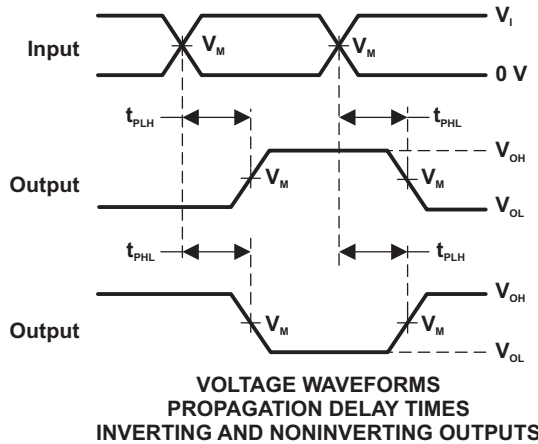
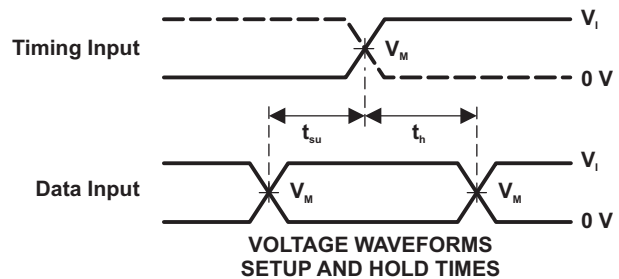
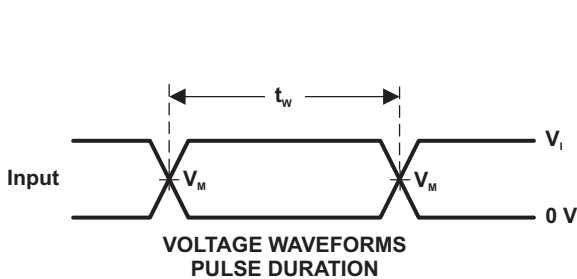
7 Parameter Measurement Information



LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_i	t_i/t_r					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_o = 50\ \Omega$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74LVC2G241 device is designed specifically to improve both the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters. The SN74LVC2G241 device is organized as two 1-bit line drivers with separate output-enable ($\overline{1OE}$, 2OE) inputs. When $\overline{1OE}$ is low and 2OE is high, the device passes data from the A inputs to the Y outputs. When $\overline{1OE}$ is high and 2OE is low, the outputs are in the high-impedance state.

The SN74LVC2G241 is also an effective redriver, with a maximum output current drive of 32 mA.

8.2 Functional Block Diagram

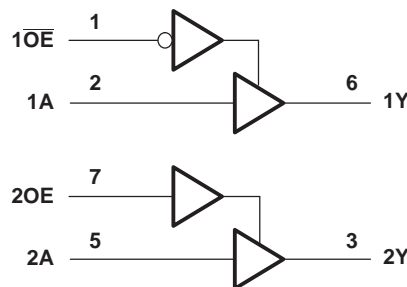


Figure 3. Logic Diagram (Positive Logic)

8.3 Feature Description

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor, and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking or the current-sourcing capability of the driver.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

8.4 Device Functional Modes

Table 1 and Table 2 list the functional modes of the SN74LVC2G241.

Table 1. Gate 1 Functional Table

INPUTS		OUTPUT 1Y
$\overline{1OE}$	1A	
L	H	H
L	L	L
H	X	Z

Table 2. Gate 2 Functional Table

INPUTS		OUTPUT 2Y
2OE	2A	
H	H	H
H	L	L
L	X	Z

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Typical Application shows a simple application where a physical push button is connected to the SN74LVC2G241. The push button is in a physical location far enough away from the processor that the input signal is weak and needs to be redriven. The SN74LVC2G241 acts as a redriver, providing a strong input signal to the processor with as little as 1 ns of propagation delay.

9.2 Typical Application

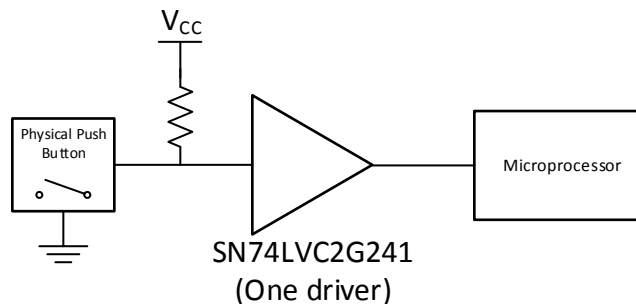


Figure 4. SN74LVC2G241 Application

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive also creates fast edges into light loads, so routing and load conditions must be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
 - Rise time and fall time specs. See ($\Delta t/\Delta V$) in *Recommended Operating Conditions*.
 - Specified high and low levels. See (V_{IH} and V_{IL}) in *Recommended Operating Conditions*.
 - Inputs are overvoltage tolerant allowing them to go as high as (V_I max) in *Recommended Operating Conditions* at any valid V_{CC} .
2. Recommend Output Conditions
 - Load currents must not exceed (I_O max) per output and must not exceed (Continuous current through V_{CC} or GND) total current for the part. These limits are located in *Absolute Maximum Ratings*.
 - Outputs must not be pulled above V_{CC} during normal operation or 5.5 V in high-z state.

Typical Application (continued)

9.2.3 Application Curve

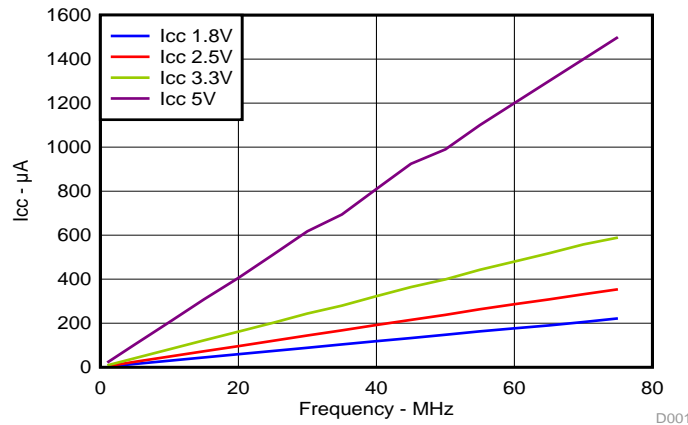


Figure 5. I_{CC} vs Frequency

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in [Recommended Operating Conditions](#).

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-µF capacitor is recommended and if there are multiple V_{CC} pins then a 0.01-µF or 0.022-µF capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices inputs must not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever make more sense or is more convenient.

11.2 Layout Example

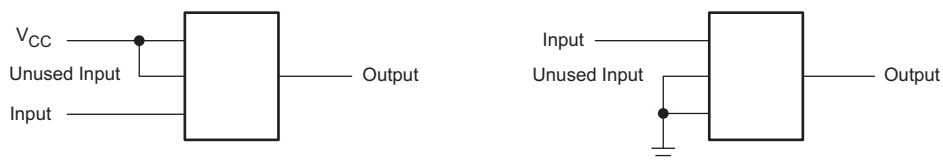


Figure 6. Layout Diagram

12 デバイスおよびドキュメントのサポート

12.1 ドキュメントのサポート

12.1.1 関連資料

関連資料については、以下を参照してください。

『低速またはフローティングCMOS入力の影響』、SCBA004

12.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™オンライン・コミュニティ TIのE2E (*Engineer-to-Engineer*) コミュニティ。エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイデアを検討して、問題解決に役立てることができます。

設計サポート TIの設計サポート 役に立つE2Eフォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

12.3 商標

NanoFree, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 静電気放電に関する注意事項



これらのデバイスは、限定的なESD(静電破壊)保護機能を内蔵しています。保存時または取り扱い時は、MOSゲートに対する静電破壊を防止するために、リード線同士をショートさせておくか、デバイスを導電フォームに入れる必要があります。

12.5 Glossary

[SLYZ022](#) — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。このデータシートのブラウザ対応版については、左側にあるナビゲーションを参照してください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74LVC2G241DCTRE4	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C41 Z
74LVC2G241DCTRE4.B	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C41 Z
74LVC2G241DCTRG4	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C41 Z
74LVC2G241DCTRG4.B	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C41 Z
74LVC2G241DCURG4.B	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C41R
74LVC2G241DCUTG4	Active	Production	VSSOP (DCU) 8	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C41R
74LVC2G241DCUTG4.B	Active	Production	VSSOP (DCU) 8	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C41R
SN74LVC2G241DCTR	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(2WP5, C41) Z
SN74LVC2G241DCTR.B	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(2WP5, C41) Z
SN74LVC2G241DCUR	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(C41J, C41Q, C41R)
SN74LVC2G241DCUR.B	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C41J, C41Q, C41R)
SN74LVC2G241DCUT	Active	Production	VSSOP (DCU) 8	250 SMALL T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(C41J, C41Q, C41R)
SN74LVC2G241DCUT.B	Active	Production	VSSOP (DCU) 8	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C41J, C41Q, C41R)
SN74LVC2G241DCUTG4.B	Active	Production	VSSOP (DCU) 8	250 SMALL T&R	-	Call TI	Call TI	-40 to 125	
SN74LVC2G241YZPR	Active	Production	DSBGA (YZP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	(C2, C27)
SN74LVC2G241YZPR.B	Active	Production	DSBGA (YZP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	(C2, C27)

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

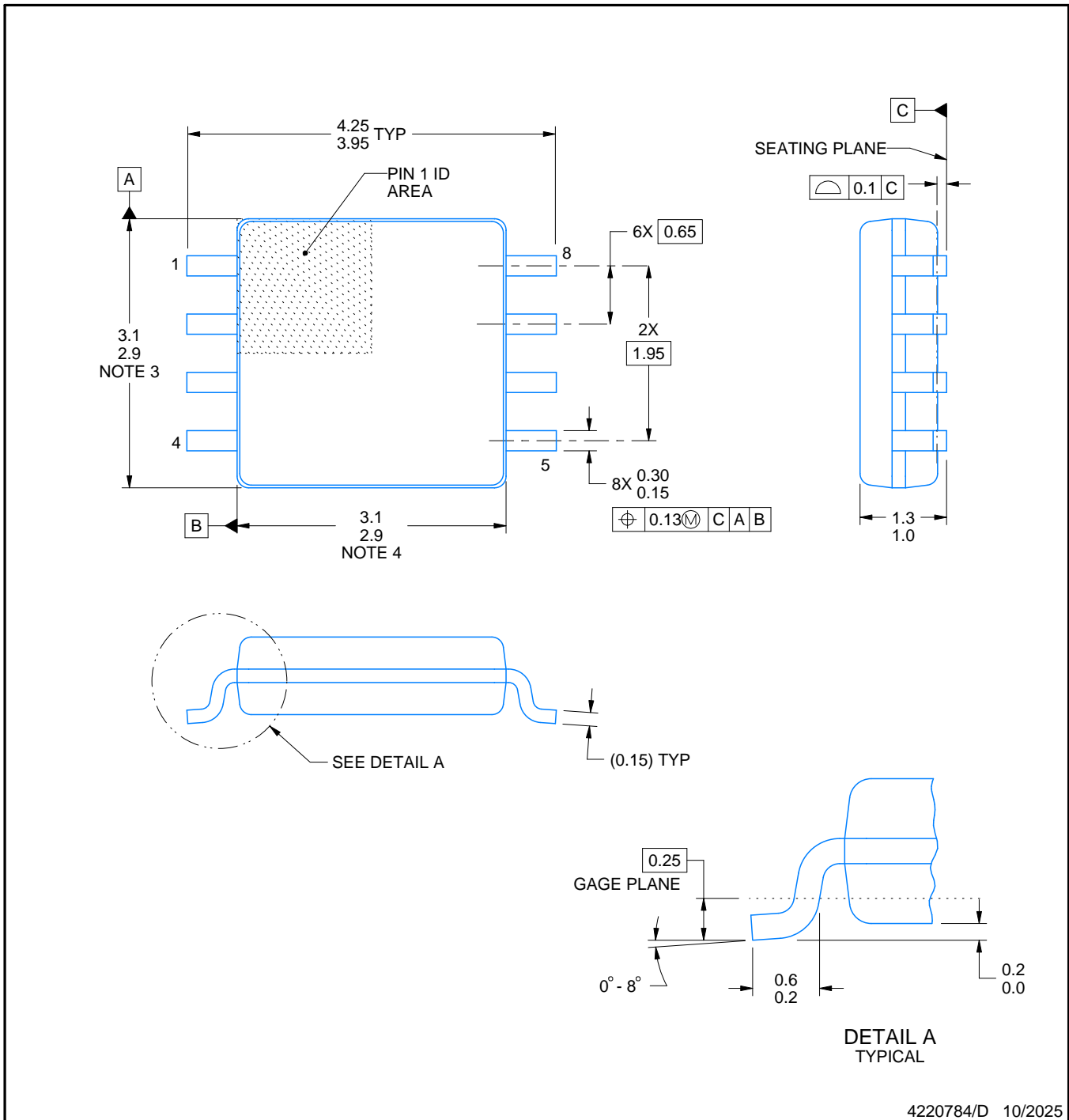
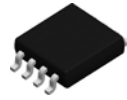
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74LVC2G241DCTRE4	SSOP	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
74LVC2G241DCTRG4	SSOP	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
74LVC2G241DCUTG4	VSSOP	DCU	8	250	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G241DCTR	SSOP	DCT	8	3000	180.0	12.4	3.15	4.35	1.55	4.0	12.0	Q3
SN74LVC2G241DCUR	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G241DCUT	VSSOP	DCU	8	250	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G241YZPR	DSBGA	YZP	8	3000	180.0	8.4	1.02	2.02	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74LVC2G241DCTRE4	SSOP	DCT	8	3000	182.0	182.0	20.0
74LVC2G241DCTRG4	SSOP	DCT	8	3000	182.0	182.0	20.0
74LVC2G241DCUTG4	VSSOP	DCU	8	250	202.0	201.0	28.0
SN74LVC2G241DCTR	SSOP	DCT	8	3000	190.0	190.0	30.0
SN74LVC2G241DCUR	VSSOP	DCU	8	3000	180.0	180.0	18.0
SN74LVC2G241DCUT	VSSOP	DCU	8	250	180.0	180.0	18.0
SN74LVC2G241YZPR	DSBGA	YZP	8	3000	182.0	182.0	20.0



4220784/D 10/2025

NOTES:

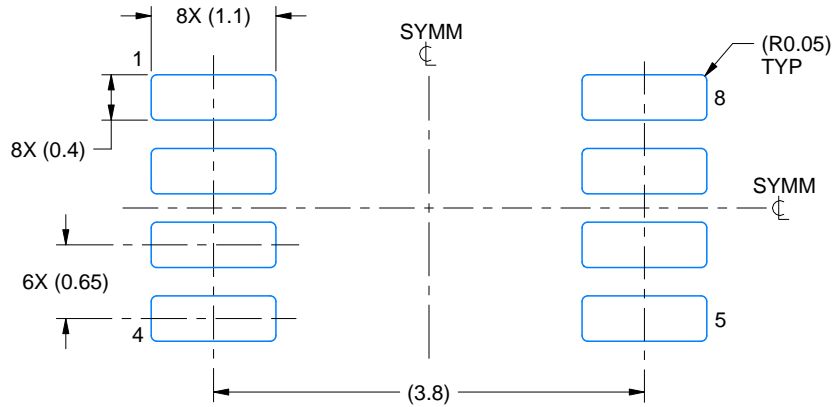
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

EXAMPLE BOARD LAYOUT

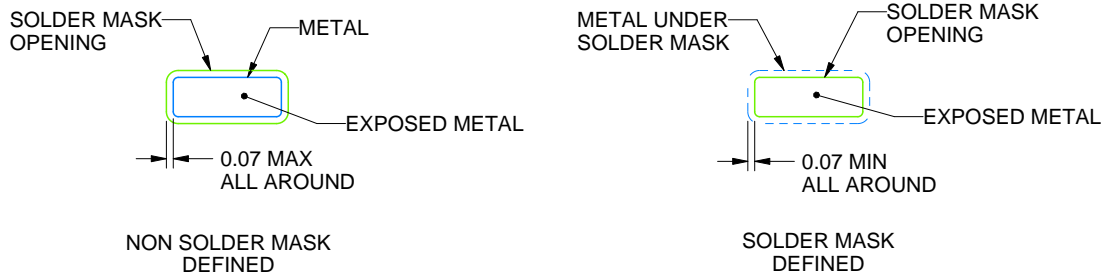
DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4220784/D 10/2025

NOTES: (continued)

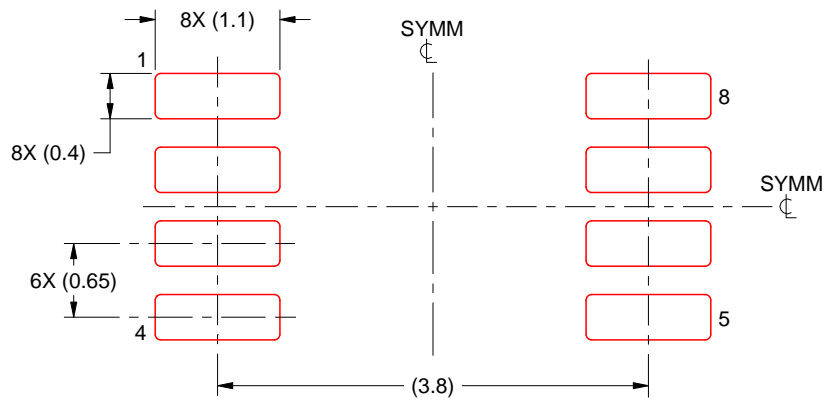
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE

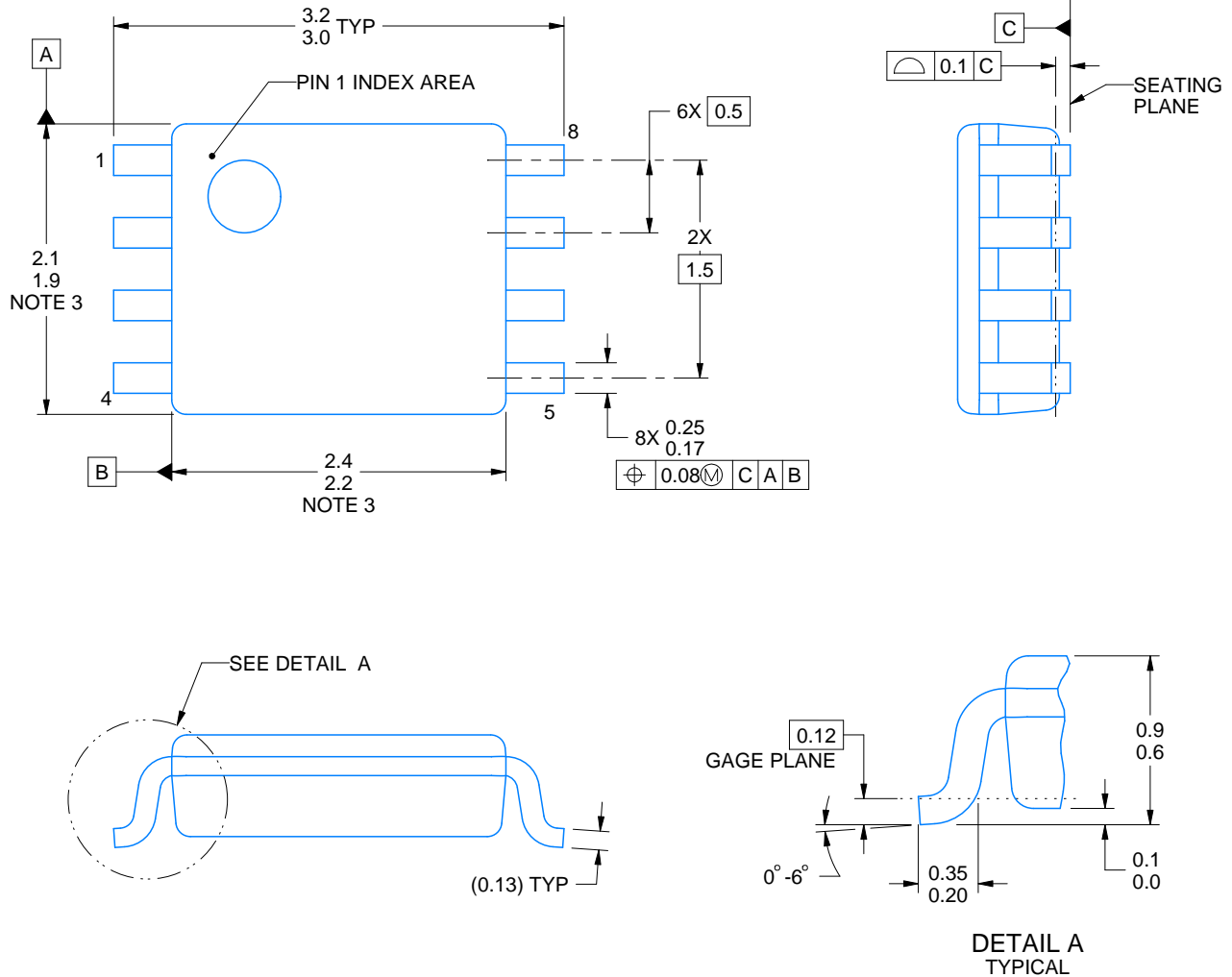


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4220784/D 10/2025

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



4225266/A 09/2014

NOTES:

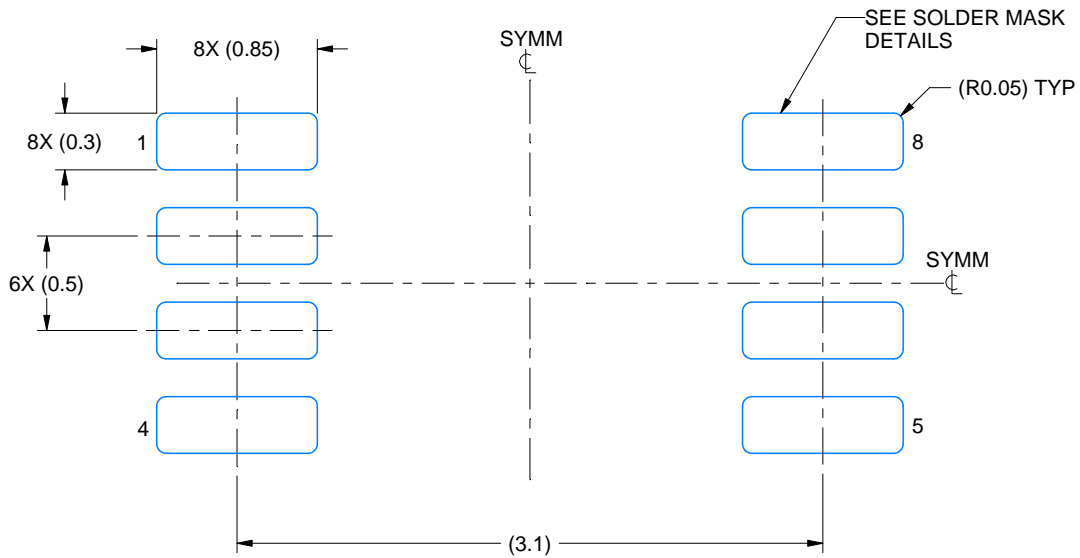
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.

EXAMPLE BOARD LAYOUT

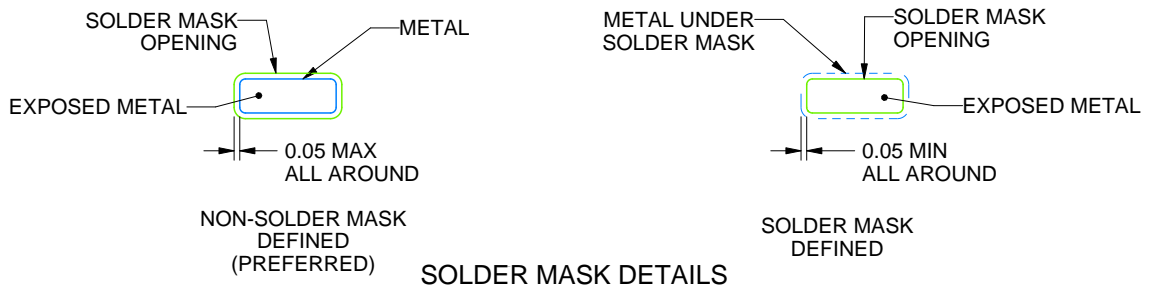
DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



4225266/A 09/2014

NOTES: (continued)

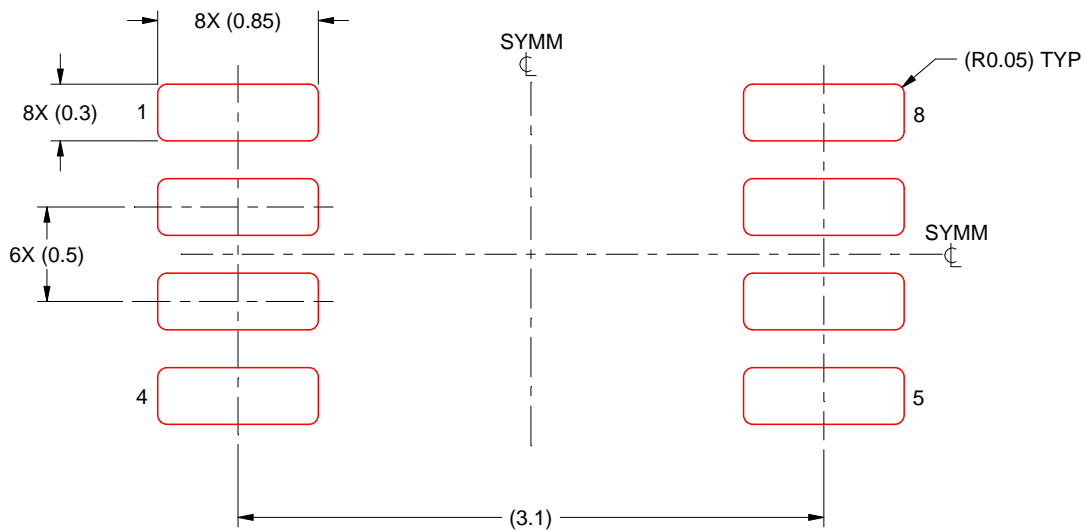
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



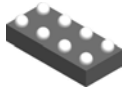
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

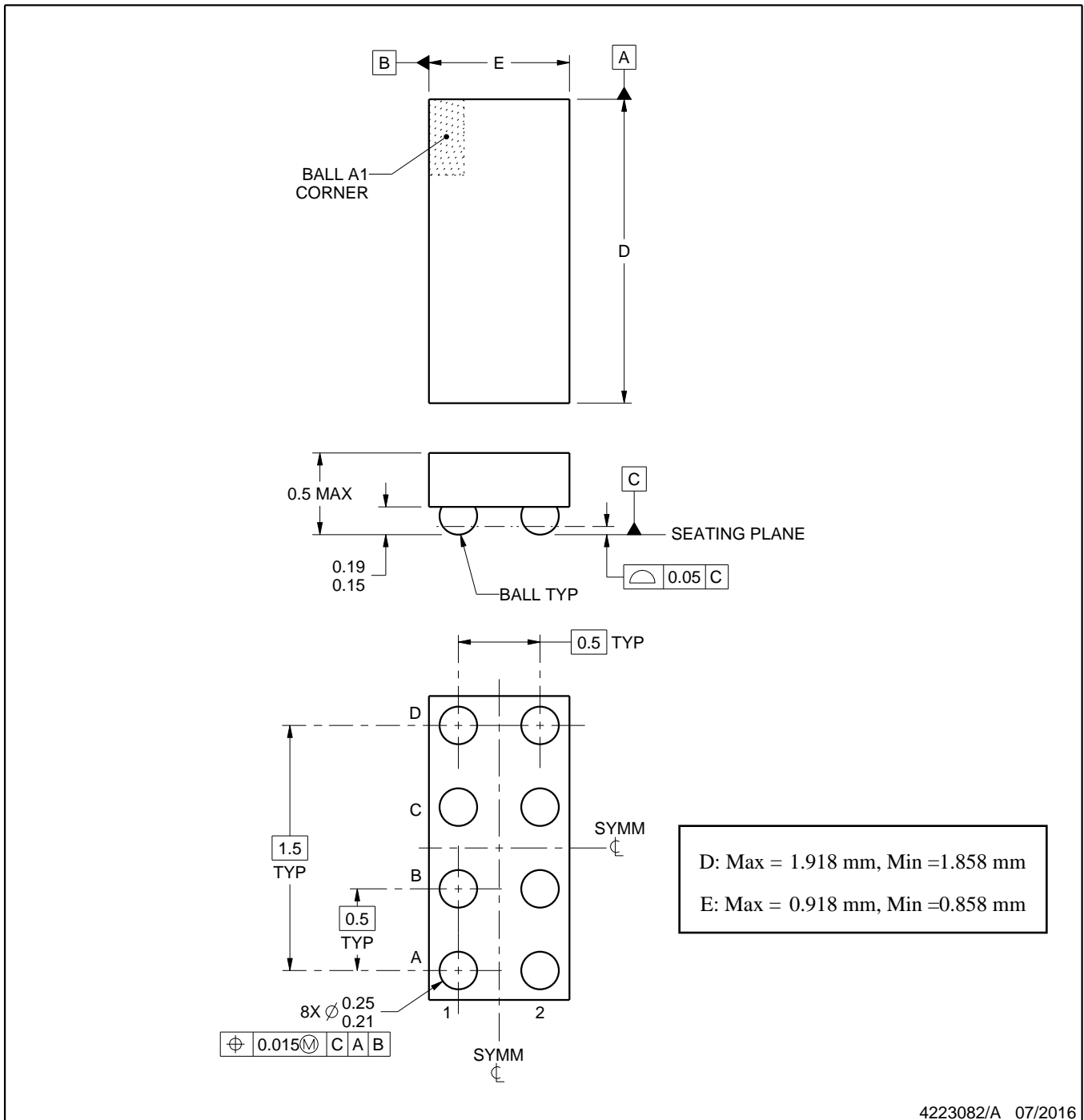
YZP0008



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4223082/A 07/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4223082/A 07/2016

NOTES: (continued)

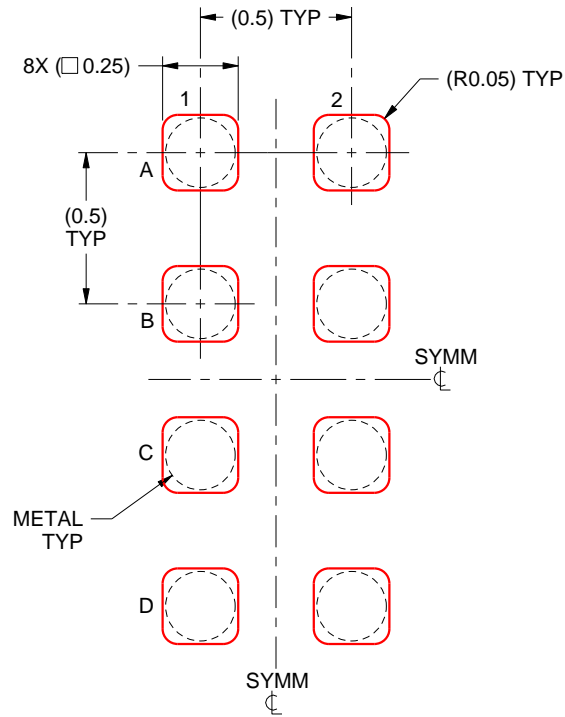
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4223082/A 07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、[TI の総合的な品質ガイドライン](#)、[ti.com](#) または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2026, Texas Instruments Incorporated

最終更新日 : 2025 年 10 月