SN74LVC2G66 デュアル双方向アナログ・スイッチ

1 特長

- テキサス・インスツルメンツのNanoFree™パッケージで供給
- 1.65V～5.5VのV_{CC}で動作
- 5.5Vまでの入力電圧に対応
- 最大t_{pd} 0.8ns (3.3V時)
- 高いオン/オフ出力電圧比
- 高度な線形性
- 高速、通常0.5ns (V_{CC} = 3V、C_L = 50pF)
- レール・ツー・レール入出力
- オン状態での低い抵抗、通常≉6Ω (V_{CC} = 4.5V)
- JESD 78, Class II準拠で100mA超のラッチアップ性能

2 アプリケーション

- ワイヤレス・デバイス
- オーディオおよびビデオ信号のルーティング
- ポータブル・コンピュータ
- ウェアラブル・デバイス
- 信号ゲーティング、チョッピング、変調または復調(モデム)
- アナログ/デジタルおよびデジタル/アナログ変換システム用の信号多重化

3 概要

このデュアル双方向アナログ・スイッチは、1.65V～5.5VのV_{CC}で動作するよう設計されています。

SN74LVC2G66は、アナログとデジタルの両方の信号を扱うことができます。SN74LVC2G66デバイスは、最高5.5V (ピーク)までの振幅の信号を、どちらの方向にも転送できます。

NanoFreeパッケージ技術はICパッケージの概念における主要なブレークスルーであり、ダイをパッケージとして使用します。

それぞれのスイッチ・セクションには、独自のイネーブル入力制御(C)が存在します。CにHIGHレベルの電圧が印加されると、対応するスイッチ・セクションがオンになります。

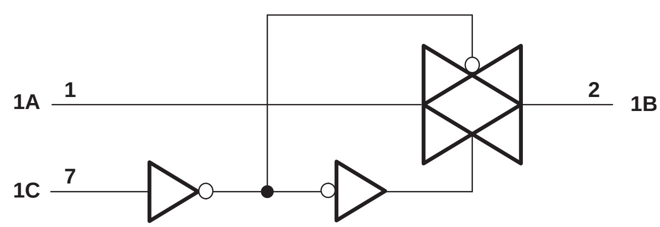
信号ゲーティング、チョッピング、変調または復調(モデム)、およびアナログ/デジタルやデジタル/アナログ変換システム用の信号多重化などのアプリケーションに使用できます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
SN74LVC2G66DCT	SSOP (8)	2.95mm×2.80mm
SN74LVC2G66DCU	VSSOP (8)	2.30mm×2.00mm
SN74LVC2G66YZP	DSBGA (8)	1.91mm×0.91mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

各スイッチの論理図(正論理)



One of Two Switches

目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision M (May 2018) から Revision N に変更 — **Page**

- Changed the YZP pin configuration 3

Revision L (September 2015) から Revision M に変更 — **Page**

- Updated pinout image and the *Pin Function* table 3
- Changed pin 3 Name From: 1C To: 2C 3
- Changed the *Thermal Information* table for the DCT package 5

Revision K (January 2014) から Revision L に変更 — **Page**

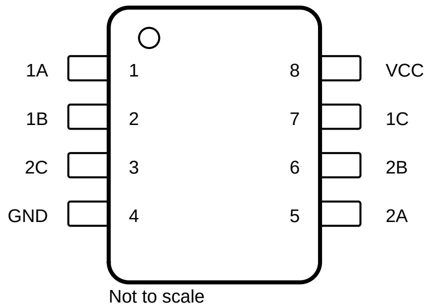
- 「*アプリケーション*」セクション、「*製品情報*」表、「*ピン構成および機能*」セクション、「*ESD定格*」表、「*代表的特性*」セクション、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加 1
- Added *Thermal Information* table 5

Revision J (December 2011) から Revision K に変更 — **Page**

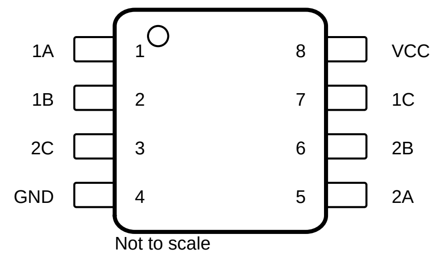
- 新しいTIデータシート・フォーマットにドキュメントを更新 - 仕様変更なし 1
- 「*注文情報*」表を削除 1

5 Pin Configuration and Functions

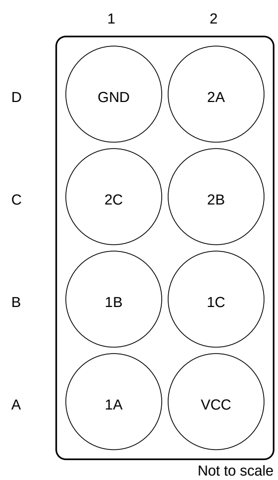
**DCT Package
8-Pin SSOP
Top View**



**DCU Package
8-Pin VSSOP
Top View**



**YZP Package
8-Pin DSBGA
Bottom View**



See mecahnical drawings for dimensions.

Pin Functions

PIN			I/O	DESCRIPTION
NAME	DCT DCU	YZP		
1A	1	A1	I/O	Bidirectional signal to be switched
1B	2	B1	I/O	Bidirectional signal to be switched
2C	3	C1	I	Controls the switch (L = OFF, H = ON)
2A	5	D2	I/O	Bidirectional signal to be switched
2B	6	C2	I/O	Bidirectional signal to be switched
1C	7	B2	I	Controls the switch (L = OFF, H = ON)
GND	4	D1	—	Ground pin
V_{CC}	8	A2	—	Power pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage[2]		–0.5	6.5	V
V_I	Input voltage[2][3]		–0.5	6.5	V
V_O	Switch I/O voltage[2][3][4]		–0.5	V_{CC} + 0.5	V
I_{IK}	Control input clamp current	V_I < 0		–50	mA
$I_{I/OK}$	I/O port diode current	$V_{I/O}$ < 0 or $V_{I/O}$ > V_{CC}		–50	mA
I_T	On-state switch current	$V_{I/O}$ = 0 to V_{CC}		±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) This value is limited to 5.5 V maximum.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

See [1].

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.65	5.5	V
$V_{I/O}$	I/O port voltage		0	V_{CC}	V
V_{IH}	High-level input voltage, control input	V_{CC} = 1.65 V to 1.95 V	V_{CC} × 0.65		V
		V_{CC} = 2.3 V to 2.7 V	V_{CC} × 0.7		
		V_{CC} = 3 V to 3.6 V	V_{CC} × 0.7		
		V_{CC} = 4.5 V to 5.5 V	V_{CC} × 0.7		
V_{IL}	Low-level input voltage, control input	V_{CC} = 1.65 V to 1.95 V		V_{CC} × 0.35	V
		V_{CC} = 2.3 V to 2.7 V		V_{CC} × 0.3	
		V_{CC} = 3 V to 3.6 V		V_{CC} × 0.3	
		V_{CC} = 4.5 V to 5.5 V		V_{CC} × 0.3	
V_I	Control input voltage		0	5.5	V
Δt/Δv	Input transition rise or fall time	V_{CC} = 1.65 V to 1.95 V		20	ns/V
		V_{CC} = 2.3 V to 2.7 V		20	
		V_{CC} = 3 V to 3.6 V		10	
		V_{CC} = 4.5 V to 5.5 V		10	
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.4 Thermal Information

THERMAL METRIC(1)		SN74LVC2G66			UNIT
		DCT (SSOP)	DCU (VSSOP)	YZP (DSBGA)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	186.1	204.4	102	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	116.5	77	—	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	98.6	83.2	—	°C/W
ψ_{JT}	Junction-to-top characterization parameter	42.2	7.1	—	°C/W
ψ_{JB}	Junction-to-board characterization parameter	97.6	82.7	—	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP(1)	MAX	UNIT
r_{on}	ON-state switch resistance	$V_I = V_{CC}$ or GND, $V_C = V_{IH}$ (see Figure 3 and Figure 1)	I_S = 4 mA	1.65 V		12.5	30	Ω
			I_S = 8 mA	2.3 V		9	20	
			I_S = 24 mA	3 V		7.5	15	
			I_S = 32 mA	4.5 V		6	10	
$r_{on(p)}$	Peak ON-state resistance	$V_I = V_{CC}$ to GND, $V_C = V_{IH}$ (see Figure 3 and Figure 1)	I_S = 4 mA	1.65 V		85	120(1)	Ω
			I_S = 8 mA	2.3 V		22	30(1)	
			I_S = 24 mA	3 V		12	20	
			I_S = 32 mA	4.5 V		7.5	15	
Δr_{on}	Difference of ON-state resistance between switches	$V_I = V_{CC}$ to GND, $V_C = V_{IH}$ (see Figure 3 and Figure 1)	I_S = 4 mA	1.65 V			7	Ω
			I_S = 8 mA	2.3 V			5	
			I_S = 24 mA	3 V			3	
			I_S = 32 mA	4.5 V			2	
$I_{S(off)}$	OFF-state switch leakage current	$V_I = V_{CC}$ and V_O = GND or V_I = GND and $V_O = V_{CC}$, $V_C = V_{IL}$ (see Figure 4)		5.5 V			±1	µA
							±0.1(1)	
$I_{S(on)}$	ON-state switch leakage current	$V_I = V_{CC}$ or GND, $V_C = V_{IH}$, V_O = Open (see Figure 5)		5.5 V			±1	µA
							±0.1(1)	
I_I	Control input current	$V_C = V_{CC}$ or GND		5.5 V			±1	µA
							±0.1(1)	
I_{CC}	Supply current	$V_C = V_{CC}$ or GND		5.5 V			10	µA
							1(1)	
ΔI_{CC}	Supply-current change	$V_C = V_{CC} – 0.6$ V		5.5 V			500	µA
C_{ic}	Control input capacitance			5 V		3.5		pF
$C_{io(off)}$	Switch input / output capacitance			5 V		6		pF
$C_{io(on)}$	Switch input / output capacitance			5 V		14		pF

(1) T_A = 25°C

6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd} (1)	A or B	B or A		2		1.2		0.8		0.6	ns
t_{en} (2)	C	A or B	2.3	10	1.6	5.6	1.5	4.4	1.3	3.9	ns
t_{dis} (3)	C	A or B	2.5	10.5	1.2	6.9	2	7.2	1.1	6.3	ns

(1) t_{PLH} and t_{PHL} are the same as t_{pd}. The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
(2) t_{PZL} and t_{PZH} are the same as t_{en}.
(3) t_{PLZ} and t_{PHZ} are the same as t_{dis}.

6.7 Analog Switch Characteristics

T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	TYP	UNIT
Frequency response (switch on)	A or B	B or A	C_L = 50 pF, R_L = 600 Ω, f_{in} = sine wave (see Figure 6)	1.65 V	35	MHz
				2.3 V	120	
				3 V	175	
				4.5 V	195	
			C_L = 5 pF, R_L = 50 Ω, f_{in} = sine wave (see Figure 6)	1.65 V	>300	
				2.3 V	>300	
				3 V	>300	
				4.5 V	>300	
Crosstalk(1) (between switches)	A or B	B or A	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Figure 7)	1.65 V	–58	dB
				2.3 V	–58	
				3 V	–58	
				4.5 V	–58	
			C_L = 5 pF, R_L = 50 Ω, f_{in} = 1 MHz (sine wave) (see Figure 7)	1.65 V	–42	
				2.3 V	–42	
				3 V	–42	
				4.5 V	–42	
Crosstalk (control input to signal output)	C	A or B	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (square wave) (see Figure 8)	1.65 V	35	mV
				2.3 V	50	
				3 V	70	
				4.5 V	100	
Feedthrough attenuation (switch off)	A or B	B or A	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Figure 9)	1.65 V	–58	dB
				2.3 V	–58	
				3 V	–58	
				4.5 V	–58	
			C_L = 5 pF, R_L = 50 Ω, f_{in} = 1 MHz (sine wave) (see Figure 9)	1.65 V	–42	
				2.3 V	–42	
				3 V	–42	
				4.5 V	–42	

(1) Adjust f_{in} voltage to obtain 0 dBm at input.

Analog Switch Characteristics (continued)

T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	TYP	UNIT
Sine-wave distortion	A or B	B or A	C_L = 50 pF, R_L = 10 kΩ, f_{in} = 1 kHz (sine wave) (see Figure 10)	1.65 V	0.1%	
				2.3 V	0.025%	
				3 V	0.015%	
				4.5 V	0.01%	
			C_L = 50 pF, R_L = 10 kΩ, f_{in} = 10 kHz (sine wave) (see Figure 10)	1.65 V	0.15%	
				2.3 V	0.025%	
				3 V	0.015%	
				4.5 V	0.01%	

6.8 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	V_{CC} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	f = 10 MHz	8	9	9.5	11	pF

6.9 Typical Characteristics

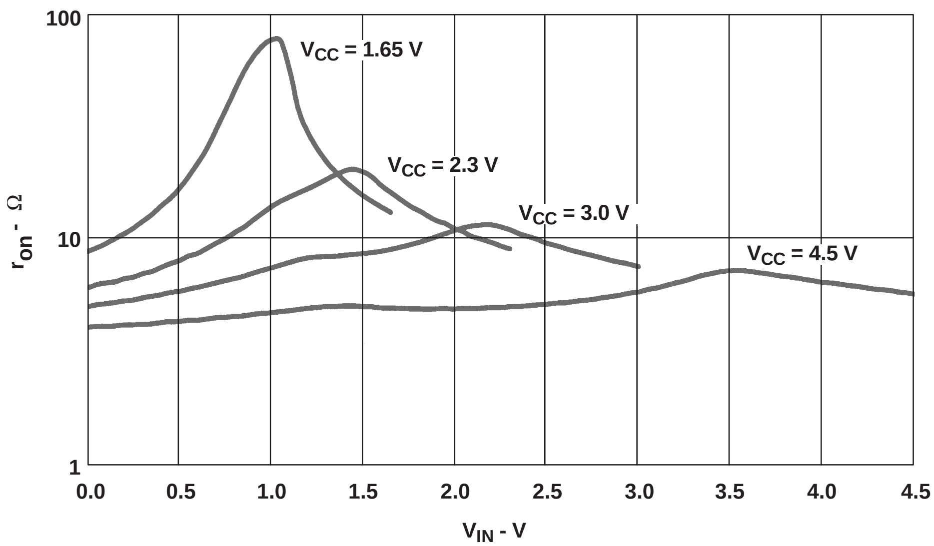
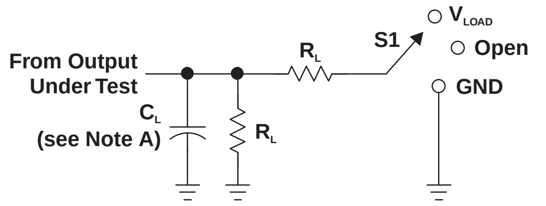


Figure 1. Typical r_{on} as a Function of Input Voltage (V_I) for V_I = 0 to V_{CC}

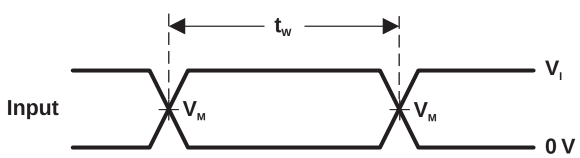
7 Parameter Measurement Information



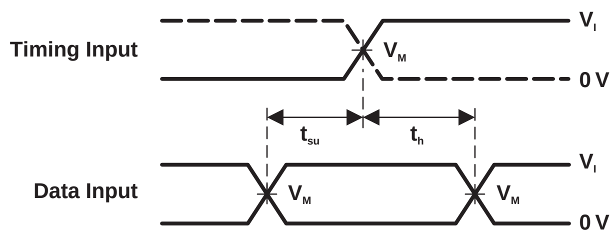
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

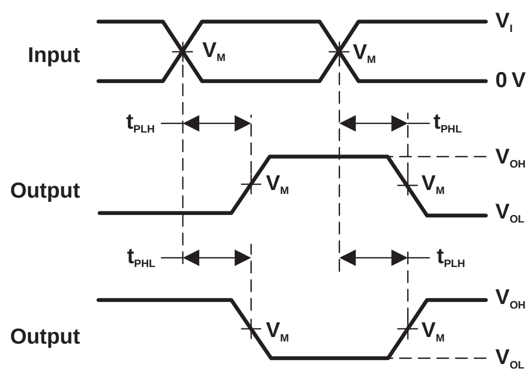
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V



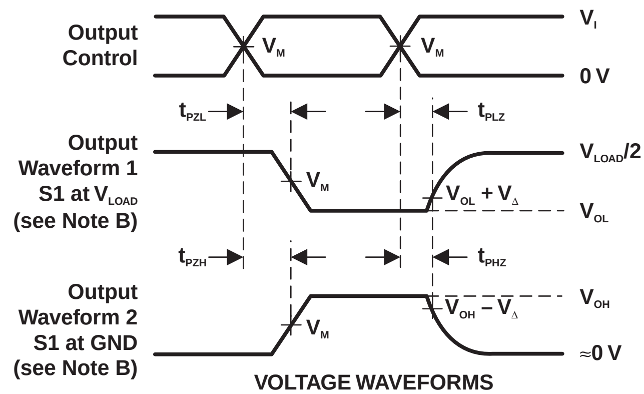
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

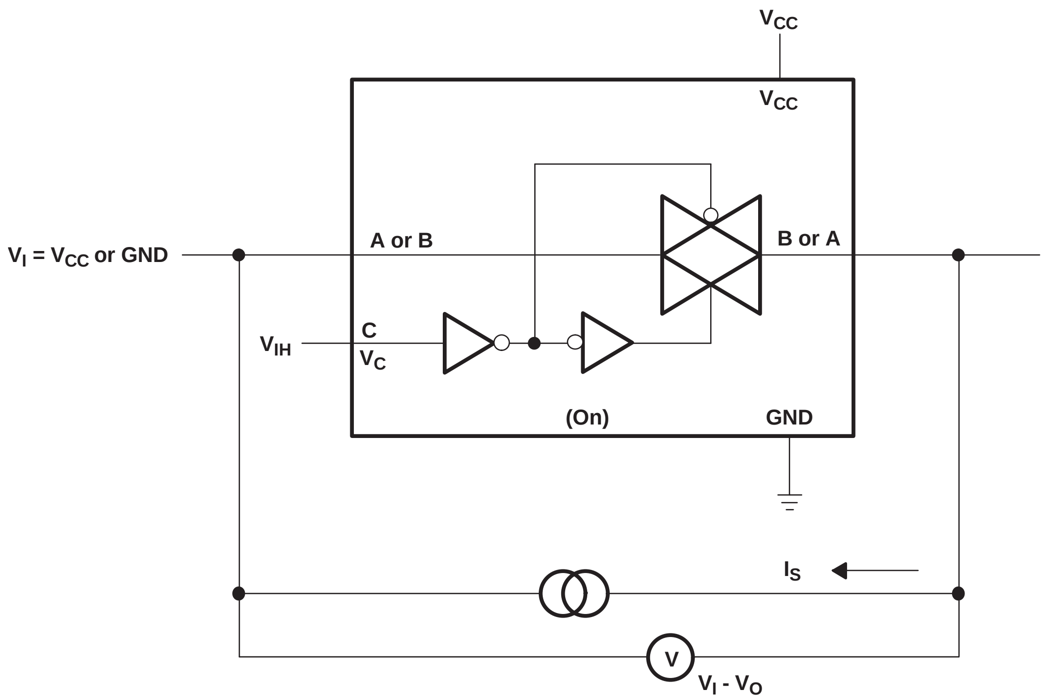


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators have the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

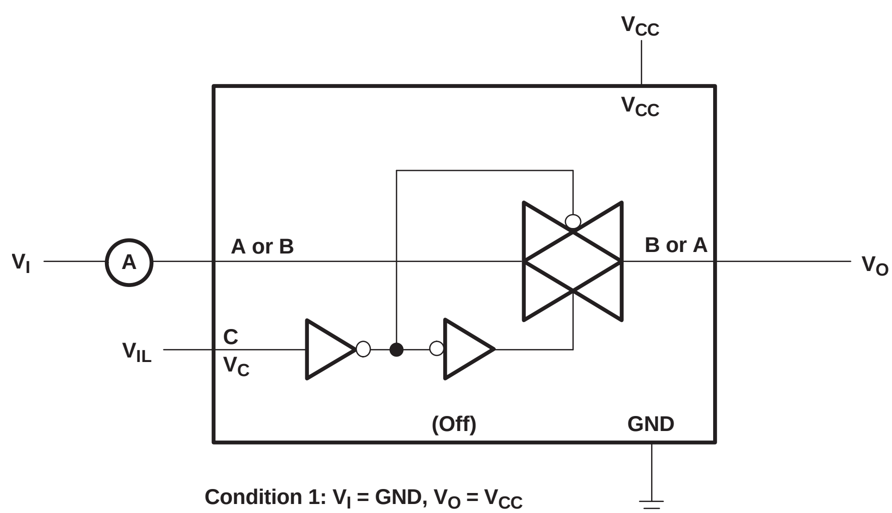
Figure 2. Load Circuit and Voltage Waveforms

Parameter Measurement Information (continued)



$$r_{on} = \frac{V_I - V_O}{I_S}\ \Omega$$

Figure 3. ON-State Resistance Test Circuit



Condition 1: V_I = GND, V_O = V_{CC}
Condition 2: V_I = V_{CC}, V_O = GND

Figure 4. OFF-State Switch Leakage-Current Test Circuit

Parameter Measurement Information (continued)

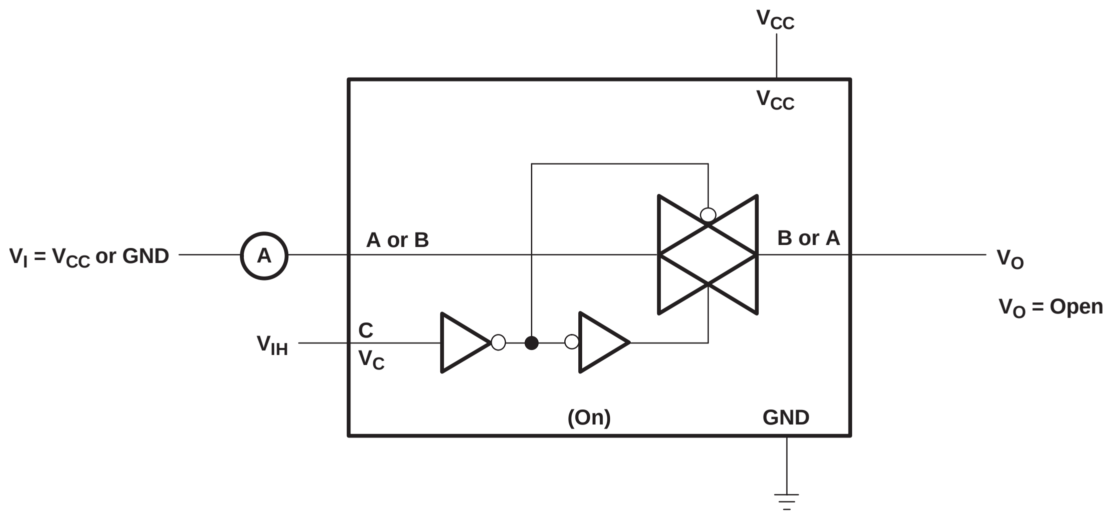


Figure 5. ON-State Leakage-Current Test Circuit

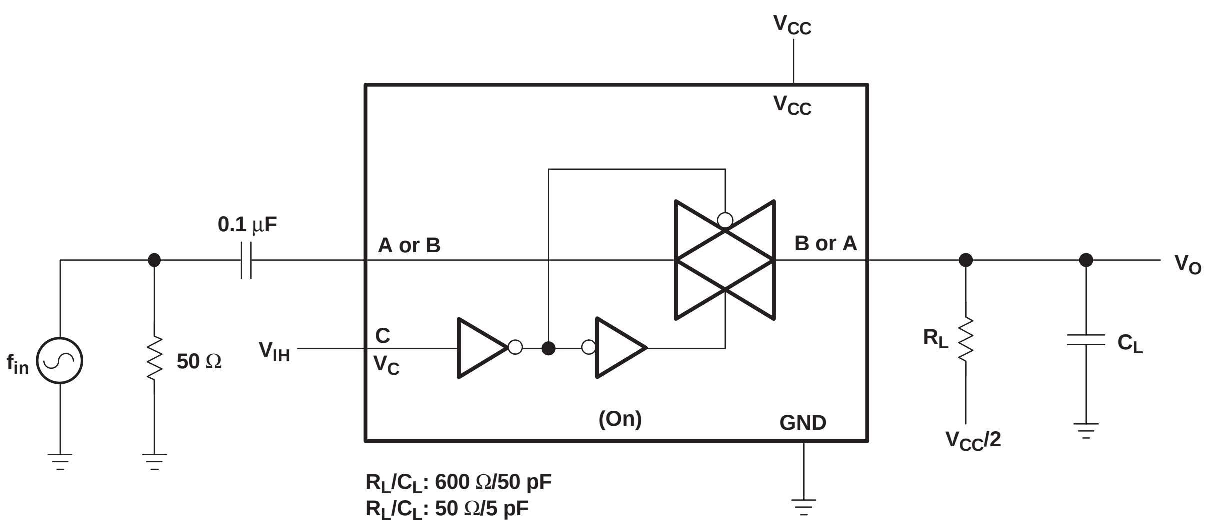


Figure 6. Frequency Response (Switch On)

Parameter Measurement Information (continued)

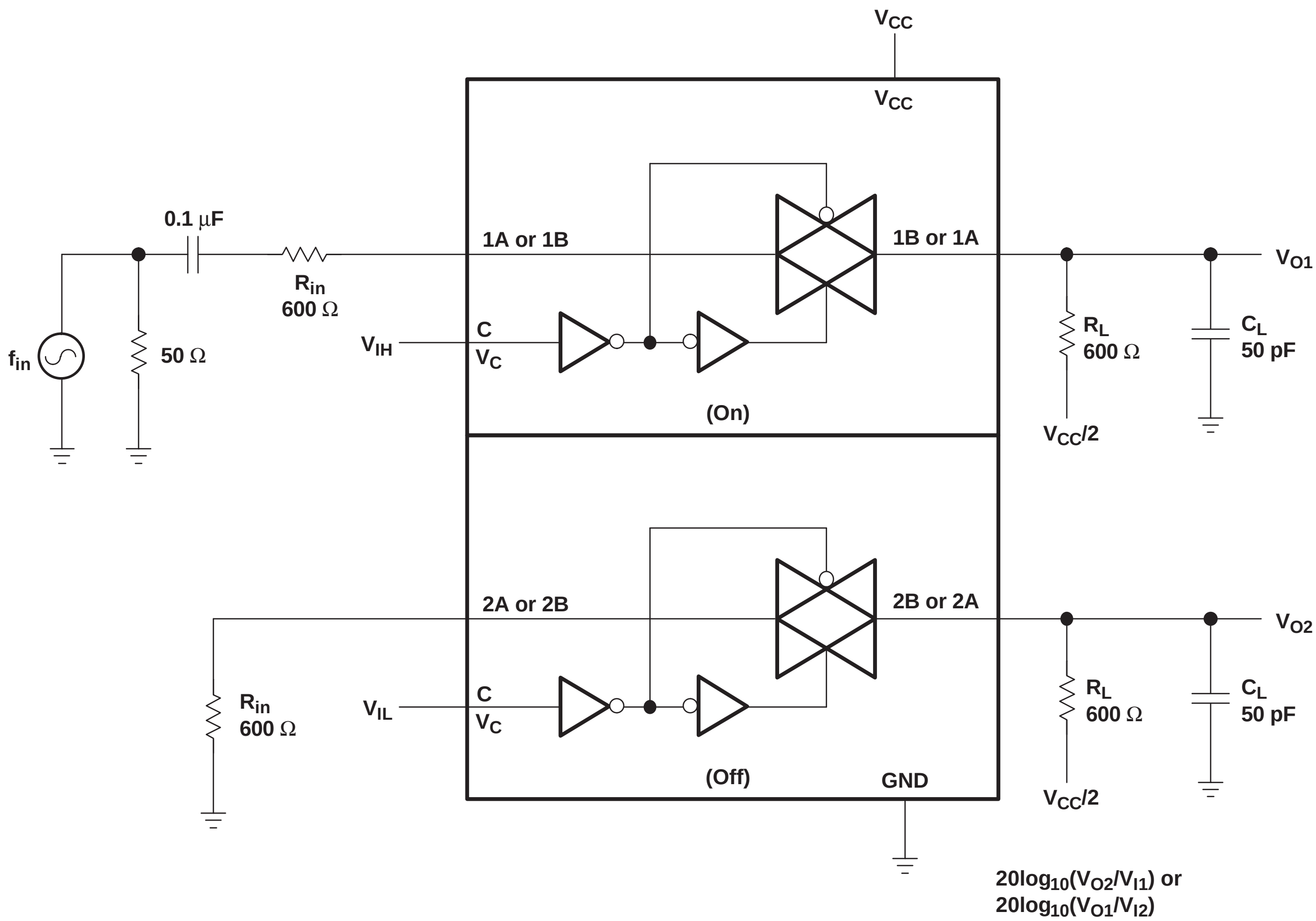


Figure 7. Crosstalk (Between Switches)

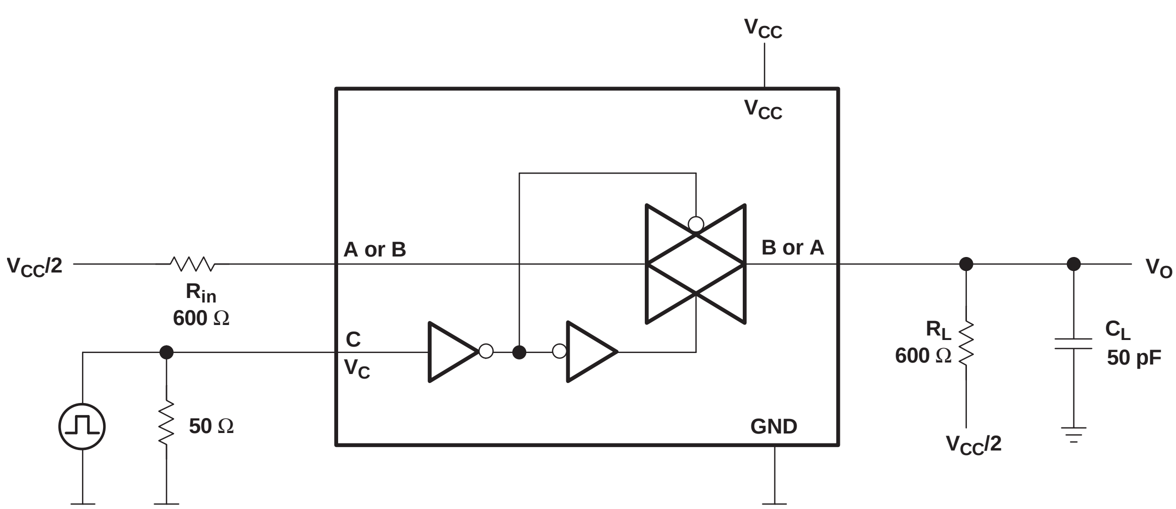


Figure 8. Crosstalk (Control Input, Switch Output)

Parameter Measurement Information (continued)

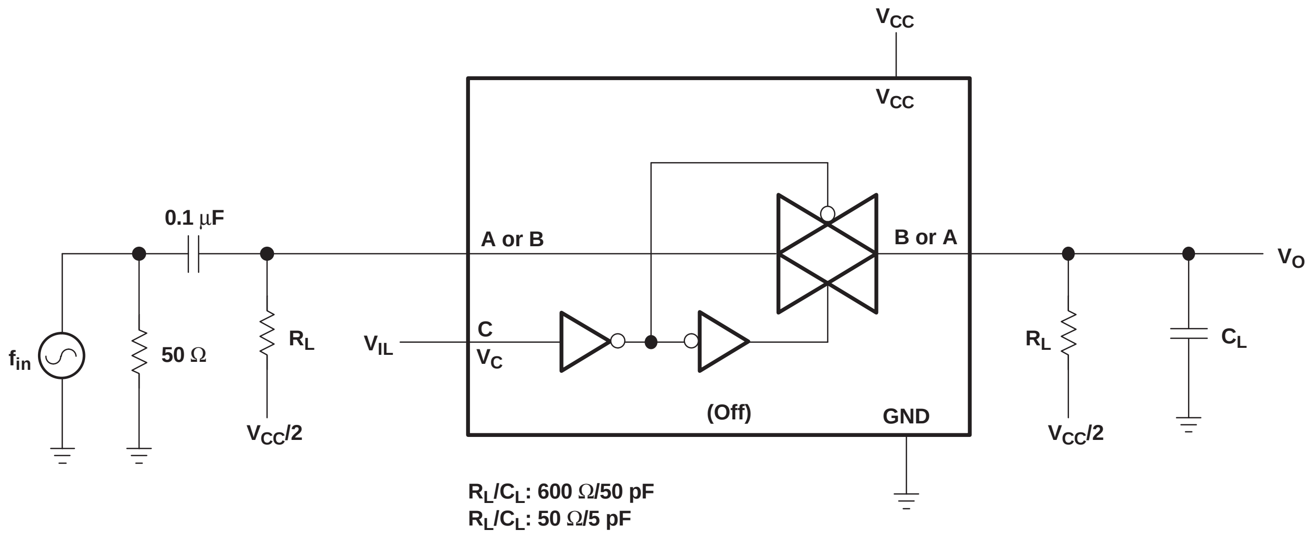


Figure 9. Feedthrough (Switch Off)

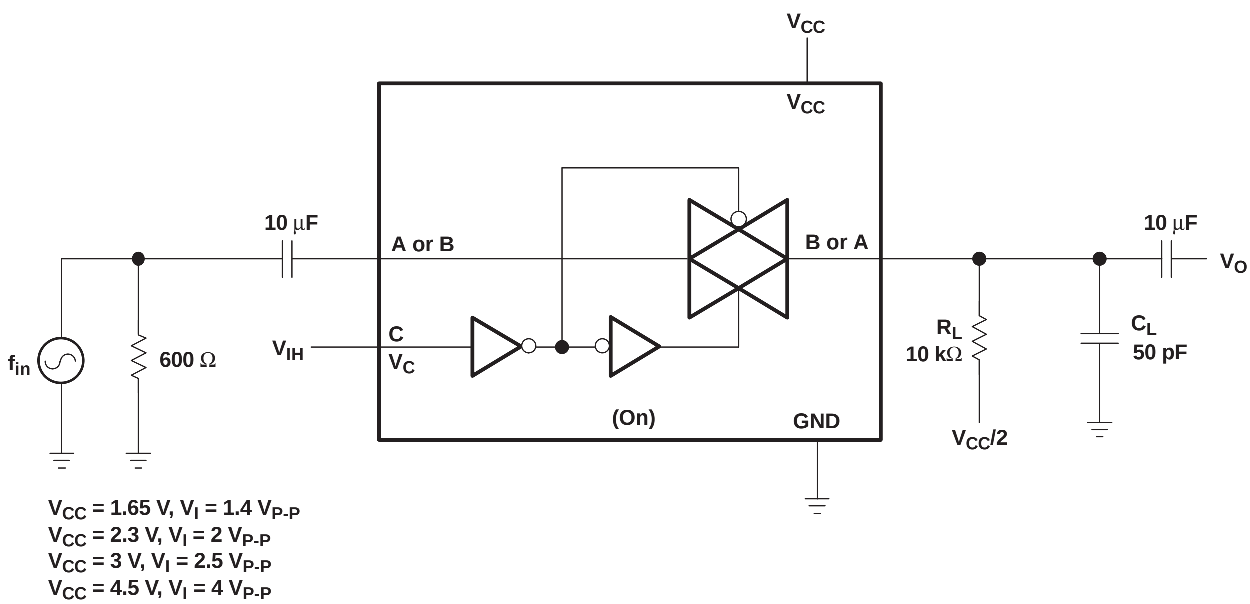


Figure 10. Sine-Wave Distortion

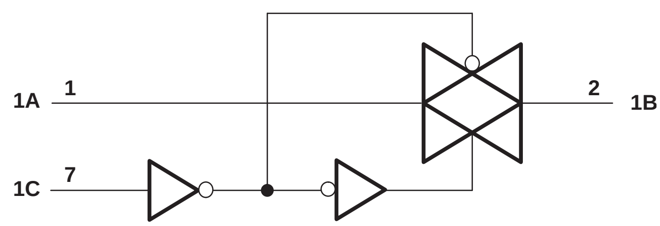
8 Detailed Description

8.1 Overview

This dual bilateral analog switch is designed for 1.65-V to 5.5-V V_{CC} operation. Robust LVC family technology allows this device to accept input voltages without connecting power to V_{CC}.

The SN74LVC2G66 device permits signals with amplitudes of up to 5.5 V (peak) to be transmitted in either direction. A high-level voltage applied to the control pin C enables the respective switch to begin propagating signals across the device. A low-level voltage disables this transmission. Each device incorporates two switches with independent control and operation.

8.2 Functional Block Diagram



One of Two Switches

8.3 Feature Description

Each switch section has its own enable-input control (C). A high-level voltage applied to C turns on the associated switch section. When C is this Signals can pass through A to B or B to A. Low ON-resistance of 6 Ω at 4.5-V V_{CC} is ideal for analog signal conditioning systems. The control signals can accept voltages up to 5.5 V without V_{CC} connected in the system. Combination of lower t_{pd} of 0.8 ns at 3.3 V and low enable and disable time make this part suitable for high-speed signal switching applications.

8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74LVC2G66.

Table 1. Function Table

CONTROL INPUT (C)	SWITCH
L	Off
H	On

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74LVC2G66 can be used in any situation where an Dual SPST switch would be used and a solid-state, voltage controlled version is preferred.

9.2 Typical Application

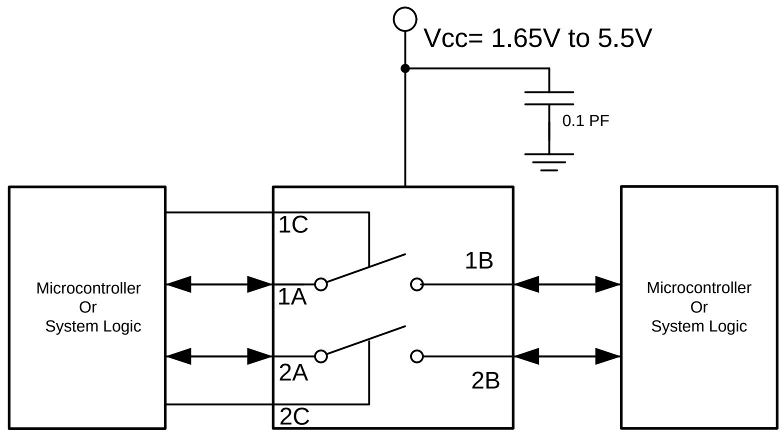


Figure 11. Typical Application Schematic

9.2.1 Design Requirements

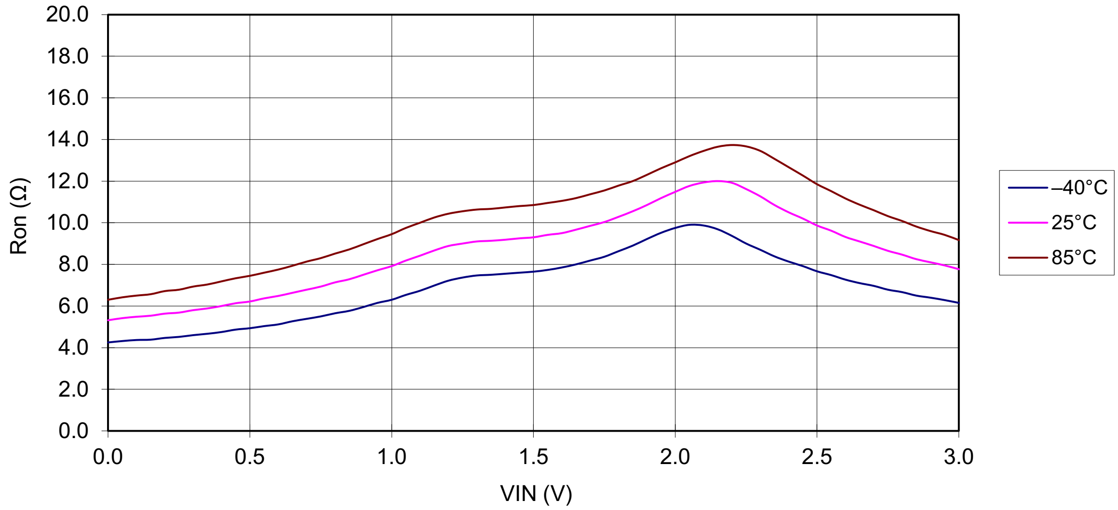
The SN74LVC2G66 allows on/off control of analog and digital signals with a digital control signal. All input signals should remain between 0 V and V_{CC} for optimal operation.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   – For rise time and fall time specifications, see Δt/Δv in the *Recommended Operating Conditions* table.
   – For specified high and low levels, see V_{IH} and V_{IL} in the *Recommended Operating Conditions* table.
   – Inputs and outputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
2. Recommended Output Conditions:
   – Load currents should not exceed ±50 mA.
3. Frequency Selection Criterion:
   – Maximum frequency tested is 150 MHz.
   – Added trace resistance or capacitance can reduce maximum frequency capability; use layout practices as directed in *Layout*.

Typical Application (continued)

9.2.3 Application Curve



Pin: A–B, V_{CC} = 3 V, I_S = 24 mA

Figure 12. r_{on} vs V_I

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-µF bypass capacitor is recommended. If there are multiple pins labeled V_{CC}, then a 0.01-µF or 0.022-µF capacitor is recommended for each V_{CC} because the VCC pins will be tied together internally. For devices with dual-supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1-µF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self–inductance of the trace — resulting in the reflection.

NOTE

Not all PCB traces can be straight, and so they will have to turn corners. Figure 13 shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

11.2 Layout Example

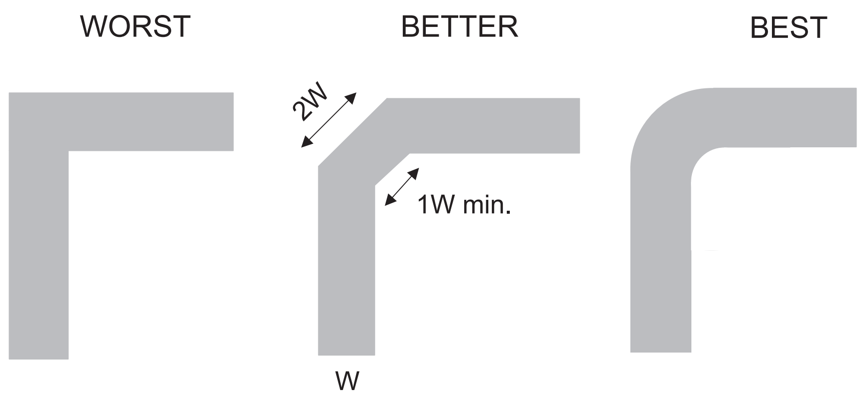


Figure 13. Trace Example

12 デバイスおよびドキュメントのサポート

12.1 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

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12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC2G66DCTR	Active	Production	SSOP (DCT) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C66 (R, Z)
SN74LVC2G66DCTR.A	Active	Production	SSOP (DCT) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C66 (R, Z)
SN74LVC2G66DCTR.B	Active	Production	SSOP (DCT) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C66 (R, Z)
SN74LVC2G66DCUR	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(66, C66Q, C66R) CZ
SN74LVC2G66DCUR.A	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(66, C66Q, C66R) CZ
SN74LVC2G66DCUR.B	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(66, C66Q, C66R) CZ
SN74LVC2G66DCURG4	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C66R
SN74LVC2G66DCURG4.B	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C66R
SN74LVC2G66DCUTE4	Active	Production	VSSOP (DCU) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C66R
SN74LVC2G66DCUTG4	Active	Production	VSSOP (DCU) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C66R
SN74LVC2G66DCUTG4.B	Active	Production	VSSOP (DCU) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C66R
SN74LVC2G66YZPR	Active	Production	DSBGA (YZP) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(C67, C6N)
SN74LVC2G66YZPR.B	Active	Production	DSBGA (YZP) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(C67, C6N)

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74LVC2G66 :

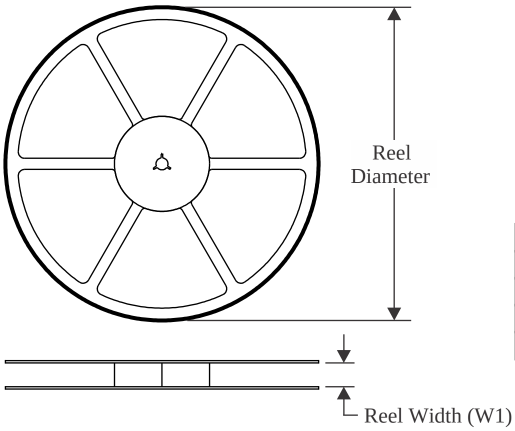
- Automotive : SN74LVC2G66-Q1

NOTE: Qualified Version Definitions:

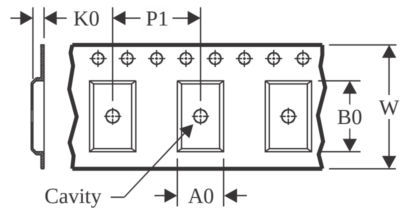
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

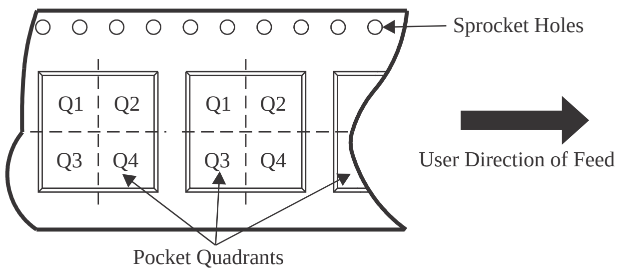


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

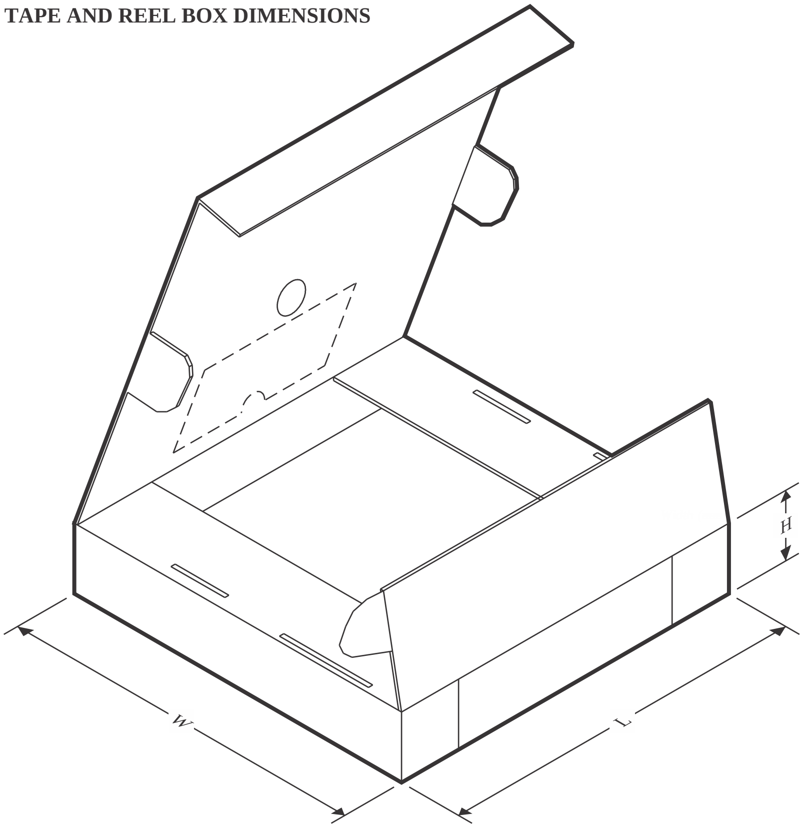
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

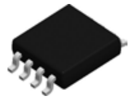
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC2G66DCTR	SSOP	DCT	8	3000	177.8	12.4	3.45	4.4	1.45	4.0	12.0	Q3
SN74LVC2G66DCTR	SSOP	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74LVC2G66DCUR	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G66DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G66DCUTG4	VSSOP	DCU	8	250	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G66YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

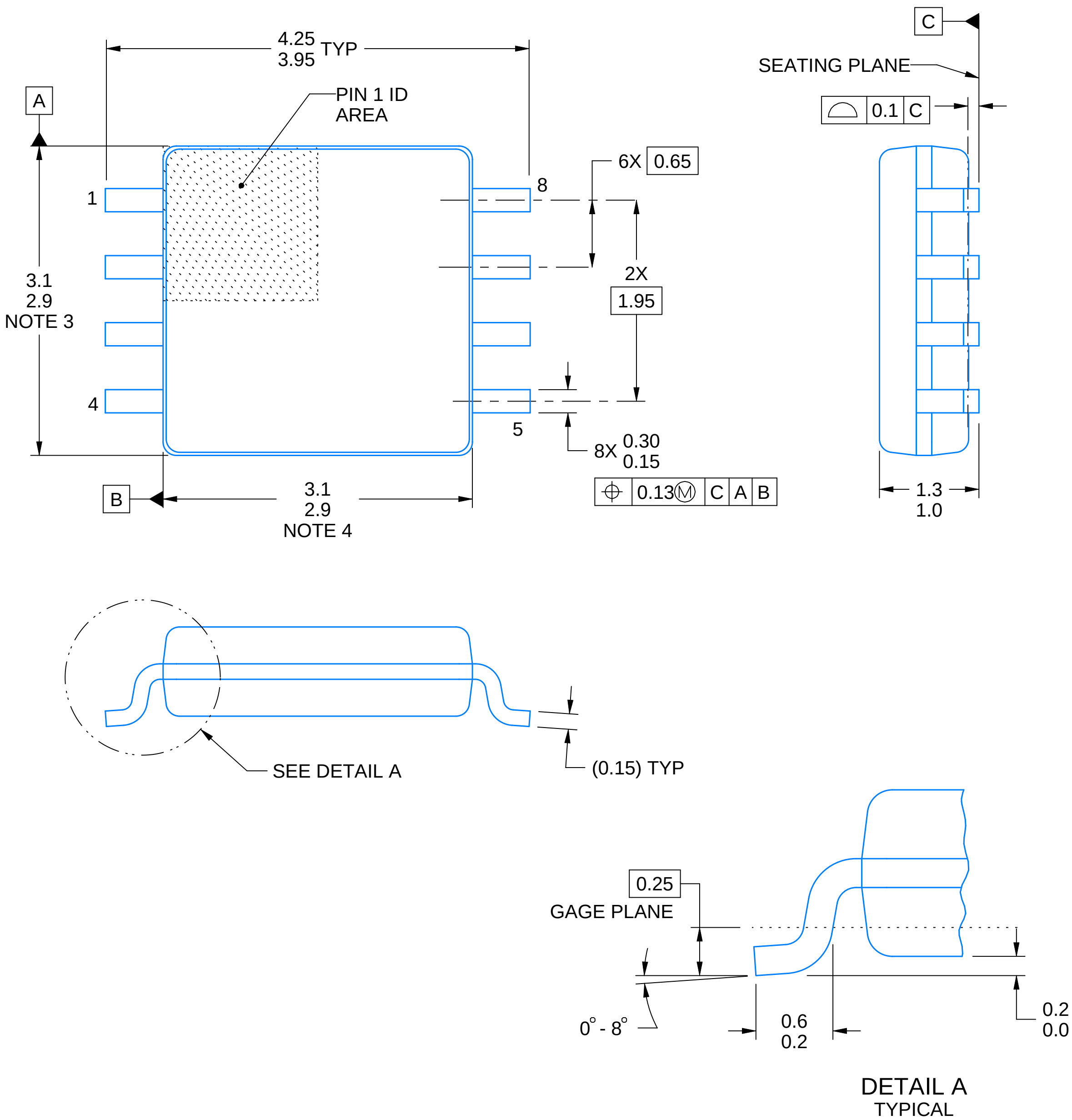
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC2G66DCTR	SSOP	DCT	8	3000	183.0	183.0	20.0
SN74LVC2G66DCTR	SSOP	DCT	8	3000	182.0	182.0	20.0
SN74LVC2G66DCUR	VSSOP	DCU	8	3000	180.0	180.0	18.0
SN74LVC2G66DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74LVC2G66DCUTG4	VSSOP	DCU	8	250	202.0	201.0	28.0
SN74LVC2G66YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0



PACKAGE OUTLINE

SSOP - 1.3 mm max height

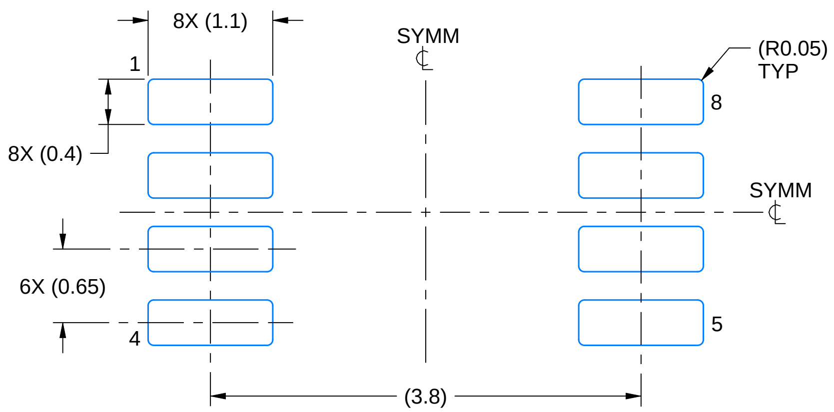
SMALL OUTLINE PACKAGE



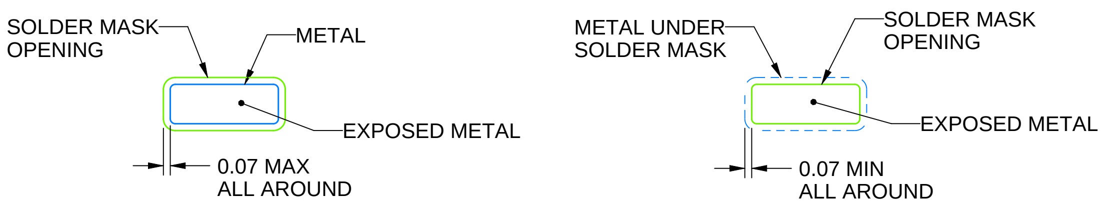
4220784/D 10/2025

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK DEFINED

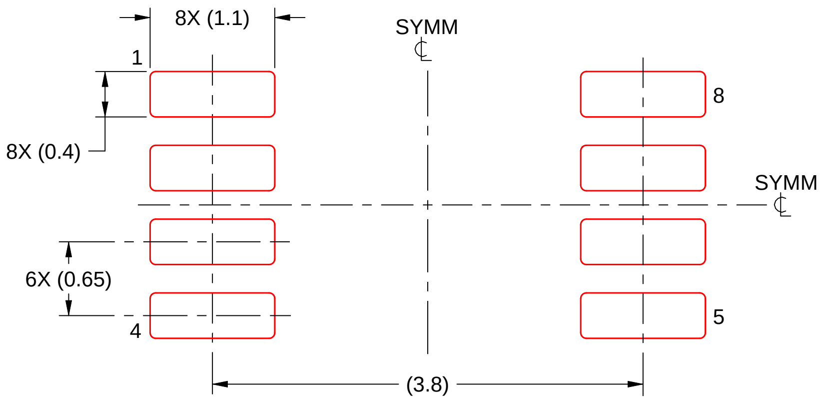
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220784/D 10/2025

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

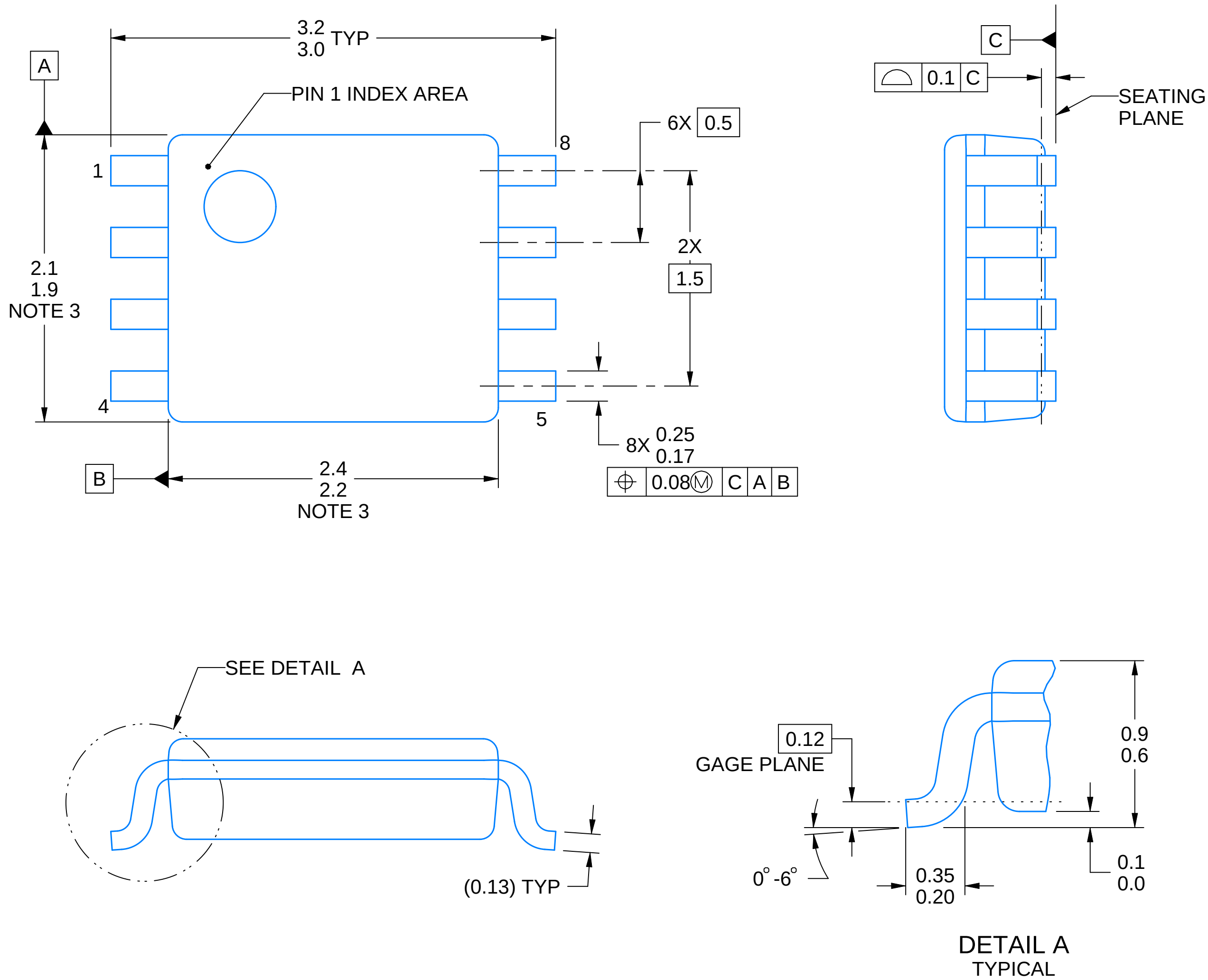


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4220784/D 10/2025

NOTES: (continued)

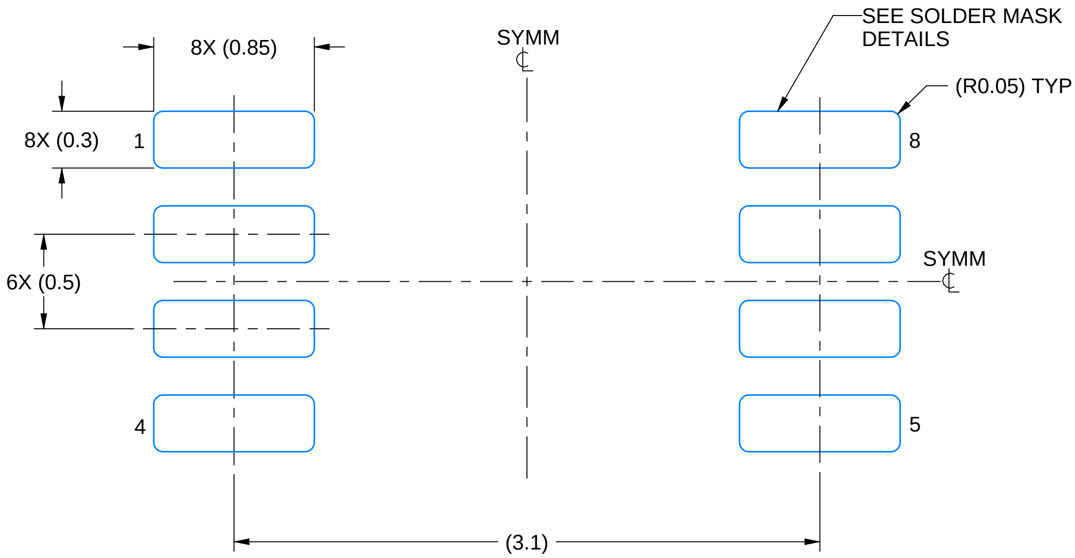
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



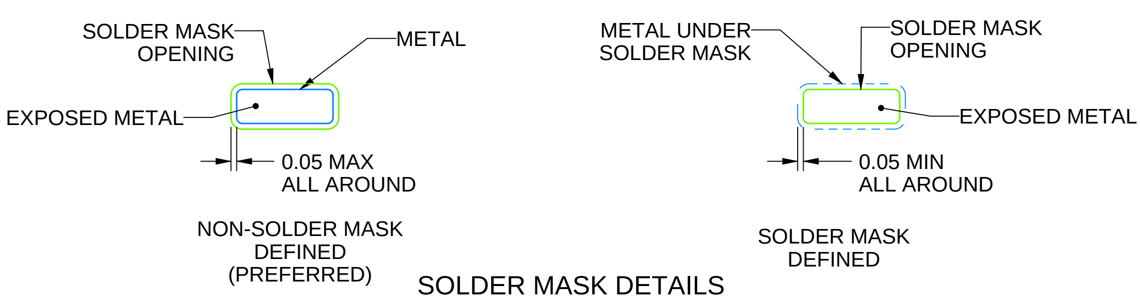
4225266/A 09/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

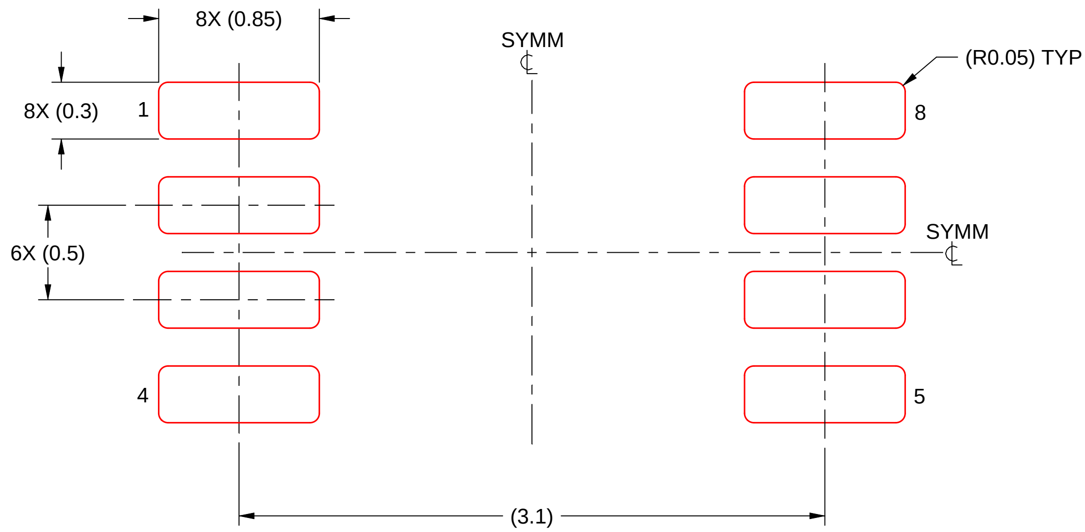


SOLDER MASK DETAILS

4225266/A 09/2014

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

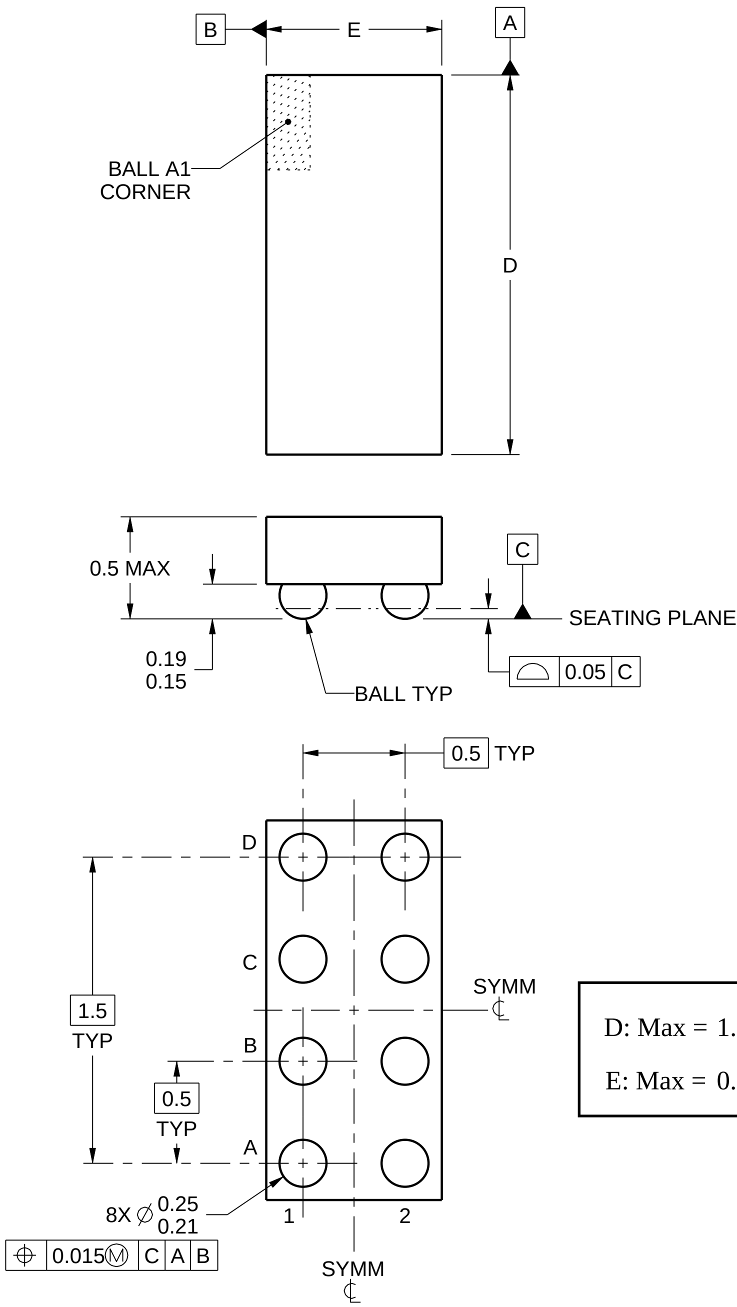


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



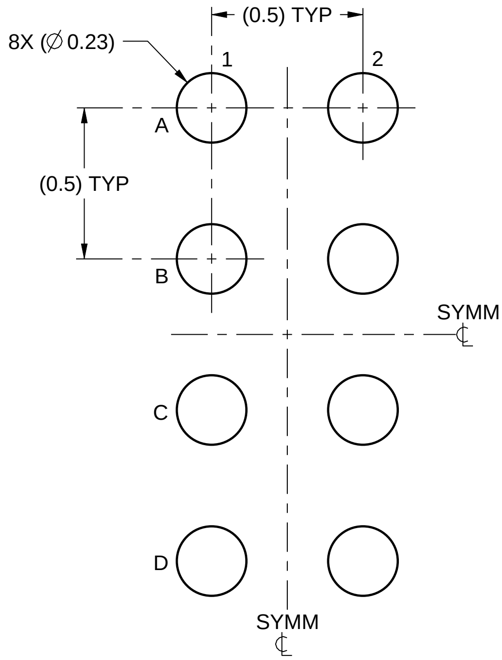
D: Max = 1.918 mm, Min =1.858 mm

E: Max = 0.918 mm, Min =0.858 mm

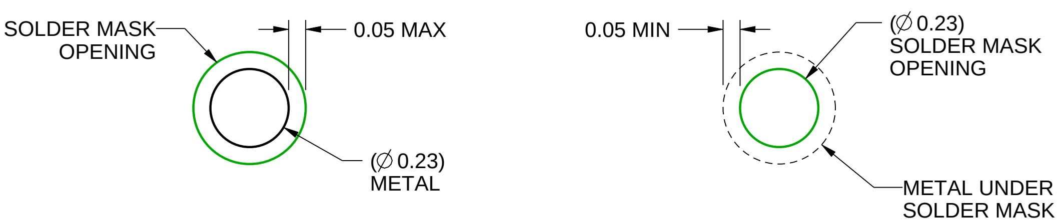
4223082/A 07/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X



NON-SOLDER MASK DEFINED (PREFERRED)

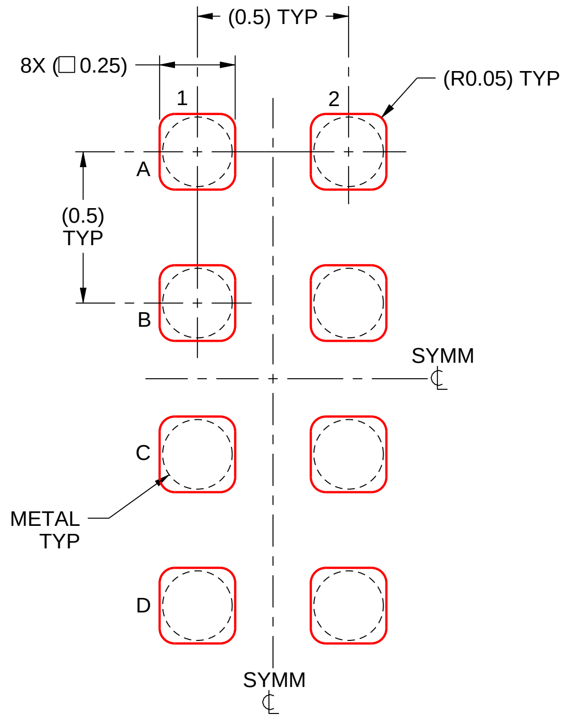
SOLDER MASK DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4223082/A 07/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4223082/A 07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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