SN75176A 差動バス・トランシーバ

1 特長

- 双方向トランシーバ
- ANSI 標準 EIA/TIA-422-B と ITU 勧告 V.11 を満たす、または超える性能
- ノイズの多い環境の、長いバスラインでのマルチポイントの伝送用に設計
- 3 ステートのドライバ / レシーバ出力
- 個別のドライバ / レシーバ・イネーブル
- 広い正および負の入力 / 出力バス電圧範囲
- ドライバ出力能力:±60mA (最大値)
- サーマル・シャットダウン保護
- ドライバの正電流制限と負電流制限
- レシーバの入力インピーダンス:12kΩ (最小値)
- レシーバの入力感度:±200mV
- レシーバの入力ヒステリシス:50mV (標準値)
- 5V 単一電源で動作
- 電力要件の低減

2 アプリケーション

- 低速 RS485 通信 (5Mbps 以下)
- 10Mbps には SN75176B を使用

3 概要

SN75176A 差動バス・トランシーバは、マルチポイント・バス伝送ライン上での双方向データ通信を目的として設計されたモノリシック IC です。平衡伝送ライン用に設計され、ANSI 標準 EIA/TIA-422-B および ITU 勧告 V.11 に準拠しています。

SN75176A は、3 ステート差動ライン・ドライバと差動入力ライン・レシーバを統合しており、どちらも 5V 単一電源で動作します。ドライバとレシーバはそれぞれアクティブ HIGH、アクティブ LOW のイネーブルを備えており、それらのイネーブルを外部で相互に接続することで、方向制御として機能させることができます。ドライバの差動出力とレシーバの差動入力は、差動入出力 (I/O) バス・ポートを構成するように内部で接続されています。これらのポートは、ドライバがディセーブルされている場合または VCC = 0 の場合、バスへの負荷を最小化するように設計されています。これらのポートは正負の同相電圧範囲が広いため、パーティライン・アプリケーションに適しています。

ドライバは、最大 60mA のシンクまたはソース電流負荷に対応するように設計されています。ドライバは、ライン・フォルト状態からの保護のために、正と負の電流制限とサーマル・シャットダウンを備えています。サーマル・シャットダウンは、約 150℃の接合部温度でトリガされるように設計されています。レシーバの最小入力インピーダンスは 12kΩ、入力感度は ±200mV、入力ヒステリシスは 50mV (標準値) です。

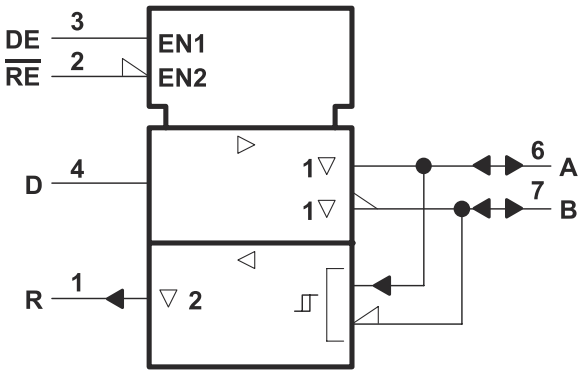
SN75176A は、SN75172 および SN75174 クワッド差動ライン・ドライバと SN75173 および SN75175 クワッド差動ライン・レシーバを採用した伝送ライン・アプリケーションで使用できます。

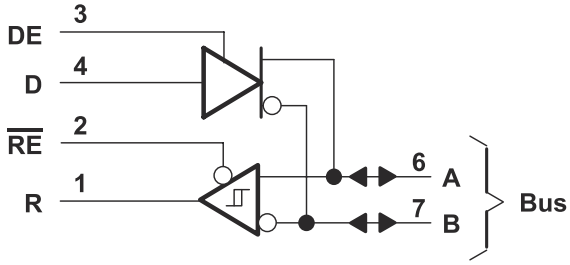
SN75176A は、0℃～70℃で動作が規定されています。

製品情報 (1)

部品番号	パッケージ (ピン)	本体サイズ (公称)
SN75176A	SOIC (8)	4.90mm × 3.91mm
	PDIP (8)	9.81mm × 6.35mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。





概略回路図

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4 Revision History

Changes from Revision B (January 2015) to Revision C (October 2022)	Page
• Deleted the *ESD Ratings* table	4
• Changed the *Thermal Information* table	4

Changes from Revision A (May 1995) to Revision B (January 2015)	Page
• 「アプリケーション」セクション、「製品情報」表、「端子機能」表、「ESD 定格」表、「熱に関する情報」表、「代表的特性」セクション、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加	1
• 「注文情報」表を削除	1

5 Pin Configuration and Functions

D OR P PACKAGE
(TOP VIEW)

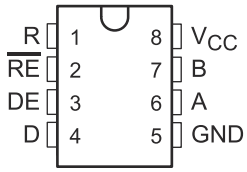


表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
R	1	O	Logic Data Output from RS-485 Receiver
$\overline{RE}$	2	I	Receive Enable (active low)
DE	3	I	Driver Enable (active high)
D	4	I	Logic Data Input to RS-485 Driver
GND	5	—	Device Ground Pin
A	6	I/O	RS-422 or RS-485 Data Line
B	7	I/O	RS-422 or RS-485 Data Line
V_{CC}	8	—	Power Input. Connect to 5-V Power Source.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply Voltage(2)		7	V
	Voltage range at any bus terminal	–10	15	V
V_I	Enable input voltage		5.5	V
	Continuous Total power Dissipation	See Dissipation Rating Table		
T_A	Operating free-air temperature range	0	70	°C
T_{stg}	Storage temperature range	65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under セクション 6.2. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.

6.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_I or V_{IC}	Voltage at any buss terminal (separately or common mode)		–7		12	V
V_{IH}	High-level input voltage	D, DE, and $\overline{RE}$	2			V
V_{IL}	Low-level input voltage	D, DE, and $\overline{RE}$			0.8	V
V_{ID}	Differential input voltage(1)				±12	V
I_{OH}	High-level output current	Driver			–60	mA
		Receiver			–400	µA
I_{OL}	Low-level output current	Driver			60	mA
		Receiver			8	
T_A	Operating free-air temperature		0		70	°C

(1) Differential-input/output bus voltage is measured at the non-inverting terminal A with respect to the inverting terminal B.

6.3 Thermal Information

THERMAL METRIC(1)		D	P	UNIT
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.7	66.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.3	55.6	
$R_{\theta JB}$	Junction-to-board thermal resistance	63.4	42.9	
ψ_{JT}	Junction-to-top characterization parameter	8.8	23.9	
ψ_{JB}	Junction-to-board characterization parameter	62.6	42.5	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.4 Dissipation Rating Table

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1100 mW	8.8 mW/°C	704 mW

6.5 Electrical Characteristics – Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18 mA				–1.5	V
V_{OH}	High-level output voltage	V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = –33 mA			3.7		V
V_{OL}	Low-level output voltage	V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = 33 mA			1.1		V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0				$2V_{OD2}$	V
$\|V_{OD2}\|$	Differential output voltage	RL = 100 Ω, see 図 7-1		2	2.7		V
		RL = 54 Ω, see 図 7-1		1.5	2.4		
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage(2)					±0.2	V
V_{OC}	Common-mode output voltage(3)	RL = 54 Ω or 100 Ω, see 図 7-1				3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage(2)					±0.2	V
I_O	Output current	Output disabled(4)	V_O = 12 V			1	mA
			V_O = –7 V			–0.8	
I_{IH}	High-level input current	V_I = 2.4 V				20	µA
I_{IL}	Low-level input current	V_I = 0.4 V				–400	µA
I_{OS}	Short-circuit output current	V_O = –7 V				–250	mA
		V_O = V_{CC}				250	
		V_O = 12 V				500	
I_{CC}	Supply current (total package)	No load	Outputs enabled		35	50	mA
			Outputs disabled		26	40	

(1) All typical values are at V_{CC} = 5 V and T_A = 25°C.
(2) $\Delta|V_{OD}|$ and $D|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.
(3) In ANSI Standard EIA/TIA-422-B, V_{OC}, which is the average of the two output voltages with respect to GND, is called output offset voltage, V_{OS}.
(4) This applies for both power on and off; refer to ANSI Standard EIA/TIA-422-B for exact conditions.

6.6 Electrical Characteristics – Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_O = 2.7 V, I_O = –0.4 mA				0.2	V
$V_{IT–}$	Negative-going input threshold voltage	V_O = 0.5 V, I_O = 8 mA		–0.2			V
V_{hys}	Input hysteresis voltage (V_{IT+} – V_{IT-})				50		mV
V_{IK}	Enable clamp voltage	I_I = –18 mA				–1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = –400 µA See 図 7-2		2.7			V
V_{OL}	Low-level output voltage	V_{ID} = 200 mV, I_{OH} = 8 mA See 図 7-2				0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	µA
I_I	Line input current	Other input = 0 V(2)	V_I = 12 V			1	mA
			V_I = –7 V			–0.8	
I_{IH}	High-level enable input current	V_{IH} = 2.7 V				20	µA
I_{IL}	Low-level enable input current	V_{IL} = 0.4 V				–100	µA
r_i	Input resistance			12			kΩ
I_{OS}	Short-circuit output current			–15		–85	mA

6.6 Electrical Characteristics – Receiver (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
I_{CC}	Supply current (total package)	No load	Outputs enabled		35	50	mA
			Outputs disabled		26	40	

(1) All typical values are at V_{CC} = 5 V, TA = 25°C.
(2) This applies for both power on and power off. Refer to ANSI Standard EIA/TIA-422-B for exact conditions.

6.7 Switching Characteristics – Driver

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential-output delay time	R_L = 60 Ω, See 図 7-3		40	60	ns
$t_{t(OD)}$	Differential-output transition time			65	95	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω, See 図 7-4		55	90	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω, See 図 7-5		30	50	ns
t_{PHZ}	Output disable time form high level	R_L = 110 Ω, See 図 7-4		85	130	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω, See 図 7-5		20	40	ns

6.8 Switching Characteristics – Receiver

V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = –1.5 V to 1.5 V, See 図 7-6		21	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output			23	35	ns
t_{PZH}	Output enable time to high level	See 図 7-7		10	30	ns
t_{PZL}	Output enable time to low level			12	30	ns
t_{PHZ}	Output disable time from high level	See 図 7-7		20	35	ns
t_{PLZ}	Output disable time from low level			17	25	ns

6.9 Typical Characteristics

Conditions listed in each chart

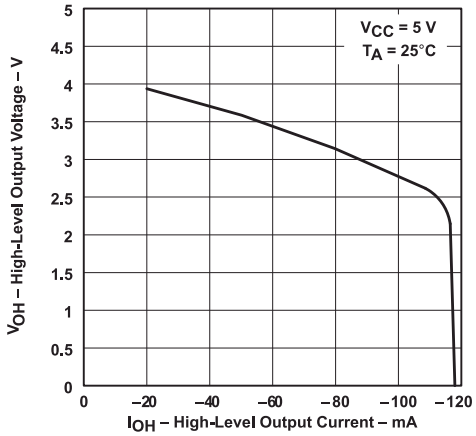


図 6-1. Driver, High-level Output Voltage vs High-Level Output Current

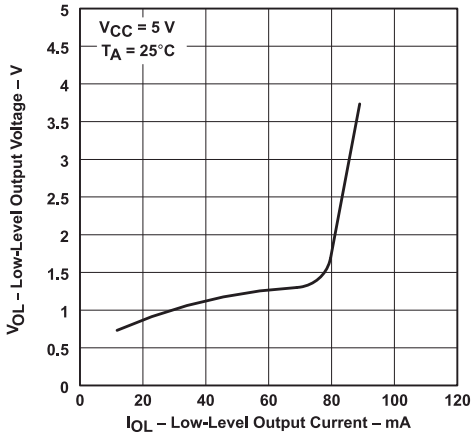


図 6-2. Driver, Low-Level Output Voltage vs Low-Level Output Current

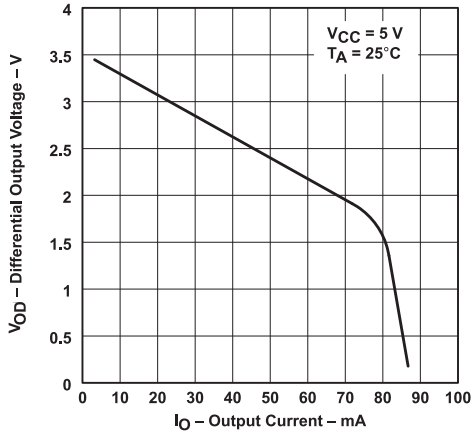


図 6-3. Driver, Differential Output Voltage vs Output Current

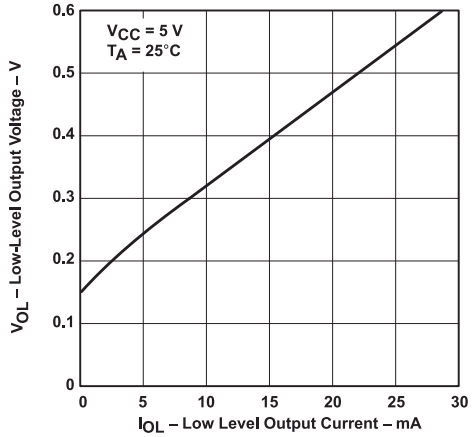


図 6-4. Receiver, Low-Level Output Voltage vs Low-Level Output Current

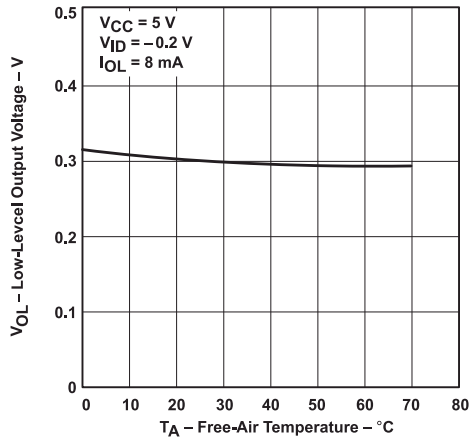


図 6-5. Receiver, Low-Level Output Voltage vs Low-Level Output Current

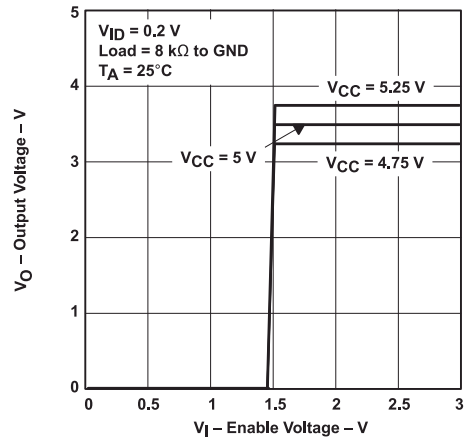


図 6-6. Low-Level Output Voltage vs Free-Air Temperature

6.9 Typical Characteristics (continued)

Conditions listed in each chart

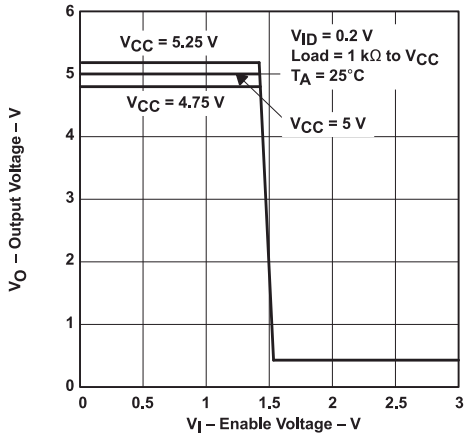


図 6-7. Output Voltage vs Enable Voltage

7 Parameter Measurement Information

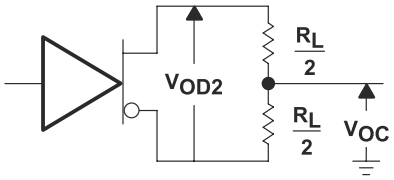


図 7-1. Driver V_{OD} and V_{OC}

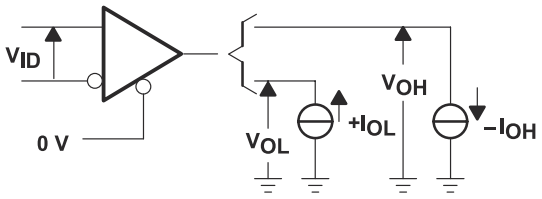
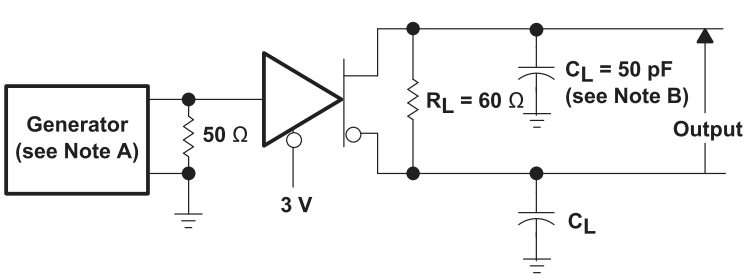
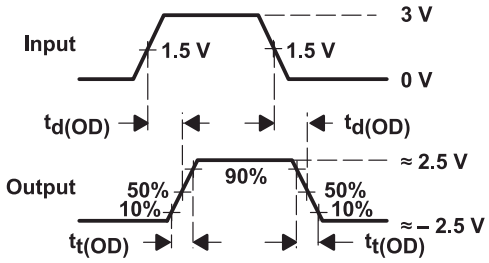


図 7-2. Receiver V_{OH} and V_{OL}



TEST CIRCUIT

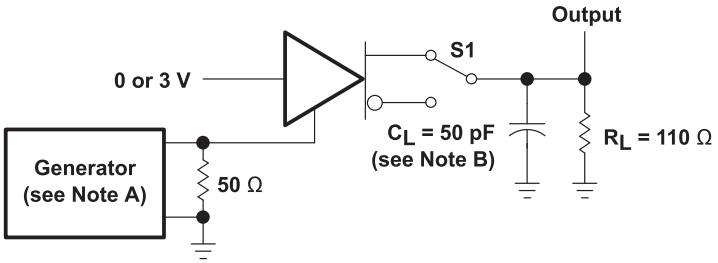


VOLTAGE WAVEFORMS

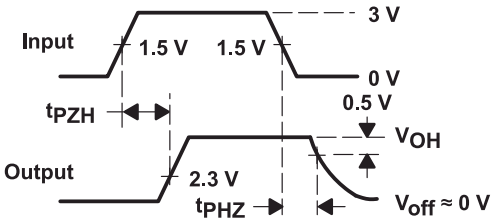
A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 W.

B. C_L includes probe and jig capacitance.

図 7-3. Driver Test Circuit and Voltage Waveforms



TEST CIRCUIT

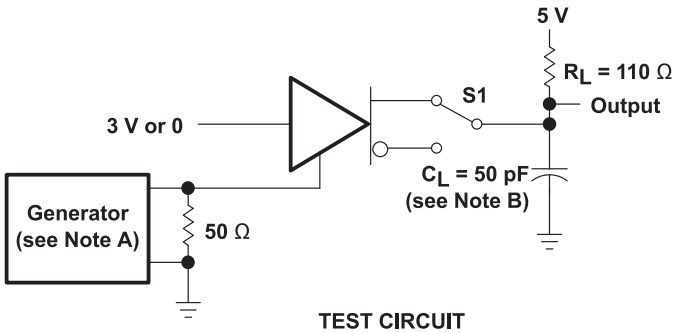


VOLTAGE WAVEFORMS

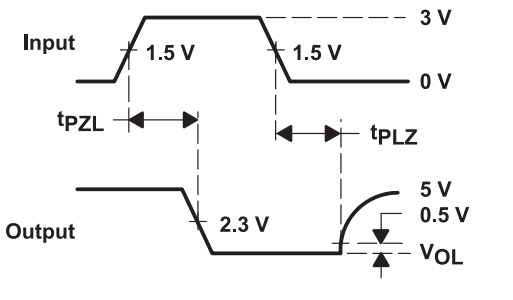
A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 W.

B. C_L includes probe and jig capacitance.

図 7-4. Driver Test Circuit and Voltage Waveforms



TEST CIRCUIT

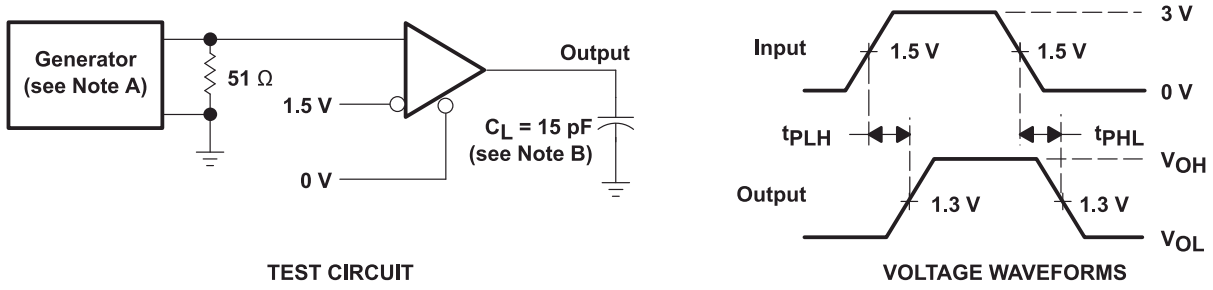


VOLTAGE WAVEFORMS

A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 W.

B. C_L includes probe and jig capacitance.

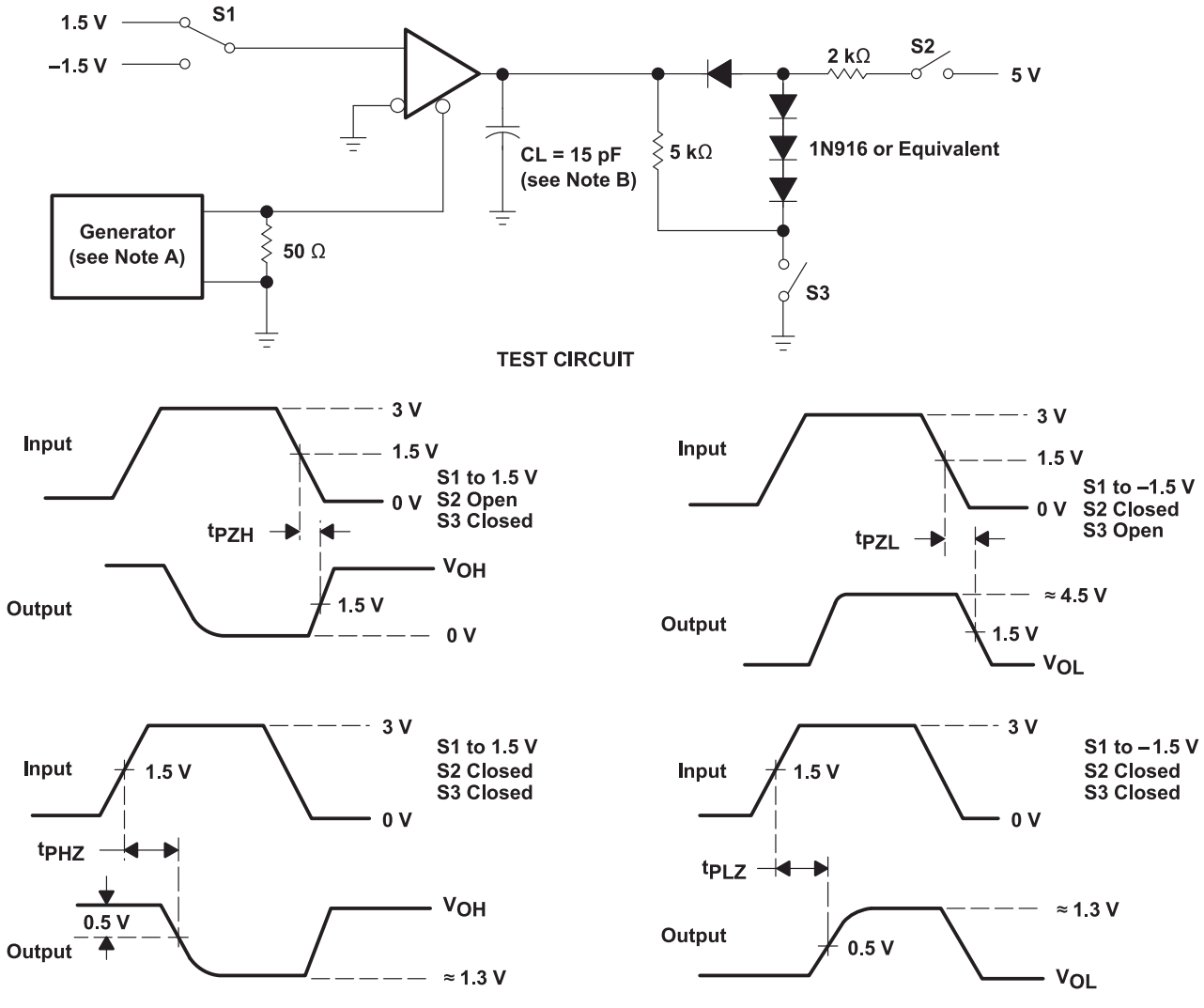
図 7-5. Driver Test Circuit and Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r \le 6$ ns, $t_f \le 6$ ns, Z_O = 50 W.

B. C_L includes probe and jig capacitance.

図 7-6. Receiver Test Circuit and Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r \le 6$ ns, $t_f \le 6$ ns, Z_O = 50 W.

B. C_L includes probe and jig capacitance.

図 7-7. Receiver Test Circuit and voltage Waveforms

8 Detailed Description

8.1 Overview

The SN75176A differential bus transceiver is a monolithic integrated circuit designed for bidirectional data communication on multipoint bus-transmission lines. It is designed for balanced transmission lines and meets ANSI Standard EIA/TIA-422-B and ITU Recommendation V.11.

The SN75176A combines a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be externally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or V_{CC} = 0. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

The driver is designed to handle loads up to 60 mA of sink or source current. The driver features positive- and negative-current limiting and thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The receiver features a minimum input impedance of 12 kΩ, an input sensitivity of ±200 mV, and a typical input hysteresis of 50 mV.

8.2 Functional Block Diagrams

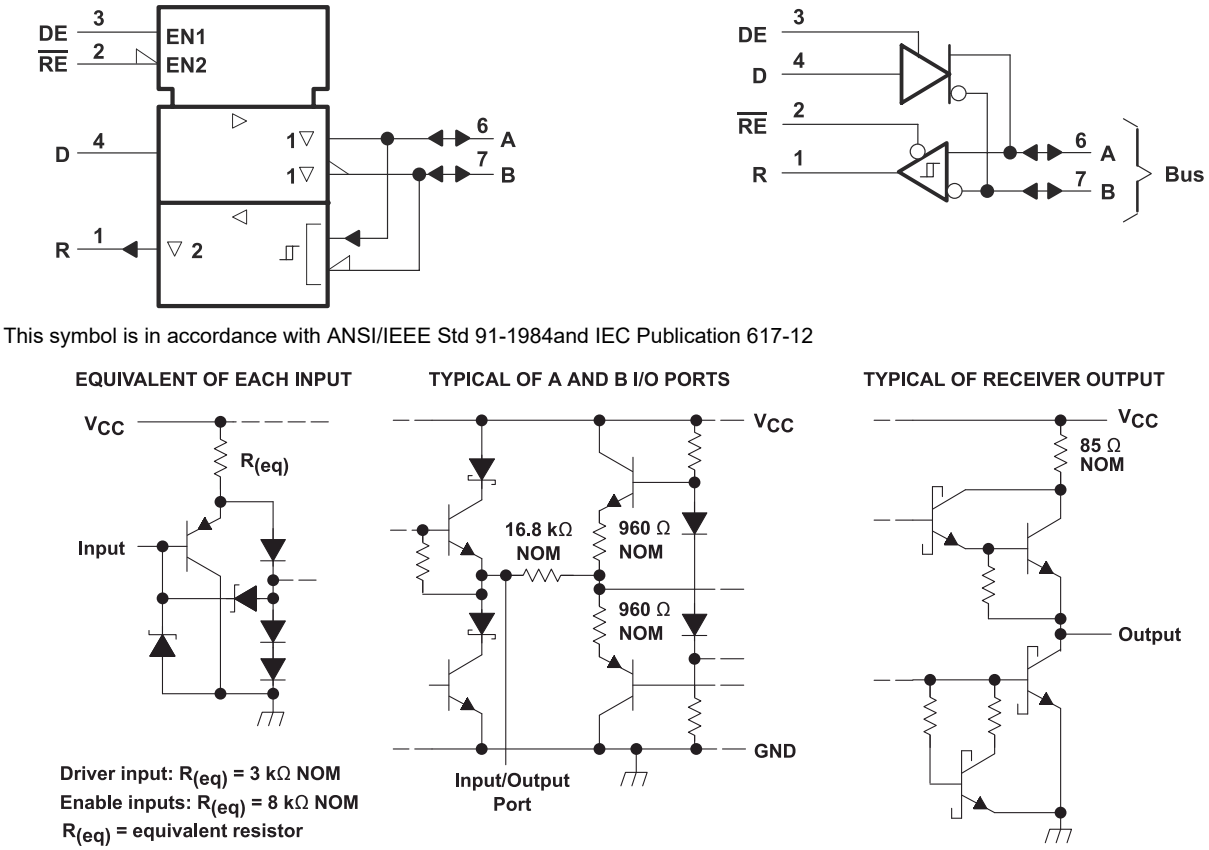


図 8-1. Schematics of Inputs and Outputs

8.3 Feature Description

8.3.1 Driver

The driver converts a TTL logic signal level to RS-422 and RS-485 compliant differential output. The TTL logic input, DE pin, can be used to turn the driver on and off.

表 8-1. Driver Function Table(1)

INPUT D	ENABLE DE	DIFFERENTIAL OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) H = high level, L = low level,
X = irrelevant, Z = high impedance (off)

8.3.2 Receiver

The receiver converts a RS-422 or RS-485 differential input voltage to a TTL logic level output. The TTL logic input, $\overline{RE}$ pin, can be used to turn the receiver logic output on and off.

表 8-2. Receiver Function Table(1)

DIFFERENTIAL INPUTS A–B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V < V_{ID} < 0.2 V	L	U
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	U

(1) H = high level,
L = low level,
U = unkown,
Z = high impedance (off)

8.4 Device Functional Modes

8.4.1 Device Powered

Both the driver and receiver can be individually enabled or disabled in any combination. DE and $\overline{RE}$ can be connected together for a single port direction control bit.

8.4.2 Device Unpowered

The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus when the driver is disabled or V_{CC} = 0.

9 Application and Implementation

注

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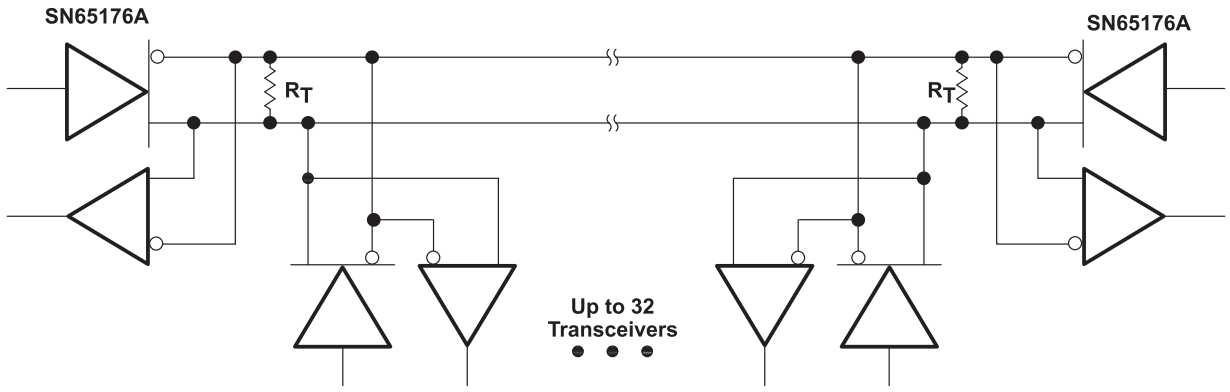
9.1 Application Information

The device can be used in RS-485 and RS-422 physical layer communications.

9.2 Typical Application



The line should be terminated at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

図 9-1. Typical Application Circuit

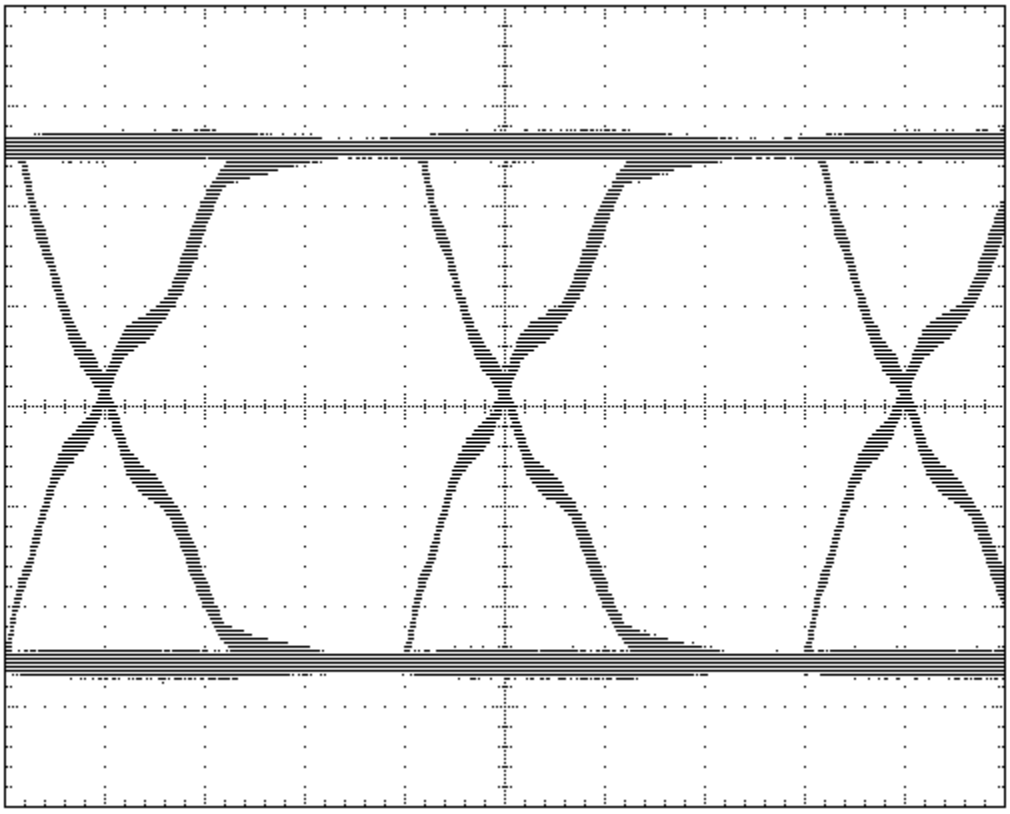
9.2.1 Design Requirements

- 5-V power source
- RS-485 bus operating at 5 Mbps or less
- Connector that ensures the correct polarity for port pins
- External fail safe implementation

9.2.2 Detailed Design Procedure

- Place the device close to bus connector to keep traces (stub) short to prevent adding reflections to the bus line
- If desired, add external fail-safe biasing to ensure +200 mV on the A-B port.

9.2.3 Application Curves



A. Scale is 1V per division and 50nS per division

図 9-2. Eye Diagram for 5-Mbps Over 100 feet of Standard CAT-5E cable 120-Ω Termination at Both Ends.

9.3 Power Supply Recommendations

Power supply should be 5 V with a tolerance less than 10%

9.4 Layout

9.4.1 Layout Guidelines

Traces from device pins A and B to connector must be short and capable of 250 mA maximum current.

9.4.2 Layout Example

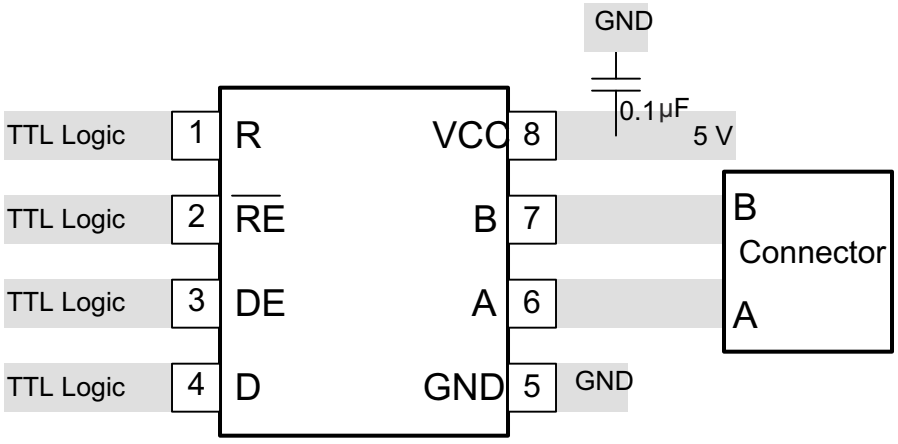


図 9-3. Layout Example

10 Device and Documentation Support

10.1 Trademarks

すべての商標は、それぞれの所有者に帰属します。

10.2 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.3 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN75176AD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	75176A
SN75176ADR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75176A
SN75176ADR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75176A
SN75176ADRE4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75176A
SN75176ADRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75176A
SN75176AP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75176AP
SN75176AP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75176AP
SN75176APE4	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75176AP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

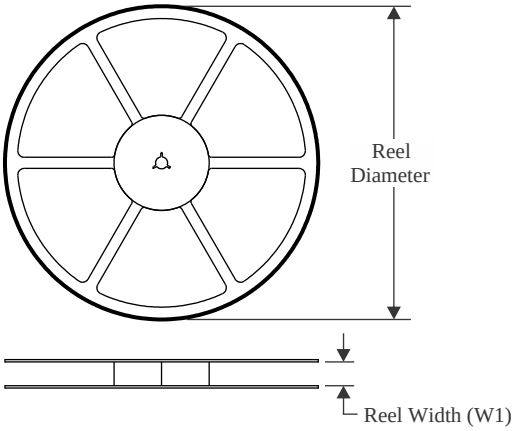
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

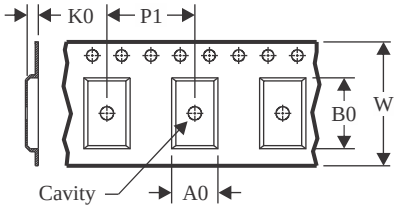
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

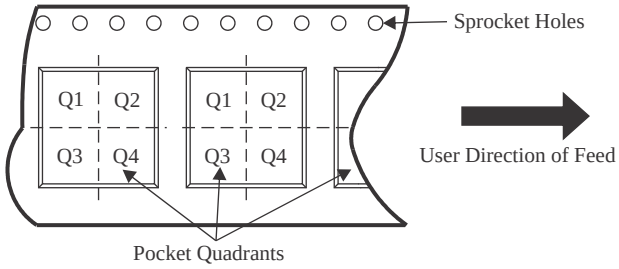


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

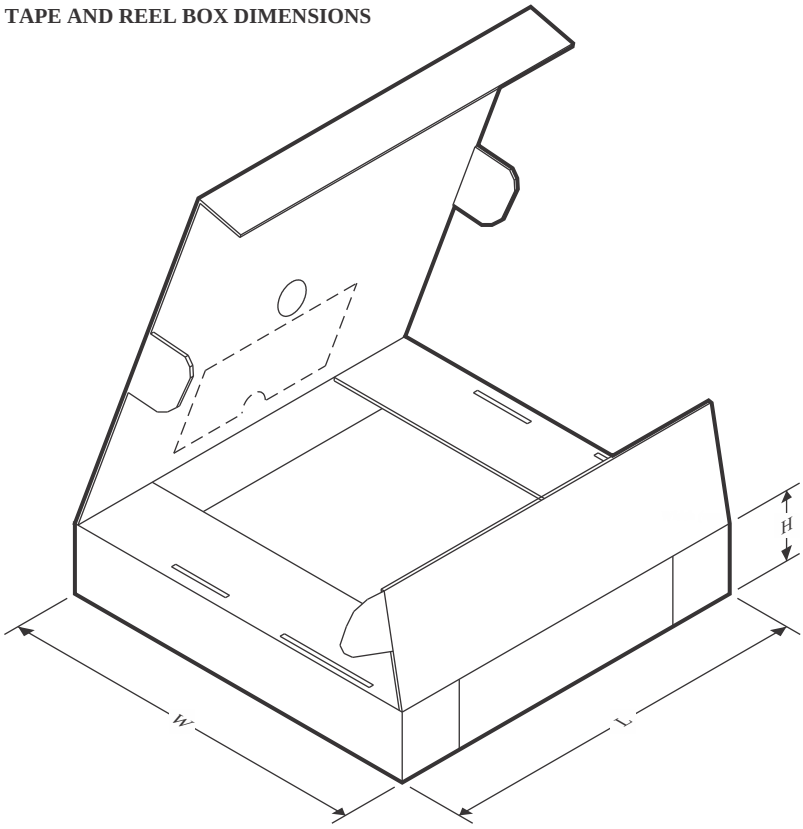
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75176ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

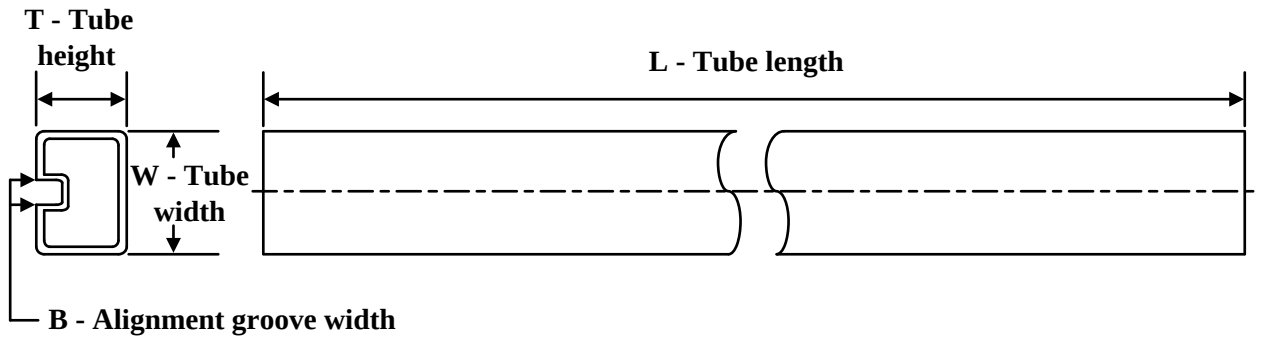
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75176ADR	SOIC	D	8	2500	340.5	336.1	25.0

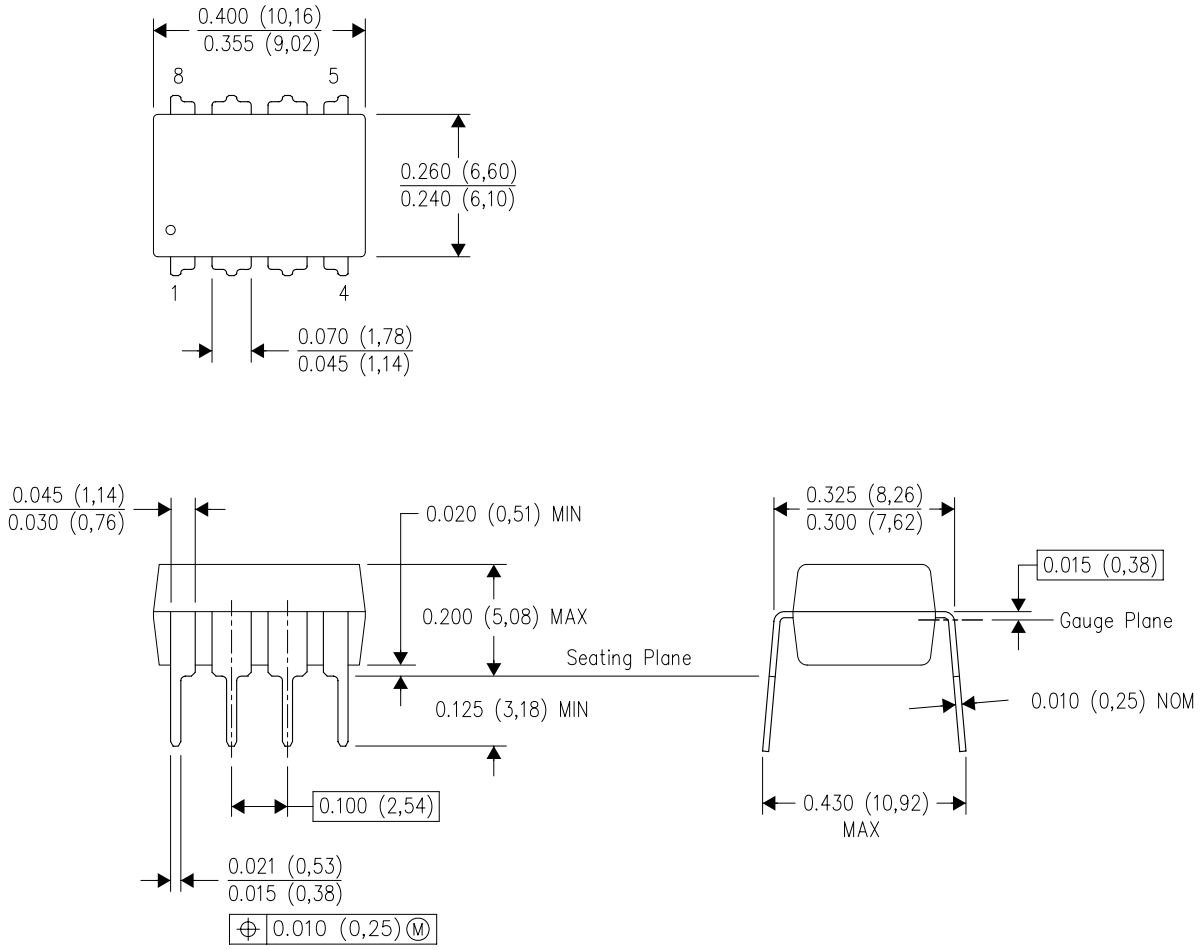
TUBE



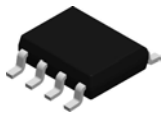
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75176AP	P	PDIP	8	50	506	13.97	11230	4.32
SN75176AP.A	P	PDIP	8	50	506	13.97	11230	4.32
SN75176APE4	P	PDIP	8	50	506	13.97	11230	4.32

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

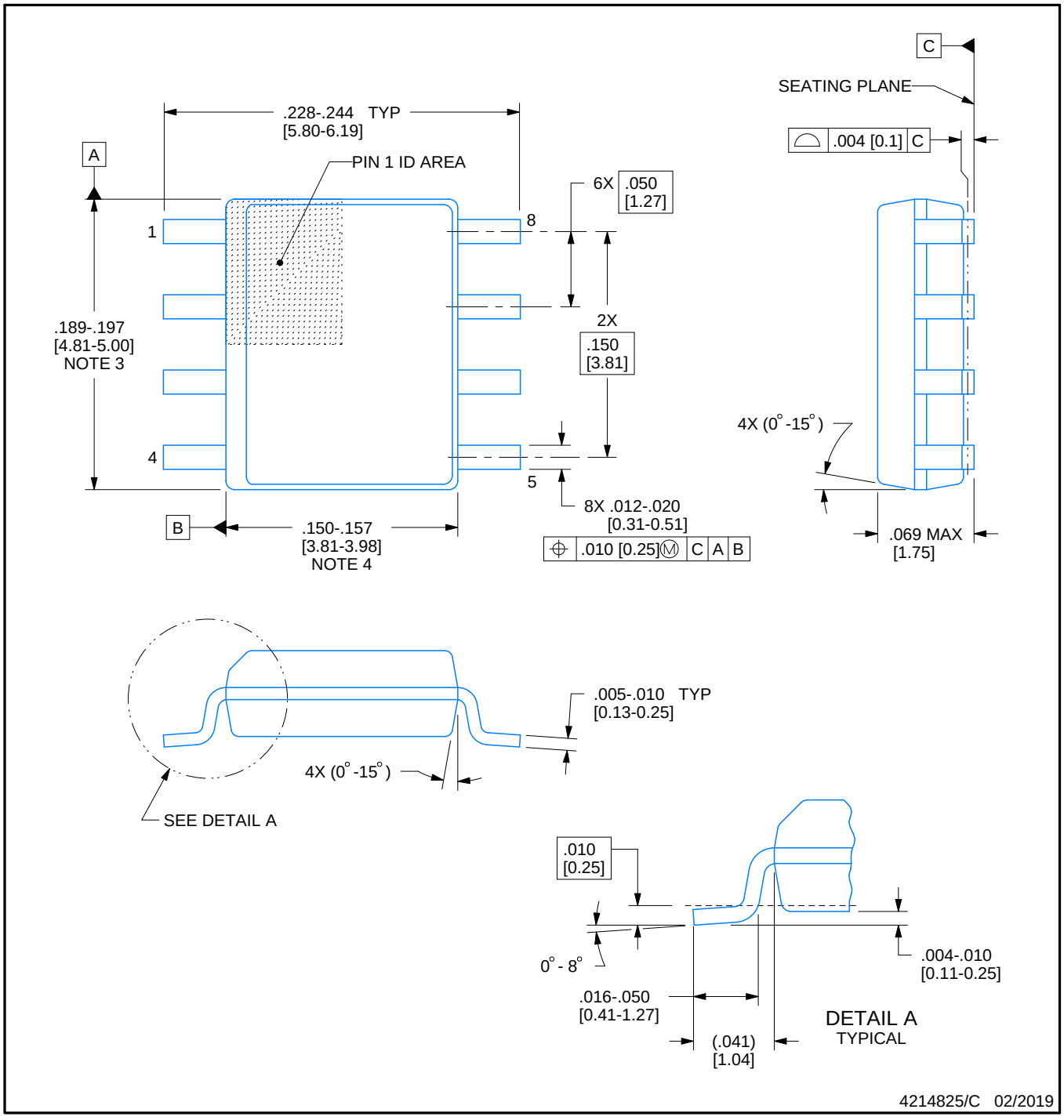


PACKAGE OUTLINE

D0008A

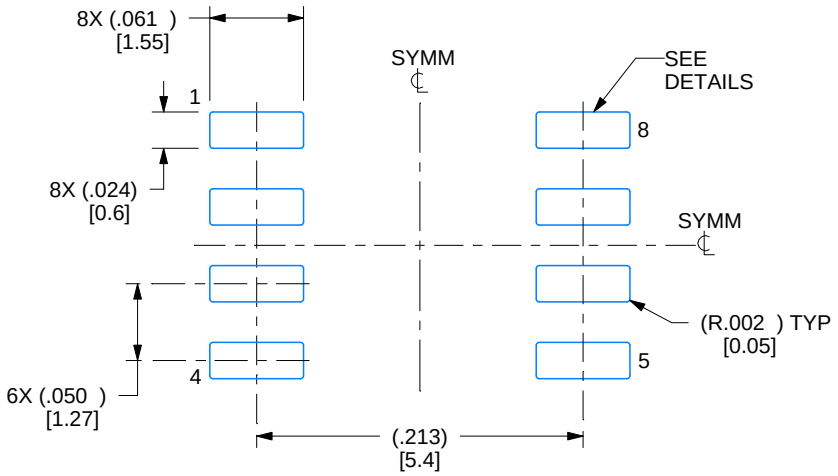
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

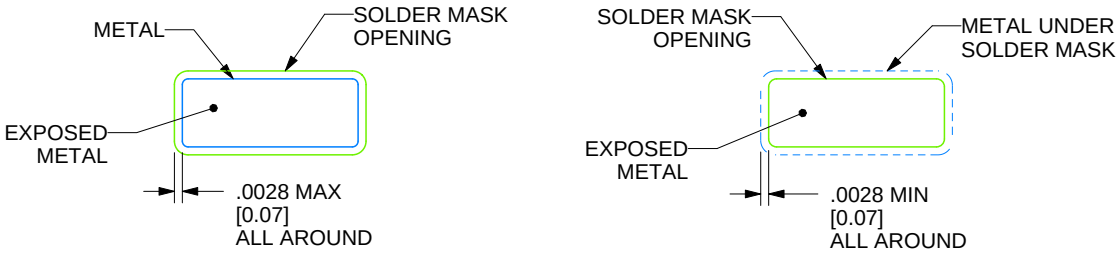


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

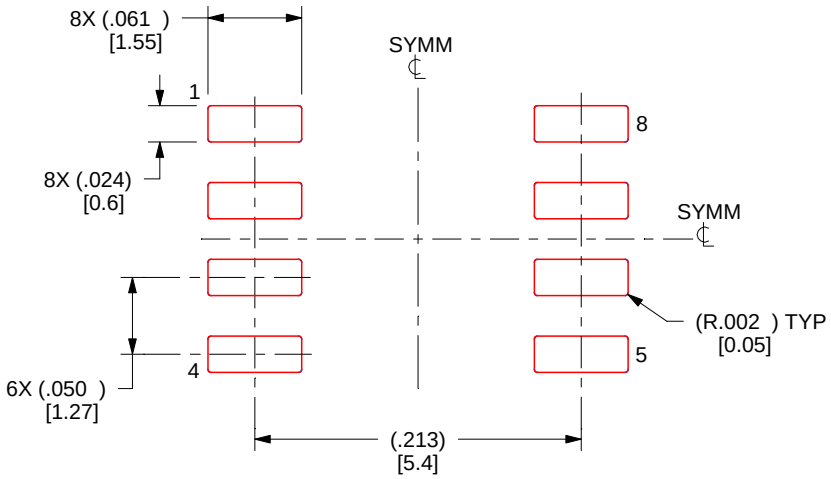
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月