TEXAS INSTRUMENTS
SN75ALS1177, SN75ALS1178
JAJSSZ4C – MARCH 1993 – REVISED FEBRUARY 2024

SN75ALS1177/SN75ALS1178 デュアル差動ドライバ / レシーバ

1 特長

- TIA/EIA-422-B および TIA/EIA-485-A の規格に適合
- ノイズの多い環境の、長いバス ラインでのマルチポイント バス伝送用に設計
- 低消費電流要件:50mA (最大値)
- ドライバの正および負電流制限
- ドライバ同相出力電圧範囲:
  -7V～12V
- サーマル シャットダウン保護、ドライバ 3 ステート出力
- アクティブ High イネーブル
- レシーバ同相入力電圧範囲:
  -12V～12V
- レシーバ入力感度:±200mV
- レシーバ ヒステリシス:50mV (標準値)
- レシーバ高入力インピーダンス:12kΩ (最小値)
- レシーバ 3 ステート出力アクティブ Low イネーブル (SN75ALS1177 のみ)
- 5V 単一電源で動作

2 アプリケーション

- モーター ドライブ
- ファクトリ オートメーション
- ビル オートメーション

3 概要

SN75ALS1177 および SN75ALS1178 デュアル差動ドライバ / レシーバは、マルチポイント バス伝送ラインでの双方向データ通信を目的として設計された集積回路です。これらのデバイスは平衡伝送ライン用に設計されており、TIA/EIA-422-B および TIA/EIA-485-A 規格に適合しています。

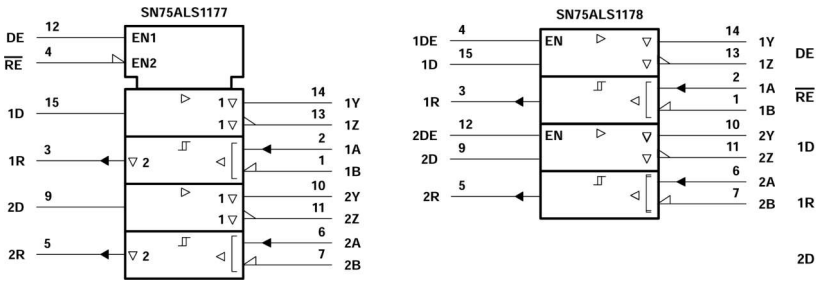
SN75ALS1177 は、デュアル 3 ステート差動ライン ドライバとデュアル 3 ステート差動入力ライン レシーバを統合しており、どちらも 5V 単一電源で動作します。ドライバとレシーバはそれぞれアクティブ High、アクティブ Low のイネーブルを備えており、それらのイネーブルを外部で互いに接続することで、方向制御として機能させることができます。SN75ALS1178 ドライバは、それぞれ個別のアクティブ High イネーブルを搭載しています。フェイルセーフ設計により、レシーバ入力がオープンのときはレシーバ出力は常に High になります。

SN75ALS1177 および SN75ALS1178 は 0℃～70℃で動作が規定されています。

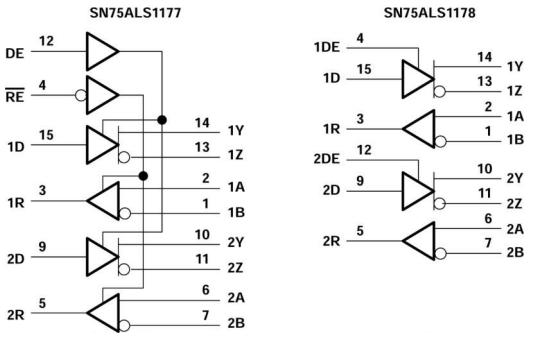
パッケージ オプション

部品番号	パッケージ (1)	パッケージ サイズ(2)
SN75ALS1177 SN75ALS1178	SOP (NS、16)	10.2mm × 7.8mm
	PDIP (N、16)	19.3mm × 9.4mm

(1) 詳細については、セクション 10 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



論理記号†



論理図 (正論理)

† これらの記号は ANSI/IEEE 規格 91-1984 と IEC Publication 617-12 に準拠しています。

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4 Pin Configuration and Functions

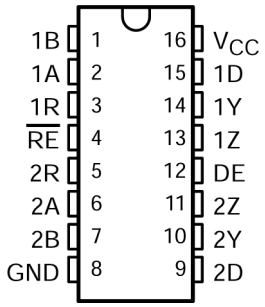


図 4-1. SN75ALS1177: N or NS Package (Top View)

PIN			TYPE	DESCRIPTION
NAME	SO	TSSOP		
1A	2	2	I	RS422 differential input (non-inverting) to receiver 1
2A	6	6	I	RS422 differential input (non-inverting) to receiver 2
1B	1	1	I	RS422 differential input (inverting) to receiver 1
2B	7	7	I	RS422 differential input (inverting) to receiver 2
1D	15	15	I	Logic data input to RS422 driver 1
2D	9	9	I	Logic data input to RS422 driver 2
DE	12	12	I	Driver enable (active high)
GND	8	8	—	Device ground pin
1R	3	3	O	Logic data output of RS422 receiver 1
2R	5	5	O	Logic data output of RS422 receiver 2
$\overline{RE}$	4	4	I	Receiver enable pin (active low)
V_{CC}	16	16	—	Power supply
1Y	14	14	O	RS-422 differential (non-inverting) driver output 1
2Y	10	10	O	RS-422 differential (non-inverting) driver output 2
1Z	13	13	O	RS-422 differential (inverting) driver output 1
2Z	11	11	O	RS-422 differential (inverting) driver output 2

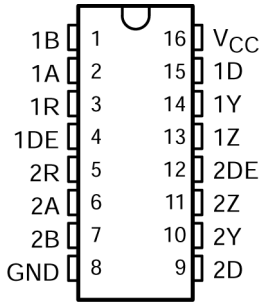


図 4-2. SN75ALS1178: N or NS Package (Top View)

PINT			TYPE	DESCRIPTION
NAME	SO	TSSOP		
1A	2	2	I	RS422 differential input (non-inverting) to receiver 1
2A	6	6	I	RS422 differential input (non-inverting) to receiver 2
1B	1	1	I	RS422 differential input (inverting) to receiver 1
2B	7	7	I	RS422 differential input (inverting) to receiver 2
1D	15	15	I	Logic data input to RS422 driver 1
2D	9	9	I	Logic data input to RS422 driver 2
1DE	4	4	I	Driver 1 enable (active high)
2DE	12	12	I	Driver 2 enable (active high)
GND	8	8	—	Device ground
1R	3	3	O	Logic data output of RS422 receiver 1
2R	5	5	O	Logic data output of RS422 receiver 2
V_{CC}	16	16	—	Power supply
1Y	14	14	O	RS-422 differential (non-inverting) driver output 1
2Y	10	10	O	RS-422 differential (non-inverting) driver output 2
1Z	13	13	O	RS-422 differential (non-inverting) driver output 1
2Z	11	11	O	RS-422 differential (non-inverting) driver output 2

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage, (see (2))		7	V
V_I	Input voltage, (DE, $\overline{RE}$, and D inputs)		7	V
V_O	Output voltage range, drivers	–9	14	V
	Input voltage range, receiver	–14	14	V
	Receiver differential-input voltage range, (see (3))	–14	14	V
	Receiver low-level output current		50	mA
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential input voltage, are with respect to the network ground terminal.
(3) Differential input voltage is measured at the noninverting terminal with respect to the inverting terminal.

5.2 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{ID}	Differential input voltage	Receiver			±12	V
V_{OC}	Common-mode output voltage	Driver	–7(1)		12	V
V_{IC}	Common-mode input voltage	Receiver			±12	V
V_{IH}	High-level input voltage	DE, $\overline{RE}$, D	2			V
V_{IL}	Low-level input voltage	DE, $\overline{RE}$, D			0.8	V
I_{OH}	High-level output current	Driver			–60	mA
		Receiver			–400	µA
I_{OL}	Low - level out output current	Driver			60	mA
		Receiver			8	
T_A	Operating free-air temperature		0		70	°C

(1) The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage level only.

5.3 Thermal Information

THERMAL METRIC(1)		PDIP (N)	SO (NS)	UNIT
		16 Pins	16 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance (see (2))	60.6	88.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	48.1	46.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	40.6	50.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	27.5	13.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	40.3	50.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.

5.4 Driver Section

5.4.1 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = -18 mA					-1.5	V
V_{OH}	High-level output voltage	V_{IH} = 2V,	V_{IL} = 0.8V,	I_{OH} = - 33mA		3.3		V
V_{OL}	Low-level output voltage	V_{IH} = 2V,	V_{IL} = 0.8V,	I_{OL} = 33mA		1.1		V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0			1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	V_{CC} = 5V,	R_L = 100Ω,	See 図 6-1	1/2V_{OD1} or 2[2]			V
		R_L = 54Ω,	See 図 6-1		1.5	2.5	5	
$\|V_{OD3}\|$	Differential output voltage	See Note 4			1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage (see Note 5)	R_L = 54Ω or 100Ω,		See 図 6-1			±0.2	V
V_{OC}	Common-mode output voltage	R_L = 54Ω or 100Ω,		See 図 6-1	-1[3]		3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage (see Note 5)	R_L = 54Ω or 100Ω,		See 図 6-1			±0.2	V
$I_{O(OFF)}$	Output current with power off	V_{CC} = 0,	V_O = -7V to 12V				±100	µA
I_{OZ}	High-impedance-state output current	V_O = -7V to 12V					±100	µA
I_{IH}	High-level input current	V_{IH} = 2.7V					100	µA
I_{IL}	Low-level input current	V_{IL} = 0.4V					-100	µA
I_{OS}	Short-circuit output current	V_O = -7V					-250	mA
		V_O = V_{CC}					250	
		V_O = 12V					250	
		V_O = 0V					150	
I_{CC}	Supply current (total package)	No load	Outputs enabled			35	50	mA
			Outputs disabled			20	50	

(1) All typical values are at V_{CC} = 5V and T_A = 25°C.
(2) The minimum V_{OD2} with a 100Ω load is either 1/2 V_{OD1} or 2V, whichever is greater.
(3) The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage levels only.
(4) See TIA/EIA-485-A 図 6-3.5, test termination measurement 2.
(5) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

5.4.2 Switching Characteristics

at V_{CC} = 5V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, high- to low-level output	R_L = 60Ω, C_{L1} = C_{L2} = 100pF, See 図 6-3		9	15	22	ns
t_{PHL}	Propagation delay time, low- to high-level output	R_L = 60Ω , C_{L1} = C_{L2} = 100pF, See 図 6-3		9	15	22	ns
t_{sk}	Output-to-output skew	R_L = 60Ω, C_{L1} = C_{L2} = 100pF, See 図 6-3		0	2	8	ns
t_{PZH}	Output enable time to high level	C_L = 100pF,	See 図 6-4	30	35	50	ns
t_{PZL}	Output enable time to low level	C_L = 100pF,	See 図 6-5	5	15	25	ns
t_{PHZ}	Output disable time from high level	C_L = 15pF,	See 図 6-4	7	15	30	ns
t_{PLZ}	Output disable time from low level	C_L = 15pF,	See 図 6-5	7	15	30	ns

5.5 Receiver Section

5.5.1 Electrical Characteristics

over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP[1]	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		V_O = 2.7V,	I_O = -0.4mA			0.2	V
V_{IT-}	Negative-going input threshold voltage		V_O = 0.5V,	I_O = 8mA	-0.2[2]			V
V_{hys}	Input hysteresis voltage (V_{IT+} - V_{IT-})					50		mV
V_{IK}	Enable input clamp voltage	SN75ALS1177	I_I = -18mA				-1.5	V
V_{OH}	High-level output voltage		V_{ID} = 200mV, I_{OH} = -400µA, See 図 6-2		2.7			V
V_{OL}	Low-level output voltage		V_{ID} = 200mV, I_{OL} = 8mA, See 図 6-2				0.45	V
I_{OZ}	High-impedance-state output current	SN75ALS1177	V_O = 0.4V to 2.4V				±20	µA
I_I	Line input current (see Note 6)		Other input at 0V	V_I = 12V			1	mA
				V_I = -7V			-0.8	
I_{IH}	High-level input current, $\overline{RE}$	SN75ALS1177	V_{IH} = 2.7V				20	µA
I_{IL}	Low-level input current, $\overline{RE}$	SN75ALS1177	V_{IL} = 0.4V				-100	µA
r_i	Input resistance				12			kΩ
I_{OS}	Short-circuit output current		V_O = 0V,	See Note 7	-15		-85	mA
I_{CC}	Supply current (total package)		No load,	outputs enabled		35	50	mA

(1) All typical values are at V_{CC} = 5V and T_A = 25°C.
(2) The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage levels only.
(3) Refer to TIA/EIA-422-B, TIA/EIA-423-A, and TIA/EIA-485-A for exact conditions.
(4) Not more than one output should be shorted at a time.

5.5.2 Switching Characteristics

at V_{CC} = 5V, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output		C_L = 15pF,	See 図 6-6	15	25	37	ns
t_{PHL}	Propagation delay time, high- to low-level output		C_L = 15pF,	See 図 6-6	15	25	37	ns
t_{PZH}	Output enable time to high level	SN75ALS1177	C_L = 100pF,	See 図 6-7	10	20	30	ns
t_{PZL}	Output enable time to low level	SN75ALS1177	C_L = 100pF,	See 図 6-7	10	20	30	ns
t_{PHZ}	Output disable time from high level	SN75ALS1177	C_L = 15pF,	See 図 6-7	3.5	12	16	ns
t_{PLZ}	Output disable time from low level	SN75ALS1177	C_L = 15pF,	See 図 6-7	5	12	16	ns

6 Parameter Measurement Information

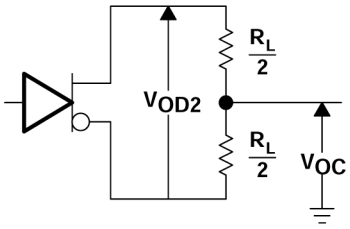


図 6-1. Driver Test Circuit, V_{OD} and V_{OC}

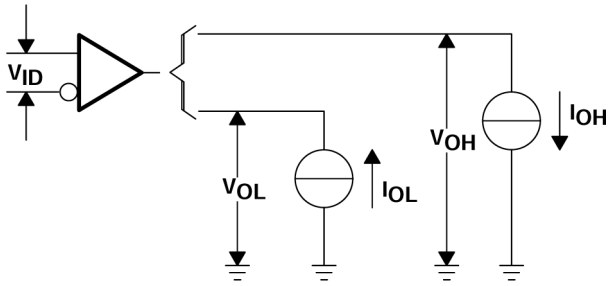
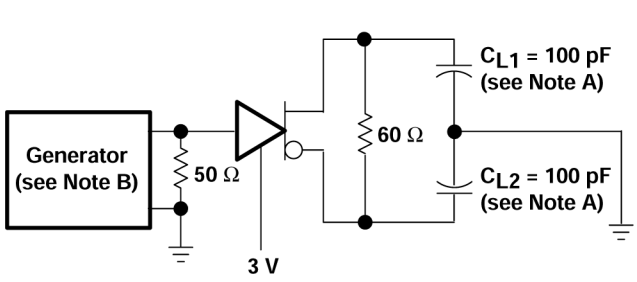
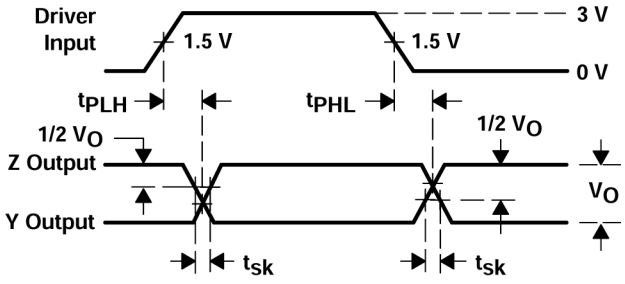


図 6-2. Receiver Test Circuit, V_{OH} and V_{OL}



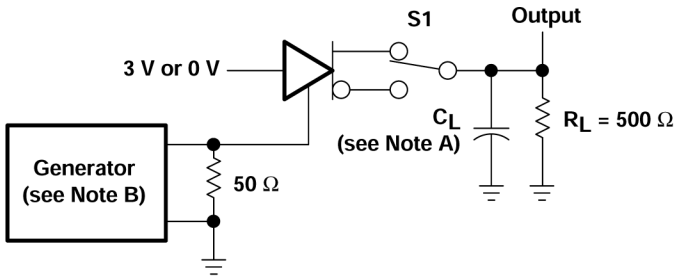
DRIVER TEST CIRCUIT



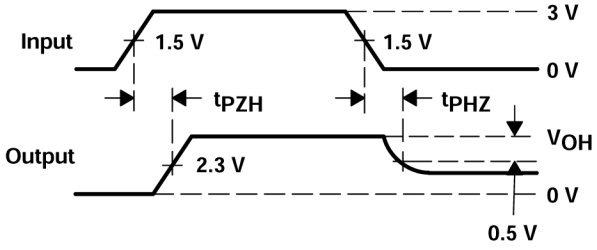
DRIVER VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR ≤ 1MHz, 50% duty cycle, t_r ≤ 10ns, t_f ≤ 10ns.

図 6-3. Driver Propagation Delay Times



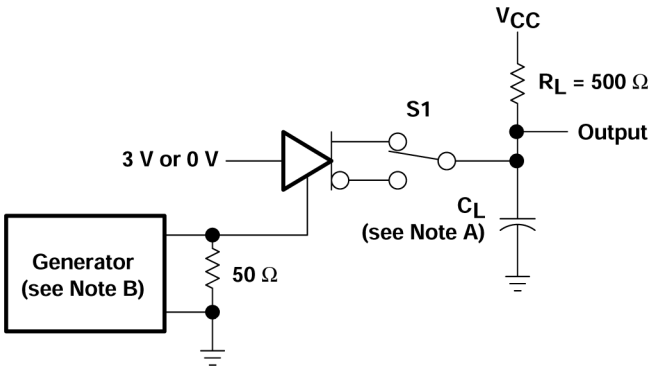
DRIVER TEST CIRCUIT



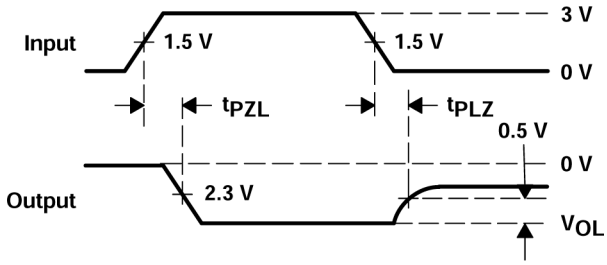
DRIVER VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR ≤ 1MHz, 50% duty cycle, t_r ≤ 10ns, t_f ≤ 10ns.

図 6-4. Driver Enable and Disable Times



DRIVER TEST CIRCUIT

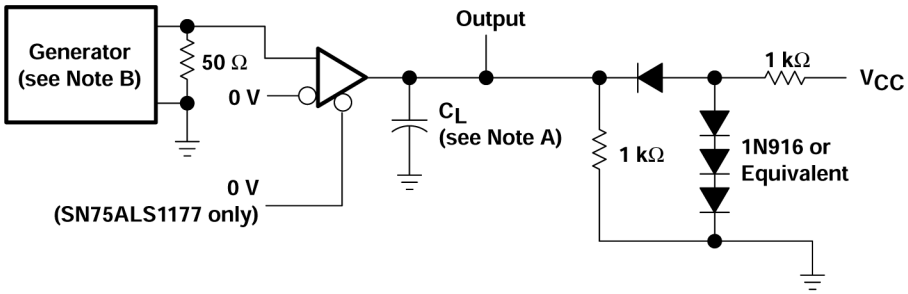


DRIVER VOLTAGE WAVEFORMS

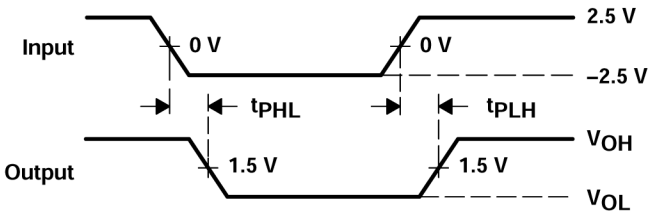
A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR ≤ 1MHz, 50% duty cycle, t_r ≤ 10ns, t_f ≤ 10ns.

図 6-5. Driver Enable and Disable Times



RECEIVER TEST CIRCUIT

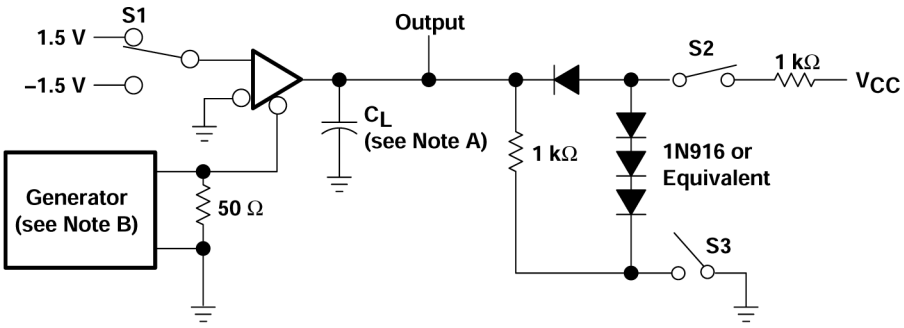


DRIVER VOLTAGE WAVEFORMS

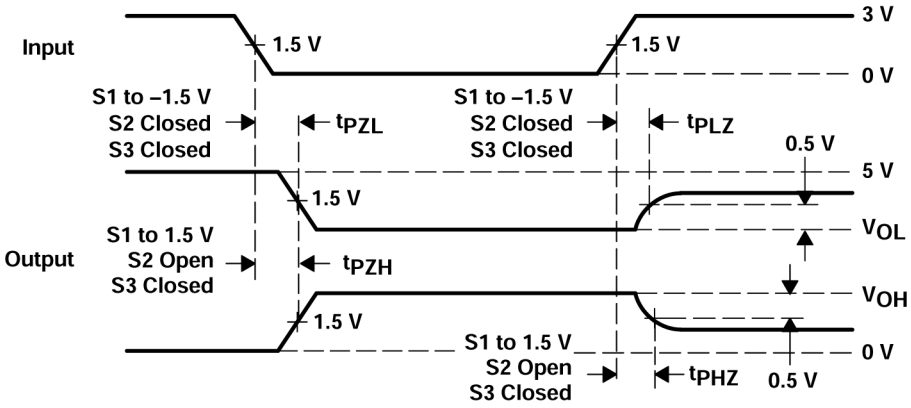
A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR ≤ 1MHz, 50% duty cycle, t_r ≤ 10ns, t_f ≤ 10ns.

図 6-6. Receiver Propagation Delay Times



RECEIVER TEST CIRCUIT



RECEIVER VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR ≤ 1MHz, 50% duty cycle, t_r ≤ 10ns, t_f ≤ 10ns.

図 6-7. Receiver Output Enable and Disable Times

7 Detailed Description

7.1 Device Functional Modes

表 7-1. SN75ALS1177, SN75ALS1178 Functional Table (Each Driver)

INPUT D	ENABLE DE	OUTPUTS(1)	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

表 7-2. SN75ALS1177 Functional Table (Each Receiver)

DIFFERENTIAL A–B	ENABLE $\overline{RE}$ (1)	OUTPUT Y(1)
$V_{ID} \geq 0.2V$	L	H
$-0.2\ V < V_{ID} < 0.2V$	L	?
$V_{ID} \leq -0.2V$	L	L
X	H	Z
Open	L	H

表 7-3. SN75ALS1178 Functional Table (Each Receiver)

DIFFERENTIAL A–B	OUTPUT Y(1)
$V_{ID} \geq 0.2V$	H
$-0.2\ V < V_{ID} < 0.2V$	?
$V_{ID} \leq -0.2V$	L
Open	H

(1) H = High level, L = Low level, ? = Indeterminate, X = Irrelevant, Z = High impedance (off)

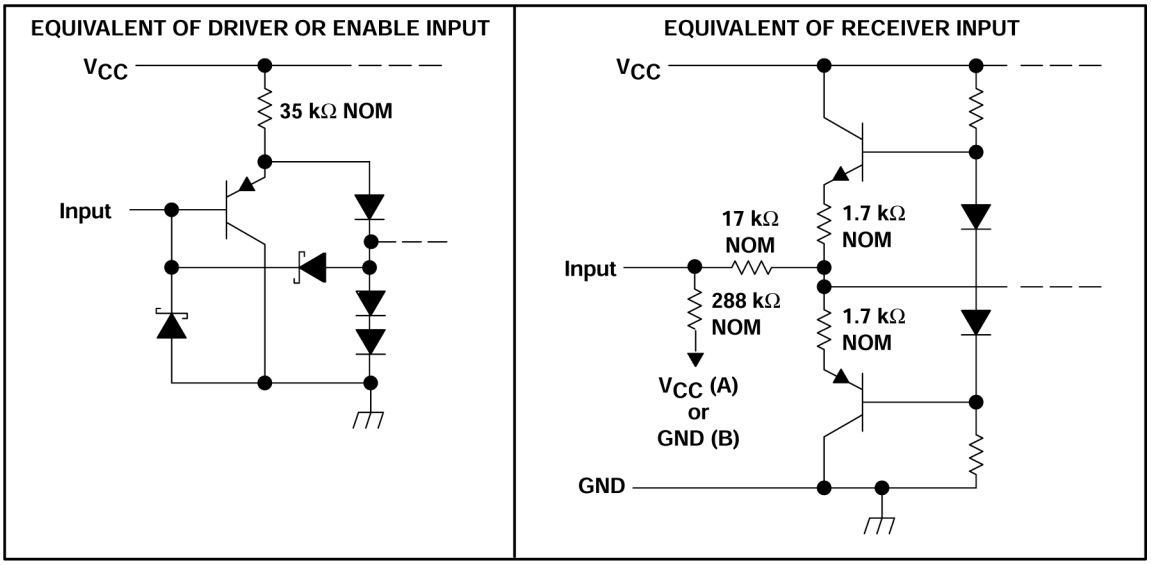


図 7-1. Equivalent Schematics

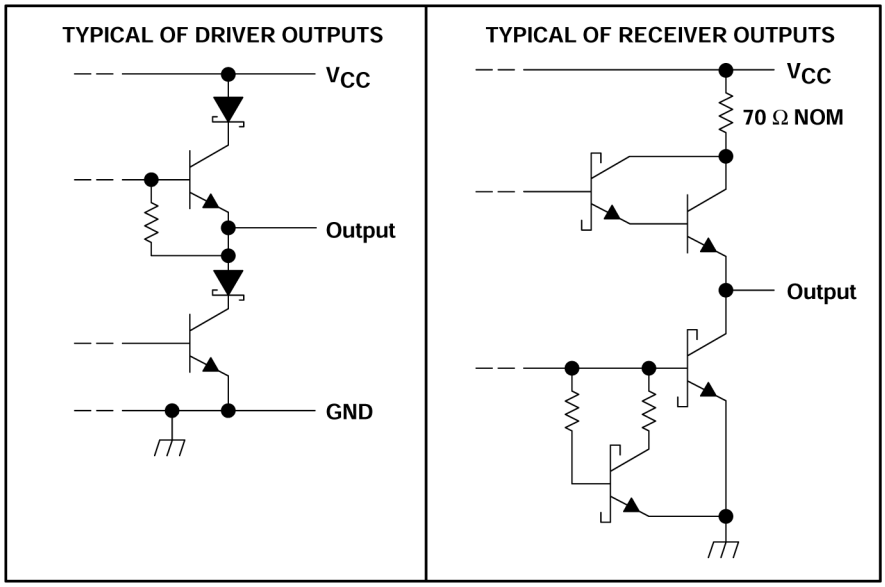


図 7-2. Schematics of Outputs

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Documentation Support

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

8.3 サポート・リソース

E2E ™サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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8.4 Trademarks

E2E ™ is a trademark of Texas Instruments.
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8.5 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

Changes from Revision B (February 2001) to Revision C (February 2024)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を変更	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN75ALS1177N	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75ALS1177N
SN75ALS1177N.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75ALS1177N
SN75ALS1177NSR	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS1177
SN75ALS1177NSR.A	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS1177
SN75ALS1178N	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75ALS1178N
SN75ALS1178N.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75ALS1178N
SN75ALS1178NSR	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS1178
SN75ALS1178NSR.A	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS1178

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

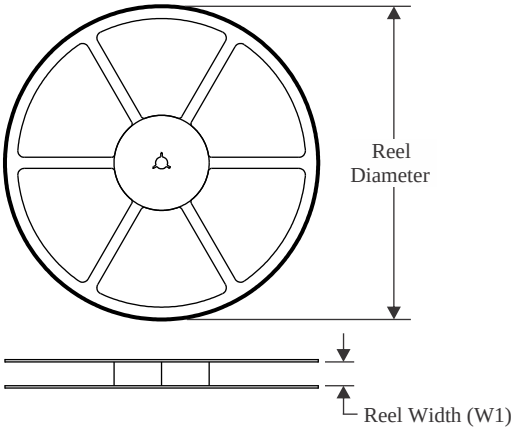
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

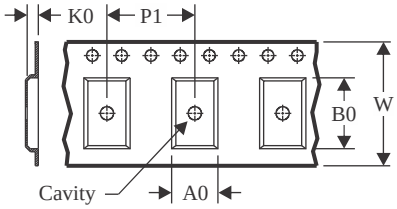
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

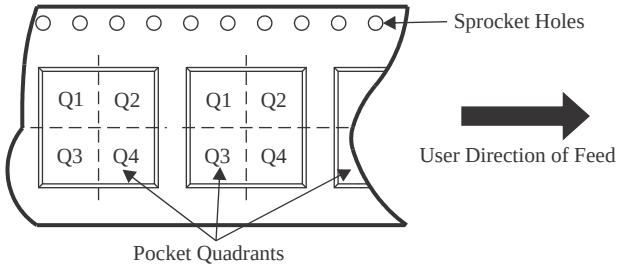


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

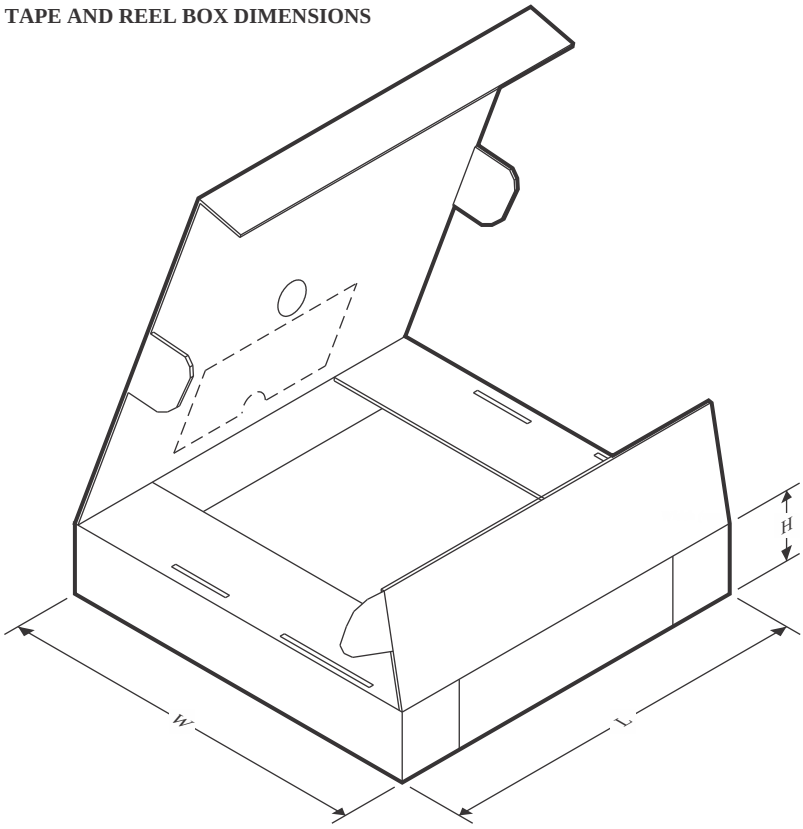
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75ALS1177NSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN75ALS1177NSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN75ALS1178NSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN75ALS1178NSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

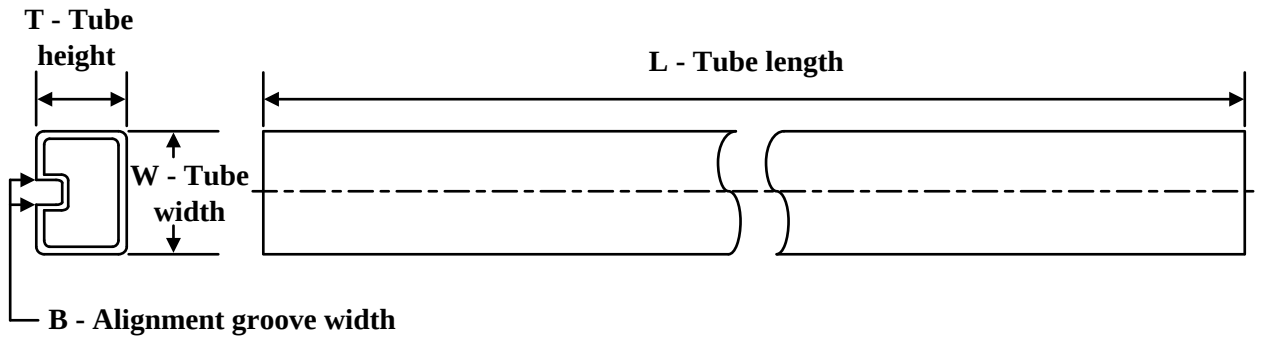
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75ALS1177NSR	SOP	NS	16	2000	353.0	353.0	32.0
SN75ALS1177NSR	SOP	NS	16	2000	353.0	353.0	32.0
SN75ALS1178NSR	SOP	NS	16	2000	353.0	353.0	32.0
SN75ALS1178NSR	SOP	NS	16	2000	353.0	353.0	32.0

TUBE



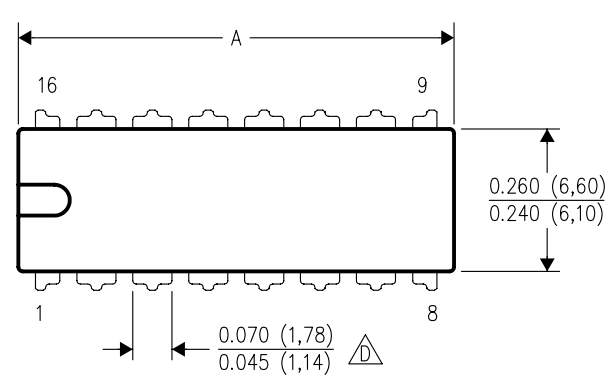
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75ALS1177N	N	PDIP	16	25	506	13.97	11230	4.32
SN75ALS1177N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN75ALS1178N	N	PDIP	16	25	506	13.97	11230	4.32
SN75ALS1178N.A	N	PDIP	16	25	506	13.97	11230	4.32

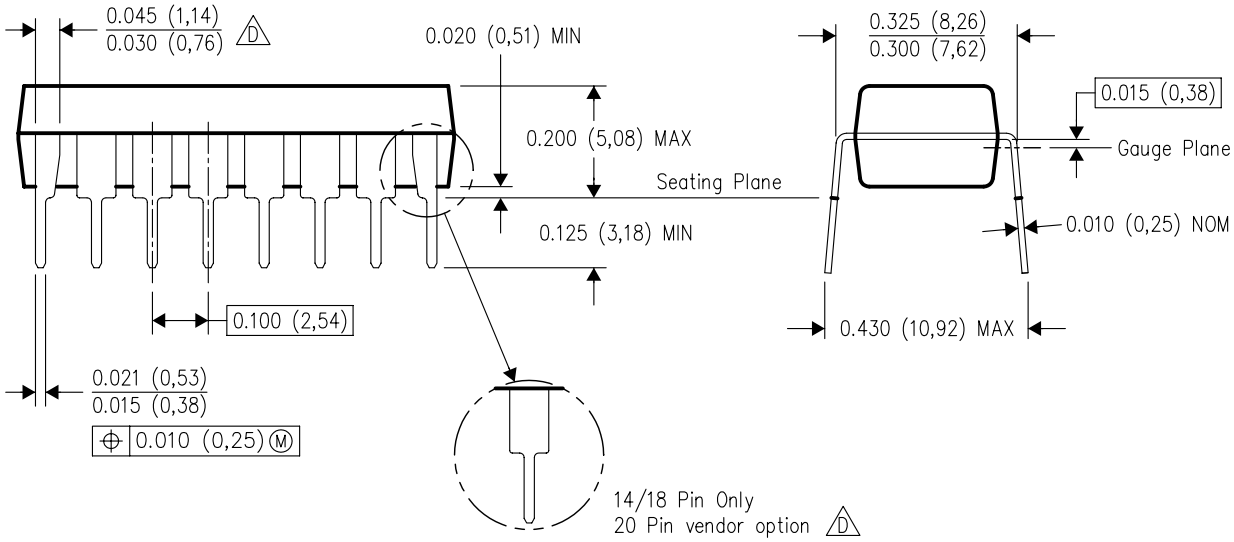
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

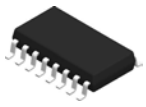


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

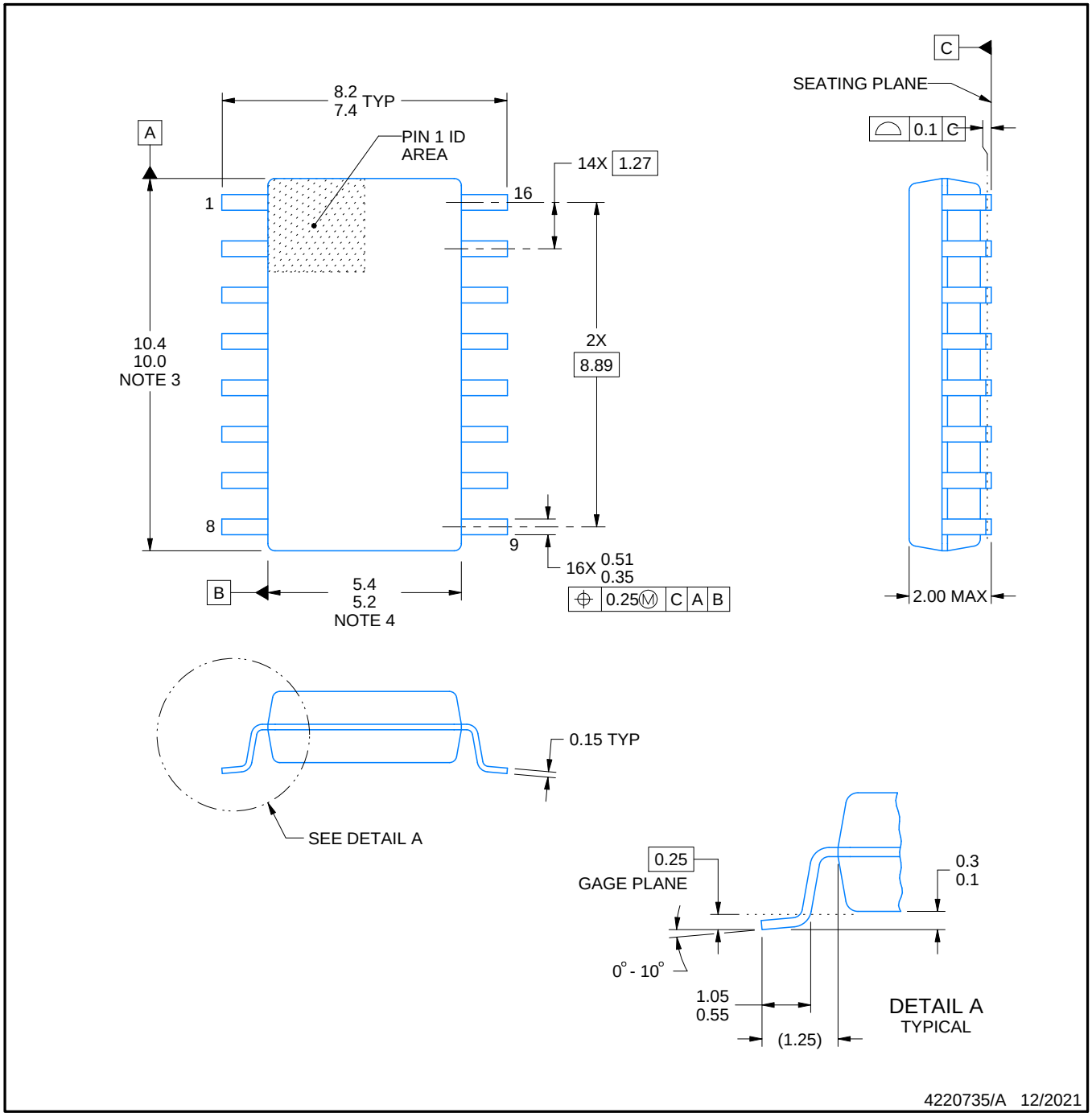


PACKAGE OUTLINE

NS0016A

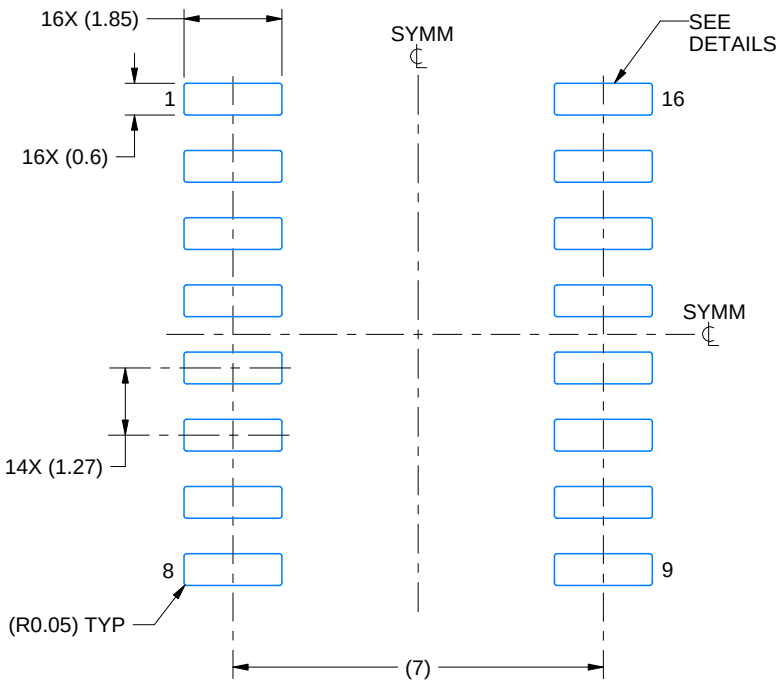
SOP - 2.00 mm max height

SOP

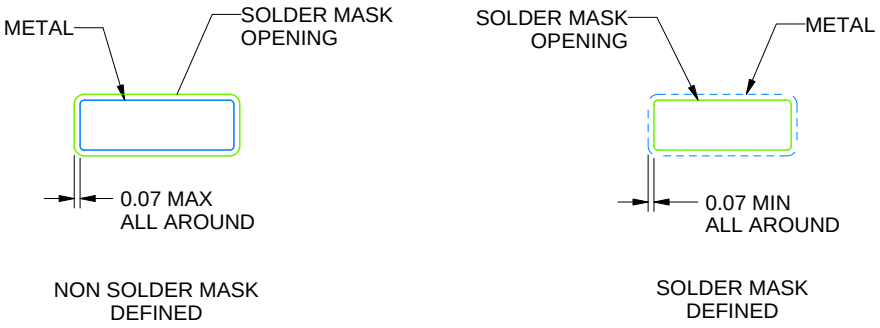


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

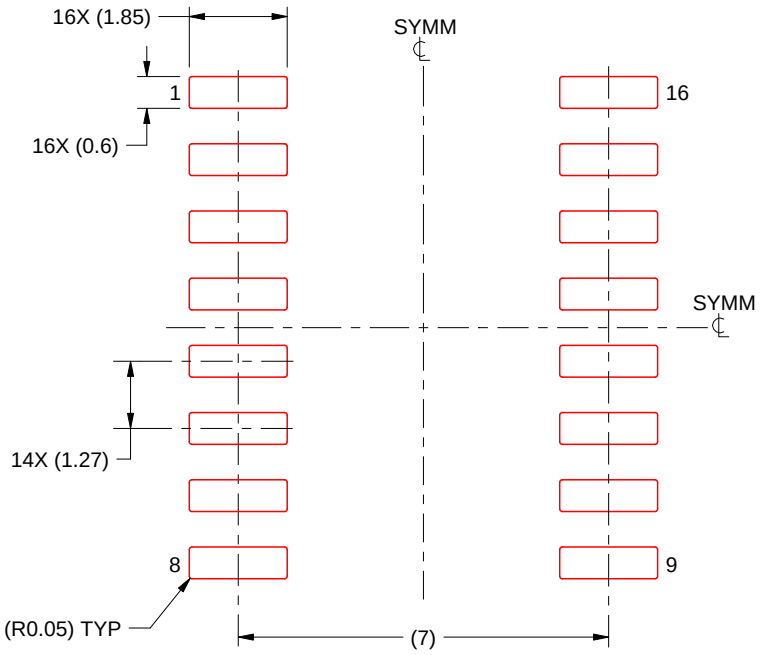
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月