SN75ALS172A クワッド差動ライン ドライバ

1 特長

- ANSI 標準 EIA/TIA-422-B、RS-485、ITU 勧告 V.11 を満たす、または上回る性能
- 高速の高度な低消費電力ショットキー回路
- シリアルとパラレルの両方のアプリケーションでの 20MBaud 動作に対応
- ノイズの多い環境の、長いバス ラインでのマルチポイントの伝送用に設計
- 小さい消費電流要件:55mA 以下
- 広い正および負の入力 / 出力バス電圧範囲
- ドライバ出力能力:±60mA
- サーマル シャットダウン保護機能
- ドライバの正 / 負電流制限
- SN75172 と論理的に互換

2 アプリケーション

- モーター ドライブ
- ファクトリ オートメーション / 制御

3 概要

SN75ALS172A は、トライステート差動出力を備えた 4 つのライン ドライバで構成されています。これらのドライバは ANSI 標準 EIA/TIA-422-B、RS-485、ITU 勧告 V.11 の要件を満たすように設計されています。本デバイスは、最高 20Mbaud の速度で、平衡マルチポイント バス伝送を行うように最適化されています。各ドライバには、広い正および負の同相出力電圧範囲があり、ノイズの多い環境でのパーティライン アプリケーションに適しています。

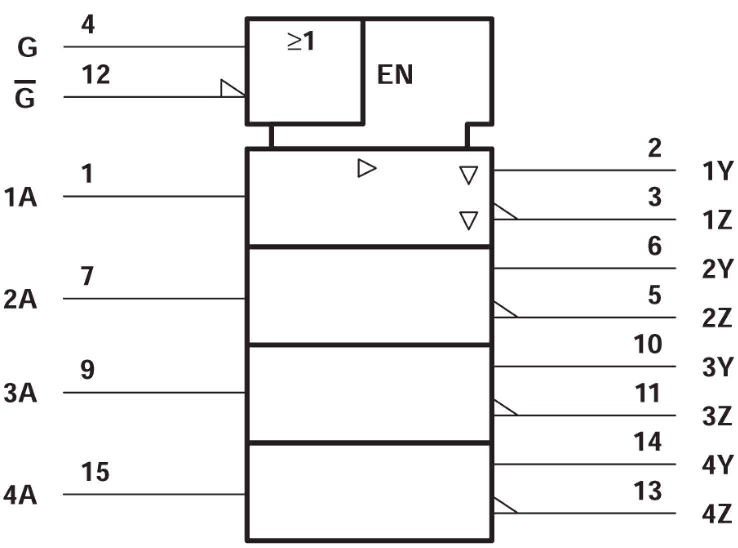
SN75ALS172A には、正および負の電流制限とサーマル シャットダウンがあり、伝送バス ラインのライン フォルト状況から保護します。シャットダウンは、接合部温度が約 150℃で発生します。

SN75ALS172A は、0℃～70℃で動作特性が規定されています。

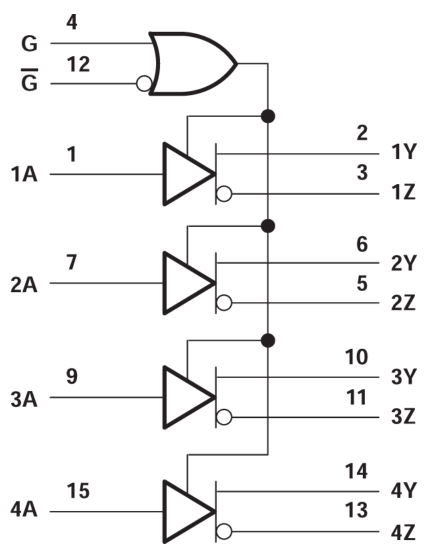
パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
SN75ALS172A	SOIC (DW、20)	12.8mm × 10.3mm
	PDIP (N、16)	19.3mm × 9.4mm

(1) 詳細については、セクション 10 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



論理記号†



A. ここに示すピン番号は、N パッケージのものです。

論理図 (正論理)

† この記号は ANSI/IEEE 規格 91-1984 と IEC Publication 617-12 に準拠しています。

Table of Contents

4 Pin Configuration and Functions

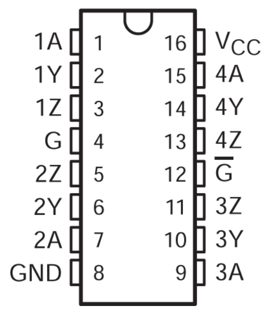
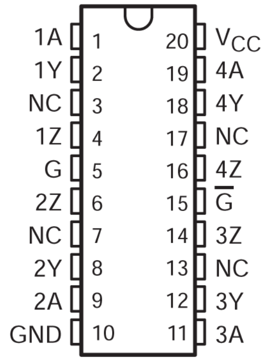


図 4-1. N Package (Top View)

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1A	1	I	Driver 1 input
1Y	2	O	Driver 1 output
1Z	3	O	Driver 1 inverted output
G	4	I	Active high enable all drivers
2Z	5	O	Driver 2 inverted output
2Y	6	O	Driver 2 output
2A	7	I	Driver 2 input
GND	8	–	Ground pin
3A	9	I	Driver 3 input
3Y	10	O	Driver 3 output
3Z	11	O	Driver 3 inverted output
$\overline{G}$	12	I	Active low enable all drivers
4Z	13	O	Driver 4 inverted output
4Y	14	O	Driver 4 output
4A	15	I	Driver 4 input
V_{CC}	16	–	Power pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.



A. NC – No internal connection

図 4-2. DW Package (Top View)

表 4-2. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1A	1	I	Driver 1 input
1Y	2	O	Driver 1 output
NC	3	–	No internal connection
1Z	4	O	Driver 1 inverted output
G	5	I	Active high enable all drivers
2Z	6	O	Driver 2 inverted output
NC	7	–	No internal connection
2Y	8	O	Driver 2 output
2A	9	I	Driver 2 input
GND	10	–	Ground pin
3A	11	I	Driver 3 input
3Y	12	O	Driver 3 output
NC	13	–	No internal connection
3Z	14	O	Driver 3 inverted output
$\overline{G}$	15	I	Active low enable all drivers
4Z	16	O	Driver 4 inverted output
NC	17	–	No internal connection
4Y	18	O	Driver 4 output
4A	19	I	Driver 4 input
V_{CC}	20	–	Power pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
V_{CC}	Supply voltage, see note [(2)]	-0.3	7	V
V_I	Input voltage	-0.3	7	V
V_O	Output voltage range	–9	14	V
P_D	Continuous total dissipation	See Dissipation Rating Table		
T_{stg}	Storage temperature range	–65	150	°C
T_{LEAD}	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

5.2 Dissipation Rating Table

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1125 mW	9 mW/°C	720 mW	585 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

5.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Common-mode output voltage, V_{OC}	-7		12	V
High-level output current, I_{OH}			–60	mA
Low-level output current, I_{OL}			60	mA
Operating free-air temperature, T_A	0		70	°C

5.4 Thermal Information

THERMAL METRIC[(1)]		DW (SOIC)	N (PDIP)	UNIT
		20-Pins	16-Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	66.8	60.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	34.4	48.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	39.7	40.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	8.9	27.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	39.0	40.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.5 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP [1]	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = -18mA					-1.5	V
V_O	Output voltage	I_O = 0			0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_o = 0			1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	V_{CC} = 5V,	R_L = 100Ω,	See 図 6-1	1/2V_{OD1} or 2[2]			V
		R_L = 54Ω,	See 図 6-1		1.5	2.5	5	
$\|V_{OD3}\|$	Differential output voltage	See Note 2			1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage[3]	R_L = 54Ω or 100Ω,	See 図 6-1				±0.2	V
V_{OC}	Common-mode output voltage[4]	R_L = 54Ω or 100Ω,	See 図 6-1		-1		3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage[3]	R_L = 54Ω or 100Ω,	See 図 6-1				±0.2	V
I_O	Output current with power off	V_{CC} = 0,	V_O = -7V to 12V				±100	μA
I_{OZ}	High-impedance-state output current	V_O = -7V to 12V					±100	μA
I_{IH}	High-level input current	V_I = 2.7V					20	μA
I_{IL}	Low-level input current	V_I = 0.4V					-100	μA
I_{OS}	Short-circuit output current	V_O = -7V to 12V					±250	mA
I_{CC}	Supply current (all drivers)	No load	Outputs enabled			36	55	mA
			Outputs disabled			15	30	

(1) All typical values are at V_{CC} = 5V and T_A = 25°C.
(2) The minimum V_{OD2} with a 100Ω load is either 1/2 V_{OD1} or 2V, whichever is greater.
(3) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
(4) In ANSI Standard EIA/TIA-422-B, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
(5) See EIA Standard RS-485, 図 6-3-5, Test Termination Measurement 2.

5.6 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature, C_L = 50pF

PARAMETER		TEST CONDITIONS		MIN	TYP[1]	MAX	UNIT
$t_{d(OD)}$	Differential-output delay time	R_L = 54Ω,	See 図 6-2	9	15	22	ns
t_{PZH}	Output enable time to high level	R_L = 110Ω,	See 図 6-3	30	45	70	ns
t_{PZL}	Output enable time to low level	RL = 110Ω,	See 図 6-4	25	40	65	ns
t_{PHZ}	Output disable time from high level	R_L = 110Ω,	See 図 6-3	10	20	35	ns
t_{PLZ}	Output disable time from low level	R_L = 110Ω,	See 図 6-4	10	30	45	ns

(1) All typical values are at V_{CC} = 5V and T_A = 25°C.

6 Parameter Measurement Information

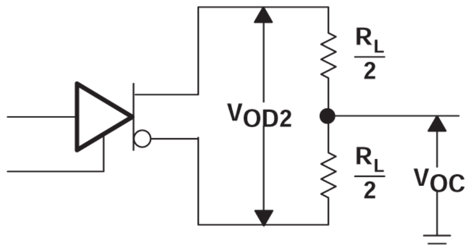
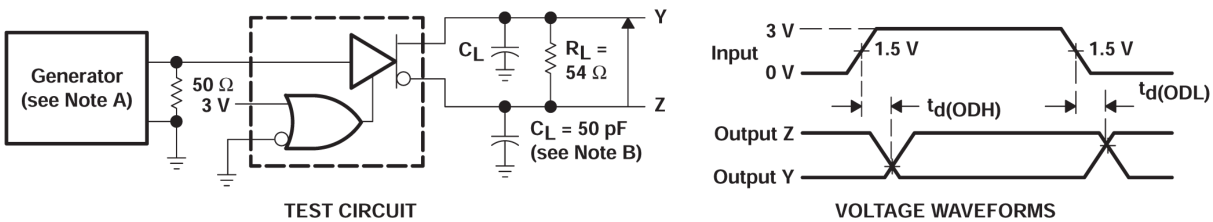


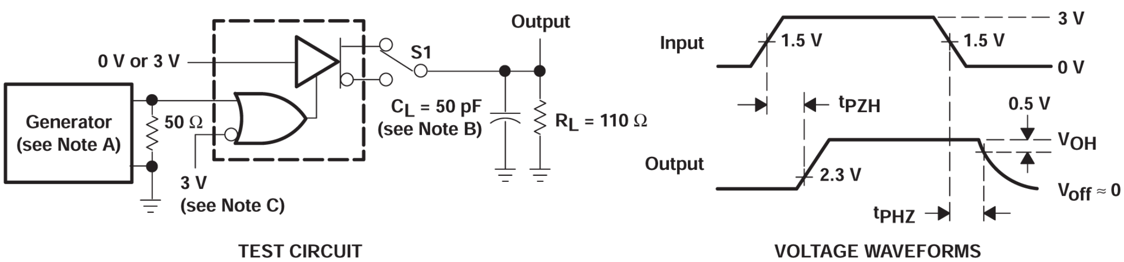
図 6-1. Differential and Common-Mode Output Voltages



A. The input pulse is supplied by a generator having the following characteristics: PRR = 1MHz, Z_O = 50Ω, duty cycle = 50%, $t_f \le$ 10ns, $t_r \le$ 10ns.

B. C_L includes probe and stray capacitance.

図 6-2. Differential Output Test Circuit and Voltage Waveforms

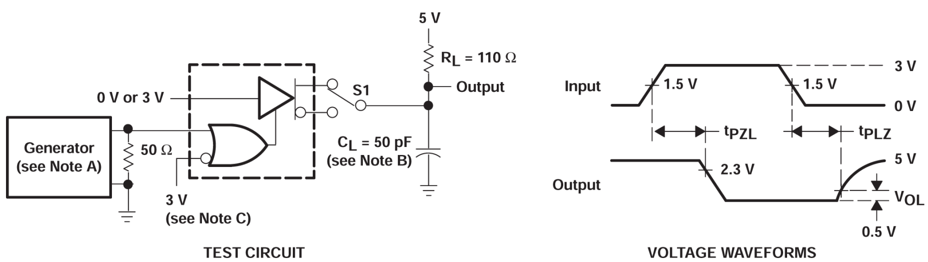


A. The input pulse is supplied by a generator having the following characteristics: PRR = 1MHz, Z_O = 50Ω, duty cycle = 50%, $t_f \le$ 5ns, $t_r \le$ 5ns.

B. C_L includes probe and stray capacitance.

C. To test the active-low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

図 6-3. Test Circuit and Voltage Waveforms, T_{PZH} and T_{PHZ}



A. The input pulse is supplied by a generator having the following characteristics: PRR = 1MHz, Z_O = 50Ω, duty cycle = 50%, $t_f \le$ 5ns, $t_r \le$ 5ns.

B. C_L includes probe and stray capacitance.

C. To test the active-low enable G, ground $\overline{G}$ and apply an inverted input waveform to $\overline{G}$.

図 6-4. Test Circuit and Voltage Waveforms, T_{PZL} and T_{PLZ}

7 Detailed Description

7.1 Device Functional Modes

表 7-1. Function Table (Each Driver)

INPUT(1) A	ENABLES		OUTPUTS	
	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off)

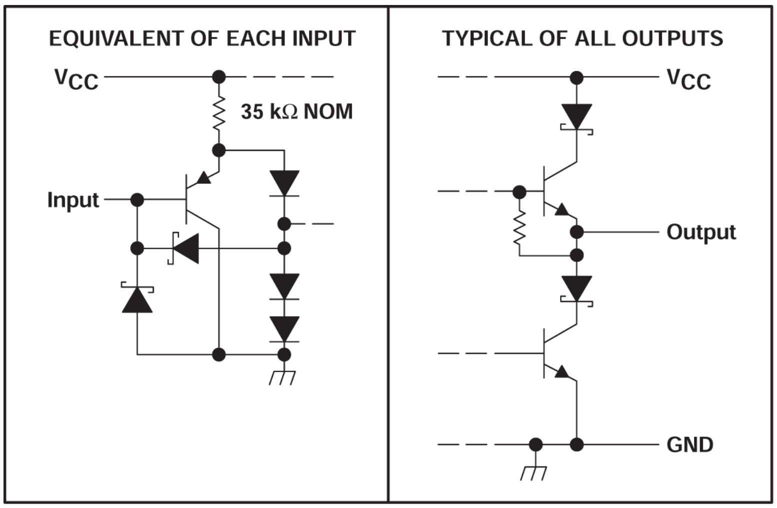


図 7-1. Schematics of Inputs and Outputs

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

8.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

8.3 商標

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

8.4 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.5 用語集

テキサス・インスツルメンツ用語集	この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (April 1998) to Revision E (April 2024) **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を変更 1
- Added the *Thermal Information* table 4
- Changed Note A in 図 6-2 6

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN75ALS172ADW	Obsolete	Production	SOIC (DW) | 20	-	-	Call TI	Call TI	0 to 70	75ALS172A
SN75ALS172ADWR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS172A
SN75ALS172ADWR.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS172A
SN75ALS172AN	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75ALS172AN
SN75ALS172AN.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75ALS172AN

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

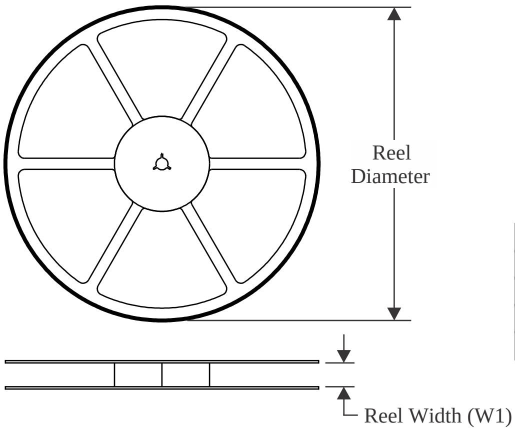
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

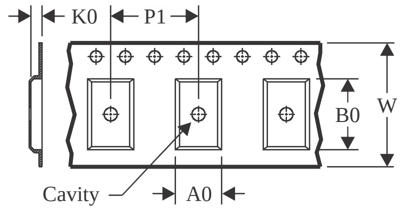
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

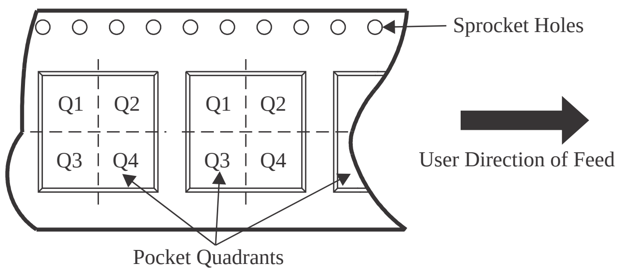


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

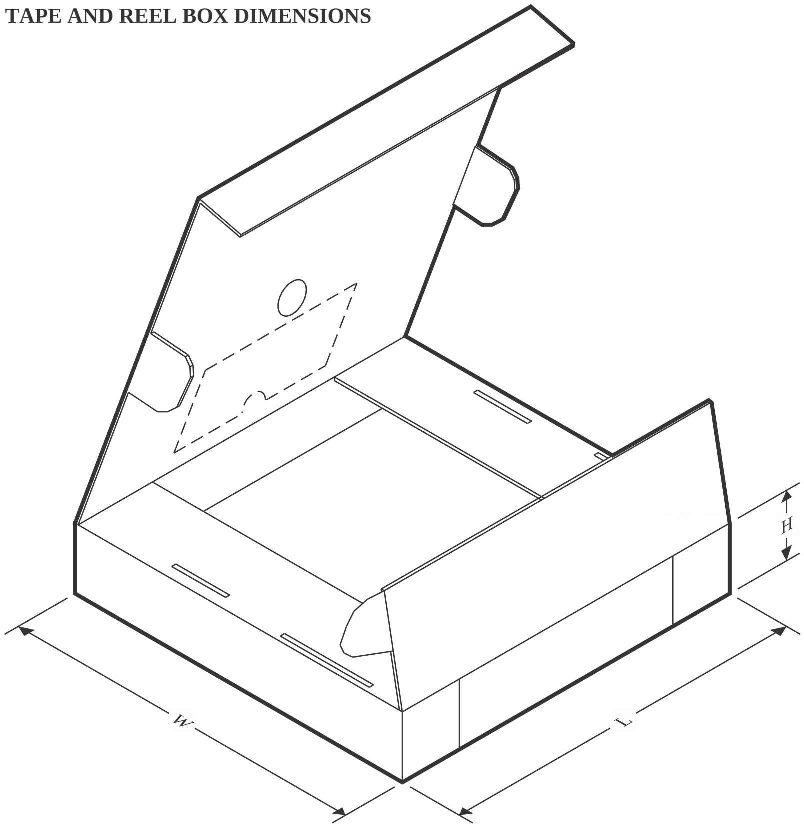
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75ALS172ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

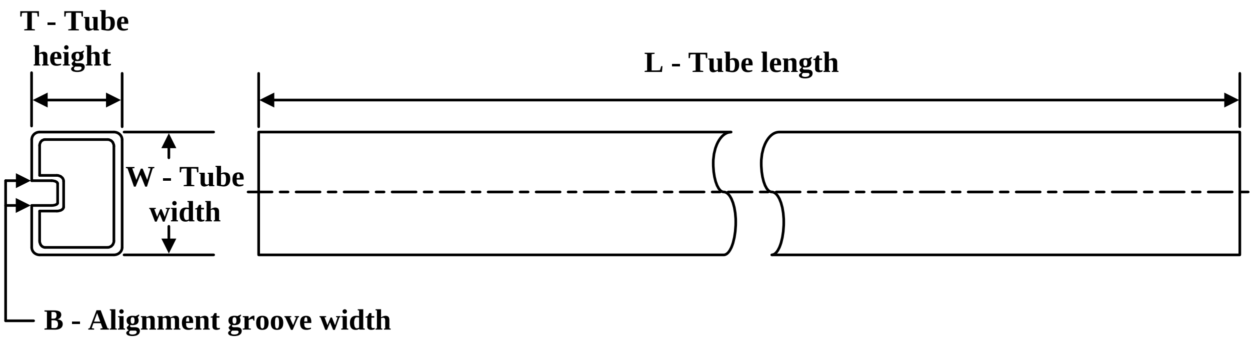
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75ALS172ADWR	SOIC	DW	20	2000	356.0	356.0	45.0

TUBE

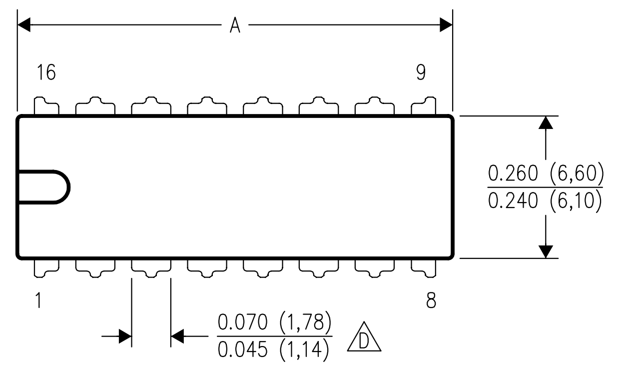


*All dimensions are nominal

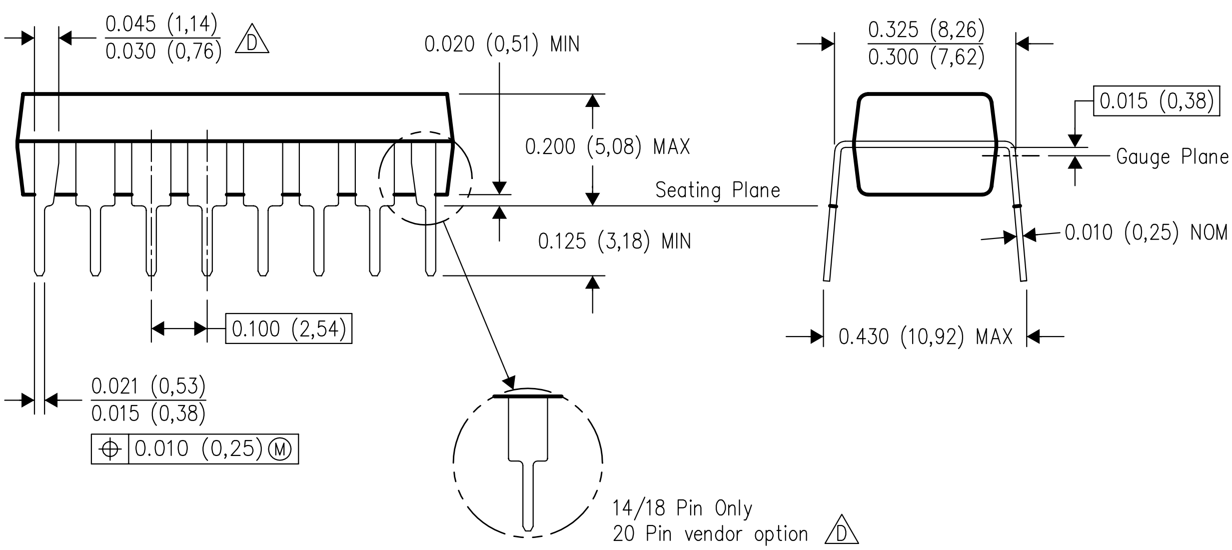
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75ALS172AN	N	PDIP	16	25	506	13.97	11230	4.32
SN75ALS172AN.A	N	PDIP	16	25	506	13.97	11230	4.32

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

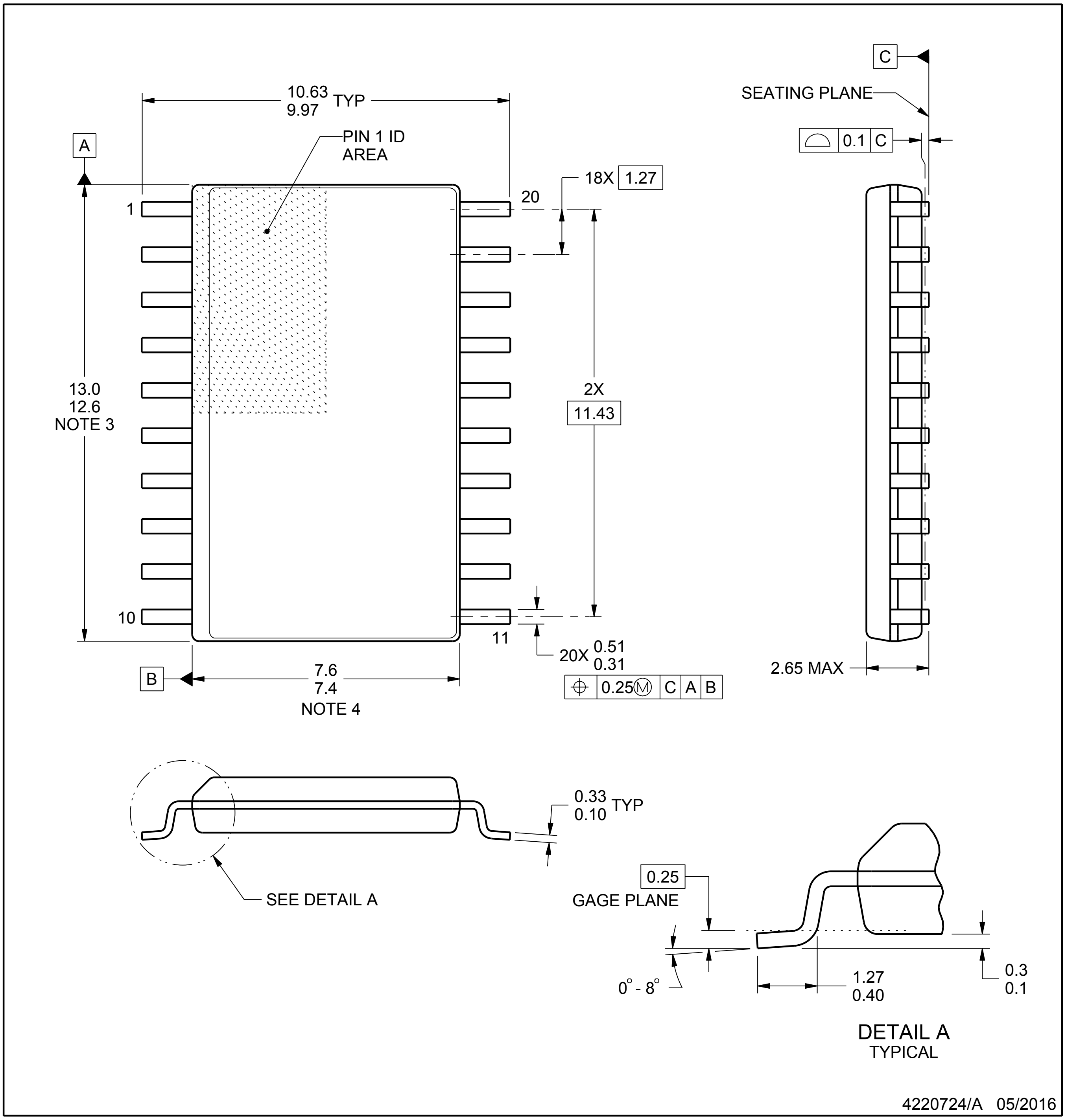


PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
C MS–001 VARIATION	AA	BB	AC	AD



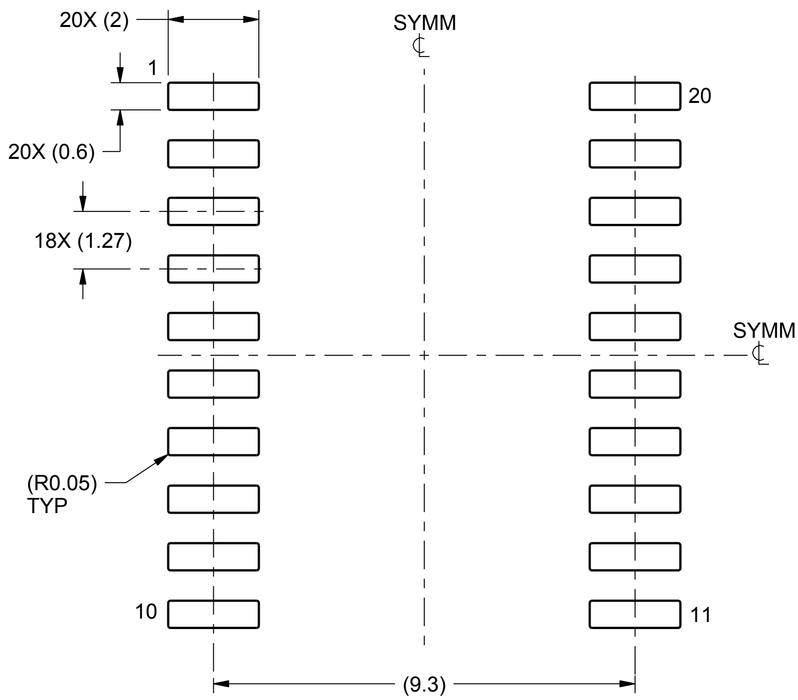
4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

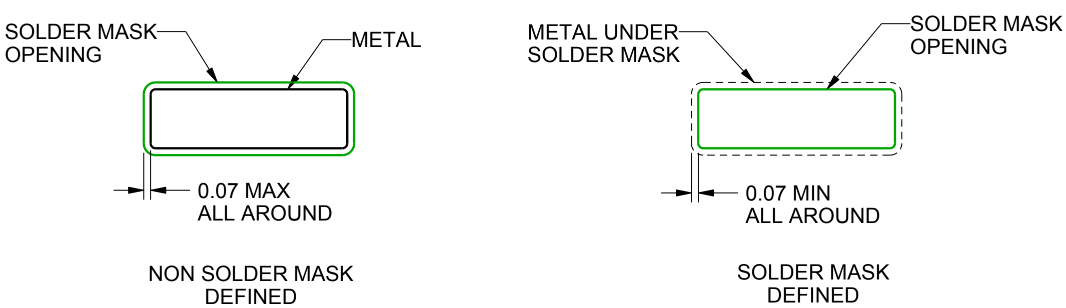


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

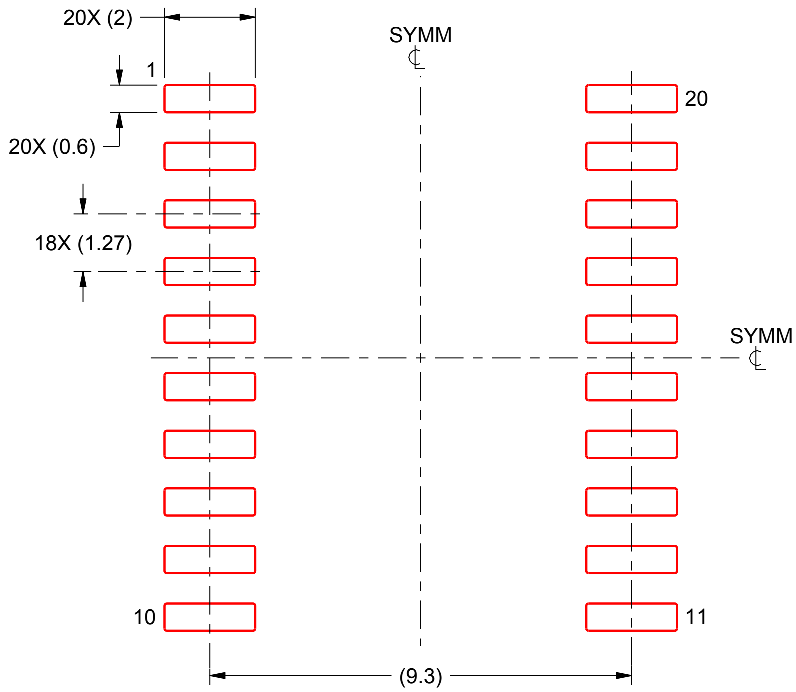


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項