SN75LVPE801 8.0 Gbps SATA Expressイコライザおよびリドライバ

1 特長

- SATA Expressに対応
- イコライゼーションとディエンファシスを選択可能
- ホットプラグ対応
- レシーバ検出およびOOBのサポート
- マルチレート動作
  - SATA: 1.5Gpbs、3.0Gpbs、6.0Gpbs
  - PCIe: 2.5Gbps、5.0Gbps、8.0Gbps
- 40インチ(1.0m)までのFR4 PC基板上で、8.0Gbpsのデータを受信するために適切
- 3GHz時に、受信側で14dBまで、送信側で1.2dBの損失を補償
- 出力スケルチ機能内蔵
- 温度範囲: 0℃～85℃
- 消費電力の自動低減機能により消費電力が90%以上低減
  - 100mW未満(アクティブ・モード、標準値)
  - 11mW未満(自動低消費電力モード、標準値)
- 3.3V単一電源
- ESD過渡電圧に対する強固な保護
  - HBM: 6kV
  - CDM: 1.5kV
- 非常に小さい占有面積: 2mm×2mmのWSONパッケージ

2 アプリケーション

- ノートブックPC
- デスクトップ
- ドッキング・ステーション
- サーバー
- ワークステーション

3 概要

SN75LVPE801は多用途の1チャネル、SATA Express信号コンディショナーで、8Gbpsまでのデータ転送速度に対応しています。このデバイスは、SATA Gen 1、2、3仕様と、PCIe 1.0、2.0、3.0をサポートしています。SN75LVPE801は単一の3.3V電源で動作し、自己バイアス機能付きの100Ωのライン終端があるため、ACカップリングに適しています。入力にはアウト・オブ・バンド(OOB)検出器が組み込まれており、入力差動電圧がスレッショルドより低くなった場合は自動的に出力をスケルチし、同時に安定した同相電圧を維持します。また、このデバイスはSATA標準に従い、拡散スペクトラム・クロック(SSC)転送を処理できるよう設計されています。

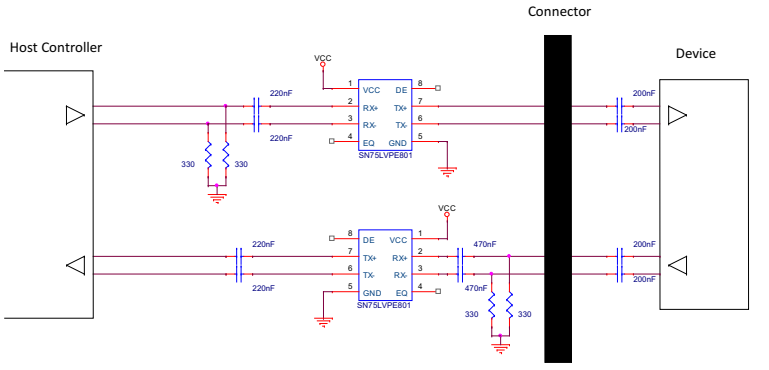
SN75LVPE801は、入力で相互接続損失を処理し、イコライザ設定を選択可能で、チャネルでの損失に応じてプログラム可能です。SN75LVPE801は、8Gbps以下のデータ転送速度について、50インチまでのFR4基板材質上で信号を均等化できます。8Gbpsのデータ転送速度では、40インチまでのFR4材質に対して補償を行えます。イコライゼーション・レベルは、信号制御ピンEQの設定により制御されます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
SN75LVPE801	WSON (8)	2.00mm×2.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

SATA Expressのリファレンス回路図



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4 改訂履歴

日付	改訂内容	注
2016年9月	*	初版

5 概要（続き）

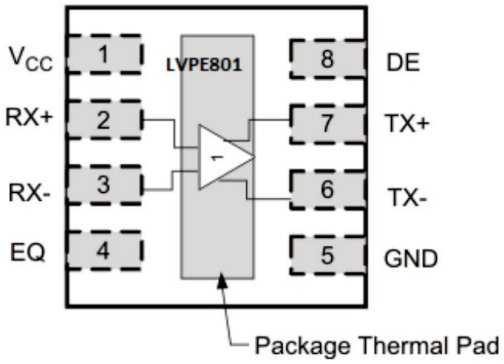
送信側で2つのディエンファシス・レベルを選択でき、0dBまたは1.2dBの追加の高周波損失補償を、出力で提供できます。

このデバイスはホットプラグ対応(1)で、非同期信号の抜き挿し、電源オフ時の抜き挿し、電源オン時の抜き挿し、意図しない抜き挿しなど、デバイスのホット挿入時にデバイスへの損害を防止します。

(1) 差動入力と出力に、ACカップリング・コンデンサを使用する必要があります。

6 Pin Configuration and Functions

DRF Package
8-Pin WSON
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
HIGH SPEED DIFFERENTIAL I/O			
RX+	2	I	Noninverting and inverting CML differential inputs. These pins are tied to an internal voltage bias by dual termination resistor circuit.
RX–	3	I	
TX+	7	O	Noninverting and inverting VML differential outputs. These pins are tied to an internal voltage bias by dual termination resistor circuit.
TX–	6	O	
CONTROL PINS			
EQ	4	I	Selects equalization settings per Table 1. Internally tied to GND.
DE	8	I	Selects de-emphasis settings per Table 1. Internally tied to GND.
POWER			
V_{CC}	1	P	Positive supply must be 3.3 V ±10%
GND	5	G	Supply ground

(1) G = Ground, I = Input, O = Output, P = Power

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_{CC}(2)		–0.5	4	V
Voltage	Differential I/O	–0.5	4	V
	Control I/O	–0.5	V_{CC} + 0.5	
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground pin.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±6000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

typical values for all parameters are at V_{CC} = 3.3 V and T_A = 25°C; all temperature limits are specified by design

		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
	Coupling capacitor	75	100	200	nF
T_A	Operating free-air temperature	0		85	°C

7.4 Thermal Information

THERMAL METRIC(1)		SN75LVPE801 DRF (WSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97.8	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	81.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	65.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	65.6	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	19.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DEVICE PARAMETERS						
ICC_{Max-s}	Active mode supply current	EQ/DE = NC, K28.5 pattern at 8 Gbps, V_{ID} = 700 mV_{pp}		29	40	mA
I_{CCPS}	Auto power save mode I_{CC}	When auto low power conditions are met		3.3	5.9	mA
	Maximum data rate				8	Gbps
OOB						
V_{OOB}	Input OOB threshold	F = 750 MHz	50	70	90	mV_{pp}
$D_{VdiffOOB}$	OOB differential delta				25	mV
D_{VCMOOB}	OOB common-mode delta				50	mV
CONTROL LOGIC						
V_{IH}	High-level input voltage	For all control pins	1.4			V
V_{IL}	Low-level input voltage				0.5	V
VIN_{HYS}	Input hysteresis			115		mV
I_{IH}	High-level input current	V_{IH} = V_{CC} (DE/EQ)			20	µA
I_{IL}	Low-level input current	V_{IL} = 0V (DE/EQ)	10			µA
RECEIVER AC/DC						
Z_{DIFFRX}	Differential input impedance		85	100	115	Ω
Z_{SERX}	Single-ended input impedance		40			Ω
VCM_{RX}	Common-mode voltage			1.7		V
RL_{DiffRX}	Differential mode return loss (RL)	f = 150 MHz to 300 MHz	20	26		dB
		f = 300 MHz to 600 MHz	18	22		
		f = 600 MHz to 1.2 GHz	14	17		
		f = 1.2 GHz to 2.4 GHz	10	12		
		f = 2.4 GHz to 3 GHz	8	12		
		f = 3 GHz to 5 GHz	6	11		
$RX_{DiffRLSlope}$	Differential mode RL slope	f = 300 MHz to 6 GHz (see Figure 6)		–13		dB/dec
RL_{CMRX}	Common-mode return loss	f = 150 MHz to 300 MHz	8	9		dB
		f = 300 MHz to 600 MHz	14	17		
		f = 600 MHz to 1.2 GHz	12	18		
		f = 1.2 GHz to 2.4 GHz	8	10		
		f = 2.4 GHz to 3 GHz	6	8		
		f = 3 GHz to 5 GHz	6	8.5		
V_{diffRX}	Differential input voltage PP	f = 1.5 GHz and 3 GHz	120		1600	mV_{pp}
IB_{RX}	Impedance balance	f = 150 MHz to 300 MHz	30	41		dB
		f = 300 MHz to 600 MHz	34	41		
		f = 600 MHz to 1.2 GHz	24	33		
		f = 1.2 GHz to 2.4 GHz	14	24		
		f = 2.4 GHz to 3 GHz	12	26		
		f = 3 GHz to 5 GHz	6	18		
		f = 5 GHz to 6.5 GHz	5	18		
TRANSMITTER AC/DC						
Z_{diffTX}	Pair differential impedance		85	100	122	Ω
Z_{SETX}	Single-ended input impedance		40			Ω
$V_{TXtrans}$	Sequencing transient voltage	Transient voltages on the serial data bus during power sequencing (lab load)	–1.2	0.3	1.2	V

Electrical Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RL_{DiffTX}	Differential mode return loss	f = 150 MHz to 300 MHz	14	22		dB
		f = 300 MHz to 600 MHz	12	21		
		f = 600 MHz to 1.2 GHz	11	18		
		f = 1.2 GHz to 2.4 GHz	10	14		
		f = 2.4 GHz to 3 GHz	10	14		
		f = 3 GHz to 5 GHz	8	14		
$TX_{DiffRLSlope}$	Differential mode RL slope	f = 300 MHz to 3 GHz (see Figure 6)		–13		dB/dec
RL_{CMTX}	Common-mode return loss	f = 150 MHz to 300 MHz	10	20		dB
		f = 300 MHz to 600 MHz	9	16		
		f = 600 MHz to 1.2 GHz	8	13.5		
		f = 1.2 GHz to 2.4 GHz	6	8.5		
		f = 2.4 GHz to 3 GHz	5	8		
		f = 3 GHz to 5 GHz	4	7		
IB_{TX}	Impedance balance	f = 150 MHz to 300 MHz	34	38		dB
		f = 300 MHz to 600 MHz	32	38		
		f = 600 MHz to 1.2 GHz	24	33		
		f = 1.2 GHz to 2.4 GHz	18	25		
		f = 2.4 GHz to 3 GHz	18	25		
		f = 3 GHz to 5 GHz	12	21		
		f = 5 GHz to 6.5 GHz	8	21		
$Diff_{VppTX}$	Differential output voltage swing	f = 3 GHz (under no interconnect loss)	400	650	900	mV_{pp}
VCM_{AC_TX}	TX AC CM voltage	At 1.5 GHz		15	50	mV_{pp}
		At 3 GHz		10	26	dBmV (rms)
		At 6 GHz		12	30	dBmV (rms)
VCM_{TX}	Common-mode voltage			1.70		V
TRANSMITTER JITTER 3 Gbps						
DJ_{TX}	Residual deterministic jitter	VID = 500 mV_{pp}, UI = 333 ps, K28.5 control character, see Figure 7		0.12	0.19	UI_{pp}
RJ_{TX}	Random jitter	VID = 500 mV_{pp}, UI = 333 ps, K28.7 control character, see Figure 7		1	2	ps-rms
TRANSMITTER JITTER 6 Gbps						
DJ_{TX}	Residual deterministic jitter	VID = 500 mV_{pp}, UI = 167 ps, K28.5 control character, see Figure 7		0.12	0.34	UI_{pp}
RJ_{TX}	Random jitter	VID = 500 mV_{pp}, UI = 167 ps, K28.7 control character, see Figure 7		0.95	2	ps-rms
TRANSMITTER JITTER 8 Gbps						
DJ_{TX}	Residual deterministic jitter	VID = 500 mV_{pp}, UI = 125 ps, K28.5 control character, see Figure 7	4.7	5.76	8.7	(ps) (DD)
RJ_{TX}	Random jitter	VID = 500 mV_{pp}, UI = 125 ps, K28.5 control character, see Figure 7	0.93	0.94	0.95	ps-rms
DJ_{TX}	Residual deterministic jitter	VID = 500 mV_{pp}, UI = 125 ps, K28.7 control character, see Figure 7	0.8	1.24	2.7	(ps) (DD)
RJ_{TX}	Random jitter	VID = 500 mV_{pp}, UI = 125 ps, K28.7 control character, see Figure 7	0.9	0.92	0.93	ps-rms

7.6 Timing Requirements

			MIN	TYP	MAX	UNIT
DEVICE PARAMETERS						
t_{PDelay}	Propagation delay	Measured using K28.5 pattern (see Figure 1)		275	350	ps
$AutoLP_{ENTRY}$	Auto low power entry time	Electrical idle at input (see Figure 3)		11		µs
$AutoLP_{EXIT}$	Auto low power exit time	After first signal activity (see Figure 3)		33	50	ns
OOB						
t_{OOB1}	OOB mode enter	See Figure 2		1	5	ns
t_{OOB2}	OOB mode exit	See Figure 2		1	5	ns
RECEIVER AC/DC						
$t_{20\text{-}80RX}$	Rise and fall time	Rise times and fall times measured between 20% and 80% of the signal. SATA 8 Gbps speed measured 1" from device pin.	62		75	ps
t_{skewRX}	Differential skew	Difference between the single-ended mid-point of the RX+ signal rising and falling edge, and the single-ended mid-point of the RX– signal falling and rising edge.			30	ps
TRANSMITTER AC/DC						
$t_{20\text{-}80TX}$	Rise and fall time	Rise times and fall times measured between 20% and 80% of the signal. At 8 Gbps under no load conditions measured at the pin.	44	58	85	ps
t_{skewTX}	Differential skew	Difference between the single-ended mid-point of the TX+ signal rising edge and falling edge, and the single-ended mid-point of the TX– signal falling edge and rising edge, D1, D0 = V_{CC}		2	15	ps
$t_{xR/Flmb}$	TX rise and fall imbalance	At 8 Gbps		6%	20%	
$t_{xAmplmb}$	TX amplitude imbalance			1%	10%	
TRANSMITTER JITTER						
	Rise and Fall time		46.5 %	47.5 %	48.3 %	
	Rise and Fall mismatch			1.5%	3%	

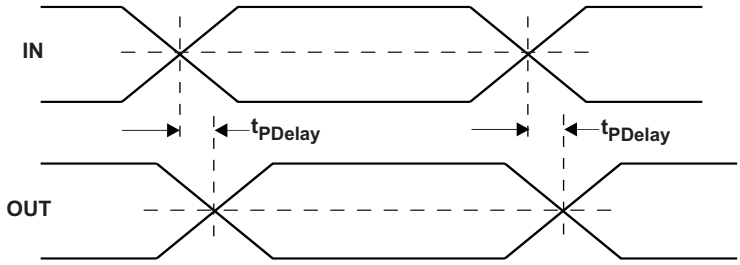


Figure 1. Propagation Delay Timing Diagram

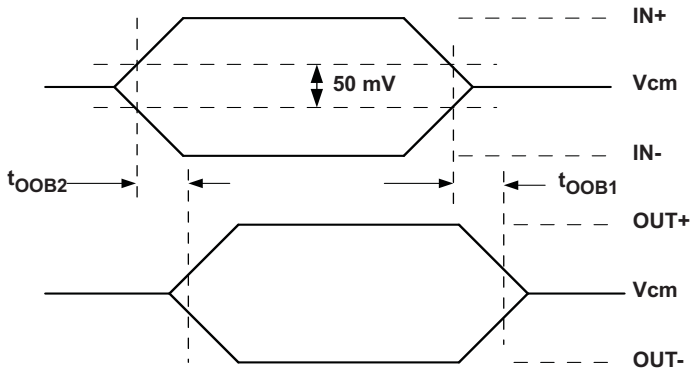


Figure 2. OOB Enter and Exit Timing

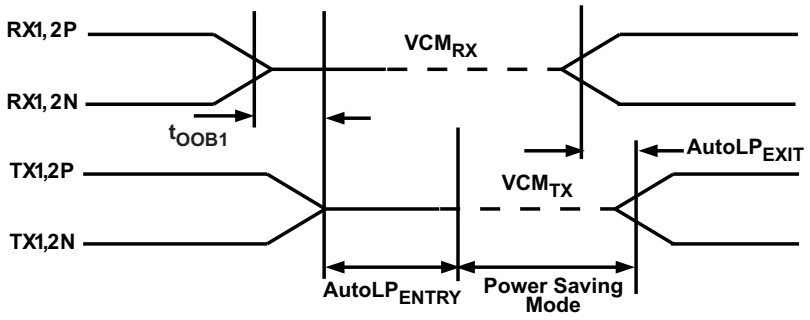
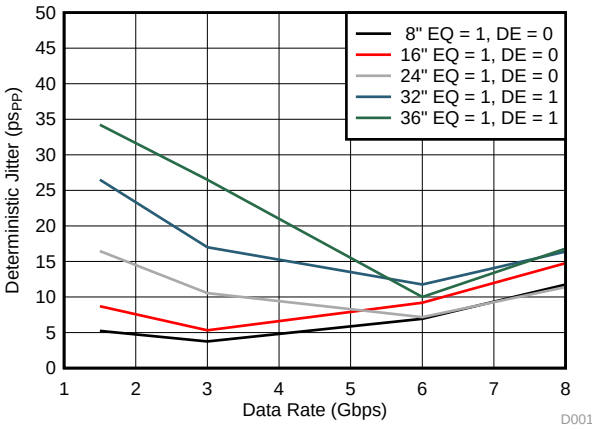


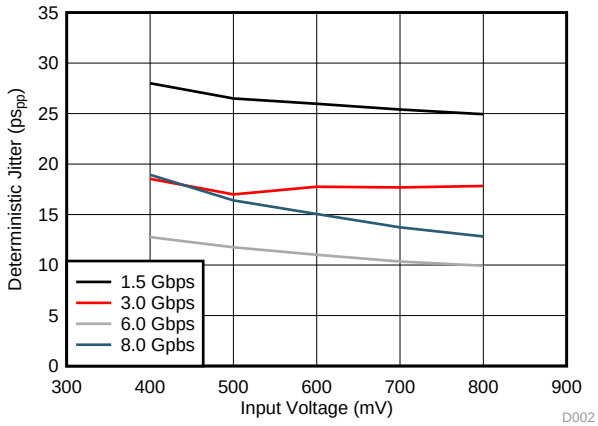
Figure 3. Auto Low Power Mode Entry and Exit Timing

7.7 Typical Characteristics



A function of input trace length of 4 mil FR-4

Figure 4. Deterministic Jitter vs Data Rate



Function of data rate after equalizing for 32" of input
FR = 4 trace, EQ = 1, DE = 1

Figure 5. Deterministic Jitter vs Launch Amplitude

8 Parameter Measurement Information

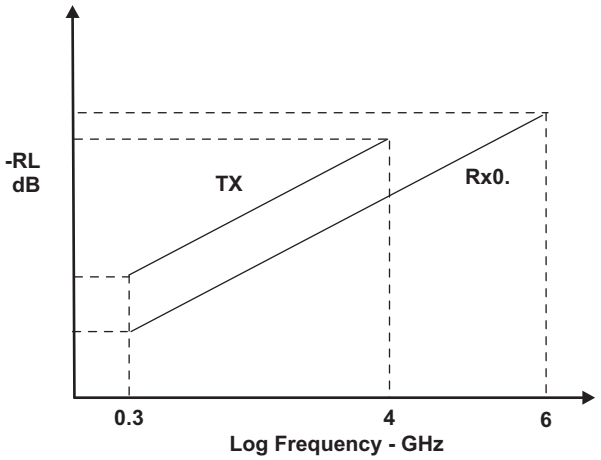


Figure 6. TX, RX Differential Return Loss Limits

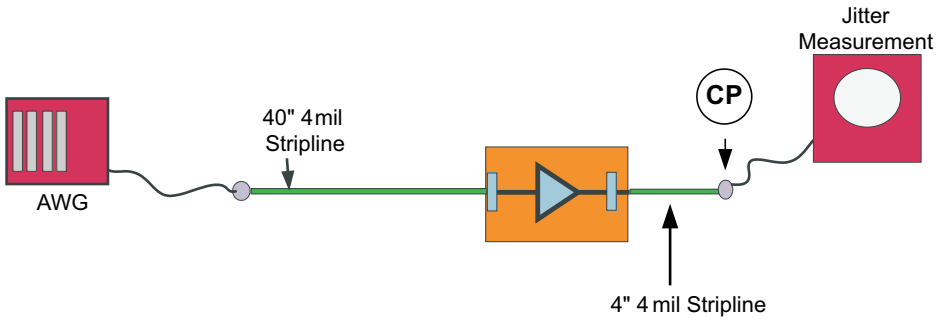


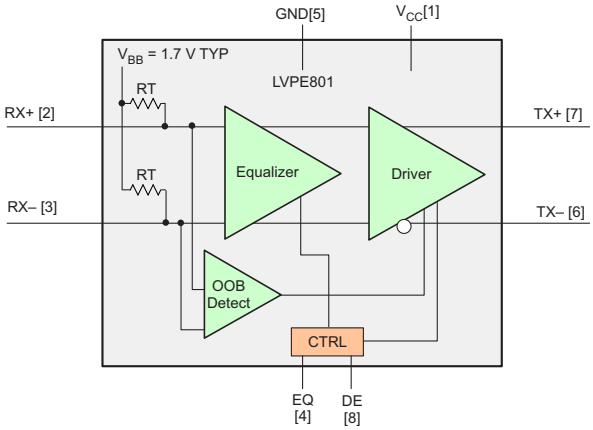
Figure 7. Jitter Measurement Test Condition

9 Detailed Description

9.1 Overview

The SN75LVPE801 is a single channel equalizer and redriver. The device operates over a wide range of signaling rates, supporting operation from DC to 8 Gbps. The wide operating range supports SATA Gen 1,2,3 (1.5 Gbps, 3.0 Gbps, and 6.0 Gbps respectively) as well as PCI Express 1.0, 2.0, 3.0 (2.5 Gbps, 5.0 Gbps, and 8.0 Gbps). The device also supports SATA Express (SATA 3.2) which is a form factor specification that allows for SATA and PCI Express signaling over a single connector.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 SATA Express

SATA Express (sometimes SATAe) is an electro-mechanical standard that supports both SATA and PCI Express storage devices. SATAe is standardized in the SATA 3.2 standard. The standard is concerned with providing a smooth transition from SATA to PCIe storage devices. The standard provides for standardized cables and connectors, and muxes the PCIe and SATA lanes at the host side so that either SATA compliant or PCIe compliant devices may operate with a host.

SATAe provides support for SATA1, SATA2 and SATA3 devices (operating from 1.5 Gbps to 6.0 Gbps), as well as PCIe1, PCIe2 and PCIe3 devices (operating from 2.5 Gbps to 8.0 Gbps).

The SN75LVPE801 provides for equalization and re-drive of a single channel input signal complying with any of the SATA or PCIe standards available with SATAe.

The SATAe standard provides for a mechanism for a host to recognize and detect whether a SATA or PCIe device is plugged into the host. See the *Typical SATA Applications* section for the details of the SATA Express Interface Detect operation.

9.3.2 Receiver Termination

The receiver has integrated terminations to an internal bias voltage. The receiver differential input impedance is nominally 100 Ω, with a ±15% variation.

For PCI Express compatibility it is necessary to include 330 Ω pull-down resistors between the connector and the AC capacitors, refer to Figure 24 for more information.

9.3.3 Receiver Internal Bias

The SN75LVPE801 receiver is internally biased to 1.7 V, providing support for AC coupled inputs.

Feature Description (continued)

9.3.4 Receiver Equalization

The SN75LVPE801 incorporates programmable equalization. The EQ input controls the level of equalization that is used to open the eye of the received input signal. If the EQ input is left open, or pulled LO, 8 dB (at 4 GHz) of equalization is applied. When the EQ input is HIGH, the equalization is set to 16 dB (again at 4 GHz).Table 1 shows the equalization values discussed.

Table 1. EQ and DE Settings

EQ	EQUALIZATION dB (at 8 Gbps)	DE	DE-EMPHASIS
0 (default)	8	0 (default)	0
1	16	1	–1.2

9.3.5 OOB/Squelch

The SN75LVPE801 receiver incorporates an Out-Of-Band (OOB) detection circuit in addition to the main signal chain receiver. The OOB detector continuously monitors the differential input signal to the device. The OOB detector has a 50-mVpp entry threshold. If the differential signal at the receiver input is less than the OOB entry threshold, the device transmitter transitions to squelch. The SN75LVPE801 enters squelch within 5 ns of the input signal falling below the OOB entry threshold. The SN75LVPE801 continues to monitor the input signal while in squelch. While in squelch, if the OOB detector determines that the input signal now exceeds the 90 mVpp exit threshold, the SN75LVPE801 exits squelch within 5 ns. See Figure 8.

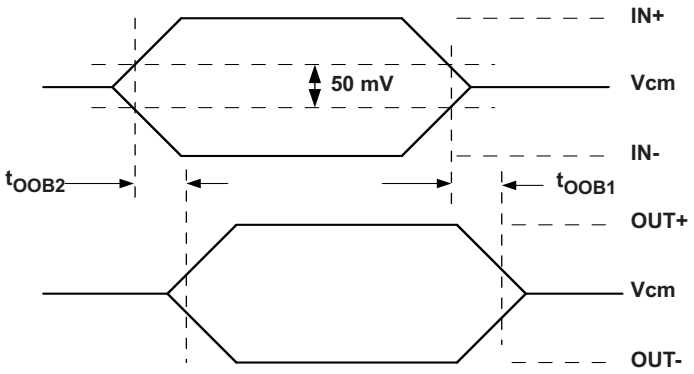


Figure 8. OOB Enter and Exit Timing
Receiver Input Termination is Disabled

When the SN75LVPE801 enters squelch state the transmitter output is squelched. The transmitter non-inverting (TX+) output and the transmitter inverting output (TX-) are both driven to the transmitter nominal common mode voltage which is 1.7 V .

9.3.6 Auto Low Power

The SN75LVPE801 also includes an Auto Low Power Mode (ALP). ALP is entered when the differential input signal has been less than 50 mV for > 10 µs. The device enters and exits Low Power Mode by actively monitoring the input signal level. In this state the device selectively shuts off internal circuitry to lower power by > 90% of its normal operating power. While in ALP mode the device continues to actively monitor input signal levels. When the input signal exceeds the OOB exit threshold level, the device reverts to the active state. Exit time from Auto Low Power Mode is < 50 ns (max). See Figure 9.

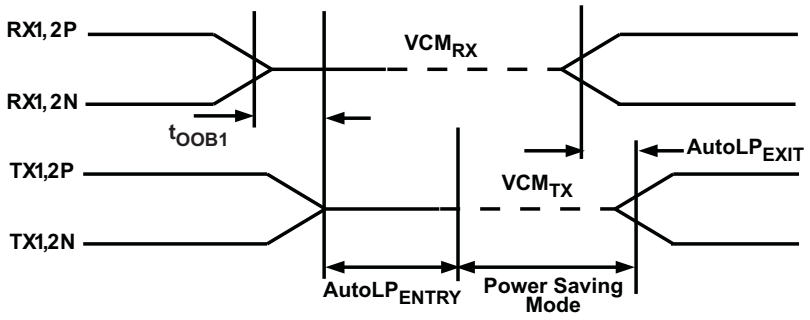


Figure 9. Auto Low Power Mode Entry and Exit Timing

9.3.7 Transmitter Output Signal

The SN75LVPE801 differential output signal is 650 mVpp when de-emphasis is disabled (DE input is open or pulled low).

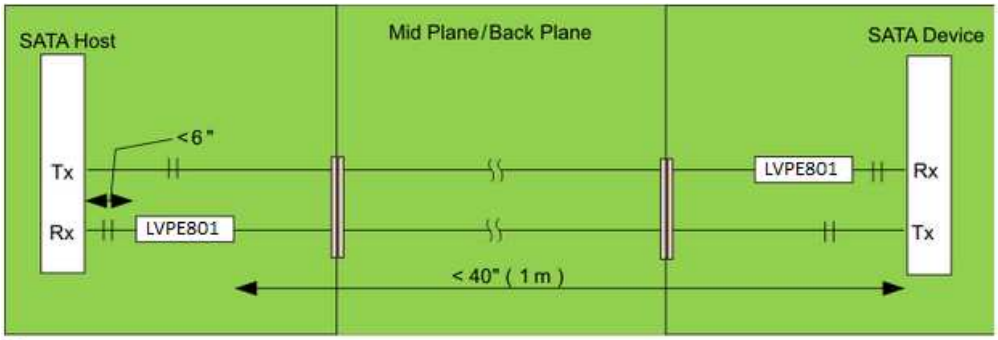
9.3.8 Transmitter Common Mode

The SN75LVPE801 transmitter common mode output is set to 1.7 V.

9.3.9 De-Emphasis

The SN75LVPE801 transmitter incorporates programmable de-emphasis to provide signal conditioning to offset the anticipated channel losses based on expected use cases for the device. Figure 10 shows an example of a SATA host communicating with a SATA device through a backplane. In such a use case, an SN75LVPE801 would be located at the end of the interconnect channels (i.e. at the device end for the host TX channel, and at the host end for the host RX channel. These locations are selected based on the signal conditioning that is incorporated into the SN75LVPE801. The SN75LVPE801 provides up to 16 dB of equalization, while supporting up to 1.2 dB of de-emphasis. The optimum location would therefore be at the end of the interconnect, allowing the receiver equalization to address the majority of the channel loss, while the de-emphasis would be employed to overcome the much shorter interconnect length.

The DE input controls the amount of de-emphasis that is applied at the transmitter output. The de-emphasis selections are shown in Table 1. When DE is left open, or pulled low, de-emphasis shall be off. When DE is pulled HIGH, 1.2 dB of de-emphasis is used at the transmitter output.



Note:
Trace lengths are suggested values based on TI HSPICE simulations (done over programmable limits of input EQ) to meet SATA loss and jitter spec.

Actual trace length supported by the LVPE801 may be more or less than suggested values and will depend on board layout, trace widths and number of connectors used in the high speed signal path.

Figure 10. Trace Length Example

9.3.10 Transmitter Termination

The SN75LVPE801 transmitter includes integrated terminations. The receiver differential output impedance is nominally 100 Ω, with a ≤ 22% variation.

9.4 Device Functional Modes

9.4.1 Active

Active mode is the normal operating mode. When power is applied to the device, and the differential input signal to the receiver is greater than 90 mV_{pp}, the device is in active mode and meets all the specifications in the data sheet.

9.4.2 Squelch

When the device is powered, and the differential input signal to the receiver is less than 50 mV_{pp}, the device is in squelch mode. In squelch mode the transmitter outputs are both set to VCM_{TX} or 1.7 V.

9.4.3 Auto Low Power

When the device is powered and the differential input signal to the receiver has been less than 50 mV_{pp} for greater than 10 ns, the device transitions to Auto Low Power (ALP) mode. In ALP, the transmitter outputs are both set to VCM_{TX}. In addition, while in ALP, the device shuts off internal circuitry to lower power to less than 10% of the power in the Active mode.

10 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

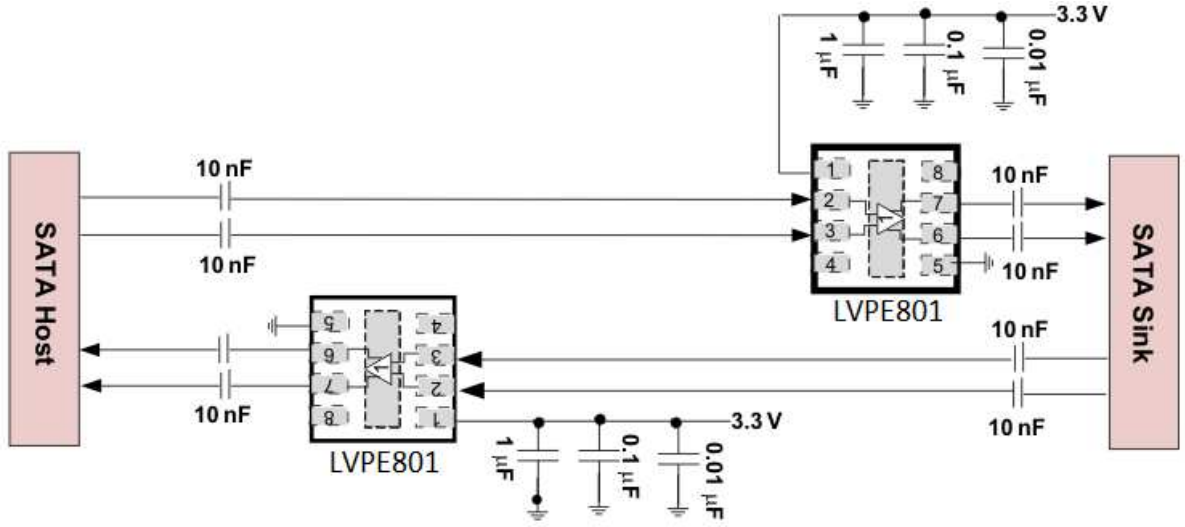
10.1 Application Information

The SN75LVPE801 can be used for SATA applications as well as SATA Express applications. The device supports SATA Gen1, Gen2, and Gen3 applications with data rates from 1.5 to 8 Gbps. The built-in equalization circuits provide up to 16 dB of equalization at 4 GHz. This equalization can support SATA GEN2 (3 Gbps) applications over up to 50 inches of FR-4 material. The same 16 dB equalizer is suited to SATA Gen3 (8 Gbps) applications up to 40 inches of FR4.

In addition to SATA applications, the SN75LVPE801 can support SATA Express applications. SATA Express provides a standardized interface to support both SATA (Gen1, Gen2, and Gen3) and PCI Express (PCIe 1.0, 2.0 and 3.0).

All applications of the SN75LVPE801 share some common applications issues. For example, power supply filtering, board layout, and equalization performance with varying interconnect losses. Other applications issues are specific, such as implementing receiver detection for SATA Express applications. The Typical Application examples demonstrate common implementations of the SN75LVPE801 supporting SATA, as well as SATA Express applications.

10.2 Typical SATA Applications



(1) Place supply caps close to the device pin

(2) EQ and DE selection at 8 dB and 0 dB respectively

(3) Actual EQ and DE settings depend on the device placement relative to the host and SATA connector

Figure 11. Typical Device Implementation

Typical SATA Applications (continued)

10.2.1 Design Requirements

DESIGN PARAMETERS	VALUE
SATA Signaling Rate	1.5 - 6.0 Gbps
AC Coupling Capacitance	10 nF
Interconnect Characteristic Impedance	100 Ohms
Interconnect Length	Up to 50" FR4 for SATA Gen2 Up to 40" FR4 for SATA Gen3
Termination Resistance	100 Ohms differential integrated into TX and RX

10.2.2 Detailed Design Procedure

Figure 11 shows a typical SATA Application. The SATA host, which may be a notebook or desktop, communicates with a SATA sink, which could be a SSD mass storage device. The SATA host and sink communicate over a backplane differential pair, or a SATA cable. When using the SN75LVPE801 as an equalizer/redriver, the designer would optimally place the SN75LVPE801 close to the end of the interconnect. The SN75LVPE801 provides up to 16 dB of equalization, and up to 1.2 dB of de-emphasis. Placing the SN75LVPE801 close to the end of the interconnect allows the device equalizer to address the majority of the high frequency losses introduced in the channel.

Ensure that the channel loss for the interconnect material and length is matched reasonably well to the selectable equalization and de-emphasis settings available on the SN75LVPE801. The table above provides an estimate of the amount of FR4 material that could be used as a function of the signal rate. In any case, channel modeling would be prudent to ensure that the SATA host, interconnect, SATA equalizer/re-driver, and SATA Sink can establish and maintain a low BER link.

The AC coupling capacitors of 10 nF are chosen to comply with the SATA standard (< 12 nF)

Often a designer may not be sure whether a signal conditioning device like the SN75LVPE801 is needed in their specific application. The SN75LVPE801 allows the user to take the guess work of using a signal conditioning device in a SATA link. With the SN75LVPE801 the designer has the option to use or remove the device based on signal conditioning needs. Figure 12 shows guidelines that could be used to allow in situ testing when a board is available. The designer would start with 0 Ω resistors in place to determine if the eye quality at the end of the link is satisfactory. If the eye opening is not sufficient, the 0 Ω resistors could be replaced with the SN75LVPE801.

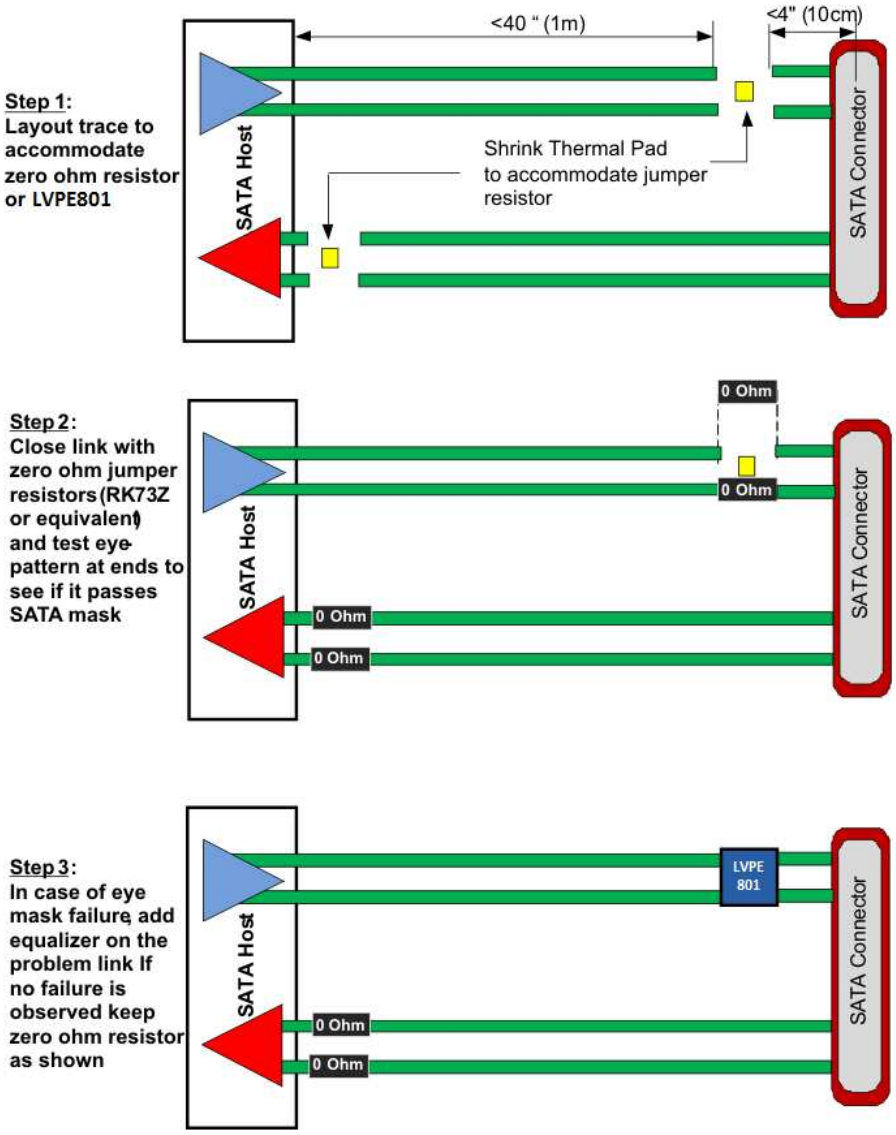


Figure 12. Implementation Guideline

To demonstrate the effectiveness of the SN75LVPE801 signal conditioning for varied configurations that may be encountered, Figure 13 is used as a reference. A Gen3, 6 Gbps SATA host communicates with a sink located at point B. The host and sink are separated by "X+Y" inches, where X represents the distance between the host and the SN75LVPE801, while Y represents the distance between the SN75LVPE801 and the sink. The *Application Curves* are for a 6-Gbps K28.5 pattern, with V_{CC} = 3.3 V and at an ambient temperature of 25°C.

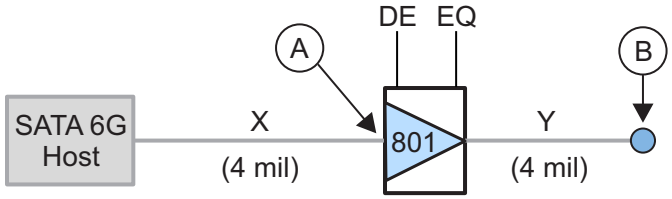
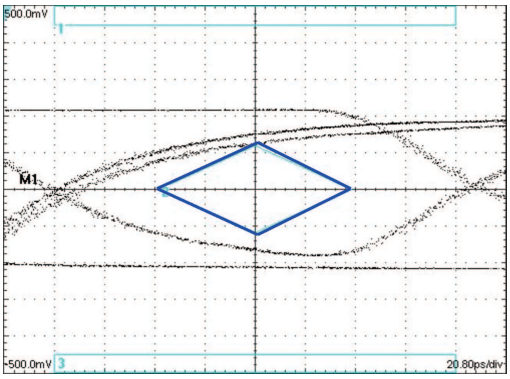


Figure 13. Test Points

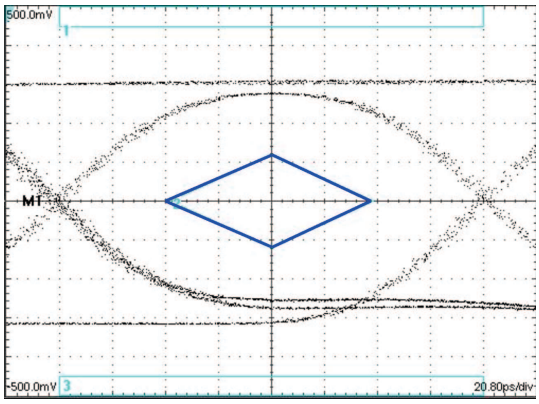
10.2.3 Application Curves

All graphs at 6 Gbps



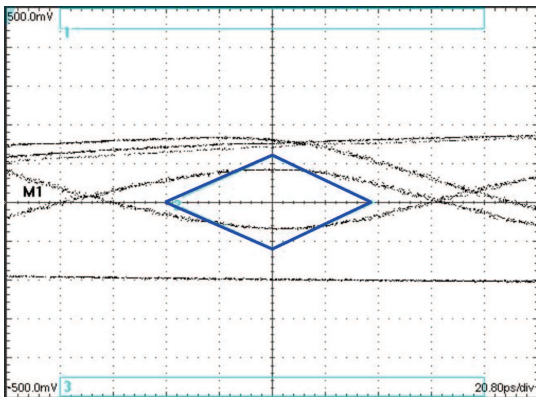
DE = 1 EQ = 0

Figure 14. Eye Pattern at A → X = 8”; Y = 2”



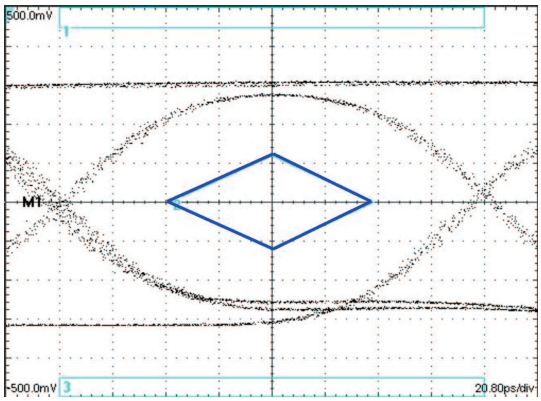
DE = 1 EQ = 0

Figure 15. Eye Pattern at B → X = 8”; Y = 2”



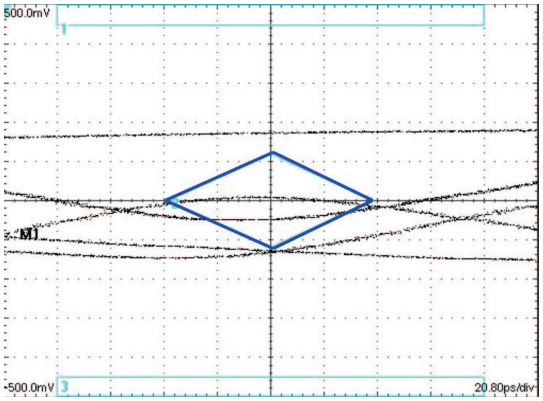
DE = 1 EQ = 0

Figure 16. Eye Pattern at A → X = 16”; Y = 2”



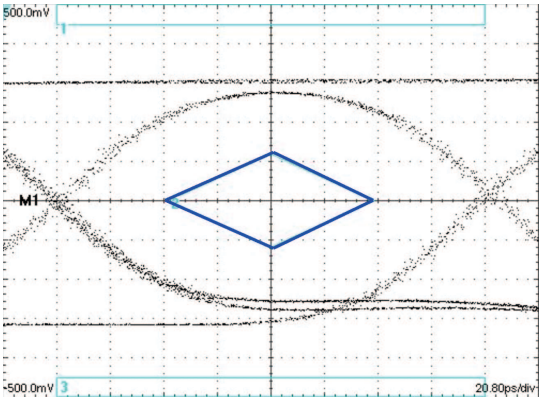
DE = 1 EQ = 0

Figure 17. Eye Pattern at B → X = 16”; Y = 2”



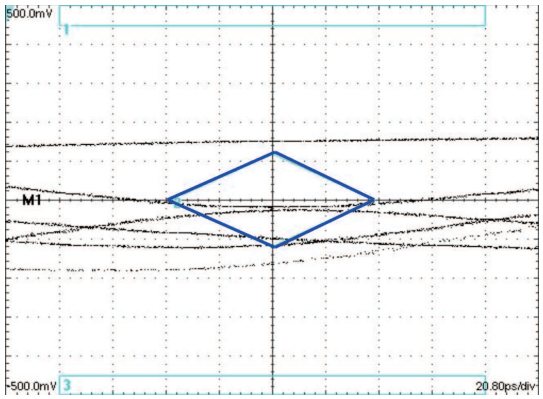
DE = 1 EQ = 0

Figure 18. Eye Pattern at A → X = 24”; Y = 2”



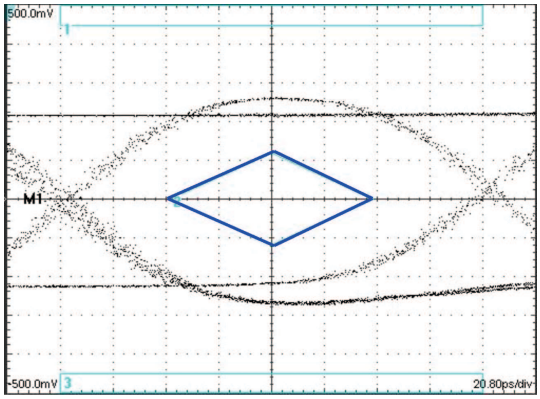
DE = 1 EQ = 0

Figure 19. Eye Pattern at B→ X = 24”; Y = 2”



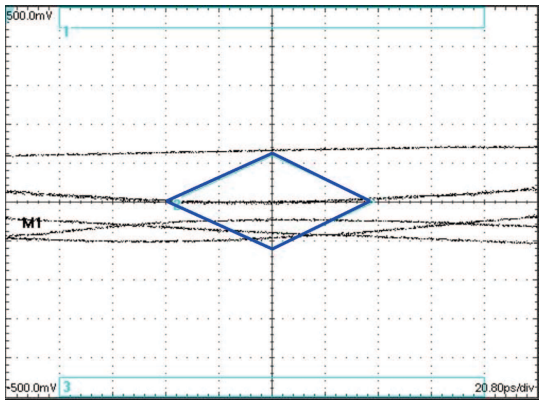
DE = 1 EQ = 1

Figure 20. Eye Pattern at A → X = 32”; Y = 2”



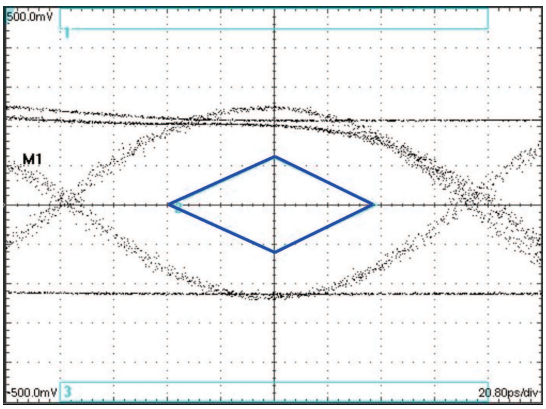
DE = 1 EQ = 1

Figure 21. Eye Pattern at B → X = 32”; Y = 2”



DE = 1 EQ = 1

Figure 22. Eye Pattern at A → X = 40”; Y = 2”



DE = 1 EQ = 1

Figure 23. Eye Pattern at B → X = 40”; Y = 2”

10.2.4 SATA Express Applications

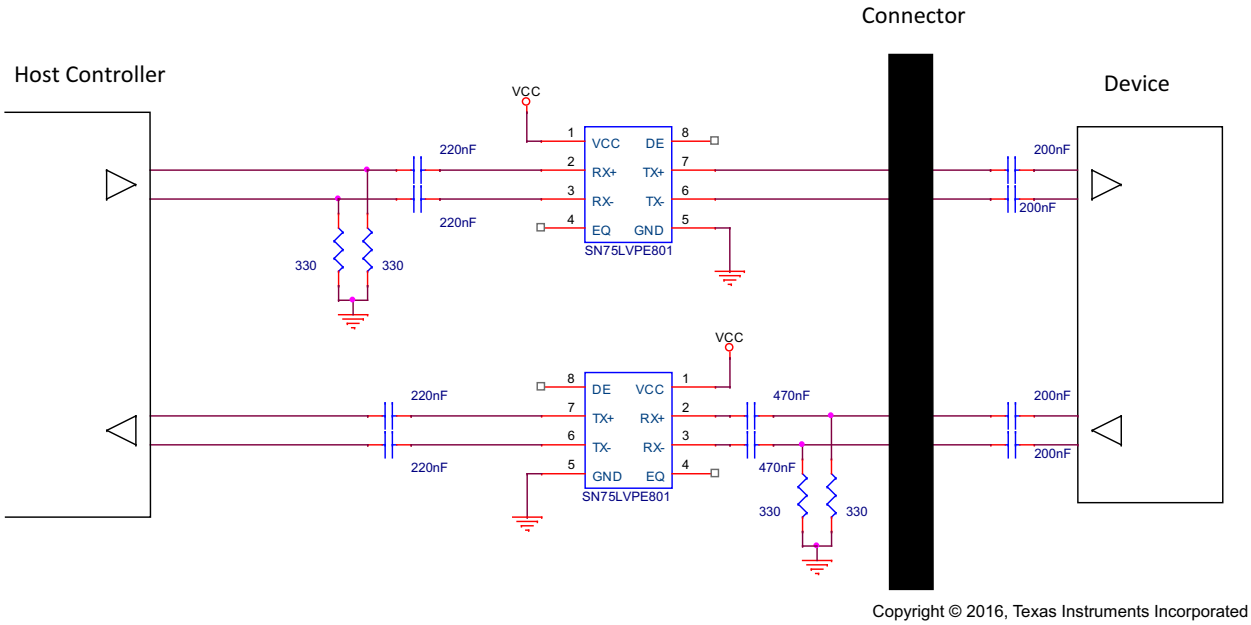


Figure 24. SN75LVPE801 SATA Express Reference Schematic
EQ: 8 dB when Floated, DE: 0 dB when Floated

10.2.4.1 Design Requirements

DESIGN PARAMETERS	VALUE
SATA Express Signaling Rate	1.5 - 8.0 Gbps
AC Coupling Capacitance	200 - 220 nF
Interconnect Characteristic Impedance	100 Ω
Interconnect Length	Up to 50" FR4 for SATA Gen2 Up to 40" FR4 for SATA Gen3
Receiver pull-down terminations	330 Ω
Termination Resistance	100 Ohms differential integrated into TX and RX

10.2.4.2 Detailed Design Procedure

Figure 24 is a reference schematic of a SATAe implementation using the SN75LVPE801. With a SATAe design, both SATA and PCI Express must be supported. SATAe supports both cabled and direct connections. Using a cabled application as an example, the SATAe power connector includes an Interface Detect (IFDet, power connector pin P4) signal that indicates whether a SATA client or a PCIe client is connected.

When the SATAe host determines that a PCIe client is connected, the SATAe host performs receiver detection. Receiver detection determines the presence of a client by detecting the load impedance. The transmitter performs a common mode voltage shift, and measures the rate at which the voltage at the transmitter output changes. The rate of change indicates if a client is present (fast charging when a low impedance load is present, or slow charging when the load is open or high impedance). With the implementation in Figure 24, 330-Ω pulldowns have been inserted between the host and the SN75LVPE801. The pulldown resistors indicate to the host that a client is present. While an actual client would be expected to have an active load of 50 Ω single ended, the 330 Ω is chosen here to meet two requirements. The 330 Ω is low enough to force the SATAe host to decide that a receiver is present, while also high enough to only marginally affect the load when the SN75LVPE801 is active, and presenting a 50-Ω load. With the 50 Ω and 330 Ω are both present, the parallel combination of 43 Ω is satisfactory for most applications.

Assuming that the SATAe host has detected (via IFDet) that a SATA client is present, the SATAe host communicates with the client via the SN75LVPE801. The SATA standard does not have a receiver detection mode as is present in PCIe. A SATA host does use OOB signaling to communicate identification information. The SN75LVPE801 incorporates an OOB detector in order to support OOB signaling through the device. The OOB detector drives a squelch circuit on the SN75LVPE801 output transmitter. (See *OOB/Squelch* for more details on the OOB/Squelch circuitry.)

Returning again to Figure 24, we see 200-nF AC coupling capacitors on the device or client side of the interface. These capacitors allow interfacing to both SATA and PCIe clients. In the case of a PCIe client, the 200 nF is within the acceptable range for all PCIe devices. When a SATA client is present, the 200 nF capacitor has little effect on the overall link, as it appears in series with the 12-nF (max) AC coupling capacitor incorporated into the SATA client. The 200 nF in series with the 12 nF presents an effective capacitance of 11.3 nF, as expected less than the 12-nF maximum permitted.

The physical placement of the resistors on the high-speed transmission lines can be made as not to create a stub on the transmission line by using resistors with the 0201 package size, an example is provided in Figure 25.

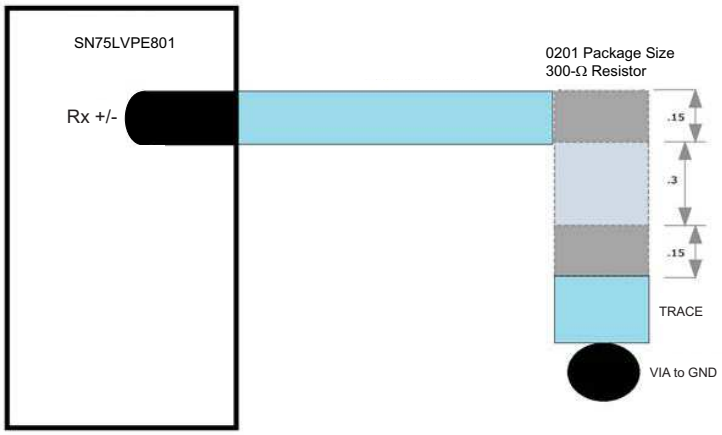


Figure 25. Resistor Placement to Avoid Stub (All Dimensions in mm)

10.2.4.3 Application Curve

Eye-diagrams were taken on the SN75LVPE801 configured as in Figure 24 above. Testing was performed at a PCIe 3.0 speed of 8Gbps.

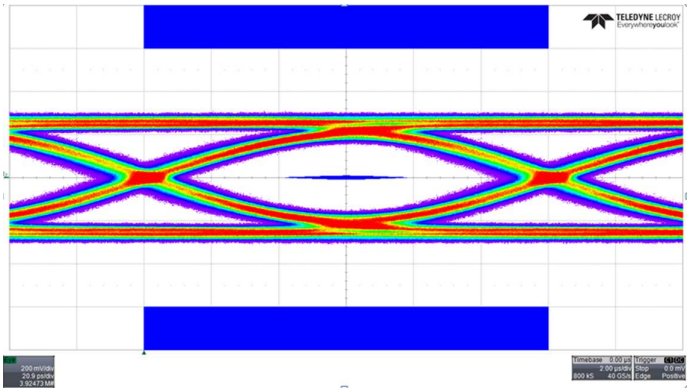


Figure 26. SN75LVPE801 8-Gbps Eye-Diagram

10.2.5 PCIe Applications

PCIe-only applications are implemented in a manner very similar to SATA Express applications as covered in *Detailed Design Procedure*. Looking at Figure 27, and comparing it to the SATA Express application in Figure 24, a single change is noted. For PCIe applications the 220 nF AC-coupling capacitors on the Host-to-Device link are relocated from the Device side of the connector to the Host side. No other changes are required.

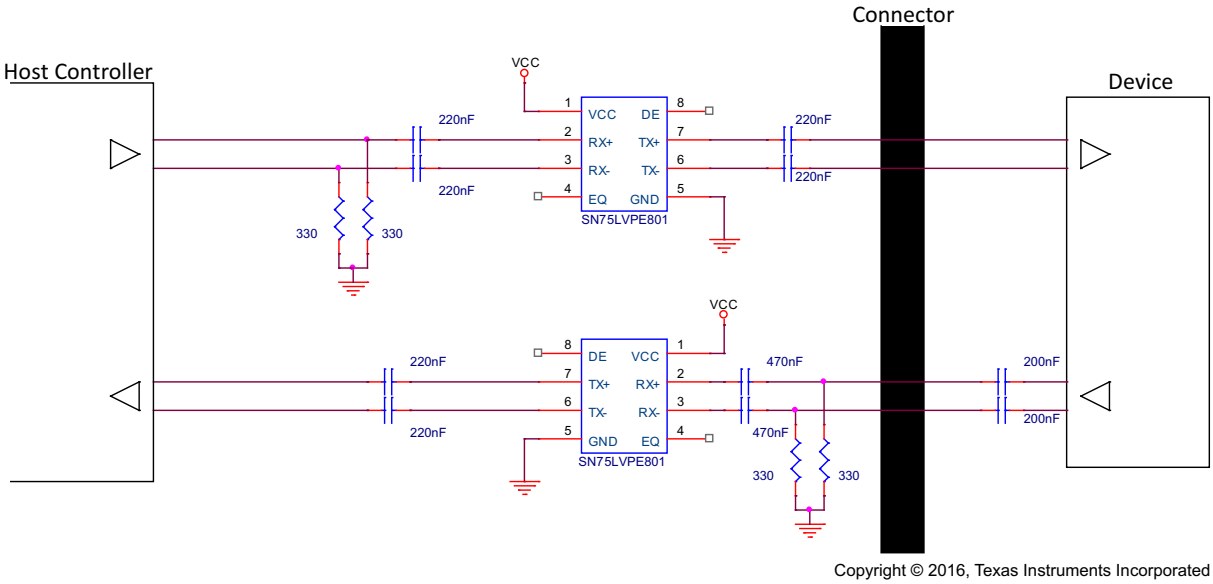


Figure 27. SN75LVPE801 PCI-Express Reference Schematic
EQ: 7 dB when Floated, DE: 0 dB when Floated

11 Power Supply Recommendations

The SN75LVPE801DRF is designed to operate from a single 3.3-V supply. Always practice proper power-supply sequencing procedure. Apply V_{CC} first before any input signals are applied to the device. The power-down sequence is in reverse order.

12 Layout

12.1 Layout Guidelines

12.1.1 Return Current and Plane References

High frequency return signal/current is defined as the path that a signal follows back to its original source as all signals flow in a closed loop. Minimizing the loop area of the closed loop is beneficial for both EMI (Electro-Magnetic Interference) reduction and signal integrity.

The best way to minimize loop area is to always have a signal reference their nearest solid ground or power plane. Obstructions to the return signal causes signal integrity problems like reflections, crosstalk, undershoot and overshoot.

Signals can reference either power or ground planes, but ground is preferred. Without solid plane references, single ended and differential impedance control is very hard to accomplish; crosstalk to other signals may happen as the return signals have no other path. This type of crosstalk is difficult to troubleshoot.

Symmetric pairing of solid planes in the layer stackup can significantly reduce warping of the PCB during the manufacturing process. Warping of the PCB is crucial to minimize on boards that uses BGA components.

12.1.2 Split Planes – What to Avoid

Never route signals over splits in their perspective reference planes.

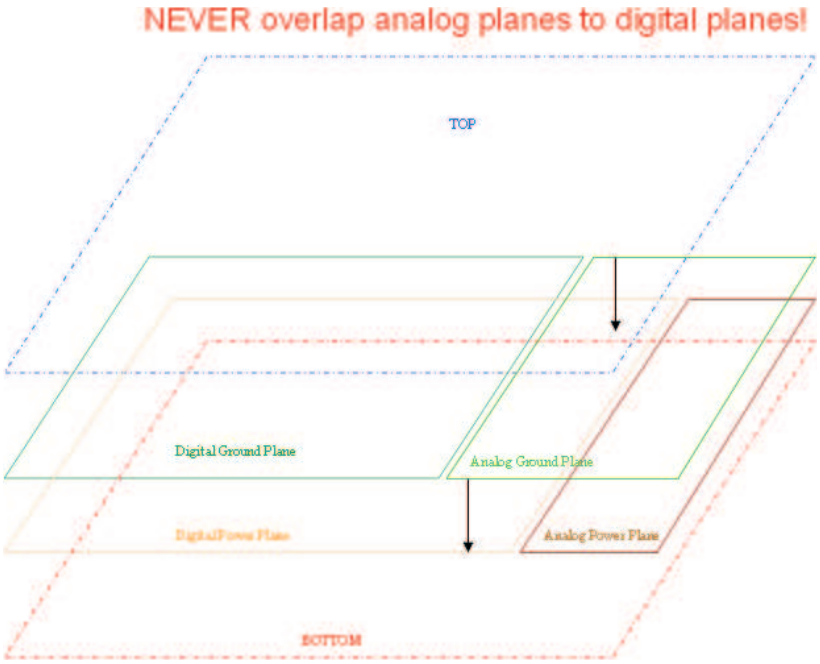


Figure 28. Overlapping Analog and Digital Planes

Layout Guidelines (continued)

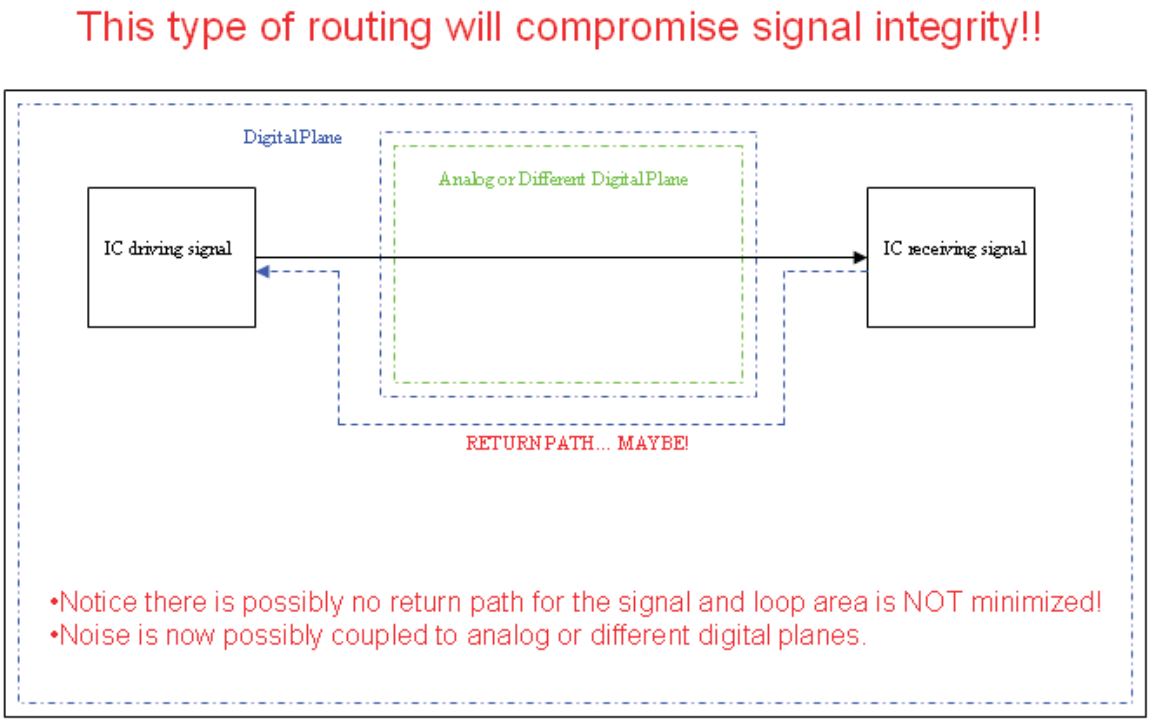


Figure 29. Incorrect Routing

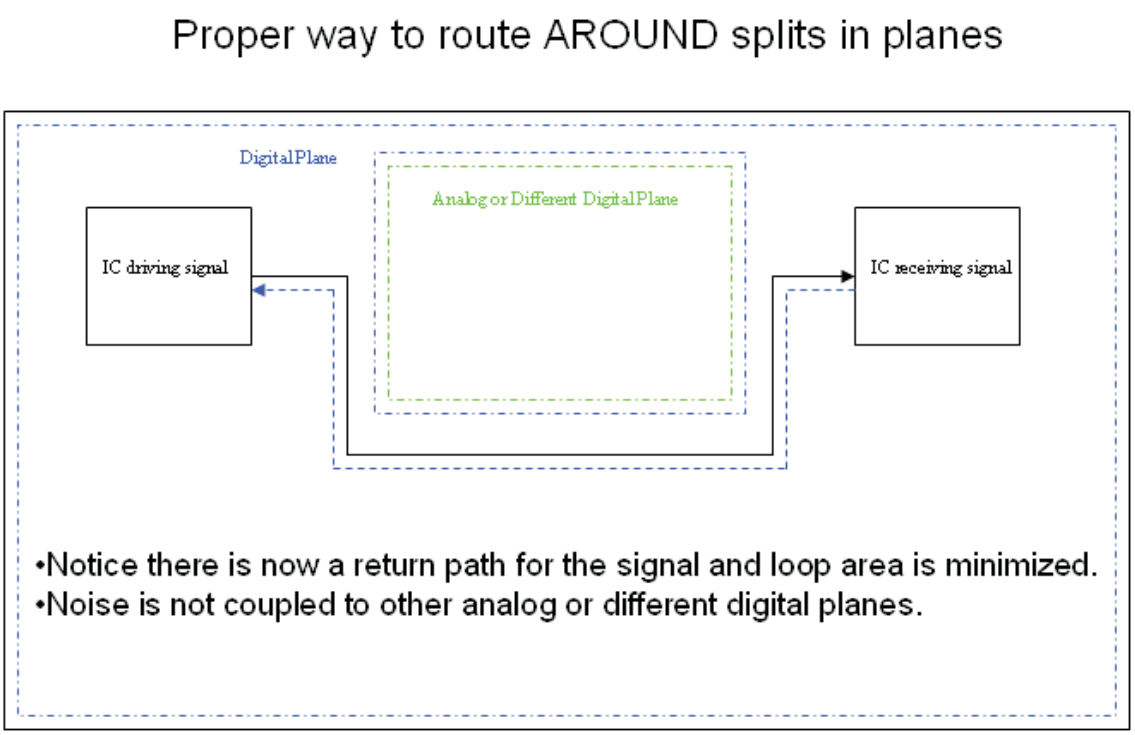


Figure 30. Proper Routing

Layout Guidelines (continued)

12.1.3 Avoiding Crosstalk

Crosstalk is defined as interference from one trace to another by either or both inductive and capacitive coupling. Best ways to avoid crosstalk are:

- Provide stable reference planes for all high speed signals (as noted in previous sections).
- Use the 3W rule (3 times the width of trace for separation) where applicable on all signals, but absolutely use on clock signals.
- Use ground traces/guards around either *victim* or *aggressor* signals prone to crosstalk.
- When space is constrained and limited on areas of the PCB to route parallel buses, series or end termination resistors can be used to route traces closer than what is normally recommended. However, calculations and simulations must be done to validate the use of series or end termination resistors to eliminate crosstalk.

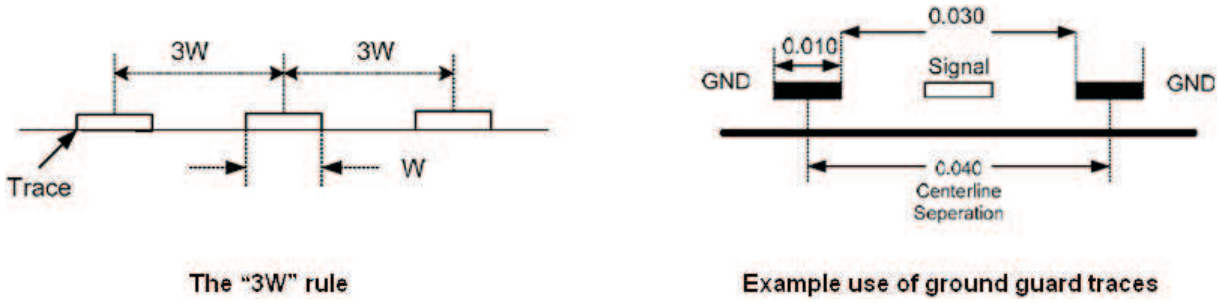


Figure 31. Ways to Avoid Crosstalk

12.2 Layout Example

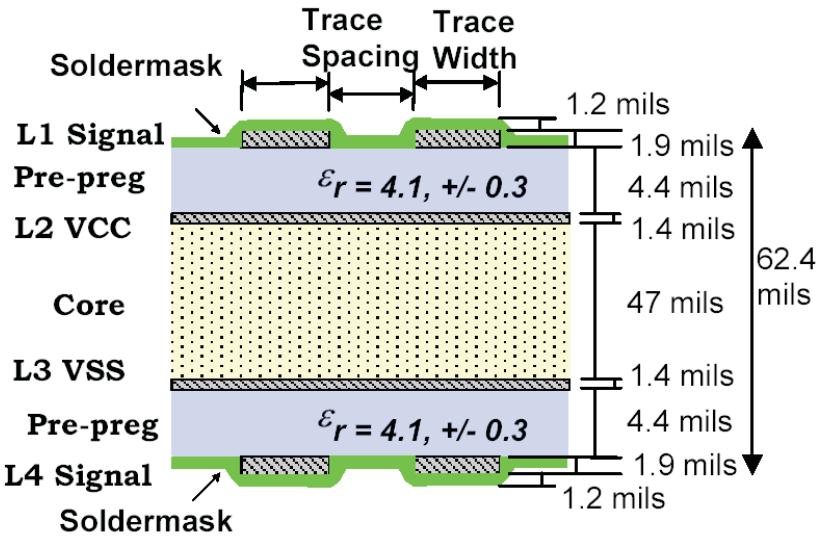


Figure 32. Printed-Circuit Board Stackup (FR-4 Example)

Layout Example (continued)

4 Layer

Layer 1	(Top)
Layer 2	(GND)
Layer 3	(PWR)
Layer 4	(Bottom)

6 Layer

Layer 1	(Top)
Layer 2	(GND)
Layer 3	(Signal)
Layer 4	(Signal)
Layer 5	(PWR)
Layer 6	(Bottom)

10 Layer

Layer 1	(Top)
Layer 2	(GND)
Layer 3	(Signal)
Layer 4	(Signal)
Layer 5	(PWR)
Layer 6	(GND)
Layer 7	(Signal)
Layer 8	(Signal)
Layer 9	(GND)
Layer 10	(Bottom)

PCB layer configuration suggestions for stackup symmetry and signal integrity.

Figure 33. PCB Layer Configuration Suggestions

13 デバイスおよびドキュメントのサポート

13.1 デバイス・サポート

13.1.1 Third-Party Products Disclaimer

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13.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 商標

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すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN75LVPE801DRFR	Active	Production	WSON (DRF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 85	801
SN75LVPE801DRFR.B	Active	Production	WSON (DRF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 85	801
SN75LVPE801DRFT	Active	Production	WSON (DRF) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 85	801
SN75LVPE801DRFT.B	Active	Production	WSON (DRF) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 85	801

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

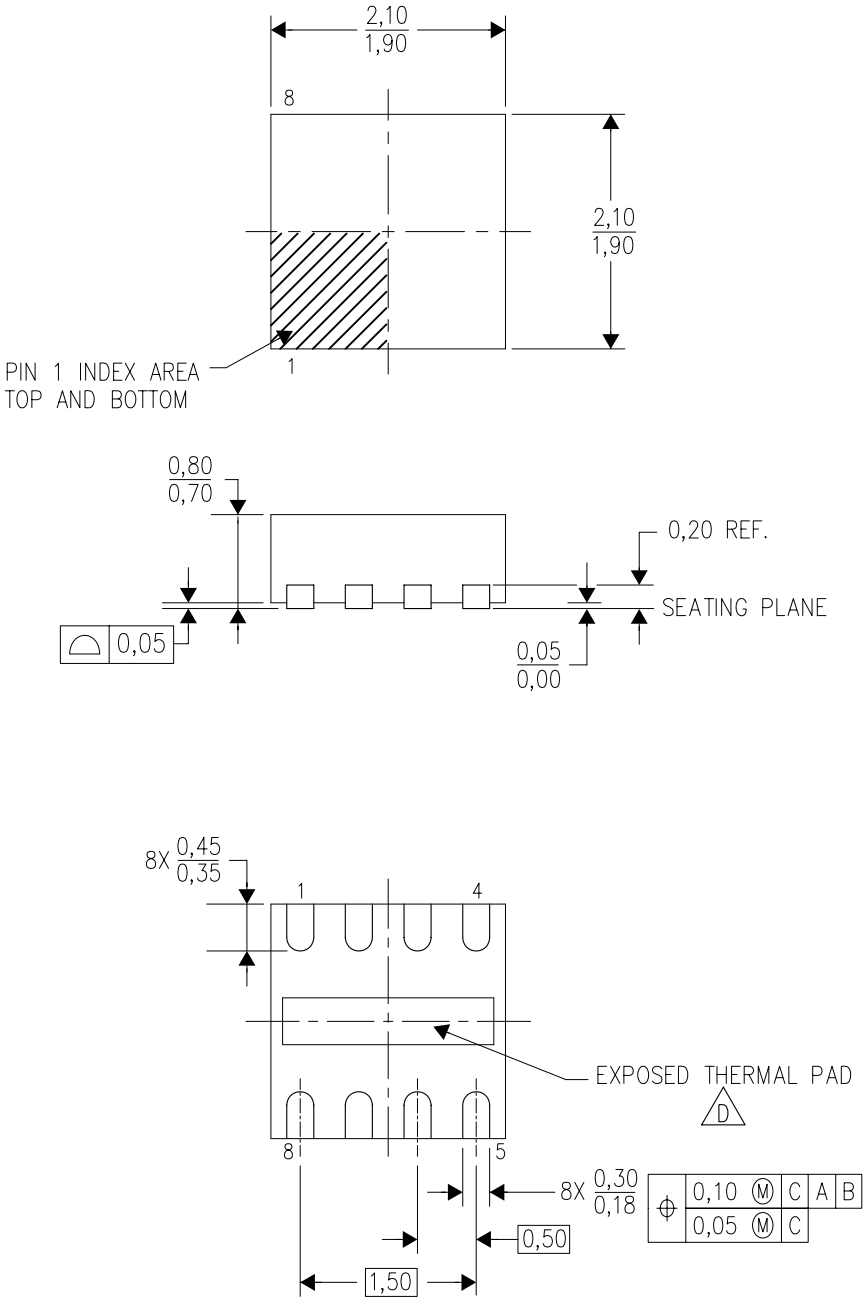
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

DRF (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



4205287/E 10/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The Package thermal pad must be soldered to the board for thermal and mechanical performance. See product data sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–229.

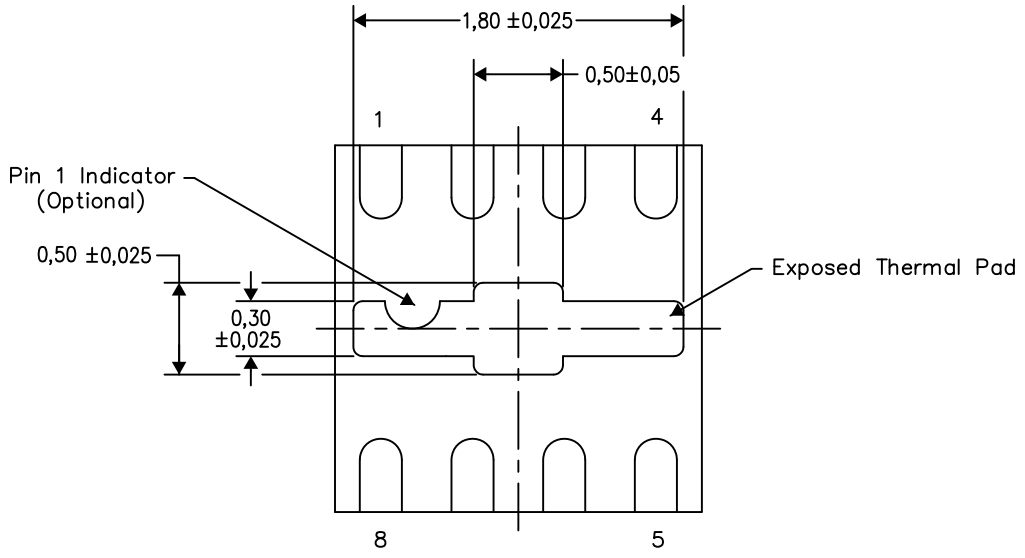
DRF (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



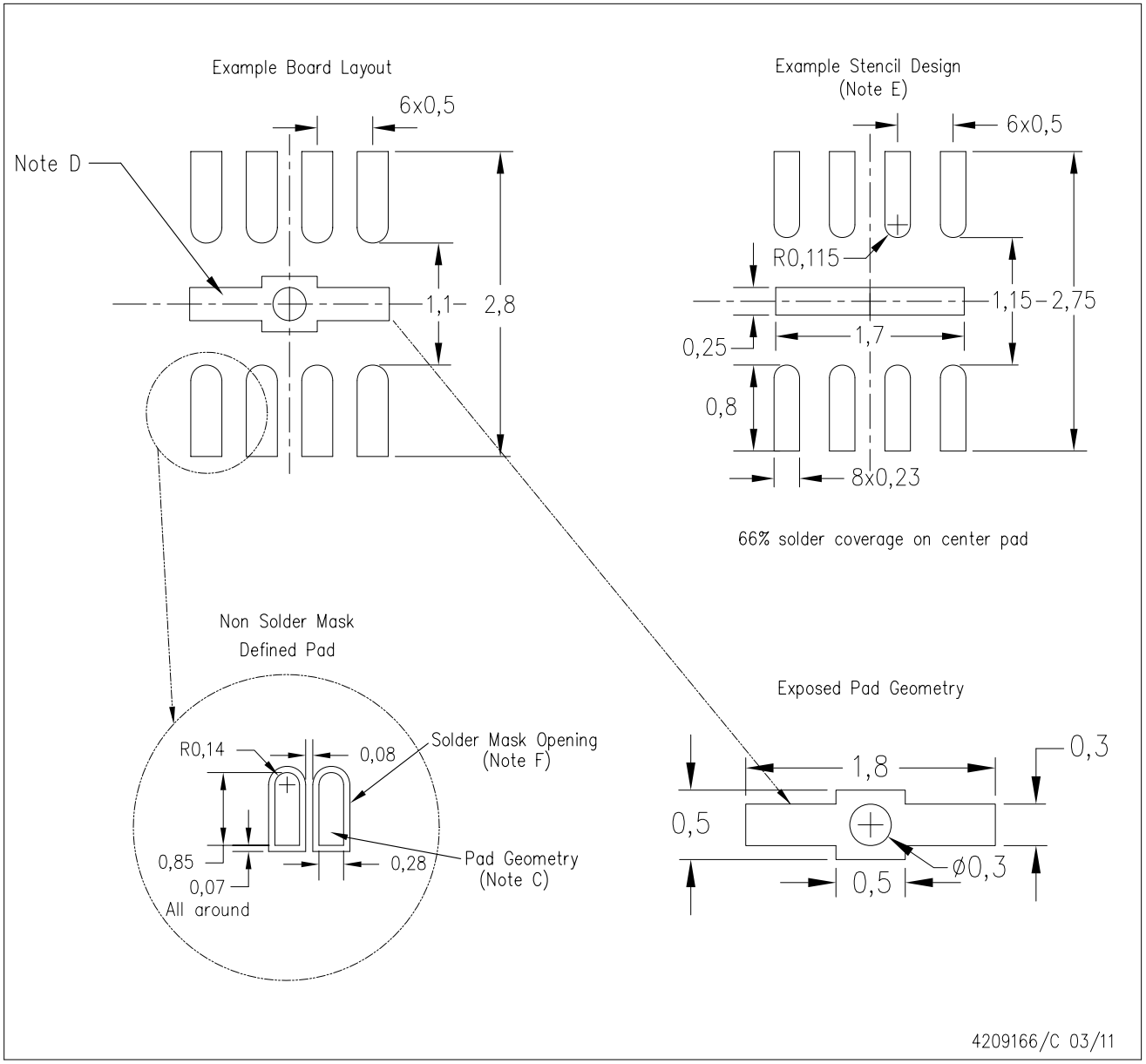
Bottom View

Exposed Thermal Pad Dimensions

4206840/H 12/14

NOTE: A. All linear dimensions are in millimeters

DRF (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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最終更新日：2025 年 10 月