

# TAS5414C 4チャンネル、アフターマーケット車載用クラスDアンプ

## 1 特長

- 4チャンネルのシングル・エンド・アナログ入力、クラスDオーディオ・アンプ
- 10% THD+N時の標準出力電力
  - 14.4Vで4Ωに対して28W/Ch
  - 14.4Vで2Ωに対して50W/Ch
  - 24Vで4Ωに対して79W/Ch
  - 24Vで2Ωに対して150W/Ch (PBTL)
- チャンネルの平行化(PBTL)によって大電流アプリケーションに対応
- THD+N < 0.02%、1kHz、4Ωに対して1W
- ポップ音およびクリック音低減テクノロジー(特許取得済み)
  - ソフト・ミュートとゲイン・ランプ制御
  - 同相ランプ
- AM干渉防止(特許取得済み)
- サイクル単位電流制限(特許取得済み)
- 75dB PSRR
- 4アドレスのI<sup>2</sup>Cシリアル・インターフェイスによるデバイス構成と制御
- チャンネル・ゲイン: 12dB、20dB、26dB、32dB
- 負荷診断機能:
  - 出力開路および負荷短絡
  - 出力と電源、出力とグラウンドの間の短絡
  - ツイータ検出(特許取得済み)
- 保護および監視機能:
  - 短絡保護
  - ロード・ダンパ保護(50V)
  - 偶発的なグラウンド・オープン/電源オープンへの耐性
  - 音楽再生中の出力DCレベル検出(特許取得済み)
  - 過熱保護
  - 過電圧および電圧低下
  - クリップ検出
- 64ピンのQFP (PHD)パワー・パッケージ、ヒート・スラグ付き
- 周囲温度範囲 -20°C~105°C

## 2 アプリケーション

- アフターマーケット用ヘッドユニット
- アフターマーケット用外部オーディオ・アンプ

## 3 概要

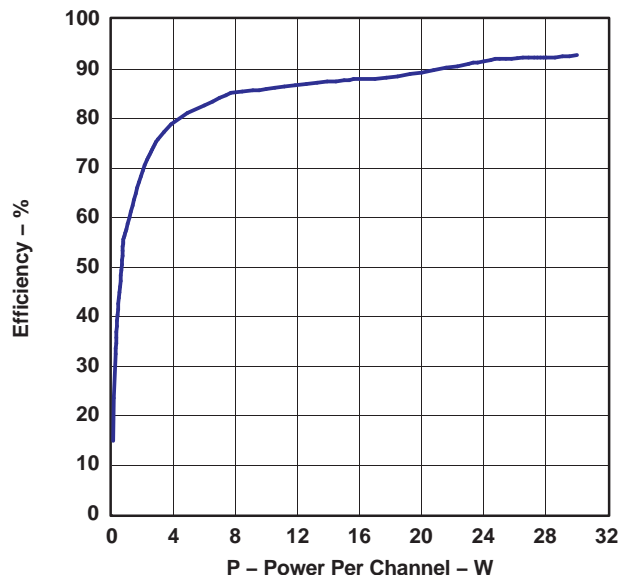
TAS5414Cは4チャンネルのクラスDオーディオ・アンプで、車載用ヘッド・ユニットおよび外部アンプ・モジュール用に設計されています。14.4V電源から1%未満のTHD+Nで、4Ωに対して連続的に23Wを4チャンネルで供給できます。各チャンネルは、1%のTHD+Nで2Ω~38Wを供給することもできます。TAS5414Cはシングル・エンドのアナログ入力を使用します。デバイスのクラスDのPWMトポロジにより、従来のリア・アンプ・ソリューションと比べて効率が劇的に向上します。これによって、一般的な音楽再生の状況において、アンプの消費電力が約10分の1に低減します。デバイスには負荷診断機能が組み込まれており、出力の誤接続を検出して診断できるため、製造プロセスにおいてテスト時間を短縮するために役立ちます。

### 製品情報<sup>(1)</sup>

| 型番       | パッケージ      | 本体サイズ(公称)       |
|----------|------------|-----------------|
| TAS5414C | HTQFP (64) | 14.00mm×14.00mm |

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

### チャンネルごとの出力と効率との関係



G007

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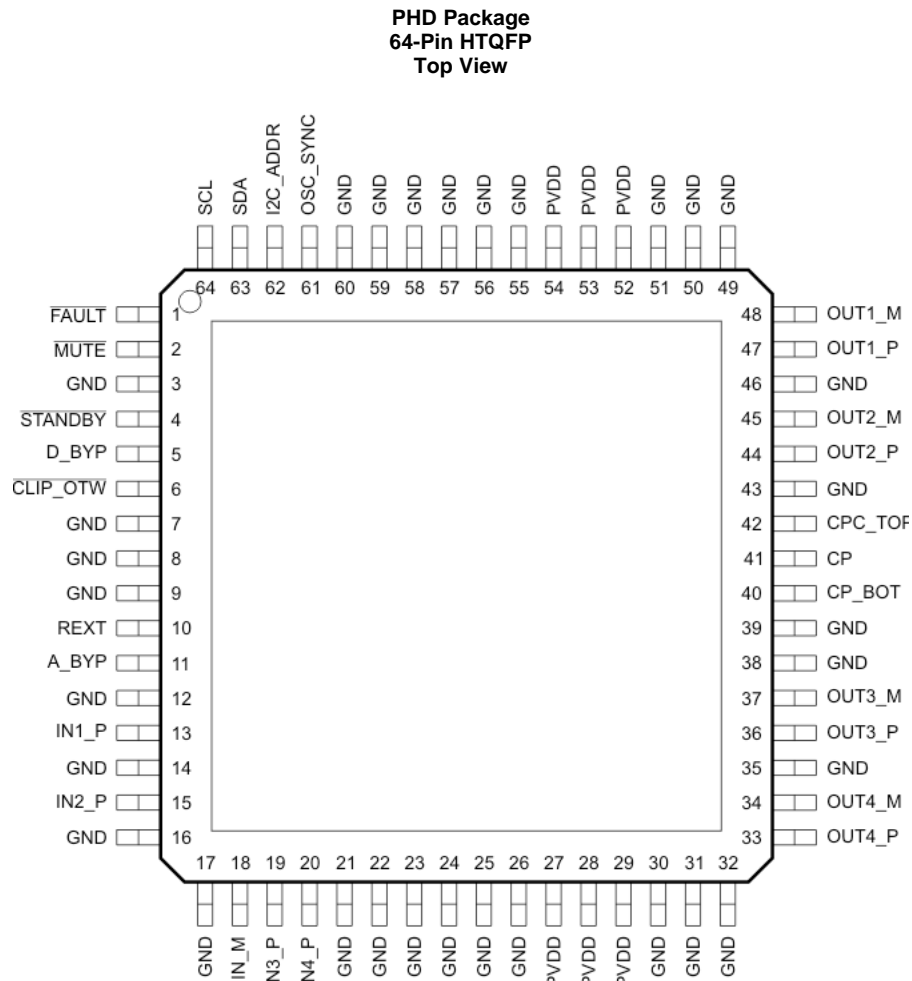
## 4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| 日付       | 改訂内容 | 注  |
|----------|------|----|
| 2016年12月 | *    | 初版 |

## 5 Pin Configuration and Functions

The pin assignments are shown as follows.



**Pin Functions**

| PIN                           |  | TYPE <sup>(1)</sup> | DESCRIPTION   |
|-------------------------------|--|---------------------|---|
| NAME                          | TAS5414C<br>PHD Package<br>NO.   |                     |   |
| A_BYP                         | 11   | PBY                 | Bypass pin for the AVDD analog regulator  |
| $\overline{\text{CLIP\_OTW}}$ | 6  | DO                  | Reports CLIP, OTW, or both. It also reports tweeter detection during tweeter mode. Open-drain |
| CP                            | 41   | CP                  | Top of main storage capacitor for charge pump (bottom goes to PVDD)                           |
| CPC_BOT                       | 40   | CP                  | Bottom of flying capacitor for charge pump  |
| CPC_TOP                       | 42   | CP                  | Top of flying capacitor for charge pump   |
| D_BYP                         | 5  | PBY                 | Bypass pin for DVDD regulator output  |
| FAULT                         | 1  | DO                  | Global fault output (open drain): UV, OV, OTSD, OCSD, DC                                      |
| GND                           | 3, 7, 8, 9, 12, 14, 16, 17,<br>21, 22, 23, 24, 25, 26, 30,<br>31, 32, 35, 38, 39, 43, 46,<br>49, 50, 51, 55, 56, 57, 58,<br>59, 60 | GND                 | Ground  |
| I2C_ADDR                      | 62   | AI                  | I <sup>2</sup> C address bit  |
| IN1_P                         | 13   | AI                  | Non-inverting analog input for channel 1  |
| IN2_P                         | 15   | AI                  | Non-inverting analog input for channel 2  |
| IN3_P                         | 19   | AI                  | Non-inverting analog input for channel 3  |
| IN4_P                         | 20   | AI                  | Non-inverting analog input for channel 4  |
| IN_M                          | 18   | ARTN                | Signal return for the four analog channel inputs (TAS5414C only)                              |
| $\overline{\text{MUTE}}$      | 2  | AI                  | Gain ramp control: mute (low), play (high)  |
| OSC_SYNC                      | 61   | DI/DO               | Oscillator input from master or output to slave amplifiers                                    |
| OUT1_M                        | 48   | PO                  | – polarity output for bridge 1  |
| OUT1_P                        | 47   | PO                  | + polarity output for bridge 1  |
| OUT2_M                        | 45   | PO                  | – polarity output for bridge 2  |
| OUT2_P                        | 44   | PO                  | + polarity output for bridge 2  |
| OUT3_M                        | 37   | PO                  | – polarity output for bridge 3  |
| OUT3_P                        | 36   | PO                  | + polarity output for bridge 3  |
| OUT4_M                        | 34   | PO                  | – polarity output for bridge 4  |
| OUT4_P                        | 33   | PO                  | + polarity output for bridge 4  |
| PVDD                          | 27, 28, 29, 52, 53, 54   | PWR                 | PVDD supply   |
| REXT                          | 10   | AI                  | Precision resistor pin to set analog reference  |
| SCL                           | 64   | DI                  | I <sup>2</sup> C clock input from system I <sup>2</sup> C master                              |
| SDA                           | 63   | DI/DO               | I <sup>2</sup> C data I/O for communication with system I <sup>2</sup> C master               |
| $\overline{\text{STANDBY}}$   | 4  | DI                  | Active-low STANDBY pin. Standby (low), power up (high)  |

(1) DI = digital input, DO = digital output, AI = analog input, ARTN = analog signal return, PWR = power supply, PBY = power bypass, PO = power output, GND = ground, CP = charge pump.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

|                                   |  |  | MIN  | MAX   | UNIT             |
|-----------------------------------|--|--|------|-------|------------------|
| PVDD                              | DC supply voltage range  | Relative to GND                            | −0.3 | 30    | V                |
| PVDD <sub>MAX</sub>               | Pulsed supply voltage range  | t ≤ 100 ms exposure                        | −1   | 50    | V                |
| PVDD <sub>RAMP</sub>              | Supply voltage ramp rate   |  |      | 15    | V/ms             |
| I <sub>PVDD</sub>                 | Externally imposed dc supply current per PVDD or GND pin                         |  |      | ±12   | A                |
| I <sub>PVDD_MAX</sub>             | Pulsed supply current per PVDD pin (one shot)                                    | t < 100 ms                                 |      | 17    | A                |
| I <sub>O</sub>                    | Maximum allowed dc current per output pin  |  |      | ±13.5 | A                |
| I <sub>O_MAX</sub> <sup>(1)</sup> | Pulsed output current per output pin (single pulse)                              | t < 100 ms                                 |      | ±17   | A                |
| I <sub>IN_MAX</sub>               | Maximum current, all digital and analog input pins <sup>(2)</sup>                | DC or pulsed                               |      | ±1    | mA               |
| I <sub>MUTE_MAX</sub>             | Maximum current on $\overline{\text{MUTE}}$ pin                                  | DC or pulsed                               |      | ±20   | mA               |
| I <sub>IN_ODMAX</sub>             | Maximum sink current for open-drain pins   |  |      | 7     | mA               |
| V <sub>LOGIC</sub>                | Input voltage range for pin relative to GND (SCL, SDA, I2C_ADDR pins)            | Supply voltage range:<br>6 V < PVDD < 24 V | −0.3 | 6     | V                |
| V <sub>MUTE</sub>                 | Voltage range for $\overline{\text{MUTE}}$ pin relative to GND                   | Supply voltage range:<br>6 V < PVDD < 24 V | −0.3 | 7.5   | V                |
| V <sub>STANDBY</sub>              | Input voltage range for $\overline{\text{STANDBY}}$ pin                          | Supply voltage range:<br>6 V < PVDD < 24 V | −0.3 | 5.5   | V                |
| V <sub>OSC_SYNC</sub>             | Input voltage range for OSC_SYNC pin relative to GND                             | Supply voltage range:<br>6 V < PVDD < 24 V | −0.3 | 3.6   | V                |
| V <sub>GND</sub>                  | Maximum voltage between GND pins   |  |      | ±0.3  | V                |
| V <sub>AIN_AC_MAX</sub>           | Maximum ac-coupled input voltage for TAS5414C <sup>(2)</sup> , analog input pins | Supply voltage range:<br>6 V < PVDD < 24 V |      | 1.9   | V <sub>rms</sub> |
| T <sub>J</sub>                    | Maximum operating junction temperature range                                     |  | −55  | 150   | °C               |
| T <sub>stg</sub>                  | Storage temperature  |  | −55  | 150   | °C               |

(1) Pulsed current ratings are maximum survivable currents externally applied to the device. The device may encounter high currents during reverse-battery, fortuitous open-ground, and fortuitous open-supply fault conditions.

(2) See the [Application Information](#) section for information on analog input voltage and ac coupling.

### 6.2 ESD Ratings

|                    |                         |  | VALUE   | UNIT |
|--------------------|-------------------------|--|---|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 <sup>(1)</sup>  | ±2500   | V    |
|                    |                         | Charged device model (CDM), per AEC Q100-011 PHD Package | Corner pins excluding SCL                     | ±750 |
|                    |                         |  | All pins (including SCL) except CP and CP_Top | ±600 |
|                    |                         |  | CP and CP_Top pins                            | ±400 |

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions <sup>(1)</sup>

|                                 |   |  | MIN | TYP  | MAX                   | UNIT             |
|---------------------------------|---|--|-----|------|-----------------------|------------------|
| PVDD <sub>OP</sub>              | DC supply voltage range relative to GND |  | 6   | 14.4 | 24                    | V                |
| V <sub>AIN</sub> <sup>(2)</sup> | Analog audio input signal level         | AC-coupled input voltage   | 0   |      | 0.25–1 <sup>(3)</sup> | V <sub>rms</sub> |
| T <sub>A</sub>                  | Ambient temperature                     |  | −20 |      | 105                   | °C               |
| T <sub>J</sub>                  | Junction temperature                    | An adequate heat sink is required to keep T <sub>J</sub> within specified range. | −40 |      | 115                   | °C               |
| R <sub>L</sub>                  | Nominal speaker load impedance          |  | 2   | 4    |                       | Ω                |

(1) The *Recommended Operating Conditions* table specifies only that the device is functional in the given range. See the *Electrical Characteristics* table for specified performance limits.

(2) Signal input for full unclipped output with gains of 32 dB, 26 dB, 20 dB, and 12 dB

(3) Maximum recommended input voltage is determined by the gain setting.

## Recommended Operating Conditions<sup>(1)</sup> (continued)

|  |   |   | MIN  | TYP      | MAX  | UNIT |
|--|---|---|------|----------|------|------|
| V <sub>PU</sub>                            | Pullup voltage supply (for open-drain logic outputs)  |   | 3    | 3.3 or 5 | 5.5  | V    |
| R <sub>PU_EXT</sub>                        | External pullup resistor on open-drain logic outputs  | Resistor connected between open-drain logic output and V <sub>PU</sub> supply | 10   |          | 50   | kΩ   |
| R <sub>PU_I2C</sub>                        | I <sup>2</sup> C pullup resistance on SDA and SCL pins  |   | 1    | 4.7      | 10   | kΩ   |
| R <sub>I2C_ADD</sub>                       | Total resistance of voltage divider for I <sup>2</sup> C address slave 1 or slave 2, connected between D_BYP and GND pins |   | 10   |          | 50   | kΩ   |
| R <sub>REXT</sub>                          | External resistance on REXT pin   | 1% tolerance required   | 19.8 | 20       | 20.2 | kΩ   |
| C <sub>D_BYP</sub> ,<br>C <sub>A_BYP</sub> | External capacitance on D_BYP and A_BYP pins  |   | 10   |          | 120  | nF   |
| C <sub>OUT</sub>                           | External capacitance to GND on OUT_X pins   |   |      | 150      | 680  | nF   |
| C <sub>IN</sub>                            | External capacitance to analog input pin in series with input signal  |   |      | 0.47     |      | μF   |
| C <sub>FLY</sub>                           | Flying capacitor on charge pump   |   | 0.47 | 1        | 1.5  | μF   |
| C <sub>P</sub>                             | Charge pump capacitor   | 50V needed for Load Dump  | 0.47 | 1        | 1.5  | μF   |
| C <sub>MUTE</sub>                          | MUTE pin capacitor  |   | 100  | 220      | 1000 | nF   |
| C <sub>OSCSYNC_MAX</sub>                   | Allowed loading capacitance on OSC_SYNC pin   |   |      | 75       |      | pF   |

## 6.4 Thermal Information

| PARAMETER   | VALUE (Typical)  | UNIT |
|---|--|------|
| R <sub>θJC</sub> Junction-to-case (heat slug) thermal resistance, PHD package | 1.2  | °C/W |
| R <sub>θJA</sub> Junction-to-ambient thermal resistance                       | This device is not intended to be used without a heatsink. Therefore, R <sub>θJA</sub> is not specified. Refer to the <a href="#">Thermal Information</a> section. | °C/W |

## 6.5 Electrical Characteristics

Test conditions (unless otherwise noted): T<sub>Case</sub> = 25°C, PVDD = 14.4 V, R<sub>L</sub> = 4 Ω, f<sub>S</sub> = 417 kHz, P<sub>out</sub> = 1 W/ch, R<sub>ext</sub> = 20 kΩ, AES17 filter, default I<sup>2</sup>C settings, master-mode operation (see [Figure 36](#))

| PARAMETER              |                                   | TEST CONDITIONS   | MIN   | TYP  | MAX | UNIT |
|------------------------|-----------------------------------|---|-------|------|-----|------|
| OPERATING CURRENT      |                                   |   |       |      |     |      |
| I <sub>PVDD_IDLE</sub> | PVDD idle current                 | All four channels in MUTE mode  | 170   | 220  |     | mA   |
| I <sub>PVDD_HI-Z</sub> |                                   | All four channels in Hi-Z mode  | 93    |      |     | mA   |
| I <sub>PVDD_STBY</sub> | PVDD standby current              | STANDBY mode, T <sub>J</sub> ≤ 85°C   | 2     | 10   |     | μA   |
| OUTPUT POWER           |                                   |   |       |      |     |      |
| P <sub>OUT</sub>       | Output power per channel          | 4 Ω, PVDD = 14.4 V, THD+N ≤ 1%, 1 kHz, T <sub>c</sub> = 75°C                    | 23    |      |     | W    |
|                        |                                   | 4 Ω, PVDD = 14.4 V, THD+N = 10%, 1 kHz, T <sub>c</sub> = 75°C                   | 25    | 28   |     |      |
|                        |                                   | 4 Ω, PVDD = 24 V, THD+N = 10%, 1 kHz, T <sub>c</sub> = 75°C                     | 63    | 79   |     |      |
|                        |                                   | 2 Ω, PVDD = 14.4 V, THD+N = 1%, 1 kHz, T <sub>c</sub> = 75°C                    | 38    |      |     |      |
|                        |                                   | 2 Ω, PVDD = 14.4 V, THD+N = 10%, 1 kHz, T <sub>c</sub> = 75°C                   | 40    | 50   |     |      |
|                        |                                   | PBTL 2-Ω operation, PVDD = 24 V, THD+N = 10%, 1 kHz, T <sub>c</sub> = 75°C      | 150   |      |     |      |
|                        |                                   | PBTL 1-Ω operation, PVDD = 14.4 V, THD+N = 10%, 1 kHz, T <sub>c</sub> = 75°C    | 90    |      |     |      |
| EFF <sub>P</sub>       | Power efficiency                  | 4 channels operating, 23-W output power/ch, L = 10 μH, T <sub>J</sub> ≤ 85°C    | 90%   |      |     |      |
| AUDIO PERFORMANCE      |                                   |   |       |      |     |      |
| V <sub>NOISE</sub>     | Noise voltage at output           | Zero input, and A-weighting   | 60    | 100  |     | μV   |
|                        | Channel crosstalk                 | P = 1 W, f = 1 kHz, enhanced crosstalk enabled via I <sup>2</sup> C (reg. 0x10) | 70    | 85   |     | dB   |
| PSRR                   | Power-supply rejection ratio      | PVDD = 14.4 Vdc + 1 Vrms, f = 1 kHz   | 60    | 75   |     | dB   |
| THD+N                  | Total harmonic distortion + noise | P = 1 W, f = 1 kHz  | 0.02% | 0.1% |     |      |
| f <sub>S</sub>         | Switching frequency               | Switching frequency selectable for AM interference avoidance                    | 336   | 357  | 378 | kHz  |
|                        |                                   |   | 392   | 417  | 442 |      |
|                        |                                   |   | 470   | 500  | 530 |      |

## Electrical Characteristics (continued)

Test conditions (unless otherwise noted):  $T_{Case} = 25^{\circ}C$ ,  $PVDD = 14.4\text{ V}$ ,  $R_L = 4\ \Omega$ ,  $f_S = 417\text{ kHz}$ ,  $P_{out} = 1\text{ W/ch}$ ,  $R_{ext} = 20\text{ k}\Omega$ , AES17 filter, default I<sup>2</sup>C settings, master-mode operation (see [Figure 36](#))

| PARAMETER                                       |   | TEST CONDITIONS  | MIN  | TYP  | MAX  | UNIT             |    |
|---|---|--|------|------|------|------------------|----|
| R <sub>AIN</sub>                                | Analog input resistance                           | Internal shunt resistance on each input pin                                | 63   | 85   | 106  | kΩ               |    |
| V <sub>IN_CM</sub>                              | Common-mode input voltage                         | AC-coupled common-mode input voltage (zero differential input)             | 1.3  |      |      | V <sub>rms</sub> |    |
| V <sub>CM_INT</sub>                             | Internal common-mode input bias voltage           | Internal bias applied to IN_M pin  | 3.3  |      |      | V                |    |
| G   | Voltage gain (V <sub>O</sub> /V <sub>IN</sub> )   | Source impedance = 0 Ω, gain measurement taken at 1 W of power per channel | 11   | 12   | 13   | dB               |    |
|   |   |  | 19   | 20   | 21   |                  |    |
|   |   |  | 25   | 26   | 27   |                  |    |
|   |   |  | 31   | 32   | 33   |                  |    |
| G <sub>CH</sub>                                 | Channel-to-channel variation                      | Any gain commanded   | −1   | 0    | 1    | dB               |    |
| PWM OUTPUT STAGE                                |   |  |      |      |      |                  |    |
| R <sub>DS(on)</sub>                             | FET drain-to-source resistance                    | Not including bond wire resistance, T <sub>J</sub> = 25°C                  | 65   |      |      | mΩ               |    |
| V <sub>O_OFFSET</sub>                           | Output offset voltage                             | Zero input signal, G = 26 dB   | ±10  |      |      | ±50              | mV |
| PVDD OVERVOLTAGE (OV) PROTECTION                |   |  |      |      |      |                  |    |
| V <sub>OV_SET</sub>                             | PVDD overvoltage shutdown set                     |  | 24.6 | 26.4 | 28.2 | V                |    |
| V <sub>OV_CLEAR</sub>                           | PVDD overvoltage shutdown clear                   |  | 24.4 | 25.9 | 27.4 | V                |    |
| PVDD UNDERVOLTAGE (UV) PROTECTION               |   |  |      |      |      |                  |    |
| V <sub>UV_SET</sub>                             | PVDD undervoltage shutdown set                    |  | 4.9  | 5.3  | 5.6  | V                |    |
| V <sub>UV_CLEAR</sub>                           | PVDD undervoltage shutdown clear                  |  | 6.2  | 6.6  | 7    | V                |    |
| AVDD  |   |  |      |      |      |                  |    |
| V <sub>A_BYP</sub>                              | A_BYP pin voltage                                 |  | 6.5  |      |      | V                |    |
| V <sub>A_BYP_UV_SET</sub>                       | A_BYP UV voltage                                  |  | 4.8  |      |      | V                |    |
| V <sub>A_BYP_UV_CLEAR</sub>                     | Recovery voltage A_BYP UV                         |  | 5.3  |      |      | V                |    |
| DVDD  |   |  |      |      |      |                  |    |
| V <sub>D_BYP</sub>                              | D_BYP pin voltage                                 |  | 3.3  |      |      | V                |    |
| POWER-ON RESET (POR)                            |   |  |      |      |      |                  |    |
| V <sub>POR</sub>                                | PVDD voltage for POR                              | I <sup>2</sup> C active above this voltage                                 | 4    |      |      | V                |    |
| V <sub>POR_HY</sub>                             | PVDD recovery hysteresis voltage for POR          |  | 0.1  |      |      | V                |    |
| REXT  |   |  |      |      |      |                  |    |
| V <sub>REXT</sub>                               | Rext pin voltage                                  |  | 1.27 |      |      | V                |    |
| CHARGE PUMP (CP)                                |   |  |      |      |      |                  |    |
| V <sub>CPUV_SET</sub>                           | CP undervoltage                                   |  | 4.8  |      |      | V                |    |
| V <sub>CPUV_CLEAR</sub>                         | Recovery voltage for CP UV                        |  | 4.9  |      |      | V                |    |
| OVERTEMPERATURE (OT) PROTECTION                 |   |  |      |      |      |                  |    |
| T <sub>OTW1_CLEAR</sub>                         | Junction temperature for overtemperature warning  |  | 96   | 112  | 128  | °C               |    |
| T <sub>OTW1_SET</sub> / T <sub>OTW2_CLEAR</sub> |   |  | 106  | 122  | 138  | °C               |    |
| T <sub>OTW2_SET</sub> / T <sub>OTW3_CLEAR</sub> |   |  | 116  | 132  | 148  | °C               |    |
| T <sub>OTW3_SET</sub> / T <sub>OTSD_CLEAR</sub> |   |  | 126  | 142  | 158  | °C               |    |
| T <sub>OTSD</sub>                               | Junction temperature for overtemperature shutdown |  | 136  | 152  | 168  | °C               |    |
| T <sub>FB</sub>                                 | Junction temperature for overtemperature foldback | Per channel  | 130  | 150  | 170  | °C               |    |
| CURRENT LIMITING PROTECTION                     |   |  |      |      |      |                  |    |
| I <sub>LIM</sub>                                | Current limit (load current)                      | Level 1  | 5.5  | 7.3  | 9    | A                |    |
|   |   | Level 2 (default)  | 10.6 | 12.7 | 15   |                  |    |
| OVERCURRENT (OC) SHUTDOWN PROTECTION            |   |  |      |      |      |                  |    |
| I <sub>MAX</sub>                                | Maximum current (peak output current)             | Level 1  | 7.8  | 9.8  | 12.2 | A                |    |
|   |   | Level 2 (default), Any short to supply, ground, or other channels          | 11.9 | 14.8 | 17.7 |                  |    |

## Electrical Characteristics (continued)

Test conditions (unless otherwise noted):  $T_{Case} = 25^{\circ}C$ ,  $PVDD = 14.4\text{ V}$ ,  $R_L = 4\ \Omega$ ,  $f_S = 417\text{ kHz}$ ,  $P_{out} = 1\text{ W/ch}$ ,  $R_{ext} = 20\text{ k}\Omega$ , AES17 filter, default I<sup>2</sup>C settings, master-mode operation (see [Figure 36](#))

| PARAMETER                  |  | TEST CONDITIONS   | MIN | TYP | MAX | UNIT |
|----------------------------|--|---|-----|-----|-----|------|
| TWEETER DETECT             |  |   |     |     |     |      |
| I <sub>TH_TW</sub>         | Load-current threshold for tweeter detect                                  |   | 330 | 445 | 560 | mA   |
| I <sub>LIM_TW</sub>        | Load-current limit for tweeter detect                                      |   |     | 2.1 |     | A    |
| STANDBY MODE               |  |   |     |     |     |      |
| V <sub>IH</sub>            | STANDBY input voltage for logic-level high                                 |   | 2   |     |     | V    |
| V <sub>IL</sub>            | STANDBY input voltage for logic-level low                                  |   |     |     | 0.7 | V    |
| I <sub>STBY</sub>          | STANDBY pin current  |   |     | 0.1 | 0.2 | μA   |
| MUTE MODE                  |  |   |     |     |     |      |
| G <sub>MUTE</sub>          | Output attenuation   | MUTE pin ≤ 0.5 V for 200ms or I <sup>2</sup> C Mute Enabled |     | 100 |     | dB   |
| DC DETECT                  |  |   |     |     |     |      |
| V <sub>TH_DC_TOL</sub>     | DC detect threshold tolerance  |   |     | 25% |     |      |
| t <sub>DCD</sub>           | DC detect step-response time for four channels                             |   |     |     | 5.3 | s    |
| CLIP_OTW REPORT            |  |   |     |     |     |      |
| V <sub>OH_CLIPOTW</sub>    | CLIP_OTW pin output voltage for logic level high (open-drain logic output) | External 47-kΩ pullup resistor to 3 V–5.5 V                 | 2.4 |     |     | V    |
| V <sub>OL_CLIPOTW</sub>    | CLIP_OTW pin output voltage for logic level low (open-drain logic output)  |   |     |     | 0.5 | V    |
| t <sub>DELAY_CLIPDET</sub> | CLIP_OTW signal delay when output clipping detected                        |   |     |     | 20  | μs   |
| FAULT REPORT               |  |   |     |     |     |      |
| V <sub>OH_FAULT</sub>      | FAULT pin output voltage for logic-level high (open-drain logic output)    | External 47-kΩ pullup resistor to 3 V–5.5 V                 | 2.4 |     |     | V    |
| V <sub>OL_FAULT</sub>      | FAULT pin output voltage for logic-level low (open-drain logic output)     |   |     |     | 0.5 |      |



## Electrical Characteristics (continued)

Test conditions (unless otherwise noted):  $T_{Case} = 25^{\circ}C$ ,  $PVDD = 14.4\text{ V}$ ,  $R_L = 4\ \Omega$ ,  $f_S = 417\text{ kHz}$ ,  $P_{out} = 1\text{ W/ch}$ ,  $R_{ext} = 20\text{ k}\Omega$ , AES17 filter, default I<sup>2</sup>C settings, master-mode operation (see [Figure 36](#))

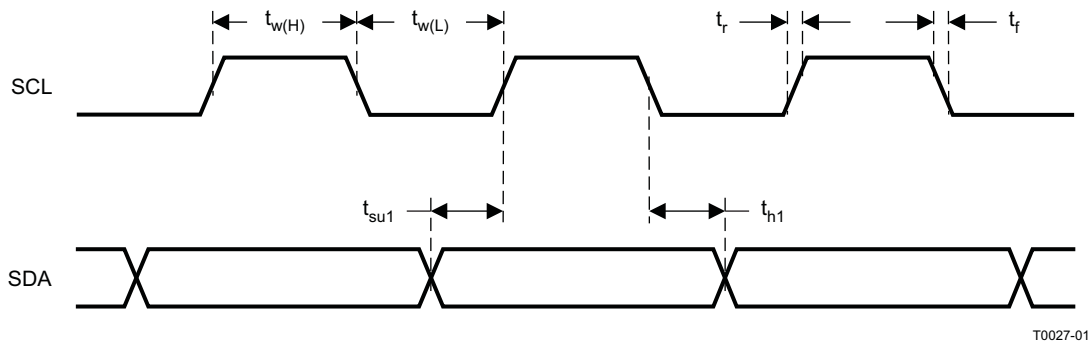
| PARAMETER                           |  | TEST CONDITIONS   | MIN  | TYP  | MAX  | UNIT               |
|-------------------------------------|--|---|------|------|------|--------------------|
| OPEN, SHORT DIAGNOSTICS             |  |   |      |      |      |                    |
| R <sub>S2P</sub> , R <sub>S2G</sub> | Maximum resistance to detect a short from OUT pin(s) to PVDD or ground |   |      |      | 200  | Ω                  |
| R <sub>OPEN_LOAD</sub>              | Minimum load resistance to detect open circuit                         | Including speaker wires   | 300  | 740  | 1300 | Ω                  |
| R <sub>SHORTED_LOAD</sub>           | Maximum load resistance to detect short circuit                        | Including speaker wires   | 0.5  | 1    | 1.5  | Ω                  |
| I <sup>2</sup> C ADDRESS DECODER    |  |   |      |      |      |                    |
| t <sub>LATCH_I2CADDR</sub>          | Time delay to latch I <sup>2</sup> C address after POR                 |   |      | 300  |      | μs                 |
| V <sub>I2C_ADDR</sub>               | Voltage on I2C_ADDR pin for address 0                                  | Connect to GND  | 0%   | 0%   | 15%  | V <sub>D_BYP</sub> |
|                                     | Voltage on I2C_ADDR pin for address 1                                  | External resistors in series between D_BYP and GND as a voltage divider               | 25%  | 35%  | 45%  |                    |
|                                     | Voltage on I2C_ADDR pin for address 2                                  |   | 55%  | 65%  | 75%  |                    |
|                                     | Voltage on I2C_ADDR pin for address 3                                  | Connect to D_BYP  | 85%  | 100% | 100% |                    |
| I <sup>2</sup> C                    |  |   |      |      |      |                    |
| t <sub>HOLD_I2C</sub>               | Power-on hold time before I <sup>2</sup> C communication               | <u>STANDBY</u> high   |      | 1    |      | ms                 |
| f <sub>SCL</sub>                    | SCL clock frequency  |   |      | 400  |      | kHz                |
| V <sub>IH</sub>                     | SCL pin input voltage for logic-level high                             | R <sub>PU_I2C</sub> = 5-kΩ pullup, supply voltage = 3.3 V or 5 V                      | 2.1  |      | 5.5  | V                  |
| V <sub>IL</sub>                     | SCL pin input voltage for logic-level low                              |   | –0.5 |      | 1.1  | V                  |
| V <sub>OH</sub>                     | SDA pin output voltage for logic-level high                            | I <sup>2</sup> C read, R <sub>I2C</sub> = 5-kΩ pullup, supply voltage = 3.3 V or 5 V  | 2.4  |      |      | V                  |
| V <sub>O</sub>                      | SDA pin output voltage for logic-level low                             | I <sup>2</sup> C read, 3-mA sink current  |      |      | 0.4  | V                  |
| V <sub>IH</sub>                     | SDA pin input voltage for logic-level high                             | I <sup>2</sup> C write, R <sub>I2C</sub> = 5-kΩ pullup, supply voltage = 3.3 V or 5 V | 2.1  |      | 5.5  | V                  |
| V <sub>IL</sub>                     | SDA pin input voltage for logic-level low                              | I <sup>2</sup> C write, R <sub>I2C</sub> = 5-kΩ pullup, supply voltage = 3.3 V or 5 V | –0.5 |      | 1.1  | V                  |
| C <sub>I</sub>                      | Capacitance for SCL and SDA pins                                       |   |      |      | 10   | pF                 |
| OSCILLATOR                          |  |   |      |      |      |                    |
| V <sub>OH</sub>                     | OSC_SYNC pin output voltage for logic-level high                       | I2C_ADDR pin set to MASTER mode   | 2.4  |      |      | V                  |
| V <sub>OL</sub>                     | OSC_SYNC pin output voltage for logic-level low                        |   |      |      | 0.5  | V                  |
| V <sub>IH</sub>                     | OSC_SYNC pin input voltage for logic-level high                        | I2C_ADDR pin set to SLAVE mode  | 2    |      |      | V                  |
| V <sub>IL</sub>                     | OSC_SYNC pin input voltage for logic-level low                         |   |      |      | 0.8  | V                  |
| f <sub>OSC_SYNC</sub>               | OSC_SYNC pin clock frequency   | I2C_ADDR pin set to MASTER mode, f <sub>S</sub> = 500 kHz                             | 3.76 | 4    | 4.24 | MHz                |
|                                     |  | I2C_ADDR pin set to MASTER mode, f <sub>S</sub> = 417 kHz                             | 3.13 | 3.33 | 3.63 |                    |
|                                     |  | I2C_ADDR pin set to MASTER mode, f <sub>S</sub> = 357 kHz                             | 2.68 | 2.85 | 3.0  |                    |

## 6.6 Timing Requirements for I<sup>2</sup>C Interface Signals

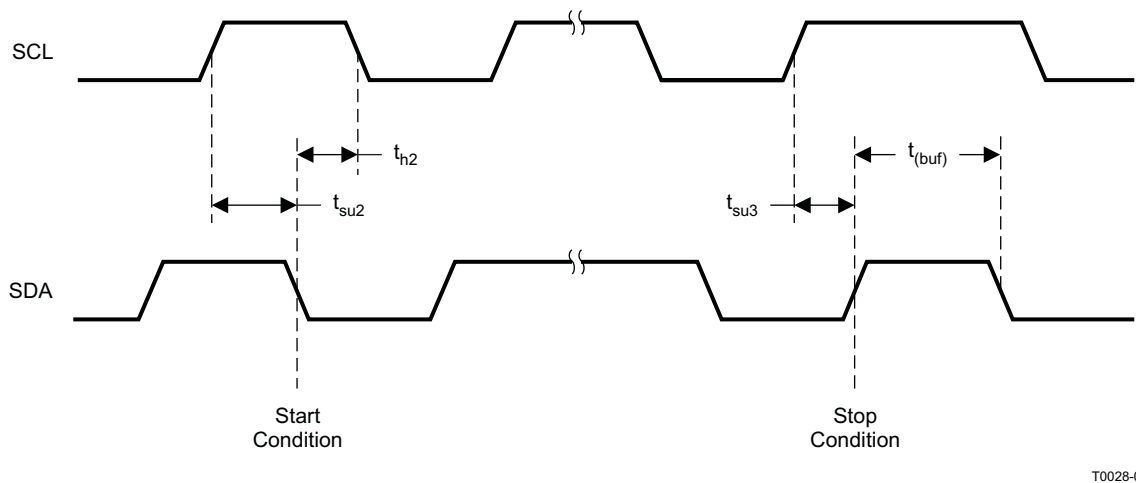
over recommended operating conditions (unless otherwise noted)

|            |   | MIN              | TYP | MAX | UNIT    |
|------------|---|------------------|-----|-----|---------|
| $t_r$      | Rise time for both SDA and SCL signals                          |                  |     | 300 | ns      |
| $t_f$      | Fall time for both SDA and SCL signals                          |                  |     | 300 | ns      |
| $t_{w(H)}$ | SCL pulse duration, high  | 0.6              |     |     | $\mu$ s |
| $t_{w(L)}$ | SCL pulse duration, low   | 1.3              |     |     | $\mu$ s |
| $t_{su2}$  | Setup time for START condition                                  | 0.6              |     |     | $\mu$ s |
| $t_{h2}$   | START condition hold time until generation of first clock pulse | 0.6              |     |     | $\mu$ s |
| $t_{su1}$  | Data setup time   | 100              |     |     | ns      |
| $t_{h1}$   | Data hold time  | 0 <sup>(1)</sup> |     |     | ns      |
| $t_{su3}$  | Setup time for STOP condition                                   | 0.6              |     |     | $\mu$ s |
| $C_B$      | Load capacitance for each bus line                              |                  |     | 400 | pF      |

- (1) A device must internally provide a hold time of at least 300 ns for the SDA signal to bridge the undefined region of the falling edge of SCL.

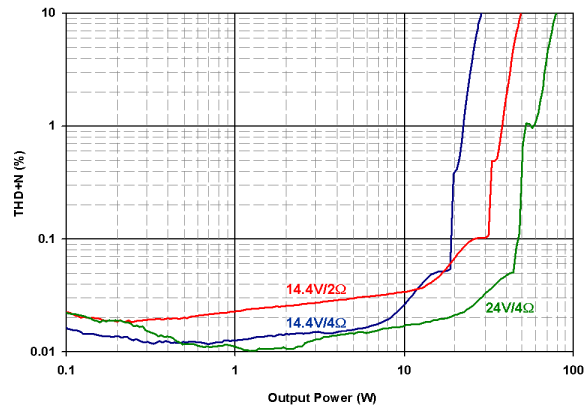


**Figure 1. SCL and SDA Timing**

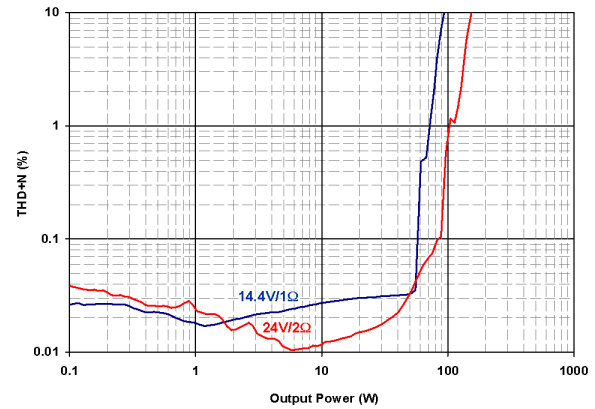


**Figure 2. Timing for Start and Stop Conditions**

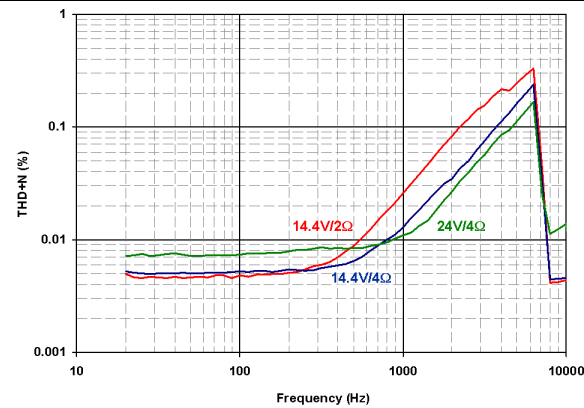
## 6.7 Typical Characteristics



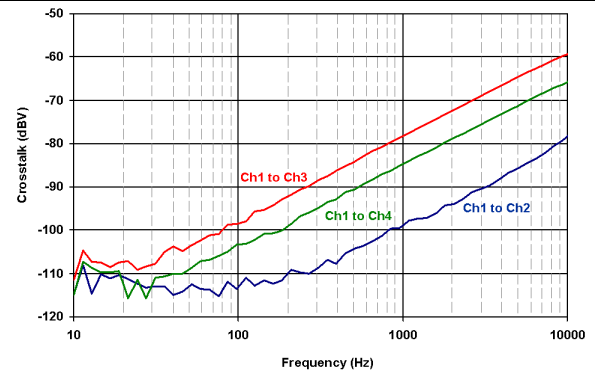
**Figure 3. THD+N vs BTL Output Power at 1kHz**



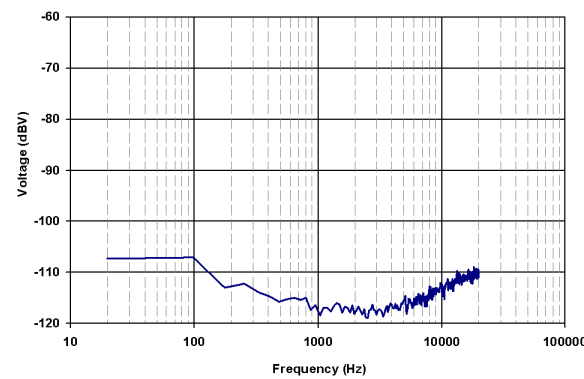
**Figure 4. THD+N vs PBTB Output Power at 1kHz**



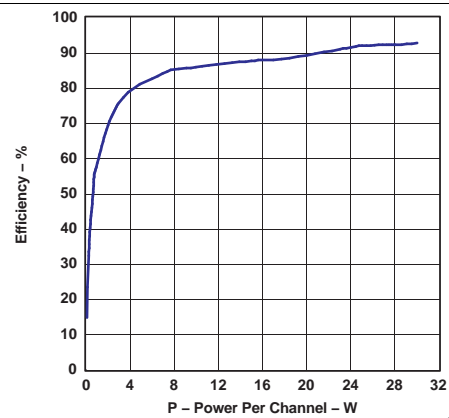
**Figure 5. THD+N vs Frequency at 1 Watt**



**Figure 6. Crosstalk vs Frequency**



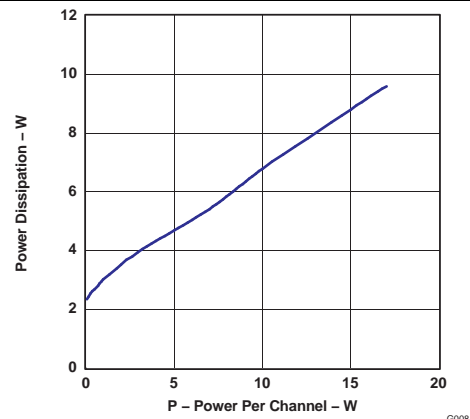
**Figure 7. Noise FFT**



**Figure 8. Efficiency  
Four Channels AT 4 Ω Each**

G007

## Typical Characteristics (continued)



**Figure 9. Device Power Dissipation  
Four Channels at 4  $\Omega$  Each**

## 7 Detailed Description

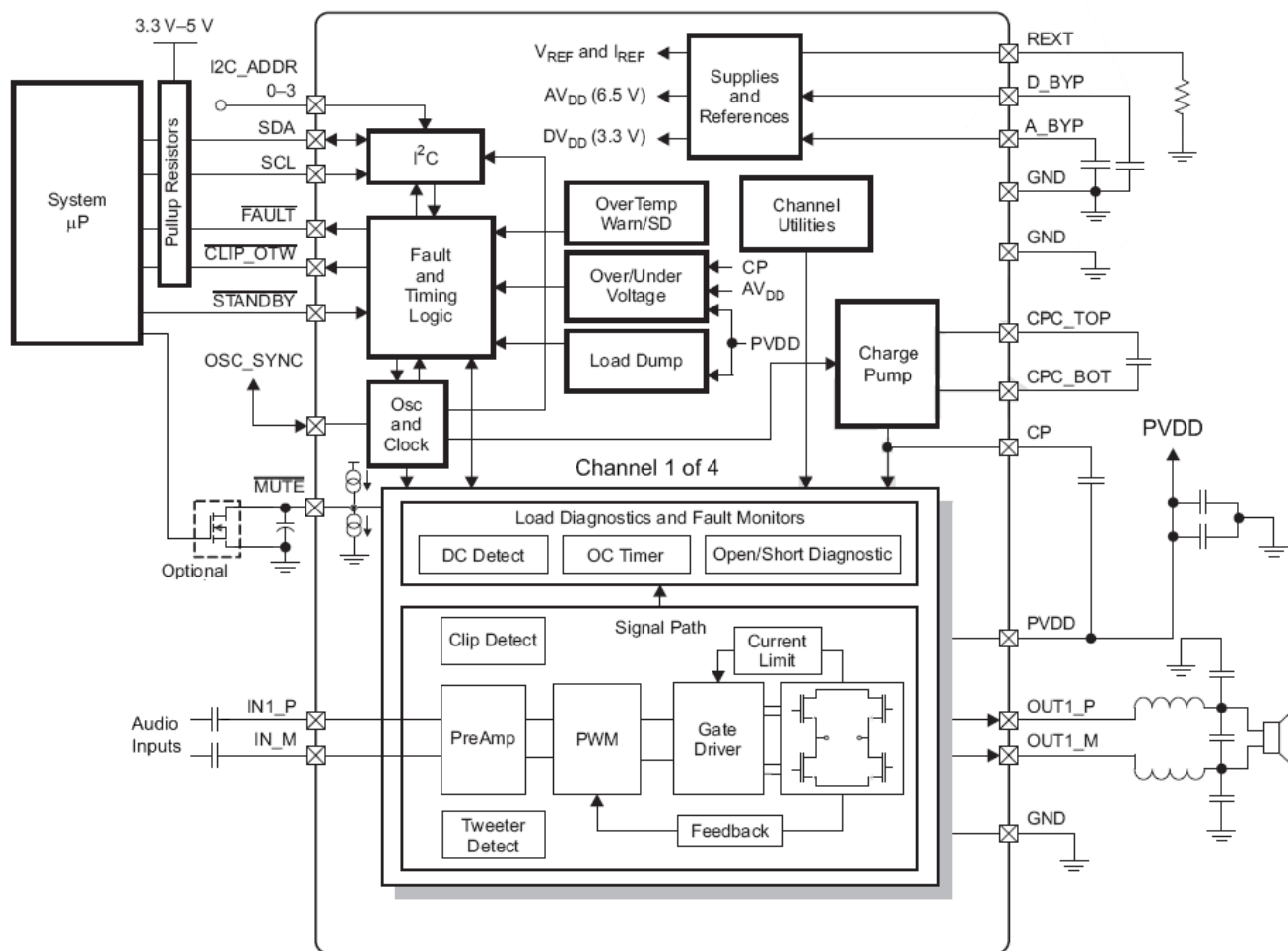
### 7.1 Overview

The TAS5414C is a single-chip, four-channel, analog-input audio amplifier. The design uses an ultra-efficient class-D technology developed by Texas Instruments. This technology allows for reduced power consumption, reduced heat, and reduced peak currents in the electrical system. The device realizes an audio sound system design with smaller size and lower weight than traditional class-AB solutions.

There are eight core design blocks:

- Preamplifier
- PWM
- Gate drive
- Power FETs
- Diagnostics
- Protection
- Power supply
- I<sup>2</sup>C serial communication bus

### 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Preamplifier

The preamplifier is a high-input-impedance, low-noise, low-offset-voltage input stage with adjustable gain. The high input impedance allows the use of low-cost input capacitors while still achieving extended low-frequency response. A dedicated, internally regulated supply powers the preamplifier, giving it excellent noise immunity and channel separation. The preamplifier also includes:

1. **Mute Pop-and-Click Control** — The device ramps the gain gradually when receiving a mute or play command. The start or stopping of switching in a class-D amplifier can cause another form of click and pop. The TAS5414C incorporates a patented method to reduce the pop energy during the switching startup and shutdown sequence. Fault conditions require rapid protection response by the TAS5414C, which does not have time to ramp the gain down in a pop-free manner. The device transitions into Hi-Z mode when encountering an OV, UV, OC, OT, or dc fault. Also, activation of the **STANDBY** pin may not be pop-free.
2. **Gain Control** — Setting of gains for the four channels occurs in the preamplifier via I<sup>2</sup>C control registers, outside of the global feedback resistors of the device, thus allowing for stability of the system at all gain settings with properly loaded conditions.

### 7.3.2 Pulse-Width Modulator (PWM)

The PWM converts the analog signal from the preamplifier into a switched signal of varying duty cycle. This is the critical stage that defines the class-D architecture. In the TAS5414C, the modulator is an advanced design with high bandwidth, low noise, low distortion, excellent stability, and full 0–100% modulation capability. The patented PWM uses clipping recovery circuitry to eliminate the deep saturation characteristic of PWMs when the input signal exceeds the modulator waveform.

### 7.3.3 Gate Drive

The gate driver accepts the low-voltage PWM signal and level-shifts it to drive a high-current, full-bridge, power FET stage. The device uses proprietary techniques to optimize EMI and audio performance.

### 7.3.4 Power FETs

The BTL output for each channel comprises four rugged N-channel 30-V 65-mΩ FETs for high efficiency and maximum power transfer to the load. These FETs can handle large voltage transients during load dump.

### 7.3.5 Load Diagnostics

The device incorporates load diagnostic circuitry designed to help pinpoint the nature of output misconnections during installation. The TAS5414C includes functions for detecting and determining the status of output connections. The device supports the following diagnostics:

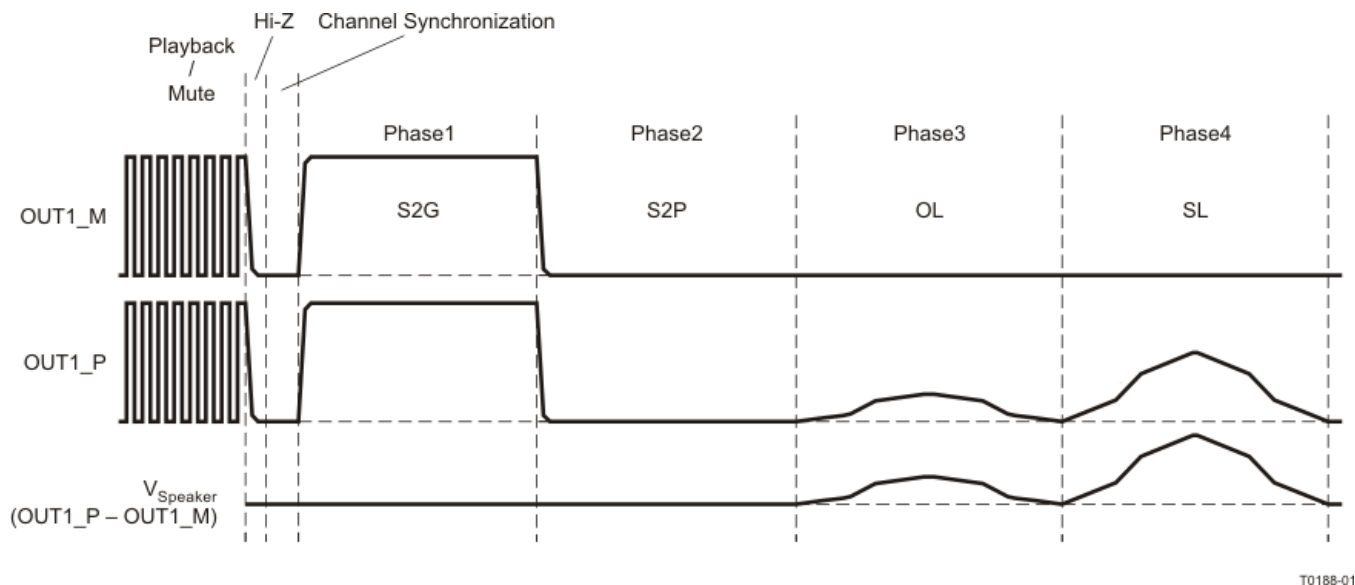
- Short to GND
- Short to PVDD
- Short across load
- Open load
- Tweeter detection

Reporting to the system of the presence of any of the short or open conditions occurs via I<sup>2</sup>C register read. One can read the tweeter-detect status from the **CLIP\_OTW** pin when properly configured.

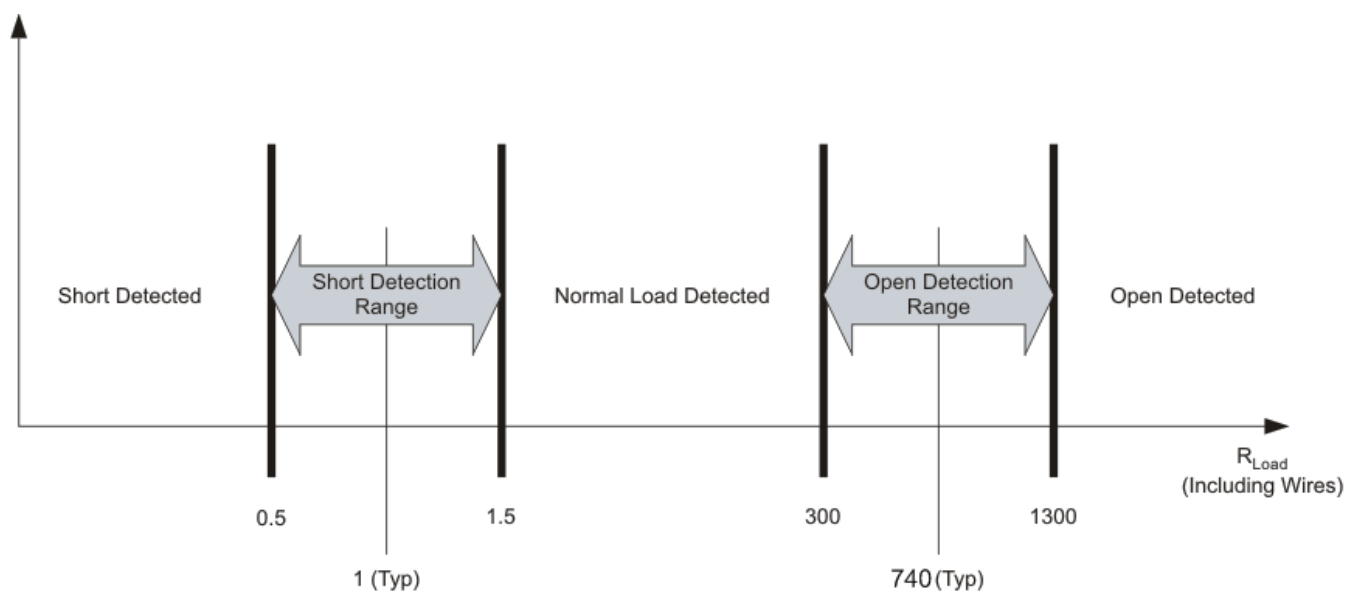
1. **Output Short and Open Diagnostics** — The device contains circuitry designed to detect shorts and open conditions on the outputs. Invocation of the load diagnostic function can only occur when the output is in the Hi-Z mode. There are four phases of test during load diagnostics and two levels of test. In the full level, all channels must be in the Hi-Z state. Testing covers all four phases on each channel, all four channels at the same time. When fewer than four channels are in Hi-Z, the reduced level of test is the only available option. In the reduced level, the only tests available are short to PVDD and short to GND. Load diagnostics can occur at power up before moving the amplifier out of Hi-Z mode. If the amplifier is already in play mode, it must *Mute* and then *Hi-Z* before performing the load diagnostic. By performing the mute function, the normal pop- and click-free transitions occur before the diagnostics begin. Performance of the diagnostics is as shown in [Figure 10](#). [Figure 11](#) shows the impedance ranges for the open-load and shorted-load diagnostics. Reading the results of the diagnostics is from the diagnostic register via I<sup>2</sup>C for each channel. With the default settings and **MUTE** capacitor, the S2G and S2P phase take approximately 20 ms each, the OL phase

## Feature Description (continued)

takes approximately 100 ms, and the SL takes approximately 230 ms. In I<sup>2</sup>C register 0x10, bit D4 can extend the test time for S2P and S2G to 80 ms each. To prevent false S2G and S2P faults, this time extension is necessary if the output pins have a capacitance higher than 680 nF to ground.



**Figure 10. Load Diagnostics Sequence of Events**



**Figure 11. Open- and Shorted-Load Detection**

- Tweeter Detection** — Tweeter detection is an alternate operating mode used to determine the proper connection of a frequency-dependent load (such as a speaker with a crossover). Invoking of tweeter detection is via I<sup>2</sup>C, with individual testing of all four channels recommended. Tweeter detection uses the average cycle-by-cycle current limit circuit (see [CBC](#) section) to measure the current delivered to the load. The proper implementation of this diagnostic function depends on the amplitude of a user-supplied test signal and on the impedance-versus-frequency curve of the acoustic load. The system (external to the TAS5414C) must generate a signal to which the load responds. The frequency and amplitude of this signal must be calibrated by the user to result in a current draw that is greater than the tweeter detection threshold when the load

## Feature Description (continued)

under test is present, and less than the detection threshold if the load is unconnected. The current level for the tweeter detection threshold, as well as the maximum current that can safely be delivered to a load when in tweeter-detection mode, is in the [Electrical Characteristics](#) section of the data sheet. Reporting of the tweeter-detection results is on the CLIP\_OTW pin during the application of the test signal. With tweeter detection activated (indicating that the tested load is present), pulses on the CLIP\_OTW pin begin to toggle. The pulses on the CLIP\_OTW pins report low whenever the current exceeds the detection threshold, and the pin remains low until the current no longer exceeds the threshold. The minimum low-pulse period that one can expect is equal to one period of the switching frequency. Having an input signal that increases the duration of detector activation (for example, increasing the amplitude of the input signal) increases the amount of time for which the pin reports low.

**NOTE:** Because tweeter detection is an alternate *operating mode*, place the channels to be tested in Play mode (via register 0x0C) after tweeter detection has been activated in order to commence the detection process. Additionally, set up the CLIP\_OTW pin via register 0x0A to report the results of tweeter detection.

### 7.3.6 Protection and Monitoring

1. **Cycle-By-Cycle Current Limit (CBC)** — The CBC current-limiting circuit terminates each PWM pulse to limit the output current flow to the average current limit ( $I_{LIM}$ ) threshold. The overall effect on the audio in the case of a current overload is quite similar to a voltage-clipping event, temporarily limiting power at the peaks of the musical signal and normal operation continues without disruption on removal of the overload. The TAS5414C does not prematurely shut down in this condition. All four channels continue in play mode and pass signal.
2. **Overcurrent Shutdown (OCS)** — Under severe short-circuit events, such as a short to PVDD or ground, the device uses a peak-current detector, and the affected channel shuts down in 200  $\mu$ s to 390  $\mu$ s if the conditions are severe enough. The shutdown speed depends on a number of factors, such as the impedance of the short circuit, supply voltage, and switching frequency. Only the shorted channels shut down in such a scenario. The user may restart the affected channel via I<sup>2</sup>C. An OCS event activates the fault pin, and the I<sup>2</sup>C fault register saves a record of the affected channels. If the supply or ground short is strong enough to exceed the peak current threshold but not severe enough to trigger the OCS, the peak current limiter prevents excess current from damaging the output FETs, and operation returns to normal after the short is removed.
3. **DC Detect**—This circuit detects a dc offset at the output of the amplifier continuously during normal operation. If the dc offset reaches the level defined in the I<sup>2</sup>C registers for the specified time period, the circuit triggers. By default, a dc detection event does not shut the output down. Disabling and enabling the shutdown function is via I<sup>2</sup>C. If enabled, the triggered channel shuts down, but the others remain playing, but with the FAULT pin asserted. The I<sup>2</sup>C registers define the dc level.
4. **Clip Detect**—The clip detect circuit alerts the user to the presence of a 100% duty-cycle PWM due to a clipped waveform. When this occurs, a signal passed to the CLIP\_OTW pin asserts it until the 100% duty-cycle PWM signal is no longer present. All four channels connect to the same CLIP\_OTW pin. Through I<sup>2</sup>C, one can change the CLIP\_OTW signal clip-only, OTW-only, or both. A fourth mode, used only during diagnostics, is the option to report tweeter detection events on this pin (see the [Tweeter Detection](#) section). The microcontroller in the system can monitor the signal at the CLIP\_OTW pin, and may have a configuration that reduces the volume to all four channels in an active clipping-prevention circuit.
5. **Overtemperature Warning (OTW), Overtemperature Shutdown (OTSD) and Thermal Foldback** — By default, the CLIP\_OTW pin setting indicates an OTW. One can make changes via I<sup>2</sup>C commands. If selected to indicate a temperature warning, CLIP\_OTW pin assertion occurs when the die temperature reaches warning level 1 as shown in the electrical specifications. The OTW has three temperature thresholds with a 10°C hysteresis. I<sup>2</sup>C register 0x04 indicates each threshold in bits 5, 6, and 7. The device still functions until the temperature reaches the OTSD threshold, at which time the outputs go into Hi-Z mode and the device asserts the FAULT pin. I<sup>2</sup>C is still active in the event of an OTSD, and one can read the registers for faults, but all audio ceases abruptly. After the OTSD resets, one can turn the device back on through I<sup>2</sup>C. The OTW indication remains until the temperature drops below warning level 1. The thermal foldback decreases the channel gain.
6. **Undervoltage (UV) and Power-on-Reset (POR)** — The undervoltage (UV) protection detects low voltages on PVDD, AVDD, and CP. In the event of an undervoltage, the device asserts the FAULT pin and updates the I<sup>2</sup>C register, depending on which voltage caused the event. Power-on reset (POR) occurs when PVDD drops low enough. A POR event causes the I<sup>2</sup>C to go into a high-impedance state. After the device recovers from the POR event, the device re-initialization occur via I<sup>2</sup>C.



## Feature Description (continued)

7. **Overvoltage (OV) and Load Dump** — The OV protection detects high voltages on PVDD. If PVDD reaches the overvoltage threshold, the device asserts the  $\overline{\text{FAULT}}$  pin and updates the I<sup>2</sup>C register. The device can withstand 50-V load-dump voltage spikes.

### 7.3.7 I<sup>2</sup>C Serial Communication Bus

The device communicates with the system processor via the I<sup>2</sup>C serial communication bus as an I<sup>2</sup>C slave-only device. The processor can poll the device via I<sup>2</sup>C to determine the operating status. All reports of fault conditions and detections are via I<sup>2</sup>C. There are also numerous features and operating conditions that one can set via I<sup>2</sup>C.

The I<sup>2</sup>C bus allows control of the following configurations:

- Independent gain control of each channel. The gain can be set to 12 dB, 20 dB, 26 dB, and 32 dB.
- Select the AM non-interference switching frequency
- Select the functionality of the OTW\_CLIP pin
- Enable or disable the dc-detect function with selectable threshold
- Place a channel in Hi-Z (switching stopped) mode (mute)
- Select tweeter detect, set the detection threshold, and initiate the function
- Initiate the open- and shorted-load diagnostic
- Reset faults and return to normal switching operation from Hi-Z mode (unmute)

In addition to the standard SDA and SCL pins for the I<sup>2</sup>C bus, the TAS5414C includes a single pin that allows up to four devices to work together in a system with no additional hardware required for communication or synchronization. The I2C\_ADDR pin sets the device in master or slave mode and selects the I<sup>2</sup>C address for that device. Tie I2C\_ADDR to DGND for master, to 1.2 Vdc for slave 1, to 2.4 Vdc for slave 2, and to D\_BYP for slave 3. The OSC\_SYNC pin is for synchronizing the internal clock oscillators, thereby avoid beat frequencies. One can apply an external oscillator to this pin for external control of the switching frequency.

**Table 1. Table 7. I2C\_ADDR Pin Connection**

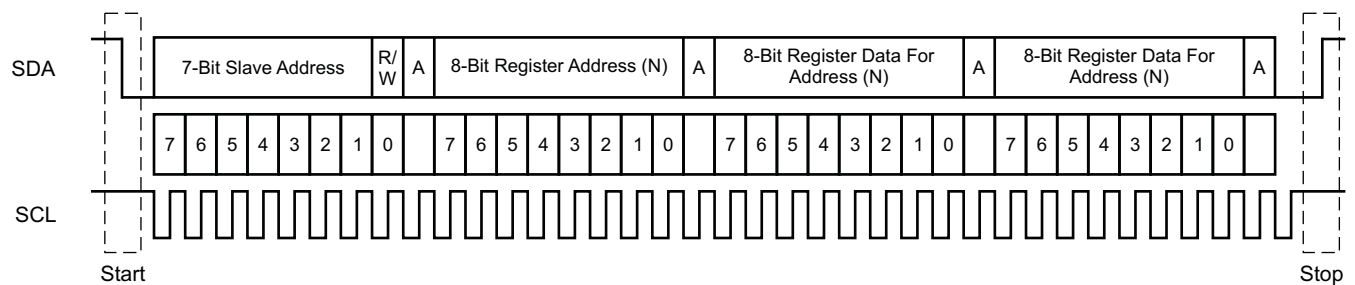
| I2C_ADDR VALUE | I2C_ADDR PIN CONNECTION  | I <sup>2</sup> C ADDRESSES |
|----------------|--|----------------------------|
| 0 (OSC MASTER) | To SGND pin  | 0xD8/D9                    |
| 1 (OSC SLAVE1) | 35% DVDD (resistive voltage divider between D_BYP pin and SGND pin) <sup>(1)</sup> | 0xDA/DB                    |
| 2 (OSC SLAVE2) | 65% DVDD (resistive voltage divider between D_BYP pin and SGND pin) <sup>(1)</sup> | 0xDC/DD                    |
| 3 (OSC SLAVE3) | To D_BYP pin   | 0xDE/DF                    |

(1) TI recommends R<sub>I2C\_ADDR</sub> resistors with 5% or better tolerance.

### 7.3.8 I<sup>2</sup>C Bus Protocol

The TAS5414C has a bidirectional serial control interface that is compatible with the Inter IC (I<sup>2</sup>C) bus protocol and supports 400-kbps data transfer rates for random and sequential write and read operations. This is a slave-only device that does not support a multimaster bus environment or wait-state insertion. The control interface programs the registers of the device and reads device status.

The I<sup>2</sup>C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. Data transfer on the bus is serial, one bit at a time. The transfer of address and data is in byte (8-bit) format with the most-significant bit (MSB) transferred first. In addition, the receiving device acknowledges each byte transferred on the bus with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data terminal (SDA) while the clock is HIGH to indicate a start and stop conditions. A HIGH-to-LOW transition on SDA indicates a start, and a LOW-to-HIGH transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period. Figure 12 shows these conditions. The master generates the 7-bit slave address and the read/write bit to open communication with another device and then wait for an acknowledge condition. The TAS5414C holds SDA LOW during the acknowledge-clock period to indicate an acknowledgment. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/W bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection. There must be an external pullup resistor for the SDA and SCL signals to set the HIGH level for the bus. There is no limit on the number of bytes that one can transmit between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus.



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**Figure 12. Typical I<sup>2</sup>C Sequence**

Use the I2C\_ADDR pin (pin 2) to program the device for one of four addresses. These four addresses are licensed I<sup>2</sup>C addresses and do not conflict with other licensed I<sup>2</sup>C audio devices. To communicate with the TAS5414C, the I<sup>2</sup>C master uses addresses shown in Figure 12. Transmission of read and write data can be via single-byte or multiple-byte data transfers.

### 7.3.9 Hardware Control Pins

There are four discrete hardware pins for real-time control and indication of device status.

1. **FAULT** pin: This active-low open-drain output pin indicates the presence of a fault condition that requires the device to go into the Hi-Z mode or standby mode. On assertion of this pin, the device has protected itself and the system from potential damage. One can read the exact nature of the fault via I<sup>2</sup>C with the exception of PVDD undervoltage faults below POR, in which case the I<sup>2</sup>C bus is no longer operational. However, the fault is still indicated due to FAULT pin assertion.
2. **CLIP\_OTW** pin: Configured via I<sup>2</sup>C, this active-low open-drain pin\ indicates one of the following conditions: overtemperature warning, the detection of clipping, or the logical OR of both of these conditions. During tweeter detect diagnostics, assertion of this pin also occurs when a tweeter is present. If overtemperature warning is set, the device can also indicate thermal foldback on this pin.
3. **MUTE** pin: This active-low pin is used for hardware control of the mute-unmute function for all four channels. Capacitor C<sub>MUTE</sub> controls the time constant for the gain ramp needed to produce a pop- and click-free mute function. For pop- and click-free operation, implementation of the mute function should be through I<sup>2</sup>C commands. The use of a hard mute with an external transistor does not ensure pop- and click-free operation, and TI does not recommended it except as an *emergency hard mute* function in case of a loss of I<sup>2</sup>C control. Sharing the C<sub>MUTE</sub> capacitor between multiple devices is disallowed.
4. **STANDBY** pin: On assertion of this active-low pin, the device goes into a complete shutdown, and the typical current-draw limit is 2  $\mu$ A, typical. STANDBY can be used to shut down the device rapidly. If all channels are in Hi-Z, the device enters standby in approximately 1 ms. All I<sup>2</sup>C register content is lost and the I<sup>2</sup>C bus goes into the high-impedance state on assertion of the STANDBY pin.

### 7.3.10 AM Radio Avoidance

To reduce interference in the AM radio band, the device has the ability to change the switching frequency via I<sup>2</sup>C commands. Table 2 lists the recommended frequencies. The fundamental frequency and its second harmonic straddle the AM radio band listed. This eliminates the tones that can be present due to demodulation of the switching frequency by the AM radio.

**Table 2. Recommended Switching Frequencies for AM Mode Operation**

| US                    |                                 | EUROPEAN              |                                 |
|-----------------------|---------------------------------|-----------------------|---------------------------------|
| AM FREQUENCY<br>(kHz) | SWITCHING<br>FREQUENCY<br>(kHz) | AM FREQUENCY<br>(kHz) | SWITCHING<br>FREQUENCY<br>(kHz) |
| 540–670               | 417                             | 522–675               | 417                             |
| 680–980               | 500                             | 676–945               | 500                             |
| 990–1180              | 417                             | 946–1188              | 417                             |
| 1190–1420             | 500                             | 1189–1422             | 500                             |
| 1430–1580             | 417                             | 1423–1584             | 417                             |
| 1590–1700             | 500                             | 1585–1701             | 500                             |

## 7.4 Device Functional Modes

Table 3 through Table 5 depict the operating modes and faults.

**Table 3. Operating Modes**

| STATE NAME       | OUTPUT FETS          | CHARGE PUMP | OSCILLATOR | I <sup>2</sup> C | AVDD and DVDD |
|------------------|----------------------|-------------|------------|------------------|---------------|
| STANDBY          | Hi-Z, floating       | Stopped     | Stopped    | Stopped          | OFF           |
| Hi-Z             | Hi-Z, weak pulldown  | Active      | Active     | Active           | ON            |
| Mute             | Switching at 50%     | Active      | Active     | Active           | ON            |
| Normal operation | Switching with audio | Active      | Active     | Active           | ON            |

**Table 4. Global Faults and Actions**

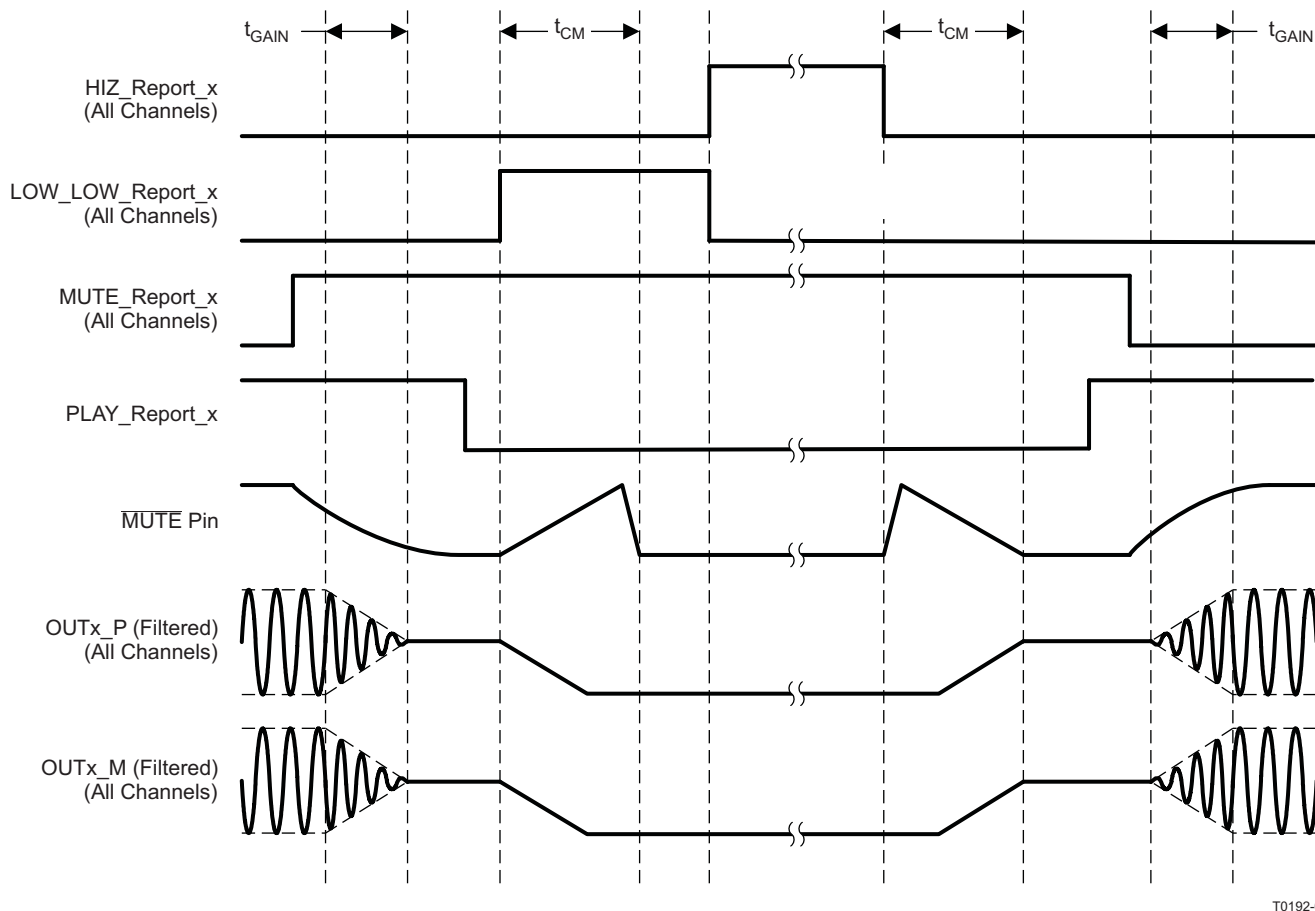
| FAULT OR EVENT | FAULT OR EVENT CATEGORY | MONITORING MODES   | REPORTING METHOD                                       | ACTION TYPE         | ACTION RESULT | LATCHED OR SELF-CLEARING |
|----------------|-------------------------|--------------------|--|---------------------|---------------|--------------------------|
| POR            | Voltage fault           | All                | $\overline{\text{FAULT}}$ pin                          | Hard mute (no ramp) | Standby       | Self-clearing            |
| UV             |                         | Hi-Z, mute, normal | $\text{I}^2\text{C} + \overline{\text{FAULT}}$ pin     |                     | Hi-Z          | Latched                  |
| CP UV          |                         |                    |  |                     |               |                          |
| OV             |                         | All                | $\overline{\text{FAULT}}$ pin                          |                     | Standby       | Self-clearing            |
| Load dump      |                         |                    |  |                     |               |                          |
| OTW            | Thermal warning         | Hi-Z, mute, normal | $\text{I}^2\text{C} + \overline{\text{CLIP\_OTW}}$ pin | None                | None          | Self-clearing            |
| OTSD           | Thermal fault           | Hi-Z, mute, normal | $\text{I}^2\text{C} + \overline{\text{FAULT}}$ pin     | Hard mute (no ramp) | Standby       | Latched                  |

**Table 5. Channel Faults and Actions**

| FAULT/<br>EVENT           | FAULT OR EVENT<br>CATEGORY | MONITORING<br>MODES               | REPORTING<br>METHOD                                     | ACTION<br>TYPE | ACTION<br>RESULT  | LATCHED OR<br>SELF-<br>CLEARING |
|---------------------------|----------------------------|-----------------------------------|---|----------------|-------------------|---------------------------------|
| Open-short<br>diagnostic  | Diagnostic                 | Hi-Z (I <sup>2</sup> C activated) | I <sup>2</sup> C  | None           | None              | Latched                         |
| Clipping                  | Warning                    | Mute / Play                       | $\overline{\text{CLIP\_OTW}}$ pin                       | None           | None              | Self-clearing                   |
| CBC load current<br>limit | Online protection          |                                   |   | Current Limit  | Start OC<br>timer | Self-clearing                   |
| OC fault                  | Output channel fault       |                                   | I <sup>2</sup> C + $\overline{\text{FAULT}}$ pin        | Hard mute      | Hi-Z              | Latched                         |
| DC detect                 |                            |                                   |   | Hard mute      | Hi-Z              | Latched                         |
| OT Foldback               | Warning                    |                                   | I <sup>2</sup> C + $\overline{\text{CLIP\_OTW}}$<br>pin | Reduce Gain    | None              | Self-clearing                   |

### 7.4.1 Audio Shutdown and Restart Sequence

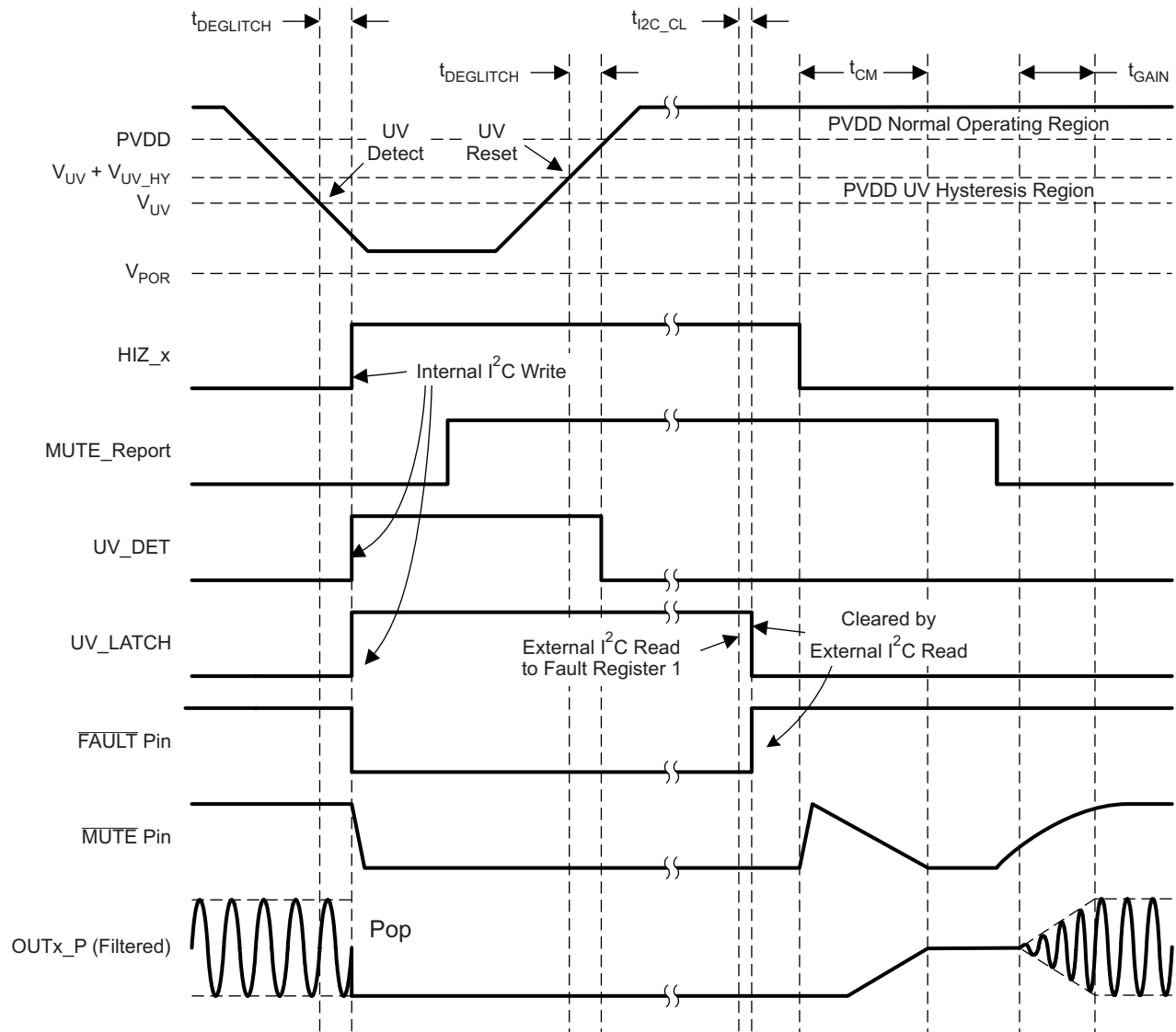
The gain ramp of the filtered output signal and the updating of the I<sup>2</sup>C registers correspond to the MUTE pin voltage during the ramping process. The value of the external capacitor on the MUTE pin dictates the length of time that the MUTE pin takes to complete its ramp. With the default 220-nF capacitor, the turnon common-mode ramp takes approximately 26 ms and the gain ramp takes approximately 76 ms.



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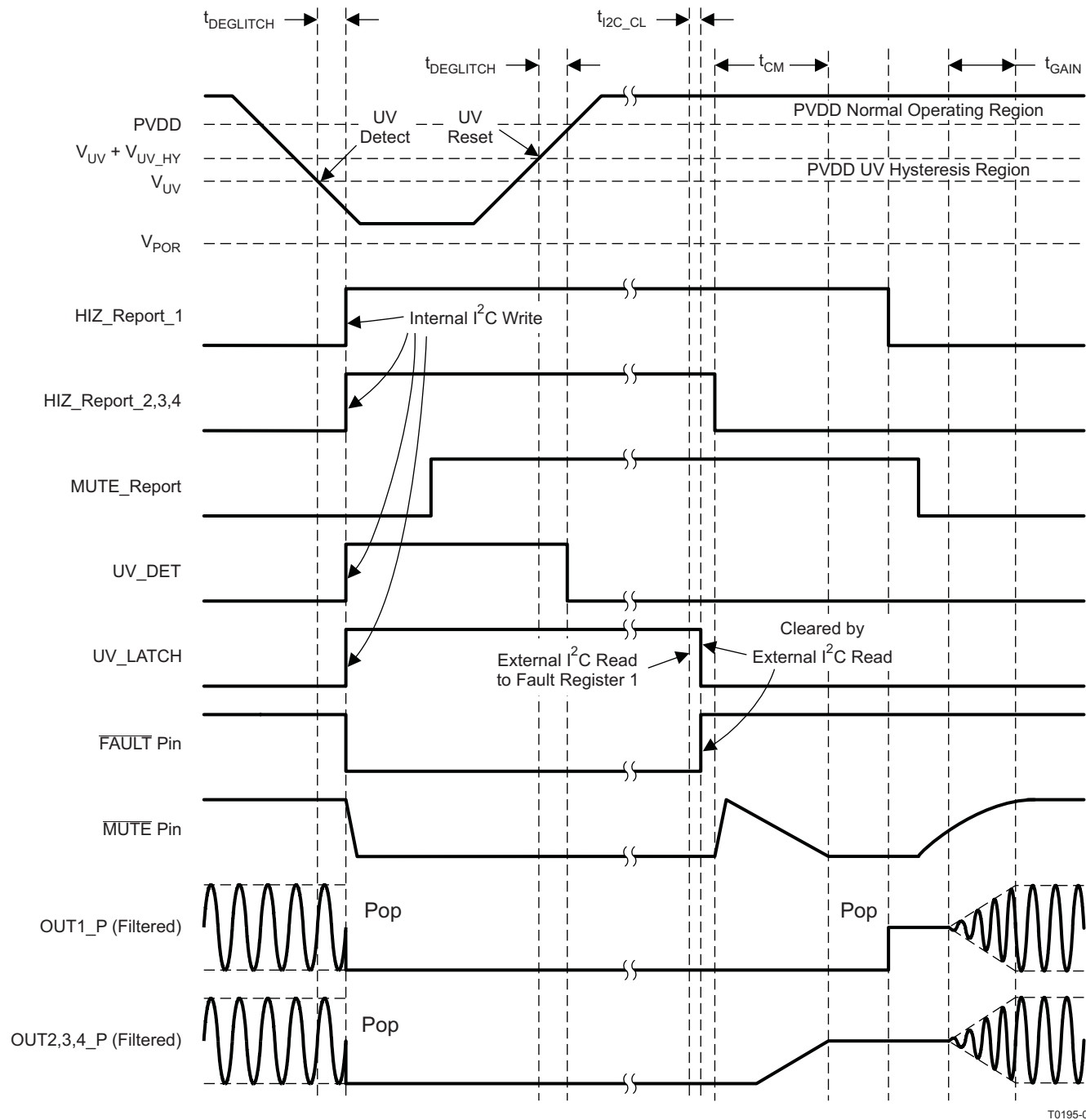
**Figure 13. Timing Diagram for Click- and Pop-Free Shutdown and Restart Sequence**

### 7.4.2 Latched-Fault Shutdown and Restart Sequence Control



T0194-02

**Figure 14. Timing Diagram for Latched-Global-Fault Shutdown and Restart (UV Shutdown and Recovery)**



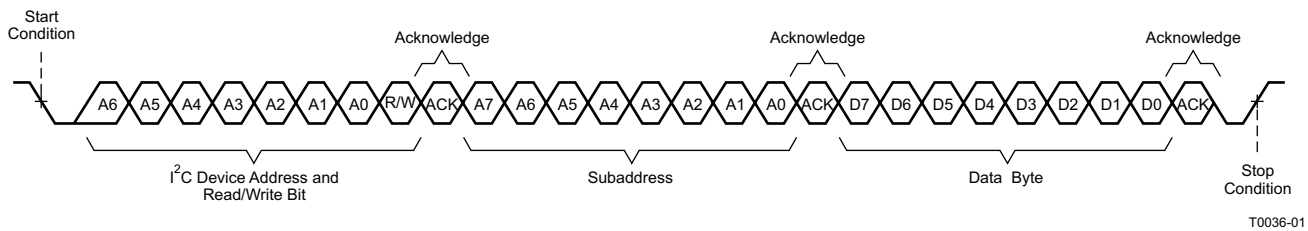
T0195-02

**Figure 15. Timing Diagram for Latched-Global-Fault Shutdown and Individual-Channel Restart (UV Shutdown and Recovery)**

## 7.5 Programming

### 7.5.1 Random Write

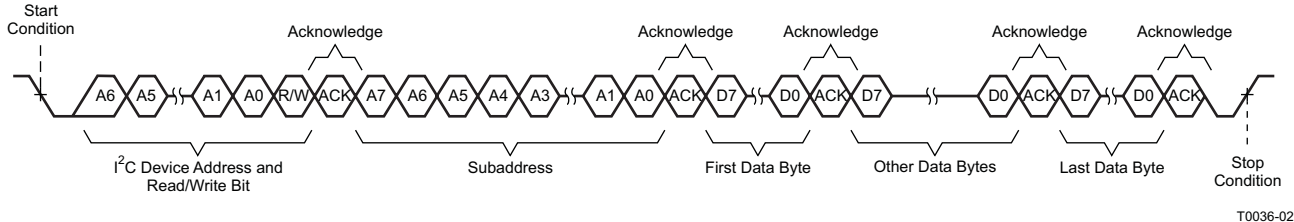
As shown in [Figure 16](#), a random write or single-byte write transfer begins with the master device transmitting a start condition followed by the I<sup>2</sup>C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a single-byte write data transfer, the read/write bit is a 0. After receiving the correct I<sup>2</sup>C device address and the read/write bit, the device responds with an acknowledge bit. Next, the master transmits the address byte or bytes corresponding to the internal memory address being accessed. After receiving the address byte, the device again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the TAS5414C again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte write transfer.



**Figure 16. Random-Write Transfer**

### 7.5.2 Sequential Write

A sequential write transfer is identical to a single-byte data-write transfer except for the transmission of multiple data bytes by the master device to TAS5414C as shown in [Figure 17](#). After receiving each data byte, the device responds with an acknowledge bit and automatically increments the I<sup>2</sup>C subaddress by one.



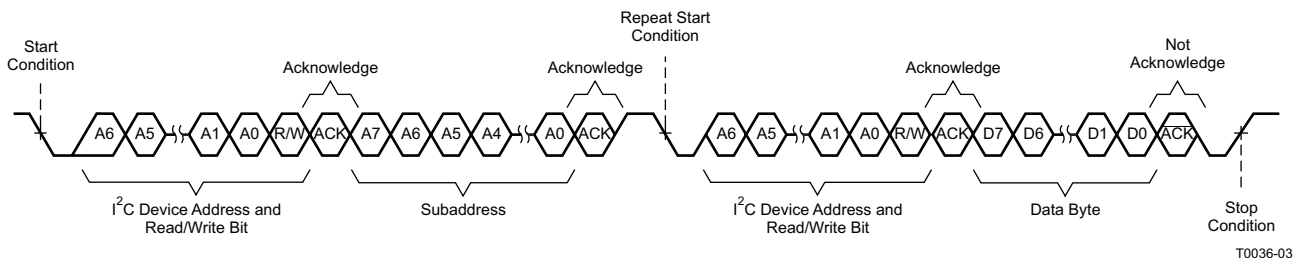
**Figure 17. Sequential Write Transfer**



## Programming (continued)

### 7.5.3 Random Read

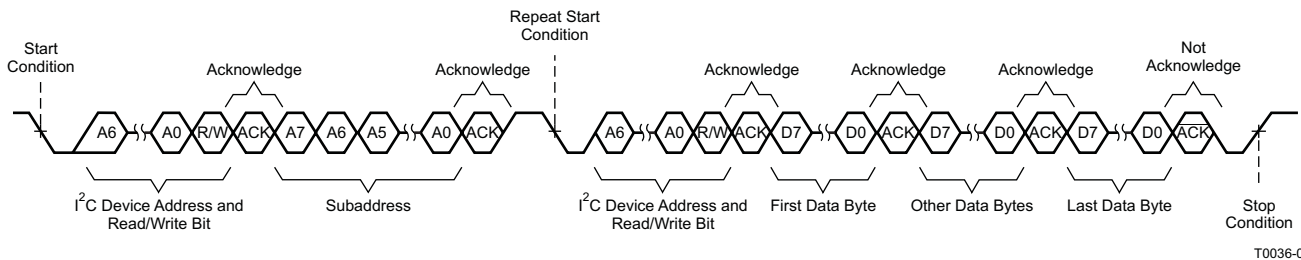
As shown in Figure 18, a random read or single-byte read transfer begins with the master device transmitting a start condition followed by the I<sup>2</sup>C device address and the read/write bit. For the single-byte read transfer, the master device transmits both a write followed by a read. Initially, a write transfers the address byte or bytes of the internal memory address to be read. Thus, the read/write bit is a 0. After receiving the address and the read/write bit, the TAS5414C responds with an acknowledge bit. In addition, after sending the internal memory address byte or bytes, the master device transmits another start condition followed by the device address and the read/write bit again. This time the read/write bit is a 1, indicating a read transfer. After receiving the address and the read/write bit, the device again responds with an acknowledge bit. Next, the TAS5414C transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the single-byte read transfer.



**Figure 18. Random Read Transfer**

### 7.5.4 Sequential Read

A sequential read transfer is identical to a single-byte read transfer except for the transmission of multiple data bytes by the TAS5414C to the master device as shown in Figure 19. Except for the last data byte, the master device responds with an acknowledge bit after receiving each data byte and automatically increments the I<sup>2</sup>C subaddress by one. After receiving the last data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the transfer.



**Figure 19. Sequential Read Transfer**

## 7.6 Register Maps

### 7.6.1 Register Summary

**Table 6. TAS5414C I<sup>2</sup>C Addresses**

| I <sup>2</sup> C_ADDR VALUE |                        | FIXED ADDRESS |   |   |   |   | SELECTABLE WITH ADDRESS PIN |   | READ/WRITE BIT | I <sup>2</sup> C ADDRESS |
|-----------------------------|------------------------|---------------|---|---|---|---|-----------------------------|---|----------------|--------------------------|
|                             |                        | MSB           | 6 | 5 | 4 | 3 | 2                           | 1 | LSB            |                          |
| 0 (OSC MASTER)              | I <sup>2</sup> C WRITE | 1             | 1 | 0 | 1 | 1 | 0                           | 0 | 0              | 0xD8                     |
|                             | I <sup>2</sup> C READ  | 1             | 1 | 0 | 1 | 1 | 0                           | 0 | 1              | 0xD9                     |
| 1 (OSC SLAVE1)              | I <sup>2</sup> C WRITE | 1             | 1 | 0 | 1 | 1 | 0                           | 1 | 0              | 0xDA                     |
|                             | I <sup>2</sup> C READ  | 1             | 1 | 0 | 1 | 1 | 0                           | 1 | 1              | 0xDB                     |
| 2 (OSC SLAVE2)              | I <sup>2</sup> C WRITE | 1             | 1 | 0 | 1 | 1 | 1                           | 0 | 0              | 0xDC                     |
|                             | I <sup>2</sup> C READ  | 1             | 1 | 0 | 1 | 1 | 1                           | 0 | 1              | 0xDD                     |
| 3 (OSC SLAVE3)              | I <sup>2</sup> C WRITE | 1             | 1 | 0 | 1 | 1 | 1                           | 1 | 0              | 0xDE                     |
|                             | I <sup>2</sup> C READ  | 1             | 1 | 0 | 1 | 1 | 1                           | 1 | 1              | 0xDF                     |

**Table 7. I<sup>2</sup>C Address Register Definitions**

| ADDRESS    | TYPE        | REGISTER DESCRIPTION  |
|------------|-------------|---|
| 0x00       | Read        | Latched fault register 1, global and channel fault                        |
| 0x01       | Read        | Latched fault register 2, dc offset and overcurrent detect                |
| 0x02       | Read        | Latched diagnostic register 1, load diagnostics                           |
| 0x03       | Read        | Latched diagnostic register 2, load diagnostics                           |
| 0x04       | Read        | External status register 1, temperature and voltage detect                |
| 0x05       | Read        | External status register 2, Hi-Z and low-low state                        |
| 0x06       | Read        | External status register 3, mute and play modes                           |
| 0x07       | Read        | External status register 4, load diagnostics                              |
| 0x08       | Read, Write | External control register 1, channel gain select                          |
| 0x09       | Read, Write | External control register 2, overcurrent control                          |
| 0x0A       | Read, Write | External control register 3, switching frequency and clip pin select      |
| 0x0B       | Read, Write | External control register 4, load diagnostic, master mode select          |
| 0x0C       | Read, Write | External control register 5, output state control                         |
| 0x0D       | Read, Write | External control register 6, output state control                         |
| 0x0E, 0x0F | –           | Not used  |
| 0x10       | Read, Write | External control register 7, dc detect threshold selection                |
| 0x13       | Read        | External status register 5, overtemperature shutdown and thermal foldback |

### 7.6.2 Registers

#### 7.6.2.1 Fault Register 1 (0x00) Protection

**Figure 20. Fault Register 1 (0x00) Protection**

| 7       | 6       | 5       | 4     | 3    | 2    | 1      | 0   |
|---------|---------|---------|-------|------|------|--------|-----|
| PVDD_OV | PVDD_UV | AVDD_UV | CP_UV | OTSD | OCSD | DC_OFF | OTW |
| R       | R       | R       | R     | R    | R    | R      | R   |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 8. Fault Register 1 (0x00) Protection Field Descriptions**

| Bit | Field   | Type | Reset | Description                     |
|-----|---------|------|-------|---------------------------------|
| 7   | PVDD_OV | R    | 0     | PVDD overvoltage has occurred.  |
| 6   | PVDD_UV | R    | 0     | PVDD undervoltage has occurred. |

**Table 8. Fault Register 1 (0x00) Protection Field Descriptions (continued)**

| Bit | Field   | Type | Reset | Description                                       |
|-----|---------|------|-------|---|
| 5   | AVDD_UV | R    | 0     | AVDD, analog voltage, undervoltage has occurred.  |
| 4   | CP_UV   | R    | 0     | Charge-pump undervoltage has occurred.            |
| 3   | OTSD    | R    | 0     | Overtemperature shutdown has occurred.            |
| 2   | OCSD    | R    | 0     | Overcurrent shutdown has occurred in any channel. |
| 1   | DC_OFF  | R    | 0     | DC offset has occurred in any channel.            |
| 0   | OTW     | R    | 0     | Overtemperature warning has occurred.             |

### 7.6.3 Fault Register 2 (0x01) Protection

**Figure 21. Fault Register 2 (0x01) Protection**

| 7          | 6          | 5          | 4          | 3        | 2        | 1        | 0        |
|------------|------------|------------|------------|----------|----------|----------|----------|
| DC_OFF_CH4 | DC_OFF_CH3 | DC_OFF_CH2 | DC_OFF_CH1 | OCSD_CH4 | OCSD_CH3 | OCSD_CH2 | OCSD_CH1 |
| R          | R          | R          | R          | R        | R        | R        | R        |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 9. Fault Register 2 (0x01) Protection Field Descriptions**

| Bit | Field      | Type | Reset | Description                                  |
|-----|------------|------|-------|--|
| 7   | DC_OFF_CH4 | R    | 0     | DC offset channel 4 has occurred.            |
| 6   | DC_OFF_CH3 | R    | 0     | DC offset channel 3 has occurred.            |
| 5   | DC_OFF_CH2 | R    | 0     | DC offset channel 2 has occurred.            |
| 4   | DC_OFF_CH1 | R    | 0     | DC offset channel 1 has occurred.            |
| 3   | OCSD_CH4   | R    | 0     | Overcurrent shutdown channel 4 has occurred. |
| 2   | OCSD_CH3   | R    | 0     | Overcurrent shutdown channel 3 has occurred. |
| 1   | OCSD_CH2   | R    | 0     | Overcurrent shutdown channel 2 has occurred. |
| 0   | OCSD_CH1   | R    | 0     | Overcurrent shutdown channel 1 has occurred. |

### 7.6.4 Diagnostic Register 1 (0x02) Load Diagnostics

**Figure 22. Diagnostic Register 1 (0x02) Load Diagnostics**

| 7      | 6      | 5       | 4       | 3      | 2      | 1       | 0       |
|--------|--------|---------|---------|--------|--------|---------|---------|
| OL_CH2 | SL_CH2 | S2P_CH2 | S2G_CH2 | OL_CH1 | SL_CH1 | S2P_CH1 | S2G_CH1 |
| R      | R      | R       | R       | R      | R      | R       | R       |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 10. Diagnostic Register 1 (0x02) Load Diagnostics Field Descriptions**

| Bit | Field   | Type | Reset | Description                                    |
|-----|---------|------|-------|--|
| 7   | OL_CH2  | R    | 0     | Open load channel 2 has occurred.              |
| 6   | SL_CH2  | R    | 0     | Shorted load channel 2 has occurred.           |
| 5   | S2P_CH2 | R    | 0     | Output short to PVDD channel 2 has occurred.   |
| 4   | S2G_CH2 | R    | 0     | Output short to ground channel 2 has occurred. |
| 3   | OL_CH1  | R    | 0     | Open load channel 1 has occurred.              |
| 2   | SL_CH1  | R    | 0     | Shorted load channel 1 has occurred.           |
| 1   | S2P_CH1 | R    | 0     | Output short to PVDD channel 1 has occurred.   |
| 0   | S2G_CH1 | R    | 0     | Output short to ground channel 1 has occurred. |

### 7.6.5 Diagnostic Register 2 (0x03) Load Diagnostics

**Figure 23. Diagnostic Register 2 (0x03) Load Diagnostics**

| 7      | 6      | 5       | 4       | 3      | 2      | 1       | 0       |
|--------|--------|---------|---------|--------|--------|---------|---------|
| OL_CH4 | SL_CH4 | S2P_CH4 | S2G_CH4 | OL_CH3 | SL_CH3 | S2P_CH3 | S2G_CH3 |
| R      | R      | R       | R       | R      | R      | R       | R       |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 11. Diagnostic Register 2 (0x03) Load Diagnostics Field Descriptions**

| Bit | Field   | Type | Reset | Description                                    |
|-----|---------|------|-------|--|
| 7   | OL_CH4  | R    | 0     | Open load channel 4 has occurred.              |
| 6   | SL_CH4  | R    | 0     | Shorted load channel 4 has occurred.           |
| 5   | S2P_CH4 | R    | 0     | Output short to PVDD channel 4 has occurred.   |
| 4   | S2G_CH4 | R    | 0     | Output short to ground channel 4 has occurred. |
| 3   | OL_CH3  | R    | 0     | Open load channel 3 has occurred.              |
| 2   | SL_CH3  | R    | 0     | Shorted load channel 3 has occurred.           |
| 1   | S2P_CH3 | R    | 0     | Output short to PVDD channel 3 has occurred.   |
| 0   | S2G_CH3 | R    | 0     | Output short to ground channel 3 has occurred. |

### 7.6.6 External Status Register 1 (0x04) Fault Detection

**Figure 24. External Status Register 1 (0x04) Fault Detection**

| 7         | 6 | 5 | 4       | 3       | 2          | 1          | 0          |
|-----------|---|---|---------|---------|------------|------------|------------|
| OTW_LEVEL |   |   | OTSD_ST | CPUV_ST | AVDD_UV_ST | PVDD_UV_ST | PVDD_OV_ST |
| R         | R | R | R       | R       | R          | R          | R          |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 12. External Status Register 1 (0x04) Fault Detection Field Descriptions**

| Bit | Field      | Type | Reset | Description  |
|-----|------------|------|-------|--|
| 7-5 | OTW_LEVEL  | R    | 000   | Overtemperature warning:<br>000: Default value<br>001: Overtemperature warning<br>011: Overtemperature warning 1<br>101: Overtemperature warning 2<br>111: Overtemperature warning 3 |
| 4   | OTSD_ST    | R    | 0     | Overtemperature shutdown is present.   |
| 3   | CPUV_ST    | R    | 0     | Charge-pump voltage fault is present.  |
| 2   | AVDD_UV_ST | R    | 0     | AVDD, analog voltage fault is present.   |
| 1   | PVDD_UV_ST | R    | 0     | PVDD undervoltage fault is present.  |
| 0   | PVDD_OV_ST | R    | 0     | PVDD overvoltage fault is present.   |

### 7.6.7 External Status Register 2 (0x05) Output State of Individual Channels

**Figure 25. External Status Register 2 (0x05) Output State of Individual Channels**

| 7         | 6         | 5         | 4         | 3          | 2          | 1          | 0          |
|-----------|-----------|-----------|-----------|------------|------------|------------|------------|
| CH4_LL_ST | CH3_LL_ST | CH2_LL_ST | CH1_LL_ST | CH4_HIZ_ST | CH3_HIZ_ST | CH2_HIZ_ST | CH1_HIZ_ST |
| R         | R         | R         | R         | R          | R          | R          | R          |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 13. External Status Register 2 (0x05) Output State of Individual Channels Field Descriptions**

| Bit | Field     | Type | Reset | Description  |
|-----|-----------|------|-------|--|
| 7   | CH4_LL_ST | R    | 0     | Channel 4 low-low mode (0 = not low-low, 1 = low-low) <sup>(1)</sup> |
| 6   | CH3_LL_ST | R    | 0     | Channel 3 low-low mode (0 = not low-low, 1 = low-low) <sup>(1)</sup> |

**Table 13. External Status Register 2 (0x05) Output State of Individual Channels Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description  |
|-----|------------|------|-------|--|
| 5   | CH2_LL_ST  | R    | 0     | Channel 2 low-low mode (0 = not low-low, 1 = low-low) <sup>(1)</sup> |
| 4   | CH1_LL_ST  | R    | 0     | Channel 1 low-low mode (0 = not low-low, 1 = low-low) <sup>(1)</sup> |
| 3   | CH4_HIZ_ST | R    | 1     | Channel 4 Hi-Z mode (0 = not Hi-Z, 1 = Hi-Z)                         |
| 2   | CH3_HIZ_ST | R    | 1     | Channel 3 Hi-Z mode (0 = not Hi-Z, 1 = Hi-Z)                         |
| 1   | CH2_HIZ_ST | R    | 1     | Channel 2 Hi-Z mode (0 = not Hi-Z, 1 = Hi-Z)                         |
| 0   | CH1_HIZ_ST | R    | 1     | Channel 1 Hi-Z mode (0 = not Hi-Z, 1 = Hi-Z)                         |

(1) Low-low is defined as both outputs actively pulled to ground.

## 7.6.8 External Status Register 3 (0x06) Play and Mute Modes

**Figure 26. External Status Register 3 (0x06) Play and Mute Modes**

| 7                | 6                | 5                | 4                | 3           | 2           | 1           | 0           |
|------------------|------------------|------------------|------------------|-------------|-------------|-------------|-------------|
| CH4_MUTE_ST<br>T | CH3_MUTE_ST<br>T | CH2_MUTE_ST<br>T | CH1_MUTE_ST<br>T | CH4_PLAY_ST | CH3_PLAY_ST | CH2_PLAY_ST | CH1_PLAY_ST |
| R                | R                | R                | R                | R           | R           | R           | R           |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 14. External Status Register 3 (0x06) Play and Mute Modes Field Descriptions**

| Bit | Field       | Type | Reset | Description                     |
|-----|-------------|------|-------|---------------------------------|
| 7   | CH4_MUTE_ST | R    | 0     | Channel 4 mute mode is enabled. |
| 6   | CH3_MUTE_ST | R    | 0     | Channel 3 mute mode is enabled. |
| 5   | CH2_MUTE_ST | R    | 0     | Channel 2 mute mode is enabled. |
| 4   | CH1_MUTE_ST | R    | 0     | Channel 1 mute mode is enabled. |
| 3   | CH4_PLAY_ST | R    | 0     | Channel 4 play mode is enabled. |
| 2   | CH3_PLAY_ST | R    | 0     | Channel 3 play mode is enabled. |
| 1   | CH2_PLAY_ST | R    | 0     | Channel 2 play mode is enabled. |
| 0   | CH1_PLAY_ST | R    | 0     | Channel 1 play mode is enabled. |

## 7.6.9 External Status Register 4 (0x07) Load Diagnostics

**Figure 27. External Status Register 4 (0x07) Load Diagnostics**

| 7        | 6        | 5        | 4        | 3               | 2               | 1               | 0               |
|----------|----------|----------|----------|-----------------|-----------------|-----------------|-----------------|
| CH4_OTFB | CH3_OTFB | CH2_OTFB | CH1_OTFB | CH4_LD_MOD<br>E | CH3_LD_MOD<br>E | CH2_LD_MOD<br>E | CH1_LD_MOD<br>E |
| R        | R        | R        | R        | R               | R               | R               | R               |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 15. External Status Register 4 (0x07) Load Diagnostics Field Descriptions**

| Bit | Field       | Type | Reset | Description                               |
|-----|-------------|------|-------|---|
| 7   | CH4_OTFB    | R    | 0     | Channel 4 is in overtemperature foldback. |
| 6   | CH3_OTFB    | R    | 0     | Channel 3 is in overtemperature foldback. |
| 5   | CH2_OTFB    | R    | 0     | Channel 2 is in overtemperature foldback. |
| 4   | CH1_OTFB    | R    | 0     | Channel 1 is in overtemperature foldback. |
| 3   | CH4_LD_MODE | R    | 0     | Channel 4 is in load diagnostics mode.    |
| 2   | CH3_LD_MODE | R    | 0     | Channel 3 is in load diagnostics mode.    |
| 1   | CH2_LD_MODE | R    | 0     | Channel 2 is in load diagnostics mode.    |
| 0   | CH1_LD_MODE | R    | 0     | Channel 1 is in load diagnostics mode.    |

## 7.6.10 External Control Register 1 (0x08) Gain Select

**Figure 28. External Control Register 1 (0x08) Gain Select**

| 7        | 6   | 5        | 4   | 3        | 2   | 1        | 0   |
|----------|-----|----------|-----|----------|-----|----------|-----|
| GAIN_CH4 |     | GAIN_CH3 |     | GAIN_CH2 |     | GAIN_CH1 |     |
| R/W      | R/W | R/W      | R/W | R/W      | R/W | R/W      | R/W |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 16. External Control Register 1 (0x08) Gain Select Field Descriptions**

| Bit | Field    | Type | Reset | Description   |
|-----|----------|------|-------|---|
| 7-6 | GAIN_CH4 | R/W  | 10    | Set channel 4 gain.<br>10: Set channel 4 gain to 26 dB (Default)<br>00: Set channel 4 gain to 12 dB<br>01: Set channel 4 gain to 20 dB<br>11: Set channel 4 gain to 32 dB |
| 5-4 | GAIN_CH3 | R/W  | 10    | Set channel 3 gain.<br>10: Set channel 3 gain to 26 dB (Default)<br>00: Set channel 3 gain to 12 dB<br>01: Set channel 3 gain to 20 dB<br>11: Set channel 3 gain to 32 dB |
| 3-2 | GAIN_CH2 | R/W  | 10    | Set channel 2 gain.<br>10: Set channel 2 gain to 26 dB (Default)<br>00: Set channel 2 gain to 12 dB<br>01: Set channel 2 gain to 20 dB<br>11: Set channel 2 gain to 32 dB |
| 1-0 | GAIN_CH1 | R/W  | 10    | Set channel 1 gain.<br>10: Set channel 1 gain to 26 dB (Default)<br>00: Set channel 1 gain to 12 dB<br>01: Set channel 1 gain to 20 dB<br>11: Set channel 1 gain to 32 dB |

## 7.6.11 External Control Register 2 (0x09) Overcurrent Control

**Figure 29. External Control Register 2 (0x09) Overcurrent Control**

| 7      | 6      | 5      | 4      | 3        | 2   | 1        | 0   |
|--------|--------|--------|--------|----------|-----|----------|-----|
| CH4_OC | CH4_OC | CH4_OC | CH4_OC | RESERVED |     | THFB_DIS |     |
| R/W    | R/W    | R/W    | R/W    | R/W      | R/W | R/W      | R/W |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 17. External Control Register 2 (0x09) Overcurrent Control Field Descriptions**

| Bit | Field    | Type | Reset | Description   |
|-----|----------|------|-------|---|
| 7   | CH4_OC   | R/W  | 1     | Set channel 4 overcurrent limit ( 0 - level 1, 1 - level 2) |
| 6   | CH3_OC   | R/W  | 1     | Set channel 3 overcurrent limit ( 0 - level 1, 1 - level 2) |
| 5   | CH2_OC   | R/W  | 1     | Set channel 2 overcurrent limit ( 0 - level 1, 1 - level 2) |
| 4   | CH1_OC   | R/W  | 1     | Set channel 1 overcurrent limit ( 0 - level 1, 1 - level 2) |
| 3-1 | Reserved | R/W  | 0     | Reserved  |
| 0   | THFB_DIS | R/W  | 0     | Disable thermal foldback                                    |

## 7.6.12 External Control Register 3 (0x0A) Switching Frequency Select and Clip\_OTW Configuration

**Figure 30. External Control Register 3 (0x0A) Switching Frequency Select and Clip\_OTW Configuration**

| 7                     | 6                 | 5            | 4                | 3                    | 2 | 1               | 0 |
|-----------------------|-------------------|--------------|------------------|----------------------|---|-----------------|---|
| CLIP_OTW_TH_FB<br>R/W | SYNC_PULSE<br>R/W | PHASE<br>R/W | HARD_STOP<br>R/W | CLIP_OTW_CONF<br>R/W |   | PWM_FREQ<br>R/W |   |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 18. External Control Register 3 (0x0A) Switching Frequency Select and Clip\_OTW Configuration Field Descriptions**

| Bit | Field         | Type | Reset | Description   |
|-----|---------------|------|-------|---|
| 7   | CLIP_OTW_THFB | R/W  | 0     | Configure $\overline{\text{CLIP\_OTW}}$ pin to report thermal foldback  |
| 6   | SYNC_PULSE    | R/W  | 0     | Send sync pulse from OSC_SYNC pin (device must be in master mode).  |
| 5   | PHASE         | R/W  | 0     | Set $f_s$ to a 180° phase difference between adjacent channels.   |
| 4   | HARD_STOP     | R/W  | 0     | Enable hard-stop mode.  |
| 3-2 | CLIP_OTW_CONF | R/W  | 11    | Configure $\overline{\text{CLIP\_OTW}}$ pin.<br>11: CLIP_OTW pin does not report thermal foldback (Default)<br>00: Configure $\overline{\text{CLIP\_OTW}}$ pin to report tweeter detect only.<br>01: Configure $\overline{\text{CLIP\_OTW}}$ pin to report clip detect only.<br>10: Configure $\overline{\text{CLIP\_OTW}}$ pin to report overtemperature warning only. |
| 1-0 | PWM_FREQ      | R/W  | 01    | Set $f_s$ .<br>01: Set $f_s$ = 417 kHz (Default)<br>00: Set $f_s$ = 500 kHz<br>10: Set $f_s$ = 357 kHz<br>11: Invalid frequency selection (do not set)  |

### 7.6.13 External Control Register 4 (0x0B) Load Diagnostics and Master/Slave Control

**Figure 31. External Control Register 4 (0x0B) Load Diagnostics and Master/Slave Control**

| 7                      | 6               | 5                | 4                 | 3                | 2                | 1                | 0                |
|------------------------|-----------------|------------------|-------------------|------------------|------------------|------------------|------------------|
| EN_CLK_OSC_SYNC<br>R/W | EN_SLAVE<br>R/W | EN_TW_DET<br>R/W | DIS_DC_DET<br>R/W | EN_CH4_LD<br>R/W | EN_CH3_LD<br>R/W | EN_CH2_LD<br>R/W | EN_CH1_LD<br>R/W |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 19. (External Control Register 4 (0x0B) Load Diagnostics and Master/Slave Control Field Descriptions**

| Bit | Field           | Type | Reset | Description   |
|-----|-----------------|------|-------|---|
| 7   | EN_CLK_OSC_SYNC | R/W  | 0     | Enable clock output on OSC_SYNC pin (valid only in master mode) |
| 6   | EN_SLAVE        | R/W  | 1     | Enable slave mode (external oscillator is necessary)            |
| 5   | EN_TW_DET       | R/W  | 0     | Enable tweeter-detect mode                                      |
| 4   | DIS_DC_DET      | R/W  | 1     | Disable dc detection on all channels                            |
| 3   | EN_CH4_LD       | R/W  | 0     | Run channel 4 load diagnostics                                  |
| 2   | EN_CH3_LD       | R/W  | 0     | Run channel 3 load diagnostics                                  |
| 1   | EN_CH2_LD       | R/W  | 0     | Run channel 2 load diagnostics                                  |
| 0   | EN_CH1_LD       | R/W  | 0     | Run channel 1 load diagnostics                                  |

### 7.6.14 External Control Register 5 (0x0C) Output Control

**Figure 32. External Control Register 5 (0x0C) Output Control**

| 7   | 6        | 5             | 4           | 3        | 2        | 1        | 0        |
|-----|----------|---------------|-------------|----------|----------|----------|----------|
| RST | Reserved | DC_DET_SD_DIS | HIZ_TO_PLAY | CH4_MUTE | CH3_MUTE | CH2_MUTE | CH1_MUTE |
| R/W | R/W      | R/W           | R/W         | R/W      | R/W      | R/W      | R/W      |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 20. External Control Register 5 (0x0C) Output Control Field Descriptions**

| Bit | Field         | Type | Reset | Description  |
|-----|---------------|------|-------|--|
| 7   | RST           | R/W  | 0     | Reset device   |
| 6   | Reserved      | R/W  | 0     | Reserved   |
| 5   | DC_DET_SD_DIS | R/W  | 0     | DC detect shutdown disabled, but still reports a fault |
| 4   | HIZ_TO_PLAY   | R/W  | 1     | Set non-Hi-Z channels to play mode, (unmute)           |
| 3   | CH4_MUTE      | R/W  | 1     | Set channel 4 to mute mode, non-Hi-Z                   |
| 2   | CH3_MUTE      | R/W  | 1     | Set channel 3 to mute mode, non-Hi-Z                   |
| 1   | CH2_MUTE      | R/W  | 1     | Set channel 2 to mute mode, non-Hi-Z                   |
| 0   | CH1_MUTE      | R/W  | 1     | Set channel 1 to mute mode, non-Hi-Z                   |

### 7.6.15 External Control Register 6 (0x0D) Output Control

**Figure 33. External Control Register 6 (0x0D) Output Control**

| 7        | 6       | 5       | 4      | 3      | 2      | 1      | 0   |
|----------|---------|---------|--------|--------|--------|--------|-----|
| Reserved | PBTL_34 | PBTL_12 | CH4_LL | CH3_LL | CH2_LL | CH1_LL |     |
| R/W      | R/W     | R/W     | R/W    | R/W    | R/W    | R/W    | R/W |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 21. External Control Register 6 (0x0D) Output Control Field Descriptions**

| Bit | Field    | Type | Reset | Description   |
|-----|----------|------|-------|---|
| 7-6 | Reserved | R/W  | 0     | Reserved  |
| 5   | PBTL_34  | R/W  | 0     | Connect channel 3 and channel 4 for parallel BTL mode |
| 4   | PBTL_12  | R/W  | 0     | Connect channel 1 and channel 2 for parallel BTL mode |
| 3   | CH4_LL   | R/W  | 0     | Set channel 4 to low-low state                        |
| 2   | CH3_LL   | R/W  | 0     | Set channel 3 to low-low state                        |
| 1   | CH2_LL   | R/W  | 0     | Set channel 2 to low-low state                        |
| 0   | CH1_LL   | R/W  | 0     | Set channel 1 to low-low state                        |

### 7.6.16 External Control Register 7 (0x10) Miscellaneous Selection

**Figure 34. External Control Register 7 (0x10) Miscellaneous Selection**

| 7              | 6        | 5            | 4     | 3        | 2            | 1          | 0   |
|----------------|----------|--------------|-------|----------|--------------|------------|-----|
| SLOWER_CM_RAMP | Reserved | SLOW_CM_RAMP | 4X_LD | ADD_20MS | EN_XTALK_ENH | DC_DET_VAL |     |
| R/W            | R/W      | R/W          | R/W   | R/W      | R/W          | R/W        | R/W |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 22. External Control Register 7 (0x10) Miscellaneous Selection**

| Bit | Field          | Type | Reset | Description  |
|-----|----------------|------|-------|--|
| 7   | SLOWER_CM_RAMP | R/W  | 0     | Slower common-mode (CM) ramp-down from mute mode                                     |
| 6   | Reserved       | R/W  | 0     | Reserved   |
| 5   | SLOW_CM_RAMP   | R/W  | 0     | Slow common-mode ramp, increase the default time by 3x                               |
| 4   | 4X_LD          | R/W  | 0     | Short-to-power (S2P) and short-to-ground (S2G) load-diagnostic phases take 4x longer |



**Table 22. External Control Register 7 (0x10) Miscellaneous Selection (continued)**

| Bit | Field        | Type | Reset | Description   |
|-----|--------------|------|-------|---|
| 3   | ADD_20MS     | R/W  | 0     | Adds a 20-ms delay between load diagnostic phases   |
| 2   | EN_XTALK_ENH | R/W  | 0     | Enable crosstalk enhancement  |
| 1-0 | DC_DET_VAL   | R/W  | 01    | Set DC detect value<br>01: Default DC detect value (1.6 V, Default)<br>01: Minimum DC detect value (0.8 V)<br>10: Maximum DC detect value (2.4 V) |

### 7.6.17 External Status Register 5 (0x13) Overtemperature and Thermal Foldback Status

**Figure 35. External Status Register 5 (0x13) Overtemperature and Thermal Foldback Status**

| 7                | 6                | 5                | 4                | 3           | 2           | 1           | 0           |
|------------------|------------------|------------------|------------------|-------------|-------------|-------------|-------------|
| CH4_OTSD_ST<br>T | CH3_OTSD_ST<br>T | CH2_OTSD_ST<br>T | CH1_OTSD_ST<br>T | CH4_THFB_ST | CH3_THFB_ST | CH2_THFB_ST | CH1_THFB_ST |
| R                | R                | R                | R                | R           | R           | R           | R           |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 23. External Status Register 5 (0x13) Overtemperature and Thermal Foldback Status Field Descriptions**

| Bit | Field       | Type | Reset | Description                           |
|-----|-------------|------|-------|---------------------------------------|
| 7   | CH4_OTSD_ST | R    | 0     | Channel 4 in overtemperature shutdown |
| 6   | CH3_OTSD_ST | R    | 0     | Channel 3 in overtemperature shutdown |
| 5   | CH2_OTSD_ST | R    | 0     | Channel 2 in overtemperature shutdown |
| 4   | CH1_OTSD_ST | R    | 0     | Channel 1 in overtemperature shutdown |
| 3   | CH4_THFB_ST | R    | 0     | Channel 4 in thermal foldback         |
| 2   | CH3_THFB_ST | R    | 0     | Channel 3 in thermal foldback         |
| 1   | CH2_THFB_ST | R    | 0     | Channel 2 in thermal foldback         |
| 0   | CH1_THFB_ST | R    | 0     | Channel 1 in thermal foldback         |

## 8 Application and Implementation

### NOTE

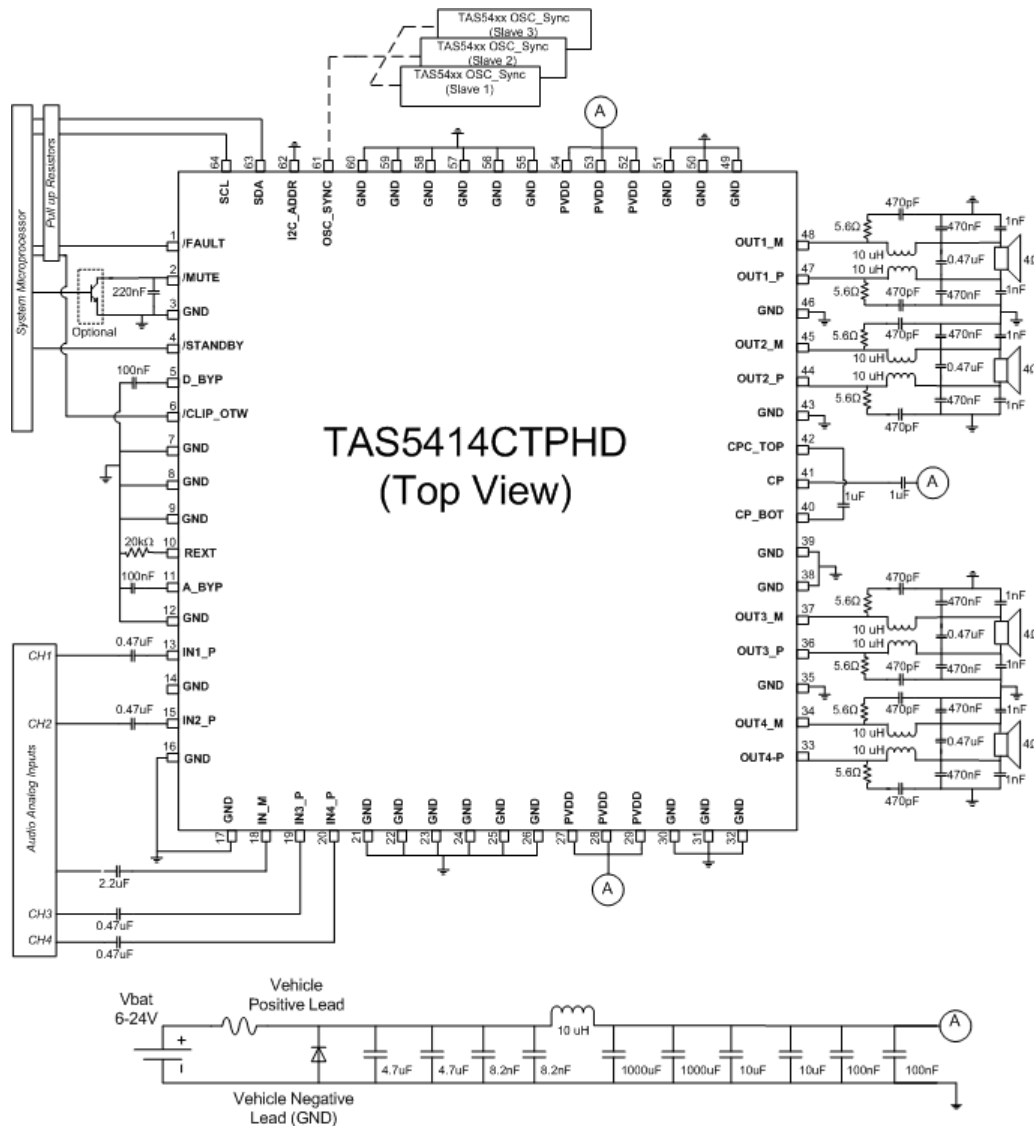
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The TAS5414C is a four-channel Class-D audio amplifier designed for use in head units and external amplifier modules. The device incorporates all the functionality needed to perform in the demanding OEM applications area.

### 8.2 Typical Application

Figure 36 shows a typical application circuit for the TAS5414C.



**Figure 36. TAS5414C Typical Application Schematic**

## Typical Application (continued)

### 8.2.1 Design Requirements

- Power Supplies  
The device needs only a single power supply compliant with the recommended operation range. The device is designed to work with either a vehicle battery or regulated boost power supply.
- Communication  
The device communicates with the system controller with both discrete hardware control pins and with I<sup>2</sup>C. The device is an I<sup>2</sup>C slave and thus requires a master. If a master I<sup>2</sup>C-compliant device is not present in the system, it is still possible to use the device, but only with the default settings. Diagnostic information is limited to the discrete reporting **FAULT** pin.
- External Components  
[Table 24](#) lists the components required for the device.

**Table 24. Supporting Components**

| EVM Designator                         | Quantity | Value                    | Size              | Description                      | Use in Application                |
|--|----------|--------------------------|-------------------|----------------------------------|-----------------------------------|
| C37, C39, C48, C52                     | 4        | 0.47 $\mu$ F $\pm$ 10%   | 1206              | Film, 16-V                       | Analog audio input filter, bypass |
| C5, C6, C7, C8                         | 4        | 330 $\mu$ F $\pm$ 20%    | 10 mm             | Low-ESR aluminum capacitor, 35-V | Power supply                      |
| C9, C10, C50, C51, C27, C28            | 6        | 1 $\mu$ F $\pm$ 10%      | 0805              | X7R ceramic capacitor, 50-V      | Power supply                      |
| C53, C55                               | 2        | 1 $\mu$ F $\pm$ 10%      | 0805              | Film, 16-V                       | Analog audio input filter, bypass |
| C14, C23, C32, C43                     | 4        | 470nF $\pm$ 10%          | 0805              | X7R ceramic capacitor, 50-V      | Amplifier output filtering        |
| C11, C15, C20, C24, C29, C34, C40, C45 | 8        | 470 pF $\pm$ 10%         | 0603              | X7R ceramic capacitor, 50-V      | Amplifier output snubbers         |
| C19, C33                               | 2        | 0.1 $\mu$ F $\pm$ 10%    | 0603              | X7R ceramic capacitor, 25-V      | Power supply                      |
| C4                                     | 1        | 2200 pF $\pm$ 10%        | 0603              | X7R ceramic capacitor, 50-V      | Power supply                      |
| C3                                     | 1        | 0.082 $\mu$ F $\pm$ 10%  | 0603              | X7R ceramic capacitor, 25-V      | Power supply                      |
| C1, C2                                 | 2        | 4.7 $\mu$ F $\pm$ 10%    | 1206              | X7R ceramic capacitor, 25-V      | Power supply                      |
| C12, C16, C21, C25, C30, C35, C41, C46 | 8        | 0.47 $\mu$ F $\pm$ 10%   | 0603              | X7R ceramic capacitor, 25-V      | Output EMI filtering              |
| C18                                    | 1        | 220nF $\pm$ 10%          | 0603              | X7R ceramic capacitor, 25-V      | Mute timing                       |
| L1                                     | 1        | 10 $\mu$ H $\pm$ 20%     | 13.5 mm x 13.5 mm | Shielded ferrite inductor        | Power supply                      |
| L2, L3, L4, L5                         | 4        | 10 $\mu$ H $\pm$ 20%     | 12 mm x 14 mm     | Dual inductor                    | Amplifier output filtering        |
| R5, R6, R7                             | 3        | 49.9 k $\Omega$ $\pm$ 1% | 0805              | Resistors, 0.125-W               | Analog audio input filter         |
| R8, R10, R12, R14, R17, R19, R26, R29  | 8        | 5.6 $\Omega$ $\pm$ 5%    | 0805              | Resistors, 0.125-W               | Output snubbers                   |
| R16                                    | 1        | 20.0 k $\Omega$ $\pm$ 1% | 0805              | Resistors, 0.125-W               | Power supply                      |

### 8.2.2 Detailed Design Procedure

#### 8.2.2.1 Hardware and Software Design

- Step 1: Hardware Schematic Design: Using the Typical Application Schematic as a guide, integrate the hardware into the system schematic.
- Step 2: Following the recommended layout guidelines, integrate the device and its supporting components into the system PCB file.
- Step 3: Thermal Design: The device has an exposed thermal pad which requires proper soldering. For more information, see the *Semiconductor and IC Package Thermal Metrics*, [SPRA953](#), and the *PowerPAD Thermally Enhanced Package*, [SLMA002G](#), application reports.
- Step 4: Develop software: The EVM User's Guide has detailed instructions for how to set up the device, interpret diagnostic information, and so forth. For information about control registers, see the [Table 7](#) section.
- For questions and support go to the [E2E forums](#).

### 8.2.2.2 Parallel Operation (PBTL)

The device can drive more current by paralleling BTL channels on the load side of the LC output filter. Parallel operation requires identical I<sup>2</sup>C settings for any two paralleled channels in order to have reliable system performance and even power dissipation on multiple channels. For smooth power up, power down, and mute operation, the same control commands (such as mute, play, Hi-Z, and so on) should be sent to the paralleled channels at the same time. The device also supports load diagnostics for parallel connection. There is no support for paralleling on the device side of the LC output filter, which can result in device failure. When paralleling channels, use the parallel BTL I<sup>2</sup>C control bits in register 0x0D. Parallel channels 1 and 2, and/or channels 3 and 4. Setting these bits allows the thermal foldback to react on both channels equally. Provide the audio input to channel 2 if paralleling channels 1 and 2, and channel 3 if paralleling channels 3 and 4.

### 8.2.2.3 Input Filter Design

For the TAS5414C device, the IN\_M pin should have an impedance to GND that is equivalent to the parallel combination of the input impedances of all IN\_P channels combined, including any source impedance from the previous stage in the system design. For example, if each of the four IN\_P channels have a 1-μF dc blocking capacitor, 1 kΩ of series resistance due to an input RC filter, and 1 kΩ of source resistance from the DAC supplying the audio signal, then the IN\_M channel should have a 4-μF capacitor in series with a 500-Ω resistor to GND ( $4 \times 1 \mu\text{F}$  in parallel = 4 μF;  $4 \times 2 \text{ k}\Omega$  in parallel = 500 Ω).

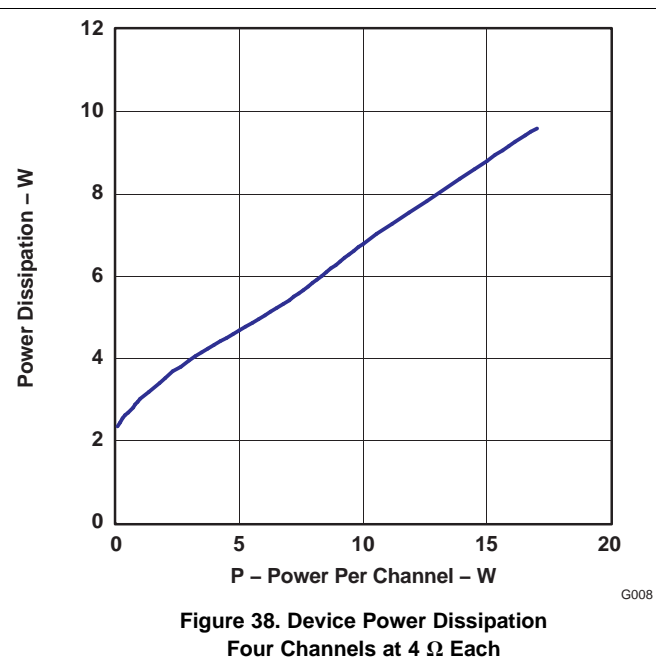
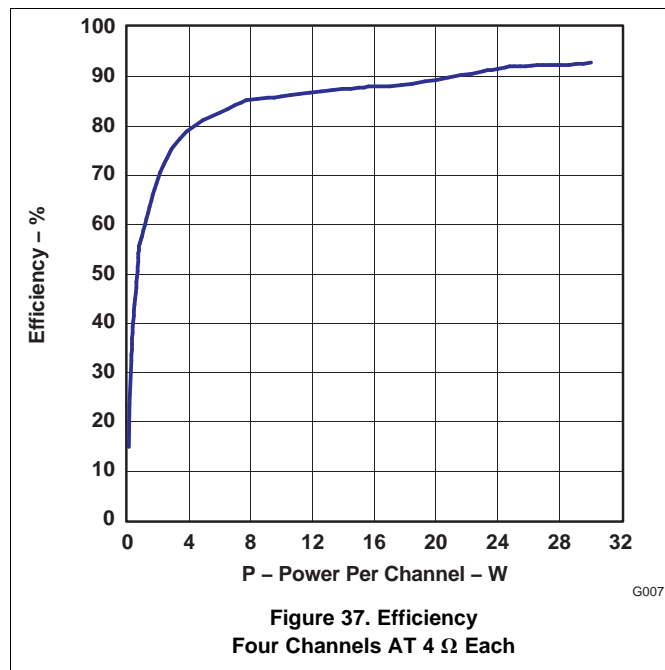
### 8.2.2.4 Amplifier Output Filtering

The output FETs drive the amplifier outputs in an H-bridge configuration. These transistors are either fully off or on. The result is a square-wave output signal with a duty cycle that is proportional to the amplitude of the audio signal. The amplifier outputs require a low-pass filter to filter out the PWM modulation carrier frequency. People frequently call this filter the L-C filter, due to the presence of an inductive element L and a capacitive element C to make up the 2-pole low-pass filter. The L-C filter attenuates the carrier frequency, reducing electromagnetic emissions and smoothing the current waveform which the load draws from the power supply. See the *Class-D LC Filter Design* application report, [SLOA119](#), for a detailed description on proper component selection and design of an L-C filter based upon the desired load and response.

### 8.2.2.5 Line Driver Applications

In many audio applications, the end user would like to use the same head unit to drive either a speaker (with several ohms of impedance) or an external amplifier (with several kilohms of impedance). The design is capable of supporting both applications; however, the one must design the output filter and system to handle the expected output load conditions.

## 8.2.3 Application Curves



## 9 Power Supply Recommendations

A car battery that can have a large voltage range most commonly provides the power for the device. PVDD is a filtered battery voltage, and it is the supply for the output FETS and the low-side FET gate driver. The supply for the high-side FET gate driver comes from a charge pump (CP). The charge pump supplies the gate-drive voltage for all four channels. AVDD, provided by an internal linear regulator powers the analog circuitry. This supply requires 0.1- $\mu$ F, 10-V external bypass capacitor at the A\_BYP pin. TI recommends not connecting any external components except the bypass capacitor to this pin. DVDD, which comes from an internal linear regulator, powers the digital circuitry. The D\_BYP pin requires a 0.1- $\mu$ F, 10-V external bypass capacitor. TI recommends not connecting any external components except the bypass capacitor to this pin.

The TAS5414C can withstand fortuitous open-ground and -power conditions. Fortuitous open ground usually occurs when a speaker wire shorts to ground, allowing for a second ground path through the body diode in the output FETs. The diagnostic capability allows debugging of the speakers and speaker wires, eliminating the need to remove the amplifier to diagnose the problem.

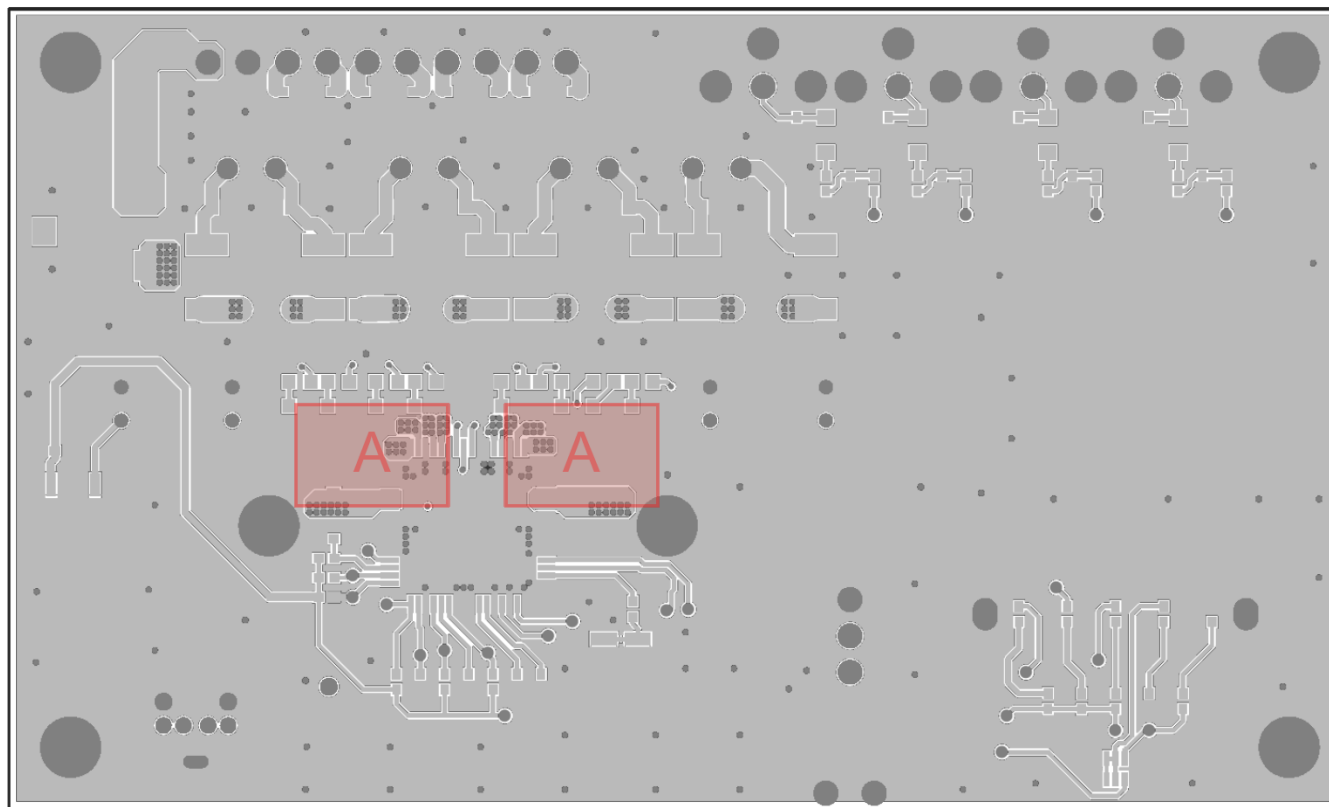
## 10 Layout

### 10.1 Layout Guidelines

- The EVM layout optimizes for low noise and EMC performance.
- The TAS5414C device has a thermal pad up, therefore a the layout must take into account an external heatsink.
- Layout also affects EMC performance.
- The EVM PCB illustrations form the basis for the layout discussions.

### 10.2 Layout Example

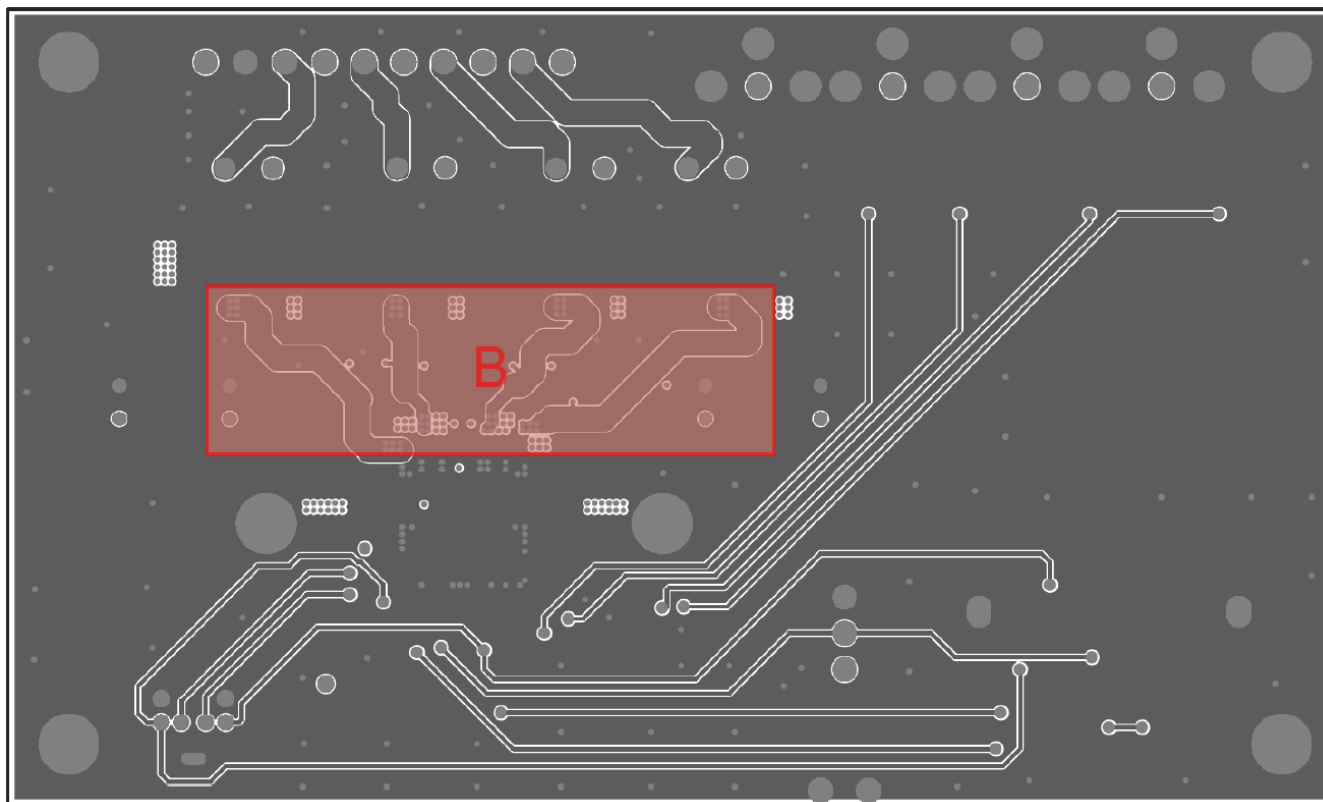
The areas indicated by the label "A", are critical to proper operation and EMC layout. The PVDD and ground decoupling capacitors should be close to the device. These decoupling capacitors must be on both groups of PVDD pins to ground. The ground connections of the snubber circuits must also be close to the grounds of the device. The grounds of the decoupling caps and the snubber circuits do not pass through vias before connecting to the device ground. This reduces the ground impedance for EMC mitigation.



**Figure 39. Top Layer**

## Layout Example (continued)

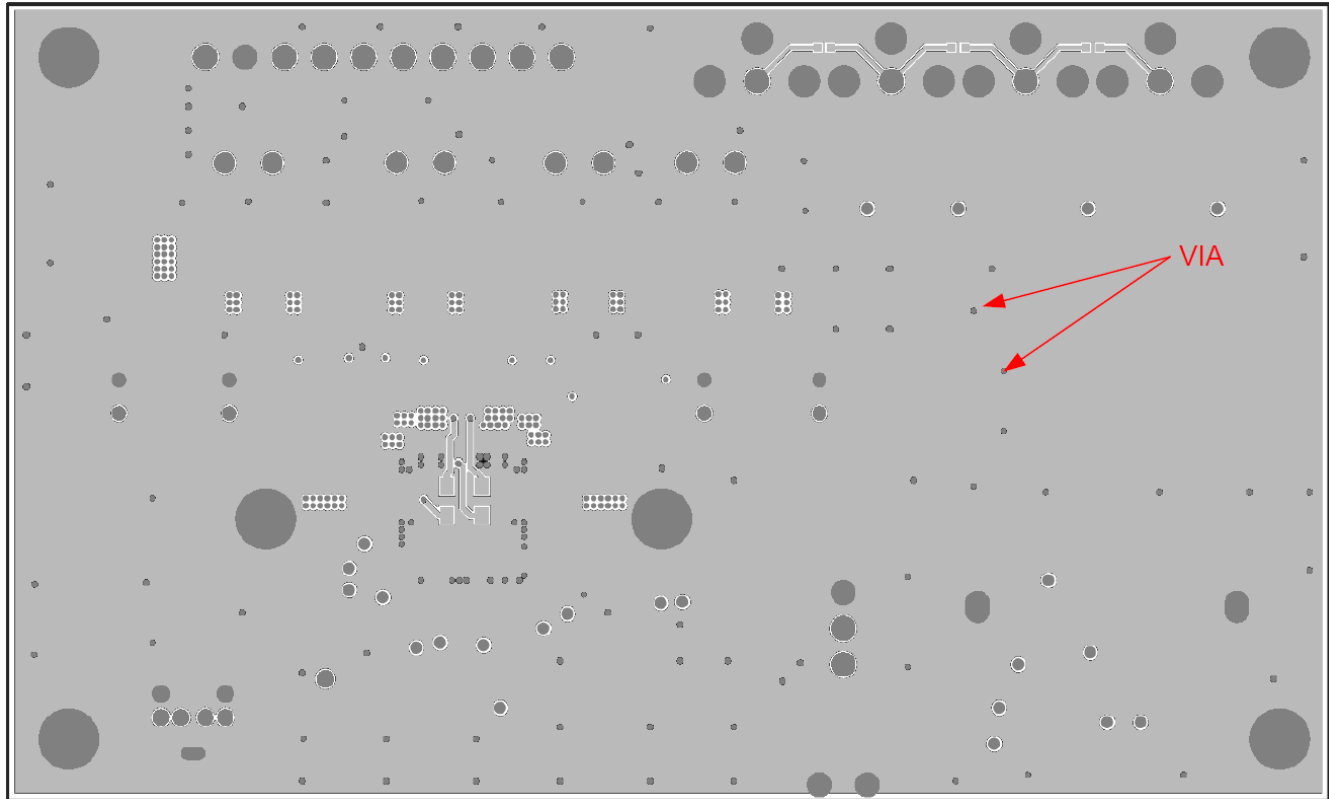
The area referenced as "B" are nets in the PCB layout that have large high frequency switching signals. These should be buried on an inner layer with ground planes on layers above and below to mitigate EMC.



**Figure 40. A Mid Layer**

## Layout Example (continued)

The bottom layer in the EVM is almost all ground plane. It can be seen that the other layers have ground planes that fill unused areas. All these ground planes need to be connected together through many vias to reduce the impedance between the ground layers. This allows for reduced EMI.



**Figure 41. Bottom Layer**



### 10.3 Thermal Consideration

The design of the thermally augmented package is for interface directly to heat sinks using a thermal interface compound (for example, Arctic Silver, Ceramique thermal compound). The heat sink then absorbs heat from the ICs and couples it to the local air. With proper thermal management this process can reach equilibrium at a lower temperature and heat can be continually removed from the ICs. Because of the device efficiency, heat sinks can be smaller than those required for linear amplifiers of equivalent performance.

$R_{0JA}$  is a system thermal resistance from junction to ambient air. As such, it is a system parameter with the following components:

- $R_{\theta JC}$  (the thermal resistance from junction to case, or in this case the heat slug)
- Thermal resistance of the thermal grease
- Thermal resistance of the heat sink

One can calculate the thermal resistance of the thermal grease from the exposed heat slug area and the manufacturer's value for the area thermal resistance of the thermal grease (expressed in  $^{\circ}\text{C}\text{-in}^2/\text{W}$  or  $^{\circ}\text{C}\text{-mm}^2/\text{W}$ ). The area thermal resistance of the example thermal grease with a 0.001-inch (0.0254-mm) thick layer is about  $0.007^{\circ}\text{C}\text{-in}^2/\text{W}$  ( $4.52^{\circ}\text{C}\text{-mm}^2/\text{W}$ ). The approximate exposed heat slug size is as follows:

64-pin QFP 0.099 in<sup>2</sup> (64 mm<sup>2</sup>)

Dividing the example area thermal resistance of the thermal grease by the area of the heat slug gives the actual resistance through the thermal grease:

64-pin QFP 0.07°C/W

The thermal resistance of thermal pads is generally considerably higher than a thin thermal-grease layer. Thermal tape has an even higher thermal resistance and should not be used at all. The heat-sink vendor generally predicts heat sink thermal resistance, either modeled using a continuous-flow dynamics (CFD) model, or measured.

Thus, for a single monaural channel in the IC, the system  $R_{0JA} = R_{0JC} + \text{thermal-grease resistance} + \text{heat-sink resistance}$ .

Table 25 indicates modeled parameters for one device on a heat sink. The junction temperature setting is at 115°C while delivering 20 watts per channel into 4-Ω loads with no clipping. The assumed thickness of the thermal grease is about 0.001 inches (0.0254 mm).

### Table 25. QFP Package Modeled Parameters

| DEVICE                               | 64-PIN QFP |
|--------------------------------------|------------|
| Ambient temperature                  | 25°C       |
| Power to load                        | 20 W × 4   |
| Power dissipation                    | 1.9 W × 4  |
| ΔT inside package                    | 7.6°C      |
| ΔT through thermal grease            | 0.46°C     |
| Required heatsink thermal resistance | 10.78°C/W  |
| Junction temperature                 | 115°C      |
| System R <sub>θJA</sub>              | 11.85°C/W  |
| R <sub>θJA</sub> × power dissipation | 90°C       |

## 10.4 Electrical Connection of Heat Slug and Heat Sink

Electrically connect the heat sink attached to the heat slug of the device to GND, or leave it floating. Do not connect the heat slug to any other electrical node.

## 10.5 EMI Considerations

EMI performance depends on both careful integrated circuit design and good system-level design. Controlling sources of electromagnetic interference (EMI) was a major consideration in all aspects of the design.

**EMI Considerations (continued)**

The design has minimal parasitic inductances due to the short leads on the package. This dramatically reduces the EMI that results from current passing from the die to the system PCB. Each channel also operates at a different phase. The phase between channels is I<sup>2</sup>C selectable to either 45° or 180°, to reduce EMI caused by high-current switching. The design also incorporates circuitry that optimizes output transitions that cause EMI.

## 11 デバイスおよびドキュメントのサポート

### 11.1 デバイス・サポート

#### 11.1.1 開発サポート

#### 11.1.2 デバイスの項目表記

### 11.2 ドキュメントのサポート

#### 11.2.1 関連資料

### 11.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

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### 11.6 用語集

**SLYZ022** — *TI用語集*.

この用語集には、用語や略語の一覧および定義が記載されています。

## 12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

## PACKAGING INFORMATION

| Orderable part number         | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier  | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-------------------------------|---------------|----------------------|------------------|------------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">TAS5414CTPHD</a>  | Active        | Production           | HTQFP (PHD)   64 | 90   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 105   | TAS5414C            |
| TAS5414CTPHD.B                | Active        | Production           | HTQFP (PHD)   64 | 90   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 105   | TAS5414C            |
| <a href="#">TAS5414CTPHDR</a> | Active        | Production           | HTQFP (PHD)   64 | 1000   LARGE T&R       | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 105   | TAS5414C            |
| TAS5414CTPHDR.B               | Active        | Production           | HTQFP (PHD)   64 | 1000   LARGE T&R       | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 105   | TAS5414C            |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF TAS5414C :**

- Automotive : [TAS5414C-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## GENERIC PACKAGE VIEW

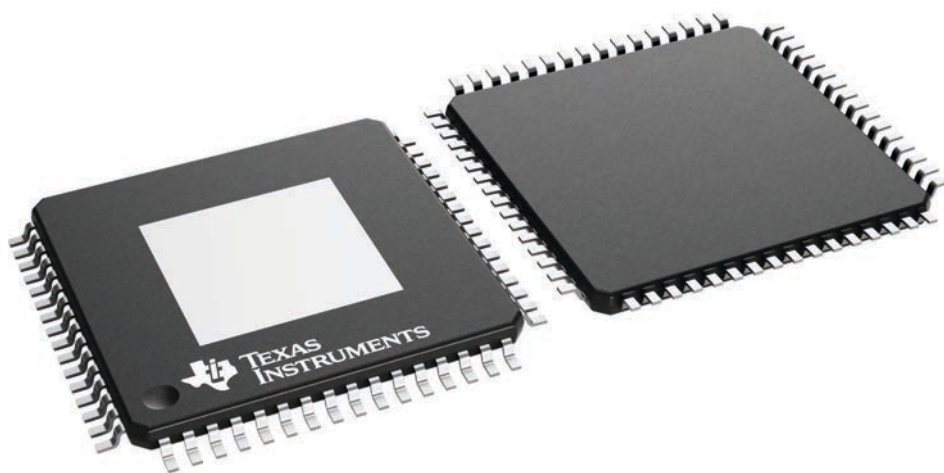
**PHD 64**

**HTQFP - 1.2 mm max height**

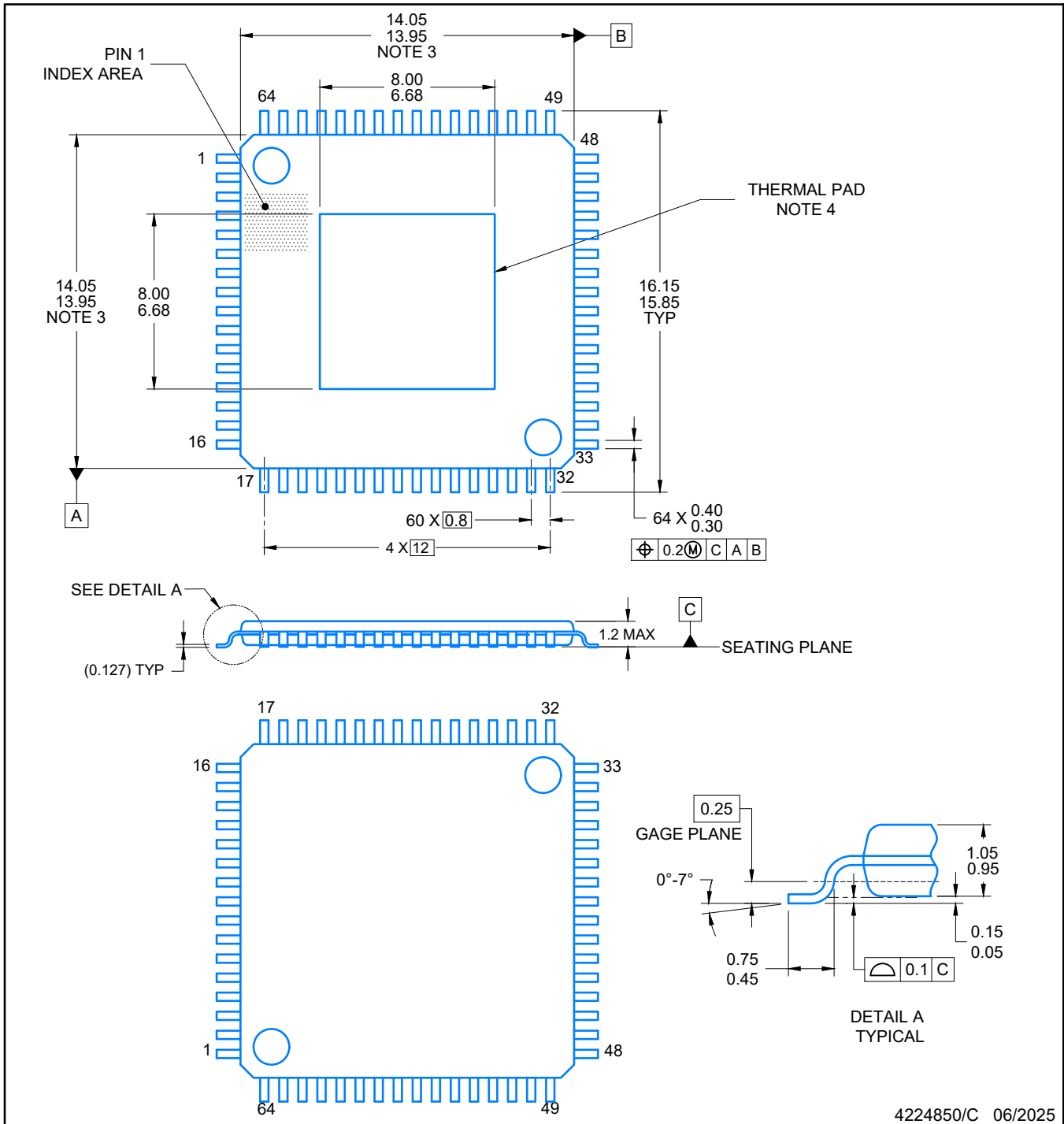
14 x 14, 0.8 mm pitch

PLASTIC QUAD FLATPACK

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224851/B

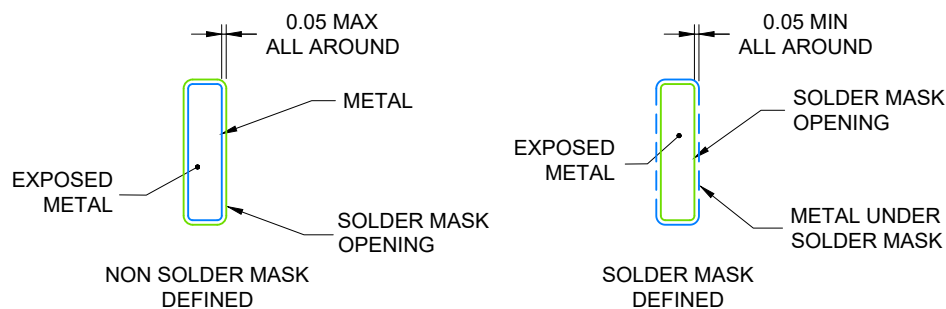
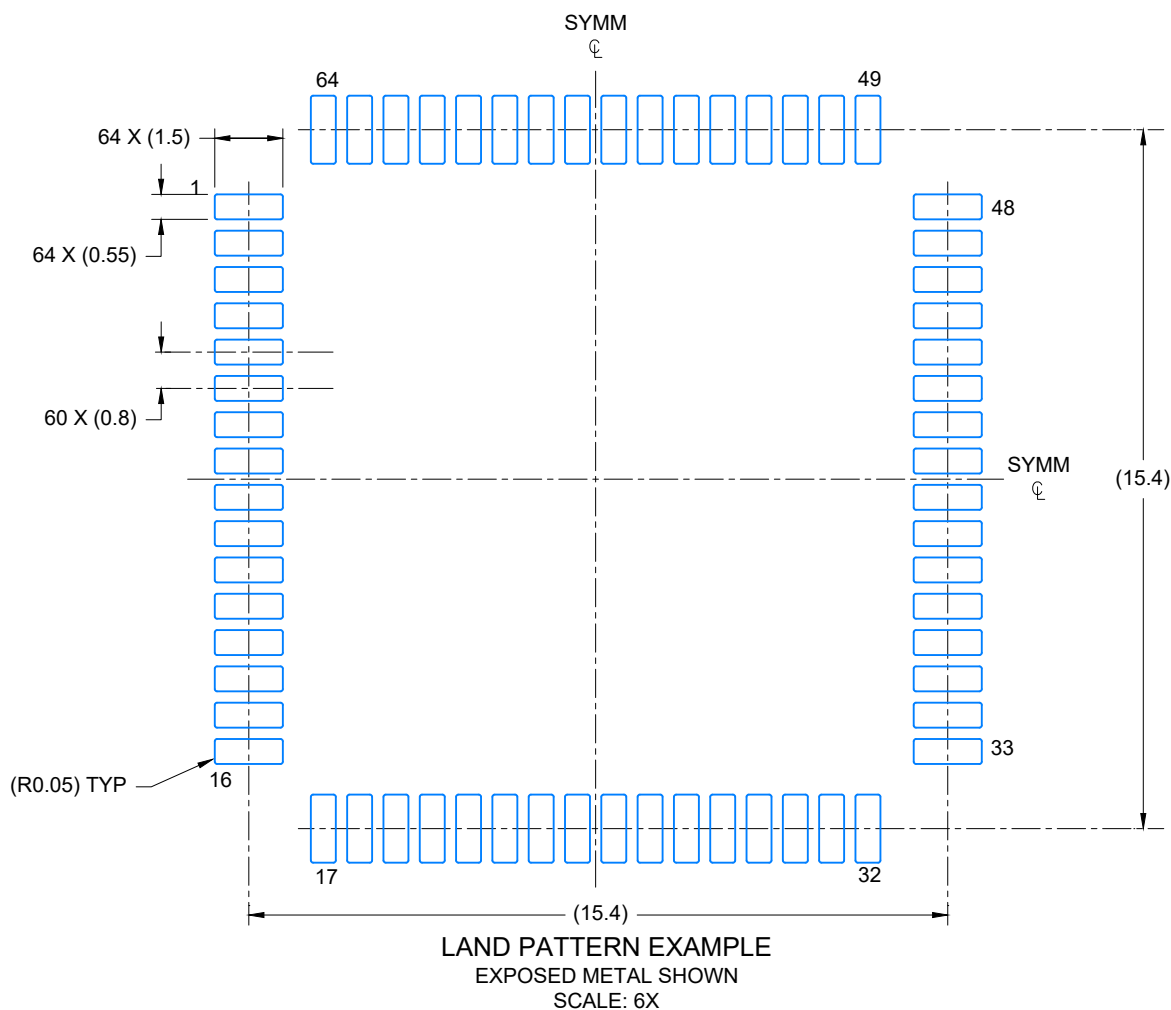


4224850/C 06/2025

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. See technical brief. PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)) for information regarding recommended board layout.

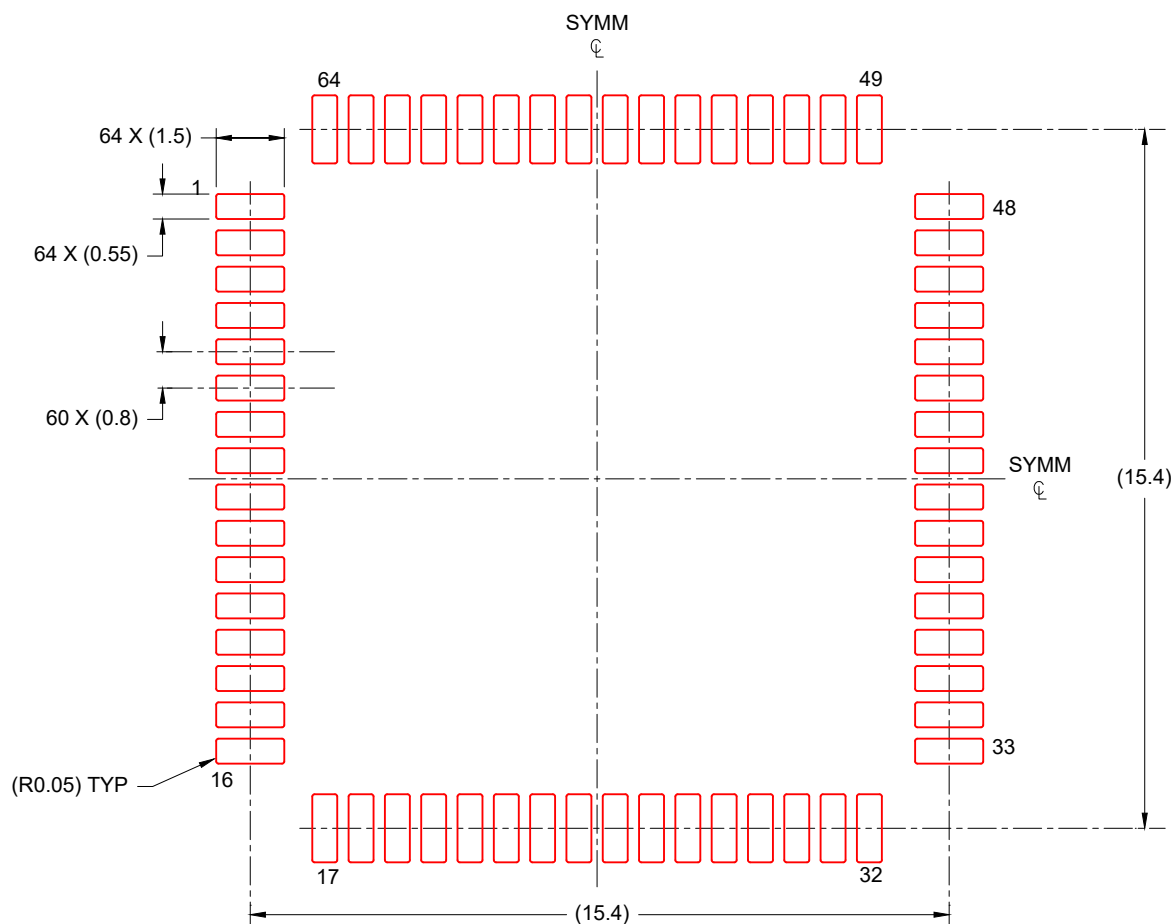




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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE  
 BASED ON 0.125 mm THICK STENCIL  
 SCALE: 6X

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## NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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