

# TDP158 6Gbps、AC カップリングから TMDS™ または HDMI™ へのレベルシフタリドライバ

## 1 特長

- AC 結合 TMDS または DisplayPort™ デュアルモード物理層入力から HDMI 2.0b TMDS 物理層出力へ、最高 6Gbps のデータレートをサポート、HDMI 2.0b の電氣的パラメータに適合
- DisplayPort デュアルモード規格バージョン 1.1 をサポート
- 4k 2k 60p および最大 WUXGA 16 ビット色深度、または高リフレッシュレート 1080p をサポート
- 固定レシーバ イコライザを最高 15.5dB にプログラム可能
- グローバルまたは独立の高速レーン制御、プリエンフィシスと送信スイング、スルーレート制御
- I<sup>2</sup>C またはピンストラップによりプログラム可能
- I<sup>2</sup>C により DisplayPort リドライバとして構成可能
- メインレーンのフルレーンスワップ
- 低消費電力
  - アクティブ時 6Gbps で -200mW、シャットダウン状態で -8mW
- 40 ピン、0.4mm ピッチ、5mm × 5mm、WQFN パッケージ、SN75DP159RSB リタイマとピン互換

## 2 アプリケーション

- ノートブック、デスクトップ、オールインワン、タブレット、ゲーム用および産業用 PC
- オーディオまたはビデオ機器
- Blu-ray™ DVD
- ゲーム機
- HDMI アダプタまたはドングル
- ドッキングステーション

## 3 概要

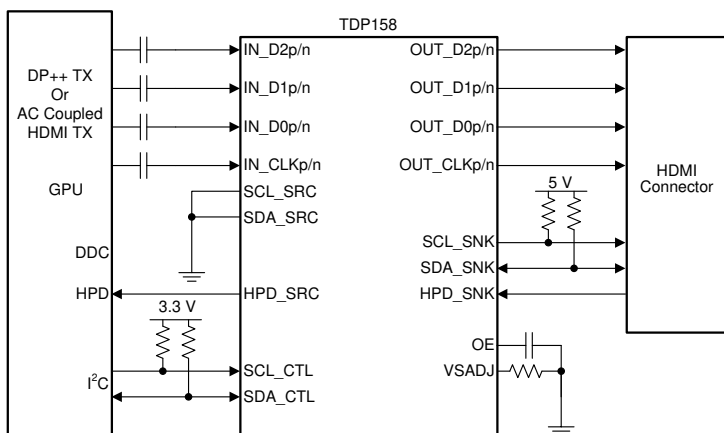
TDP158 デバイスは、AC カップリングされた HDMI 信号から、遷移が最小化された差動信号 (TMDS) へのリドライバであり、デジタルビデオ インターフェイス (DVI) 1.0 および高解像度マルチメディア インターフェイス (HDMI) 1.4b および 2.0b の出力信号をサポートしています。TDP158 は、4 つの TMDS チャンネルと、デジタルディスプレイ制御 (DDC) インターフェイスをサポートします。TDP158 は、最大 6Gbps の信号速度に対応し、最高解像度 4k 2k 60p 24 ビットピクセル および最大 WUXGA 16 ビット色深度、または高リフレッシュレートの 1080p に使用できます。TDP158 は、HDMI2.0 規格をサポートするように構成可能です。

TDP158 は、V<sub>DD</sub> で 1.1V、V<sub>CC</sub> で 3.3V のデュアル電源レールをサポートしているため、消費電力を削減できます。全体的な消費電力を低減するために、いくつかの電力管理手法が組み込まれています。TDP158 は、I<sup>2</sup>C またはピンストラップを使用して固定レシーバ EQ ゲインをサポートし、入力ケーブルや基板のトレース長の相違を補償できます。

### パッケージ情報

部品番号	パッケージ <sup>(1)</sup>	パッケージサイズ <sup>(2)</sup>
TDP158	RSB (WQFN, 40)	5mm × 5mm

- 詳細については、[セクション 11](#) を参照してください。
- パッケージサイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



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概略回路図



ディスプレイ



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## 4 Pin Configuration and Functions

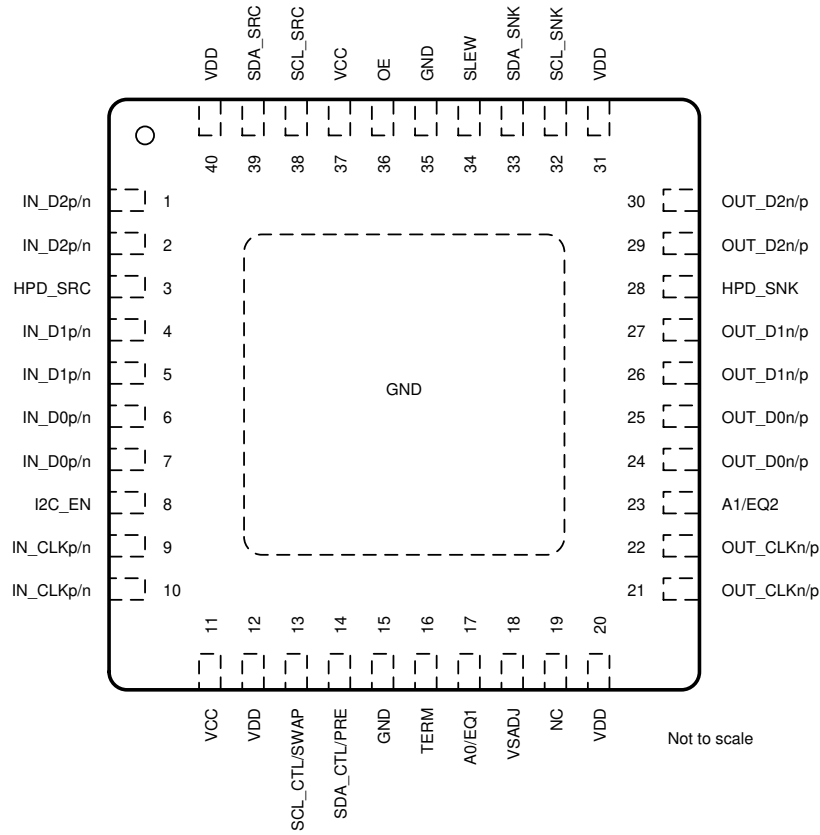


図 4-1. RSB Package, 40-Pin WQFN (Top View)

表 4-1. Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
<b>SUPPLY AND GROUND PINS</b>			
VCC	11, 37	P	3.3V Power Supply
VDD	12,20,31,40	P	1.1V Power Supply
GND	15, 35 Thermal Pad	G	Ground
<b>MAIN LINK INPUT PINS</b>			
IN_D2p/n	1, 2	I	Channel 2 Differential Input
IN_D1p/n	4, 5	I	Channel 1 Differential Input
IN_D0p/n	6, 7	I	Channel 0 Differential Input
IN_CLKp/n	9, 10	I	Clock Differential Input
<b>MAIN LINK OUTPUT PINS (FAIL SAFE)</b>			
OUT_D2n/p	29, 30	O	TMDS Data 2 Differential Output
OUT_D1n/p	26, 27	O	TMDS Data 1 Differential Output
OUT_D0n/p	24, 25	O	TMDS Data 0 Differential Output
OUT_CLKn/p	21, 22	O	TMDS Data Clock Differential Output

表 4-1. Pin Functions (続き)

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
<b>HOT PLUG DETECT AND DDC PINS</b>			
HPD_SRC	3	O	Hot Plug Detect Output to source side
HPD_SNK	28	I	Hot Plug Detect Input from sink side
SDA_SNK	33	I/O	Sink Side Bidirectional DDC Data Line
SCL_SNK	32	I/O	Sink Side Bidirectional DDC Clock Line
SDA_SRC	39	I/O	Source Side Bidirectional DDC Data Line
SCL_SRC	38	I/O	Source Side Bidirectional DDC Clock Line
<b>CONTROL PINS</b>			
OE	36	I	Operation Enable/Reset Pin OE = L: Power Down Mode OE = H: Normal Operation Internal weak pullup: Resets device when transitions from H to L
I2C_EN	8	I	I2C_EN = High; Puts Device into I2C Control Mode I2C_EN = Low; Puts Device into Pin Strap Mode
SDA_CTL/PRE	14	I/O	I2C Data Signal: When I2C_EN = High; Pre-emphasis: When I2C_EN = Low: See <a href="#">セクション 7.3.11</a> DE = L: None 0dB DE = H: 3.5dB
SCL_CTL/SWAP	13	I	I2C Clock Signal: When I2C_EN = High; Lane SWAP: When I2C_EN = Low: See <a href="#">セクション 7.3.4</a> HDMI Mode Only SWAP = L: Normal Operation SWAP = H: Lane Swap
VSADJ	18	I	TMDS Compliant Voltage Swing Control (Nominal 6 kΩ for HDMI and DP combination; 6.49 kΩ for HDMI only)
A0/EQ1	17	I 3 Level	Address Bit 1 for I2C Programming when I2C_EN = High EQ1 Pin Setting when I2C_EN = Low; Works in conjunction with A1/EQ2; See <a href="#">セクション 7.3.5</a> for settings. For pin control, Low = 1kΩ pulldown resistor to GND, High = 1kΩ pullup resistor to VCC, NC = Floating.
A1/EQ2	23	I 3 Level	Address Bit 2 for I2C Programming when I2C_EN = High EQ2 Pin Setting when I2C_EN = Low; Works in conjunction with A0/EQ1; See <a href="#">セクション 7.3.5</a> for settings. For pin control, Low = 1kΩ pulldown resistor to GND, High = 1kΩ pullup resistor to VCC, NC = Floating.
SLEW	34	I 3 Level	Clock Slew Rate Control: See <a href="#">セクション 7.3.10</a> SLEW = L: Slowest $\approx$ 203ps SLEW = NC (Default): Mid-range 1 $\approx$ 180ps SLEW = H: Fastest $\approx$ 122ps For pin control, L = 1kΩ pulldown resistor to GND, H = 1kΩ pullup resistor to VCC, NC = Floating.
TERM	16	I 3 Level	Source Termination Control: See <a href="#">セクション 7.3.8</a> TERM = H, 75Ω $\approx$ 150Ω TERM = L, Transmit Termination impedance in 150Ω $\approx$ 300Ω TERM = NC, No transmit Termination Note: When TMDS_CLOCK_RATIO_STATUS bit = 1 the TDP158 sets source termination to 75Ω $\approx$ 150Ω Automatically For pin control, L = 1kΩ pulldown resistor to GND, H = 1kΩ pullup resistor to VCC, NC = Floating.
NC	19	NA	No Connect. Optionally connect 0.1μF to GND to reduce noise.

(1) I = Input, O = Output, P = Power, G = Ground

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

		MIN	MAX	UNIT
Supply Voltage Range <sup>(3)</sup>	VCC	-0.3	4	V
	VDD	-0.3	1.4	V
Voltage Range	Main Link Input Differential Voltage (IN_Dx)	0	1.56	V
	Main Link Input Single Ended on Pin	-0.3	1.4	V
	TMDS Output ( OUT_Dx)	-0.3	4	V
	HPD_SRC, VSADJ, SDA_CTL/PRE, OE, A1/EQ2, A0/EQ1, TERM, I2C_EN, SLEW, SCL_CTL/SWAP, SDA_SRC, SCL_SRC	-0.3	4	V
	HDP_SNK, SDA_SNK, SCL_SNK	-0.3	6	V
Continuous power dissipation	See <a href="#">セクション 5.4</a>			
Storage temperature, T <sub>stg</sub>	-65	150	°C	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to network ground terminal.
- (3) Tested in accordance with JEDEC Standard 22, Test Method A114-B.

### 5.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply Voltage Nominal Value 3.3V for DP mode	3		3.6	V
	Supply Voltage Nominal Value 3.3V for HDMI mode	3.13		3.47	V
V <sub>DD</sub>	Supply Voltage Nominal Value 1.1V	1		1.27	V
T <sub>J</sub>	Junction temperature	0		105	°C
T <sub>A</sub>	Operating free-air temperature (TDP158)	0		85	°C
<b>MAIN LINK DIFFERENTIAL PINS</b>					
V <sub>ID(EYE)</sub>	Peak-to-peak input differential voltage See <a href="#">図 6-14</a>	75		1200	mV
V <sub>ID(DC)</sub>	The input differential voltage Peak-to peak DC level, See <a href="#">図 6-14</a>	200		1200	mV
V <sub>IC</sub>	Input Common Mode Voltage (Internally Biased)	0.5		0.9	V
d <sub>R</sub>	Data rate	0.25		6	Gbps
V <sub>SADJ</sub>	TMDS compliant swing voltage bias resistor (Nominal 6kΩ for HDMI and DP combination; 6.49kΩ for HDMI only) <sup>(1)</sup>	4.5		8	kΩ
<b>DDC, I2C, HPD, AND CONTROL PINS</b>					
V <sub>I(DC)</sub> DC Input Voltage	HDP_SNK, SDA_SNK, SCL_SNK,	-0.3		5.5	V
	SDA_SRC, SCL_SRC; All other Local I2C, and control pins	-0.3		3.6	V

### 5.3 Recommended Operating Conditions (続き)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>IL</sub>	Low-level input voltage at DDC			0.3 x V <sub>CC</sub>	V
	Low-level input voltage at HPD			0.8	V
	Low-level input voltage at SDA_CTL/PRE, OE, A1/EQ2, A0/EQ1, TERM, I2C_EN, SLEW, SCL_CTL/SWAP pins only			0.3	V
V <sub>IM</sub>	Mid-Level input voltage at A1/EQ2, A0/EQ1, TERM, SLEW pins only	1.2		1.6	V
V <sub>IH</sub>	High-level input voltage at OE, A1/EQ2, A0/EQ1, TERM, I2C_EN, SLEW pins only	0.7 x V <sub>CC</sub>			V
	High-level input voltage at SDA_SRC, SCL_SRC, SDA_CTL/PRE, SCL_CTL/SWAP	0.7 x V <sub>CC</sub>			V
	High-level input voltage at SDA_SNK, SCL_SNK	3.2			V
	High-level input voltage at HPD	2			V
V <sub>OL</sub>	Low-level output voltage			0.4	V
V <sub>OH</sub>	High-level output voltage	2.4			V
f <sub>SCL</sub>	SCL clock frequency fast I <sup>2</sup> C mode for local I2C control			400	kHz
C <sub>(bus,DDC)</sub>	Total capacitive load for each bus line supporting 400kHz (DDC terminals)			400	pF
C <sub>(bus,I2C)</sub>	Total capacitive load for each bus line (local I2C terminals)			100	pF
d <sub>R(DDC)</sub>	DDC Data rate			400	Kbps
I <sub>IH</sub>	High level input current	-30		30	μA
I <sub>IM</sub>	Mid level input current	-20		20	μA
I <sub>IL</sub>	Low level input current	-10		10	μA
I <sub>OZ</sub>	High impedance output current			10	μA
R <sub>(OEP)</sub>	Pull up resistance on OE pin	150		250	kΩ

(1) Reducing resistor in V<sub>SADJ</sub> will increase V<sub>OD</sub>, care should be taking since resistors below ≈6kΩ may lead to compliance failures.

### 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TDP158	UNIT
		RSB (WQFN)	
		40 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	3.7	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	23.1	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	9.9	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.3	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	3.8	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	3.2	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.5 Electrical Characteristics, Power Supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX <sup>(1)</sup>	UNIT
P <sub>DD1</sub>	Device power Dissipation	OE = H, V <sub>CC</sub> = 3.3V/3.6V, V <sub>DD</sub> = 1.1V/1.27V IN_Dx: VID_PP = 1200mV, 6Gbps TMDS pattern, V <sub>I</sub> = 3.3V, I <sub>2C_EN</sub> = L, SDA_CTL/PRE = L, EQ1/EQ2 = H		200	350	mW
P <sub>DD2</sub>	Device power Dissipation in DP- Mode	OE = H, V <sub>CC</sub> = 3.3V/3.6V, V <sub>DD</sub> = 1.1V/1.27V IN_Dx: VID_PP = 400mV, 5.4Gbps DP pattern, I <sub>2C_EN</sub> = H, V <sub>OD</sub> = 400mV PRE = 0dB		330	680	mW
P <sub>(STBY1)</sub>	Stage 1: Standby Power	OE = H, V <sub>CC</sub> = 3.3V/3.6V, V <sub>DD</sub> = 1.1V/ 1.27V, HPD = H, No input Signal: Stage 1 See <a href="#">セクション 8.3.2</a>			34	mW
	Stage 2: Standby Power	OE = H, V <sub>CC</sub> = 3.3V/3.6V, V <sub>DD</sub> = 1.1V/ 1.27V, HPD = H, Noise on input Signal: Stage 2 See <a href="#">セクション 8.3.2</a>			60	mW
P <sub>(SD1)</sub>	Device power in PowerDown	OE = L, V <sub>CC</sub> = 3.3V/3.6V, V <sub>DD</sub> = 1.1V/1.27V		8	34	mW
P <sub>(SD2)</sub>	Device power in PowerDown in DP- Mode	OE = L, V <sub>CC</sub> = 3.3V/3.6V, V <sub>DD</sub> = 1.1V/1.27V		8	34	mW
I <sub>CC1</sub>	V <sub>CC</sub> Supply current	OE = H, V <sub>CC</sub> = 3.3V/3.6V, V <sub>DD</sub> = 1.1V/1.27V IN_Dx: VID_PP = 1200mV, 6Gbps TMDS pattern I <sub>2C_EN</sub> = L, SDA_CTL/PRE = L, EQ1/EQ2 = H,		8	20	mA
I <sub>CC2</sub>	V <sub>CC</sub> Supply current in DP-Mode	OE = H, V <sub>CC</sub> = 3.3V/3.6V, V <sub>DD</sub> = 1.1V/1.27V IN_Dx: VID_PP = 400mV, 5.4Gbps DP pattern, I <sub>2C_EN</sub> = H, V <sub>OD</sub> = 400mV PRE = 0dB		45	110	mA
I <sub>DD1</sub>	V <sub>DD</sub> Supply current	OE = H, V <sub>CC</sub> = 3.3V/3.6V, V <sub>DD</sub> = 1.1V/1.27V IN_Dx: VID_PP = 1200mV, 6Gbps TMDS pattern I <sub>2C_EN</sub> = L, SDA_CTL/PRE = L, EQ1/EQ2 = H		160	220	mA
I <sub>DD2</sub>	V <sub>DD</sub> Supply current DP-Mode	OE = H, V <sub>CC</sub> = 3.3V/3.6V, V <sub>DD</sub> = 1.1V/1.27V IN_Dx: VID_PP = 400mV, 5.4Gbps DP pattern, I <sub>2C_EN</sub> = H, V <sub>OD</sub> = 40mV PRE =dB		160	220	mA
I <sub>(STBY1)</sub>	Stage 1: Standby current See <a href="#">セクシ ョン 8.3.2</a>	OE = H, V <sub>CC</sub> = 3.3V/3.6V, V <sub>DD</sub> = 1.1V/1.27V, HPD = H: No signal on IN_CLK	3.3V Rail		7	mA
			1.1V Rail		7	mA
	Stage 2: Standby current See <a href="#">セクシ ョン 8.3.2</a>	OE = H, V <sub>CC</sub> = 3.3V/3.6V, V <sub>DD</sub> = 1.1V/1.27V, HPD = H: No valid signal on IN_CLK	3.3V Rail		7	mA
			1.1V Rail		27	mA
I <sub>(SD11)</sub>	PowerDown current – HDMI Mode	OE = L, V <sub>CC</sub> = 3.3V/3.6V, V <sub>DD</sub> = 1.1V/1.27V, or OE = H, HPD = L	3.3V Rail	1	7	mA
			1.1V Rail	4	7	mA
I <sub>(SD2)</sub>	PowerDown current in DP-Mode	OE = L, V <sub>CC</sub> = 3.3V/3.6V, V <sub>DD</sub> = 1.1V/1.27V	3.3V Rail	1	7	mA
			1.1V Rail	4	7	mA

(1) The maximum rating is simulated at 3.6V V<sub>CC</sub> and 1.27V V<sub>DD</sub> and at 85°C temperature unless otherwise noted.

(2) The typical rating is simulated at 3.3V V<sub>CC</sub> and 1.1V V<sub>DD</sub> and at 27°C temperature unless otherwise noted.

## 5.6 Electrical Characteristics, Differential Input

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX <sup>(1)</sup>	UNIT
$D_{R(RX\_DATA)}$	TMDS data lanes data rate		0.25		6	Gbps
$D_{R(RX\_CLK)}$	TMDS clock lanes clock rate		25		340	MHz
$t_{RX\_DUTY}$	Input clock duty circle		40%	50%	60%	
$R_{(INT)}$	Input differential termination impedance		80	100	120	$\Omega$
$V_{(TERM)}$	Input Common Mode Voltage	OE = H		0.7		V

(1) The maximum rating is simulated at 3.6V  $V_{CC}$  and 1.27V  $V_{DD}$  and at 85°C temperature unless otherwise noted.

(2) The typical rating is simulated at 3.3V  $V_{CC}$  and 1.1V  $V_{DD}$  and at 27°C temperature unless otherwise noted.

## 5.7 Electrical Characteristics, TMDS Differential Output

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX <sup>(1)</sup>	UNIT
$V_{OD(PP)}$	Output differential voltage before pre-emphasis; See セクション 7.3.11	$V_{SADJ} = 6k\Omega$ ; SDA_CTL/PRE = H; See 図 6-4	600		1400	mV
$V_{OD(SS)}$	Steady state output differential voltage See セクション 7.3.11	$V_{SADJ} = 6k\Omega$ ; SDA_CTL/PRE = H, See 図 6-4	350		720	mV
		$V_{SADJ} = 5.5k\Omega$ ; SDA_CTL/PRE = L, See 図 6-3	350		1000	mV
$I_{OS}$	Short circuit current limit	Main link output shorted to GND			50	mA
$R_{(TERM)}$	Source Termination resistance for HDMI 2.0		75		150	$\Omega$

## 5.8 Electrical Characteristics, DDC, I2C, HPD, and ARC

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX <sup>(1)</sup>	UNIT
<b>DDC and I2C</b>						
$V_{IL}$	SCL/SDA_CTL, SCL/SDA_SRC low level input voltage				$0.3 \times V_{CC}$	V
$V_{IH}$	SCL/SDA_CTL, input voltage		$0.7 \times V_{CC}$		$V_{CC} + 0.5$	V
$V_{OL}$	SCL/SDA_CTL, SCL/SDA_SRC low level output voltage	$I_O = 3mA$ and $V_{CC} > 2V$			0.4	V
		$I_O = 3mA$ and $V_{CC} > 2V$			$0.2 \times V_{CC}$	V
<b>HPD</b>						
$V_{IH}$	High-level input voltage	HPD_SNK	2.1			V
$V_{IL}$	Low-level input voltage	HPD_SNK			0.8	V
$V_{OH}$	High-level output voltage	$I_{OH} = -500\mu A$ ; HPD_SRC,	2.4		3.6	V
$V_{OL}$	Low-level output voltage	$I_{OL} = 500\mu A$ ; HPD_SRC,	0		0.4	V
$I_{LKG}$	Failsafe condition leakage current	$V_{CC} = 0V$ ; $V_{DD} = 0V$ ; HPD_SNK = 5V;			40	$\mu A$
$I_{H(HPD)}$	High level input current	Device powered; $V_{IH} = 5V$ ; $I_{H(HPD)}$ includes $R_{(pdHPD)}$ resistor current			40	$\mu A$
		Device powered; $V_{IL} = 0.8V$ ; $I_{L(HPD)}$ includes $R_{(pdHPD)}$ resistor current			30	$\mu A$
$R_{(pdHPD)}$	HPD input termination to GND	$V_{CC} = 0V$	150	190	220	k $\Omega$

(1) The maximum rating is simulated at 3.6V  $V_{CC}$  and 1.27V  $V_{DD}$  and at 85°C temperature unless otherwise noted.

(2) The typical rating is simulated at 3.3V  $V_{CC}$  and 1.1V  $V_{DD}$  and at 27°C temperature unless otherwise noted.

## 5.9 Electrical Characteristics, TMDS Differential Output in DP-Mode

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX <sup>(1)</sup>	UNIT
$V_{(TX\_DIFFPP\_LVL0)}$	Differential peak-to-peak output voltage level 0	Based on default state of V0_P0_VOD register		415		V
$V_{(TX\_DIFFPP\_LVL1)}$	Differential peak-to-peak output voltage level 1	Based on default state of V1_P0_VOD register		660		V
$V_{(TX\_DIFFPP\_LVL2)}$	Differential peak-to-peak output voltage level 2	Based on default state of V2_P0_VOD register		880		V
$\Delta V_{OD(L0L1)}$	Output peak-to-peak differential voltage delta	$\Delta V_{ODn} = 20 \times \log(V_{ODL(n+1)} / V_{ODL(n)})$ measured in compliance with latest PHY CTS 1.2	1		6	dB
$\Delta V_{OD(L1L2)}$			1		5	dB
$V_{(TX\_PRE\_RATIO\_0)}$	Pre-emphasis level 0	RBR, HBR and HBR2		0		dB
$V_{(TX\_PRE\_RATIO\_1)}$	Pre-emphasis level 1	RBR, HBR and HBR2	2		4.2	dB
$V_{(TX\_PRE\_RATIO\_2)}$	Pre-emphasis level 2	RBR, HBR and HBR2	5		7.2	dB
$\Delta V_{PRE(L1L0)}$	Pre-emphasis delta	Measured in compliance with latest PHY CTS 1.2	2			dB
$\Delta V_{PRE(L2L1)}$			1.6			dB

(1) Does not support Level 3 swing or pre-emphasis.

## 5.10 Switching Characteristics, TMDS

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX <sup>(1)</sup>	UNIT
$d_R$	Data rate		250		6000	Mbps
$t_{T(DATA)}$	Transition time (rise and fall time); measured at 20% and 80%. SDA_CTL = L, OE = H, All Data	Reg0Ah[1:0] = 11 (default)		60		ps
		Reg0Ah[1:0] = 10		80		ps
		Reg0Ah[1:0] = 01		95		ps
		Reg0Ah[1:0] = 00		110		ps
$t_{T(CLOCK)}$	Rates Note: Data lane control by I2C only: See <a href="#">セクション 7.3.10</a>	TERM = H; Reg0Bh[7:6] = 11		122		ps
		Reg0Bh[7:6] = 10		150		ps
		TERM = L; Reg0Bh[7:6] = 00		180		ps
		TERM = NC; Reg0Bh[7:6] = 01		203		ps

(1) The maximum rating is simulated at 3.6V  $V_{CC}$  and 1.27V  $V_{DD}$  and at 85°C temperature unless otherwise noted.

(2) The typical rating is simulated at 3.3V  $V_{CC}$  and 1.1V  $V_{DD}$  and at 27°C temperature unless otherwise noted.

## 5.11 Switching Characteristics, HPD

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX <sup>(1)</sup>	UNIT
$t_{PD(HPD)}$	Propagation delay from HPD_SNK to HPD_SRC; rising edge and falling edge	see <a href="#">図 6-8</a> ; not valid during switching time		40	120	ns
$t_{T(HPD)}$	HPD logical disconnected timeout	see <a href="#">図 6-9</a>	2			ms

(1) The Maximum rating is simulated at 3.6V  $V_{CC}$  and 1.27V  $V_{DD}$  and at 85°C temperature unless otherwise noted

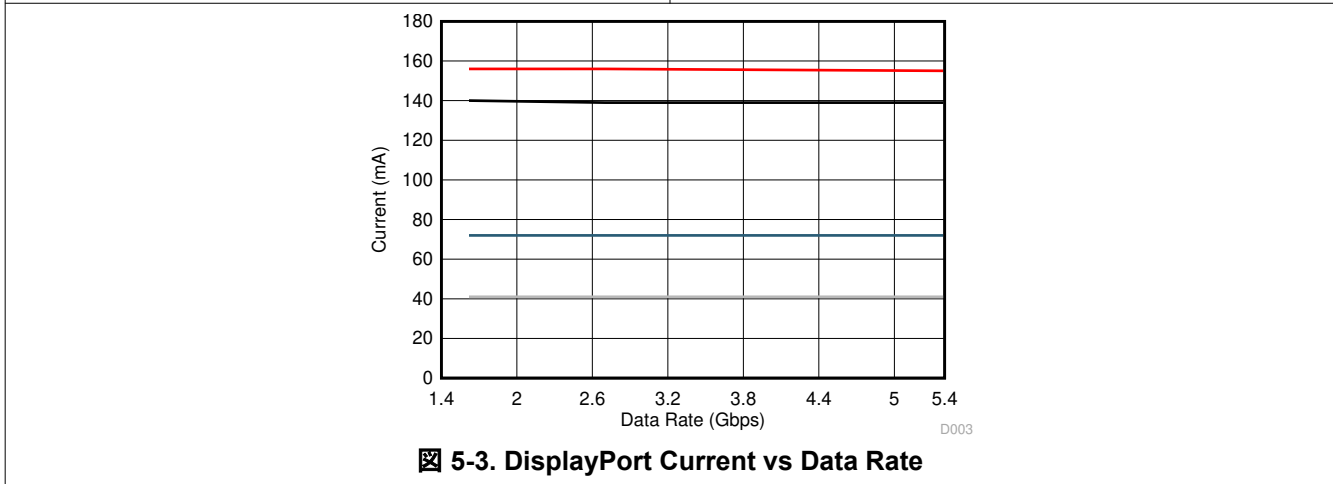
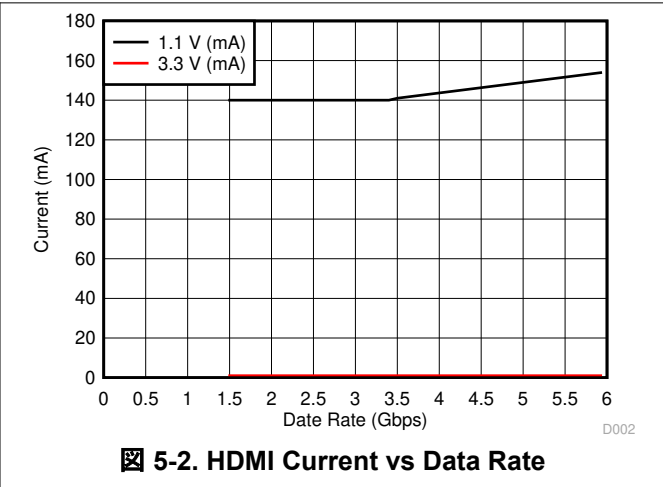
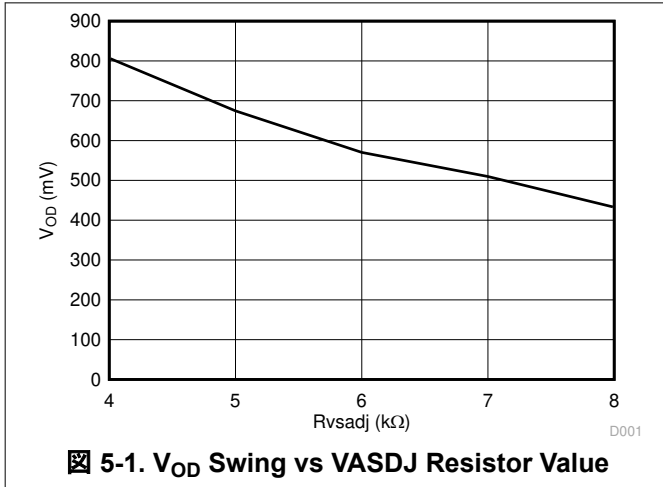
(2) The Typical rating is simulated at 3.3V  $V_{CC}$  and 1.1V  $V_{DD}$  and at 27°C temperature unless otherwise noted

## 5.12 Switching Characteristics, DDC and I<sup>2</sup>C

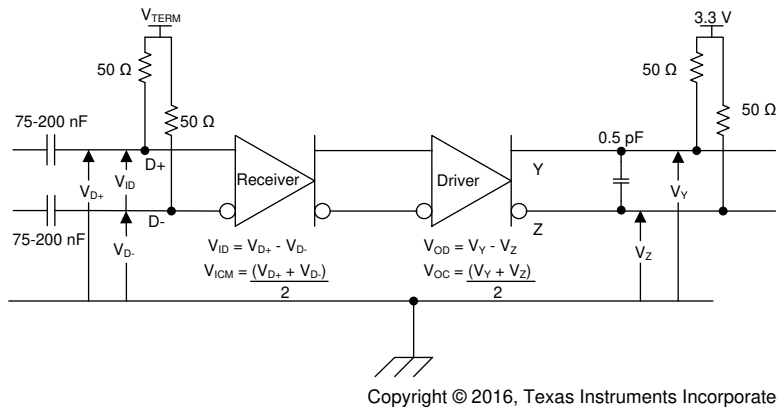
over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_r$	Rise time of both SDA and SCL signals	$V_{CC} = 3.3V$ ; See <a href="#">6-12</a>			300	ns
$t_f$	Fall time of both SDA and SCL signals	See <a href="#">6-12</a>			300	ns
$t_{HIGH}$	Pulse duration , SCL high	See <a href="#">6-11</a>	0.6			$\mu s$
$t_{LOW}$	Pulse duration , SCL low	See <a href="#">6-11</a>	1.3			$\mu s$
$t_{SU1}$	Setup time, SDA to SCL	See <a href="#">6-11</a>	100			ns
$t_{ST, STA}$	Setup time, SCL to start condition	See <a href="#">6-11</a>	0.6			$\mu s$
$t_{HD, STA}$	Hold time, start condition to SCL	See <a href="#">6-10</a>	0.6			$\mu s$
$t_{HD, DAT}$	Data Hold Time		0			ns
$t_{VD, DAT}$	Data valid time		0.9			$\mu s$
$t_{VD, ACK}$	Data valid acknowledge time		0.9			$\mu s$
$t_{ST, STO}$	Setup time, SCL to stop condition	See <a href="#">6-10</a>	0.6			$\mu s$
$t_{(BUF)}$	Bus free time between stop and start condition	See <a href="#">6-10</a>	1.3			$\mu s$

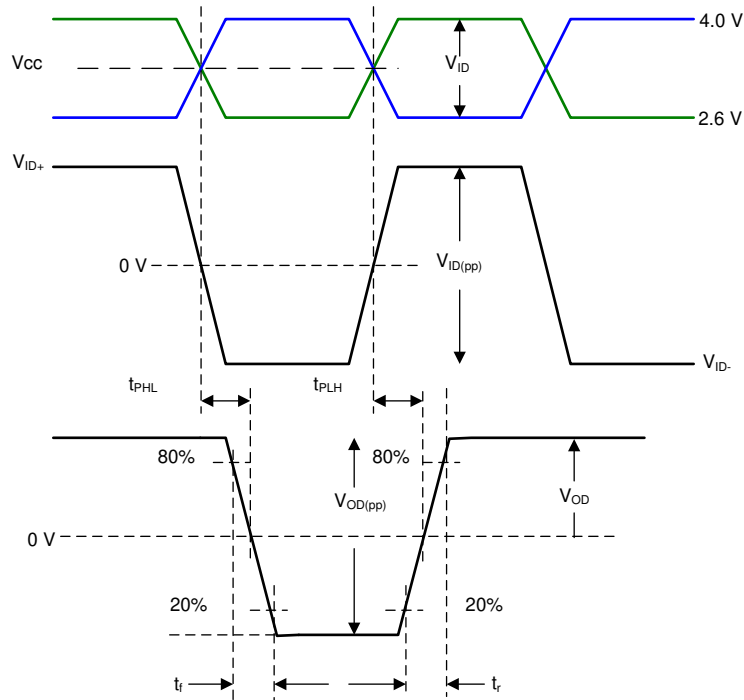
### 5.13 Typical Characteristics



## 6 Parameter Measurement Information



**图 6-1. TMD5 Main Link Test Circuit**



**图 6-2. Input or Output Timing Measurements**

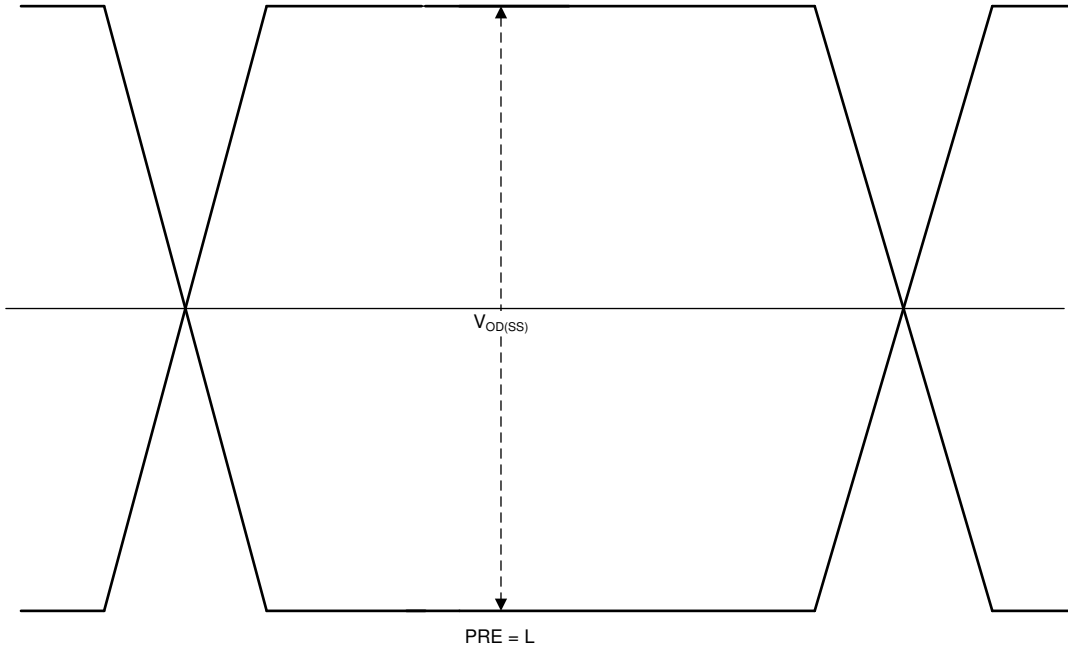


図 6-3. Output Differential Waveform

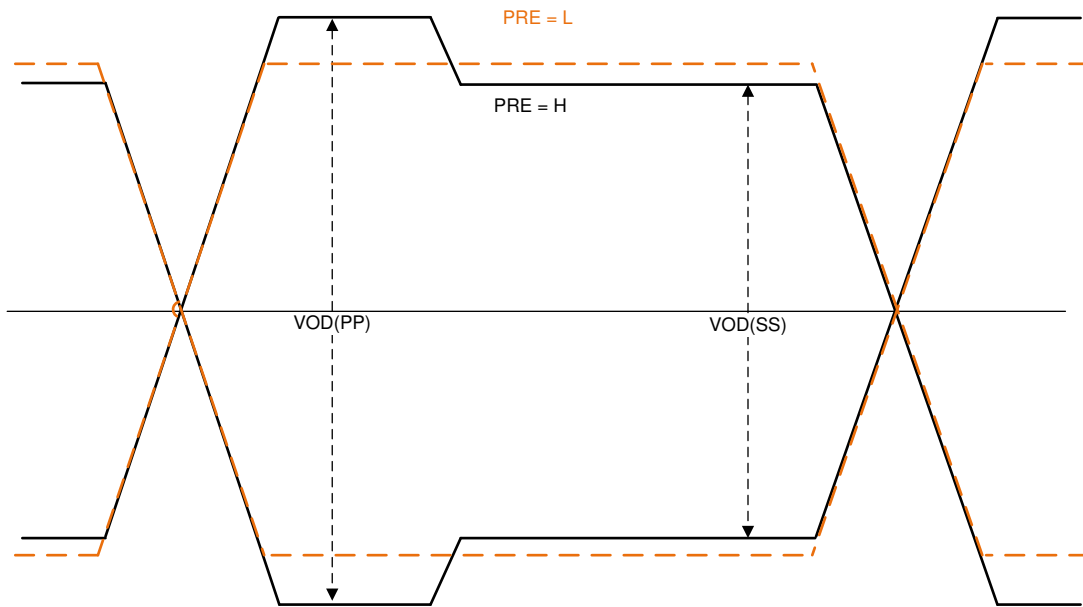
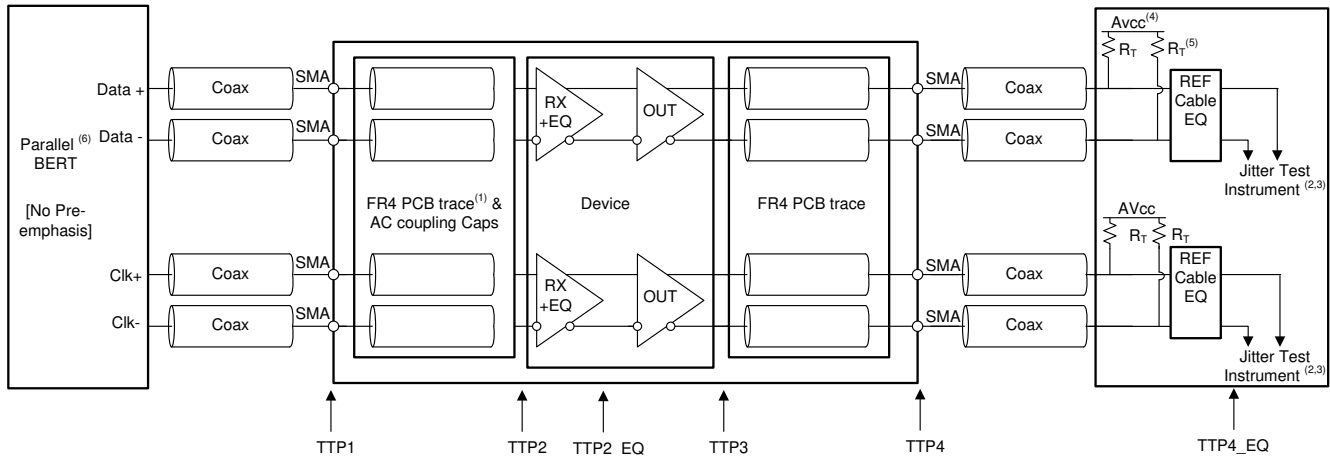


図 6-4. Output Differential Waveform with De-Emphasis



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- A. The FR4 trace between TTP1 and TTP2 is designed to emulate 1-8" of FR4, AC coupling capacitor, connector and another 1-8" of FR4. Trace width – 4 mils. 100Ω differential impedance.
- B. All Jitter is measured at a BER of 10<sup>9</sup>
- C. Residual jitter reflects the total jitter measured at TTP4 minus the jitter measured at TTP
- D. AVCC = 3.3V
- E. R<sub>T</sub> = 50Ω
- F. The input signal from parallel Bert does not have any pre-emphasis. Refer to *Recommended Operating Conditions*.

图 6-5. HDMI Output Jitter Measurement

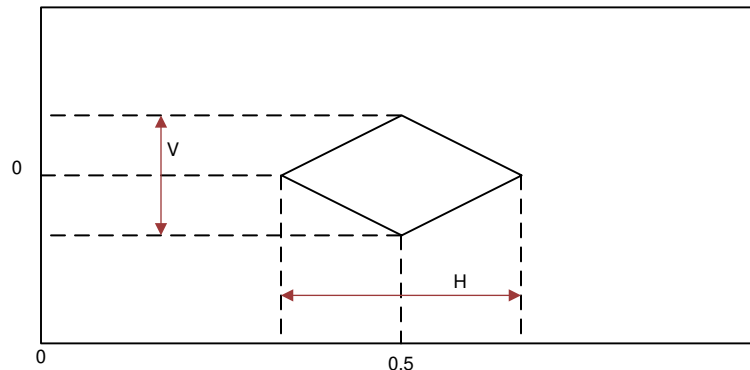


图 6-6. Output Eye Mask at TTP4\_EQ for HDMI 2.0

TMDS Data Rate (Gbps)	H (Tbit)	V (mV)
3.4 < DR < 3.712	0.6	335
3.712 < DR < 5.94	$-0.0332R_{bit}^2 + 0.2312 R_{bit} + 0.1998$	$-19.66R_{bit}^2 + 106.74R_{bit} + 209.58$
$5.94 \leq DR \leq 6.0$	0.4	150

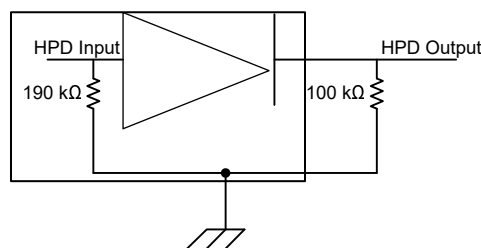
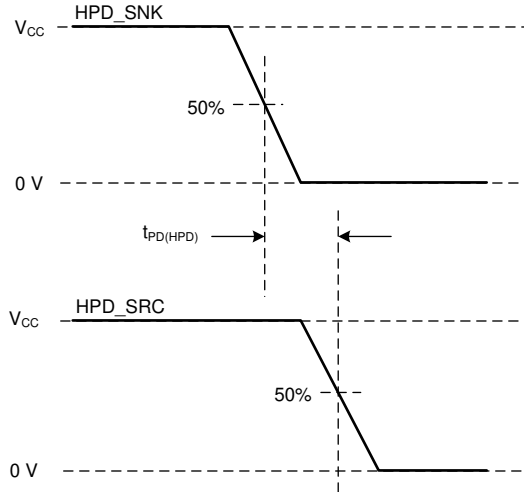
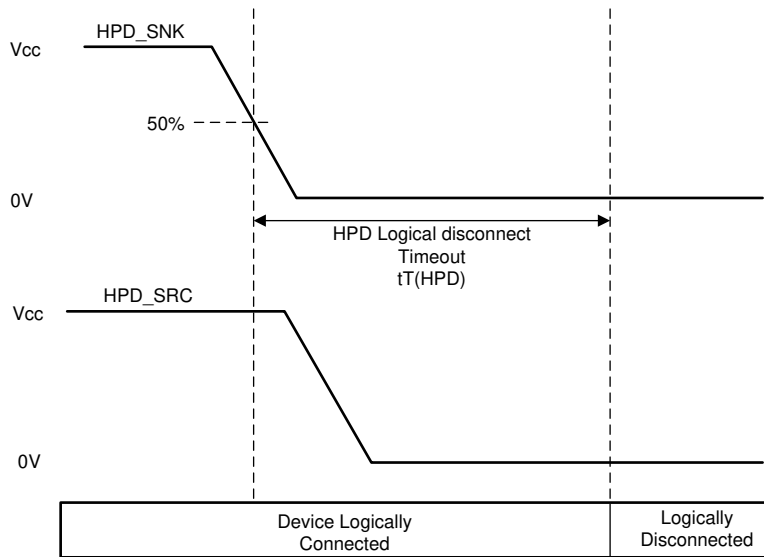


图 6-7. HPD Test Circuit



**図 6-8. HPD Timing Diagram No. 1**



**図 6-9. HPD Logic Disconnect Timeout**

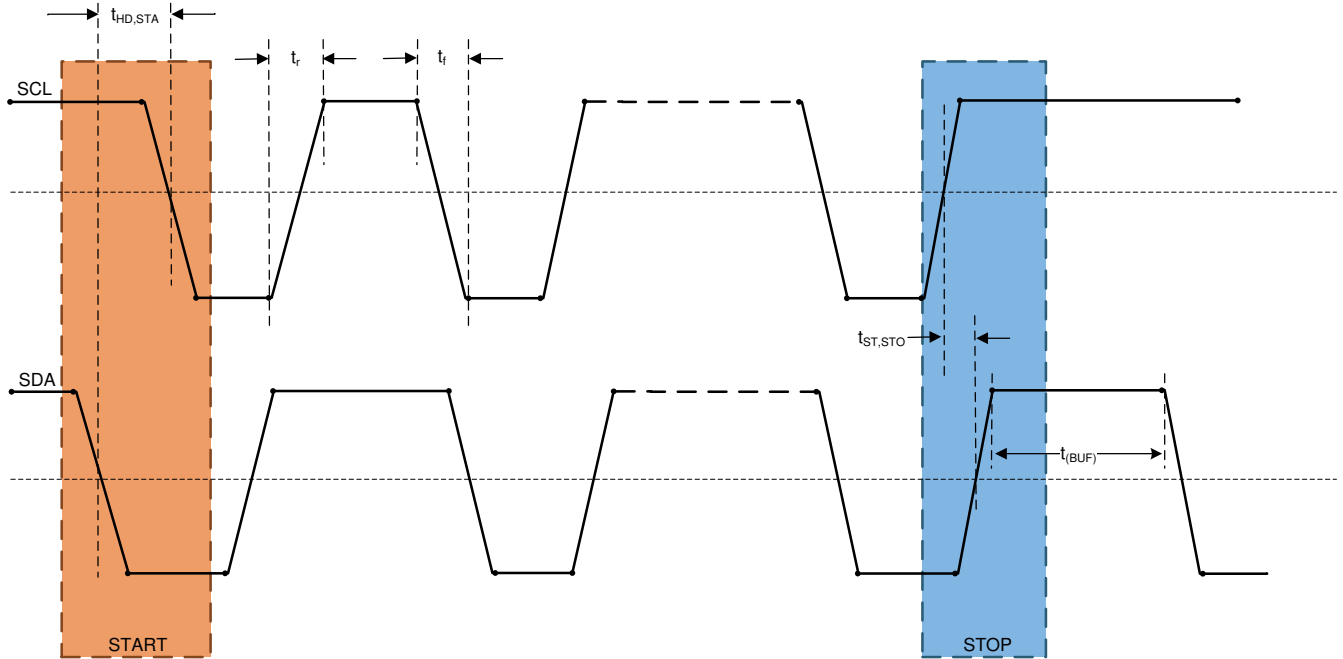


図 6-10. Start and Stop Condition Timing

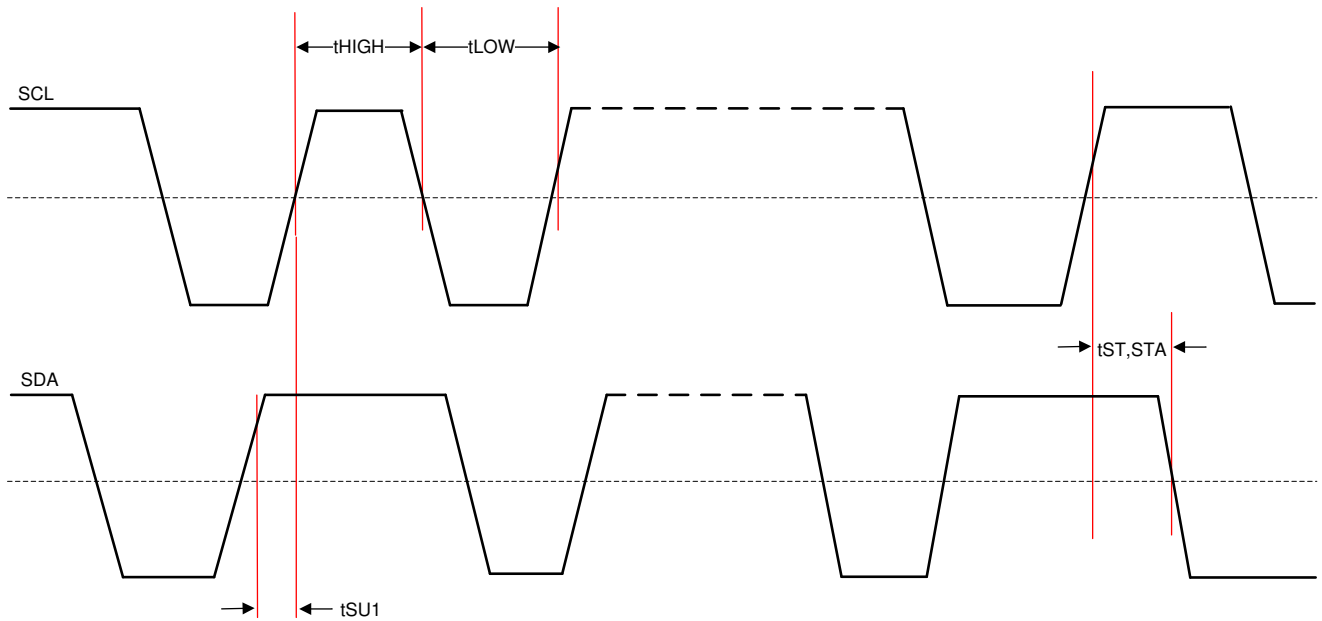


図 6-11. SCL and SDA Timing

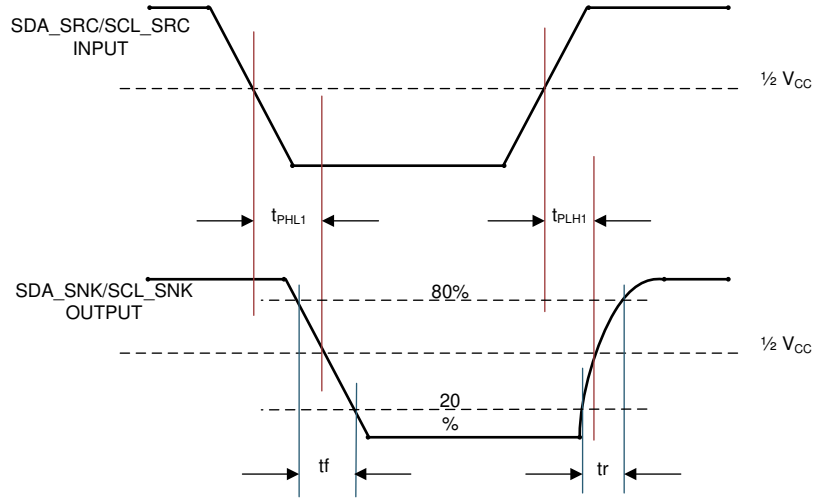


図 6-12. DDC Propagation Delay – Source to Sink

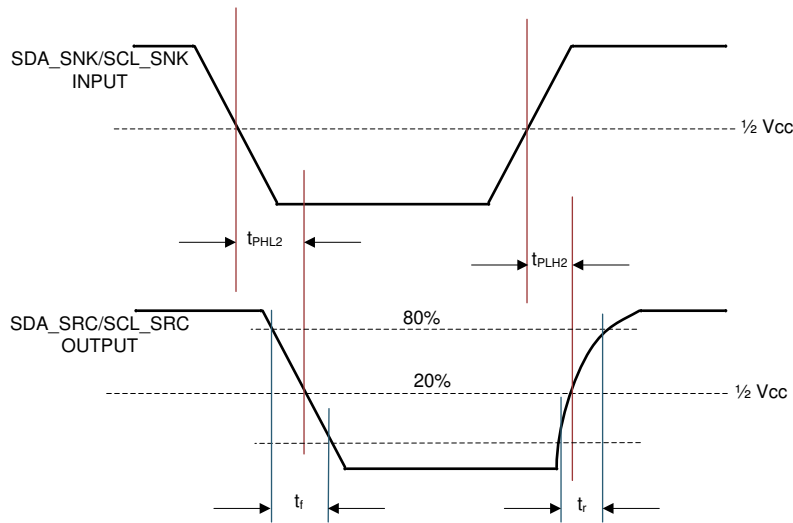


図 6-13. DDC Propagation Delay – Sink to Source

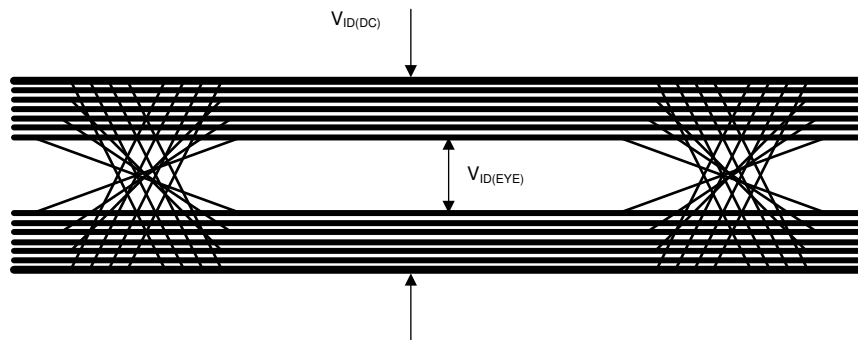


図 6-14.  $V_{ID(DC)}$  and  $V_{ID(EYE)}$

## 7 Detailed Description

### 7.1 Overview

The TDP158 is an AC-coupled digital video interface (DVI) or high-definition multimedia interface (HDMI) signal input to Transition Minimized Differential Signal (TMDS) level shifting Redriver. The TDP158 supports four TMDS channels, Hot Plug Detect, and a Digital Display Control (DDC) interfaces. The TDP158 supports signaling rates up to 6Gbps to allow for the highest resolutions of 4k 2k 60p 24 bits per pixel and up to WUXGA 16-bit color depth or 1080p with higher refresh rates. For passing compliance and reducing system level design issues, several features have been included such as TMDS output amplitude adjust using an external resistor on the VSADJ pin, source termination selection, pre-emphasis, and output slew rate control. Device operation and configuration can be programmed by pin strapping or I<sup>2</sup>C. Four TDP158 devices can be used on one I<sup>2</sup>C bus when I2C\_EN is high with device address set by A0/A1.

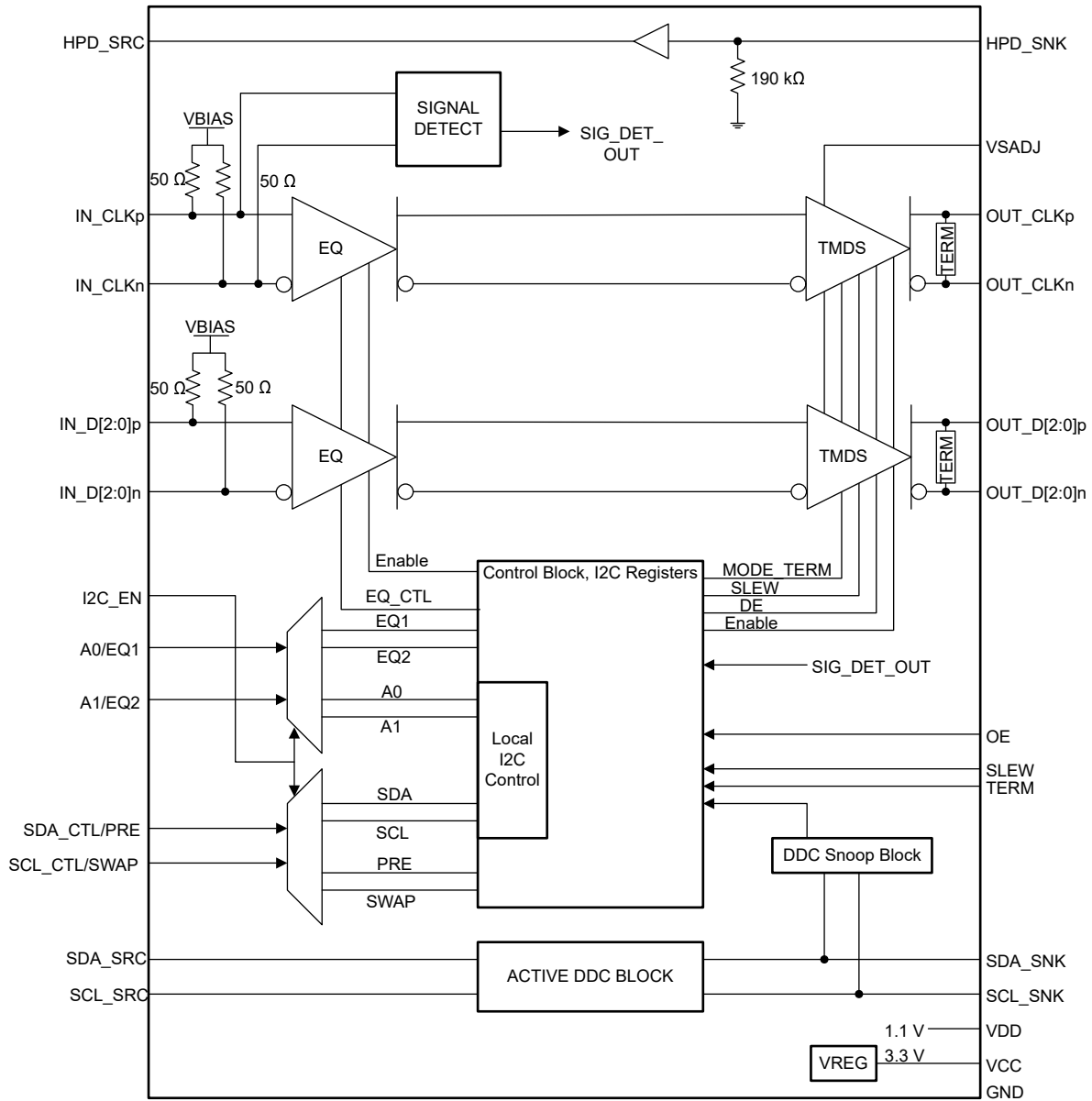
To reduce active power the TDP158 supports dual power supply rails of 1.1V on VDD and 3.3V on VCC. There are several methods of power management such as going into power down mode using three methods:

1. HPD is low
2. Writing a 1 to register 09h[3]
3. De-asserting OE

De-asserting OE clears the I<sup>2</sup>C registers, thus once re-asserted, the device must be reprogrammed if I<sup>2</sup>C was used for device setup. The TDP158 requires the source to write a 1 to the TMDS\_CLOCK\_RATIO\_STATUS register for the TDP158 to resume 75Ω to 150Ω source termination upon return to normal active operation from re-asserted, OE, or re-asserted HPD. If this bit is already set as a one during the source to sink read, then the TDP158 automatically sets this bit to 1. The SIG\_EN register enables the signal detect circuit that provides an automatic power-management feature during normal operation. When no valid signal is present on the clock input, the device enters Standby mode. DDC link supports the HDMI 2.0b SCDC communication, 100Kbps data rate default and 400Kbps adjustable by software.

TDP158 supports fixed EQ gain control to compensate for different lengths of input cables or board traces. The EQ gain can be software adjusted by I<sup>2</sup>C control or pin strapping EQ1 and EQ2 pins. Customers can use the TERM to change to one of three source termination impedance for better output performance when working in HDMI 1.4b or HDMI 2.0b. When the TMDS\_CLOCK\_RATIO\_STATUS bit is set to 1, the TDP158 automatically switches in 75Ω to 150Ω source termination. To assist in ease of implementation, the TDP158 supports lanes swapping, see [セクション 7.3.3](#). The device's available extended commercial temperature range is 0°C to 85°C.

## 7.2 Functional Block Diagram

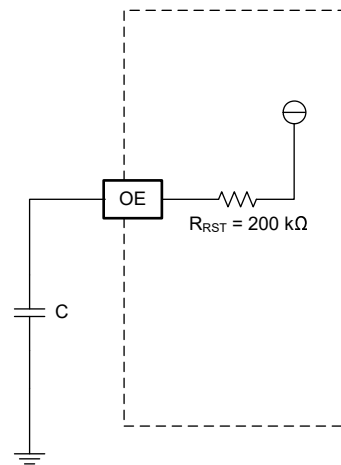


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## 7.3 Feature Description

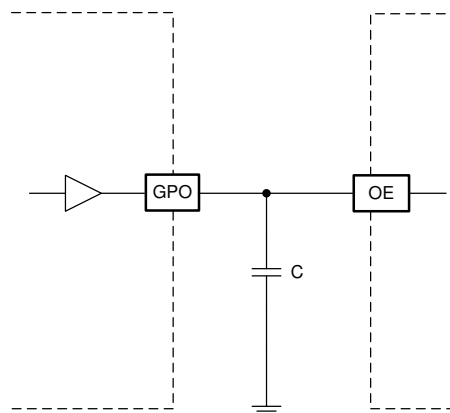
### 7.3.1 Reset Implementation

When OE is low, control signal inputs are ignored; the HDMI inputs and outputs are high impedance. It is critical to transition the OE from a low level to high after the  $V_{CC}$  supply has reached the minimum recommended operating voltage. This is achieved by a control signal to the OE input, or by an external capacitor connected between OE and GND. To properly reset the TDP158, the OE pin must be de-asserted for at least 100  $\mu$ s before being asserted. When OE is re-asserted the TDP158 must be reprogrammed if it was programmed by I<sup>2</sup>C and not pin strapping. When implementing the external capacitor, the size of the external capacitor depends on the power up ramp of the  $V_{CC}$  supply, where a slower ramp-up results in a larger value external capacitor. Refer to the latest reference schematic for TDP158; consider approximately 0.1  $\mu$ F capacitor as a reasonable first estimate for the size of the external capacitor. Both OE implementations are shown in [Figure 7-1](#) and [Figure 7-2](#).



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図 7-1. External Capacitor Controlled OE



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図 7-2. OE Input from Active Controller

### 7.3.2 Operation Timing

TDP158 starts to operate after the OE signal is properly set after power up timing is complete. See 図 7-3 and 表 7-1. Keeping OE low until  $V_{DD}$  and  $V_{CC}$  becomes stable avoids any timing requirements as shown in 図 7-3.

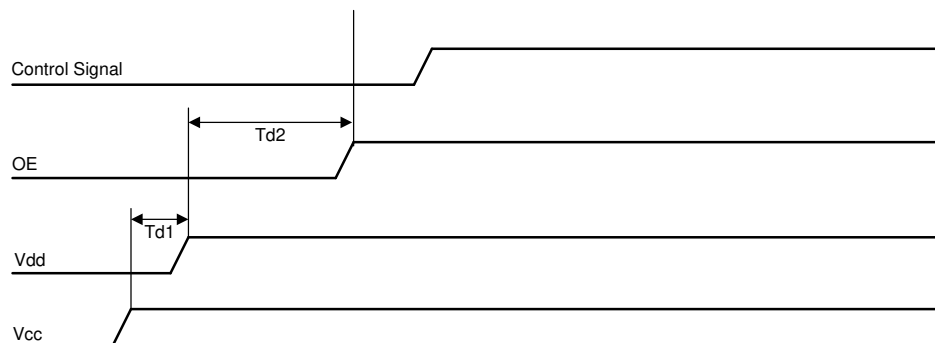


図 7-3. Power Up Timing for TDP158

表 7-1. Power Up and Operation Timing Requirements

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
$t_{d1}$	$V_{CC}$ stable before $V_{DD}$	0		200	$\mu$ s
$t_{d1}$	$V_{DD}$ and $V_{CC}$ stable before OE de-assertion	100			$\mu$ s
$V_{DD(ramp)}$	$V_{DD}$ supply ramp up requirements	0.002		100	ms
$V_{CC(ramp)}$	$V_{CC}$ supply ramp up requirements	0.002		100	ms

### 7.3.3 Lane Control

The TDP158 has various lane control features. By default the high speed lanes are globally controlled. Pin strapping can globally control features like receiver equalization,  $V_{OD}$  swing and pre-emphasis. I<sup>2</sup>C programming performs the same global programming using default configurations. Through I2C a method to control receive equalization, transmitter swing ( $V_{OD}$ ) and pre-emphasis on each individual lane. Setting reg09h[5] = 1 puts the device into independent lane configuration mode.

Reg31h[7:3] controls the clock lane, reg32h[7:3] controls lane D0, reg33h[7:3] controls lane D1 and reg34h[7:3] controls lane D2 while Reg4E and Reg4F control the individual lane EQ control.

注

If the swap function is enabled and individual lane control has been implemented, then it is recommended to reprogram the lanes to ensure they match the expected results. Registers are mapped to the pin name convention.

### 7.3.4 Swap

TDP158 incorporates a swap function which can swap the lanes, see 図 7-4. The EQ, Pre-emphasis, termination, and slew setup will follow the new mapping. This function can be used with the SCL\_CTL/SWAP pin 13 when I2C\_EN pin 8 is low or can be implemented using control the register 0x09h bit 7 and is only valid for HDMI mode.

表 7-2. Swap Functions

Normal Operation	SWAP = L or CSR 0x09h bit 7 is 1'b1	Pin Numbers
IN_D2 → OUT_D2	IN_CLK → OUT_CLK	[1, 2] → [30, 29]
IN_D1 → OUT_D1	IN_D0 → OUT_D0	[4, 5] → [27, 26]
IN_D0 → OUT_D0	IN_D1 → OUT_D1	[6, 7] → [25, 24]
IN_CLK → OUT_CLK	IN_D2 → OUT_D2	[9, 10] → [22, 21]

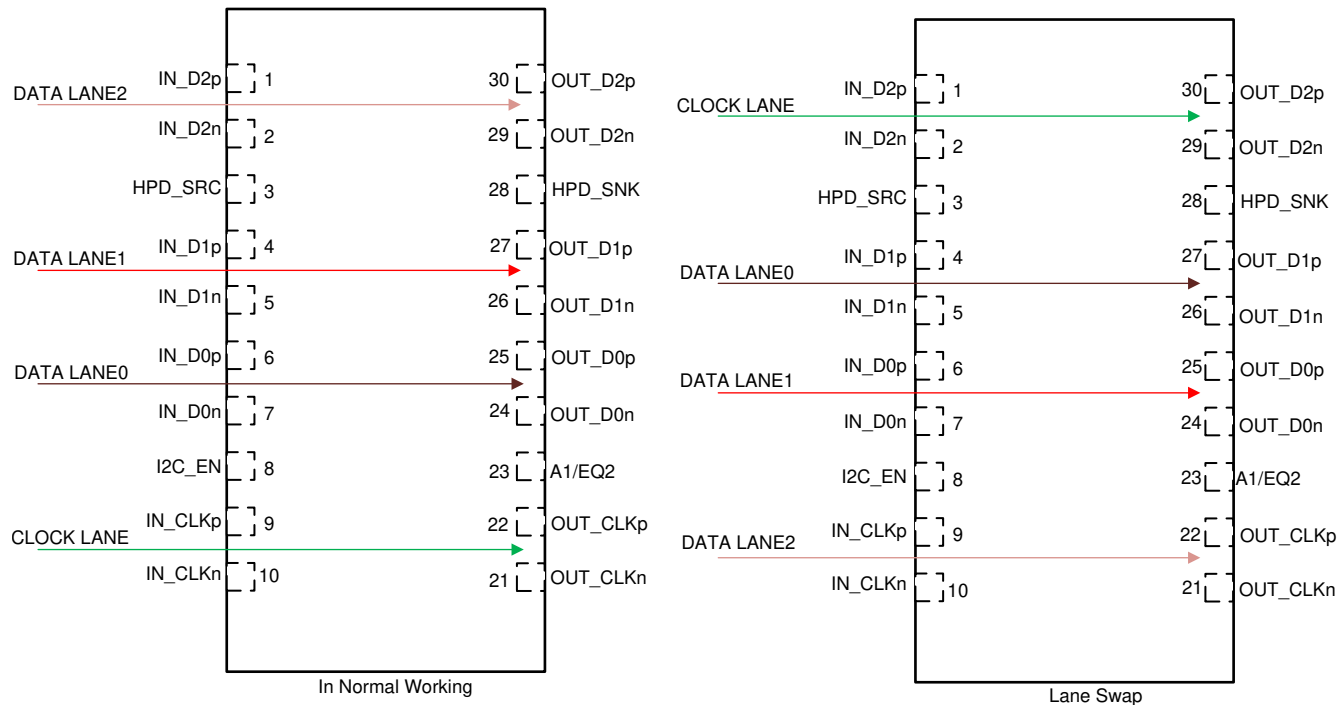


图 7-4. TDP158 Swap Function

### 7.3.5 Main Link Inputs

Standard Dual Mode DisplayPort terminations are integrated on all inputs with expected AC coupling capacitors on board prior to input pins. External terminations are not required. Each input data channel contains an equalizer to compensate for cable or board losses. The voltage at the input pins must be limited under the absolute maximum ratings.

### 7.3.6 Receiver Equalizer

The equalizer is used to clean up inter-symbol interference (ISI) jitter/loss from the bandwidth-limited board traces or cables. TDP158 supports fixed receiver equalizer by setting the A0/EQ1 and A1/EQ2 pins or through I<sup>2</sup>C. 表 7-3 provides the pin strap settings and EQ values.

表 7-3. Receiver EQ Programming and Values

RX EQ (dB)	Pin Control <sup>(1)</sup> {EQ2,EQ1}	Global	Independent Lane Control			
		I2C Control	I2C Control <sup>(2)</sup>			
		P0_Reg0D[6:3]	D2 P0_Reg4E[3:0]	D1 P0_Reg4E[7:4]	D3 P0_Reg4F[3:0]	CLK <sup>(2) (3)</sup> P0_Reg4F[7:4]
2	2'b00	4'b0000	4'b0000	4'b0000	4'b0000	4'b0000
3	2'b0Z	4'b0001	4'b0001	4'b0001	4'b0001	4'b0001
4		4'b0010	4'b0010	4'b0010	4'b0010	4'b0010
5	2'b01	4'b0011	4'b0011	4'b0011	4'b0011	4'b0011
6.5	2'bZ0	4'b0100	4'b0100	4'b0100	4'b0100	4'b0100
7.5		4'b0101	4'b0101	4'b0101	4'b0101	4'b0101
8.5	2'bZZ	4'b0110	4'b0110	4'b0110	4'b0110	4'b0110
9		4'b0111	4'b0111	4'b0111	4'b0111	4'b0111
10	2'bZ1	4'b1000	4'b1000	4'b1000	4'b1000	4'b1000
11	2'b10	4'b1001	4'b1001	4'b1001	4'b1001	4'b1001
12		4'b1010	4'b1010	4'b1010	4'b1010	4'b1010
13		4'b1011	4'b1011	4'b1011	4'b1011	4'b1011
14		4'b1100	4'b1100	4'b1100	4'b1100	4'b1100

表 7-3. Receiver EQ Programming and Values (続き)

RX EQ (dB)	Global		Independent Lane Control			
	Pin Control <sup>(1)</sup>	I2C Control	I2C Control <sup>(2)</sup>			
	{EQ2,EQ1}	P0_Reg0D[6:3]	D2 P0_Reg4E[3:0]	D1 P0_Reg4E[7:4]	D3 P0_Reg4F[3:0]	CLK <sup>(2) (3)</sup> P0_Reg4F[7:4]
14.5	2'b1Z	4'b1101	4'b1101	4'b1101	4'b1101	4'b1101
15		4'b1110	4'b1110	4'b1110	4'b1110	4'b1110
15.5	2'b11	4'b1111	4'b1111	4'b1111	4'b1111	4'b1111

- (1) For Pin Control 0 = 1kΩ pulldown resistor to GND, 1 = 1kΩ pullup resistor to VCC, Z = Floating (No Connect)  
(2) Individual Lane control is based upon the pin names with no swap  
(3) The CLK EQ in HDMI mode is controlled by register P0\_Reg0D[2:1]

### 7.3.7 Input Signal Detect Block

When SIG\_EN is enabled through I<sup>2</sup>C the receiver looks for a valid HDMI clock signal input and is fully functional when a valid signal is detected. If no valid HDMI clock signal is detected, then the device enters standby mode waiting for a valid signal at the clock input. All of the TMDS outputs and IN\_D[0:2] are in high-Z status. HDMI signal detect circuit is default enabled. If there is a loss of signal, then reg20h[5] can be read to determine if the TDP158 has detected a valid signal or not.

### 7.3.8 Transmitter Impedance Control

HDMI 2.0 standard requires a source termination impedance in the 75Ω to 150Ω range for data rates > 3.4Gbps. HDMI 1.4b requires no source termination but has a provision for using 150Ω to 300Ω for higher data rates. The TDP158 has three termination levels that are selectable using pin 16 when programming through pin strapping or when using I<sup>2</sup>C programming through reg0Bh[4:3]. When the TMDS\_CLOCK\_RATIO\_STATUS bit, reg0Bh[1] = 1 the TDP158 automatically turns on the 75Ω to 150Ω source termination otherwise the termination must be selected. 表 7-4 provides more information.

表 7-4. Source Termination Control Table

Pin 16	Reg0Bh[4:3]	Source Termination
TERM = L	00	150Ω ≅ 300Ω
TERM = NC	01	None
	10	Automatic set based upon TMDS_CLOCK_RATIO_STATUS bit
TERM = H	11	75Ω ≅ 150Ω

注

If the TMDS\_CLOCK\_RATIO\_STATUS bit = 1, then the TDP158 automatically switches in 75Ω ≅ 150Ω termination.

### 7.3.9 TMDS Outputs

A 1% precision resistor, connected from VSADJ pin to ground is recommended to allow the differential output swing to comply with TMDS signal levels. The differential output driver provides a typical 10-mA current sink capability, which provides a typical 500mV voltage drop across a 50Ω termination resistor.

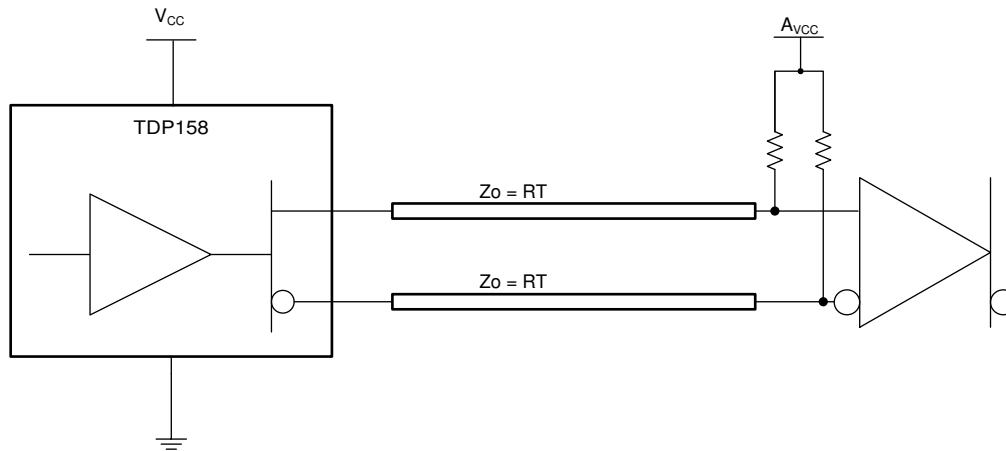


図 7-5. TMDS Driver and Termination Circuit

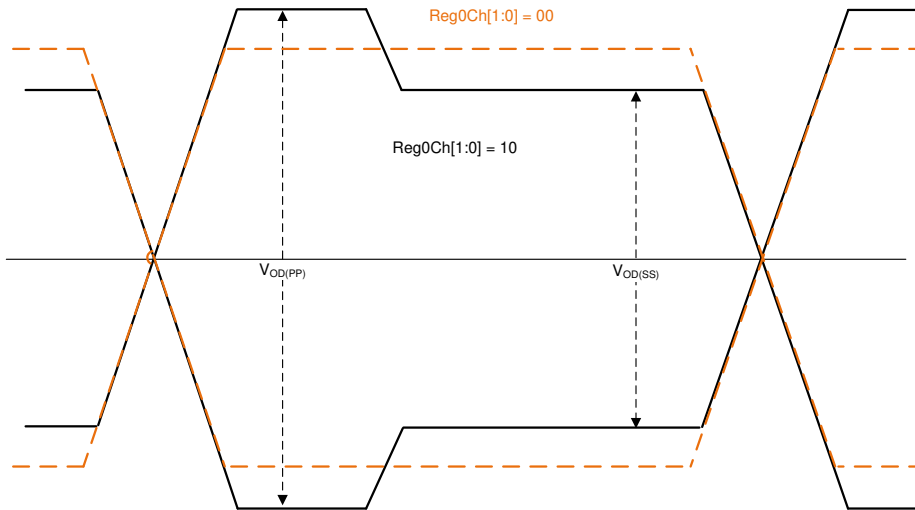
Referring to 図 7-5, if  $V_{CC}$  (TDP158 supply) and  $A_{VCC}$  (sink termination supply) are both powered, the TMDS output signals are high impedance when OE = low. Both supplies being active is the normal operating condition. A total of approximately 33-mW of power is consumed by the terminations independent of the OE logical selection. When  $A_{VCC}$  is powered on, normal operation (OE controls output impedance) is resumed. When the power source of the device is off and the power source to termination is on, the  $I_{O(off)}$ , output leakage current, specification ensures the leakage current is limited 45- $\mu$ A or less. The clock and data lanes  $V_{OD}$  can be changed through I<sup>2</sup>C reg0Ch[7:2], VSWING\_DATA and VSWING\_CLK.

### 7.3.10 Slew Rate Control

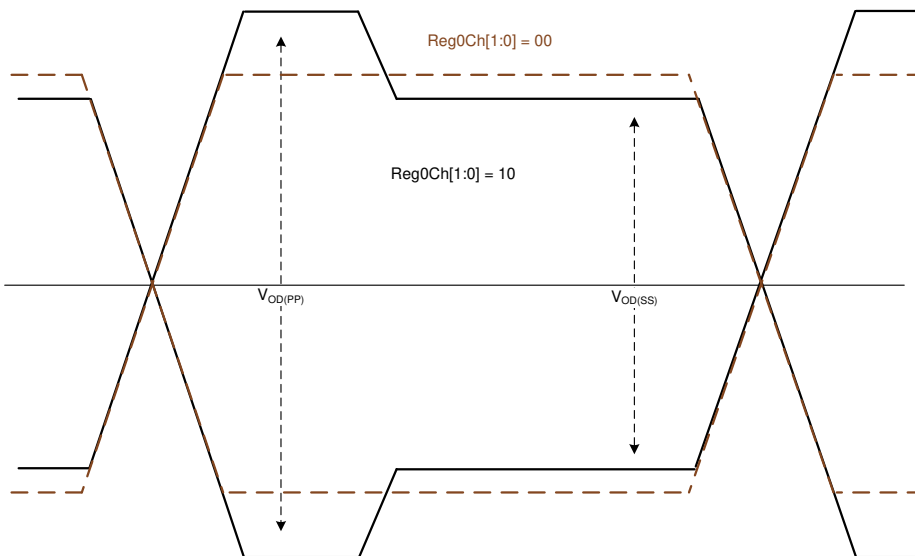
As the clock signal tends to be a primary source of EMI, the TDP158 provides the ability to slow down the TMDS output edge rates. There are two ways of changing the slew rate, pin strapping for clock lane and I<sup>2</sup>C for both clock and data lanes. Refer to [セクション 5.10](#)

### 7.3.11 Pre-Emphasis

The TDP158 provides pre-emphasis on the data lanes allowing the output signal pre-conditioning to offset interconnect losses between the TDP158 outputs and a TMDS receiver. Pre-emphasis is not implemented on the clock lane unless the TDP158 is in DP mode; at which time, it becomes a data lane. The default value for pre-emphasis is 0dB. There are two methods to implement pre-emphasis, pin strapping or through I<sup>2</sup>C programming. When using pin strapping, the SDA\_CTL/PRE pin controls global pre-emphasis values of 0dB or 3.5dB. Through I<sup>2</sup>C, reg0Ch[1:0] pre-emphasis values are 0dB, 3.5dB, and 6dB. The 6dB value has different meanings when the device is in normal operational mode (reg09h[5] = 0) or when the TDP158 has been put into DP-mode (reg09h[5] = 1). As 7-6 shows, the 6dB pre-emphasis setting will result in an output of 3dB of pre-emphasis with 3dB of de-emphasis when device is in normal HDMI operation. As 7-7 shows, the output will be about 5dB pre-emphasis with a 1dB de-emphasis when selecting 6dB pre-emphasis setting for DP-mode.  $V_{OD(PP)}$  value will not go above 1V.



7-6. 6dB Pre-Emphasis Setting in Normal Operation



7-7. 6dB Pre-Emphasis in DP-Mode

表 7-5. Swing and Pre-Emphasis Programming Based Upon 6kΩ VSADJ Resistor

Mode	Global Control			Independent Lane Control		
	Reg09h[6] Lane CTL	Reg09[5] Mode CTL	P0_Reg0C[7:0]	Reg09h[6] Lane CTL	Reg09[5] Mode CTL	P0_Reg0C[7:0]
HDMI	0	0	8'h00	1	0	8'h00
DP SWG0, PRE0	0	1	8'h80	1	1	8'h80
DP SWG0, PRE1	0	1	8'hC1	1	1	8'hC1
DP SWG0, PRE2	0	1	8'h42	1	1	8'h42
DP SWG1, PRE0	0	1	8'hC0	1	1	8'hA0
DP SWG1, PRE1	0	1	8'hF1	1	1	8'h21
DP SWG1, PRE2	0	1	8'h52	1	1	8'h62
DP SWG2, PRE0	0	1	8'h20	1	1	8'h00
DP SWG2, PRE1	0	1	8'h51	1	1	8'h61

### 7.3.12 DP-Mode Description

The TDP158 has the ability to perform as a DisplayPort redriver under the right conditions. The TDP158 is put into this mode by setting reg09h[5] to 1. The device is now programmable through I<sup>2</sup>C only. As the transmitter is a DC coupled transmitter supporting TMDS some external circuits are required to level shift the signal to an AC-coupled DisplayPort signal, see [図 8-6](#). Note that the AUX lines bypass the TDP158. To set the device up correctly during link training, the TDP158 must be programmed using I<sup>2</sup>C. When this bit is set, the TDP158 does the following:

- Ignore SWAP function
- Ignore SIG\_EN function
- Enable all four lanes and set to support 5.4Gbps data rate
- Sets V<sub>OD</sub> swing to the lowest level based on a 6 kΩ VSADJ resistor value
- Sets pre-emphasis to 0dB
- Defaults to global lane control
- Can be set to independent lane control by setting P0\_Reg09[6] to a 1. This should be done after implementing DP mode. Individual Lane control starts on P0\_Reg30 through P0\_Reg34 and also P0\_Reg4E and 4F

For the system implementer to configure the TDP158 output to the properly requested levels during link training, the following registers are used.

- Reg0Ch[7:5] is a global V<sub>OD</sub> swing control for all four lanes; [表 7-5](#) provides more information
- Reg0Ch[1:0] is a global pre-emphasis control for all four lanes; [表 7-5](#) provides more information. This register works with Reg30h[7:6]
- Reg0D[6:3] is a global EQ control for all four lanes
- Reg30h[7:6] is to let the TDP158 know what the data rate is. This is used for the delay component for pre-emphasis signal.
- Reg30h[5:2] is used to turn on or off individual lanes

Power down states while in DP-Mode are implemented the same as if in normal operation. See [セクション 5.7](#) for the outputs based upon the VSADJ 6kΩ VSADJ resistor.

## 7.4 Device Functional Modes

### 7.4.1 DDC Training for HDMI 2.0 Data Rate Monitor

As part of discovery, the source reads the sink E-EDID information to understand the sink's capabilities. The supported data rate comes from the HDMI Forum Vendor Specific Data Block (HF-VSDB) MAX\_TMDS\_Character\_Rate byte. Depending upon the value, the source will write to target address 0xA8 offset 0x20 bit1, TMDS\_CLOCK\_RATIO\_STATUS. The TDP158 snoops the DDC link to determine the TMDS clock ratio status and thus sets its own TMDS\_CLOCK\_RATIO\_STATUS bit accordingly. If a '1' is written by the source the TMDS clock is 1/40 of TMDS bit period. If a '0' is written, then the TMDS clock is 1/10 of TMDS bit period.

The TDP158 will always default to 1/10 of TMDS bit period unless a '1' is written to address 0xA8 offset 0x20 bit 1 or during a read by the source this bit is set. This helps determine source termination when automatic source termination select is enabled. Otherwise this bit has no other impact on the TDP158. When HPD\_SNK is de-asserted this bit is reset to default values of 0 if this feature is enabled. If the source does not write this bit to the sink or during the read the bit is not set the TDP158 will not set the output termination to 75Ω to 150Ω in support of HDMI 2.0. If the TDP158 has entered a power down state using HDP\_SNK = low or OE = low this bit is cleared and will be set on a read or write where this bit is set. When DDC\_TRAIN\_SETDISABLE is 1'b0 the TMDS\_CLOCK\_RATIO\_STATUS bit will reflect the value of the DDC snoop. When DDC\_TRAIN\_SETDISABLE is 1'b1 the TMDS\_CLOCK\_RATIO\_STATUS bit is set by I<sup>2</sup>C and DDC snoop is ignored and thus automatic TERM control is ignored and must be manually set. To go back to snoop and automatic TERM control the DDC\_TRAIN\_SETDISABLE bit has to be cleared and TERM set back to automatic control.

#### 7.4.2 DDC Functional Description

The TDP158 solves sink/source level issues by implementing a controller/target control mode for the DDC bus. When the TDP158 detects the start condition on the DDC bus from the SDA\_SRC/SCL\_SRC it transfers the data or clock signal to the SDA\_SNK/SCL\_SNK with little propagation delay. When SDA\_SNK detects the feedback from the downstream device, the TDP158 pulls up or pulls down the SDA\_SRC bus and delivers the signal to the source.

The DDC link defaults to 100Kbps but can be set to various values including 400Kbps by setting the correct value to address 22h through the I<sup>2</sup>C interface. The HPD goes to high impedance when VCC is under low power conditions, < 1.5V.

#### 注

The TDP158 uses clock stretching for DDC transactions. As there are sources and sinks that do not perform this function correctly, a system may not work correctly as DDC transactions are incorrectly transmitted/received. To overcome this, a snoop configuration can be implemented where the SDA/SCL from the source is connected directly to the SDA/SCL pins. The TDP158 needs the SDA\_SNK and SCL\_SNK pins connected to the sink DDC pins so that the TMDS\_CLOCK\_RATIO\_STATUS bit can be automatically set; otherwise, it will have to be set through I<sup>2</sup>C. For best noise immunity, the SDA\_SRC and SCL\_SRC pins should be connected to GND. Care must be taken when this configuration is being implemented as the voltage level for DDC between the source and sink may be different, 3.3V versus 5V.

### 7.5 Register Maps

The TDP158 local I<sup>2</sup>C interface is enabled when I<sup>2</sup>C\_EN is high. The SCL\_CTL and SDA\_CTL terminals are used for I<sup>2</sup>C clock and data respectively. The TDP158 I<sup>2</sup>C interface conforms to the two-wire serial interface defined by the I<sup>2</sup>C Bus Specification, Version 2.1 (January 2000), and supports the fast mode transfer up to 400Kbps. The device address byte is the first byte received following the START condition from the controller device. The 7 bit device address for TDP158 decides by the combination of A0/EQ1 and A1/EQ2. 表 7-6 provides the TDP158 target address.

表 7-6. TDP158 I2C Device Address Description

A1/A0	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (W/R)	HEX
00	1	0	1	1	1	1	0	0/1	BC/BD
01	1	0	1	1	1	0	1	0/1	BA/BB
10	1	0	1	1	1	0	0	0/1	B8/B9
11	1	0	1	1	0	1	1	0/1	B6/B7

The local I<sup>2</sup>C is 5-V tolerant, and no additional circuitry required. Local I<sup>2</sup>C buses run at 400kHz supporting fast-mode I<sup>2</sup>C operation.

The following procedure is followed to write to the TDP158 I<sup>2</sup>C registers:

1. The controller initiates a write operation by generating a start condition (S), followed by the TDP158 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The TDP158 acknowledges the address cycle.
3. The controller presents the sub-address (I<sup>2</sup>C register within TDP158) to be written, consisting of one byte of data, MSB-first.
4. The TDP158 acknowledges the sub-address cycle.
5. The controller presents the first byte of data to be written to the I<sup>2</sup>C register.
6. The TDP158 acknowledges the byte transfer.
7. The controller may continue presenting additional bytes of data to be written, with each byte transfer completing with an acknowledge from the TDP158.
8. The controller terminates the write operation by generating a stop condition (P).

The following procedure is followed to read the TDP158 I<sup>2</sup>C registers:

1. The controller initiates a read operation by generating a start condition (S), followed by the TDP158 7-bit address and a one-value “W/R” bit to indicate a read cycle.
2. The TDP158 acknowledges the address cycle.
3. The TDP158 transmit the contents of the memory registers MSB-first starting at register 00h.
4. The TDP158 will wait for either an acknowledge (ACK) or a not-acknowledge (NACK) from the controller after each byte transfer; the I<sup>2</sup>C controller acknowledges reception of each data byte transfer.
5. If an ACK is received, the TDP158 transmits the next byte of data.
6. The controller terminates the read operation by generating a stop condition (P).

#### 注

Upon reset, the TDP158 sub-address will always be set to 0x00. When no sub-address is included in a read operation, the TDP158 sub-address will increment from previous acknowledged read or write data byte. If it is required to read from a sub-address that is different from the TDP158 internal sub-address, a write operation with only a sub-address specified is needed before performing the read operation.

Refer to [セクション 7.5.1](#) for TDP158 local I<sup>2</sup>C register descriptions. Reads from reserved fields or addresses that are not specified return zeros. The value written to reserved fields must match the value read from the reserved field to not impact device features or performance.

#### 7.5.1 Local I<sup>2</sup>C Control BIT Access TAG Convention

Reads from reserved fields shall return zero, and writes to read-only reserved registers shall be ignored. Writes to reserved register which are marked with ‘W’ will produce unexpected behavior. All addresses not defined by this specification shall be considered reserved. Reads from these addresses shall return zero and writes shall be ignored.

#### 7.5.2 BIT Access Tag Conventions

A table of bit descriptions is typically included for each register description that indicates the bit field name, field description, and the field access tags. The field access tags are provided in [表 7-7](#).

**表 7-7. Field Access Tags**

Access Tag	Name	DESCRIPTION
R	Read	The field shall be read by software
W	Write	The field shall be written by software
S	Set	The field shall be set by a write of one. Writes of Zero to the field have no effect
C	Clear	The field shall be cleared by a write of one. Writes of Zero to the field have no effect
U	Update	Hardware may autonomously update this field
NA	No Access	Not accessible or not applicable

### 7.5.3 CSR Bit Field Definitions, DEVICE\_ID (address = 00h≐07h)

図 7-8. DEVICE\_ID

7	6	5	4	3	2	1	0
DEVICE_ID							
R							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-8. DEVICE\_ID Field Descriptions

Bit	Field	Type	Default	Description
7:0		R		These fields return a string of ASCII characters "TDP158" followed by one space characters TDP158: Address 0x00 – 0x07 = {- 0x54"T", 0x44"D", 0x50"P", 0x31"1", 0x35"5", 0x38"8, 0x20, 0x20

### 7.5.4 CSR Bit Field Definitions, REV\_ID (address = 08h )

図 7-9. REV\_ID Field Descriptions

7	6	5	4	3	2	1	0
REV_ID							
R							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-9. REV\_ID

Bit	Field	Type	Default	Description
7:0	REV_ID	R	00000001	This field identifies the device revision. 00000001 – TDP158 Revision

### 7.5.5 CSR Bit Field Definitions – MISC CONTROL 09h (address = 09h)

図 7-10. MISC CONTROL 09h Field Descriptions

7	6	5	4	3	2	1	0
LANE_SWAP	Lane Control	DP-Mode	SIG_EN	PD_EN	HPD_AUTO_P WRDWN_DISA BLE	I2C_DR_CTL	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-10. MISC CONTROL 09h

Bit	Field	Type	Default	Description
7	LANE_SWAP	R/W	1'b0	This field Swaps the input lanes as per 図 7-4 and セクション 7.3.4 and valid when in HDMI mode only. 0 – Disable (default) No Lane Swap 1 – Enable: Swaps both Input and Output Lanes
6	Lane Control	R/W	1'b0	See セクション 7.3.3 0 – Global (Default) 1 – Independent Note: In default mode reg0C and reg0D control all lanes. When set to 1 each lane can be individually controlled for Swing, EQ, Pre-emphasis.

表 7-10. MISC CONTROL 09h (続き)

Bit	Field	Type	Default	Description
5	DP-Mode	R/W	1'b0	See <a href="#">セクション 7.3.12</a> 0 – Normal DP158 Operation (Default) 1 – All lanes behave as data lanes and full control through I2C only
4	SIG_EN	R/W	1'b1	This field enables the clock lane activity detect circuitry. See <a href="#">セクション 7.3.7</a> 0 – Disable Clock detector circuit closed and receiver always works in normal operation. 1 – Enable (default), Clock detector circuit will make the receiver automatically enter the standby state when no valid data detect.
3	PD_EN	R/W	1'b0	0 – Normal working (default) 1 – Forced Power down by I2C, Lowest Power state
2	HPD_AUTO_PWRDWN_DISABL	R/W	1'b0	0 – Automatically enters Power Down mode based on HPD_SNK (default) 1 – Will not automatically enter Power Down mode
1:0	I2C_DR_CTL	R/W	2'b10	I2C data rate supported for configuring device. 00 – 5Kbps 01 – 10Kbps 10 – 100Kbps( Default ) 11 – 400Kbps

## 7.5.6 CSR Bit Field Definitions – MISC CONTROL 0Ah (address = 0Ah)

図 7-11. MISC CONTROL 0Ah Field Descriptions

7	6	5	4	3	2	1	0
Reserved	HPDSNK_GATE_EN	Reserved				SLEW_CTL_DATA	
R	R/W	R				R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-11. MISC CONTROL 0Ah

Bit	Field	Type	Default	Description
7	Reserved	R	1'b0	Reserved
6	HPDSNK_GATE_EN	R/W	1'b0	The field set the HPD_SNK signal pass through to HPD_SRC or not and HPD_SRC whether held in the de-asserted state. 0 – HPD_SNK passed through to the HPD_SRC (default) 1 – HPD_SNK will not pass through to the HPD_SRC.
5:2	Reserved	R	4'b0000	Reserved
1:0	SLEW_CTL_DATA	R/W	2'b11	See <a href="#">セクション 7.3.10</a> 00 – Slowest $\cong$ 110 01 – Mid-Range 1 $\cong$ 95 10 – Mid-Range 2 $\cong$ 80ps 11 – Fastest (Default) $\cong$ 60ps Values are typical

## 7.5.7 CSR Bit Field Definitions – MISC CONTROL 0Bh (address = 0Bh)

図 7-12. MISC CONTROL 0Bh Field Descriptions

7	6	5	4	3	2	1	0
SLEW_CTL_CLK	Reserved	TERM	DDC_DR_SEL	TMDS_CLOCK_RATIO_STATUSES	DDC_TRAIN_SETDISABLE		
R/W	R	R/W	R/W	R/W/U	R/W	R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-12. MISC CONTROL 0Bh

Bit	Field	Type	Reset	Description
7:6	SLEW_CTL_CLK	R/W	2'b01	See <a href="#">セクション 7.3.10</a> 00 – Slowest $\approx$ 215ps 01 – Mid-Range 1 (Default) $\approx$ 185ps 10 – Mid-Range 2 $\approx$ 155ps 11 – Fastest $\approx$ 125ps Values are typical
5	Reserved	R	1'b0	Reserved
4:3	TERM	R/W	2'b10	Controls termination for HDMI TX. See <a href="#">セクション 7.3.8</a> 00 – 150 to 300 $\Omega$ 01 – No termination 10 – Follows TMDS_CLOCK_RATIO_STATUS bit (default). When = 1 termination value is 75 to 150 $\Omega$ : When = 0 No termination 11 – 75 to 150 $\Omega$ : Note: When TMDS_CLOCK_RATIO_STATUS bit reg0Bh[1] = 1 this register will automatically be set to 11 for 75 to 150 $\Omega$ but can be overwritten using this address
2	DDC_DR_SEL	R/W	1'b0	Defines the DDC output speed for DDC bridge 0 – 100Kbps (default) 1 – 400Kbps
1	TMDS_CLOCK_RATIO_STATUS	R/W/U	1'b0	This field is updated from snoop of I2C write to target address 0xA8 offset 0x20 bit 1 that occurred on the SDA_SRC/SCL_SRC interface. When bit 1 of address 0xA8 offset 0x20 is written to a 1'b1 or read as a 1'b1, then this field will be set to a 1'b1. When bit 1 of address 0xA8 offset 0x20 is written to a 1'b0, then this field will be set to a 1'b0. This field is reset to default value whenever HPD_SNK is de-asserted for greater than 2 ms. The main function of this bit is to automatically set the proper TX termination when value = 1. 0 – HDMI 1.4b (default) 1 – HDMI 2.0 Note 1. When DDC_TRAIN_SETDISABLE is 1'b0 this bit will reflect the value of the DDC snoop. Note 2. When DDC_TRAIN_SETDISABLE is 1'b1 this bit is set by I2C and DDC snoop is ignored. If this bit was set to 1 during snoop prior to the DDC_TRAIN_SETDISABLE being set to 1 it will be cleared to 0.
0	DDC_TRAIN_SETDISABLE	R/W	1'b0	This field indicate the DDC training block function status. 0 – DDC training enable (default) 1 – DDC training disable –DDC snoop disabled Note 1. When DDC_TRAIN_SETDISABLE is 1'b0 the TMDS_CLOCK_RATIO_STUATU bit will reflect the value of the DDC snoop. Note 2. When DDC_TRAIN_SETDISABLE is 1'b1, this bit is set by I2C and DDC snoop is ignored and thus automatic TERM control is ignored and must be manually set and TMDS_CLOCK_RATIO_STATUS bit will be cleared. Note 3. To go back to snoop and automatic TERM control this bit has to be cleared and TERM set back to automatic control.

### 7.5.8 CSR Bit Field Definitions – MISC CONTROL 0Ch (address = 0Ch)

図 7-13. MISC CONTROL 0Ch Field Descriptions

7	6	5	4	3	2	1	0
VSWING_DATA			VSWING_CLK			HDMI_TWPST1[1:0]	
R/W			R/W			R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-13. MISC CONTROL 0Ch

Bit	Field	Type	Reset	Description
7:5	VSWING_DATA	R/W	3'b000	Data Output Swing Control 000 – Vsadj set (default) 001 – Increase by 7% 010 – Increase by 14% 011 – Increase by 21% 100 – Decrease by 30% 101 – Decrease by 21% 110 – Decrease by 14% 111 – Decrease by 7%
4:2	VSWING_CLK	R/W	3'b000	Clock Output Swing Control: Default is set by Vsadj resistor value and the value of reg0Dh[0]. 000 – Vsadj set (default) 001 – Increase by 7% 010 – Increase by 14% 011 – Increase by 21% 100 – Decrease by 30% 101 – Decrease by 21% 110 – Decrease by 14% 111 – Decrease by 7%
1:0	HDMI _TWPST1[1:0]	R/W	2'b00	HDMI Pre-emphasis 00 – No Pre-emphasis (default) 01 – 3.5dB 10 – 6dB 11 – Reserved NOTE: See Pre-emphasis Section for 6dB explanation during normal operation supporting HDMI

## 7.5.9 CSR Bit Field Definitions, Equalization Control Register (address = 0Dh)

図 7-14. Equalization Control Register

7	6	5	4	3	2	1	0
Reserved	Data Lane Fixed EQ Values			Clock EQ Values		DIS_HDMI_2_SWG	
R	R/W			R/W			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-14. Equalization Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	1'b0	Reserved
6:3	Data Lane Fixed EQ Values	R/W	4'b0000	(Section <a href="#">セクション 7.3.6</a> and <a href="#">表 7-3</a> for values) 0000 – 0dB (default)
2:1	Clock EQ Values	R/W	2'b00	00 – 0dB (default) 01 – 1.5dB 10 – 3dB 11 – 4.5dB
0	DIS_HDMI_2_SWG	R/W	1'b0	Disables halving the clock output swing when entering HDMI 2.0 mode from TMDS_CLOCK_RATIO_STATUS. 0 – Disables TMDS_CLOCK_RATIO_STATUS control of the clock VOD so output swing is at full swing (default) 1 – Clock VOD is half of set values when TMDS_CLOCK_RATIO_STATUS states in HDMI 2.0 mode

## 7.5.10 CSR Bit Field Definitions, POWER MODE STATUS (address = 20h)

図 7-15. POWER MODE STATUS

7	6	5	4	3	2	1	0
Power Down Status Bit	Standby Status Bit	Loss of Signal Status Bit – LOS	Reserved				
R/U	R/U	R/U	R				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-15. POWER MODE STATUS Field Descriptions

Bit	Field	Type	Reset	Description
7	Power Down Status Bit	R/U	1'b0	0 – Normal Operation 1 – Device in Power Down Mode.
6	Standby Status Bit	R/U	1'b0	0 – Normal Operation 1 – Device in Standby Mode
5	Loss of Signal Status Bit – LOS	R/U	1'b0	0 – Clock present 1 – No Clock present
4:0	Reserved	R	5'b00000	Reserved

### 7.5.11 CSR Bit Field Definitions, DP-Mode and INDIVIDUAL LANE CONTROL (address = 30h)

See [セクション 7.3.12](#) and [セクション 7.3.3](#). Note: DP-Mode is valid only when DP-Mode Register P0\_Reg09[5] is set to one.

図 7-16. DP-Mode and INDIVIDUAL LANE CONTROL

7	6	5	4	3	2	1	0
Data Rate Select	Clock Lane	Lane D0	Lane D1	Lane D2	Reserved		
R/W	R/W	R/W	R/W	R/W	R/W	R	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-16. DP-Mode and INDIVIDUAL LANE CONTROL Field Descriptions

Bit	Field	Type	Reset	Description
7:6	Data Rate Select	R/W	2'b00	00 – 5.4Gbps (default) 01 – 2.7Gbps 10 – 1.62Gbps 11 – Reserved
5	Clock Lane	R/W	1'b1	0 – Disabled 1 – Enabled (default)
4	Lane D0	R/W	1'b1	0 – Disabled 1 – Enabled (default)
3	Lane D1	R/W	1'b1	0 – Disabled 1 – Enabled (default)
2	Lane D2	R/W	1'b1	0 – Disabled 1 – Enabled (default)
1:0	Reserved	R	2'b00	Reserved

### 7.5.12 CSR Bit Field Definitions, DP-Mode and INDIVIDUAL LANE CONTROL (address = 31h)

See Section [セクション 7.3.12](#) and [セクション 7.3.3](#) Note: DP-Mode is valid only when DP-Mode Register PO\_Reg09[5] is set to one.

図 7-17. DP-Mode and INDIVIDUAL LANE CONTROL

7	6	5	4	3	2	1	0
VOD Swing Adjust for CLK Lane			Pre-emphasis Adjust for CLK Lane		Reserved		
R/W			R/W		R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-17. DP-Mode and INDIVIDUAL LANE CONTROL Field Descriptions

Bit	Field	Type	Reset	Description
7:5	VOD Swing Adjust for CLK Lane	R/W	3'b000	000 – Vsadj set (default) 001 – Increase by 7% 010 – Increase by 14% 011 – Increase by 21% 100 – Decrease by 30% 101 – Decrease by 21% 110 – Decrease by 14% 111 – Decrease by 7% Note: reg09h[6] = 1 otherwise all lanes are global control.
4:3	Pre-emphasis Adjust for CLK Lane	R/W	2'b00	00 – No Pre-emphasis (default) 01 – 3.5dB Pre-emphasis. 10 – 6dB Pre-emphasis 11 – Reserved Note 1. reg09h[6] = 1 otherwise all lanes are global control. Note 2. If in HDMI mode writes will be ignored and reg09h[7] SWAP = 0. No pre-emphasis on clock.
2:0	Reserved	R/W	3'b000	Reserved

### 7.5.13 CSR Bit Field Definitions, DP-Mode and INDIVIDUAL LANE CONTROL (address = 32h)

See Section [セクション 7.3.12](#) and [セクション 7.3.3](#) Note: DP-Mode is valid only when DP-Mode Register PO\_Reg09[5] is set to one

図 7-18. DP-Mode and INDIVIDUAL LANE CONTROL

7	6	5	4	3	2	1	0
VOD Swing Adjust for D0 Lane			Pre-emphasis Adjust for D0 Lane		Reserved		
R/W			R/W		R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-18. DP-Mode and INDIVIDUAL LANE CONTROL Field Descriptions

Bit	Field	Type	Reset	Description
7:5	VOD Swing Adjust for D0 Lane	R/W	3'b000	000 – Vsadj set (default) 001 – Increase by 7% 010 – Increase by 14% 011 – Increase by 21% 100 – Decrease by 30% 101 – Decrease by 21% 110 – Decrease by 14% 111 – Decrease by 7% Note: reg09h[6] = 1 otherwise all lanes are global control.

表 7-18. DP-Mode and INDIVIDUAL LANE CONTROL Field Descriptions (続き)

Bit	Field	Type	Reset	Description
4:3	Pre-emphasis Adjust for D0 Lane	R/W	2'b00	00 – No Pre-emphasis (default) 01 – 3.5dB Pre-emphasis. 10 – 6dB Pre-emphasis 11 – Reserved Note: reg09h[6] = 1 otherwise all lanes are global control.
2:0	Reserved	R/W	3'b000	Reserved

#### 7.5.14 CSR Bit Field Definitions, DP-Mode and INDIVIDUAL LANE CONTROL (address = 33h)

See Section [セクション 7.3.12](#) and [セクション 7.3.3](#) Note: DP-Mode is valid only when DP-Mode Register PO\_Reg09[5] is set to one

図 7-19. DP-Mode and INDIVIDUAL LANE CONTROL

7	6	5	4	3	2	1	0
VOD Swing Adjust for D1 Lane			Pre-emphasis Adjust for D1 Lane			Reserved	
R/W			R/W			R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-19. DP-Mode and INDIVIDUAL LANE CONTROL Field Descriptions

Bit	Field	Type	Reset	Description
7:5	VOD Swing Adjust for D1 Lane	R/W	3'b000	000 – Vsadj set (default) 001 – Increase by 7% 010 – Increase by 14% 011 – Increase by 21% 100 – Decrease by 30% 101 – Decrease by 21% 110 – Decrease by 14% 111 – Decrease by 7% Note: reg09h[6] = 1 otherwise all lanes are global control.
4:3	Pre-emphasis Adjust for D1 Lane	R/W	2'b00	00 – No Pre-emphasis (default) 01 – 3.5dB Pre-emphasis. 10 – 6dB Pre-emphasis 11 – Reserved Note: reg09h[6] = 1 otherwise all lanes are global control.
2:0	Reserved	R/W	3'b000	Reserved

#### 7.5.15 CSR Bit Field Definitions, DP-Mode and INDIVIDUAL LANE CONTROL (address = 34h)

See Section [セクション 7.3.12](#) and [セクション 7.3.3](#) Note: DP-Mode is valid only when DP-Mode Register PO\_Reg09[5] is set to one

図 7-20. DP-Mode and INDIVIDUAL LANE CONTROL

7	6	5	4	3	2	1	0
VOD Swing Adjust for D2 Lane			Pre-emphasis Adjust for D2 Lane			Reserved	
R/W			R/W			R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**表 7-20. DP-Mode and INDIVIDUAL LANE CONTROL Field Descriptions**

Bit	Field	Type	Reset	Description
7:5	VOD Swing Adjust for D2 Lane	R/W	3'b000	000 – Vsadj set (default) 001 – Increase by 7% 010 – Increase by 14% 011 – Increase by 21% 100 – Decrease by 30% 101 – Decrease by 21% 110 – Decrease by 14% 11 – Decrease by 7% Note: reg09h[6] = 1 otherwise all lanes are global control.
4:3	Pre-emphasis Adjust for D2 Lane	R/W	2'b00	00 – No pre-emphasis (default) 01 – 3.5dB pre-emphasis 10 – 6dB pre-emphasis 11 – Reserved Note 1. reg09h[6] = 1 otherwise all lanes are global control. Note 2. If in HDMI mode writes will be ignored and reg09h[7] SWAP = 1. No pre-emphasis on clock.
2:0	Reserved	R/W	3'b000	Reserved

**7.5.16 CSR Bit Field Definitions, DP-Mode and INDIVIDUAL LANE CONTROL (address = 35h)**

See Section [セクション 7.3.12](#) and [セクション 7.3.3](#) Note: DP-Mode is valid only when DP-Mode Register PO\_Reg09[5] is set to one

**図 7-21. DP-Mode and INDIVIDUAL LANE CONTROL**

7	6	5	4	3	2	1	0
Reserved							
R							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**表 7-21. DP-Mode and INDIVIDUAL LANE CONTROL Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	Reserved	R	'h00	Reserved

**7.5.17 CSR Bit Field Definitions, DP-Mode and INDIVIDUAL LANE CONTROL (address = 4Dh)**

See Section [セクション 7.3.12](#) and [セクション 7.3.3](#) Note: DP-Mode is valid only when DP-Mode Register PO\_Reg09[5] is set to one

**図 7-22. DP-Mode and INDIVIDUAL LANE CONTROL**

7	6	5	4	3	2	1	0
Reserved							
R							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**表 7-22. DP-Mode and INDIVIDUAL LANE CONTROL Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	Reserved	R	'h00	Reserved

**7.5.18 CSR Bit Field Definitions, DP-Mode and INDIVIDUAL LANE CONTROL (address = 4Eh)**

See Section [セクション 7.3.12](#) and [セクション 7.3.3](#) Note: DP-Mode is valid only when DP-Mode Register PO\_Reg09[5] is set to one

図 7-23. DP-Mode and INDIVIDUAL LANE CONTROL

7	6	5	4	3	2	1	0
Data Lane 1 Fixed EQ Values				Data Lane 2 Fixed EQ Values			
R/W				R/W			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-23. DP-Mode and INDIVIDUAL LANE CONTROL Field Descriptions

Bit	Field	Type	Reset	Description
7:4	Data Lane 1 Fixed EQ Values	R/W	4'b0000	Section 8.3.6 and Table 8 2 for values 0000 – 0dB (default)
3:0	Data Lane 2 Fixed EQ Values	R/W	4'b0000	Section 8.3.6 and Table 8 2 for values 0000 – 0dB (default)

### 7.5.19 CSR Bit Field Definitions, DP-Mode and INDIVIDUAL LANE CONTROL (address = 4Fh)

See [セクション 7.3.12](#) and [セクション 7.3.3](#). Note: DP-Mode is valid only when DP-Mode Register P0\_Reg09[5] is set to one

図 7-24. DP-Mode and INDIVIDUAL LANE CONTROL

7	6	5	4	3	2	1	0
CLK Lane Fixed EQ Values				Data Lane 0 Fixed EQ Values			
R/W				R/W			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-24. DP-Mode and INDIVIDUAL LANE CONTROL Field Descriptions

Bit	Field	Type	Reset	Description
7:4	CLK Lane Fixed EQ Values	R/W	4'b0000	Section 8.3.6 and Table 8 2 for values 0000 – 0dB (default)
3:0	Data Lane 0 Fixed EQ Values	R/W	4'b0000	Section 8.3.6 and Table 8 2 for values 0000 – 0dB (default)

## 8 Application and Implementation

### 注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 8.1 Application Information

The TDP158 was designed to work mainly in source applications such as Blu-Ray DVD players, gaming systems, desktops, notebooks, or AVRs. The following sections provide design consideration for various types of applications.

### 8.2 Typical Application

図 8-1 shows a schematic representation of what is considered a standard implementation.

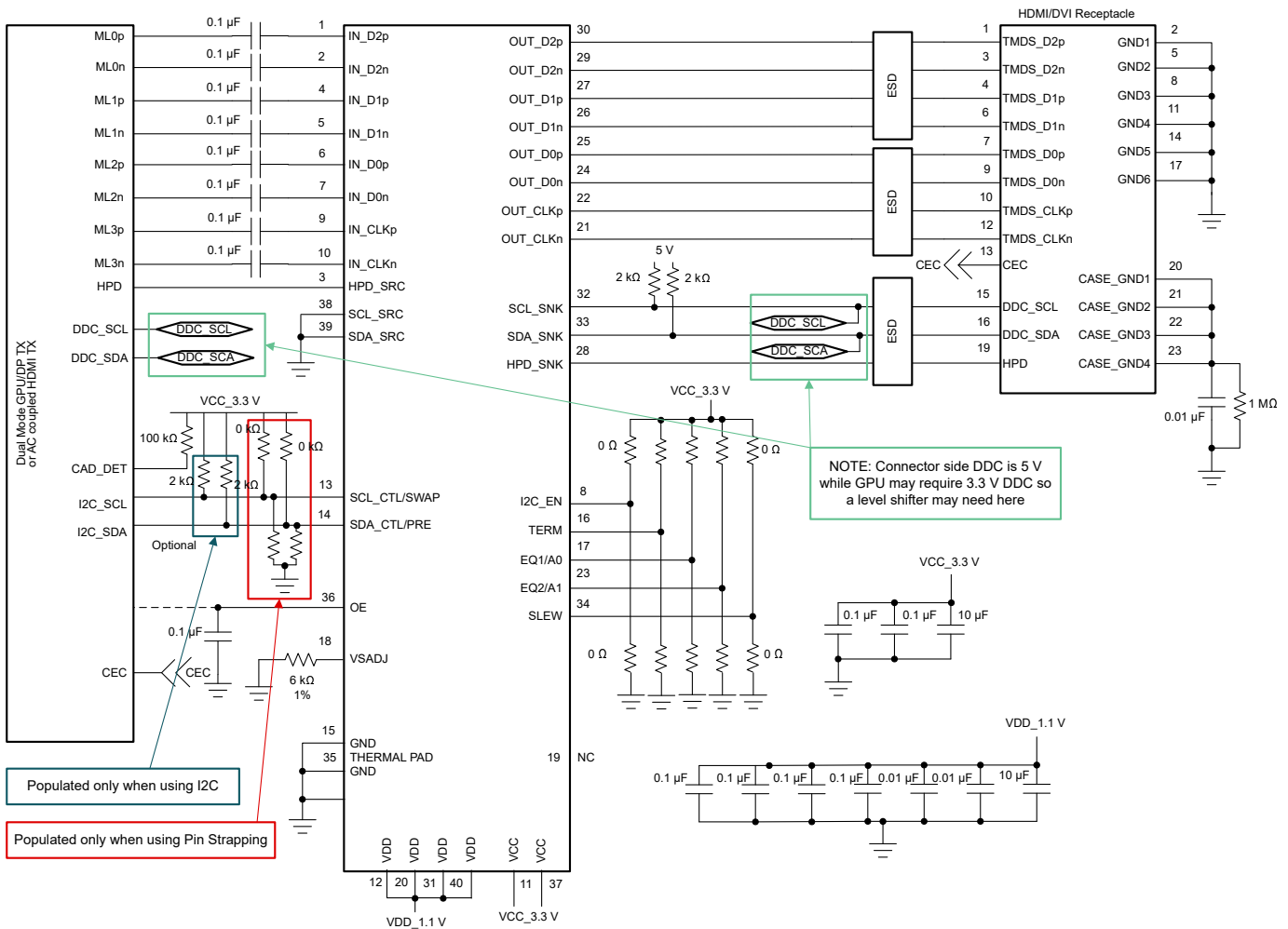


図 8-1. TDP158 in Source Side Application

## 8.2.1 Design Requirements

The TDP158 can be designed into many different applications. In all the applications there are certain requirements for the system to work properly. Two voltage rails are required to support the lowest power consumption possible. The OE pin must have a 0.1- $\mu$ F capacitor to ground. This pin can be driven by a processor but the pin needs to change states after the voltage rails have stabilized. Using the I<sup>2</sup>C is the best way to configure the device, but pin strapping is also provided as I<sup>2</sup>C, which is not available in all cases. As sources may have many different naming conventions, it is necessary to confirm that the link between the source and the TDP158 are correctly mapped. A swap function is provided for the input pins in case signaling is reversed between source and the device. The following control pin values are based upon driving pins with a microcontroller; otherwise, the shown pullup/down configuration meets the device levels. The following table provides information on the expected values to perform properly.

For this design, use the parameters provided in [表 8-1](#).

**表 8-1. Design Parameters**

Design Parameter	Value
V <sub>CC</sub>	3.3V
V <sub>DD</sub>	1.1V
Main Link Input Voltage	V <sub>ID</sub> = 0.15 to 1.4Vpp
Control Pin Max Voltage for Low	Connect to 1k $\Omega$ pulldown resistor to GND
Control Pin Voltage Range Mid	Connect to 1k $\Omega$ pulldown resistor to GND
Control Pin Min Voltage for High	Connect to 1k $\Omega$ pullup resistor to V <sub>CC</sub>
R <sub>(VSADJ)</sub> Resistor	6.49 k $\Omega$ 1%

## 8.2.2 Detailed Design Procedure

### 8.2.2.1 Source Side

The TDP158 is a signal conditioning device that provides several forms of signal conditioning to support compliance for HDMI or DVI at a source connector. These forms of signal conditioning are accomplished using receive equalization, re-timing, and output driver configurability. The transmitter will drive 1"– 2" of board trace and connector when compliance is required at the connector.

To design in the TDP158 the following need to be understood for a source side application:

- Determine the loss profile between the GPU/chipset and the HDMI /DVI connector.
- Based upon this loss profile and signal swing determine optimal location for the TDP158, to pass source electrical compliance. Usually within 1"– 2" of the connector.
- Use the typical application [図 8-1](#) for information on control pin resistors.
- The TDP158 has a receiver equalizer but can also be configured using EQ1 and EQ2 control pins.
- Set the V<sub>OD</sub>, pre-emphasis, termination, and edge rate levels appropriately to support compliance by using the appropriate VSADJ resistor value and setting SDA\_CTL/PRE, TERM and SLEW control pins.
- The thermal pad must be connected to ground.
- See schematics in [図 8-1](#) on recommended decouple caps from V<sub>CC</sub> pins to ground.

### 8.2.2.2 DDC Pull Up Resistors

This section is for information only and subject to change depending upon system implementation. The pull-up resistor value is determined by two requirements:

1. The maximum sink current of the I<sup>2</sup>C buffer:

The maximum sink current is 3mA or slightly higher for an I<sup>2</sup>C driver supporting standard-mode I<sup>2</sup>C operation.

$$R_{UP (min)} = \frac{V_{CC}}{I_{sink}} \quad (1)$$

2. The maximum transition time on the bus:

The maximum transition time, T, of an I<sup>2</sup>C bus is set by an RC time constant, where R is the pull-up resistor value, and C is the total load capacitance. The parameter, k, can be calculated from 式 3 by solving for t, the times at which certain voltage thresholds are reached. Different input threshold combinations introduce different values of t. 表 8-2 provides the possible values of k under different threshold combinations.

$$T = k \times RC \quad (2)$$

$$V(t) = V_{DD} \times \left(1 - e^{-\frac{t}{RC}}\right) \quad (3)$$

**表 8-2. Value k Upon Different Input Threshold Voltages**

V <sub>th</sub> -V <sub>th+</sub>	0.7V <sub>CC</sub>	0.65V <sub>CC</sub>	0.6V <sub>CC</sub>	0.55V <sub>CC</sub>	0.5V <sub>CC</sub>	0.45V <sub>CC</sub>	0.4V <sub>CC</sub>	0.35V <sub>CC</sub>	0.3V <sub>CC</sub>
0.1V <sub>CC</sub>	1.0986	0.9445	0.8109	0.6931	0.5878	0.4925	0.4055	0.3254	0.2513
0.15V <sub>CC</sub>	1.0415	0.8873	0.7538	0.6360	0.5306	0.4353	0.3483	0.2683	0.1942
0.2V <sub>CC</sub>	0.9808	0.8267	0.6931	0.5754	0.4700	0.3747	0.2877	0.2076	0.1335
0.25V <sub>CC</sub>	0.9163	0.7621	0.6286	0.5108	0.4055	0.3102	0.2231	0.1431	0.0690
0.3V <sub>CC</sub>	0.8473	0.6931	0.5596	0.4418	0.3365	0.2412	0.1542	0.0741	

From 式 1,  $R_{up(min)} = 5.5V/3mA = 1.83k\Omega$  to operate the bus under a 5-V pull-up voltage and provide less than 3mA when the I<sup>2</sup>C device is driving the bus to a low state. If a higher sink current, for example 4mA, is allowed,  $R_{up(min)}$  can be as low as 1.375kΩ.

If DDC working at standard mode of 100Kbps, the maximum transition time T is fixed, 1 μs, and using the k values provided in 表 8-2, then the recommended maximum total resistance of the pull-up resistors on an I<sup>2</sup>C bus can be calculated for different system setups. If DDC working in fast mode of 400Kbps, the transition time should be set at 300 ns according to I<sup>2</sup>C specification.

To support the maximum load capacitance specified in the HDMI specification,  $C_{(cable)}(max) = 700$  pF,  $C_{(source)} = 50$  pF,

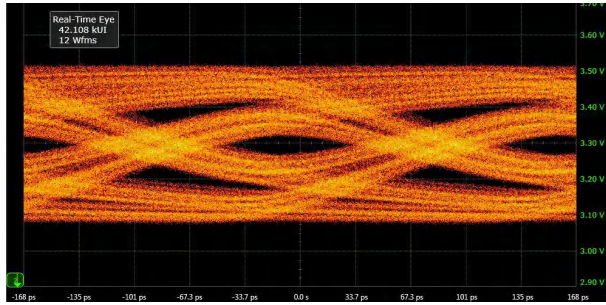
$C_1 = 50$  pF,  $R(max)$  can be calculated as provided in 表 8-3.

**表 8-3. Pull-Up Resistor Upon Different Threshold Voltages and 800-pF Loads**

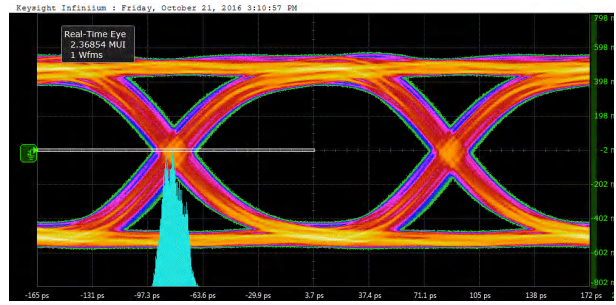
V <sub>th</sub> -V <sub>th+</sub>	0.7V <sub>CC</sub>	0.65V <sub>CC</sub>	0.6V <sub>CC</sub>	0.55V <sub>CC</sub>	0.5V <sub>CC</sub>	0.45V <sub>CC</sub>	0.4V <sub>CC</sub>	0.35V <sub>CC</sub>	0.3V <sub>CC</sub>	UNIT
0.1V <sub>CC</sub>	1.14	1.32	1.54	1.8	2.13	2.54	3.08	3.84	4.97	kΩ
0.15V <sub>CC</sub>	1.2	1.41	1.66	1.97	2.36	2.87	3.59	4.66	6.44	kΩ
0.2V <sub>CC</sub>	1.27	1.51	1.8	2.17	2.66	3.34	4.35	6.02	9.36	kΩ
0.25V <sub>CC</sub>	1.36	1.64	1.99	2.45	3.08	4.03	5.6	8.74	18.12	kΩ
0.3V <sub>CC</sub>	1.48	1.8	2.23	2.83	3.72	5.18	8.11	16.87	—	kΩ

To accommodate the 3-mA drive current specification, a narrower threshold voltage range is required to support a maximum 800-pF load capacitance for a standard-mode I<sup>2</sup>C bus.

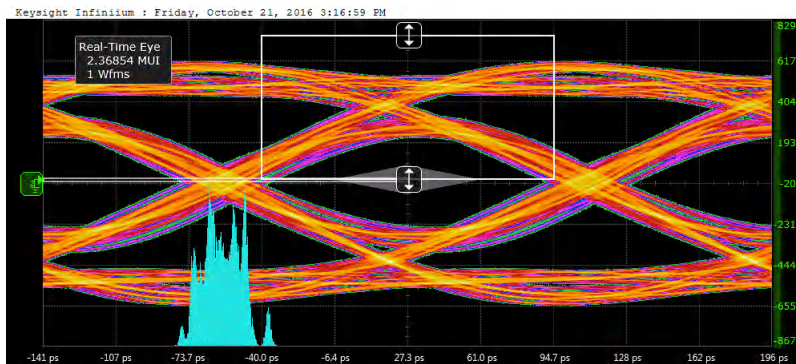
### 8.2.3 Application Curves



**8-2. High Loss Input Eye –20” 4 mil Trace at TDP158 Pin**



**8-3. Output Eye from High Loss Input Eye at TDP158 Pin**



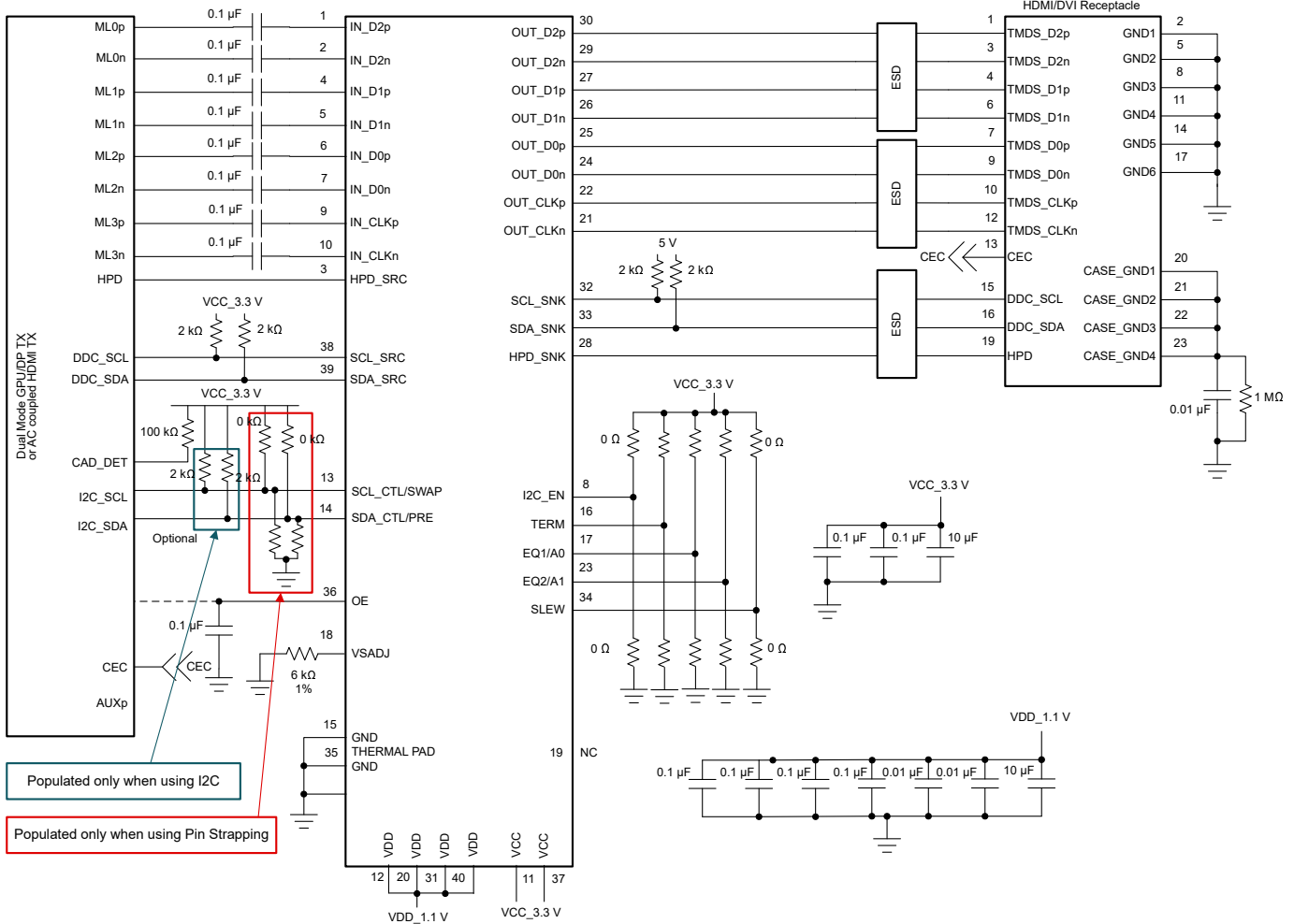
**8-4. HDMI 2 Compliance Eye from High Loss Input Eye**

## 8.2.4 Application with DDC Snoop

### 8.2.4.1 Source Side HDMI Application

In source side applications, the TDP158 takes an AC-coupled HDMI signal and provides signal conditioning and level shifting to support TMDS signaling. [Figure 8-5](#) provides an example of a DDC snoop version. Notes in both schematics provide important system design considerations. To help reduce overall EMI in a system the VCC and VDD decoupling capacitors need to be as close to the pins as possible. The drawings shown one set but multiple sets may be needed for each pin.

Control pins should be tied to 1kΩ pullup to VCC, 1kΩ pulldown to GND, or left floating. Drawings show 0Ω resistors as this provides flexibility. In noisy systems a 0.1-μF capacitor to GND may reduce glitches on these pins and are not shown in the drawings. As [Figure 8-5](#) shows, connect the DDC source and sink pins to GND as the SCL/SDA\_SRC if an application requires the DDC source and sink pins to be completely bypassed. If this is done, then the TX termination must be controlled by the TERM pin or through I<sup>2</sup>C.

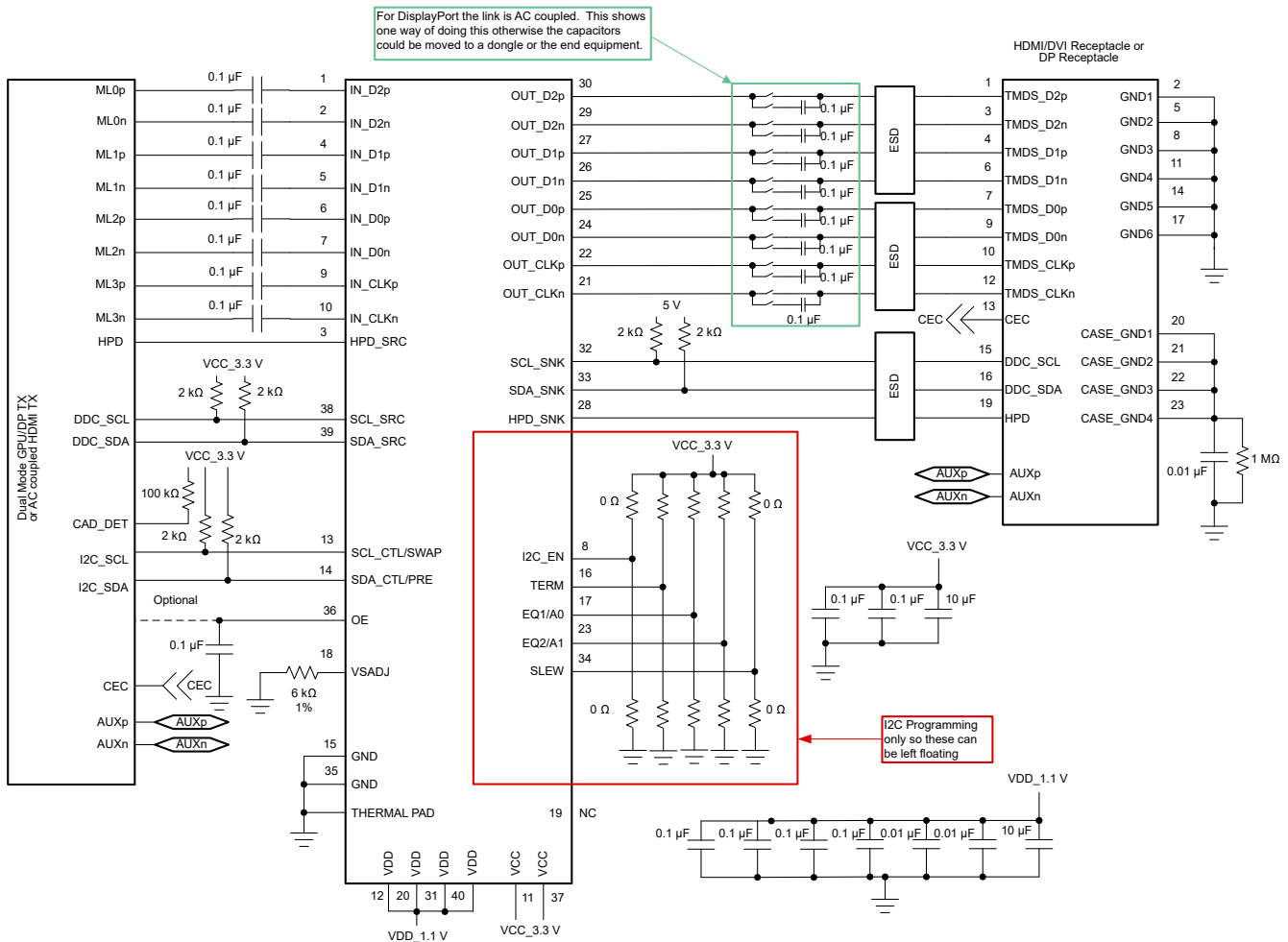


**Figure 8-5. TDP158 Source Side Application with DDC Snoop**

### 8.2.5 9.1.2 Source Side HDMI /DP Application Using DP-Mode

The TDP158 has a special mode that will allow the device to support either HDMI or DP applications. The device is put into this mode by setting reg09h[5] to 1. The device will self-configure with the following settings and become I<sup>2</sup>C programmable only. The TDP158 does not support automatic Link Training for DisplayPort. AUX channel bypasses device.

- All four lanes are turned on and configured for 5.4Gbps data rate.
- Sets V<sub>OD</sub> swing to  $\approx 410\text{mV}$  (This value is based upon a VSADJ value of 6k $\Omega$ ).
- Reg0Ch[7:5] is used to control VOD swing for all lanes.
- Reg0Ch[1:0] is used to control pre-emphasis for all lanes.
- Reg30h[7:2] is used to turn on or off individual lanes as well as informing the TDP158 what the data rate is. This is used for the delay component for pre-emphasis signal.



8-6. TDP158 in Dual Role Source Side Application

## 8.3 Power Supply Recommendations

### 8.3.1 Power Management

To minimize the power consumption of customer application, TDP158 used the dual power supply. V<sub>CC</sub> is 3.3V with 10% range to support the I/O voltage. The V<sub>DD</sub> is 1.1V with  $\approx 5\%$  range to supply the internal digital control circuit. TDP158 operates in 3 different working states.

- Power Down mode:

- When OE = Low, the device will put itself into the lowest power state by shutting down all function blocks.
  - OE re-asserted means the pin transitions from low to high. Transitioning the OE pin from L → H creates a reset. If the device is programmed through I<sup>2</sup>C, then it must be reprogrammed.
- Writing a 1 to register 09h[3].
- OE = High, HPD\_SNK = Low for > 2 ms
- Standby mode:
  - HPD\_SNK = High but no valid clock signal detect on clock lane.
- Normal operation:
  - When HPD assert, the device output will enable based on the signal detector circuit result.
  - HPD\_SRC = HPD\_SNK in all conditions. The HPD channel operational when V<sub>CC</sub> over 3V.

---

注

When the TDP158 is put into a power down state the I<sup>2</sup>C registers are cleared. This is important as the TMDS\_CLOCK\_RATIO\_STATUS bit will be cleared. If cleared and HDMI 2.0 resolutions are to be supported the TDP158 expects the source to write a 1 to this bit location. If the read has the bit set, the TDP158 will set this bit; otherwise, the source termination must be set manually.

---

### 8.3.2 Standby Power

The TDP158/I implement a two stage standby power process.

Stage 1: If there is no signal on the clock line, then the maximum I<sub>VCC</sub> ≅ 7mA and maximum I<sub>VDD</sub> ≅ 7mA.

Stage 2: If a signal (like a noise or clock signal) is on the clock line, then the TDP158 investigates the clock line for 3 μs to 5 μs and detects if a signal is present.

- If a clock is detected, then the TDP158 will go into normal operation.
- If it is determined that no clock is present, then the TDP158 will re-enter stage 1.

In stage 2; maximum I<sub>VCC</sub> ≅ 7mA and maximum I<sub>VDD</sub> ≅ 27mA.

**表 8-4. Power Modes**

INPUTS				STATUS					
OE	HPD_SNK	Reg09[2]	IN_CLK	HPD_SRC	IN_Dx	SDA/SCL_CTL	OUT_Dx OUT_CLK	DDC	Mode
L	X	X	X	H	High-Z	Disable	High-Z	Disabled	Power Down Mode
H	X	1	X	HPD_SNK	RX Active	Active	TX Active	Active	Normal operation
H	X	1	No Valid TMDS Clock	HPD_SNK	D0-D2 Disabled IN_CLK Active	Active	High-Z	Active	Standby Mode (Squelch waiting)
H	X	1	Valid TMDS Clock	HPD_SNK	RX Active	Active	TX Active	Active	Normal operation
H	H	0	No Valid TMDS Clock	HPD_SNK	D0-D2 Disabled IN_CLK Active	Active	High-Z	Active	Standby Mode (Squelch waiting)
H	H	0	Valid TMDS Clock	HPD_SNK	RX Active	Active	TX Active	Active	Normal operation

## 8.4 Layout

### 8.4.1 Layout Guidelines

For the TDP158 on a high-K board, it is required to solder the PowerPAD™ onto the thermal land to ground. A thermal land is the area of solder-tinned-copper underneath the PowerPAD™ package. On a high-K board the TDP158 can operate over the full temperature range by soldering the PowerPAD™ onto the thermal land. On a low-K board, for the device to operate across the temperature range on a low-K board, a 1-oz Cu trace connecting the GND pins to the thermal land must be used. A simulation shows R<sub>θJA</sub> = 100.84°C/W allowing 545mW power dissipation at 70°C ambient temperature. A general PCB design guide for PowerPAD packages is

provided in the document [SLMA002](#). TI recommends using a four layer stack up at a minimum to accomplish a low-EMI PCB design. TI recommends six layers as the TDP158 is a two voltage rail device.

- Routing the high-speed TMDS traces on the top layer avoids the use of vias, avoids the introduction of their inductances, and allows for clean interconnects from the HDMI connectors to the Redriver inputs and outputs. It is important to match the electrical length of these high speed traces to minimize both inter-pair and intra-pair skew.
- Placing a solid ground plane next to the high-speed single layer establishes controlled impedance for transmission link interconnects and provides an excellent low inductance path for the return current flow.
- Placing a power plane next to the ground plane creates an additional high-frequency bypass capacitance.
- Routing slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.
- If an additional supply voltage plane or signal layer is needed, add a second power/ground plane system to the stack to keep symmetry. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high frequency bypass capacitance significantly.

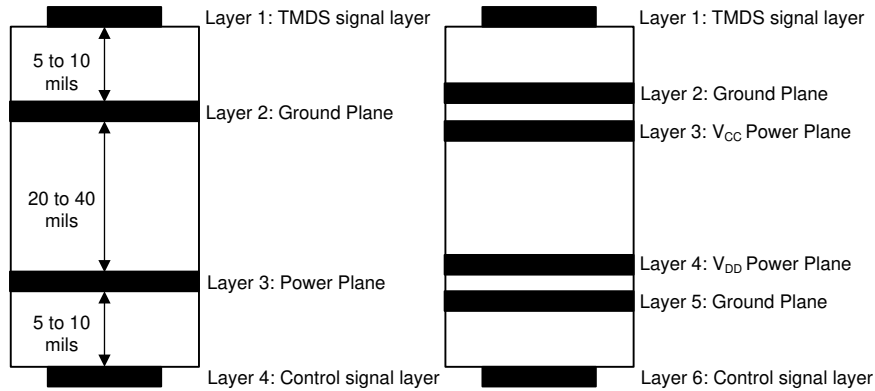
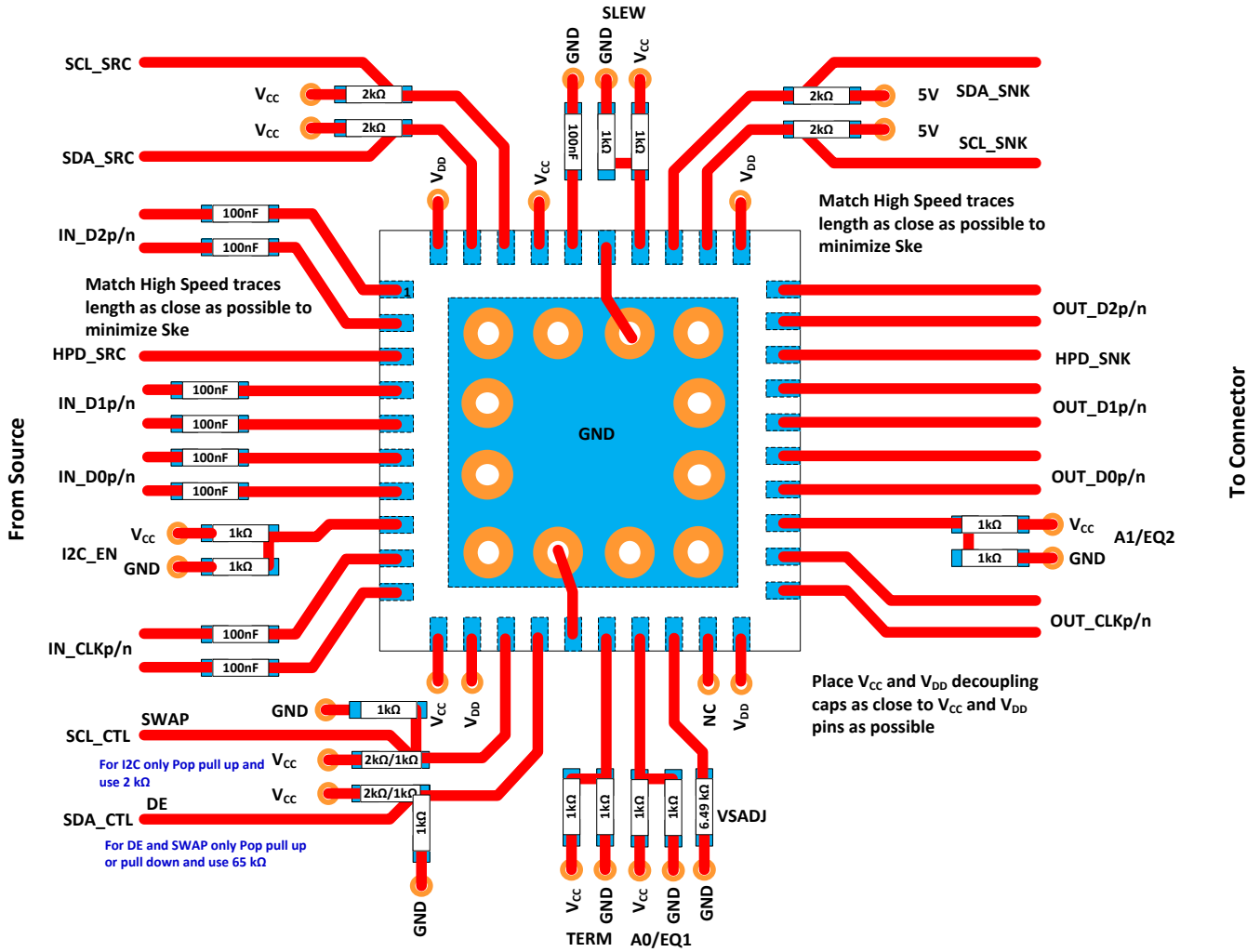


図 8-7. Recommended 4 – or 6 – Layer PCB Stack

### 8.4.2 Layout Example



The differential input lanes and differential output lanes should be separated as close to the TDP158 as feasible to minimize crosstalk. Adding a ground flood plain between each differential lane further reduces crosstalk and thus improves signal integrity at high speed data rates.

图 8-8. Example Layout for Source Side Application

## 9 Device and Documentation Support

### 9.1 Documentation Support

#### 9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [PowerPAD Thermally Enhanced Package](#)
- [HDMI ] High-definition Multimedia Interface CTS Version 1.4b October, 2011
- [HDMI ] High-definition Multimedia Interface CTS Version 2.0o June 2016
- [HDMI ] High-definition Multimedia Interface Specification Version 1.4b October, 2011
- [HDMI ] High-definition Multimedia Interface Specification Version 2.0 September 4, 2013
- [I2C] The I2C-Bus specification version 2.1 January 2000

### 9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[www.tij.co.jp](http://www.tij.co.jp) のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

### 9.3 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 9.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision E (July 2022) to Revision F (April 2024)	Page
• 「パッケージ情報」表のフォーマットを更新し、パッケージリードを追加 .....	1
• Changed $V_{DD(ramp)}$ and $V_{CC(ramp)}$ min requirement from 0.2 ms to 0.002 ms in the <i>Operation Timing</i> section	20

Changes from Revision D (March 2020) to Revision E (July 2022)	Page
ドキュメント全体にわたって表、図、相互参照の採番方法を更新.....	1
データシート全体にわたって包括的な用語を追加.....	1
Updated the <i>TDP158 in Source Side Application</i> figure with ESD between device and receptacle.....	38
Updated the <i>TDP158 Source Side Application with DDC Snoop</i> figure with ESD between device and receptacle.....	42
Updated the <i>TDP158 in Dual Role Source Side Application</i> figure with ESD between device and receptacle.....	43

Changes from Revision C (October 2019) to Revision D (March 2020)	Page
HDMI 2.0a を HDMI 2.0b に変更.....	1

Changes from Revision B (June 2017) to Revision C (October 2019)	Page
「特長」の次のセクションを削除: 拡張商業用および産業用の両方の温度のデバイス オプション.....	1
「特長」から「SN65DP159RSB および SN75DP159RSB リタイマとピン互換」を「SN75DP159RSB リタイマとピン互換」に変更.....	1
「製品情報」表から TDP158I を削除.....	1
Changed the T <sub>J</sub> MIN value From: -40°C To: 0°C in the <i>Recommended Operating Conditions</i> table.....	5
Deleted T <sub>A</sub> for TDP158I in the <i>Recommended Operating Conditions</i> table.....	5
Changed the last sentence of the <i>Overview</i> section to remove the TDP158I device.....	18

Changes from Revision A (January 2017) to Revision B (June 2017)	Page
タイトルを「HDMI™ リドライバ」から「HDMI™ レベル シフタ リドライバ」に変更.....	1
「特長」の一覧を変更.....	1
「アプリケーション」の一覧を変更.....	1
Added text to pins 17, 23, 34, 16 in the <i>Pin Functions</i> table: "For pin control, Low = 1kΩ pulldown resistor to GND, High = 1kΩ pullup resistor to VCC, NC = Floating".....	3
Added text to pin NC in the <i>Pin Functions</i> table: "Optionally connect 0.1μF to GND to reduce noise".....	3
V <sub>SADJ</sub> : Added Note "Reducing resistor ..", and Changed values in the <i>Recommended Operating Conditions</i> table.....	5
Changed R <sub>vsdj</sub> maximum value to 8kΩ in <i>VOD Swing vs VASDJ Resistor Value</i> figure.....	11
Changed the paragraph in the <i>Operation Timing</i> section.....	20
Added column Pin Number to <i>Swap Function</i> table, Changed IN_CLK → OUT_CLK To: IN_D2 → OUT_D2 in the last row of the SWAP column.....	21
Changed Note 1 of <i>Receiver EQ Programming and Values</i> table.....	22
Changed the last two sentences of the paragraph in the <i>pre-emphasis</i> section.....	25
Changed the title of <i>6dB Pre-Emphasis Setting in Normal Operation</i> figure from: 3.5dB pre-emphasis in Normal Operation to: 6dB pre-emphasis Setting in Normal Operation.....	25
Changed From: Reg0Ch[1:0] = 01 To: Reg0Ch[1:0] = 10 in <i>6dB Pre-Emphasis in DP-Mode</i> figure.....	25
Changed the Default setting in <i>REV_ID</i> From: TBD To: 00000001.....	29
Added paragraph to the <i>Application and Implementation</i> section: "TDP158 is designed ..".....	38
Changed the <i>Application Information</i> paragraph.....	38
Changed From: 0Ω resistors To: 1kΩ resistors, and a noise filter (capacitor) for the no connect in <i>Source Side Application</i> figure.....	38
Added text "1kΩ pulldown resistor " to the connect values in <i>Design Parameters</i> table.....	39
Changed text in the second paragraph of the <i>Source Side HDMI Application</i> section From: "Control pins can be tied directly to VCC, GND or left floating." To: "Control pins should be tied to 1kΩ pullup to VCC, 1kΩ pulldown to GND, or left floating.".....	42

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• Changed From: 0Ω resistors To: 1kΩ resistors, and a noise filter (capacitor) for the no connect in <i>Source Side Application with DDC Snoop</i> figure.....	42
• Changed From: 0Ω resistors To: 1kΩ resistors, and a noise filter (capacitor) for the no connect in <i>Dual Role Source Side Application</i> figure.....	43
• Changed From: 0Ω resistors To: 1kΩ resistors, and a noise filter (capacitor) for the no connect in <i>Example Layout for Source Side Application</i> figure.....	46

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**Changes from Revision \* (December 2016) to Revision A (January 2017)**
**Page**

• 以下のように変更:「プレビュー」から「量産データ」に変更.....	1
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## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TDP158RSBR</a>	Active	Production	WQFN (RSB)   40	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 85	TDP158
TDP158RSBR.A	Active	Production	WQFN (RSB)   40	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 85	TDP158
<a href="#">TDP158RSBT</a>	Active	Production	WQFN (RSB)   40	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 85	TDP158
TDP158RSBT.A	Active	Production	WQFN (RSB)   40	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 85	TDP158

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

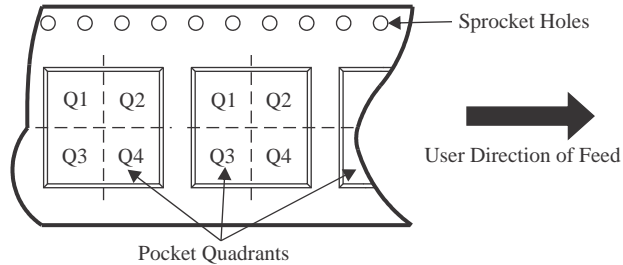
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TDP158RSBR	WQFN	RSB	40	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TDP158RSBT	WQFN	RSB	40	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TDP158RSBR	WQFN	RSB	40	3000	346.0	346.0	33.0
TDP158RSBT	WQFN	RSB	40	250	182.0	182.0	20.0

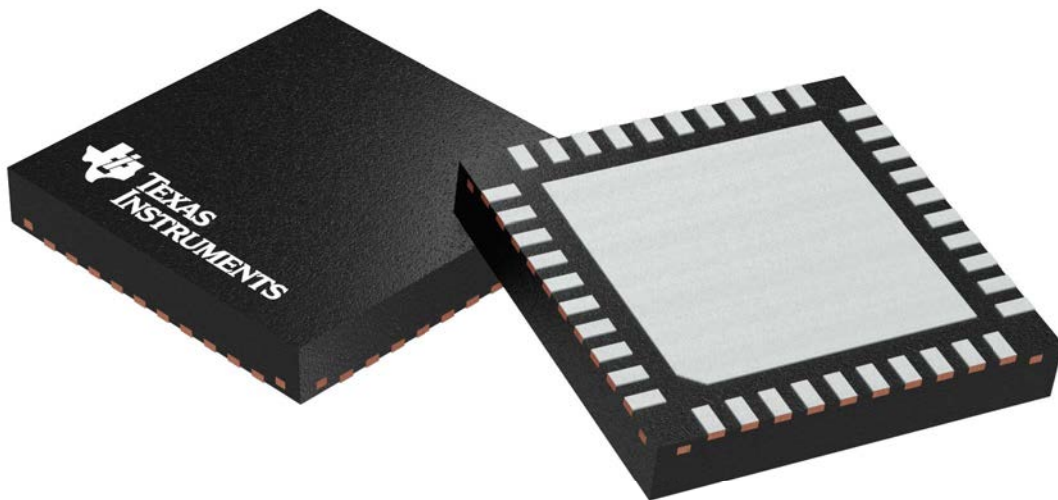
## GENERIC PACKAGE VIEW

**RSB 40**

**WQFN - 0.8 mm max height**

5 x 5 mm, 0.4 mm pitch

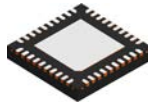
PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4207182/D

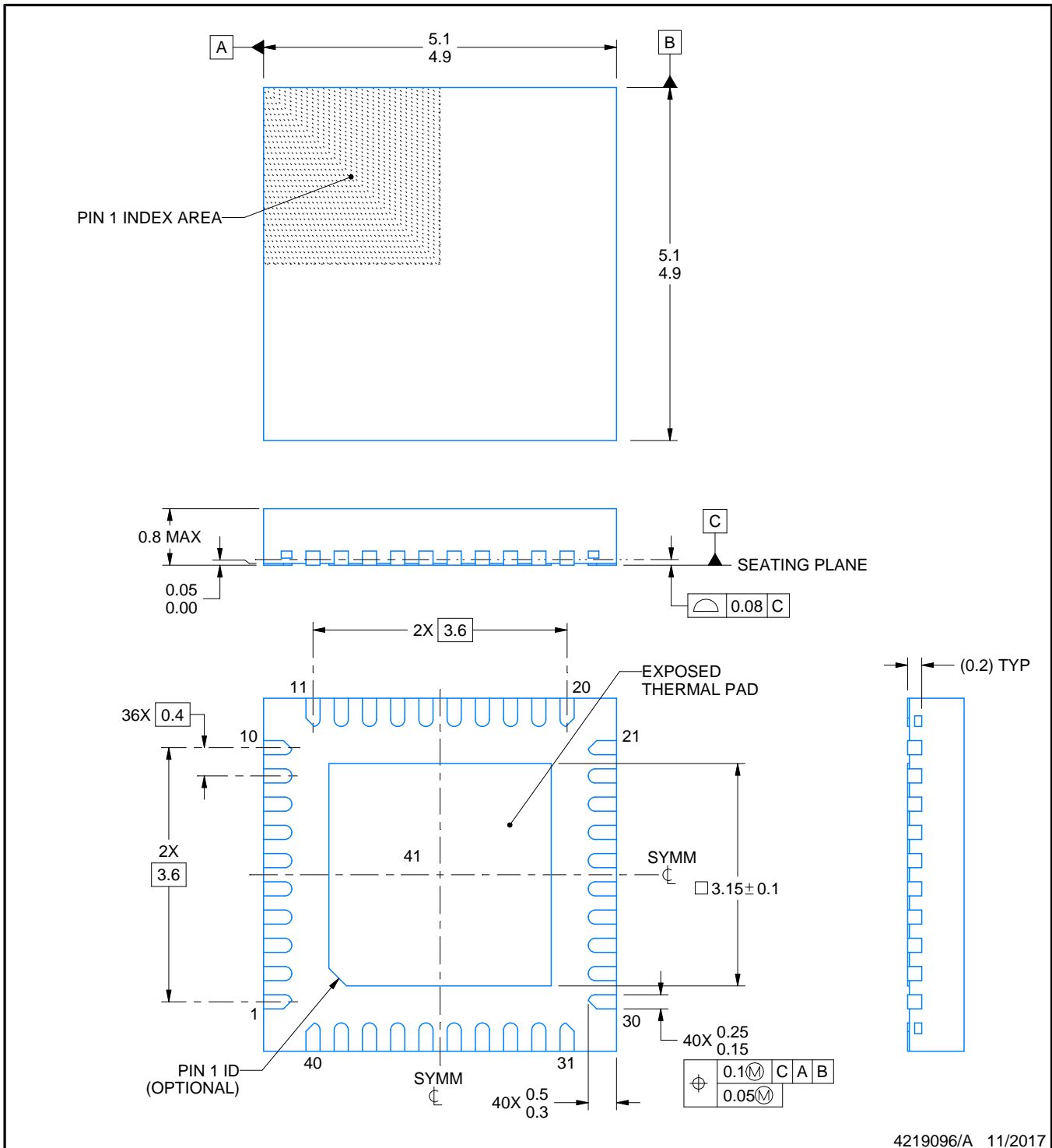
# RSB0040E



# PACKAGE OUTLINE

## WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4219096/A 11/2017

**NOTES:**

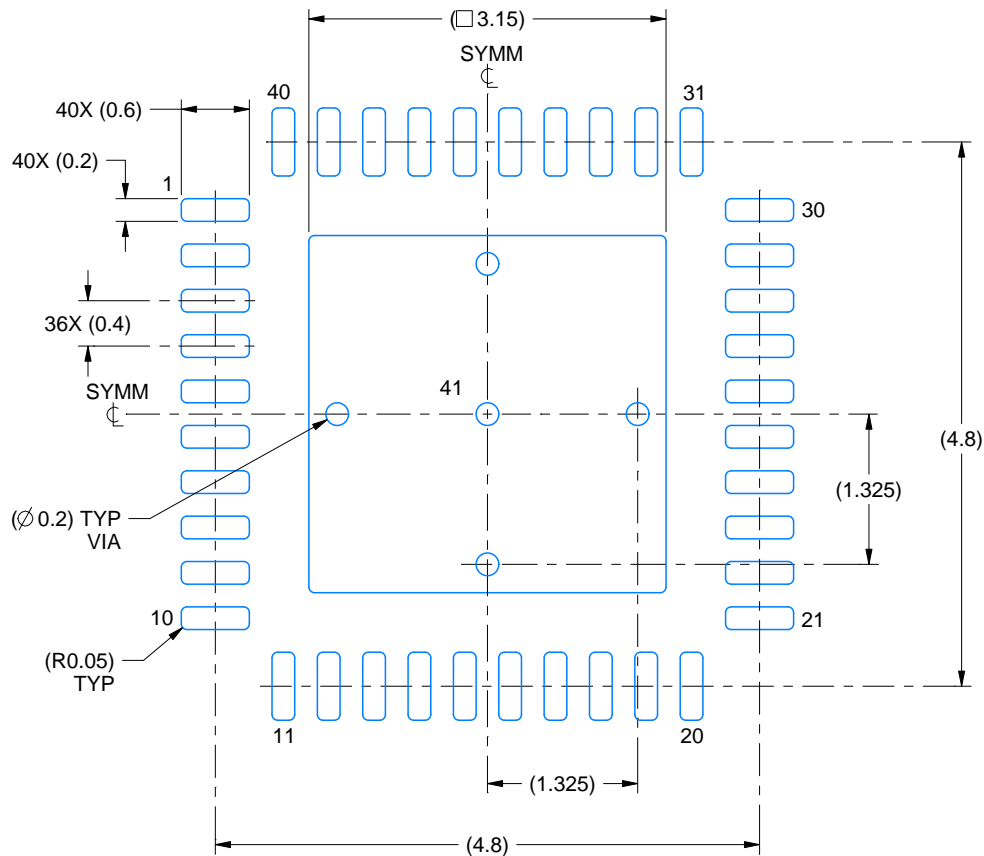
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

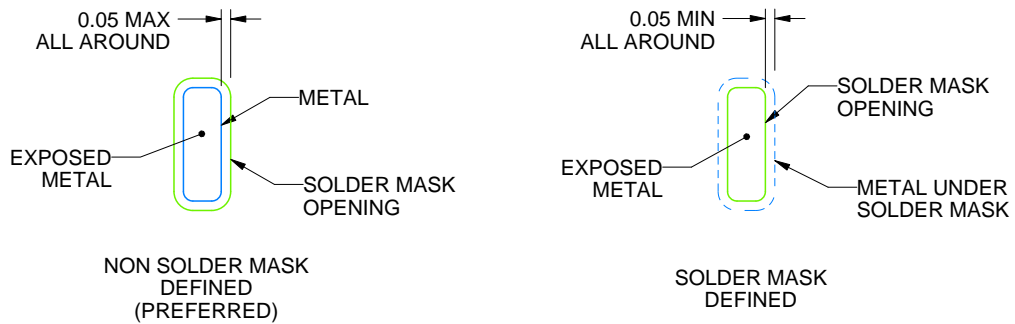
RSB0040E

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4219096/A 11/2017

NOTES: (continued)

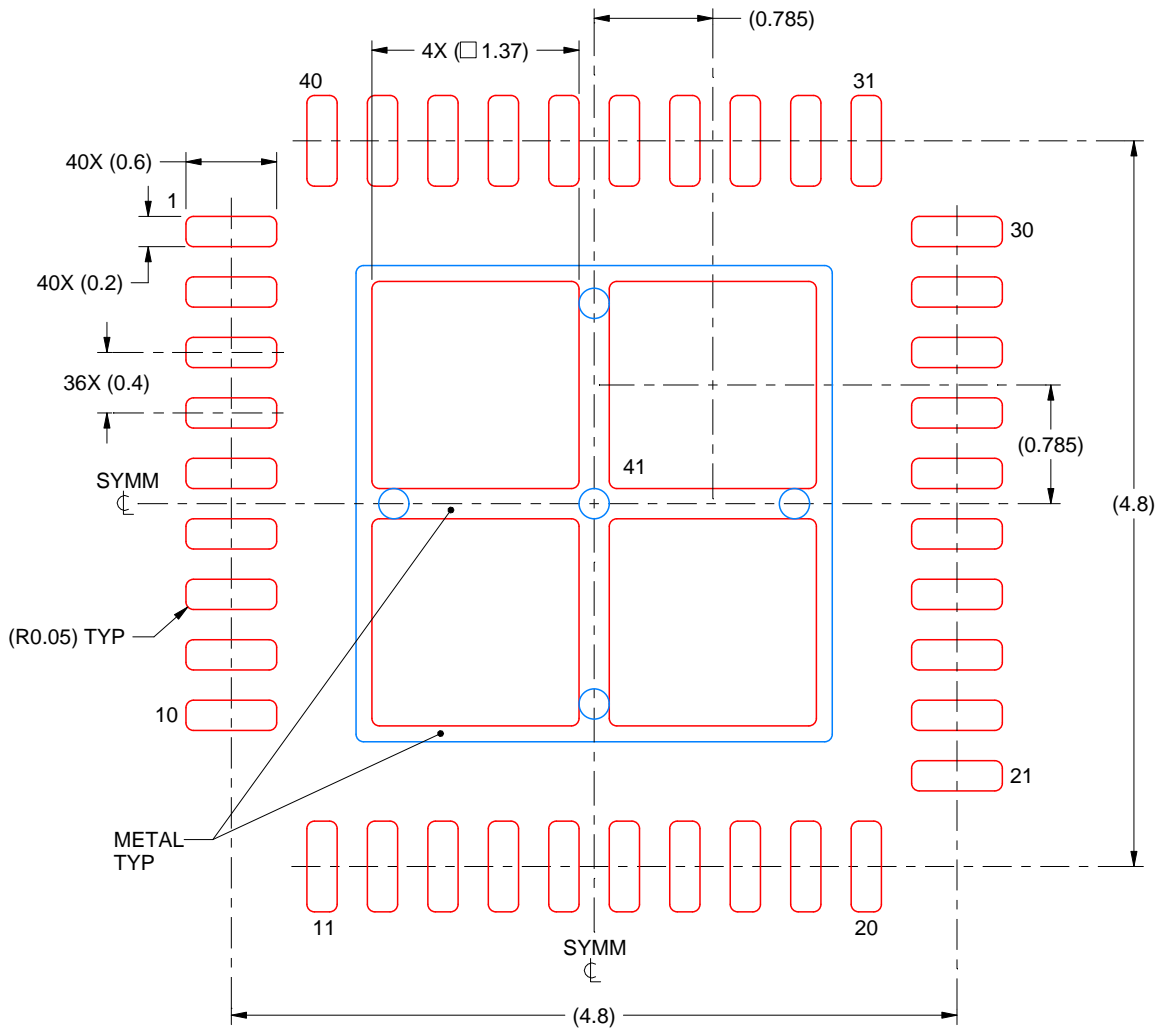
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RSB0040E

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 41  
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:20X

4219096/A 11/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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