

TDP2044 4 チャンネル 20Gbps DisplayPort 2.1 リニア リドライバ、USB Type-C 用 クロスポイント付き

1 特長

- 最大 20Gbps の DisplayPort 2.1 をサポート (UHBR20)
- クロスポイント マルチプレクサを内蔵した USB-C DP のみ (USB 3.x ではない) のソース/シンク用に設計
- 最大 20Gbps までのほとんどの AC 結合インターフェイスをサポートする、プロトコルに依存しないリニア イコライザ
- 20Gbps (10Ghz ナイキスト) での優れた電氣的性能:
 - 19dB のイコライゼーション
 - 1.8V DC の直線性、1.08V AC の直線性
 - -15/-16dB Rx/Tx リターンロス
 - -60dB の NEXT、-43dB の FEXT クロストーク
 - PRBS データによる 70fs の低付加 RJ
- DisplayPort 1.4 および 2.1 リンクトレーニングに対して透過的
- 3.3V 単一電源、チャンネルあたり 160mW のアクティブ電力
- 内部電圧レギュレータにより電源ノイズへの耐性を実現
- 高い直線性により DP コンプライアンス テストが容易
- 高い BW による優れたリニア EQ カーブ
- ピンストラップ、I²C または EEPROM プログラミング
 - 18 個の EQ ブースト設定と 5 個のフラット ゲイン 設定
- TDP2044: 0°C ~ 70°C の商業用温度範囲
- TDP2044I: -40°C ~ 85°C の産業用温度範囲
- 4mm × 6mm、40 ピン WQFN パッケージ

2 アプリケーション

- デスクトップ PC またはマザーボード
- PC、ノート PC、およびタブレット
- ドッキング・ステーション
- TV、ゲーム、ホームシアター、およびエンターテインメント
- 業務用オーディオ、ビデオ、サイネージ

- 試験 / 測定機器
- 医療用
- フラットパネル モニタ

3 概要

TDP2044 は、VESA USB Type-C™ Alt モード アプリケーションをサポートするためのクロスポイントを内蔵した 4 チャンネルの低消費電力高性能リニア リピータまたはリドライバで、最大 20Gbps の DisplayPort 2.1 をサポートするよう設計されています。

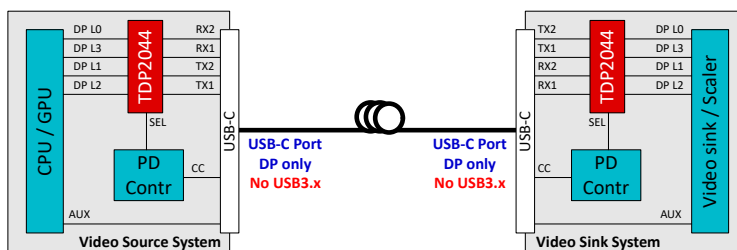
TDP2044 のレシーバは、連続時間リニア イコライザ (CTLE) を搭載し、プログラマブルな高周波数での昇圧を実現しています。イコライザは、相互接続媒体 (例: PCB 配線、ケーブル) に起因する符号間干渉 (ISI) によって完全に閉じた入力アイ パターンを開くことができます。TDP2044 のリニアなデータパスは、送信プリセット信号特性を保持します。高帯域幅で、チャンネル間クロストークが少なく、付加ジッタが小さく、反射損失特性が非常に優れた本デバイスは、便利なイコライゼーション機能を備えていることを除いて、リンク内でほとんど受動素子のように振舞います。DisplayPort リンクのトレーニングは、ソース Tx とシンク Rx の間でパッシブ チャンネルの一部となるリニア リドライバを使用して効果的に行われます。このリンク トレーニング プロトコルの透過性は、最適な電氣的リンクと最短のレイテンシをもたらします。本デバイスのデータ パスは、基板上のすべての電源ノイズに対して高い耐性を示す内部的に安定化された電源レールを使用しています。

また、このデバイスは AC および DC ゲインの変動が小さいため、大容量プラットフォームを展開する際の一貫したイコライゼーションにも対応しています。

パッケージ情報

| 部品番号 | パッケージ ⁽¹⁾ | パッケージサイズ ⁽²⁾ |
|---------|----------------------|-------------------------|
| TDP2044 | RNQ (WQFN, 40) | 4mm × 6mm |

- 詳細については、[セクション 10](#) を参照してください。
- パッケージサイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



代表的なアプリケーション



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4 Pin Configuration and Functions

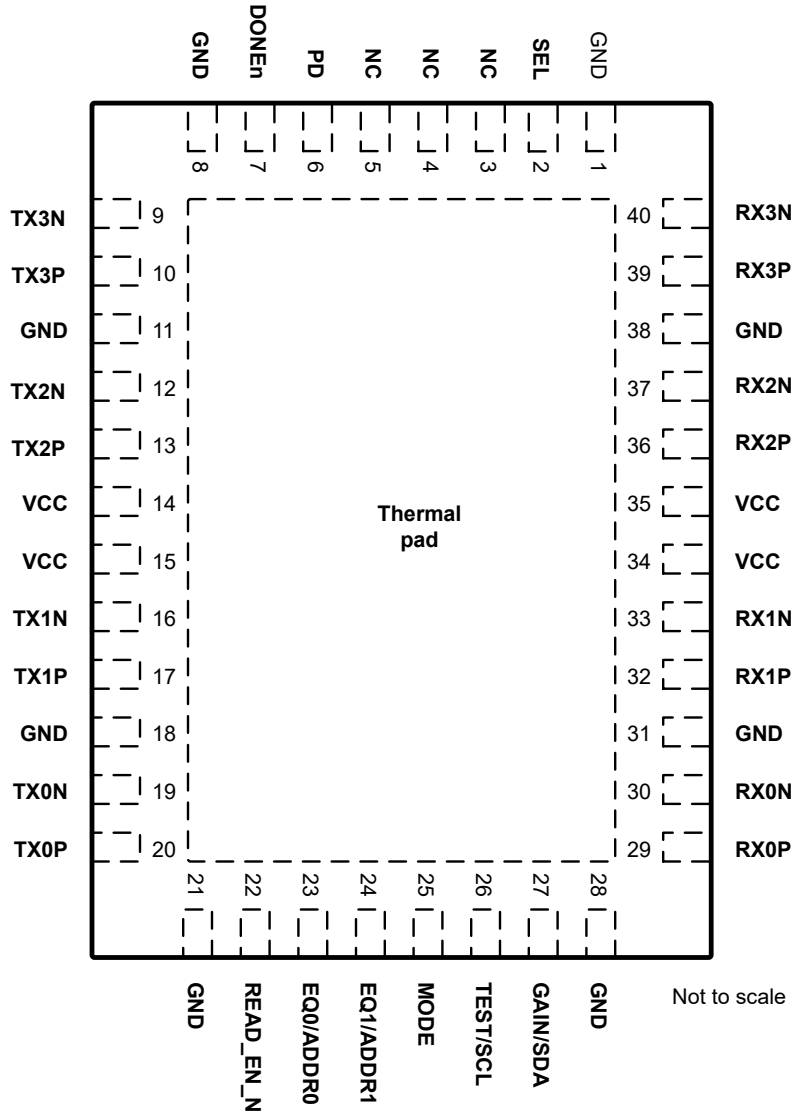


図 4-1. RNQ Package, 40-Pin WQFN (Top View)

表 4-1. Pin Functions

| PIN | | TYPE ⁽¹⁾ | DESCRIPTION |
|-------|-----|---------------------|---|
| NAME | NO. | | |
| DONEn | 7 | O, 3.3V open drain | <p>In SMBus/I²C Primary mode: Indicates the completion of a valid EEPROM register load operation. External pullup resistor such as 4.7kΩ required for operation. High: External EEPROM load failed or incomplete Low: External EEPROM load successful and complete</p> <p>In SMBus/I²C Secondary/Pin mode: This output is High-Z. The pin can be left floating.</p> |

表 4-1. Pin Functions (続き)

| PIN | | TYPE ⁽¹⁾ | DESCRIPTION |
|-------------|--|--|---|
| NAME | NO. | | |
| MODE | 25 | I, 5-level | Sets device control configuration modes. 5-level IO pin as provided in 表 6-3. The pin can be exercised at device power up or in normal operation mode. L0: Pin mode – device control configuration is done solely by strap pins. L1: SMBus/I²C Primary mode – device control configuration is read from external EEPROM. When the TDP2044 finishes reading from the EEPROM successfully, DONE pin is pulled LOW. SMBus/I ² C secondary operation is available in this mode before, during or after EEPROM reading. Note: during EEPROM reading if the external SMBus/I ² C primary wants to access TDP2044 registers, the external controller must support arbitration. L2: SMBus/I²C Secondary mode – device control configuration is done by an external controller with SMBus/I ² C primary. L3 and L4 (Float): RESERVED – TI internal test modes. |
| EQ0 / ADDR0 | 23 | I, 5-level | In Pin mode: Sets receiver linear equalization (CTLE) boost for channels 0-3 as provided in 表 6-1. These pins are sampled at device power up only. In SMBus/I²C mode: Sets SMBus / I ² C secondary address as provided in 表 6-4. These pins are sampled at device power up only. |
| EQ1 / ADDR1 | 24 | I, 5-level | |
| GAIN / SDA | 27 | I, 5-level / I/O, 3.3V LVCMOS, open drain | In Pin mode: Flat gain (DC and AC) from the input to the output of the device for channels 0-3. The pin is sampled at device power up only. In SMBus/I²C mode: 3.3V SMBus/I ² C data. External 1kΩ to 5kΩ pullup resistor is required as per SMBus / I ² C interface standard. |
| GND | 1, 8, 11, 18, 21, 28, 31, 38, EP | P | Ground reference for the device. EP: the Exposed Pad at the bottom of the QFN package, which is used as the GND return for the device. The EP must be connected to one or more ground planes through the low resistance path. A via array provides a low impedance path to GND. The EP also improves thermal dissipation. |
| PD | 6 | I, 3.3V LVCMOS | 2-level logic controlling the operating state of the redriver. Active in all device control modes. The pin has internal 1MΩ weak pulldown resistor. High: power down for channels 0-3 Low: power up, normal operation for channels 0-3 |
| READ_EN_N | 22 | I, 3.3V LVCMOS | In SMBus/I²C Primary mode: After power up, when the pin is low, the device initiates the SMBus / I ² C Primary mode EEPROM read function. When EEPROM read is complete (indicated by assertion of DONE low), this pin can be held low for normal device operation. During the EEPROM load process the signal path of the device is disabled. In SMBus/I²C Secondary and Pin modes: In these modes the pin is not used. The pin can be left floating. The pin has internal 1MΩ weak pulldown resistor. |
| SEL | 2 | I, 3.3V LVCMOS | The pin selects the mux configuration. L: straight data path – RX[0/1/2/3][P/N] connected to TX[0/1/2/3][P/N] through the redriver. H: cross data path – RX[0/1/2/3][P/N] connected to TX[1/0/3/2][P/N] through the redriver. Active in all device control modes. 59kΩ internal pulldown. |
| TEST / SCL | 26 | I, 5-level / I/O, 3.3V LVCMOS, open drain | In Pin mode: TI test mode. External 1kΩ pulldown resistor must be installed. In SMBus/I²C mode: 3.3V SMBus/I ² C clock. External 1kΩ to 5kΩ pullup resistor is required as per SMBus / I ² C interface standard. |
| RX0N | 30 | I | Inverting differential inputs to the equalizer. Integrated 50Ω termination resistor from the pin to internal CM bias voltage. Channel 0. |
| RX0P | 29 | I | Noninverting differential inputs to the equalizer. Integrated 50Ω termination resistor from the pin to internal CM bias voltage. Channel 0. |
| RX1N | 33 | I | Inverting differential inputs to the equalizer. Integrated 50Ω termination resistor from the pin to internal CM bias voltage. Channel 1. |

表 4-1. Pin Functions (続き)

| PIN | | TYPE ⁽¹⁾ | DESCRIPTION |
|------|----------------|---------------------|--|
| NAME | NO. | | |
| RX1P | 32 | I | Noninverting differential inputs to the equalizer. Integrated 50Ω termination resistor from the pin to internal CM bias voltage. Channel 1. |
| RX2N | 37 | I | Inverting differential inputs to the equalizer. Integrated 50Ω termination resistor from the pin to internal CM bias voltage. Channel 2. |
| RX2P | 36 | I | Noninverting differential inputs to the equalizer. Integrated 50Ω termination resistor from the pin to internal CM bias voltage. Channel 2. |
| RX3N | 40 | I | Inverting differential inputs to the equalizer. Integrated 50Ω termination resistor from the pin to internal CM bias voltage. Channel 3. |
| RX3P | 39 | I | Noninverting differential inputs to the equalizer. Integrated 50Ω termination resistor from the pin to internal CM bias voltage. Channel 3. |
| TX0N | 19 | O | Inverting pin for 100Ω differential driver output. Channel 0. |
| TX0P | 20 | O | Noninverting pin for 100Ω differential driver output. Channel 0. |
| TX1N | 16 | O | Inverting pin for 100Ω differential driver output. Channel 1. |
| TX1P | 17 | O | Noninverting pin for 100Ω differential driver output. Channel 1. |
| TX2N | 12 | O | Inverting pin for 100Ω differential driver output. Channel 2. |
| TX2P | 13 | O | Noninverting pin for 100Ω differential driver output. Channel 2. |
| TX3N | 9 | O | Inverting pin for 100Ω differential driver output. Channel 3. |
| TX3P | 10 | O | Noninverting pin for 100Ω differential driver output. Channel 3. |
| VCC | 14, 15, 34, 35 | P | Power supply pins. VCC = 3.3V ±10%. The VCC pins on this device must be connected through a low-resistance path to the board VCC plane. Install a decoupling capacitor to GND near each VCC pin. |

(1) I = input, O = output, P = power

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|------------------------|--|------|------|------|
| VCC_ABSMAX | Supply voltage (VCC) | -0.5 | 4.0 | V |
| VIO_CMOS_ABSMAX | 3.3V LVCMOS and open drain I/O voltage | -0.5 | 4.0 | V |
| VIO_5LVL_ABSMAX | 5-level input I/O voltage | -0.5 | 2.75 | V |
| VIO_HS-RX_ABSMAX | High-speed I/O voltage (RXnP, RXnN) | -0.5 | 3.2 | V |
| VIO_HS-TX_ABSMAX | High-speed I/O voltage (TXnP, TXnN) | -0.5 | 2.75 | V |
| T _{J,ABS} MAX | Junction temperature | | 150 | °C |
| T _{stg} | Storage temperature range | -65 | 150 | °C |

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

| | | | VALUE | UNIT |
|--------------------|-------------------------|---|-------|------|
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 | V |
| | | Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾ | ±500 | |

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2KV may actually have higher performance.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---------------------------------|---|---|-------|-----|------|------|
| VCC | Supply voltage, VCC to GND | DC plus AC power must not exceed these limits | 3.0 | 3.3 | 3.6 | V |
| N _{VCC} ⁽¹⁾ | Supply noise tolerance | DC to <50Hz, sinusoidal | | | 250 | mVpp |
| | | 50Hz to 500kHz, sinusoidal | | | 100 | mVpp |
| | | 500kHz to 2.5MHz, sinusoidal | | | 33 | mVpp |
| | | Supply noise, >2.5MHz, sinusoidal | | | 10 | mVpp |
| T _{RampVCC} | VCC supply ramp time | From 0V to 3.0V | 0.150 | | 100 | ms |
| T _A | Operating ambient temperature | TDP2044 | 0 | | 70 | °C |
| | | TDP2044I | -40 | | 85 | °C |
| T _J | Operating junction temperature | TDP2044 | | | 105 | °C |
| | | TDP2044I | | | 125 | °C |
| PW _{LVCMOS} | Minimum pulse width required for the device to detect a valid signal on LVCMOS inputs | PD, SEL, and READ_EN_N | 200 | | | µs |
| VCC _{SMBUS} | SMBus/I ² C SDA and SCL open-drain termination voltage | Supply voltage for open-drain pullup resistor | | | 3.6 | V |
| F _{SMBus} | SMBus/I ² C clock (SCL) frequency | SMBus secondary mode | 10 | | 400 | kHz |
| VID _{LAUNCH} | Source launch amplitude | Differential signaling | | | 1200 | mVpp |

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|----|-----------|-----|-----|-----|------|
| DR | Data rate | 1 | | 20 | Gbps |

- (1) Sinusoidal noise is superimposed to supply voltage with negligible impact to device function or critical performance shown in the Electrical Table. Steps must be taken to ensure the combined AC plus DC supply noise meets the specified VDD supply voltage limits.

5.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | TDP2044 | UNIT |
|-------------------------------|--|--------------|------|
| | | RNQ, 40 Pins | |
| R _{θJA} -High K | Junction-to-ambient thermal resistance | 30.7 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 20.8 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 11.4 | °C/W |
| Ψ _{JT} | Junction-to-top characterization parameter | 0.3 | °C/W |
| Ψ _{JB} | Junction-to-board characterization parameter | 11.4 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | 3.8 | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application note](#).

5.5 DC Electrical Characteristics

over operating free-air temperature and voltage range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|--|------|------|------|------|
| Power | | | | | | |
| P _{ACT} | Device active power | 4 channels active, EQ = 0-2 | | 0.57 | 0.71 | W |
| | | 4 channels active, EQ = 5-19 | | 0.69 | 0.85 | W |
| P _{STBY} | Device power consumption in standby power mode | All channels disabled (PD = H) | | 17 | 25 | mW |
| Control IO | | | | | | |
| V _{IH} | High level input voltage | SDA, SCL, PD, READ_EN_N, SEL pins | 2.1 | | | V |
| V _{IL} | Low level input voltage | SDA, SCL, PD, READ_EN_N, SEL pins | | | 1.08 | V |
| V _{OH} | High level output voltage | R _{pullup} = 4.7kΩ (SDA, SCL, DONE pins) | 2.1 | | | V |
| V _{OL} | Low level output voltage | I _{OL} = -4mA (SDA, SCL, DONE pins) | | | 0.4 | V |
| I _{IH} | Input high leakage current | V _{Input} = VCC, (SCL, SDA, PD, READ_EN_N pins) | | | 10 | μA |
| I _{IL} | Input low leakage current | V _{Input} = 0V, (SCL, SDA, PD, READ_EN_N, SEL pins) | -10 | | | μA |
| I _{IH,FS} | Input high leakage current for fail safe input pins | V _{Input} = 3.6V, VCC = 0V, (SCL, SDA, PD, READ_EN_N, SEL pins) | | | 200 | μA |
| C _{IN-CTRL} | Input capacitance | SDA, SCL, PD, READ_EN_N, SEL pins | | 1.6 | | pF |
| 5 Level IOs (MODE, GAIN, EQ0, EQ1 pins) | | | | | | |
| I _{IH_5L} | Input high leakage current, 5-level IOs | VIN = 2.5V | | | 10 | μA |
| I _{IL_5L} | Input low leakage current for all 5-level IOs except MODE. | VIN = GND | -10 | | | μA |
| I _{IL_5L,MODE} | Input low leakage current for MODE pin | VIN = GND | -200 | | | μA |
| Receiver | | | | | | |

over operating free-air temperature and voltage range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------|------------------------------|--|-----|-----|-----|------|
| V _{RX-DC-CM} | RX DC common mode voltage | Device is in active or standby state | | 1.4 | | V |
| Z _{RX-DC} | Rx DC single-ended impedance | | | 50 | | Ω |
| Transmitter | | | | | | |
| Z _{TX-DIFF-DC} | DC differential Tx impedance | Impedance of Tx during active signaling, VID,diff = 1Vpp | | 100 | | Ω |
| V _{TX-DC-CM} | Tx DC common mode voltage | | | 1.0 | | V |
| I _{TX-SHORT} | Tx short circuit current | Total current the Tx can supply when shorted to GND | | 70 | | mA |

5.6 High Speed Electrical Characteristics

over operating free-air temperature and voltage range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------|--|--|-----|------|-----|------|
| Receiver | | | | | | |
| R _{L-RX-DIFF} | Input differential return loss | 3GHz | | -19 | | dB |
| | | 4GHz | | -18 | | dB |
| | | 5GHz | | -18 | | dB |
| | | 6GHz | | -17 | | dB |
| | | 10GHz | | -15 | | dB |
| X _{T-RX} | Receiver-side pair-to-pair isolation; Port A or Port B | Minimum over 10MHz to 10GHz range | | -60 | | dB |
| Transmitter | | | | | | |
| R _{L-TX-DIFF} | Output differential return loss | 3GHz | | -19 | | dB |
| R _{L-TX-DIFF} | Output differential return loss | 4.0GHz | | -18 | | dB |
| R _{L-TX-DIFF} | Output differential return loss | 5.0GHz | | -18 | | dB |
| R _{L-TX-DIFF} | Output differential return loss | 6.0GHz | | -17 | | dB |
| R _{L-TX-DIFF} | Output differential return loss | 10GHz | | -16 | | dB |
| X _{T-TX} | Transmit-side pair-to-pair isolation | Minimum over 10MHz to 10GHz range | | -60 | | dB |
| Device Datapath | | | | | | |
| T _{PLHD/PHLD} | Input-to-output latency (propagation delay) through a data channel | For either low-to-high or high-to-low transition. | | 100 | 130 | ps |
| L _{TX-SKEW} | Lane-to-lane output skew | Between any two lanes within a single transmitter. | | | 20 | ps |
| T _{RJ-DATA} | Additive random jitter with data | Jitter through redriver minus the calibration trace. 20Gbps PRBS15. 800mVpp-diff input swing | | 70 | | fs |
| XT | Channel to channel xtalk (between adjacent active channels, FEXT) | Minimum over 10MHz to 10GHz range, normalized to EQ gain of 0dB | | -43 | | dB |
| FLAT-GAIN | Broadband DC and AC flat gain - input to output, measured at DC | Minimum EQ, GAIN = L0 | | -5.6 | | dB |
| | | Minimum EQ, GAIN = L1 | | -3.8 | | dB |
| | | Minimum EQ, GAIN = L2 | | -1.2 | | dB |
| | | Minimum EQ, GAIN = L3 | | 2.6 | | dB |
| | | Minimum EQ, GAIN = L4 (Float) | | 0.6 | | dB |
| EQ-MAX _{10G} | EQ boost at max setting (EQ INDEX = 19) | AC gain at 10GHz relative to gain at 100MHz. | | 19 | | dB |
| LINEARITY-DC | Output DC linearity | at GAIN = L4 | | 1750 | | mVpp |

over operating free-air temperature and voltage range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------|---------------------|---------------------------|-----|------|-----|------|
| LINEARITY-AC | Output AC linearity | at 10Gbps, with GAIN = L4 | | 1100 | | mVpp |
| | | at 20Gbps, with GAIN = L4 | | 1080 | | mVpp |

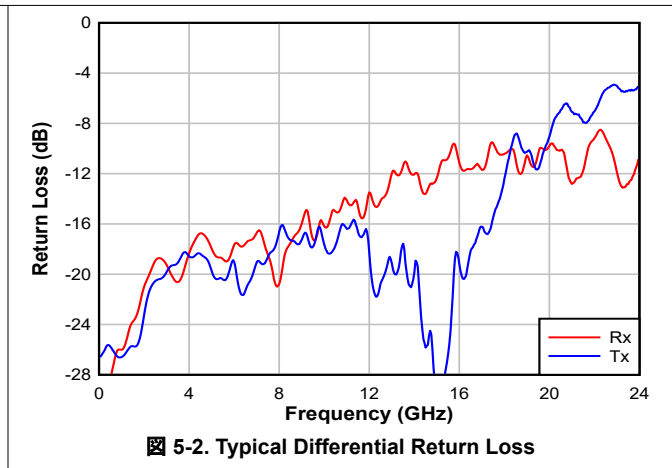
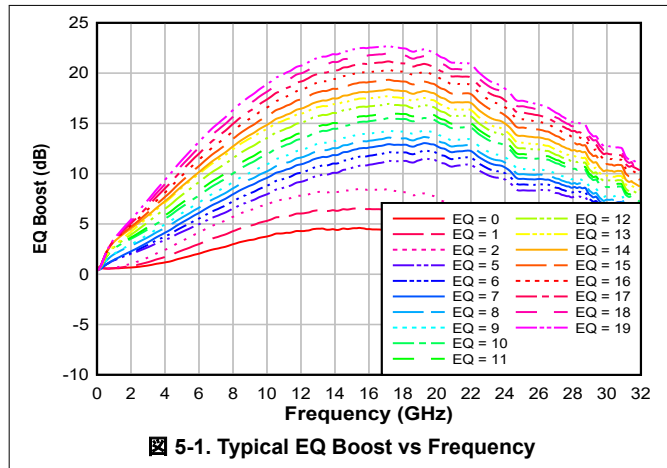
5.7 SMBUS/I²C Timing Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|---|---|-----|------|-----|------|
| Secondary Mode | | | | | | |
| t _{SP} | Pulse width of spikes which must be suppressed by the input filter | | | | 50 | ns |
| t _{HD-STA} | Hold time (repeated) START condition. After this period, the first clock pulse is generated | | 0.6 | | | μs |
| t _{LOW} | LOW period of the SCL clock | | 1.3 | | | μs |
| T _{HIGH} | HIGH period of the SCL clock | | 0.6 | | | μs |
| t _{SU-STA} | Setup time for a repeated START condition | | 0.6 | | | μs |
| t _{HD-DAT} | Data hold time | | 0 | | | μs |
| T _{SU-DAT} | Data setup time | | 0.1 | | | μs |
| t _r | Rise time of both SDA and SCL signals | Pullup resistor = 4.7kΩ, C _b = 10pF | | 120 | | ns |
| t _f | Fall time of both SDA and SCL signals | Pullup resistor = 4.7kΩ, C _b = 10pF | | 2 | | ns |
| t _{SU-STO} | Setup time for STOP condition | | 0.6 | | | μs |
| t _{BUF} | Bus free time between a STOP and START condition | | 1.3 | | | μs |
| t _{VD-DAT} | Data valid time | | | | 0.9 | μs |
| t _{VD-ACK} | Data valid acknowledge time | | | | 0.9 | μs |
| C _b | Capacitive load for each bus line | | | | 400 | pF |
| Primary Mode | | | | | | |
| f _{SCL-M} | SCL clock frequency | | | 303 | | kHz |
| t _{LOW-M} | SCL low period | | | 1.90 | | μs |
| T _{HIGH-M} | SCL high period | | | 1.40 | | μs |
| t _{SU-STA-M} | Setup time for a repeated START condition | | | 2 | | μs |
| t _{HD-STA-M} | Hold time (repeated) START condition. After this period, the first clock pulse is generated | | | 1.5 | | μs |
| T _{SU-DAT-M} | Data setup time | | | 1.4 | | μs |
| t _{HD-DAT-M} | Data hold time | | | 0.5 | | μs |
| t _{R-M} | Rise time of both SDA and SCL signals | Pullup resistor = 4.7kΩ, C _b = 10pF | | 120 | | ns |
| T _{F-M} | Fall time of both SDA and SCL signals | Pullup resistor = 4.7kΩ, C _b = 10pF | | 2 | | ns |
| t _{SU-STO-M} | Stop condition setup time | | | 1.5 | | μs |
| EEPROM Timing | | | | | | |
| T _{EEPROM} | EEPROM configuration load time | Time to assert DONE _n after READ_EN_N has been asserted. | | 7.5 | | ms |
| T _{POR} | Time to first SMBus access | Power supply stable after initial ramp. Includes initial power-on reset time. | | 50 | | ms |

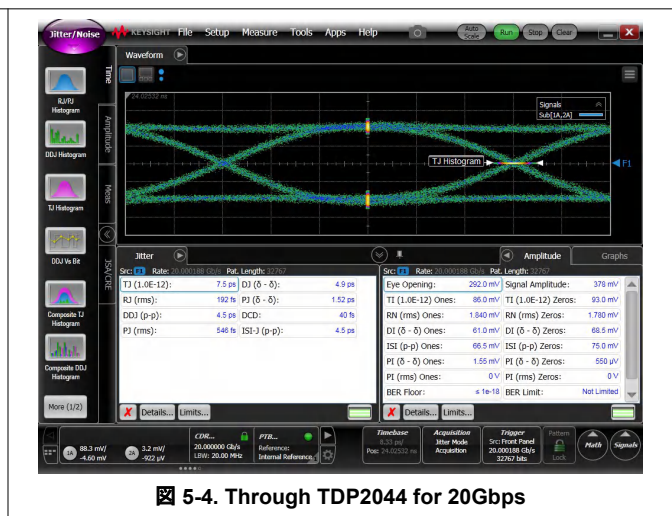
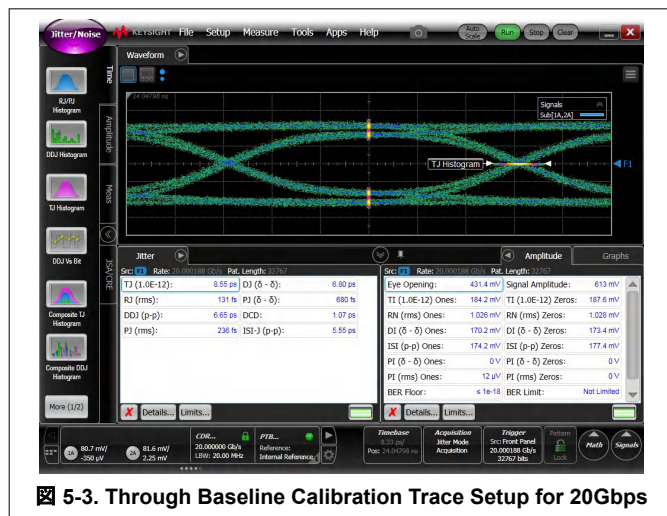
5.8 Typical Characteristics

Figure 5-1 shows typical EQ gain curves versus frequency for different EQ settings. Figure 5-2 shows typical differential return loss for Rx and Tx pins.



5.9 Typical Jitter Characteristics

Figure 5-3 and Figure 5-4 show eye diagrams at 20Gbps that compare jitter through calibration traces (left), and jitter through TDP2044 (right) at TI evaluation boards with minimal channels. The eye diagrams illustrate that TDP2044 adds very little random jitter (RJ).



6 Detailed Description

6.1 Overview

The TDP2044 is a four-channel multi-rate linear repeater with integrated signal conditioning. The signal channels of the device operate independently from one another. Each channel includes a continuous-time linear equalizer (CTLE) and a linear output driver, which together compensate for a lossy transmission channel between the source transmitter and the final receiver. The linearity of the data path is specifically designed to preserve any transmit equalization while keeping receiver equalization effective.

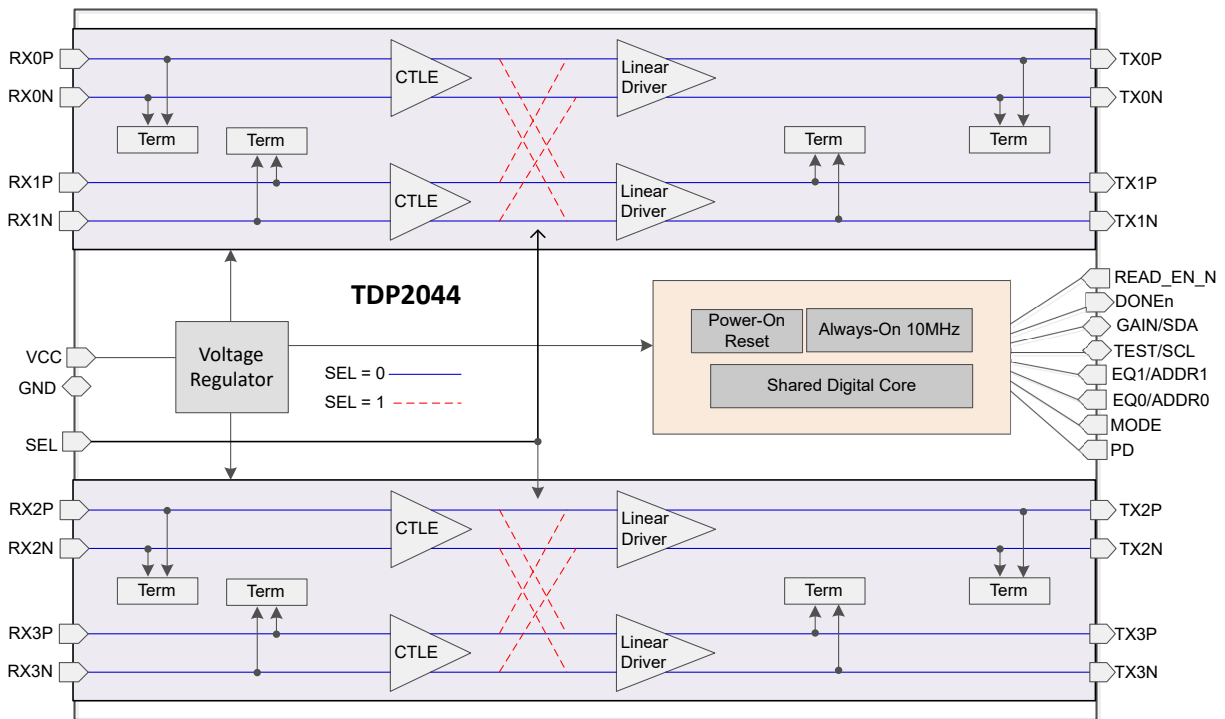
The TDP2044 can be configured three different ways:

Pin mode – device control configuration is done solely by strap pins. Pin mode is expected to be satisfactory for many system implementation needs.

SMBus/I²C Primary mode – device control configuration is read from external EEPROM. When the TDP2044 has finished reading from the EEPROM successfully, the device drives the DONE_n pin LOW. SMBus/I²C secondary operation is available in this mode before, during, or after EEPROM reading. Note: during EEPROM reading, if the external SMBus/I²C primary wants to access TDP2044 registers, the external controller must support arbitration. The mode is preferred when software implementation is not desired.

SMBus/I²C Secondary mode – provides most flexibility. Requires a SMBus/I²C primary device to configure TDP2044 though writing to the secondary address.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Linear Equalization

The TDP2044 receivers feature a continuous-time linear equalizer (CTLE) that applies high-frequency boost and low-frequency attenuation to help equalize the frequency-dependent insertion loss effects of the passive channel. The receivers implement two stage linear equalizer for wide range of equalization capability. The equalizer stages also provide flexibility to make subtle modifications of mid-frequency boost for best EQ gain profile match with wide range of channel media characteristics. The EQ profile control feature is only available in SMBus/I²C mode. In Pin mode the settings are optimized for FR4 traces.

表 6-1 provides available equalization boost at 20Gbps (10GHz Nyquist frequency) through EQ control pins or SMBus/I²C registers. In Pin Control mode EQ1 and EQ0 pins set equalization boost for channels 0-3. In I²C mode individual channels can be independently programmed for EQ boost. If the TDP2044 is used for other data rates equalization gain can be extracted from [図 5-1](#).

表 6-1. Equalization Control Settings

| EQ INDEX | EQUALIZATION SETTING | | | | | | TYPICAL EQ BOOST (dB) at 10GHz |
|----------|----------------------|-----|-----------------------------|---------------|----------------|------------------|---------------------------------------|
| | Pin mode | | SMBus/I ² C Mode | | | | |
| | EQ1 | EQ0 | eq_stage1_3:0 | eq_stage2_2:0 | eq_profile_3:0 | eq_stage1_bypass | |
| 0 | L0 | L0 | 0 | 0 | 0 | 1 | 4.0 |
| 1 | L0 | L1 | 1 | 0 | 0 | 1 | 5.0 |
| 2 | L0 | L2 | 3 | 0 | 0 | 1 | 7.0 |
| 5 | L1 | L0 | 0 | 0 | 1 | 0 | 8.0 |
| 6 | L1 | L1 | 1 | 0 | 1 | 0 | 9.0 |
| 7 | L1 | L2 | 2 | 0 | 1 | 0 | 9.5 |
| 8 | L1 | L3 | 3 | 0 | 3 | 0 | 10.0 |
| 9 | L1 | L4 | 4 | 0 | 3 | 0 | 11.0 |
| 10 | L2 | L0 | 5 | 1 | 7 | 0 | 12.0 |
| 11 | L2 | L1 | 6 | 1 | 7 | 0 | 12.5 |
| 12 | L2 | L2 | 8 | 1 | 7 | 0 | 13.5 |
| 13 | L2 | L3 | 10 | 1 | 7 | 0 | 14.5 |
| 14 | L2 | L4 | 10 | 2 | 15 | 0 | 15.0 |
| 15 | L3 | L0 | 11 | 3 | 15 | 0 | 15.5 |
| 16 | L3 | L1 | 12 | 4 | 15 | 0 | 16.5 |
| 17 | L3 | L2 | 13 | 5 | 15 | 0 | 17.0 |
| 18 | L3 | L3 | 14 | 6 | 15 | 0 | 18.0 |
| 19 | L3 | L4 | 15 | 7 | 15 | 0 | 19.0 |

6.3.2 Flat-Gain

The GAIN pin can be used to set the overall data-path flat gain (DC and AC) of the TDP2044 when the device is in Pin mode. The pin GAIN sets the Flat-Gain for channels 0-3. In I²C mode each channel can be independently set. 表 6-2 provides flat gain control configuration settings. For most systems the default setting of GAIN = L4 (float) is recommended that provides flat gain of 0dB.

The flat-gain and equalization of the TDP2044 must be set such that the output signal swing at DC and high frequency does not exceed the DC and AC linearity ranges of the devices, respectively.

表 6-2. Flat Gain Configuration Settings

| Pin mode GAIN | I ² C Mode flat_gain_2:0 | Flat Gain |
|---------------|-------------------------------------|--------------------------------|
| L0 | 0 | -5.6dB |
| L1 | 1 | -3.8dB |
| L2 | 3 | -1.2dB |
| L4 (float) | 5 | 0.6dB (default recommendation) |
| L3 | 7 | +2.6dB |

6.4 Device Functional Modes

6.4.1 Active Mode

The device is in normal operation. In this mode, the TDP2044 redrives and equalizes video mainlink signals to provide better signal integrity.

6.4.2 Standby Mode

The device is in standby mode invoked by PD = H. In this mode, the device is in standby mode conserving power.

6.5 Programming

6.5.1 Pin mode

The TDP2044 can be fully configured through pin-strap pins. In this mode the device uses 2-level and 5-level pins for device control and signal integrity optimum settings.

6.5.1.1 Five-Level Control Inputs

The TDP2044 has four (EQ0, EQ1, GAIN, and MODE) 5-level input pins that are used to control the configuration of the device. These 5-level inputs use a resistor divider to help set the 5 valid levels and provide a wider range of control settings. External resistors must be of 10% tolerance or better. The 5-level pins except MODE are sampled at powerup only. The MODE pin can be exercised at device power up or in normal operation mode.

表 6-3. 5-Level Control Pin Settings

| LEVEL | SETTING |
|-------|---------------|
| L0 | 1kΩ to GND |
| L1 | 8.25kΩ to GND |
| L2 | 24.9kΩ to GND |
| L3 | 75kΩ to GND |
| L4 | F (Float) |

6.5.2 SMBUS/I²C Register Control Interface

If MODE = L2 (SMBus/I²C Secondary control mode), then the TDP2044 is configured through a standard I²C or SMBus interface that can operate up to 400kHz. The secondary address of the TDP2044 is determined by the pin strap settings on the ADDR1 and ADDR0 pins. The sixteen possible secondary addresses for channels 0-3 are provided in 表 6-4. In SMBus/I²C modes the SCL and SDA pins must be pulled up to a 3.3V supply with a pullup resistor. The value of the resistor depends on total bus capacitance. 4.7kΩ is a good first approximation for a bus capacitance of 10pF.

表 6-4. SMBUS/I²C Secondary Address Settings

| ADDR1 | ADDR0 | 7-bit Secondary Address Channels 0-3 |
|-------|-------|--------------------------------------|
| L0 | L0 | 0x18 |
| L0 | L1 | 0x1A |
| L0 | L2 | 0x1C |
| L0 | L3 | 0x1E |
| L0 | L4 | Reserved |
| L1 | L0 | 0x20 |
| L1 | L1 | 0x22 |
| L1 | L2 | 0x24 |
| L1 | L3 | 0x26 |
| L1 | L4 | Reserved |
| L2 | L0 | 0x28 |

表 6-4. SMBUS/I²C Secondary Address Settings (続き)

| ADDR1 | ADDR0 | 7-bit Secondary Address Channels 0-3 |
|-------|-------|--------------------------------------|
| L2 | L1 | 0x2A |
| L2 | L2 | 0x2C |
| L2 | L3 | 0x2E |
| L2 | L4 | Reserved |
| L3 | L0 | 0x30 |
| L3 | L1 | 0x32 |
| L3 | L2 | 0x34 |
| L3 | L3 | 0x36 |
| L3 | L4 | Reserved |

The TDP2044 has two types of registers:

- **Shared Registers:** these registers can be accessed at any time and are used for device-level configuration, status read back, control, or to read back the device ID information.
- **Channel Registers:** these registers are used to control and configure specific features for each individual channel. All channels have the same register set and can be configured independent of each other or configured as a group through broadcast writes to Channels 0-3.

表 6-5. Channel Register Access

| Channel Registers Base Address | Channel 0-3 Access |
|--------------------------------|---|
| 0x00 | Channel 0 registers |
| 0x20 | Channel 1 registers |
| 0x40 | Channel 2 registers |
| 0x60 | Channel 3 registers |
| 0x80 | Broadcast write channel 0-3 registers, read channel 0 registers |
| 0xA0 | Broadcast write channel 0-1 registers, read channel 0 registers |
| 0xC0 | Broadcast write channel 2-3 registers, read channel 2 registers |
| 0xE0 | Channel 0-3 share registers |

6.5.2.1 Shared Registers

表 6-6. General Registers (Offset = 0xE2)

| Bit | Field | Type | Reset | Description |
|-----|--------------|--------|-------|---|
| 7 | RESERVED | R | 0x0 | Reserved |
| 6 | rst_i2c_regs | R/W/SC | 0x0 | Device reset control: Reset all I ² C registers to default values (self-clearing). |
| 5 | rst_i2c_mas | R/W/SC | 0x0 | Reset I ² C Primary (self-clearing). |
| 4-1 | RESERVED | R | 0x0 | Reserved |
| 0 | frc_eeprm_rd | R/W/SC | 0x0 | Override MODE and READ_EN_N status to force manual EEPROM configuration load. |

表 6-7. EEPROM_Status Register (Offset = 0xE3)

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|-------|---|
| 7 | eecfg_cmplt | R | 0x0 | EEPROM load complete. |
| 6 | eecfg_fail | R | 0x0 | EEPROM load failed. |
| 5 | eecfg_atmpt_1 | R | 0x0 | Number of attempts made to load EEPROM image. |
| 4 | eecfg_atmpt_0 | R | 0x0 | |
| 3 | eecfg_cmplt | R | 0x0 | EEPROM load complete 2. |
| 2 | eecfg_fail | R | 0x0 | EEPROM load failed 2. |

表 6-7. EEPROM_Status Register (Offset = 0xE3) (続き)

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|-------|---|
| 1 | eecfg_atmpt_1 | R | 0x0 | Number of attempts made to load EEPROM image 2. |
| 0 | eecfg_atmpt_0 | R | 0x0 | |

表 6-8. DEVICE_ID0 Register (Offset = 0xF0)

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|-----------------------|
| 7-4 | RESERVED | R | 0x0 | Reserved |
| 3 | device_id0_3 | R | 0x0 | Device ID0 [3:1]: 011 |
| 2 | device_id0_2 | R | 0x1 | |
| 1 | device_id0_1 | R | 0x1 | |
| 0 | RESERVED | R | X | Reserved |

表 6-9. DEVICE_ID1 Register (Offset = 0xF1)

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|------------------------------|
| 7 | device_id[7] | R | 0x0 | Device ID 0010 1001: TDP2044 |
| 6 | device_id[6] | R | 0x0 | |
| 5 | device_id[5] | R | 0x1 | |
| 4 | device_id[4] | R | 0x0 | |
| 3 | device_id[3] | R | 0x1 | |
| 2 | device_id[2] | R | 0x0 | |
| 1 | device_id[1] | R | 0x0 | |
| 0 | device_id[0] | R | 0x0 | |

6.5.2.2 Channel Registers

表 6-10. EQ Gain Control Register (Channel register base + Offset = 0x01)

| Bit | Field | Type | Reset | Description |
|-----|------------------|------|-------|--|
| 7 | eq_stage1_bypass | R/W | 0x0 | Enable EQ stage 1 bypass: 0: Bypass disabled 1: Bypass enabled |
| 6 | eq_stage1_3 | R/W | 0x0 | EQBoost stage 1 control See 表 6-1 for details |
| 5 | eq_stage1_2 | R/W | 0x0 | |
| 4 | eq_stage1_1 | R/W | 0x0 | |
| 3 | eq_stage1_0 | R/W | 0x0 | |
| 2 | eq_stage2_2 | R/W | 0x0 | EQ Boost stage 2 control See 表 6-1 for details |
| 1 | eq_stage2_1 | R/W | 0x0 | |
| 0 | eq_stage2_0 | R/W | 0x0 | |

表 6-11. EQ Gain / Flat Gain Control Register (Channel register base + Offset = 0x03)

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|---|
| 7 | RESERVED | R | 0x0 | Reserved |
| 6 | eq_profile_3 | R/W | 0x0 | EQ mid-frequency boost profile See 表 6-1 for details |
| 5 | eq_profile_2 | R/W | 0x0 | |
| 4 | eq_profile_1 | R/W | 0x0 | |
| 3 | eq_profile_0 | R/W | 0x0 | |

表 6-11. EQ Gain / Flat Gain Control Register (Channel register base + Offset = 0x03) (続き)

| Bit | Field | Type | Reset | Description |
|-----|-------------|------|-------|--|
| 2 | flat_gain_2 | R/W | 0x1 | Flat gain select: See 表 6-2 for details |
| 1 | flat_gain_1 | R/W | 0x0 | |
| 0 | flat_gain_0 | R/W | 0x1 | |

表 6-12. TI Test Mode Control Register (Channel register base + Offset = 0x04)

| Bit | Field | Type | Reset | Description |
|----------|--------------|------|-------|--|
| 7-3, 1-0 | RESERVED | R | 0x0 | Reserved |
| 2 | TI test mode | R/W | 0x0 | Set TI test mode: 0: test mode is enabled 1: test mode is disabled. Must be set to "1" for normal operation. |

表 6-13. PD Override Register (Channel register base + Offset = 0x05)

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|----------|--|
| 7 | device_en_override | R/W | 0x0 | Enable power down overrides through SMBus/I ² C 0: Manual override disabled 1: Manual override enabled |
| 6-0 | device_en | R/W | 0x111111 | Manual power down of redriver various blocks of a channel – gated by device_en_override = 1 111111: All blocks in the channel are enabled 000000: All blocks in the channel are disabled |

表 6-14. Bias Register (Channel register base + Offset = 0x06)

| Bit | Field | Type | Reset | Description |
|---------|--------------|------|---------|--|
| 5-3 | Bias current | R/W | 0x100 | Control bias current Set 001 for best performance |
| 7,6,2-0 | Reserved | R/W | 0x00000 | Reserved |

6.5.3 SMBus/I²C Primary Mode Configuration (EEPROM Self Load)

The TDP2044 can also be configured by reading from EEPROM. To enter into this mode MODE pin must be set to L1. The EEPROM load operation only happens once after the initial powerup of the device. If the TDP2044 is configured for SMBus Primary mode, the device remains in the SMBus IDLE state until the READ_EN_N pin is asserted to LOW. After the READ_EN_N pin is driven LOW, the TDP2044 becomes an SMBus primary and attempts to self-configure by reading the device settings stored in an external EEPROM (SMBus 8-bit address 0xA0). When the TDP2044 has finished reading from the EEPROM successfully, the device drives the DONE pin LOW. SMBus/I²C secondary operation is available in this mode before, during, or after EEPROM reading. Note: during EEPROM reading, if the external SMBus/I²C primary wants to access TDP2044 registers, the external controller must support arbitration.

When designing a system for using the external EEPROM, the user must follow these specific guidelines:

- EEPROM size of 2Kb (256 × 8-bit) is recommended.
- Set MODE = L1, configure for SMBus Primary mode.
- The external EEPROM device address byte must be 0xA0 and capable of 400kHz operation at 3.3V supply
- In SMBus/I²C modes the SCL and SDA pins must be pulled up to a 3.3V supply with a pullup resistor. The value of the resistor depends on total bus capacitance. 4.7kΩ is a good first approximation for a bus capacitance of 10pF.

Multiple TDP2044 can be cascaded to read from single EEPROM. Tie the READ_EN_N pin of the first device low (GND) to automatically initiate EEPROM read at power up. DONE of the first device can be fed into READ_EN_N of the next device with 4.7kΩ pullup resistors. Leave the DONE pin of the final device floating, or connect the pin to a microcontroller input to monitor the completion of the final EEPROM read.

7 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TDP2044 is a high-speed linear repeater which extends the reach of differential channels impaired by loss from transmission media like PCBs and cables. The device can be deployed in a variety of different systems. The following sections outline typical applications and their associated design considerations.

7.2 Typical Applications

The TDP2044 is a linear redriver with integrated cross-point mux to account for USB Type-C plug orientation that can be used as DisplayPort mainlink signal conditioner. The TDP2044 can be used in both source and sink applications as illustrated in [図 7-1](#).

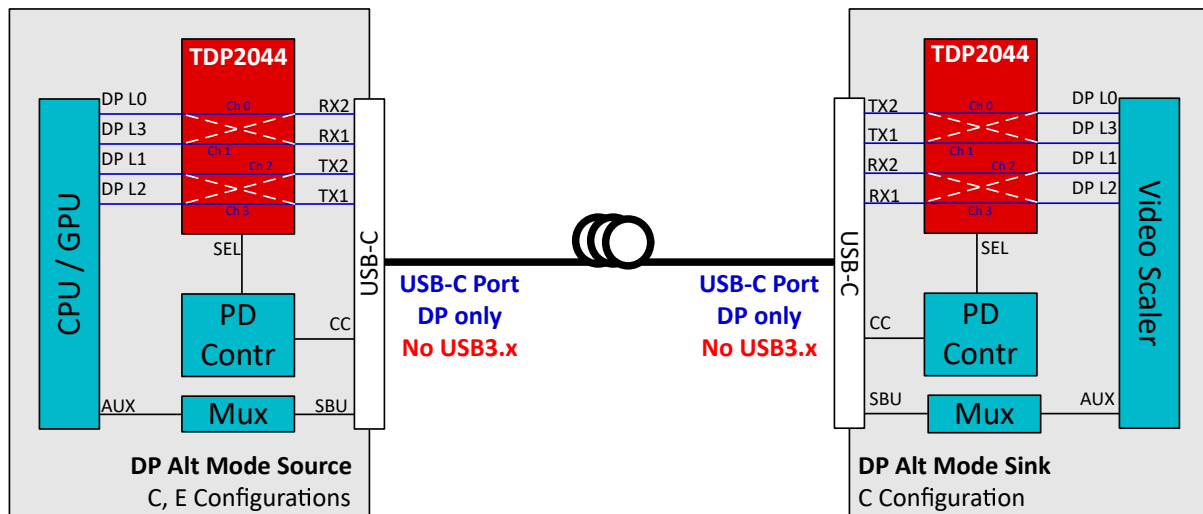


図 7-1. Typical Application

7.2.1 USB Type-C DP Only Source Applications

The TDP2044 can be used in a video source/sink systems such as PC motherboard, industrial PCs, docking stations, industrial display/signs, display monitor among other applications to boost DisplayPort mainlink signals to increase the reach of the source and sink channel while providing cross-point function. The following sections outline detailed procedures and design requirements for a typical DP 2.1 application. However, the design recommendations can be used in other use cases.

7.2.1.1 Design Requirements

As with any high-speed design, there are many factors which influence the overall performance. The following list indicates critical areas for consideration during design.

- Match the length between the P and N traces of the single-end segments of the differential pair.
- Use a uniform trace width and trace spacing for differential pairs.
- Place AC-coupling capacitors near the receiver end of each channel segment to minimize reflections.

- AC-coupling capacitors of 220nF are recommended. Set the maximum body size to 0402 and add a cutout void on the GND plane below the landing pad of the capacitor to reduce parasitic capacitance to GND.
- Surface mount connector is recommended. For through hole connection, back-drill connector vias and signal vias to minimize stub length.
- Use ground reference plane vias for a low inductance path for the return current.

7.2.1.2 Detailed Design Procedure

The TDP2044 provides signal conditioning for four DP mainlink channels along with 4:4 cross-point (channel re-orientation) function. The device is a linear redriver which is agnostic to DP link training. The DP link training negotiation between a display source and sink stays effective through the device. The redriver becomes part of the electrical channel along with passive traces, cables, and other channel elements, resulting in optimum source and sink parameters for best electrical link. 7-2 shows a simplified schematic for DisplayPort application using TDP2044 to implement USB Type-C DP alternate mode in a source application. A USB power delivery (PD) device control the cross-point mux polarity signal SEL according to USB Type-C cable plug position.

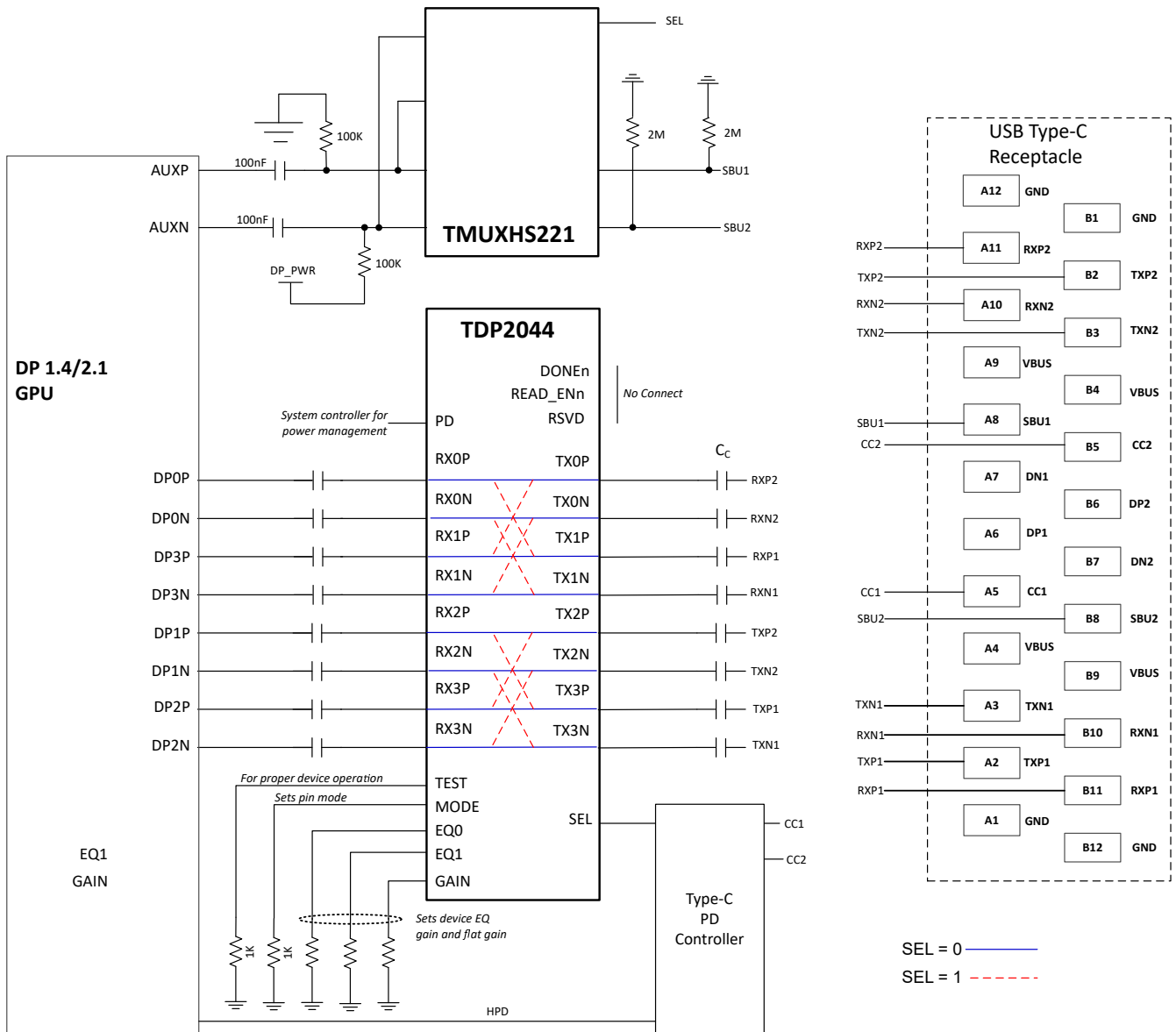


图 7-2. Simplified Schematic for USB-C Alternate Mode Source Application

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DisplayPort side-band signals AUXp,n and HPD are bypassed. An external mux such as [TMUXHS221](#) can provide flipping functions for SBU signals as illustrated in [図 7-2](#). An inverted HPD signal can be used to control the device standby operation using the PD pin; however appropriate filtering out of HPD interrupt signals must be provisioned.

In some applications where a microcontroller or other link monitoring device has DP link state information, the controller can exercise I²C registers of TDP2044 for additional power management.

[表 7-1](#) shows how DP signals are routed to a USB Type-C connector for a source applications for both SEL = 0 and SEL =1 configurations

表 7-1. DP Alt Mode Source Pin Assignment C or E

| SEL pin | DP Lane from Source | TDP2044 RX PIN | TDP2044 TX PIN | USB-C Receptacle pin |
|---------|---------------------|----------------|----------------|----------------------|
| 0 | DP0P/N | RX0P/N | TX0P/N | RXP/N2 |
| 0 | DP3P/N | RX1P/N | TX1P/N | RXP/N1 |
| 0 | DP1P/N | RX2P/N | TX2P/N | TXP/N2 |
| 0 | DP2P/N | RX3P/N | TX3P/N | TXP/N1 |
| 1 | DP0P/N | RX0P/N | TX1P/N | RXP/N1 |
| 1 | DP3P/N | RX1P/N | TX0P/N | RXP/N2 |
| 1 | DP1P/N | RX2P/N | TX3P/N | TXP/N1 |
| 1 | DP2P/N | RX3P/N | TX2P/N | TXP/N2 |

While a DP alternate mode sink implementation is similar, the TDP2044 can not support both configuration C and E in the same DP sink board. If the both configurations are required the DP Sink must handle the DP lane order and polarity inversion. Most sink implementations use configuration C illustrated in [表 7-2](#).

表 7-2. DP Alt Mode Sink Pin Assignment C

| SEL pin | USB-C Receptacle pin | TDP2044 RX PIN | TDP2044 TX PIN | DP Lane to Sink |
|---------|----------------------|----------------|----------------|-----------------|
| 0 | TXP/N2 | RX0P/N | TX0P/N | DP0P/N |
| 0 | TXP/N1 | RX1P/N | TX1P/N | DP3P/N |
| 0 | RXP/N2 | RX2P/N | TX2P/N | DP1P/N |
| 0 | RXP/N1 | RX3P/N | TX3P/N | DP2P/N |
| 1 | TXP/N1 | RX0P/N | TX1P/N | DP0P/N |
| 1 | TXP/N2 | RX1P/N | TX0P/N | DP3P/N |
| 1 | RXP/N1 | RX2P/N | TX3P/N | DP1P/N |
| 1 | RXP/N2 | RX3P/N | TX2P/N | DP2P/N |

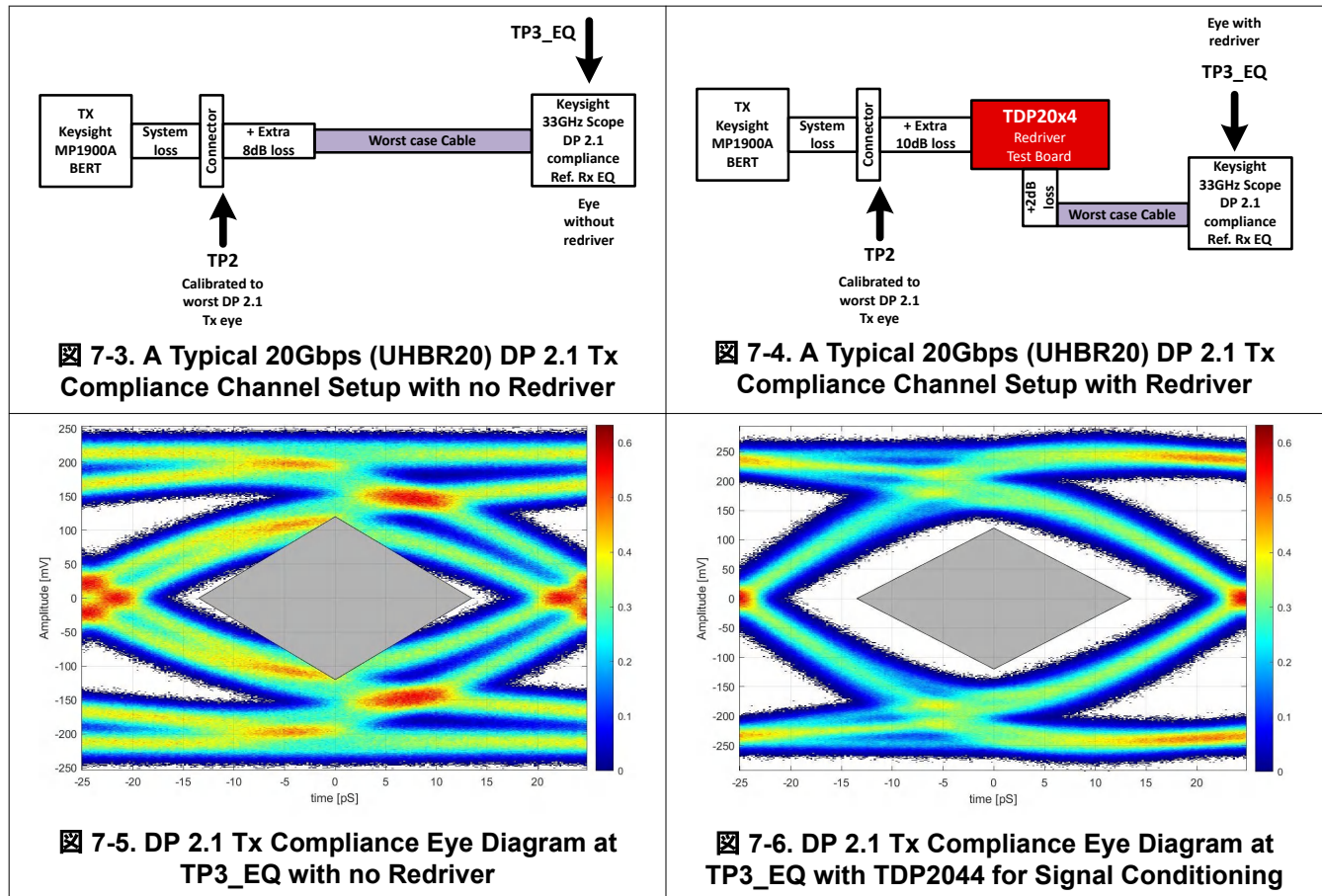
USB PD controller is used to negotiate DP Alternate Mode with a link partner. USB PD specification require that the TDP2044 TX/RX pins connected to USB Type-C pins support USB safe state electrical requirements. To support USB safe state the TDP2044 must be entered into standby mode with PD = H. [表 7-3](#) shows electrical characteristics in standby mode.

表 7-3. TX and RX Pins in Standby Mode

| Parameters | Standby mode (PD = H) |
|---------------------|-----------------------|
| Rx CMV | 1.4V |
| Rx impedance to GND | 230K |
| Tx CMV | 0.9V |
| Tx impedance to GND | 3M |

7.2.1.3 Application Curves

The TDP2044 is a linear redriver that can be used to extend channel reach of a DP link. The redriver can help to pass compliance by removing ISI deterministic jitter at data rates up to 20Gbps (UHBR20). [7-3](#) - [7-6](#) shows a typical DP 2.1 Tx compliance channel setup along with compliance Eye Diagrams at TP3_EQ with or without redriver. The comparison of eye diagrams show that TDP2044 can provide signal conditioning by extending horizontal and vertical eye openings that makes a failing eye to pass.



7.3 Power Supply Recommendations

Follow these general guidelines when designing the power supply:

1. The power supply must be designed to provide the operating conditions outlined in the recommended operating conditions section in terms of DC voltage, AC noise, and start-up ramp time.
2. The TDP2044 does not require any special power supply filtering, such as ferrite beads, provided that the recommended operating conditions are met. Only standard supply decoupling is required. Typical supply decoupling consists of a 0.1µF capacitor per VCC pin, one 1.0µF bulk capacitor per device, and one 10µF bulk capacitor per power bus that delivers power to one or more TDP2044 devices. The local decoupling (0.1µF) capacitors must be connected as close to the VCC pins as possible and with minimal path to the TDP2044 ground pad.

7.4 Layout

7.4.1 Layout Guidelines

Refer to following guidelines when designing the layout of the system implementation:

1. Place the decoupling capacitors as close to the VCC pins as possible. Placing the decoupling capacitors directly underneath the device is recommended if the board design permits.
2. Make sure the high-speed differential signals TXnP/TXnN and RXnP/RXnN are tightly coupled, skew matched, and impedance controlled.
3. Avoid vias when possible on the high-speed differential signals. When vias must be used, take care to minimize the via stub, either by transitioning through most or all layers or by back drilling.
4. GND relief can be used (but is not required) beneath the high-speed differential signal pads to improve signal integrity by counteracting the pad capacitance.
5. Place GND vias directly beneath the device connecting the GND plane attached to the device to the GND planes on other layers. This has the added benefit of improving thermal conductivity from the device to the board.
6. Refer to land pattern example in the mechanical drawing section for the device thermal pad design recommendation.

7.4.2 Layout Example

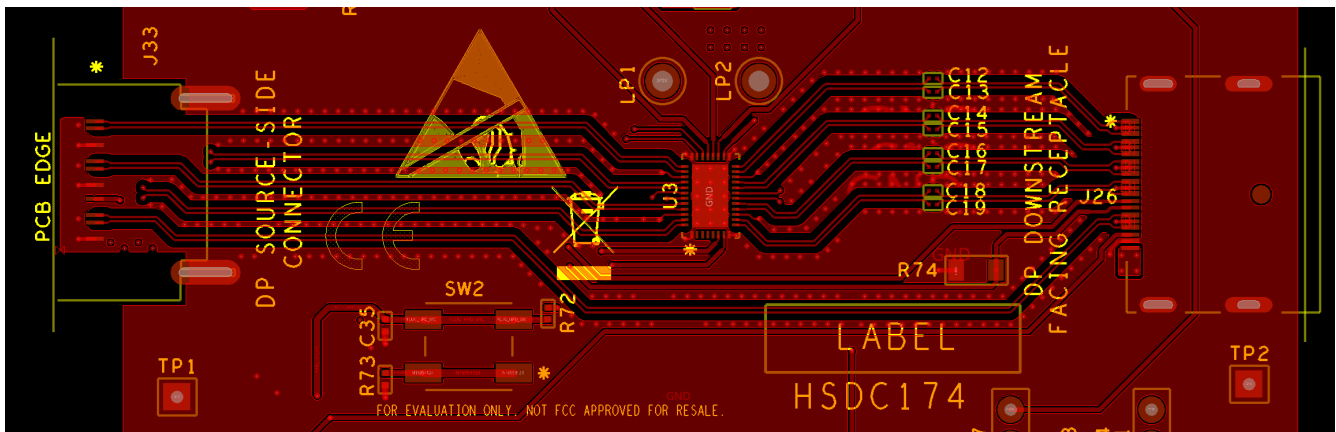


图 7-7. TDP2044 Layout Example – Sub-Section of TI Evaluation Board with DP Connectors

8 Device and Documentation Support

8.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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8.5 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

| DATE | REVISION | NOTES |
|-----------|----------|-----------------|
| June 2024 | * | Initial Release |

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| TDP2044IRNQR | Active | Production | WQFN (RNQ) 40 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TDP2 |
| TDP2044IRNQR.B | Active | Production | WQFN (RNQ) 40 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TDP2 |
| TDP2044IRNQT | Active | Production | WQFN (RNQ) 40 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TDP2 |
| TDP2044IRNQT.B | Active | Production | WQFN (RNQ) 40 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TDP2 |
| TDP2044RNQR | Active | Production | WQFN (RNQ) 40 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TDP2 |
| TDP2044RNQR.B | Active | Production | WQFN (RNQ) 40 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TDP2 |
| TDP2044RNQT | Active | Production | WQFN (RNQ) 40 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TDP2 |
| TDP2044RNQT.B | Active | Production | WQFN (RNQ) 40 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TDP2 |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TDP2044IRNQR | WQFN | RNQ | 40 | 3000 | 330.0 | 12.4 | 4.3 | 6.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TDP2044IRNQT | WQFN | RNQ | 40 | 250 | 180.0 | 12.4 | 4.3 | 6.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TDP2044RNQR | WQFN | RNQ | 40 | 3000 | 330.0 | 12.4 | 4.3 | 6.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TDP2044RNQT | WQFN | RNQ | 40 | 250 | 180.0 | 12.4 | 4.3 | 6.3 | 1.1 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

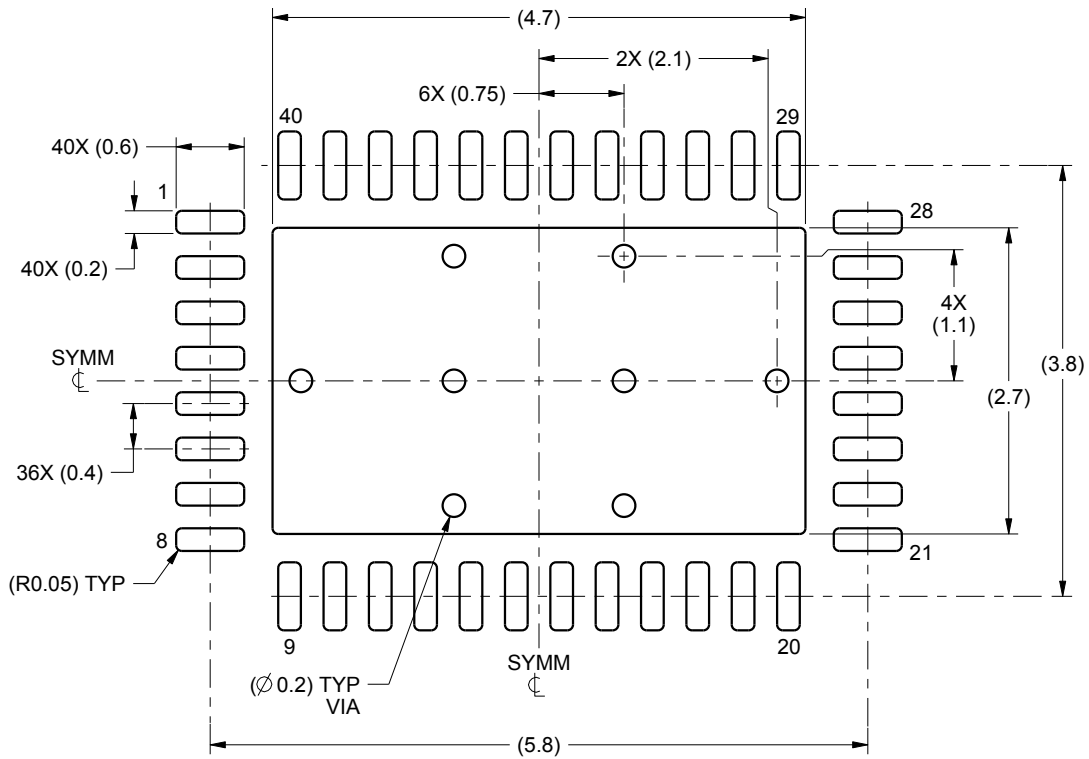
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TDP2044IRNQR | WQFN | RNQ | 40 | 3000 | 367.0 | 367.0 | 35.0 |
| TDP2044IRNQT | WQFN | RNQ | 40 | 250 | 210.0 | 185.0 | 35.0 |
| TDP2044RNQR | WQFN | RNQ | 40 | 3000 | 367.0 | 367.0 | 35.0 |
| TDP2044RNQT | WQFN | RNQ | 40 | 250 | 210.0 | 185.0 | 35.0 |

EXAMPLE BOARD LAYOUT

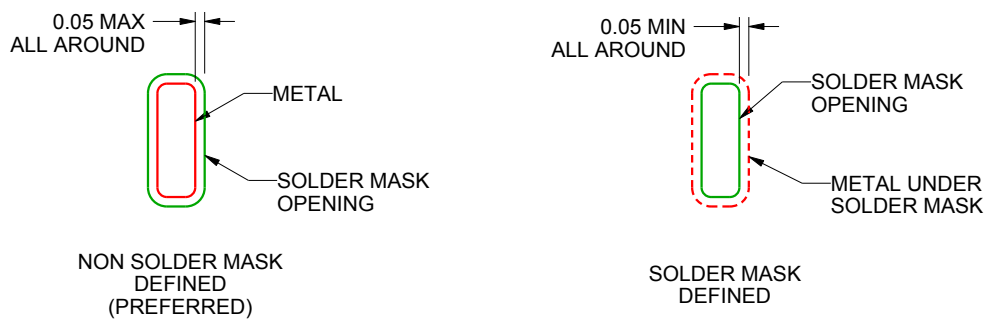
RNQ0040A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

4222125/B 01/2016

NOTES: (continued)

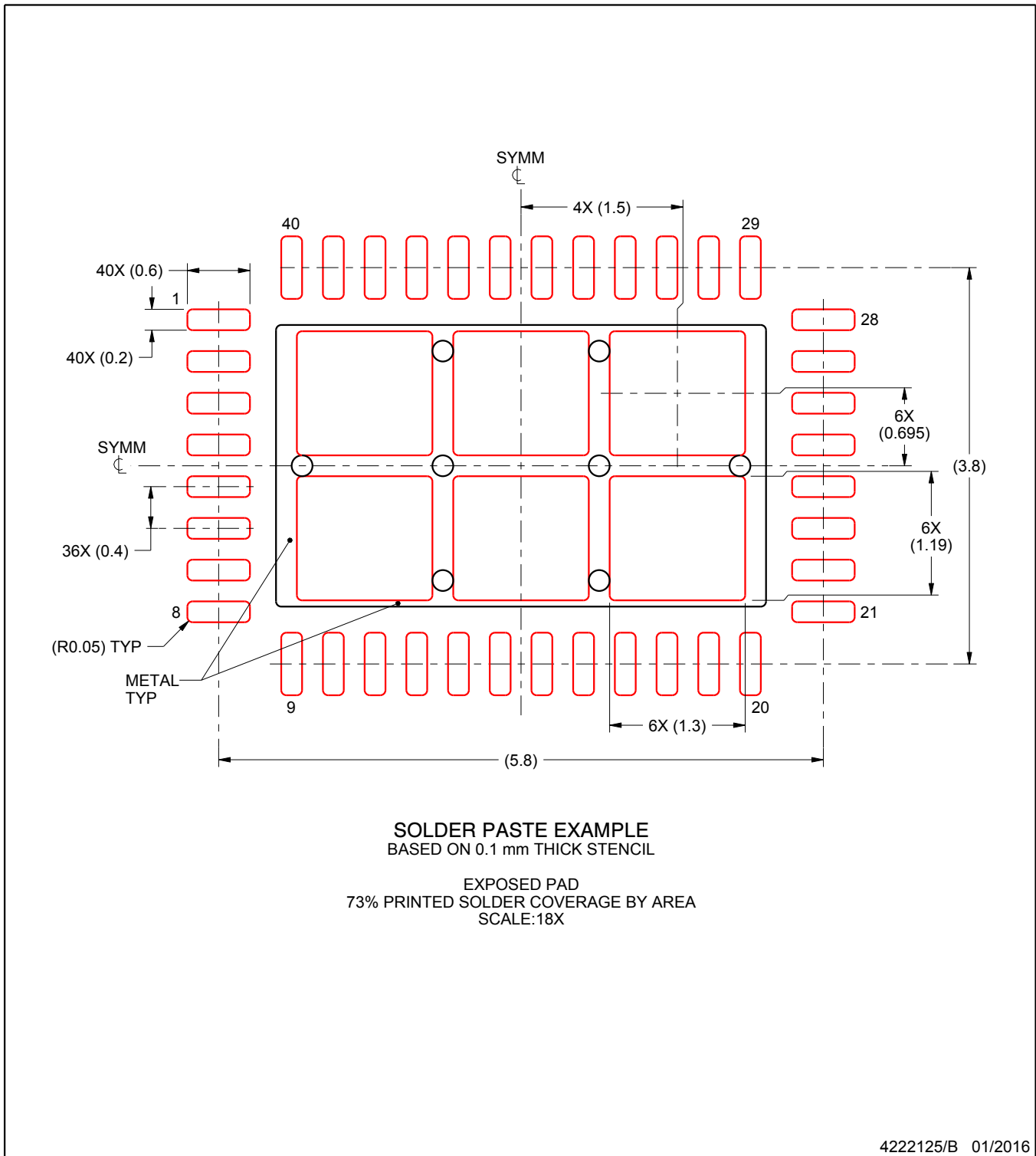
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RNQ0040A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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