THS3215 650MHz、差動からシングルエンドへの変換、DAC 出力アンプ

1 特長

- 入力段:内部ゲイン 2V/V
  - バッファ付き差動入力
  - シングルエンドの低インピーダンス出力
  - フルパワー帯域幅:350MHz ($2V_{PP}$)
- 出力段:外部でゲインを変更可能
  - フルパワー帯域幅:270MHz ($5V_{PP}$)
  - スルーレート:3000V/µs
  - SPDT 入力スイッチとマルチプレクサ
- 全信号パス:入力段 + 出力段
  - HD2 (20MHz、$5V_{PP}$、100Ω 負荷):–66dBc
  - HD3 (20MHz、$5V_{PP}$、100Ω 負荷):–68dBc
  - 100Ω 負荷に $10V_{PP}$ を出力 (±6.5V 両電源を使用)
  - 重い容量性負荷に $12V_{PP}$ を出力 (15V 単電源を使用)
- 低インピーダンス出力を備えた内部 DC 基準バッファ
- 電源電圧範囲
  - 両電源:±4V～±7.9V
  - 単電源:8V～15.8V

2 アプリケーション

- D/A コンバータ (DAC) の出力アンプ
- 広帯域任意波形ジェネレータ (AWG) の出力ドライバ
- $20V_{PP}$ を超える出力アンプ (THS3091) へのプリドライバ
- ピエゾ素子用の単一電源、大容量性負荷のドライバ

3 概要

THS3215 は、相補電流出力のデジタル / アナログ・コンバータ (DAC) と接続するために必要な主要信号チェーン・コンポーネントを統合しています。

この 2 段アンプ・システムがもたらす柔軟性は、各種システムが必要とする差動入力シングルエンド出力 DC 結合低歪み信号処理を実現します。入力段は DAC の抵抗性終端をバッファリングし、2V/V の固定ゲインで差動からシングルエンドに信号を変換します。この差動からシングルエンドへの出力は、外部で直接使用することができ、RLC フィルタまたはアッテネータ経由で内部出力電力段 (OPS) の入力に接続することもできます。この広帯域電流帰還出力電力段は、外部ピンでゲインを柔軟に設定できます。

出力電力段の非反転入力に接続された内部 2×1 マルチプレクサ (mux) により、内部差動 - シングルエンド段 (D2S) 出力と外部入力を簡単に切り替えることできます。

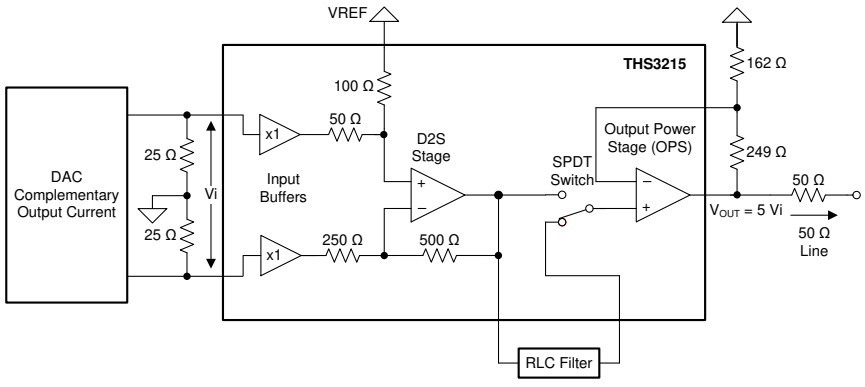
オプションのオンチップ中間電源バッファは、単一電源動作中に信号パス段を経由してバイアス印加するための広帯域低出力インピーダンスの電圧源となります。この機能により、最高 15.8V の電源で動作する単一電源 AC 結合アプリケーションで、非常に簡単にバイアスを印加できます。このバッファへの外部入力を使うと、DC 誤差補正ループや、簡単な出力 DC オフセット機能を実現できます。

類似デバイスの THS3217 も同じ機能を備えていますが、静止電力と帯域幅がより大きくなります。THS3215 と THS3217 は、テキサス・インスツルメンツの新しい AWG アプリケーション用高速 DAC である DAC38J82 などをサポートしています。

製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
THS3215	VQFN (16)	4.00mm × 4.00mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にあるパッケージ・オプションについての付録を参照してください。



ゲイン = 5V/V、差動からシングルエンドへのライン・ドライバと、オプションの外部フィルタ

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (December 2018) to Revision C (June 2021) — **Page**

- 文書全体にわたって表、図、相互参照の採番方法を更新 ... 1
- Changed the minimum *Supply current* parameter from: 23 mA to: 26 mA ... 6
- Changed the minimum *VREF input pin gain* parameter from: 0.985 V/V to: 0.975 V/V ... 6
- Changed the minimum *Noninverting input resistance* parameter from: 17.6 kΩ to: 16 kΩ ... 7
- Changed the minimum *Internal feedback resistor, R_F* parameter from: 17.6 kΩ to: 16 kΩ ... 7
- Changed the *Inverting input bias current – either input selected at T_J≈ 25°C* from: -35 µA to: -75 µA (MIN) and from: 35 µA to: 75 µA (MAX) ... 7
- Changed the maximum *Input pin bias current at 0-V input* from: 4 µA to: 15µA ... 7
- Changed the maximum *Supply current* parameter from: 37.9 mA to: 39 mA ... 10
- Changed the minimum *VREF input pin gain* parameter from: 0.985 V/V to: 0.975 V/V ... 31
- Changed the I_{bi} parameter from: -35 µA to: -75 µA (MIN) and -35 µA to: -75 µA (MAX) ... 42
- Changed the I_{bi} × R_F error term from: –7.095 µA to: -15.203 µA (MIN) and from: 7.095 µA to: 15.203 µA (MAX) ... 42
- Changed *Total error* from: –53.08 µA to: -61.19 µA (MIN) and from: 55.35 µA to: 63.46 µA (MAX) ... 42

Changes from Revision A (April 2016) to Revision B (December 2018) — **Page**

- Changed *DC output impedance* parameter: deleted maximum specification, changed test level from A to C ... 6
- Changed *DC output impedance* parameter: deleted maximum specification, changed test level from A to C ... 7
- Deleted minimum and maximum specifications from *DC output impedance* parameter ... 11

Changes from Revision * (March 2016) to Revision A (April 2016) **Page**

- データシートのステータスを製品プレビューから量産データへ変更.....1

Device Comparison Table

DEVICE	SMALL-SIGNAL BANDWIDTH 0.1 V_{PP} (A_V = 5 V/V)(1)	LARGE-SIGNAL BANDWIDTH 5V_{PP} (A_V = 5 V/V)	QUIESCENT CURRENT, Icc (±6-V SUPPLIES)	TOTAL HARMONIC DISTORTION (5 V_{PP}, R_{LOAD} = 100 Ω, 20 MHz)	CONTINUOUS OUTPUT CURRENT	PEAK OUTPUT CURRENT
THS3215	650 MHz	270 MHz	35 mA	–64 dBc	95 mA	140 mA
THS3217	800 MHz	500 MHz	55 mA	–60 dBc	120 mA	175 mA

(1) A_V is the voltage gain.

5 Pin Configuration and Functions

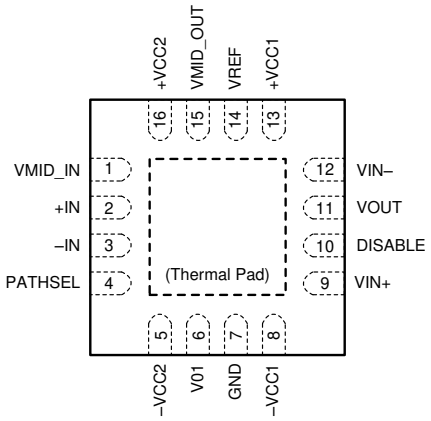


図 5-1. RGV Package 16-Pin VQFN Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	VMID_IN	Input	DC reference buffer input
2	+IN	Input	Positive signal input to D2S
3	–IN	Input	Negative signal input to D2S
4	PATHSEL	Input	Internal SPDT switch control: low selects the internal path, and high selects the external path
5	–VCC2(1)	Power	Negative supply for input stage
6	VO1	Output	D2S external output
7	GND	Power	Ground for control pins reference
8	–VCC1(1)	Power	Negative supply for output stage
9	VIN+	Input	External OPS noninverting input
10	DISABLE	Input	Output power stage shutdown control: low enables the OPS, and high disables the OPS
11	VOUT	Output	OPS output
12	VIN–	Input	OPS inverting input
13	+VCC1(1)	Power	Positive supply for output stage
14	VREF	Input	DC offsetting input to D2S
15	VMID_OUT	Output	DC reference buffer output
16	+VCC2(1)	Power	Positive supply for input stage
Thermal Pad		—	Connect the thermal pad to GND for single-supply and split-supply operation. See *セクション 10.1* section for more information.

(1) Throughout this document +V_{CC} refers to the voltage applied at the +VCC1 and +VCC2 pins, and –V_{CC} is the voltage applied at the –VCC1 and –VCC2 pins.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply, $+V_{CC} – (–V_{CC})$		16.2	V
	Input/output	$(–V_{CC}) – 0.5$	$(+V_{CC}) + 0.5$	
	Differential input voltage (IN+ – IN–)		±8	
Current	Continuous input current (IN+, IN–, VMID_IN, VIN+, VIN–)(2)		±10	mA
	Continuous output current(2)		±30	
Temperature	Operating, T_A	–55	105	°C
	Junction, T_J	–45	150	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Long-term continuous current for electromigration limits.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	Bipolar supply	±4	±6	±7.9	V
		Single supply	8	12	15.8	
T_A	Operating free-air temperature		–40	25	85	°C

6.4 Thermal Information

THERMAL METRIC(1)		THS3215 RGV (VQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	45	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics: D2S

at $+V_{CC}$ = 6.0 V, $-V_{CC}$ = –6.0 V, A_V = 2 V/V, 25-Ω source impedance, input common-mode voltage (V_{IC}) = 0.25 V, external OPS input selected (PATHSEL ≥ 1.3 V), V_{REF} = GND, R_{LOAD} = 100 Ω, and T_J ≈ 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL (1)
AC PERFORMANCE (Power Stage Disabled: DISABLE pin ≥ 1.3 V) (5)						
Small-signal bandwidth (SSBW)	V_{OUT} = 250 mV_{PP}, peaking < 1.0 dB		450		MHz	C
Large-signal bandwidth (LSBW)	V_{OUT} = 2 V_{PP}		350		MHz	C
Bandwidth for 0.2-dB flatness	V_{OUT} = 2 V_{PP}		65		MHz	C
Slew rate(2)	V_{OUT} = 4-V step		1500		V/µs	C
Overshoot and undershoot	Input t_r = 1 ns, V_{OUT} = 2-V step		2%			C
Rise and fall time	Input t_r = 1 ns, V_{OUT} = 2-V step		1.2		ns	C
Settling time to 0.1%	Input t_r = 1 ns, V_{OUT} = 2-V step		5		ns	C
2nd-order harmonic distortion (HD2)	f = 20 MHz, V_{OUT} = 2 V_{PP}		–72		dBc	C
3rd-order harmonic distortion (HD3)	f = 20 MHz, V_{OUT} = 2 V_{PP}		–88		dBc	C
Output voltage noise	f > 200 kHz		12		nV/√Hz	C
Input current noise (each input)	f > 200 kHz		2.0		pA/√Hz	C
Output impedance	f = 20 MHz		0.9		Ω	C
DC PERFORMANCE (5)						
Differential to single-ended gain	±100-mV output	1.975	2.0	2.025	V/V	A
Differential to single-ended gain drift	T_J = –40°C to +125°C		37	43	ppm/°C	B
VREF input pin gain	Differential inputs = 0 V, V_{REF} = ±100 mV	0.975	1.0	1.015	V/V	A
VREF input pin gain drift	T_J = –40°C to +125°C		–67	–74	ppm/°C	B
Output offset voltage	T_J ≈ 25°C	–35	±8	35	mV	A
	T_J = 0°C to 70°C	–37		36	mV	B
	T_J = –40°C to +125°C	–39		38	mV	B
Output offset voltage drift	T_J = –40°C to +125°C	–4	–25	–45	µV/°C	B
Input bias current – each input(3)	T_J ≈ 25°C	–4	±2	4	µA	A
	T_J = 0°C to 70°C	–4.2		4.3	µA	B
	T_J = –40°C to +125°C	–4.3		4.5	µA	B
Input bias current drift	T_J = –40°C to +125°C	3	4	5	nA/°C	B
Input offset current	T_J ≈ 25°C	–400	±50	400	nA	A
	T_J = 0°C to 70°C	–475		535	nA	B
	T_J = –40°C to +125°C	–595		700	nA	B
Input offset current drift	T_J = –40°C to +125°C	–3	0.2	3	nA/°C	B
INPUTS(4)						
Common-mode input negative supply headroom	T_J ≈ 25°C		1.8	1.9	V	A
	T_J = –40°C to +85°C			2.0	V	B
Common-mode input positive supply headroom	T_J ≈ 25°C		1.3	1.4	V	A
	T_J = –40°C to +125°C			1.5	V	B
Common-mode rejection ratio (CMRR)	–1 V ≤ V_{IC} ≤ 3 V	42	48		dB	A
Input impedance differential mode	V_{CM} = 0 V		20 || 2.3		kΩ || pF	C
Input impedance common mode	V_{CM} = 0 V		20 || 2.3		kΩ || pF	C
OUTPUT(6)						
Output voltage headroom to either supply	T_J ≈ 25°C	1.4	1.5	1.75	V	A
	T_J = –40°C to +85°C			1.95	V	B

6.5 Electrical Characteristics: D2S (continued)

at $+V_{CC}$ = 6.0 V, $–V_{CC}$ = –6.0 V, A_V = 2 V/V, 25-Ω source impedance, input common-mode voltage (V_{IC}) = 0.25 V, external OPS input selected (PATHSEL ≥ 1.3 V), V_{REF} = GND, R_{LOAD} = 100 Ω, and T_J ≈ 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL (1)
Output current drive	±0.8 V_{PP}, R_{LOAD} = 20 Ω	±35	±45		mA	A
DC output impedance	Load current = ±20 mA		0.3		Ω	C
POWER SUPPLY (D2S + Midsupply Buffer Only; OPS Disabled: DISABLE pin ≥ 1.3 V)						
Supply current	±6-V supplies	20.2	21.3	26	mA	A
Supply current temperature coefficient			8		µA/°C	C
Positive power-supply rejection ratio (+PSRR)	Referred to input	62	71		dB	A
Negative power-supply rejection ratio (–PSRR)	Referred to input	61	71		dB	A

(1) Test levels (all values set by characterization and simulation): (A) 100% tested at T_A≈ T_J≈ 25°C; over temperature limits by characterization and simulation. (B) Not tested in production; limits set by characterization and simulation. (C) Typical value only for information. DC limits tested with no self-heating. Add internal self heating to T_A for T_J.
(2) This slew rate is the average of the rising and falling time estimated from the large-signal bandwidth as: (Vpeak / $\sqrt{2}$) × 2π × $f_{–3dB}$.
(3) Currents out of pin treated as a positive polarity.
(4) Applies to input pins 2 (IN+) and 3 (IN–).
(5) Output measured at pin 6.
(6) Output measured at pin 6.

6.6 Electrical Characteristics: OPS

at $+V_{CC}$ = 6.0 V, $–V_{CC}$ = –6.0 V, 25-Ω D2S source impedance, D2S input common-mode voltage (V_{IC}) = 0.25 V, V_{REF} = GND, R_F = 249 Ω(1), R_G = 162 Ω, A_V = 2.5 V/V, OPS R_{LOAD} = 100 Ω, OPS enabled (DISABLE ≤ 0.7 V or floated), external OPS input selected (PATHSEL ≥ 1.3 V), and T_J ≈ 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL (2)
AC PERFORMANCE (4)						
Small-signal bandwidth (SSBW)	V_{OUT} = 100 mV_{PP}, peaking < 2.0 dB		700		MHz	C
Large-signal bandwidth (LSBW)	V_{OUT} = 5 V_{PP}		270		MHz	C
Bandwidth for 0.2-dB flatness	V_{OUT} = 5 V_{PP}		110		MHz	C
Slew rate(3)	V_{OUT} = 5-V step		3000		V/µs	C
Overshoot and undershoot	Input t_r = 1 ns, V_{OUT} = 5-V step		4%			C
Rise and fall time	Input t_r = 1 ns, V_{OUT} = 5-V step		1.7		ns	C
Settling time to 0.1%	Input t_r = 1 ns, V_{OUT} = 5-V step		25		ns	C
2nd-order harmonic distortion (HD2)	f = 20 MHz, V_{OUT}= 5 V_{PP}		–66		dBc	C
3rd-order harmonic distortion (HD3)	f = 20 MHz, V_{OUT}= 5 V_{PP}		–68		dBc	C
Noninverting input voltage noise	f > 200 kHz		2.7		nV/$\sqrt{Hz}$	C
Noninverting input current noise	f > 200 kHz		1.3		pA/$\sqrt{Hz}$	C
Inverting input current noise	f > 200 kHz		18		pA/$\sqrt{Hz}$	C
Closed-loop ac output impedance	f = 20 MHz		0.25		Ω	C

6.6 Electrical Characteristics: OPS (continued)

at $+V_{CC}$ = 6.0 V, $-V_{CC}$ = –6.0 V, 25-Ω D2S source impedance, D2S input common-mode voltage (V_{IC}) = 0.25 V, V_{REF} = GND, R_F = 249 Ω(1), R_G = 162 Ω, A_V = 2.5 V/V, OPS R_{LOAD} = 100 Ω, OPS enabled (DISABLE ≤ 0.7 V or floated), external OPS input selected (PATHSEL ≥ 1.3 V), and T_J ≈ 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL (2)
DC PERFORMANCE (4)						
Open-loop transimpedance gain(1)	V_{OUT} = ±1 V, R_{LOAD}= 500-Ω	800	1700		kΩ	A
Closed-loop gain	0.1% external R_F and R_G resistors	2.495	2.515	2.53	V/V	A
INPUT						
External input offset voltage (pin 9 to pin 12)	T_J ≈ 25°C	–12	±2.5	12	mV	A
	T_J = 0°C to 70°C	–13		12.5	mV	B
	T_J = –40°C to +125°C	–14.1		13.7	mV	B
External input offset voltage drift (pin 9 to pin 12)	T_J = –40°C to +125°C	–3	–12	–21	µV/°C	B
Internal input offset voltage (pin 6 to pin 12)	T_J ≈ 25°C	–15	±2.5	15	mV	A
	T_J = 0°C to 70°C	–15.7		15.4	mV	B
	T_J = –40°C to +125°C	–16.6		16	mV	B
Internal input offset voltage drift (pin 6 to pin 12)	T_J = –40°C to +125°C	–3	–10	–16	µV/°C	B
External to internal input offset voltage match		–7	±1.2	7	mV	C
External noninverting input bias current (pin 9)(5)	T_J ≈ 25°C	–5	±5	15	µA	A
	T_J = 0°C to 70°C	–5		15.2	µA	B
	T_J = –40°C to +125°C	–5.2		15.4	µA	B
External noninverting input bias current drift (pin 9)	T_J = –40°C to +125°C	0	2	3.3	nA/°C	B
Inverting input bias current – either input selected(5)	T_J ≈ 25°C	–75	±5	75	µA	A
	T_J = 0°C to 70°C	–39		37	µA	B
	T_J = –40°C to +125°C	–43.5		40.5	µA	B
Inverting input bias current drift	T_J = –40°C to +125°C	–15	–50	–85	nA/°C	B
Input headroom to either supply			2.6	3.0	V	A
Common-mode rejection ratio (CMRR)	±3.4-V input range	45	53		dB	A
Noninverting input resistance		16	18.5	22.4	kΩ	A
Noninverting input capacitance			3.3		pF	C
Open-loop inverting input impedance			74		Ω	C
OUTPUT(6)						
Output voltage headroom to either supply	R_{LOAD} = 500 Ω, T_J ≈ 25°C	1.3	1.4	1.6	V	A
	R_{LOAD} = 500 Ω, T_J = –40°C to +125°C			1.8	V	B
Linear output current	±1.7 V into 20-Ω R_{LOAD}	75	90		mA	A
Peak output current	±2.6-V into 20-Ω R_{LOAD}	120	140		mA	A
DC output impedance	0-V output, load current = ±40 mA		0.05		Ω	C
Internal feedback resistor, R_F	Between pins 11 and 12	16	18.5	22.4	kΩ	A

6.6 Electrical Characteristics: OPS (continued)

at $+V_{CC}$ = 6.0 V, $–V_{CC}$ = –6.0 V, 25-Ω D2S source impedance, D2S input common-mode voltage (V_{IC}) = 0.25 V, V_{REF} = GND, R_F = 249 Ω(1), R_G = 162 Ω, A_V = 2.5 V/V, OPS R_{LOAD} = 100 Ω, OPS enabled (DISABLE ≤ 0.7 V or floated), external OPS input selected (PATHSEL ≥ 1.3 V), and T_J ≈ 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL (2)
PATHSEL (Pin 4; Logic Reference = Pin 7 = GND)						
Input low logic level	Internal path selected	0.7	0.9		V	A
Input high logic level	External input selected at VIN pin		0.9	1.3	V	A
Input voltage range		–0.5		$+V_{CC}$	V	A
PATHSEL voltage when floated	Internal input from D2S selected	0	20	40	mV	A
Input pin bias current(7)	0-V input	0		15	µA	A
	3.3-V input	–150		–250	µA	A
Input pin impedance			18 || 1.5		kΩ || pF	C
Switching time	To 1% of final value		80		ns	C
Input switching glitch	Both inputs at GND		50		mV	C
Deselected input dc isolation	± 2-V input	70	80		dB	A
Deselected input ac isolation	2 V_{PP}, at 20-MHz input	55	65		dB	C
DISABLE (Pin 10; Logic Reference = Pin 7 = GND)						
Input low logic level		0.7	0.9		V	A
Input high logic level			0.9	1.3	V	A
Shutdown control voltage range		–0.5		$+V_{CC}$	V	B
Shutdown voltage when floated	Output stage enabled	0	20	40	mV	A
Input pin bias current(7)	0-V input	0		4	µA	A
	3.3-V input	–150		–250	µA	A
Input pin impedance			18 || 1.5		kΩ || pF	C
Switching time (turn on or off)	To 10% of final value		200		ns	C
Shutdown dc isolation (either input)	±2-V input	70	80		dB	A
Shutdown ac isolation (either input)	2 V_{PP} at 20-MHz input	55	65		dB	C
POWER SUPPLY						
Supply current (OPS only)	±6-V supplies	9.6	10.8	12	mA	A
Disabled supply current in OPS	±6-V supplies	1.5	2	2.9	mA	B
Logic reference current at pin 7(7)	Pins 4, 7, and 10 held at 0 V	200	280	380	µA	A
Positive power-supply rejection ratio (+PSRR)	Referred to input	55	60		dB	A
Negative power-supply rejection ratio (–PSRR)	Referred to input	53	56		dB	A

(1) Output power stage includes an internal 18.5-kΩ feedback resistor. This internal resistor, in parallel with an external 249-Ω R_F and 162-Ω R_G, results in a gain of 2.5 V/V after including a nominal gain loss of 0.9935 V/V due to the input buffer and loop-gain effects.
(2) Test levels (all values set by characterization and simulation): (A) 100% tested at T_A≈ T_J≈ 25°C; over temperature limits by characterization and simulation. (B) Not tested in production; limits set by characterization and simulation. (C) Typical value only for information. DC limits tested with no self-heating. Add internal self heating to T_A for T_J.
(3) This slew rate is the average of the rising and falling time estimated from the large-signal bandwidth as: (Vpeak / $\sqrt{2}$) × 2π × $f_{–3dB}$.
(4) Output measured at pin 11.
(5) Currents out of pin treated as a positive polarity.
(6) Output measured at pin 11.
(7) Currents out of pin treated as a positive polarity.

6.7 Electrical Characteristics: D2S + OPS

at $+V_{CC}$ = 6.0 V, $–V_{CC}$ = –6.0 V, 25-Ω D2S source impedance, D2S input V_{IC} = 0.25 V, internal path selected to OPS (PATHSEL ≤ 0.7 V or floated), V_{REF} = GND, combined A_V = 5 V/V, D2S R_{LOAD}= 200 Ω, R_F = 249 Ω(1), R_G = 162 Ω (OPS A_V = 2.5 V/V), OPS enabled (DISABLE ≤ 0.7 V or floated), OPS R_{LOAD} = 100 Ω, and T_J ≈ 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL (2)
AC PERFORMANCE(4)						
Small-signal bandwidth (SSBW)	V_{OUT} = 100 mV_{PP}, peaking < 1.5 dB		650		MHz	C
Large-signal bandwidth (LSBW)	V_{OUT} = 5 V_{PP}		270		MHz	C
Bandwidth for 0.2-dB flatness	V_{OUT} = 2 V_{PP}		110		MHz	C
Slew rate(3)	V_{OUT} = 8-V step		3000		V/µs	C
Overshoot and undershoot	Input t_r = 1 ns, V_{OUT} = 5-V step		4%			C
Rise and fall time	Input t_r = 1 ns, V_{OUT} = 5-V step		1.7		ns	C
Settling time to 0.1%	Input t_r = 1 ns, V_{OUT} = 5-V step		25		ns	C
2nd-order harmonic distortion (HD2)	f = 20 MHz, V_{OUT}= 5 V_{PP}		–66		dBc	C
3rd-order harmonic distortion (HD3)	f = 20 MHz, V_{OUT}= 5 V_{PP}		–68		dBc	C
Output voltage noise	f > 200 kHz, A_V = 5 V/V		33		nV/√Hz	C
DC PERFORMANCE(4)						
Total gain D2S to OPS output(1)	0.1% tolerance external resistors, dc, ±100-mV output test	4.92	5.02	5.12	V/V	A
POWER SUPPLY (Combined D2S, OPS, and Midscale Reference Buffer)						
Supply current	±6-V supplies	32.7	34.5	39	mA	A
Supply current temperature coefficient	T_J = 0°C to 100°C		±5		µA/°C	C

(1) Output power stage includes an internal 18.5-kΩ feedback resistor. This internal resistor, in parallel with an external 249-Ω R_F and 162-Ω R_G, results in a gain of 2.5 V/V after including a nominal gain loss of 0.9935 V/V due to the input buffer and loop-gain effects.
(2) Test levels (all values set by characterization and simulation): (A) 100% tested at T_A≈ T_J≈ 25°C; over temperature limits by characterization and simulation. (B) Not tested in production; limits set by characterization and simulation. (C) Typical value only for information.
(3) This slew rate is the average of the rising and falling time estimated from the large-signal bandwidth as: (Vpeak / √2) × 2π × $f_{–3dB}$.
(4) Output measured at pin 11.

6.8 Electrical Characteristics: Midscale (DC) Reference Buffer

at $+V_{CC}$ = 6.0 V, $-V_{CC}$ = –6.0 V, R_{LOAD} = 150 Ω at pin 15, and T_J ≈ 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL (1)
AC PERFORMANCE (Output measured at pin 15)						
Small-signal bandwidth (SSBW)	V_{OUT} = 100 mV_{PP}		200		MHz	C
Large-signal bandwidth (LSBW)	V_{OUT} = 1 V_{PP}		50		MHz	C
Slew rate(2)	V_{OUT} = 4-V step		110		V/µs	C
Input voltage noise	f > 5 kHz		4.6		nV/√Hz	C
Input current noise	f > 5 kHz		1.3		pA/√Hz	C
AC output impedance	f = 20 MHz, no load current		2.5		Ω	C
DC AND I/O PERFORMANCE (R_S = 25 Ω, and output measured at pin 15, unless otherwise noted)						
Buffer gain	V_I = ±1 V, R_{LOAD} = 200 Ω	.9985	0.999	1.001	V/V	A
Buffer gain drift	T_J = –40°C to +125°C		–1.2	–2.2	ppm/°C	B
Output offset from midsupply	Input floating, pin 1 open	–120	30	70	mV	A
Output offset voltage	Input driven to 0 V from 0-Ω source	–1.0	4.0	15	mV	A
Input offset voltage drift	T_J = –40°C to +125°C, input driven to 0 V	4	9	15	µV/°C	B
Input bias current(3)		–10	±1	10	µA	A
Input bias current drift	T_J = –40°C to +125°C	–5	±1	5	nA/°C	B
Input/output headroom to either supply	gain change < 1%		1.1	1.4	V	A
Input impedance	Internal 50-kΩ divider resistors to each supply		22 || 1.5		kΩ || pF	C
Linear output current into resistive load	±1.62 V into 36 Ω	40	65		mA	A
DC output impedance	Load current = ±30 mA		0.3		Ω	C
Positive power-supply rejection ratio (+PSRR)	Referred to input with VMID_IN (pin 1) at GND	60			dB	A
Negative power-supply rejection ratio (—PSRR)	Referred to input with VMID_IN (pin 1) at GND	69			dB	A

(1) Test levels (all values set by characterization and simulation): (A) 100% tested at T_A≈ T_J≈ 25°C; over temperature limits by characterization and simulation. (B) Not tested in production; limits set by characterization and simulation. (C) Typical value only for information.
(2) This slew rate is the average of the rising and falling time estimated from the large-signal bandwidth as: $(V_{PEAK} / \sqrt{2}) \times 2\pi \times f_{-3dB}$.
(3) Currents out of pin treated as a positive polarity.

6.9 Typical Characteristics: D2S + OPS

at $+V_{CC}$ = 6 V, $–V_{CC}$ = –6 V, 25-Ω D2S source impedance , V_{IC} = 0.25 V, internal path selected (PATHSEL = GND), V_{REF} = GND, D2S R_{LOAD} = 200 Ω at pin 6, R_F = 249 Ω, R_G = 162 Ω, OPS A_V = 2.5 V/V, OPS On (DISABLE = GND), OPS R_{LOAD} = 100 Ω at pin 11, and T_J ≈ 25°C (unless otherwise noted)

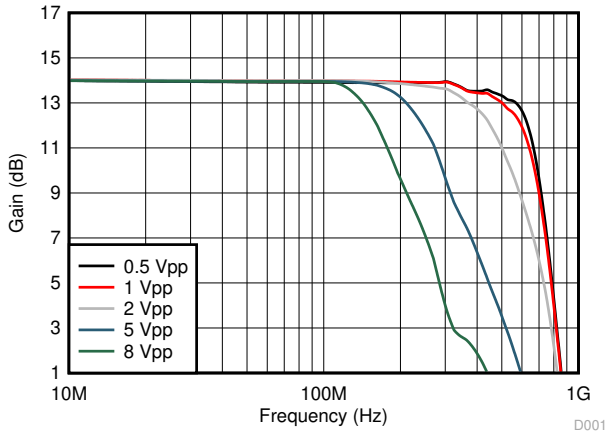


図 6-1. Frequency Response vs Output Voltage

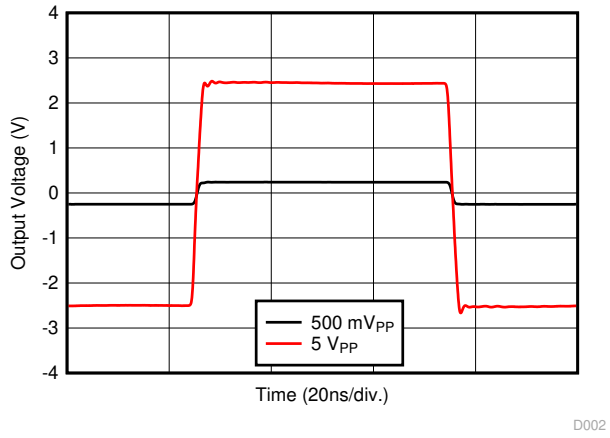


図 6-2. Small- and Large-Signal Step Response

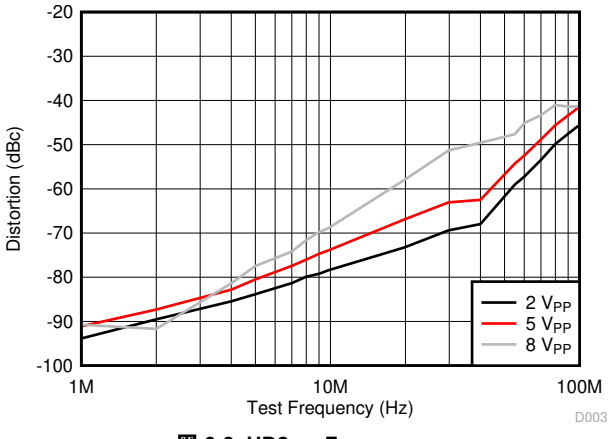


図 6-3. HD2 vs Frequency

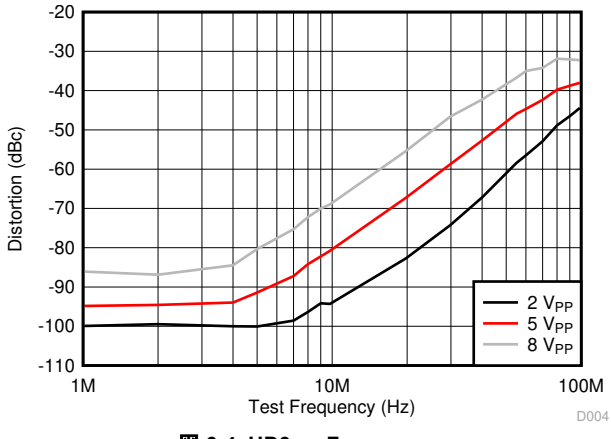
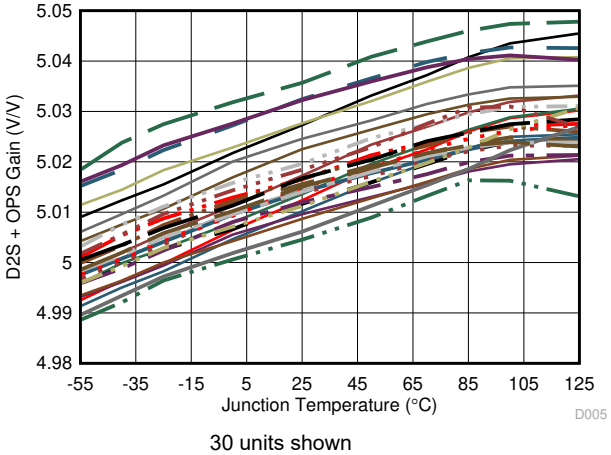
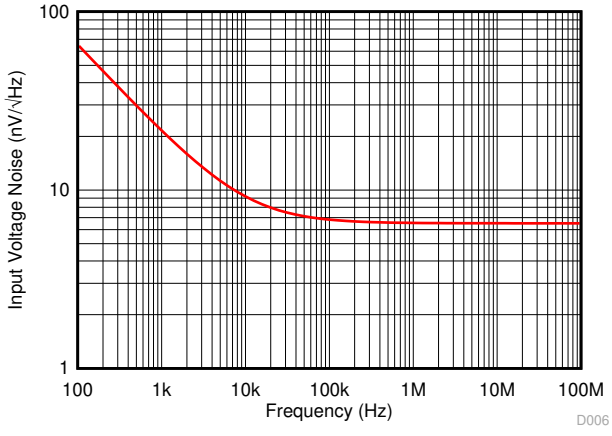


図 6-4. HD3 vs Frequency



30 units shown

図 6-5. Gain vs Temperature

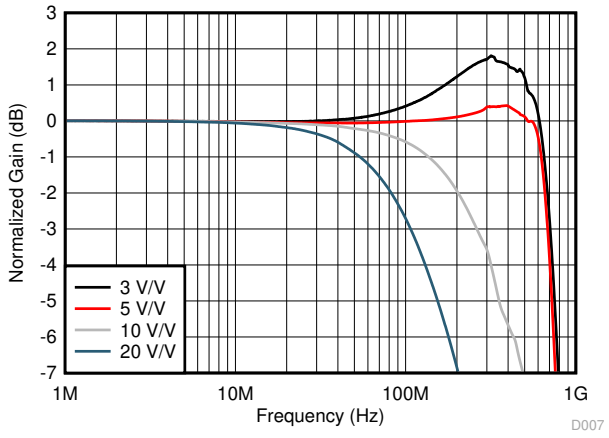


25-Ω source impedance on each D2S input

図 6-6. Input-Referred Differential Noise

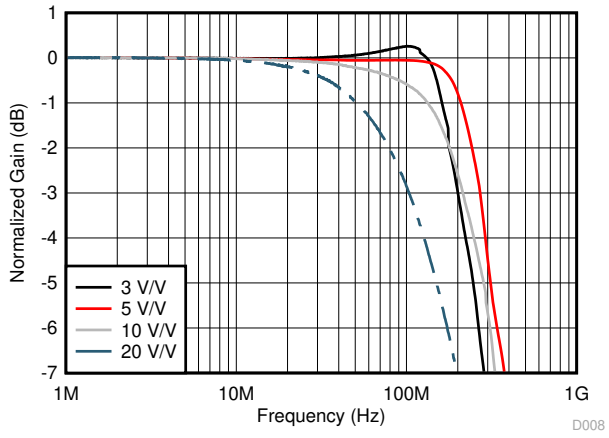
6.9 Typical Characteristics: D2S + OPS (continued)

at $+V_{CC}$ = 6 V, $–V_{CC}$ = –6 V, 25-Ω D2S source impedance , V_{IC} = 0.25 V, internal path selected (PATHSEL = GND), V_{REF} = GND, D2S R_{LOAD} = 200 Ω at pin 6, R_F = 249 Ω, R_G = 162 Ω, OPS A_V = 2.5 V/V, OPS On (DISABLE = GND), OPS R_{LOAD} = 100 Ω at pin 11, and T_J ≈ 25°C (unless otherwise noted)



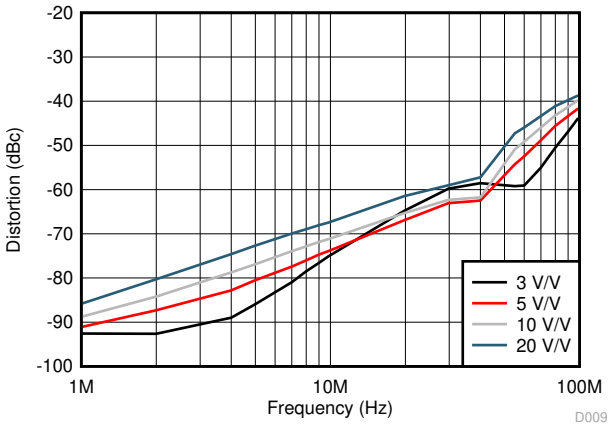
V_{OUT} = 500 mV_{PP}, see 表 8-1

図 6-7. Small-Signal Frequency Response vs Gain



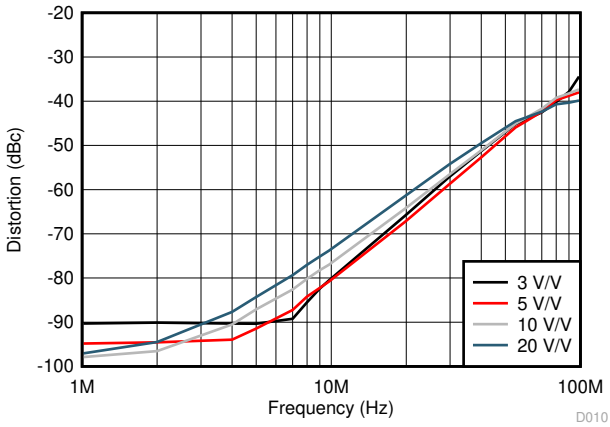
V_{OUT} = 5 V_{PP}, see 表 8-1

図 6-8. Large-Signal Frequency Response vs Gain



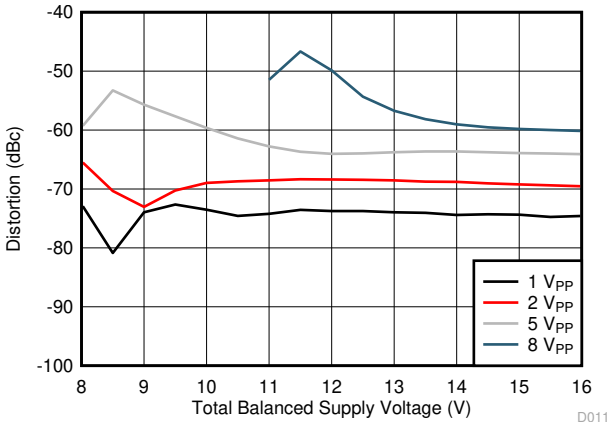
V_{OUT} = 5 V_{PP}, see 表 8-1

図 6-9. HD2 vs Gain



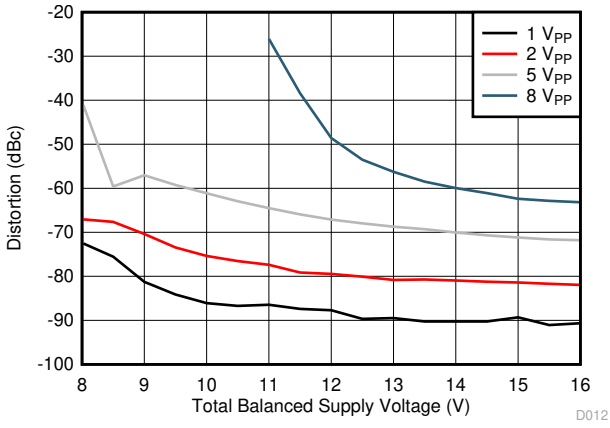
V_{OUT} = 5 V_{PP}, see 表 8-1

図 6-10. HD3 vs Gain



Test frequency = 20 MHz

図 6-11. HD2 vs Supply Voltage

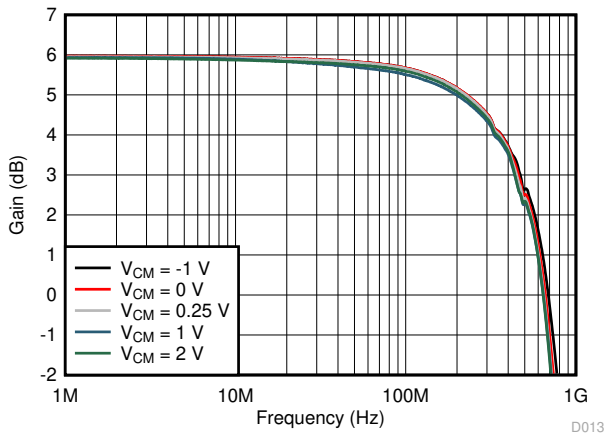


Test frequency = 20 MHz

図 6-12. HD3 vs Supply Voltage

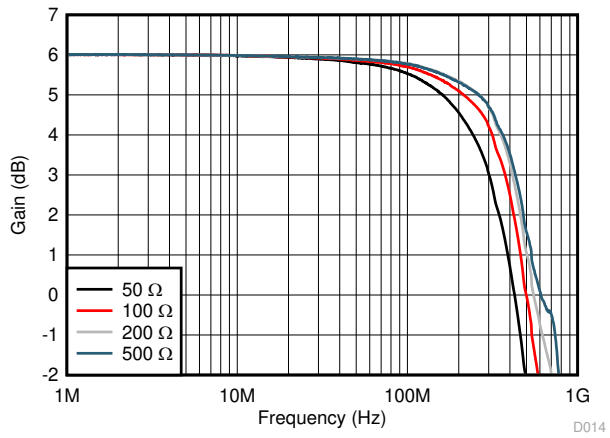
6.10 Typical Characteristics: D2S Only

at $+V_{CC}$ = 6.0 V, $-V_{CC}$ = –6.0 V, fixed gain of 2 V/V, 25-Ω D2S source impedance, V_{IC} = 0.25 V, external path selected (PATHSEL = $+V_{CC}$), V_{REF} = GND, D2S R_{LOAD} = 100 Ω at pin 6, and $T_J \approx 25°C$ (unless otherwise noted)



V_{OUT} = 250 mV_{PP}

図 6-13. Frequency Response vs Input Common-Mode Voltage



V_{OUT} = 2 V_{PP}

図 6-14. Frequency Response vs Load Resistance

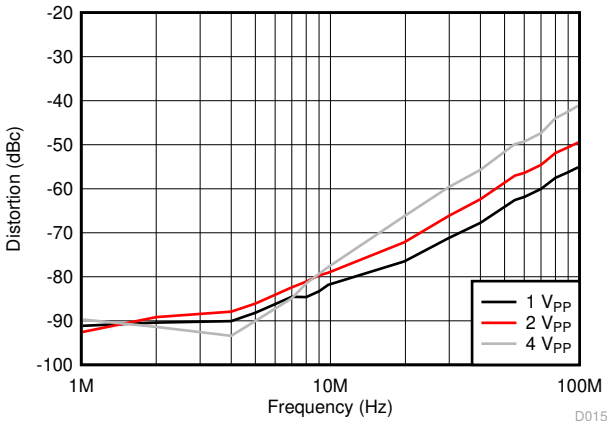


図 6-15. HD2 vs Output Voltage

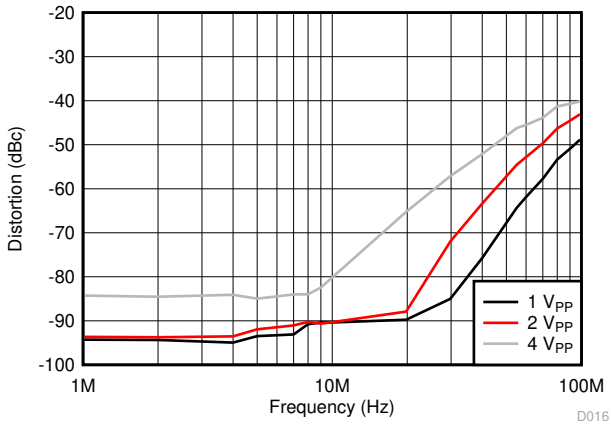


図 6-16. HD3 vs Output Voltage

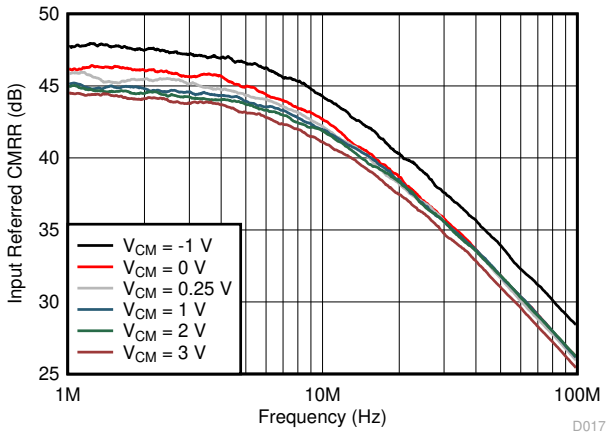


図 6-17. Common-Mode Rejection Ratio vs Input Common-Mode Voltage

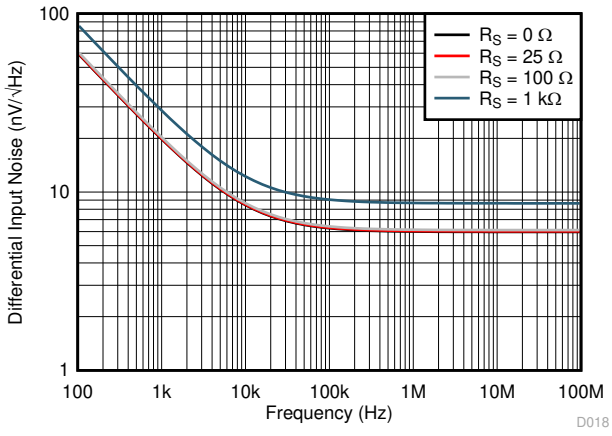
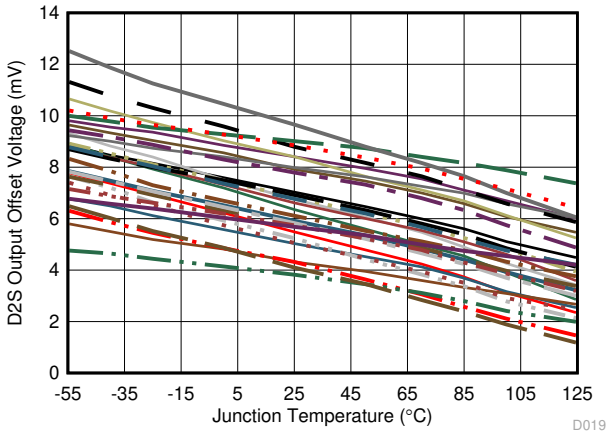


図 6-18. Differential Input Noise vs Source Impedance

6.10 Typical Characteristics: D2S Only (continued)

at $+V_{CC}$ = 6.0 V, $-V_{CC}$ = –6.0 V, fixed gain of 2 V/V, 25-Ω D2S source impedance, V_{IC} = 0.25 V, external path selected (PATHSEL = $+V_{CC}$), V_{REF} = GND, D2S R_{LOAD} = 100 Ω at pin 6, and $T_J \approx 25°C$ (unless otherwise noted)



30 units shown

図 6-19. Output DC Offset Voltage vs Die Temperature

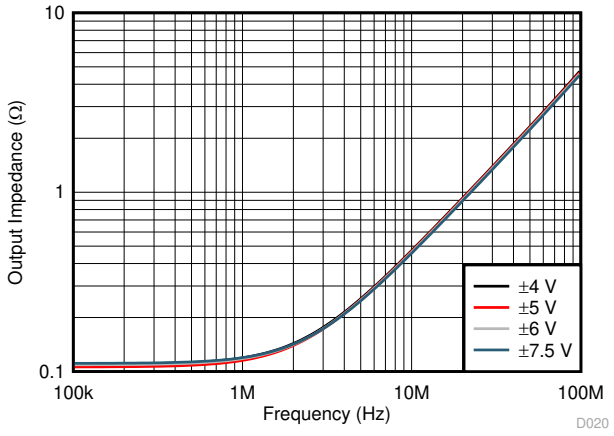
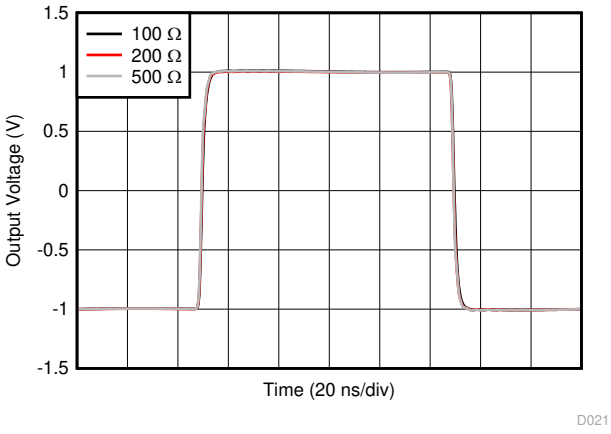
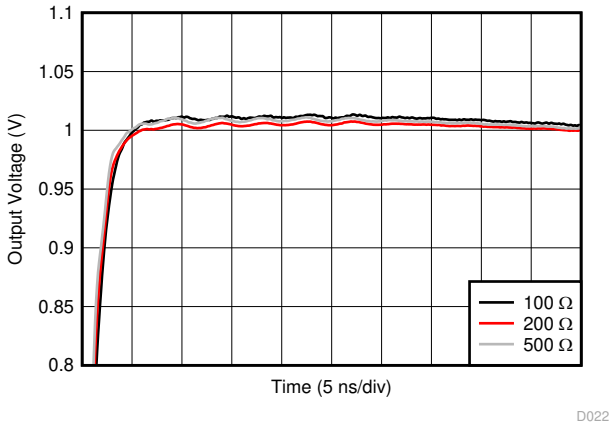


図 6-20. Output Impedance vs Supply Voltage



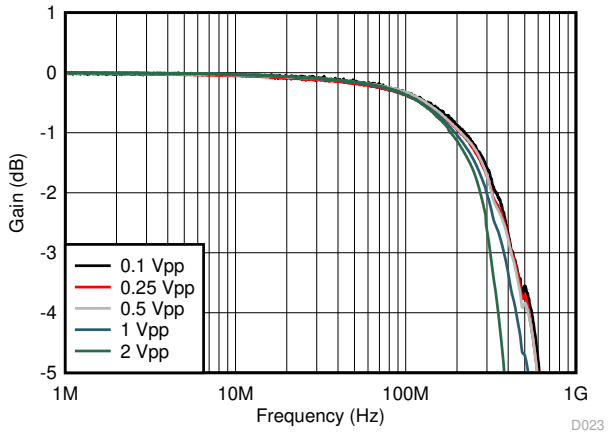
±1-V output pulse

図 6-21. Large-Signal Step Response vs Load Resistance



±1-V output pulse

図 6-22. Large-Signal Pulse Settling Response vs Load Resistance



25-Ω D2S source impedance on each input

図 6-23. VREF Input Pin Frequency Response

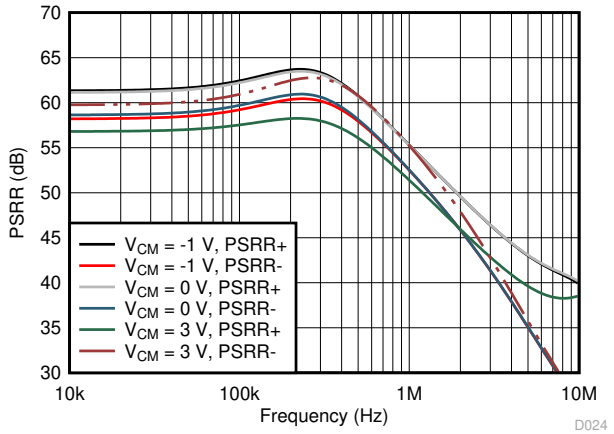
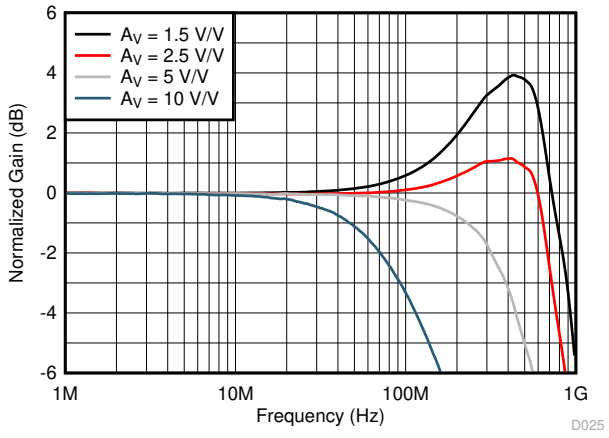


図 6-24. Simulated Power-Supply Rejection Ratio vs Input Common-Mode Voltage

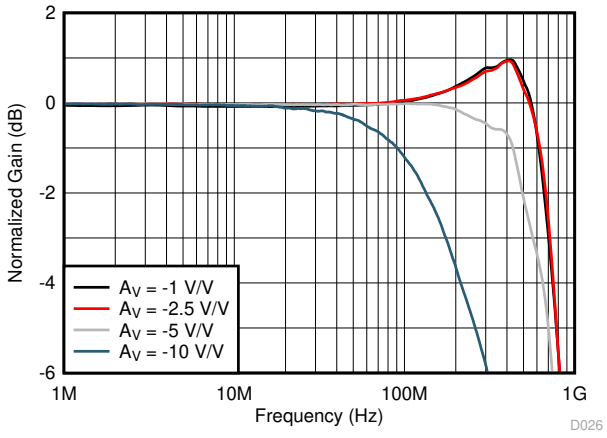
6.11 Typical Characteristics: OPS Only

at $+V_{CC}$ = 6.0 V, $–V_{CC}$ = –6.0 V, 25-Ω D2S source impedance, V_{REF} = GND, R_F = 249 Ω, R_G = 162 Ω, OPS A_V = 2.5V/V, OPS R_{LOAD} = 100 Ω at pin 11, OPS enabled (DISABLE = GND), external input path selected (PATHSEL = $+V_{CC}$), and $T_J \approx 25°C$ (unless otherwise noted)



V_{OUT} = 100 mV_{PP}, see 表 8-1 for R_F values vs gain

図 6-25. Frequency Response vs Noninverting Gain



V_{OUT} = 100 mV_{PP}, see 表 8-3 for R_F values vs gain

図 6-26. Frequency Response vs Inverting Gain

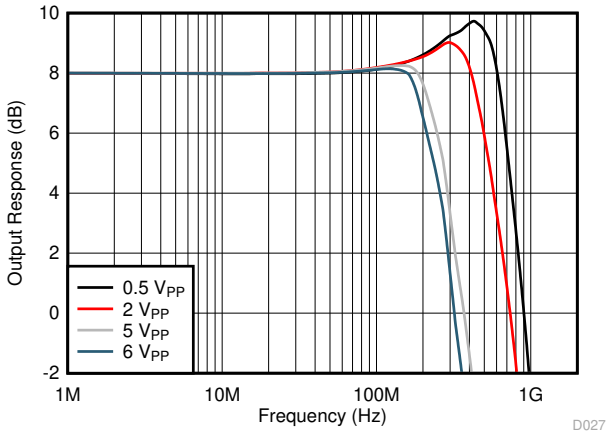
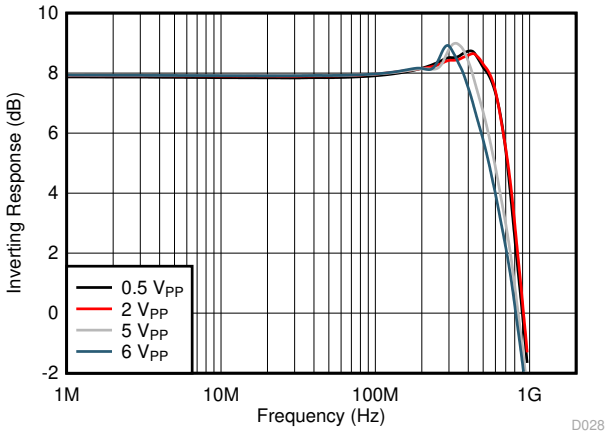


図 6-27. Noninverting Response vs Output Voltage



A_V = –2.5 V/V, see 表 8-3 for R_F value

図 6-28. Inverting Response vs Output Voltage

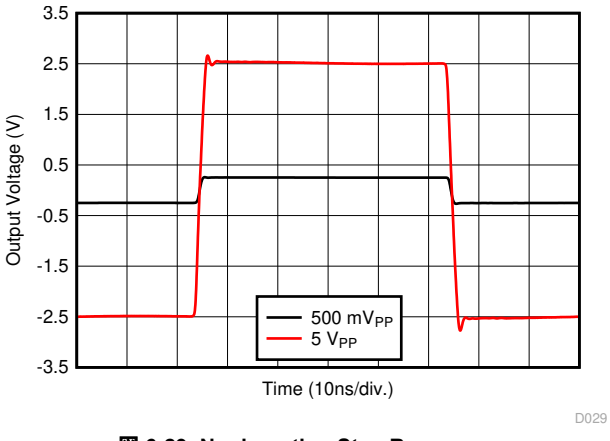
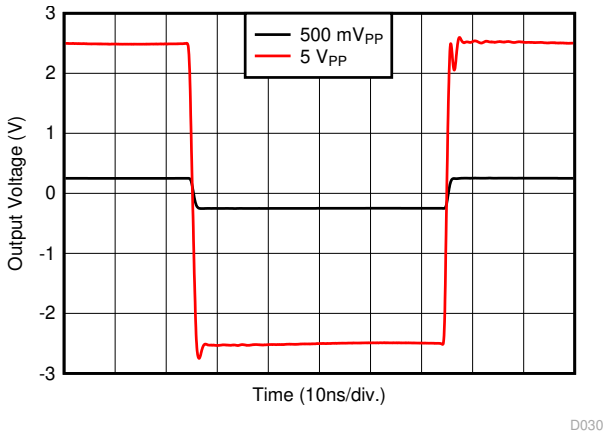


図 6-29. Noninverting Step Response



A_V = –2.5 V/V, see 表 8-3 for R_F value

図 6-30. Inverting Step Response

6.11 Typical Characteristics: OPS Only (continued)

at $+V_{CC}$ = 6.0 V, $-V_{CC}$ = –6.0 V, 25-Ω D2S source impedance, V_{REF} = GND, R_F = 249 Ω, R_G = 162 Ω, OPS A_V = 2.5V/V, OPS R_{LOAD} = 100 Ω at pin 11, OPS enabled (DISABLE = GND), external input path selected (PATHSEL = $+V_{CC}$), and $T_J \approx 25°C$ (unless otherwise noted)

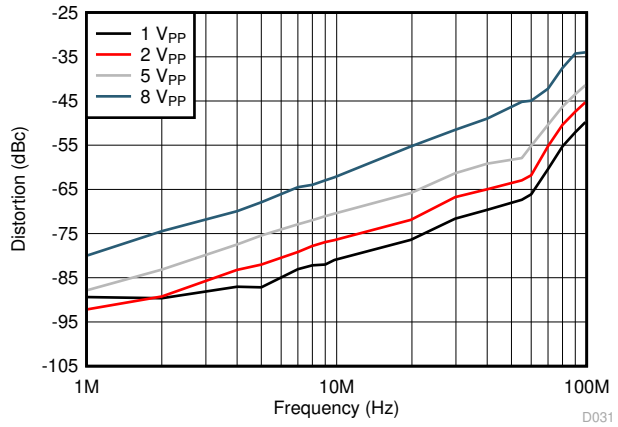


図 6-31. HD2 vs Output Voltage

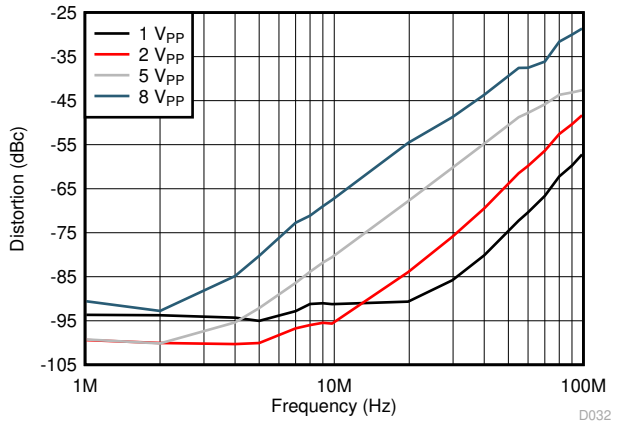
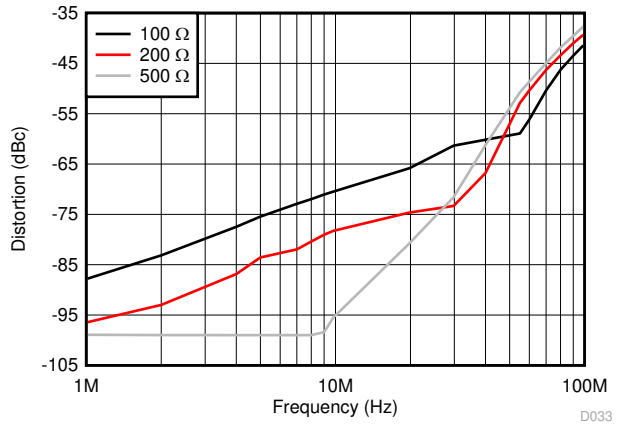
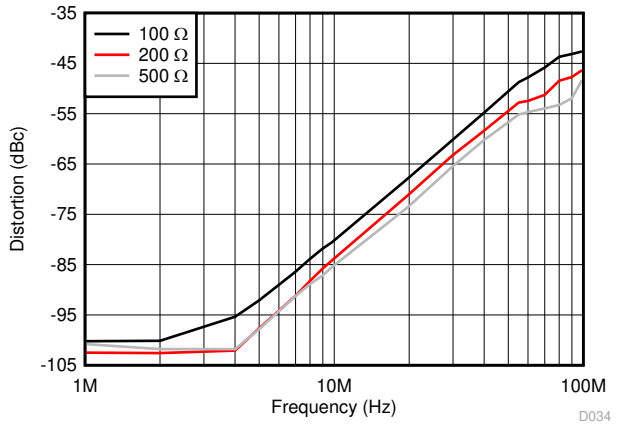


図 6-32. HD3 vs Output Voltage



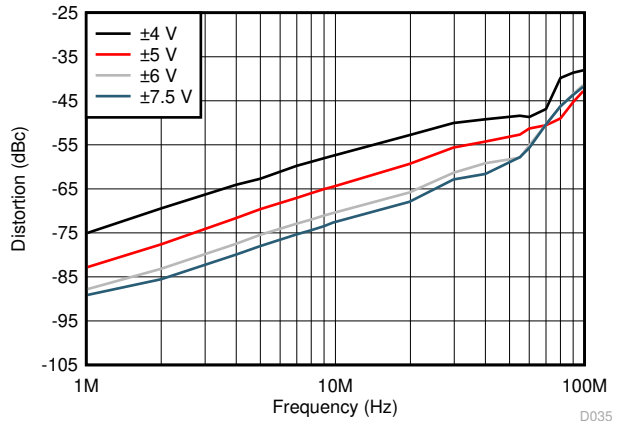
V_{OUT} = 5 V_{PP}

図 6-33. HD2 vs Load Resistance



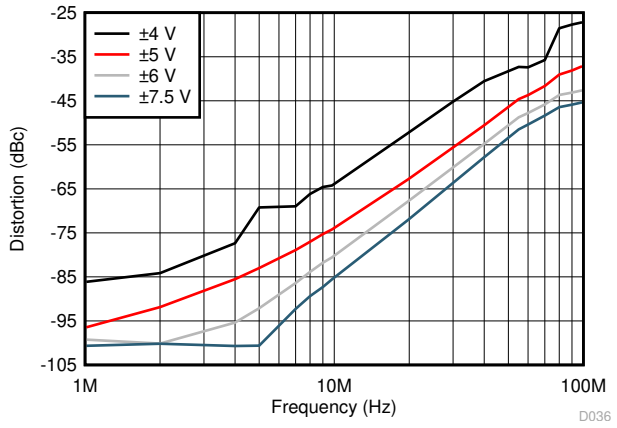
V_{OUT} = 5 V_{PP}

図 6-34. HD3 vs Load Resistance



V_{OUT} = 5 V_{PP}

図 6-35. HD2 vs Supply Voltage

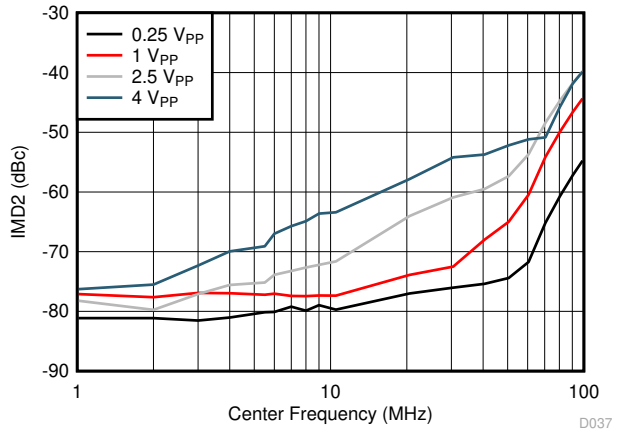


V_{OUT} = 5 V_{PP}

図 6-36. HD3 vs Supply Voltage

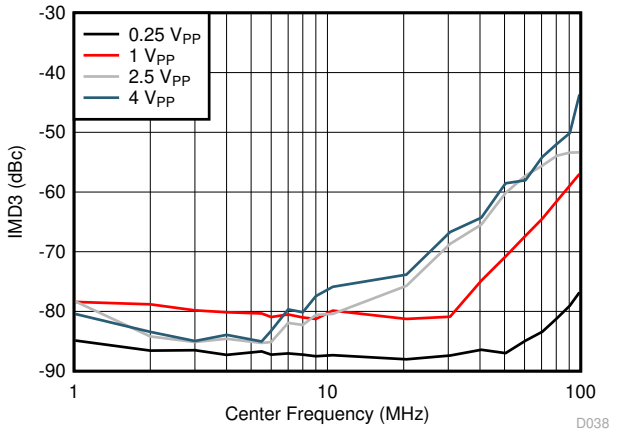
6.11 Typical Characteristics: OPS Only (continued)

at $+V_{CC}$ = 6.0 V, $–V_{CC}$ = –6.0 V, 25-Ω D2S source impedance, V_{REF} = GND, R_F = 249 Ω, R_G = 162 Ω, OPS A_V = 2.5V/V, OPS R_{LOAD} = 100 Ω at pin 11, OPS enabled (DISABLE = GND), external input path selected (PATHSEL = $+V_{CC}$), and $T_J \approx 25°C$ (unless otherwise noted)



±100-kHz tone separation, output voltage for each tone

図 6-37. Second-Order Intermodulation Distortion vs Output Voltage



±100-kHz tone separation, output voltage for each tone

図 6-38. Third-Order Intermodulation Distortion vs Output Voltage

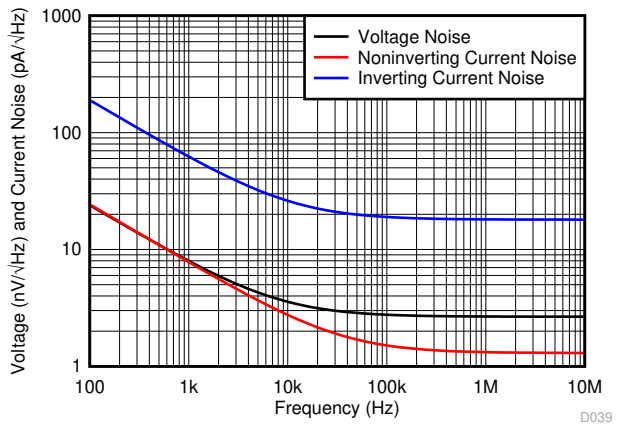
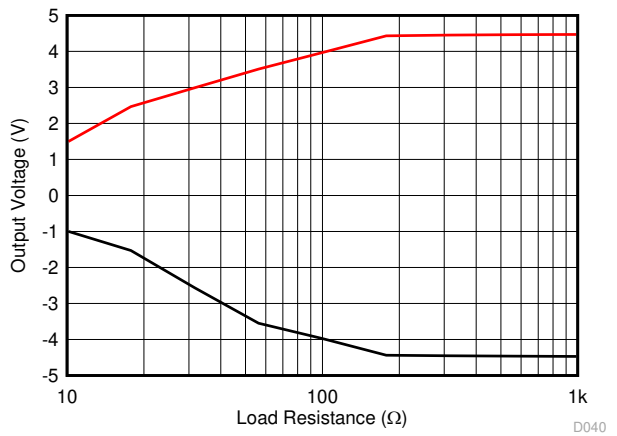
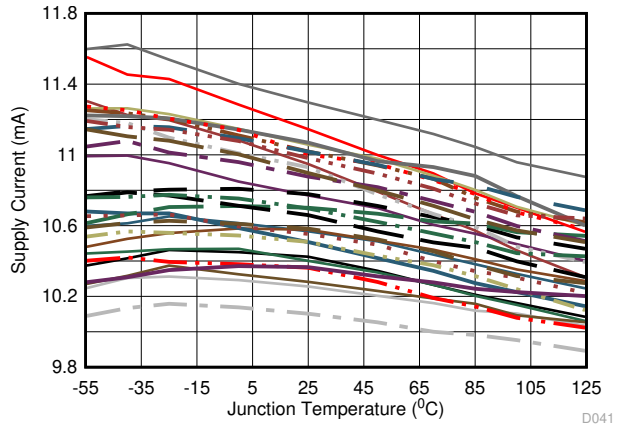


図 6-39. Input-Referred Spot Noise vs Frequency



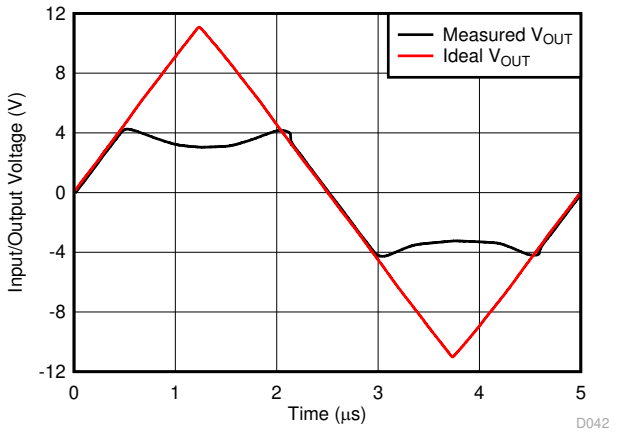
Output swing with better than 0.1% linearity

図 6-40. Linear Output Swing vs Load Resistance



30 units shown

図 6-41. Quiescent Supply Current vs Temperature

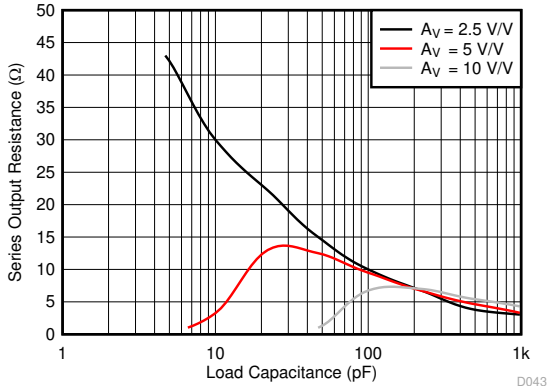


±4.5-V input triangular wave, OPS A_V = –2.5 V/V

図 6-42. Output Overdrive Response

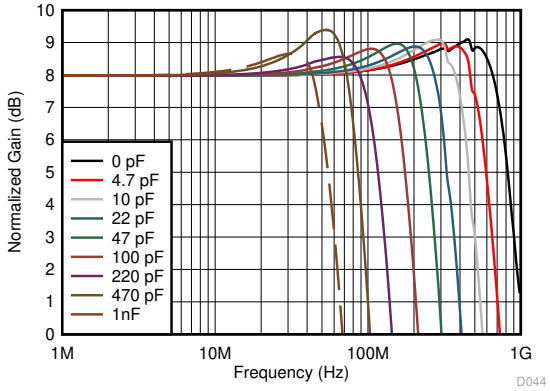
6.11 Typical Characteristics: OPS Only (continued)

at $+V_{CC}$ = 6.0 V, $-V_{CC}$ = –6.0 V, 25-Ω D2S source impedance, V_{REF} = GND, R_F = 249 Ω, R_G = 162 Ω, OPS A_V = 2.5V/V, OPS R_{LOAD} = 100 Ω at pin 11, OPS enabled (DISABLE = GND), external input path selected (PATHSEL = $+V_{CC}$), and $T_J \approx 25°C$ (unless otherwise noted)



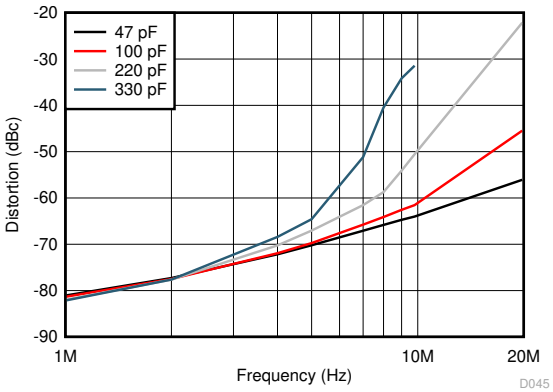
See 表 8-6 for R_F values vs OPS gain

図 6-43. Series Output Resistance vs Load Capacitance



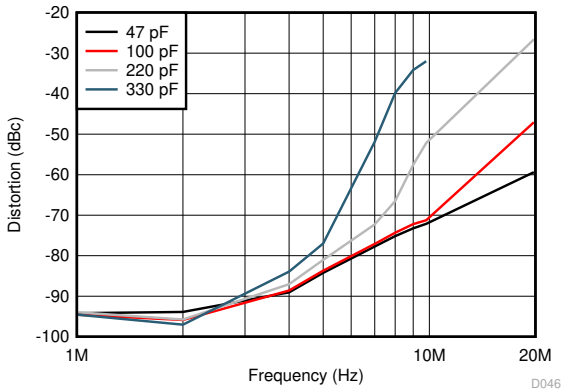
V_{OUT} = 500 mV_{PP}, see Series Output Resistance vs Load Capacitance for R_S value

図 6-44. Frequency Response vs Load Capacitance



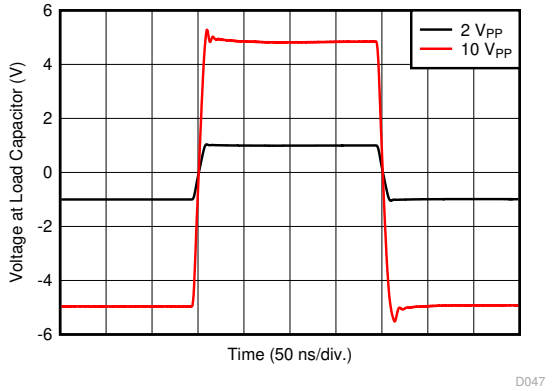
$\pm V_{CC}$ = ±7.5 V, R_F = 158 Ω, A_V = 5 V/V, V_{OUT} = 10 V_{PP}, see Series Output Resistance vs Load Capacitance for R_S value

図 6-45. HD2 vs Load Capacitance



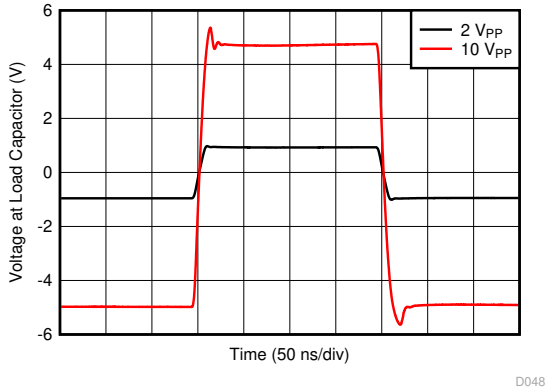
$\pm V_{CC}$ = ±7.5 V, R_F = 158 Ω, A_V = 5 V/V, V_{OUT} = 10 V_{PP}, see Series Output Resistance vs Load Capacitance for R_S value

図 6-46. HD3 vs Load Capacitance



$\pm V_{CC}$ = ±7.5 V, C_{LOAD} = 100 pF, R_F = 158 Ω, A_V = 5 V/V, see Series Output Resistance vs Load Capacitance for R_S value

図 6-47. Pulse Response



$\pm V_{CC}$ = ±7.5 V, C_{LOAD} = 150 pF, R_F = 158 Ω, A_V = 5 V/V, see Series Output Resistance vs Load Capacitance for R_S value.

図 6-48. Pulse Response

6.12 Typical Characteristics: Midscale (DC) Reference Buffer

at $+V_{CC}$ = 6.0 V, $-V_{CC}$ = –6.0 V, R_{LOAD} = 150 Ω, and $T_J \approx 25°C$ (unless otherwise noted)

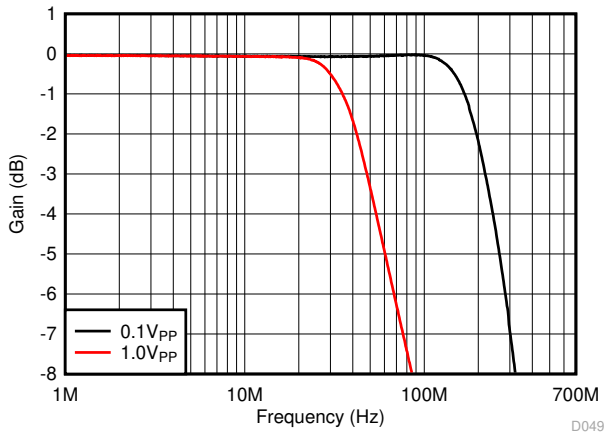


図 6-49. Frequency Response vs Output Voltage

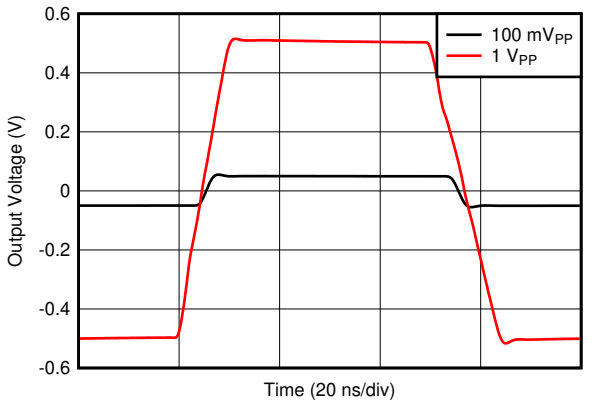


図 6-50. Step Response

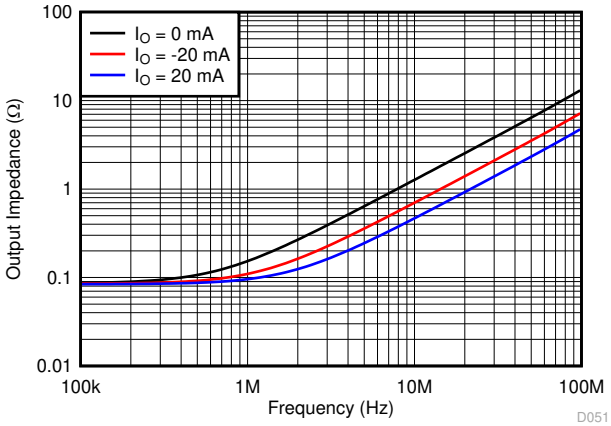


図 6-51. Buffer Output Impedance vs Load Current

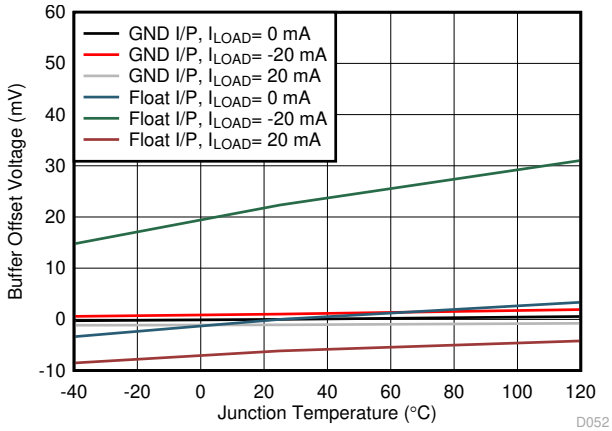
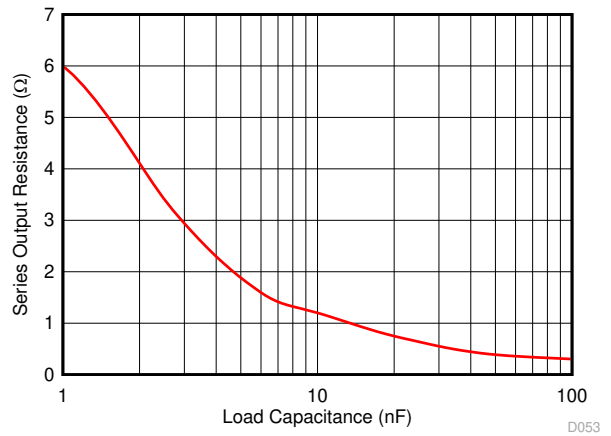
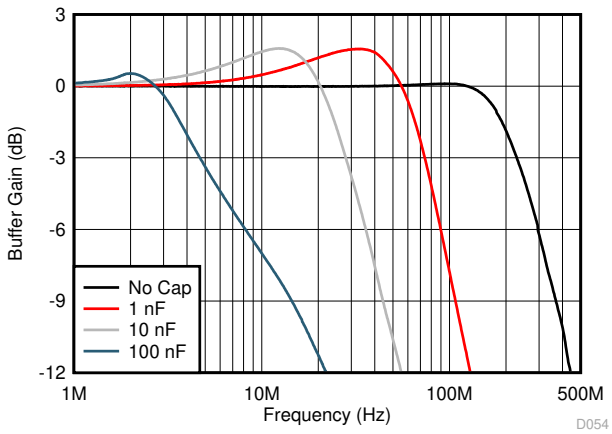


図 6-52. Buffer Output Offset vs Load Current (I_{LOAD})



R_{LOAD} = 150 Ω in parallel with C_{LOAD}, see the *セクション 7.8* section for circuit setup

図 6-53. Series Resistance vs Capacitive Load

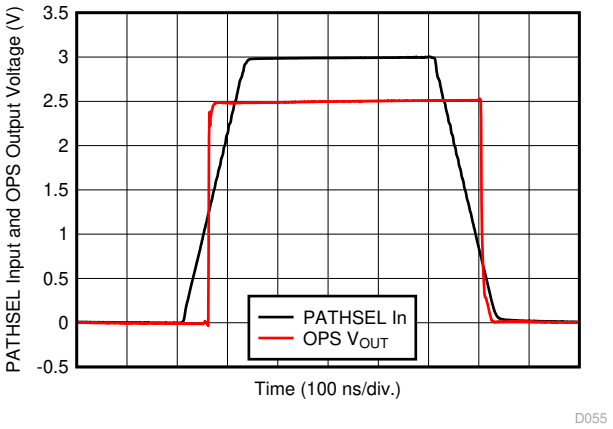


V_{OUT} = 100 mV_{PP}, R_{LOAD} = 150 Ω in parallel with C_{LOAD}, see *セクション 7.8* for circuit setup

図 6-54. Frequency Response vs Capacitive Load

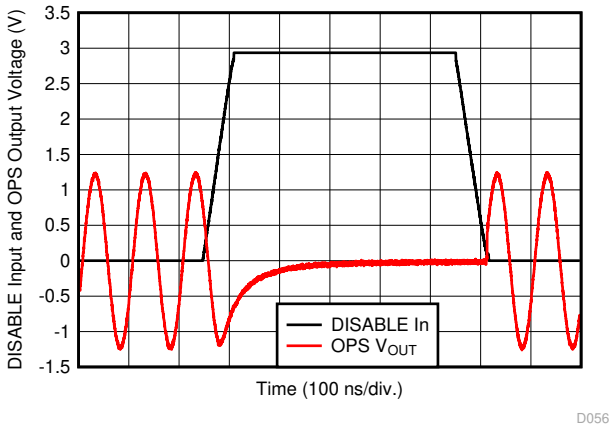
6.13 Typical Characteristics: Switching Performance

at $+V_{CC}$ = 6 V, $–V_{CC}$ = –6 V, 25-Ω D2S source impedance , V_{IC} = 0.25 V, internal path selected (PATHSEL = GND), V_{REF} = GND, D2S R_{LOAD} = 200 Ω at pin 6, R_F = 249 Ω, R_G = 162 Ω, OPS On (DISABLE = GND), OPS R_{LOAD} = 100 Ω at pin 11, and $T_J \approx 25°C$ (unless otherwise noted)



D2S Inputs: IN+ = IN– = GND, OPS input: VIN+ = 1 V

図 6-55. PATHSEL Switching Time



PATHSEL = high, OPS input: VIN+ = 1 V_{PP} , 10-MHz sine wave

図 6-56. OPS Enable and Disable Time

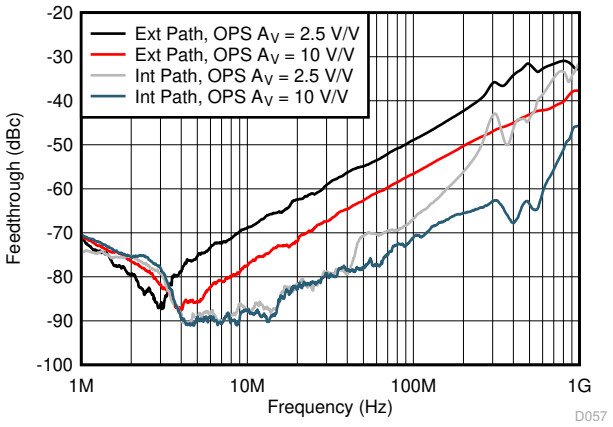


図 6-57. OPS Forward Feedthrough in Disable

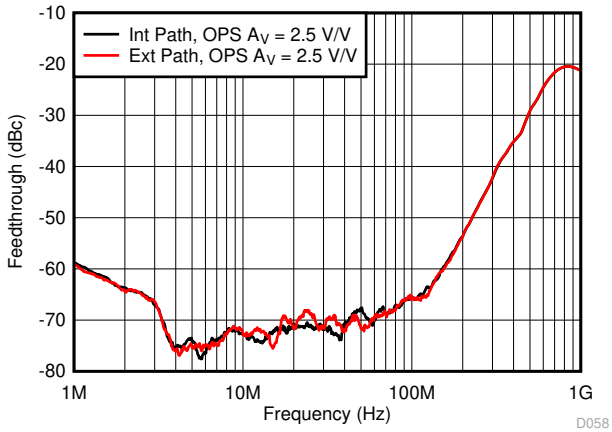
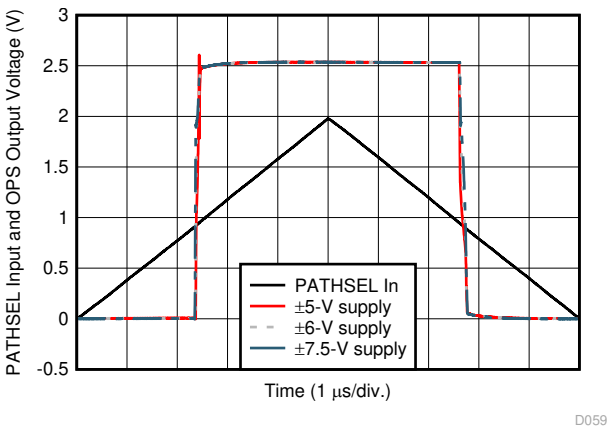
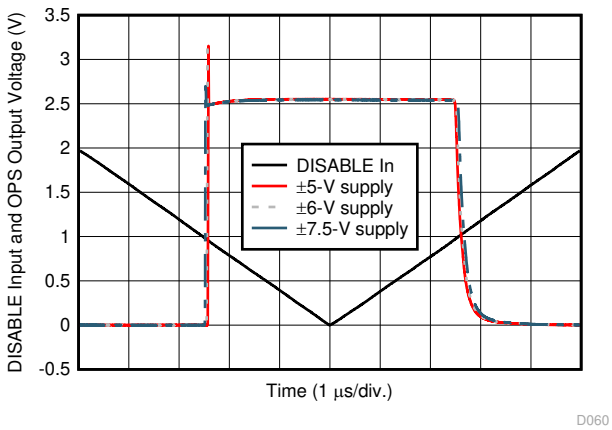


図 6-58. OPS Reverse Feedthrough in Disable



D2S inputs: IN+ = IN– = GND, OPS input: VIN+ = 1 V

図 6-59. PATHSEL Switching Threshold vs Power Supply

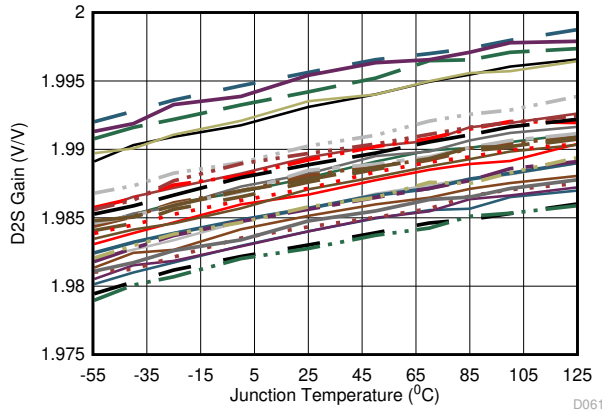


PATHSEL = high, OPS input: VIN+ = 1 V

図 6-60. OPS Shutdown Threshold vs Power Supply

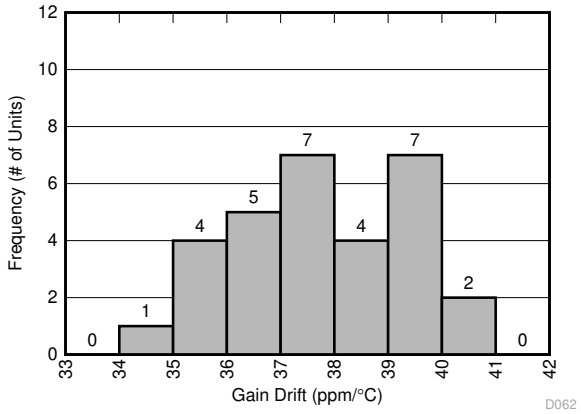
6.14 Typical Characteristics: Gain Drift

at $+V_{CC}$ = 6 V, $–V_{CC}$ = –6 V, 50-Ω D2S source impedance , V_{IC} = 0.25 V, internal path selected (PATHSEL = GND), V_{REF} = GND, D2S R_{LOAD} = 100 Ω at pin 6, R_F = 249 Ω, R_G = 162 Ω, OPS on (DISABLE = GND), OPS R_{LOAD} = 100 Ω at pin 11, and T_J ≈ 25°C (unless otherwise noted)



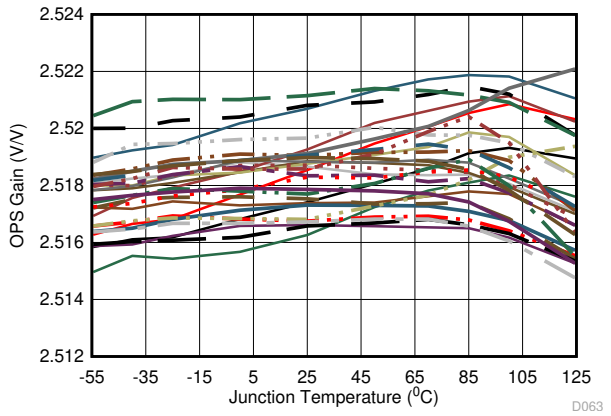
30 units shown

図 6-61. D2S Gain Over Temperature



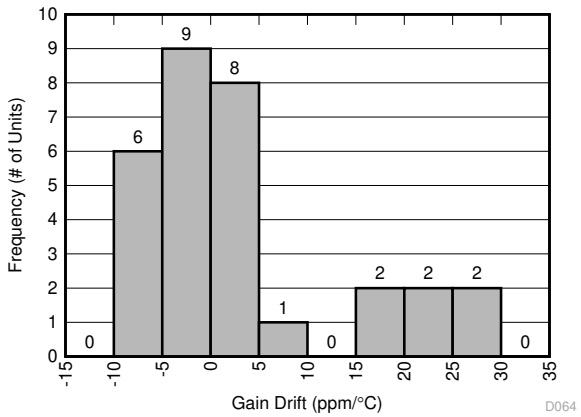
30 units from –40°C to +125°C

図 6-62. D2S Gain Drift Histogram



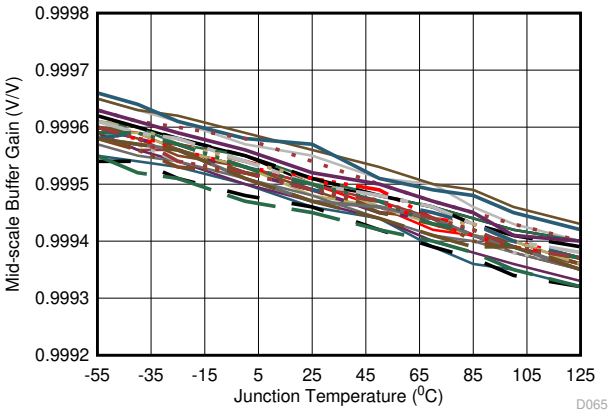
30 units shown

図 6-63. OPS Gain Over Temperature



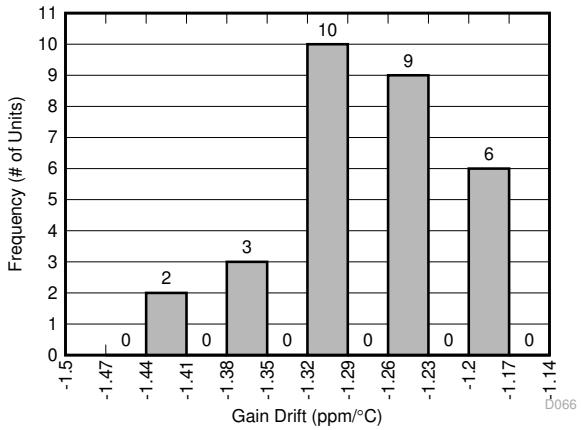
30 units from –40°C to +125°C

図 6-64. OPS Gain Drift Histogram



30 units shown

図 6-65. Midscale Buffer Gain Over Temperature



30 units from –40°C to +125°C

図 6-66. Midscale Buffer Gain Drift Histograms

7 Parameter Measurement Information

7.1 Overview

The THS3215 comprises three blocks of high-performance amplifiers. Each block requires both frequency-response and step-response characterization. The midscale buffer and OPS use standard, single-ended I/O test methods with network analyzers, pulse generators, and high-speed oscilloscopes. The differential to single-ended input stage (D2S) requires a wideband differential source for test purposes. All ac characterization tests were performed using the THS3215 evaluation module (EVM). The THS3215EVM offers many configuration options. For most of the D2S-only tests, the OPS was disabled. 図 7-1 shows a typical configuration for an ac frequency-response test of the D2S.

The THS3215EVM includes unpopulated, optional, passive elements at the D2S inputs to implement a differential filter. These elements were not used in the D2S characterization, and the two input pins were terminated to ground through 49.9 Ω resistors. DC test points are provided through 10 kΩ or 20 kΩ resistors on all THS3215 nodes. 図 7-1 also shows the output network used to emulate a 200 Ω load resistance (R_{LOAD}) while presenting a 50 Ω source back to the D2S output pin. The R3 (= 169 Ω) and R4 (= 73.2 Ω) resistors combine with the 50 Ω network analyzer input impedance to present a 200 Ω load at VO1 (pin 6), The impedance presented from the input of the network analyzer back to the D2S output (VO1, pin 6) is 50 Ω. The 16.5 dB insertion loss intrinsic to this dc-coupled impedance network is removed from the characterization curves. VREF (pin 14) was connected to GND for all the tests.

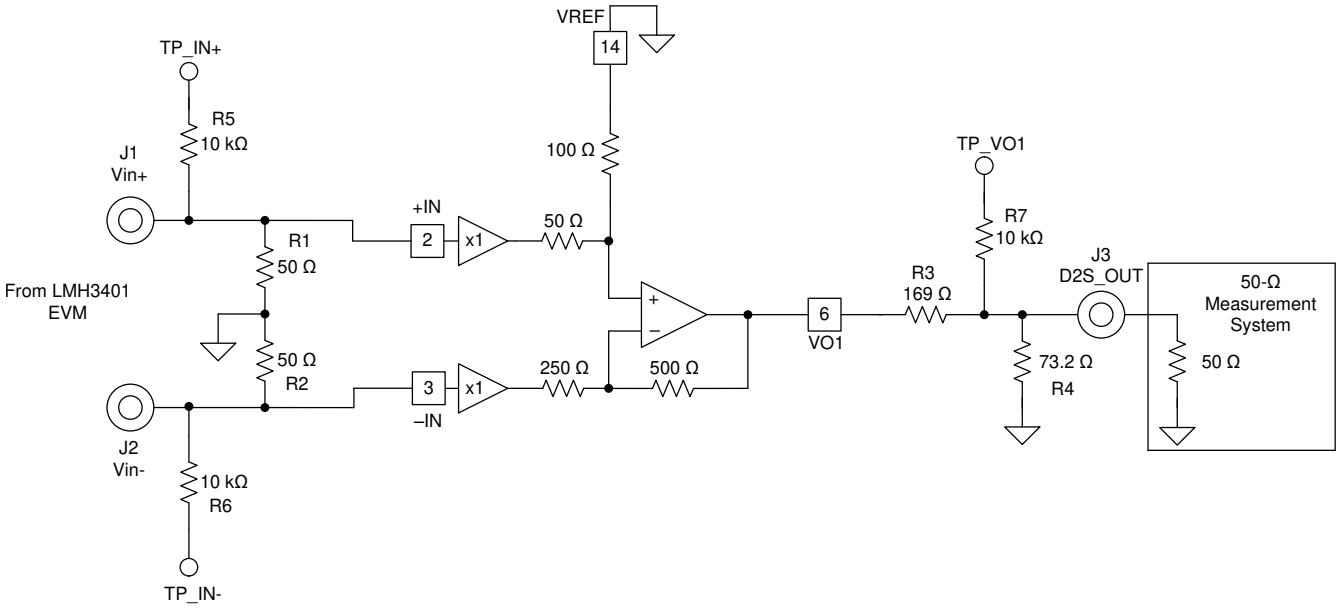


図 7-1. D2S Input and Output Interface Showing 50 Ω Differential Input, and 200 Ω R_{LOAD} at VO1

7.2 Frequency Response Measurement

For D2S and full-signal path (D2S + OPS) characterization, the LMH3401, a very wideband, dc-coupled, single-ended to differential amplifier, was used. The LMH3401EVM was used as an interface between a single-ended source and the differential input required by the D2S, shown in 図 7-2. The LMH3401 provides an input impedance of 50 Ω, and converts a single-ended input to a differential output driving through 50 Ω outputs on each side to what is a 50 Ω termination at each input of the THS3215 D2S.

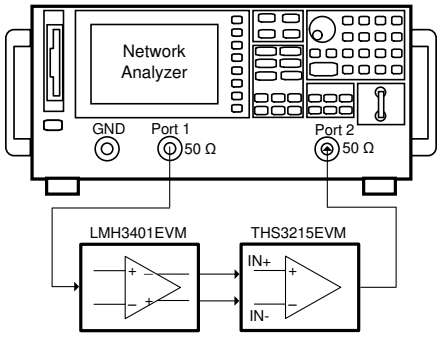


図 7-2. Frequency-Response Measurement: D2S and Full-Path (D2S + OPS) Circuit Configurations

The LMH3401 provides 7 GHz bandwidth with 0.1-dB flatness through 700 MHz. From the single-ended matched input (using active match through an internal 12.5 Ω resistor), the LMH3401 produces a differential output with 16-dB gain to the internal output pins. Building out to a 50 Ω source by adding external 40.2 Ω resistors on both differential outputs in series with the internal 10 Ω resistor, results in a net gain of 10 dB to the matched 50 Ω load on the THS3215EVM.

The maximum output swing test for the D2S is 4 V_{PP} (see HD2 vs Output Voltage and HD3 vs Output Voltage). With a fixed gain of 2 V/V, the tests in HD2 vs Output Voltage and HD3 vs Output Voltage require a 2 V_{PP} differential input. In order to achieve the 2 V_{PP} differential swing at the D2S inputs, the LMH3401 internal outputs must drive a 4 V_{PP} differential signal around the V_{OCM} of the LMH3401. This LMH3401 single-to-differential preamplifier is normally operated with ±2.5 V supplies, and V_{OCM} set to ground. Under these conditions, the LMH3401 supports ±1.4 V on each internal output pin; well beyond the maximum required for THS3215 D2S characterization of ±1 V.

The output of the LMH3401EVM connects directly to the Vin+ (J1) and Vin– (J2) SMA connectors on the THS3215EVM, as shown in 図 7-1. The physical spacing of the SMA connectors lines up for a direct (no cabling) connection between the two different EVMs using SMA barrels. For THS3215 designs that must be evaluated before any DAC connection, consider using the LMH3401EVM as a gain of 10 dB, single-to-differential interface to the inputs of the D2S. This setup allows single-ended sources to generate differential output signals through the combined LMH3401EVM to THS3215EVM configuration. The D2S, small-signal, frequency-response curves over input common-mode voltage (see Frequency Response vs Input Common-Mode Voltage) were generated by adjusting the LMH3401 voltage supplies and maintaining V_{OCM} at midsupply to preserve input headroom on the LMH3401. In order to make single-ended, frequency-response measurements, the configuration shown in 図 7-3 was used.

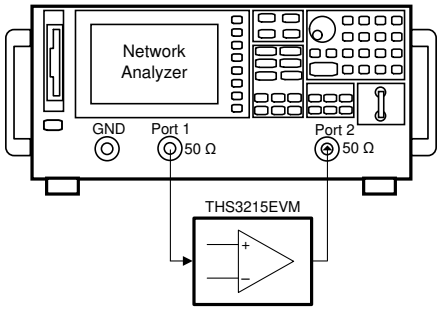


図 7-3. Frequency-Response Measurement: OPS Inverting and Noninverting, Midscale Buffer, and VREF-Input Circuit Configurations

7.3 Harmonic Distortion Measurement

The distortion plots for all stages used a filtered high-frequency function generator to generate a very low-distortion input signal. The LMH3401 interface was used when testing the D2S and the full-signal path (D2S + OPS) harmonic distortion performance. Running the filtered signal through the LMH3401, as shown in 図 7-4, provided adequate input signal purity because of the approximately –100-dBc harmonic distortion performance through 100 MHz provided by the LMH3401. In order to test the harmonic-distortion performance of the OPS and midscale buffer, the configuration shown in 図 7-5 was used.

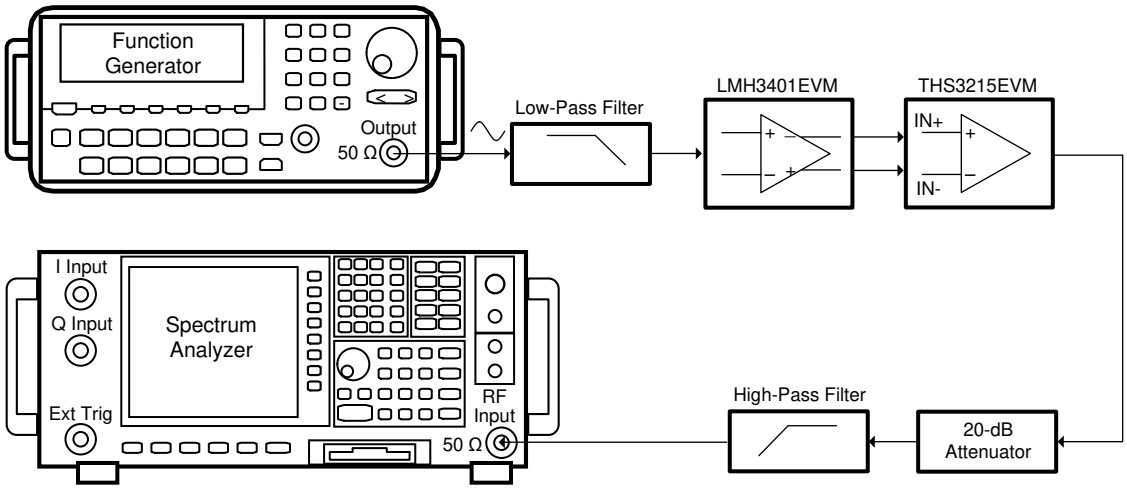


図 7-4. Harmonic-Distortion Measurement: D2S and Full-Path (D2S + OPS) Circuit Configurations

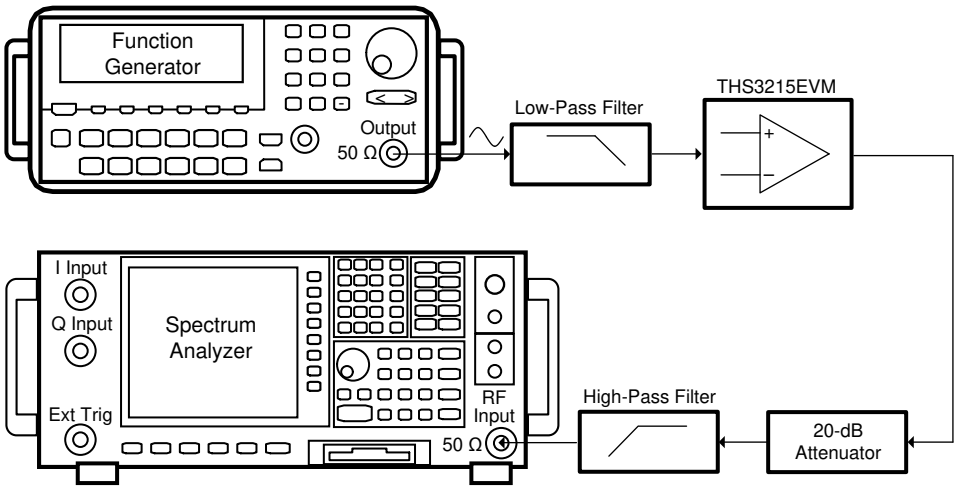


図 7-5. Harmonic-Distortion Measurement: OPS Inverting and Noninverting and Midscale Buffer Circuit Configurations

7.4 Noise Measurement

All the noise measurements were made using the very low-noise, high-gain bandwidth LMH6629 as a low-noise preamplifier to boost the output noise from the THS3215 before measurement on a spectrum analyzer, as shown in 図 7-6. The 0.69-nV/√ Hz input-voltage noise specification of the LMH6629 provides flat gain of 20 V/V through 100 MHz with its ultrahigh, 6.3-GHz gain bandwidth product. The D2S and OPS noise was measured with the common-mode voltage at GND.

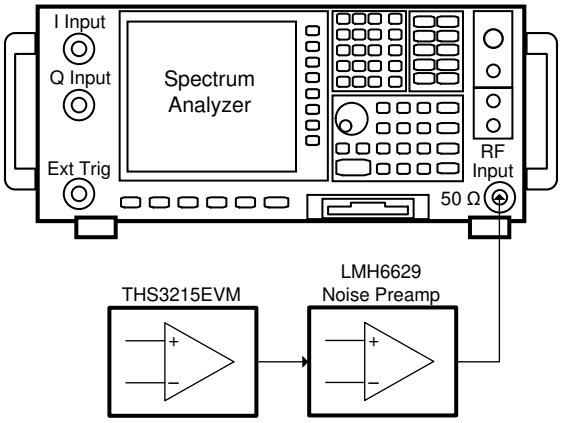


図 7-6. Noise Measurement Using LMH6629 Preamplifier

7.5 Output Impedance Measurement

Output impedance measurement for the three stages under different conditions were performed as a small-signal measurement calibrated to the device pins using an impedance analyzer. Calibrating the measurement to the device pins removes the THS3215EVM parasitic resistance, inductance, and capacitance from the measured data.

7.6 Step-Response Measurement

Generating a clean, fast, differential-input step for time-domain testing presents a considerable challenge. A multichannel pulse generator with adjustable rise and fall times was used to generate the differential pulse to drive D2S inputs in Large-Signal Step Response vs Load Resistance. A high-speed scope was used to digitize the pulse response.

7.7 Feedthrough Measurement

In order to test the forward-feedthrough performance of the OPS in the disabled state, the circuit shown in 図 7-7 was used. The PATHSEL pin was driven low to select the internal path between the D2S and OPS. A 100 mV_{PP}, swept-frequency, sinusoidal signal was applied at the VREF pin, and the output signal was measured at the OPS output pin (VOUT, pin 11). The transfer function from VREF to the output of the D2S at VO1 has a gain of 0 dB, as shown in VREF Input Pin Frequency Response. The results shown in OPS Forward Feedthrough in Disable account for the 6 dB loss due to the doubly-terminated OPS output, and report the forward feedthrough between VOUT and VO1 at different OPS gains. The D2S inputs were grounded through 50 Ω resistors for this test.

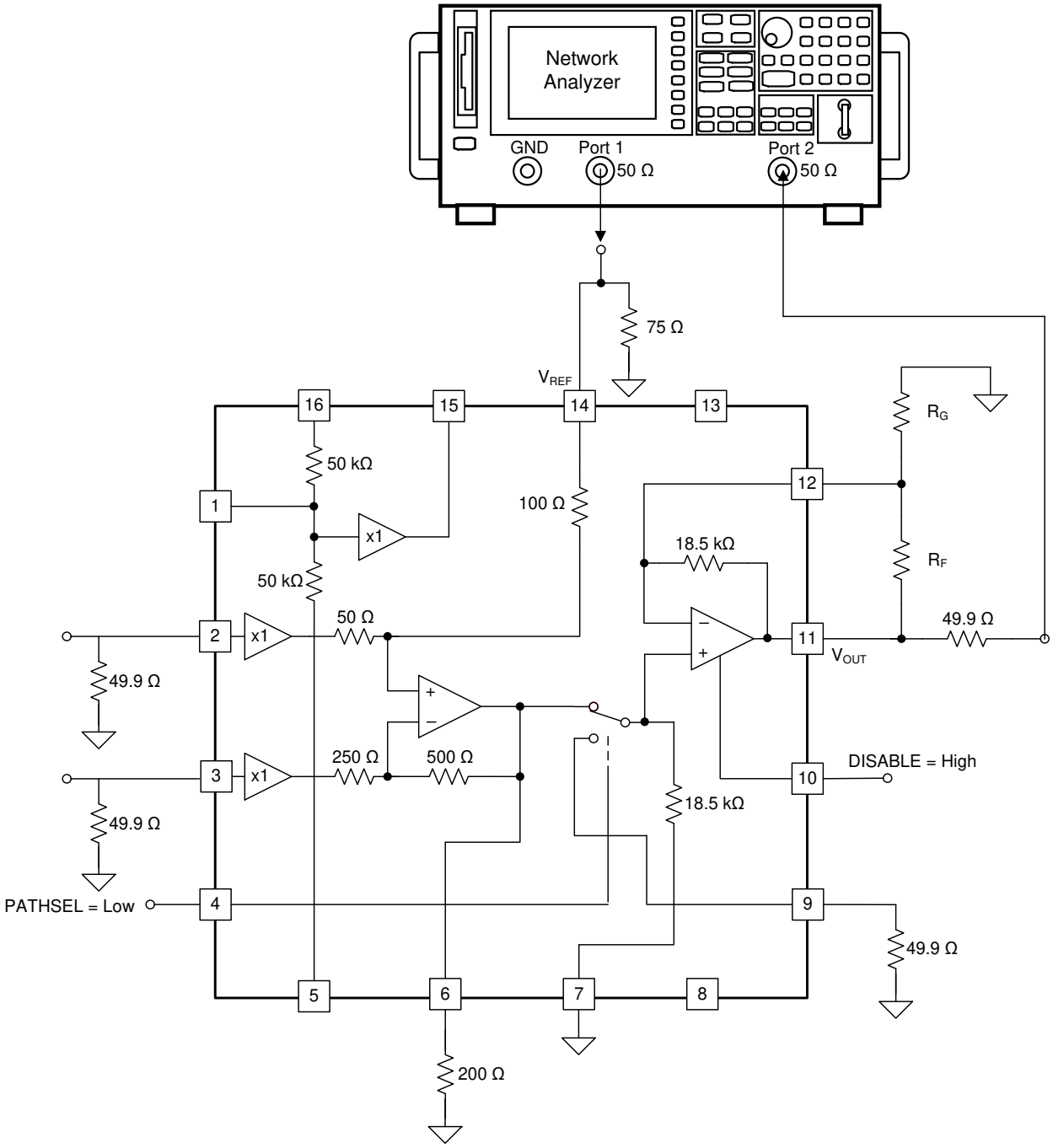


図 7-7. Forward-Feedthrough Test Circuit

In order to test the reverse feedthrough performance of the OPS in its disabled state, the circuit shown in 図 7-8 was used. The PATHSEL pin was driven high to select the external path to the OPS noninverting pin, VIN+, pin 9. A 100 mV_{PP}, swept-frequency, sinusoidal signal was applied at the VIN+ pin and the output signal was measured at the D2S output pin (VO1, pin 6). The results shown in OPS Reverse Feedthrough in Disable account for the 16.5 dB loss due to the D2S termination, and the test reports the reverse feedthrough between the VO1 and VIN+ pins. The D2S inputs were grounded through 50 Ω resistors for this test.

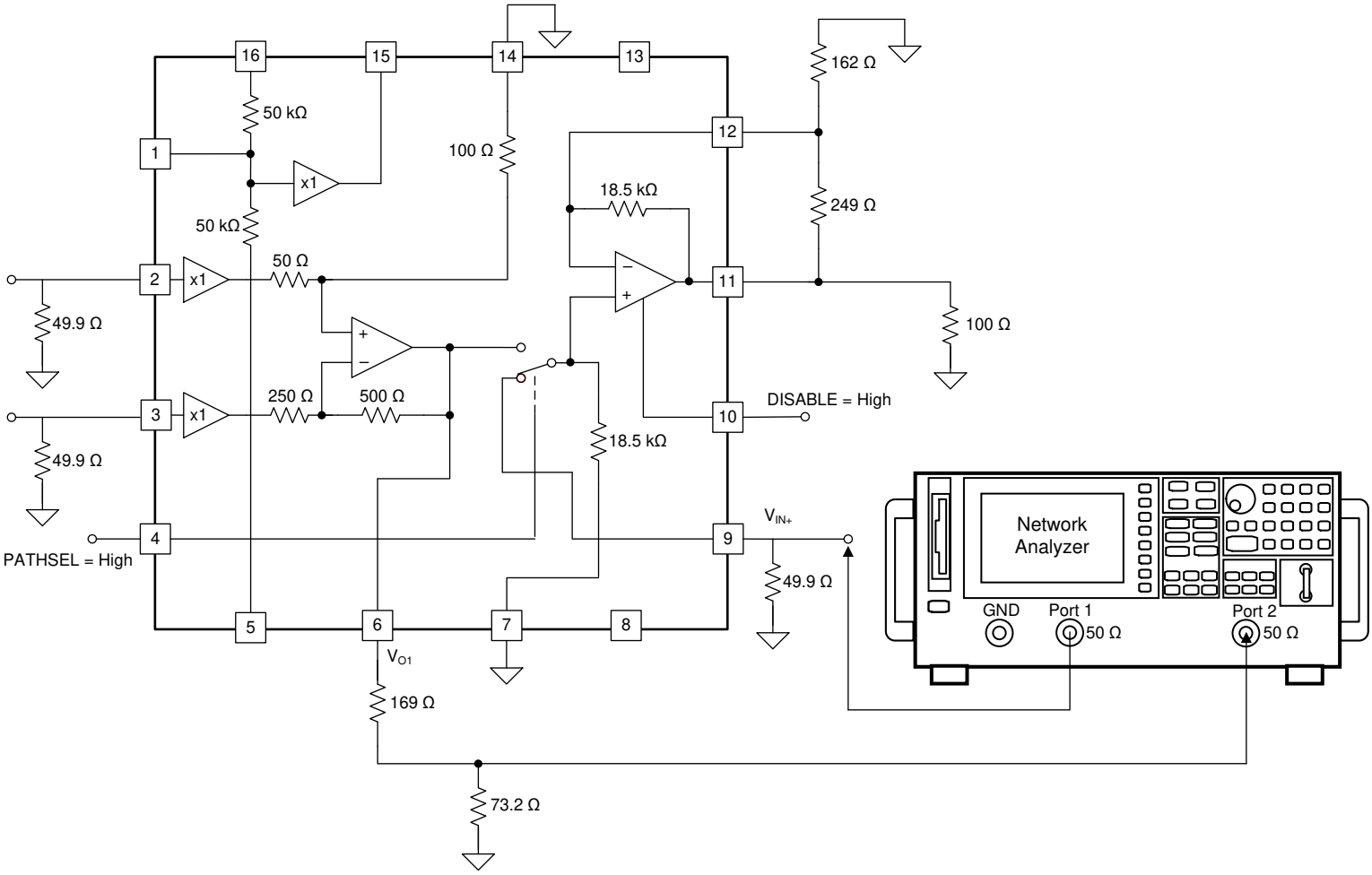


図 7-8. Reverse-Feedthrough Test Circuit

7.8 Midscale Buffer R_{OUT} Versus C_{LOAD} Measurement

For the tests in Series Resistance vs Capacitive Load and Frequency Response vs Capacitive Load, the circuit shown in 図 7-9 was used. The 150 Ω load circuit configured as shown, provides a 50 Ω path from the network analyzer back to the output of the buffer. As shown in 図 7-9, place R_{OUT} below the load capacitor to improve the phase margin of the closed-loop buffer output, while adding 0 Ω dc impedance into the line connecting VMID_OUT (pin 15) to the VREF pin. When using the midscale buffer to drive the VREF input, use a decoupling capacitor at VMID_OUT to reduce broadband noise and source impedance.

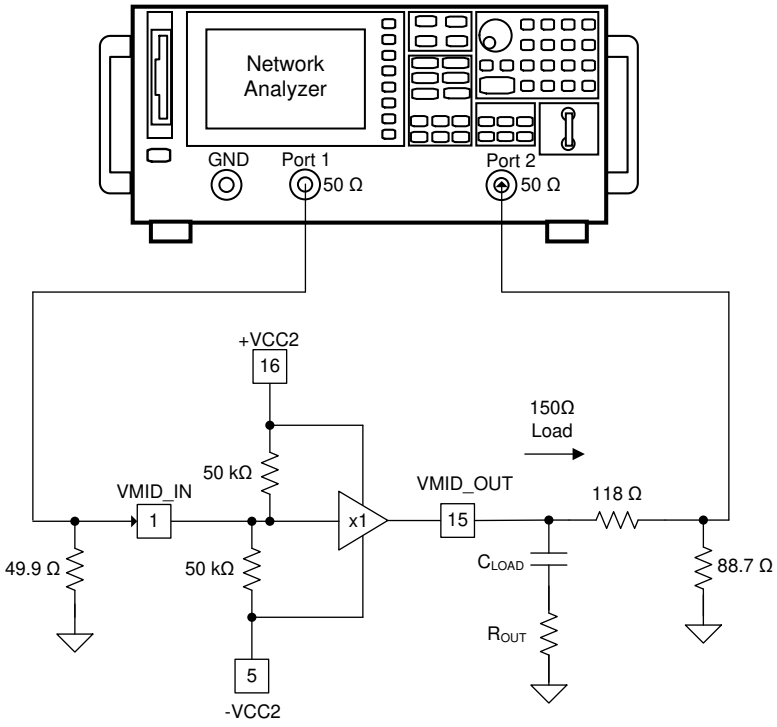


図 7-9. R_{OUT} Versus C_{LOAD} Measurement Circuit

8 Detailed Description

8.1 Overview

The THS3215 is a differential-input to single-ended output amplifier system that provides the necessary functional blocks to convert a differential output signal from a wideband DAC to a dc-coupled, single-ended, high-power output signal. The THS3215 typically operates using balanced, split supplies. Signal swings through the device can be adjusted around ground at several points within the device. Single-supply operation is also supported for an ac-coupled signal path. The THS3215 supply voltage ranges from ±4.0 V to ±7.9 V. The two internal logic gates rely on a logic reference voltage at pin 7 that is usually tied to ground for any combination of power-supply voltages. The DISABLE control (pin 10) turns the output power stage (OPS) off to reduce power consumption when not in use.

A differential-to-single-ended stage (D2S) provides a high input impedance for a high-speed DAC (plus any reconstruction filter between the DAC and THS3215) operating over a common-mode input voltage range from –1 V to +3.0 V. This range is intended to support either current sourcing or current sinking DACs. The D2S is internally configured to reject the input common-mode voltage and convert the differential inputs to a single-ended output at a fixed gain of 2 V/V (6 dB).

An uncommitted, on-chip, wideband, unity-gain buffer is provided (between pins 1 and 15) to drive the VREF pin. The buffer offers extremely broad bandwidth to achieve very-low output impedance to high frequencies (Buffer Output Impedance vs Load Current). The buffer does not provide a high full-power bandwidth because of a relatively low slew rate. The buffer stage includes a default midsupply bias resistor string of 50 kΩ each to set the default input to midsupply. This 25 kΩ Thevinin impedance is easily overridden with an external input source, but is intended to provide a midsupply bias for single-supply operation. The buffer amplifier that drives the VREF pin has two functions:

- Provides an easy-to-interface, dc-correction, servo-loop input
- Provides an optional offset injection point for the D2S output

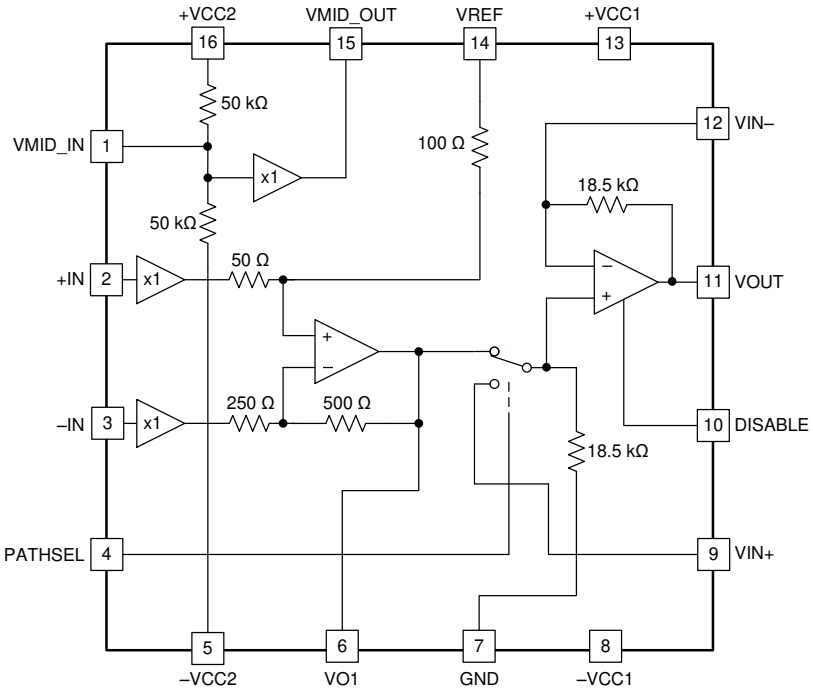
The final OPS provides a very high-performance, current-feedback amplifier for line-driving applications. The 700 MHz small-signal bandwidth (SSBW) stage provides 3000 V/µs of slew-rate, sufficient to drive a 5 V_{PP} output with 270 MHz bandwidth. In addition, the OPS is able to drive a very-high continuous and peak output current sufficient to drive the most demanding loads at very high speeds. A unique feature added to the OPS is a 2 × 1 input multiplexer at the noninverting input. The PATHSEL control (pin 4) is used to select the appropriate signal path to the OPS noninverting input. One of the multiplexer select paths passes the internal D2S output directly to the OPS. The other select path accepts an external input to the OPS at VIN+ (pin 9). This configuration allows the D2S output, available at VO1 (pin 6), to pass through an external RLC filter and back into the OPS at VIN+ (pin 9).

If the OPS does not require power for certain application configurations, a shutdown feature has been included to reduce power consumption. For designs that do not use the OPS at all, two internal fixed resistors are included to define the operating points for the disabled OPS. An approximate 18.5 kΩ resistor to the logic reference (GND, pin 7) from VIN+ (pin 9), and an approximate 18.5 kΩ, fixed, internal feedback resistor are included to hold the OPS pin voltages in range if no external resistors are used around the OPS. These resistors must be included in the design calculations for any external network.

Two sets of power supply-pins have been provided for both the positive and negative supplies. –VCC2 (pin 5) and +VCC2 (pin 16) power the D2S and midscale buffer stages, while –VCC1 (pin 8) and +VCC1 (pin 13) supply power to the OPS. The supply rails are connected internally by antiparallel diodes. Externally, connect power first to the OPS, then connect back on each side with a π-filter (ferrite bead + capacitor) to the input-stage supply pins (see 図 8-15). Do not use mismatched supply voltages on either the positive or negative sides because the supplies are internally connected through the antiparallel diodes. Imbalanced positive and negative supplies are acceptable, however.

When the OPS is disabled, the output pin goes to high impedance. Do not connect two OPS outputs from different devices together and select them as a *wired-or* multiplexer. Although the high-impedance output is disabled, the inverting node is still available through the feedback resistor, and can load the active signal. The signal path through the inverting node typically degrades the distortion on the desired active signal in a wired-or multiplexer configuration using current-feedback amplifiers (CFAs).

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Differential to Single-Ended Stage (D2S) With Fixed Gain of 2 V/V (Pins 2, 3, 6, and 14)

This buffered-amplifier stage isolates the DAC output pins from the differential to single-ended conversion. Present two high-impedance inputs to allow the DAC to operate in its best configuration independent of subsequent operations. The two very wideband input buffers hold an approximately constant response shape over a wide input common-mode operating voltage. Frequency Response vs Input Common-Mode Voltage shows 6 dB of gain with 0.5 dB flatness through 100 MHz over the intended –1 V to +3 V input common-mode range. In this case, the VREF pin is grounded, forcing the D2S output to be centered on ground for any input common-mode voltage. For the D2S-only tests, a 100 Ω load is used to showcase the performance of this stage directly driving a doubly-terminated cable. The wide, input common-mode range of the D2S satisfies the required compliance voltage over a wide range of DAC types. Most current sourcing DACs require an average dc compliance voltage on their outputs near ground. Current sinking DACs require an average dc compliance voltage near their positive supply voltage for the analog section. The 3 V maximum common-mode range is intended to support DAC supplies up to 3.3 V, where the average output operating current pulls down from 3.3 V by the termination impedance from the supply. For instance, a 20 mA tail current DAC must level shift from a 3.3 V bias on the output resistors down to 3 V or lower. This DAC-to-THS3215 configuration requires at least a 300 mV dc level shift with half the tail current in each side, implying a 30 Ω load impedance to the supply on each output side using a 20 mA reference current.

The overriding limits to the input common-mode operating range are due to the input buffer headroom. Over temperature, the D2S input headroom specification is 2 V to the negative supply and 1.5 V to the positive supply. Therefore, operation at a 3 V input common-mode voltage requires at least a 4.5 V positive supply, where 5 V is a more conservative minimum.

While DAC outputs rarely have any common-mode signal present (unless the reference current is being modulated), the D2S does a reasonable job of rejecting input common-mode signals over frequency. Common-Mode Rejection Ratio vs Input Common-Mode Voltage shows the CMRR to decrease above 10 MHz. For current-sinking DACs coming from a positive supply voltage, any noise on the positive supply looks like an input common-mode signal. Keeping the noise low at higher frequencies reduces the possibility of feedthrough to the D2S output due to the decreasing CMRR at higher frequencies. A current-sinking DAC uses pull-up resistors to the voltage supply to convert the DAC output current to a voltage. Make sure that the DAC voltage supply is properly decoupled through a ferrite-bead-and-capacitor, π-filter network, similar to the supply decoupling for the THS3215 shown in 図 8-15.

The D2S provides a differential gain of 6 dB. The gain is reasonably precise using internal resistor matching with extremely low gain drift over temperature (see D2S Gain Over Temperature and D2S Gain Drift Histogram). The single-ended D2S output signal can be placed over a wide range of dc offset levels using the VREF pin. The VREF pin shows a precise gain of 1 V/V to the D2S output. Grounding VREF places the first stage output centered on ground (with some offset voltage). For best ac performance through the D2S, anything driving the VREF pin must have a very wide bandwidth with very low output impedance over frequency while driving a 150 Ω load. The on-chip midscale buffer provides these features (see Buffer Output Impedance vs Load Current). When a dc offset (or other small-level ac signal) must be applied to the VREF pin, buffer the signal through the midscale buffer stage. Maintain the total range of the dc offset plus signal swing within the available output swing range of the D2S. The headroom to the supplies is a symmetric ±2.1 V (maximum) over temperature. Therefore, on the minimum ±4 V supply, the D2S operates over a ±1.9 V output range. At the maximum ±7.9 V supply, a ±5.8 V output range is supported. At the higher swings, account for available linear output current, including the current into the internal feedback resistor load of approximately 500-Ω.

図 8-1 shows the internal structure of the D2S functional block. It consists of two internal stages:

1. The first stage consists of two wideband, closed-loop, fixed gain of 1 V/V buffers to isolate the requirements of the complementary DAC output from the difference operation of the D2S.
2. The second stage is a wideband CFA configured as a difference amplifier, operating in a fixed gain of 2 V/V, performing the differential to single-ended conversion.

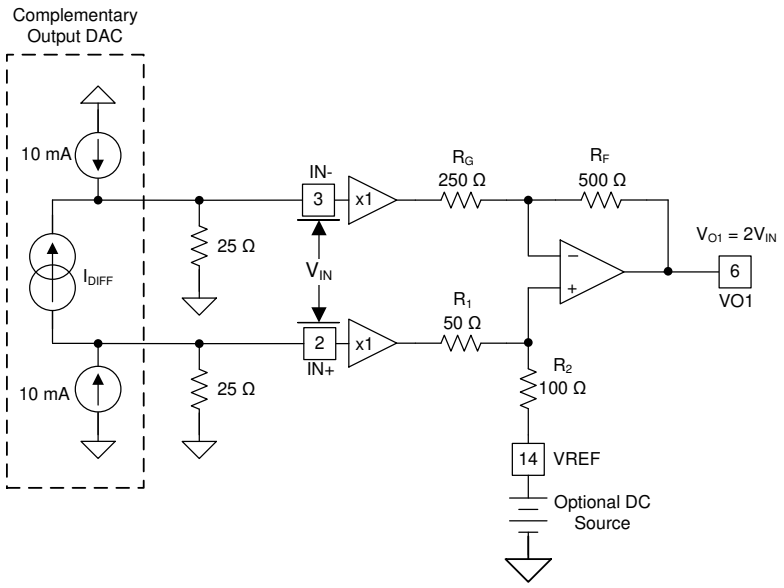


図 8-1. D2S Operating Example

The CFA design offers the best, full-power bandwidth versus supply current, with moderate noise and dc precision. 図 8-1 shows a typical current-sourcing DAC with a 20 mA total tail current. The tail current is split equally between the 25 Ω termination resistors to produce a dc common-mode voltage and a differential ac current signal. This example sets the input common-mode voltage at 0.25 V, and is also the *compliance* voltage of the DAC. The 25 Ω termination resistors shown here are typically realized as a 50 Ω matched reconstruction (or Nyquist) filter between the DAC and the THS3215 buffer inputs for most AWG applications. The DAC signal is further amplified by 6 dB in the second stage for a net transimpedance gain of 100 Ω to the D2S output at VO1. This configuration produces a 2 V_{PP} output for the 20 mA reference current assumed in the example of 図 8-1. The input common-mode voltage is cancelled on the two sides of the op amp circuit to give a ground referenced output. Any voltage applied to VREF (pin 14) has a gain transfer function of 1 V/V to VO1, independent of the signal path, as long as the source impedance of VREF is very low at dc and over frequency.

The IN+ buffer output drives a 150 Ω load with VREF grounded. Any source driving VREF must have the ability to drive a 150 Ω load with low output impedance across frequency. For differential input signals, the IN– buffer drives a 150 Ω active load. The active load is realized by a combination of the 250 Ω R_G resistor and the inverted and attenuated signal present at the inverting terminal of the difference amplifier stage. If only IN– is driven (with IN+ at a dc fixed level), the load is 250 Ω.

The resistor values around the D2S difference amplifier are derived in the following sequence, as shown in 図 8-2:

1. Select the feedback resistor value to set the response shape for the wideband CFA stage. The 500 Ω design used here was chosen as a compromise between loading and noise.
2. Set the input resistor on the inverting input side to give the desired single-sided gain for that path. Setting R_G= 250 Ω results in a gain of –2 V/V from the buffered signal (–V) to the output of the difference amplifier.
3. Solve the required attenuation to the noninverting input to get a matched gain magnitude for the signal provided at the buffer output (+V) on the noninverting path. If α = R2 / (R1 + R2), as shown in 図 8-2, then the solution for α is shown in 式 2:

$$\alpha\left(1+\frac{R_F}{R_G}\right)=2 \tag{1}$$

$$\alpha=\frac{2}{3}=\frac{R1}{(R1+R2)} \tag{2}$$

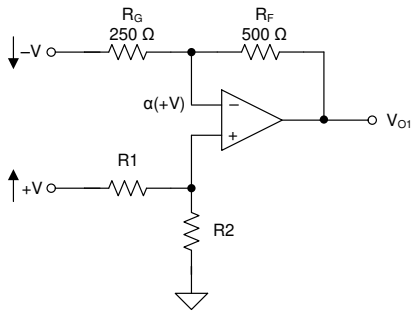


図 8-2. D2S Impedance Analysis

4. After solving the attenuation from the buffer output to the amplifier noninverting input, set the impedance (R1 + R2). It is preferable to have the two first-stage buffer outputs drive the same load impedance to match nonlinearity in their outputs in order to improve even-order harmonic distortion. The load impedance from –V to R_G has an active impedance because of the inverted and attenuated version of the input signal appearing at the inverting amplifier node from the +V input signal. Assuming a positive input signal into the +V path, an attenuated version of the signal appears at the amplifier summing junction side of R_G, while the inverted version of the signal appears on the input side of R_G.

The impedance seen at node –V in 図 8-2 is derived in 式 3 by solving for the V/I expression across R_G.

$$Z_i = \frac{R_G}{(1+\alpha)} = \frac{250\ \Omega}{1+\frac{2}{3}} = 150\ \Omega \tag{3}$$

For load balancing, (R1 + R2) = 150 Ω while the attenuation is α. More generally, all the terms are now available to solve for R2, as shown in 式 4:

$$R2 = R_G \frac{\alpha}{(\alpha+1)} = 250\ \Omega \frac{\frac{2}{3}}{1+\frac{2}{3}} = 100\ \Omega \tag{4}$$

R1 is then simply (Z_i – R2) = 50 Ω.

This analysis for matched gains and buffer loads can be applied to a more general, discrete design using different target gains and starting R_F values. It is clearly useful to have the attenuation and buffer loading accurately controlled. Therefore, it is very important to control the impedance at VREF (pin 14) to be as low as possible. For instance, using the midscale buffer to drive VREF only adds 0.21 Ω dc impedance in series with R2. This low, dc output impedance can only be delivered with a closed-loop buffer design. For discrete implementations of this D2S, consider the BUF602 buffer and LMH6702 wideband CFA. For even better dc and ac output impedance in the buffers (and possibly better gain), use a closed-loop, dual, wideband op amp like the OPA2889 for lower frequency applications, or the OPA2822 for higher frequency. These unity gain stable op amps can be used as buffers, offering different performance options along with the LMH6702 wideband CFA over the design point chosen for the THS3215.

After gain matching is achieved in the single op amp differential stage, the common-mode input voltage is cancelled to the output, and the VREF input voltage is amplified by 1 V/V to the output. The analysis circuit is shown in 図 8-3, where VREF is shown grounded at the R2 element.

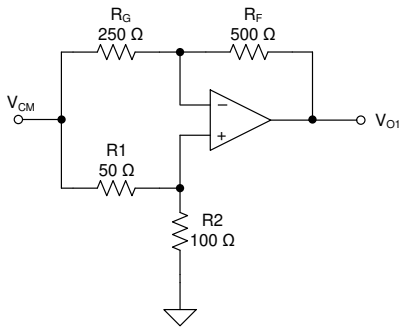


図 8-3. D2S Common-Mode Cancellation

The gain magnitudes are equal on each side of the differential inputs; therefore, the common-mode inputs achieve the same gain magnitude, but opposite phase, resulting in common-mode signal cancellation. The inverting path gain is $V_{CM} \times (R_F / R_G)$. The noninverting path gain is $V_{CM} \times \alpha \times (1 + R_F / R_G)$. Using 式 5:

$$\alpha = \frac{\frac{R_F}{R_G}}{\left(1 + \frac{R_F}{R_G}\right)} \tag{5}$$

the noninverting path gain becomes $+V_{CM} \times R_F / R_G$, and adding that result to the inverting path signal cancels the input common-mode voltage to zero. Slight gain mismatches reduce this rejection to the 48 dB typical CMRR, with a 42 dB tested minimum. The 42 dB minimum over the 3 V maximum common-mode input range adds another ±23.8 mV worst-case D2S output offset term to the specified maximum ±35 mV output offset with 0 V input common-mode voltage. The polarity of the gain mismatch is random.

The VREF pin input voltage (V_{REF}) generates a gain of 1 V/V using the analysis shown in 図 8-4.

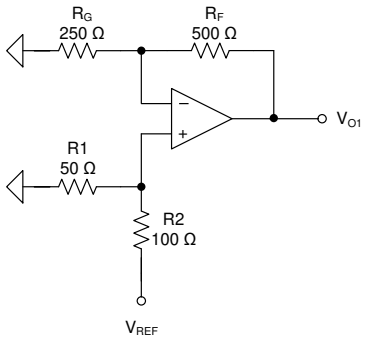


図 8-4. Gain Transfer Function from VREF to VO1

The gain from VREF to VO1 is shown in 式 6:

$$V_{REF} \frac{R1}{(R1 + R2)}\left(1 + \frac{R_F}{R_G}\right) = V_{O1} \tag{6}$$

Getting both R1 and (R1 + R2) in terms of R_G and the target attenuation, α simplifies, as shown in 式 7:

$$\frac{R1}{(R1 + R2)} = \frac{R_G \frac{1 - \alpha}{1 + \alpha}}{R_G \frac{1}{1 + \alpha}} = (1 - \alpha) \tag{7}$$

Putting 式 7 back into the gain expression (式 6), and expanding out gives:

$$V_{REF}(1-\alpha)\left(1+\frac{R_F}{R_G}\right)=V_{O1} \tag{8}$$

Substituting the value of α from 式 5 into 式 8 reduces the expression to $V_{O1} = V_{REF}$, a gain of 1 V/V. This gain is very precise, as shown in the *D2S Electrical Characteristics* table, where the tested dc limits are 0.975 V/V to 1.015 V/V.

The D2S output offset and drift are largely determined by the internal elements. The only external consideration is the dc source impedance at the two buffer inputs. With low source impedance, the D2S output offset is tested to be within ±35 mV, that becomes a maximum ±17 mV input differential offset specification. Assuming the dc source impedances are closely matched, the mismatch in the two input bias currents adds another input offset term for higher source impedances. The input bias offset current is limited in test to be < ±0.40 µA. This error term does not rise to add more than ±1 mV input differential offset until the dc source impedance exceeds 2.5 kΩ. A high dc source impedance most commonly occurs in an input ac-coupled, single-supply application, where dc offsets are less critical.

The absolute input bias currents modify the common-mode input voltage if the dc source resistance is too large. The input bias current is tested to a limit of ±4 µA on each input. In order to move the input common-mode voltage by ±100 mV, the dc source impedance must exceed 25 kΩ. This added input common-mode voltage is cancelled by the D2S at the output (pin 6) and is set to the reference voltage applied at VREF (pin 14).

The D2S output noise is largely fixed by the internal elements. The D2S shows a differential input voltage noise of 6 nV/√Hz, and a current noise of 2 pA/√Hz on each input. Higher termination resistors increase this source noise, as given by 式 9, where R_t is the dc termination impedance at each buffer input. The D2S has a 1/f corner at approximately 10 kHz (see Differential Input Noise vs Source Impedance).

$$e_{i\_diff}=\sqrt{(6\text{ nV})^2+2(4kTR_t)+2(2\text{ pA}\times R_t)^2} \tag{9}$$

The total differential input noise is dominated by the differential voltage noise. For instance, evaluating this expression for R_t = 200 Ω on each input, increases the total differential input noise to 6.5 nV/√Hz, only slightly greater than the 6 nV/√Hz for the D2S with 0 Ω source R_t on each input. If higher final output SNR is desired, consider generating as much input swing as the DAC can support by increasing the termination impedance. It is possible that a lower tail current with higher R_t can yield improved SNR at the D2S input. This differential input noise appears at the D2S output times a gain of 2 V/V.

$$e_{out\_diff}=2\times e_{i\_diff} \tag{10}$$

8.3.2 Midscale (DC) Reference Buffer (Pin 1 and Pin 15)

This optional block can be completely unconnected and not used if the design does not require this feature. Internal 50 kΩ resistors to the power supplies bias the input of the buffer to the midpoint of the supplies used. The internal resistors set a midsupply operating point when the buffer is not used, as well as a default midsupply point at the buffer output to be used in other stages for single-supply, ac-coupled applications.

The buffer provides a very wideband, low output-impedance when used to drive VREF, pin 14 (see Buffer Output Impedance vs Load Current). To provide this low broadband impedance, the closed-loop midscale (dc) reference buffer offers a very broadband SSBW, but only a modest large-signal bandwidth (LSBW); see Frequency Response vs Output Voltage. This path is not normally intended to inject a wideband signal, but can be used for lower-amplitude signals. Driving the buffer output into the VREF pin allows a wideband small-signal term to be added into the D2S along with the signal from the differential inputs.

The midscale (or dc) reference buffer injects an offset voltage to the output offset of the D2S when it drives the VREF pin. The offset has very low drift, but consider the effect of the input bias current times the dc source impedance at VMID_IN (pin 1). When used as a default midsupply reference for single-supply operation, the input to this buffer is just the average of the total power supplies though a 25 kΩ source impedance. Add an external capacitor to filter the supply and the 50 kΩ internal resistors. A 1-µF capacitor on VMID_IN adds a 6-Hz pole to the noise sources. If lower noise at lower frequencies is required, implement a midscale divider with external, lower-valued resistors in parallel with the internal 50 kΩ values.

If the midscale buffer drives the VREF pin, the buffer noise is added to 式 9 and 式 10. The midscale buffer 4.4 nV/√Hz voltage noise is amplified by 0 dB, and adds (RMS) a negligible impact to the total D2S output noise. The biggest impact comes when the internal default 50 kΩ dividers are used. Be sure to decouple VMID_IN with at least a 1 µF capacitor in the application to reduce the noise contribution through this path. 図 8-5 shows the simulation circuit with the 1 µF capacitor installed. 図 8-6 shows the simulated output noise for the midscale buffer using the internal 50 kΩ divider with and without the 1 µF capacitor on VMID_IN.

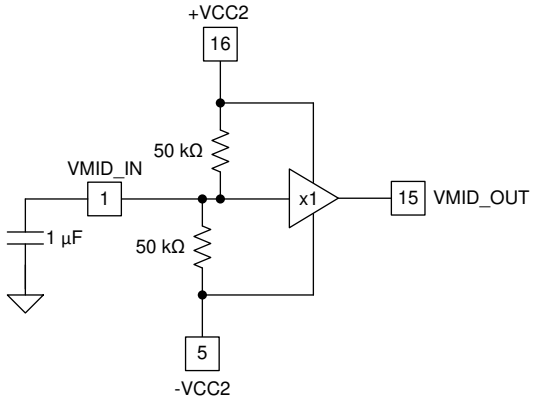


図 8-5. Midscale Buffer Noise Model

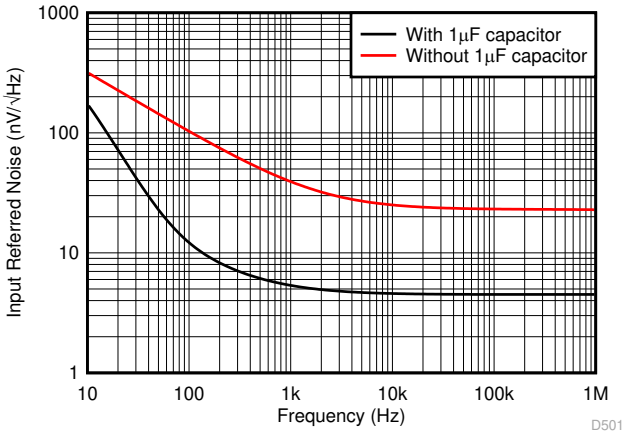


図 8-6. Buffer-Output Noise Comparison With and Without the 1 µF Bypass Capacitor on VMID_IN

In the flat region, the 1 µF capacitor reduces the midscale buffer output spot noise from approximately 55 nV/√Hz to 4.4 nV/√Hz. If the noise below 100 Hz is unacceptable, either add a low-noise buffer to drive this input, or add lower-value resistors externally to set up the midsupply bias. Also, consider the noise impact of any reference voltage source driving the midscale buffer path.

8.3.3 Output Power Stage (OPS) (Pins 4, 7, 9, 10, 11, and 12)

A wideband CFA provides a flexible output driver with several unique features. The OPS can be left unused if the specific application only uses the D2S alone, or a combination of the D2S with an off-chip power driver. If left unused, simply tie DISABLE (pin 10) and PATHSEL (pin 4) to the positive supply. This logic configuration turns the OPS off and opens up the external and internal OPS noninverting input paths. An internal fixed 18.5 kΩ resistor holds the external input pin at the logic reference voltage on GND (pin 7). Additionally, the OPS output is connected to the inverting input through another internal 18.5 kΩ resistor when no external resistors are installed on VIN+, VOUT, or VIN– (pins 9, 11, or 12, repectively). Disabling the OPS saves approximately 11 mA of supply current from the nominal total 35 mA, with all stages operating on ±6 V supplies.

The noninverting input to the OPS provides two possible paths controlled by the PATHSEL logic control. With the logic reference (pin 7) at ground, floating PATHSEL or controlling it to a voltage < 0.7 V connects the input path directly to the internal D2S output. Tying PATHSEL to the positive supply, or controlling it to a logic level > 1.3 V, connects the input path to the external input at VIN+. The intent for this switched input is to allow an external filter to be inserted between the D2S output and OPS inputs when needed, and bypass the filter when not. Alternatively, this switched input also allows a completely different signal path to be inserted at the OPS input, independent of that available at the internal D2S output.

In situations where the D2S output at VO1 (pin 6) is switched into another off-chip power driver, the OPS can be disabled using DISABLE. With the logic reference (pin 7) at ground, floating DISABLE, or controlling it to a voltage < 0.7 V, enables the OPS. Tying DISABLE to the positive supply, or controlling it to a logic level > 1.3 V, disables the OPS.

Operation of the wideband, current-feedback OPS requires an external feedback resistor and a gain element. After configuring, the OPS can amplify the D2S output through either the noninverting path, or be configured as an inverting amplifier stage using the external OPS input at VIN+ as a dc reference.

One of the first considerations when designing with the OPS is determining the external resistor values as a function of gain in order to hold the best ac performance. The loop gain (LG) of a CFA is set by the internal open-loop transimpedance gain from the inverting error current to the output, and the effective feedback impedance to the inverting input. The nominal internal open-loop transimpedance gain (Z_{OL}) magnitude and phase are shown in 図 8-7.

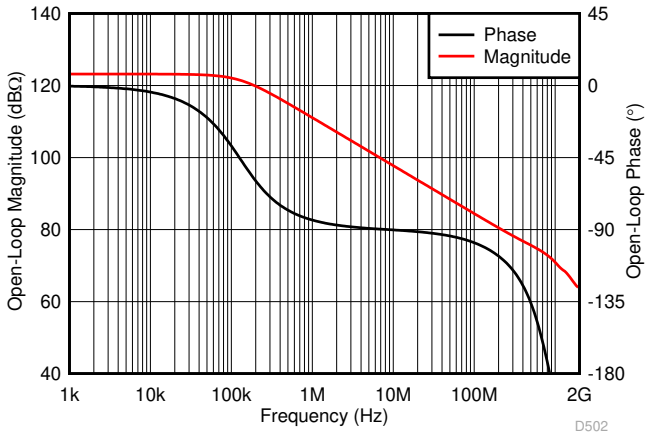


図 8-7. Simulated OPS Z_{OL} Gain Magnitude and Phase

The feedback transimpedance (Z_{OPT}) can be approximated as shown in 式 11, where R_i is the open-loop, high-frequency impedance into the inverting node of the OPS. For a detailed derivation of 式 11, see the *Setting Resistor Values to Optimize Bandwidth* section in the OPA695 datasheet (SBOS293).

$$Z_{OPT} \approx R_F + \left(1 + \frac{R_F}{R_G}\right) R_i \tag{11}$$

As the signal gain is varied, hold Z_{OPT} approximately constant to hold the ac response constant over gain. Holding Z_{OPT} constant is a requirement to solve for R_F. An example of the THS3215 OPS R_F derivation is shown in 式 12:

$$R_F = 430\ \Omega - \left(1 + \frac{R_F}{R_G}\right) \times 74\ \Omega \tag{12}$$

The calculations are complicated by the internal feedback resistor value of approximately 18.5 kΩ. After the external R_F is approximately set by the constant bandwidth consideration, the R_G must be set considering the other gain error terms. From the noninverting input of a CFA, the total gain to the output includes a loss through the input buffer stage (described by the CMRR) and the loop gain (LG) loss set by the typical dc open-loop transimpedance gain and the feedback transimpedance. Extract the buffer gain from the VIN+ input to the VIN– input from the CMRR using 式 13. This gain loss only applies to the noninverting mode of operation and can be ignored in inverting mode operation.

$$\beta = \left(1 - 10^{\frac{-CMRR}{20}}\right) = \text{Buffer Gain CFA} \tag{13}$$

The OPS has a typical CMRR of 53 dB (buffer gain, β = 0.9978) with a tested minimum of 47 dB (minimum buffer gain of 0.9955). The dc LG adds to the gain error. The LG is given by 式 14, where the typical design gain of 2.5 V/V value is also shown (the 245 Ω shown for R_F is the external 249 Ω feedback resistor in parallel with the internal 18.5 kΩ feedback resistor).

$$LG = \frac{Z_{OL}}{\left(R_F + NG \times R_i\right)} = \frac{1.7\ M\Omega}{\left(245\ \Omega + 2.5 \times 74\ \Omega\right)} = 3593 \tag{14}$$

The closed-loop output impedance with a heavy load also adds a minor gain loss that is neglected here. The total noninverting gain is then set by 式 15 (remember to include the internal R_F in this analysis). The $R_{F'}$ shown here is the parallel combination of the internal and external feedback resistors.

$$A_v^+ = \beta \times \left(1 + \frac{R_F}{R_G}\right) \times \frac{LG}{(1 + LG)} \tag{15}$$

Using nominal values for each term at the specified R_F = 249 Ω and R_G = 162 Ω gives the gain calculation in 式 16, yielding a nominal gain very close to 2.5 V/V.

$$A_v^+ = 0.9978 \times \left(1 + \frac{245.7}{162}\right) \times \frac{3593}{1 + 3593} = 2.51 \tag{16}$$

Testing the total gain spread with the internal variation in buffer gain, open-loop transimpedance gain, internal feedback resistor, and ±1% external resistor variation gives a worst-case gain spread of 2.5 V/V to 2.52 V/V. The gain error is primarily dominated by the external 1% resistors. For the tighter tolerance shown in 表 8-1, use 0.1% precision resistors.

At very low gains (< 1.5 V/V), parasitic effects at the inverting input due to stray inductance and capacitance render a flat frequency response impossible. Looking then at gains from 1.5 V/V and up, a table of nominally recommended R_F and R_G values is shown in 表 8-1. Do not operate the OPS in noninverting gains of less than 2.5 V/V for large output signals because the limited slew-rate of the CFA input buffer causes signal degradation. 表 8-1 accounts for the nominal gain losses described previously, and uses standardized resistor values to minimize the nominal gain-error to target gain. The calculation also restricts the solution to a minimum R_G = 20 Ω. The gain calculations include the nominal buffer gain loss, the loop-gain effect, and the nominal internal feedback resistor = 18.5 kΩ.

表 8-1. Optimized R_F Values for Different OPS Noninverting Signal Gains

TARGET GAIN (V/V)	MEASURED SSBW (MHz)	BEST R_F (Ω)	BEST R_G (Ω)	CALCULATED GAIN		GAIN ERROR (%)
				(V/V)	(dB)	
1.5	890	324	634	1.498	3.513	-0.1
2	—	287	280	2.004	6.039	0.22
2.5	700	249	162	2.510	7.995	0.41
3	—	205	102	2.980	9.485	-0.66
3.5	—	169	66.5	3.510	10.905	0.27
4	—	150	49.9	3.972	11.980	-0.7
4.5	—	158	44.2	4.533	13.128	0.73
5	390	158	39.2	4.984	13.952	-0.32
5.5	—	165	36.5	5.467	14.755	-0.6
6	—	169	33.2	6.029	15.605	0.49
6.5	—	169	30.1	6.547	16.321	0.73
7	—	174	28.7	6.989	16.888	-0.16
7.5	—	174	26.7	7.437	17.429	-0.83
8	—	178	24.9	8.060	18.127	0.75
8.5	—	178	23.2	8.578	18.668	0.92
9	—	178	22.1	8.955	19.041	-0.5
9.5	—	182	21	9.558	19.608	0.61
10	93	187	20.5	10.006	20.005	0.06

The measured bandwidths in 表 8-1 come from Frequency Response vs Noninverting Gain using the resistor values in the table and a 100 Ω load. Plotting the R_F value versus gain gives the curve of 図 8-8. The curve shows some ripple due to the standard value resistors used to minimize the target dc gain error.

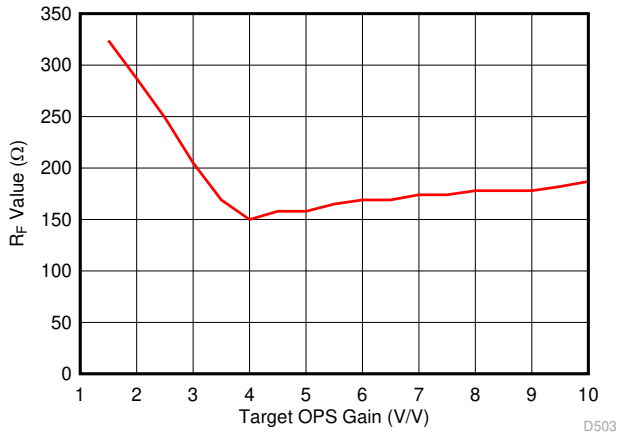


図 8-8. Suggested External R_F Value vs Noninverting Gain for the OPS

Using R_F values greater than the recommended values in 表 8-1 band-limits the response, whereas using less than the recommended R_F values peaks the response. Using the values shown in 表 8-1 results in a more constant SSBW (see Frequency Response vs Noninverting Gain. Holding a more constant loop-gain over the external gain setting also acts to hold a more constant output impedance profile, as shown in 図 8-9. The swept-frequency, closed-loop, output impedance is shown for gains of 2.5 V/V, 5 V/V, and 10 V/V using the R_F and R_G values of 表 8-1. The first two steps do a good job of delivering the same (and very low) output impedance over frequency, while the gain of 10 V/V shows the expected higher closed-loop output impedance due to the reduced loop-gain and bandwidth.

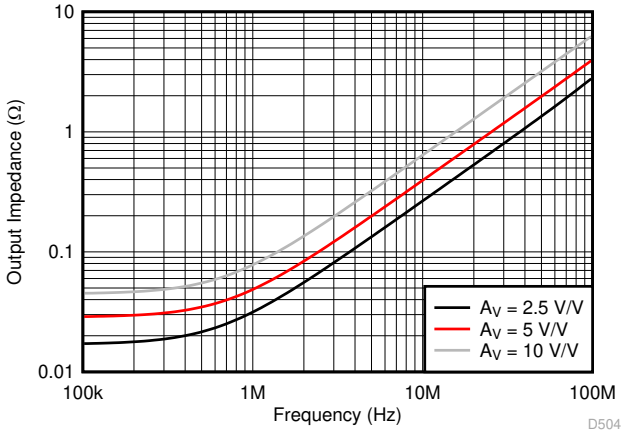


図 8-9. OPS Closed-Loop Output Impedance vs Gain Setting

Reducing the R_F value with increasing gain also helps minimize output noise versus a fixed R_F design. See Input-Referred Spot Noise vs Frequency for the three noise terms for the OPS. The total output noise calculation is shown in 式 17:

$$e_o = \sqrt{\left(e_{ni}^2 + 4kTR_S + \left(i_{bn}R_S\right)^2\right)NG^2 + \left(i_{bi}R_F\right)^2 + \left(4kTR_F\right)NG} \quad (17)$$

where

- R_S is the source impedance on the noninverting input. If the OPS is driven from the D2S directly using the internal path, $R_S \approx 0\ \Omega$.
- $NG = (1 + R_F / R_G)$ for the design point.
- The flat-band noise numbers for the OPS are:
  - $E_{ni} = 2.7\ nV/\sqrt{Hz}$
  - $I_{bn} = 1.3\ pA/\sqrt{Hz}$
  - $I_{bi} = 18\ pA/\sqrt{Hz}$

Using the values of R_F and R_G listed in 表 8-1, a swept gain output- and input-referred noise estimate is computed, as shown in 表 8-2. In this sweep, $R_S = 0\ \Omega$. The input-referred noise (E_{ni}) in 表 8-1 is at the noninverting input of the OPS. To refer the noise to the D2S differential inputs, divide the output noise by two if there is no interstage loss. Dividing the E_{ni} column by 2 V/V shows that the OPS noise contribution is negligible when referred to the D2S inputs, where the 6 $nV/\sqrt{Hz}$ differential input noise dominates. Operating with higher feedback resistors in the OPS quickly increases the output noise due to the inverting input current noise term. Although increasing R_F improves phase margin (for example, when driving a capacitive load), be careful to check the total output noise using 式 17.

表 8-2. Total Input- and Output-Referred Noise of the OPS Versus Gain

TARGET GAIN (V/V)	BEST R_F (Ω)	BEST R_G (Ω)	E_O ($nV/\sqrt{Hz}$)	E_{in} ($nV/\sqrt{Hz}$)
1.5	324	634	7.63	5.09
2	287	280	8.07	4.03
2.5	249	162	8.72	3.47
3	205	102	9.39	3.15
3.5	169	66.5	10.42	2.97
4	150	49.9	11.48	2.89
4.5	158	44.2	13.01	2.87
5	158	39.2	14.21	2.85
5.5	165	36.5	15.53	2.84

表 8-2. Total Input- and Output-Referred Noise of the OPS Versus Gain (continued)

TARGET GAIN (V/V)	BEST R_F (Ω)	BEST R_G (Ω)	E_O (nV/√Hz)	E_{in} (nV/√Hz)
6	169	33.2	17.04	2.83
6.5	169	30.1	18.42	2.81
7	174	28.7	19.63	2.81
7.5	174	26.7	20.83	2.8
8	178	24.9	22.51	2.79
8.5	178	23.2	23.89	2.79
9	178	22.1	29.41	2.78
9.5	182	21	26.54	2.78
10	187	20.5	27.77	2.78

Operating the OPS as an inverting amplifier is also possible. When driving the OPS directly from the D2S to the R_G resistor, use the values shown in 表 8-1 for the noninverting mode in order to achieve optimal results. Note that the R_G resistor is the load for the D2S. Operating with the D2S driving an R_G < 80 Ω increases the harmonic distortion of the D2S. In that case, scaling up R_F and R_G in order to reduce the loading results in better system performance at the cost of a lower OPS bandwidth. In order to reduce layout parasitics, consider splitting the R_G resistor in two, with the first half close to VO1 and the second half close to VIN– (pin 12). Splitting R_G in this manner places the trace capacitance inside the two resistors, thus keeping both active nodes more stable.

Using the OPS to receive and amplify a signal in the inverting mode with a matched terminating impedance requires another resistor to ground (R_M) along with R_G. This R_M resistor is shown in 図 8-10 for a 50 Ω matched input impedance design.

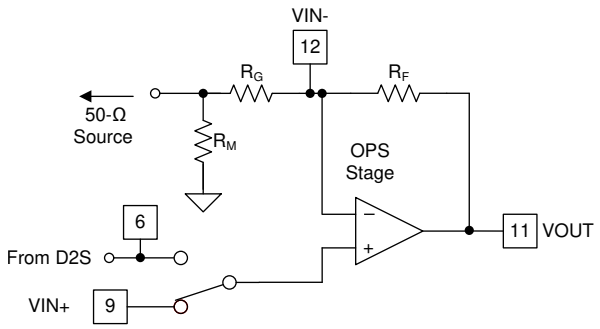


図 8-10. Inverting OPS Operation With Matched Input Impedance

表 8-3 gives the recommended external resistor values versus gain for the inverting gain mode with input matching configuration. 表 8-3 solves for the required R_F to simultaneously allow the gain, input impedance (50 Ω), and feedback transimpedance to be set to the optimal target values. The table includes the effect of the internal 18.5 kΩ feedback resistor, and minimizes the RMS error to input impedance target (Z_I) and overall gain.

表 8-3. Resistor Values Versus Gain for the Inverting OPS Configuration

TARGET GAIN —(V/V)	MEASURED SSBW (MHz)	BEST R_F (Ω)	BEST R_G (Ω)	BEST R_M (Ω)	CALCULATED GAIN		GAIN ERROR (%)	Z_I (Ω)	Z_I ERROR (%)
					—(V/V)	(dB)			
1	700	294	287	60.4	1.008	0.072	0.835	49.90	-0.003
1.5	—	267	174	69.8	1.533	3.712	2.213	49.82	-0.168
2	—	237	118	86.6	2.009	6.061	0.469	49.95	0.091
2.5	700	226	88.7	113	2.543	8.106	1.705	49.69	-0.415
3	—	215	71.5	169	3.017	9.592	0.577	50.24	0.688
3.5	—	210	59	316	3.553	11.011	1.508	49.72	-0.366
4	—	205	51.1	1910	4.006	12.055	0.161	49.77	-0.264

表 8-3. Resistor Values Versus Gain for the Inverting OPS Configuration (continued)

TARGET GAIN —(V/V)	MEASURED SSBW (MHz)	BEST R_F (Ω)	BEST R_G (Ω)	BEST R_M (Ω)	CALCULATED GAIN		GAIN ERROR (%)	Z_I (Ω)	Z_I ERROR (%)
					—(V/V)	(dB)			
4.5	—	226	49.9	Open	4.529	13.120	0.645	49.90	–0.200
5	570	249	49.9	Open	4.990	13.962	-0.201	49.90	–0.200
5.5	—	274	49.9	Open	5.491	14.793	-0.164	49.90	–0.200
6	—	301	49.9	Open	6.032	15.609	0424	49.90	–0.200
6.5	—	324	49.9	Open	6.493	16.249	-0.108	49.90	–0.200
7	—	348	49.9	Open	6.974	16.870	-0.372	49.90	–0.200
7.5	—	374	49.9	Open	7.495	17.495	-0.067	49.90	–0.200
8	—	402	49.9	Open	8.056	18.122	0.701	49.90	–0.200
8.5	—	422	49.9	Open	8.457	18.544	-0.507	49.90	–0.200
9	—	449	49.9	Open	8.998	19.083	-0.023	49.90	–0.200
9.5	—	475	49.9	Open	9.519	19.572	0.200	49.90	–0.200
10	175	499	49.9	Open	10.000	20.000	0.000	49.90	–0.200

At higher gains, R_M increases to larger values, and the resistor is excluded from the circuit. The resulting input impedance of the network is resistor R_G. From that point, R_F simply increases to get higher gains, thereby rapidly reducing the SSBW. However, below a gain of –5 V/V, the inverting design with the values shown in 表 8-3 holds a more constant SSBW versus the noninverting mode (see Frequency Response vs Inverting Gain).

8.3.3.1 Output DC Offset and Drift for the OPS

The OPS provides modest dc precision with typical, minimum, and maximum dc error terms in 表 8-4. The input offset voltage applies to either input path with very little difference between the internal and external paths.

表 8-4. Typical Offset and Bias Current Values for the OPS

PARAMETER	TYPICAL	MINIMUM	MAXIMUM	UNIT
V_{IO}	±1	–15	15	mV
I_{bn}	5	–5	15	µA
I_{bi}	±5	–75	75	µA

Selecting the internal path results in no source resistance for I_{bn}, so that term drops out. When the external path is selected, a dc source impedance may be present, so the I_{bn} term creates another error term, and adds to the total output offset.

Stepping through an example design for the OPS output dc offset using the external path with a low insertion loss filter shown in 図 8-17, along with its R_F and R_G values, gives the following results:

- R_S for the I_{bn} term = 90.9 Ω || 464 Ω = 76 Ω. (dc source impedance for the filter design)
- R_F including the internal 18.5 kΩ resistor = 205 Ω || 18.5 kΩ = 202.7 Ω
- Resulting gain with the 102 Ω R_G element = 2.99 V/V

表 8-5 shows the typical and worst-case output error terms. Note that a positive current out of the noninverting input gives a positive output offset term, whereas a positive current out of the inverting input gives a negative output term.

表 8-5. Output Offset Voltage Contribution From Various Error Terms at 25°C

ERROR TERM	TYPICAL	MINIMUM	MAXIMUM	UNIT
$I_{bn} \times R_S \times A_V$	1.136	–1.136	3.408	mV
$V_{IO} \times A_V$	±2.99	–44.85	44.85	mV
$I_{bi} \times R_F$	±1.014	–15.203	15.203	mV

表 8-5. Output Offset Voltage Contribution From Various Error Terms at 25°C (continued)

ERROR TERM	TYPICAL	MINIMUM	MAXIMUM	UNIT
Total error	–2.87 to +5.14	–61.19	63.46	mV

The input offset voltage dominates the error terms. The worst-case numbers are calculated by adding the individual errors algebraically, but is rarely seen in practice. None of the OPS input dc error terms are correlated. To compute output drift numbers, use the same gains shown in 表 8-5 with the specified drift numbers.

The OPS PATHSEL control responds extremely quickly with low-switching glitches, as shown in 図 8-11. For this test, the D2S input is set to GND, and the output of the D2S is connected to the external OPS input. The PATHSEL switch is then toggled at 10 MHz. The results show the offset between the internal and external paths as well matched.

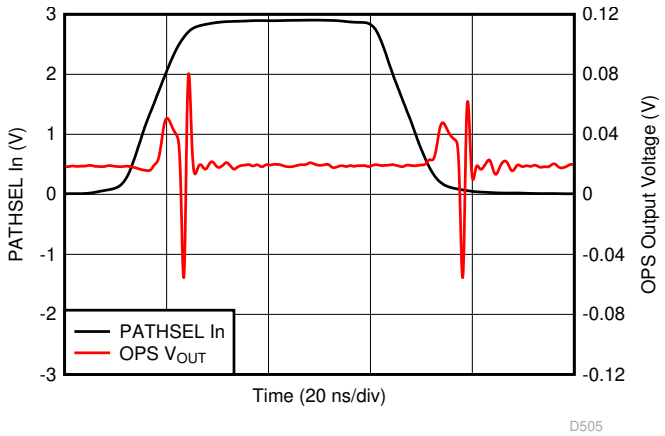


図 8-11. OPS Path-Select Switching Glitch

The OPS includes a disable feature that reduces power consumption from approximately 11 mA to 2 mA. The logic controls are intended to be ground-referenced regardless of the power supplies used. The logic reference (GND, pin 7) is normally grounded and also provides a connection to the internal 18.5 kΩ resistor on VIN+ (pin 9, default bias to pin 7). Operating in a single-supply configuration with $-V_{CC}$ at GND and the external OPS input (VIN+) floated, places VIN+ internally at $-V_{CC}$ = GND. Driving the external OPS input (VIN+) from a source within the operating range overrides the bias to $-V_{CC}$. However, if the application requires VIN+ to be floated in a single-supply operation, consider centering the voltage on VIN+ with an added 18.5 kΩ external resistor to the $+V_{CC}$ supply.

If the disable feature is not needed, simply float or ground DISABLE (pin 10) to hold the OPS in the enabled state. Increasing the voltage on the DISABLE pin to greater than 1.3 V disables the OPS and reduces the current to approximately 2 mA. In a single-supply design, the OPS can be disabled by setting DISABLE to $+V_{CC}$, even up to the maximum operating supply of 15.8 V.

Do not move the logic threshold away from those set by the logic ground at pin 7. If a different logic swing level is required, and GND (pin 7) is biased to a different voltage, be sure the source can sink the typical 280 µA coming out of GND. Also recognize that the 18.5 kΩ bias resistor on the external OPS input (VIN+) is connected to GND voltage internally.

As shown in OPS Enable and Disable Time, the OPS enables in approximately 100 ns from the logic threshold at 1.0 V, while disabling to a final value in approximately 500 ns.

8.3.3.2 OPS Harmonic Distortion (HD) Performance

The OPS in the THS3215 provides one of the best HD solutions available through high power levels and frequencies. HD2 vs Output Voltage and HD3 vs Output Voltage show the swept-frequency HD2 and HD3, where the second harmonic is clearly the dominant term over the third harmonic. Typical wideband CFA distortion is reported only through 2 V_{PP} output, while HD2 vs Output Voltage and HD3 vs Output Voltage

provide sweeps at 5 V_{PP} and 8 V_{PP} into a 100 Ω load. These curves show an approximate 20 dB per decade rise with frequency due to loop-gain roll-off.

The distortion performance is extremely robust as a function of load resistance (see HD2 vs Load Resistance and HD3 vs Load Resistance). Normally, heavier loads degrade the distortion performance, as shown by the HD2 in HD2 vs Load Resistance. However at frequencies greater than 30 MHz, the HD2 actually improves slightly as the output load is increased from 500 Ω to 100 Ω.

One of the key advantages offered by the CFA design in the OPS is that the distortion performance holds approximately constant over gain, as seen in the full-path distortion measurements of HD2 vs Gain and HD3 vs Gain. Here, the D2S provides a fixed gain of 2 V/V driving a 200 Ω interstage load and using the internal path to drive the OPS at gains from 1.5 V/V to 10 V/V. Hold the loop-gain approximately constant by adjusting the feedback R_F value with gain to achieve vastly improved performance versus a voltage-feedback-based design.

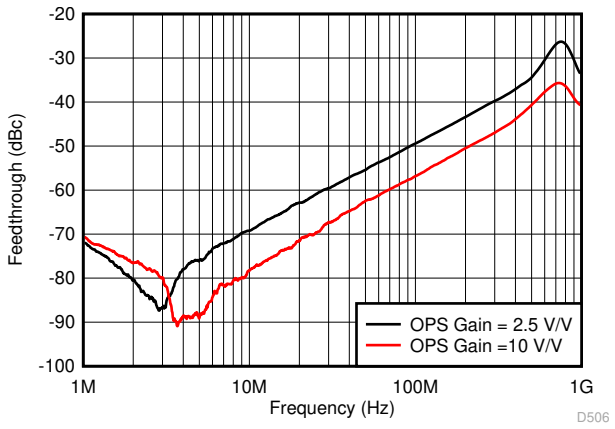
Testing a 5 V_{PP} output from the OPS with the supplies swept from the minimum ±4 V to ±7.5 V in HD2 vs Supply Voltage and HD3 vs Supply Voltage show:

1. The 1.5 V headroom on ±4 V supplies and ±2.5 V output voltage results in degraded performance. At the lower supplies, target lower output swings for improved linearity performance.
2. The HD2 does not change significantly with supply voltages above ±6 V. The HD3 does improve slightly at higher supply-voltage settings.

From these plots at ±7.5 V supplies, a 5 V_{PP} output into 100 Ω load shows better than –60 dBc HD2 and HD3 performance through 30 MHz. This exceptional performance is available with the OPS configured as a standalone amplifier. Combining the standalone OPS performance with the D2S (see HD2 vs Frequency and HD3 vs Frequency) does not degrade the full, signal-path distortion levels. With the D2S and OPS running together at a final 5 V_{PP} output and 30 MHz, the HD2 changes to –63 dBc and HD3 changes to –59 dBc on ±6 V supplies. Lower output swings for the combined stages provide much lower distortion. The 2 V_{PP} output curves on HD2 vs Frequency and HD3 vs Frequency show –61 dBc for HD2 and HD3 at 50 MHz.

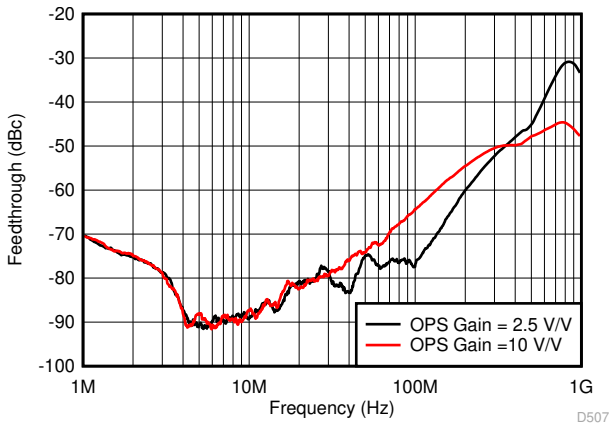
8.3.3.3 Switch Feedthrough to the OPS

The THS3215 uses two logic control pins that enable one of four combinations of states; therefore, various feedthrough effects must be considered. OPS Forward Feedthrough in Disable and OPS Reverse Feedthrough in Disable show the feedthrough of the switches with the OPS disabled. With the OPS enabled, the signal feedthrough from the deselected input to the OPS output is shown in Forward Feedthrough With OPS Enabled, Internal Path Selected and Forward Feedthrough With OPS Enabled, External Path Selected at different closed-loop OPS gains. The results are shown for a 100 mV_{PP} signal at the deselected input, and are not normalized to the gain of the OPS. When the external input of the OPS is selected, add a low-pass filter between the DAC and the D2S inputs to reduce the feedthrough of the DAC high-frequency content .



PATHSEL < 0.7 V,
100 mV_{PP} signal to VIN (pin 9)

図 8-12. Forward Feedthrough With OPS Enabled, Internal Path Selected



PATHSEL > 1.3 V,
100 mV_{PP} signal to VREF (pin 14) with D2S inputs grounded

図 8-13. Forward Feedthrough With OPS Enabled, External Path Selected

8.3.3.4 Driving Capacitive Loads

The OPS can drive heavy capacitive loads very well, as shown in Series Output Resistance vs Load Capacitance to Pulse Response. All high-speed amplifiers benefit from the addition of an external series resistor to isolate the load capacitor from the feedback loop. Not using a series isolation resistor often leads to response peaking and possibly oscillation. If frequency response flatness under capacitive load is the design goal, use slightly higher R_F values at the lower gains. Target a slightly-higher feedback transimpedance to increase the nominal phase margin before the capacitive load acts to decrease it. Using a higher R_F value increases the frequency response flatness across a range of capacitive loads using lower external series resistor values. Although the suggested R_F and R_G values of 表 8-1 apply when driving a 100 Ω load, if the intended load is capacitive (for example, a passive filter with a shunt capacitor as the first element, another amplifier, or a Piezo element), use the values reported in 表 8-6 as a starting point. The values in 表 8-6 were used to generate Series Output Resistance vs Load Capacitance and Frequency Response vs Load Capacitance. The results come from a nominal total feedback transimpedance target of 405 Ω (versus 351 Ω used for 表 8-3), and includes the internal 18.5 kΩ resistor in the design. 表 8-6 finds the least error to target gain in the selection of standard resistor values, and limits the minimum R_G to 20 Ω. The gains calculated here put 18.5 kΩ in parallel with the reported external standard value R_F.

表 8-6. Suggested R_F and R_G Over Gain When Driving a Capacitive Load

TARGET GAIN (V/V)	BEST R_F (Ω)	BEST R_G (Ω)	CALCULATED GAIN		GAIN ERROR (%)
			(V/V)	(dB)	
1.5	487	953	1.494	3.488	–0..389
2	432	422	1.995	6	–0.233
2.5	402	261	2.501	7.963	0.048
3	332	162	3.006	9.559	0.191
3.5	274	107	3.515	10.917	0.416
4	221	73.2	3.974	11.984	–0.662
4.5	165	46.4	4.513	13.090	0.295
5	158	39.2	4.984	13.952	–0.320
5.5	165	36.5	5.467	14.755	–0.602
6	169	33.2	6.029	15.605	0.486
6.5	169	30.1	6.547	16.321	0.729
7	174	28.7	6.989	16.888	–0.161
7.5	174	26.7	7.437	17.429	–0.833

表 8-6. Suggested R_F and R_G Over Gain When Driving a Capacitive Load (continued)

TARGET GAIN (V/V)	BEST R_F (Ω)	BEST R_G (Ω)	CALCULATED GAIN		GAIN ERROR (%)
			(V/V)	(dB)	
8	178	24.9	8.060	18.127	0.753
8.5	178	23.2	8.578	18.668	0.915
9	178	22.1	8.955	19.041	–0.499
9.5	182	21	9.558	19.608	0.613
10	187	20.5	10.006	20.005	0.056

As the capacitive load or amplifier gain increases, the series resistor values can be reduced to hold a flat response (see Series Output Resistance vs Load Capacitance). See Frequency Response vs Load Capacitance for the measured SSBW shapes for various capacitive loads configured with the suggested series resistor from the output of the OPS and the R_F and R_G values suggested in 表 8-6 for a gain of 2.5 V/V. This measurement includes a 200 Ω shunt resistor in parallel with the capacitive load as a measurement path.

HD2 vs Load Capacitance and HD3 vs Load Capacitance demonstrate the OPS harmonic distortion performance when driving a range of capacitive loads. These figures show suitable performance for large-signal, piezo-driver applications. If voltage swings higher than 12 V_{PP} are required, consider driving the OPS output into a step-up transformer. The high peak-output current for the OPS supports very fast charging edge rates into heavy capacitive loads, as shown in the step response plots (see Pulse Response and Pulse Response). This peak current occurs near the center of the transition time driving a capacitive load. Therefore, the I × R drop to the capacitive load through the series resistor is at a maximum at midtransition, and 0 V at the extremes (low dV/dT points). For even better performance driving heavy capacitive loads, consider using the THS3217, a DAC output amplifier with higher output current and slew rate.

8.3.4 Digital Control Lines

The THS3215 provides two logic input lines that control the input path to the OPS and the OPS power disable feature; both are referenced to GND (pin 7). The control logic defaults to a logic-low state when the pins are externally floated. The GND pin must have a dc path to some reference voltage for correct operation. Float the two logic control lines to enable the OPS and select the internal path connecting the D2S internal output to the OPS noninverting input. 図 8-14 shows a simplified internal schematic for either logic control input pin.

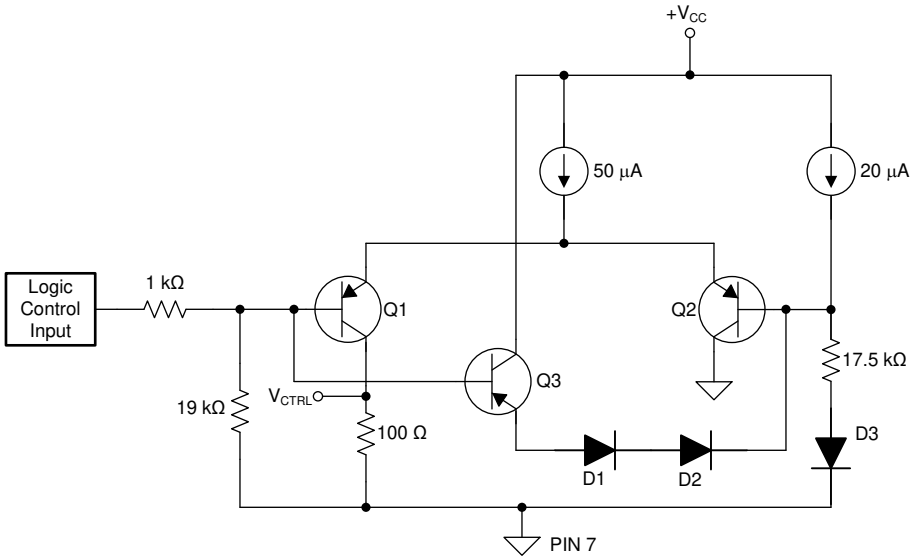


図 8-14. Logic Control Internal Schematic

The Q2 branch of the differential pair sets up a switch threshold approximately 1 V greater than the voltage applied to the GND pin. If the control input is floating or < 0.7 V, the differential-pair tail current diverts to the 100-Ω detector load, and results in an output voltage (V_{CTRL}, shown in 図 8-14) that activates the desired mode. The floated pin default voltage is the PNP base current into the 19 kΩ resistor. As the control pin voltage rises above 1.3 V, the differential-pair current is completely diverted away from the 100 Ω side, thus switching states.

This unique design allows the logic control inputs to be connected to a single-supply as high as 15.9 V, in order to hold the inputs permanently high, while still accepting a low ground-referenced logic swing for single-supply operation. The NPN transistor (Q3) and two diodes (D1 and D2) act as a clamp to prevent large voltages from appearing across the differential stage.

When the OPS is disabled, both input paths to the OPS are also opened up regardless of the state of PATHSEL (pin 4).

8.4 Device Functional Modes

Any combination of the three internal blocks can be used separately, or in various combinations. The following sections describe the various functional modes of the THS3215.

8.4.1 Full-Signal Path Mode

The full-signal path from the D2S to the OPS is available in various options. Three options are described in the following subsections.

8.4.1.1 Internal Connection With Fixed Common-Mode Output Voltage

The most basic operation is to ground VREF (pin 14), and use the internal connection from the D2S to the OPS to provide a differential to single-ended, high-power driver. 図 8-15 shows the characterization circuit used for the combined performance specifications.

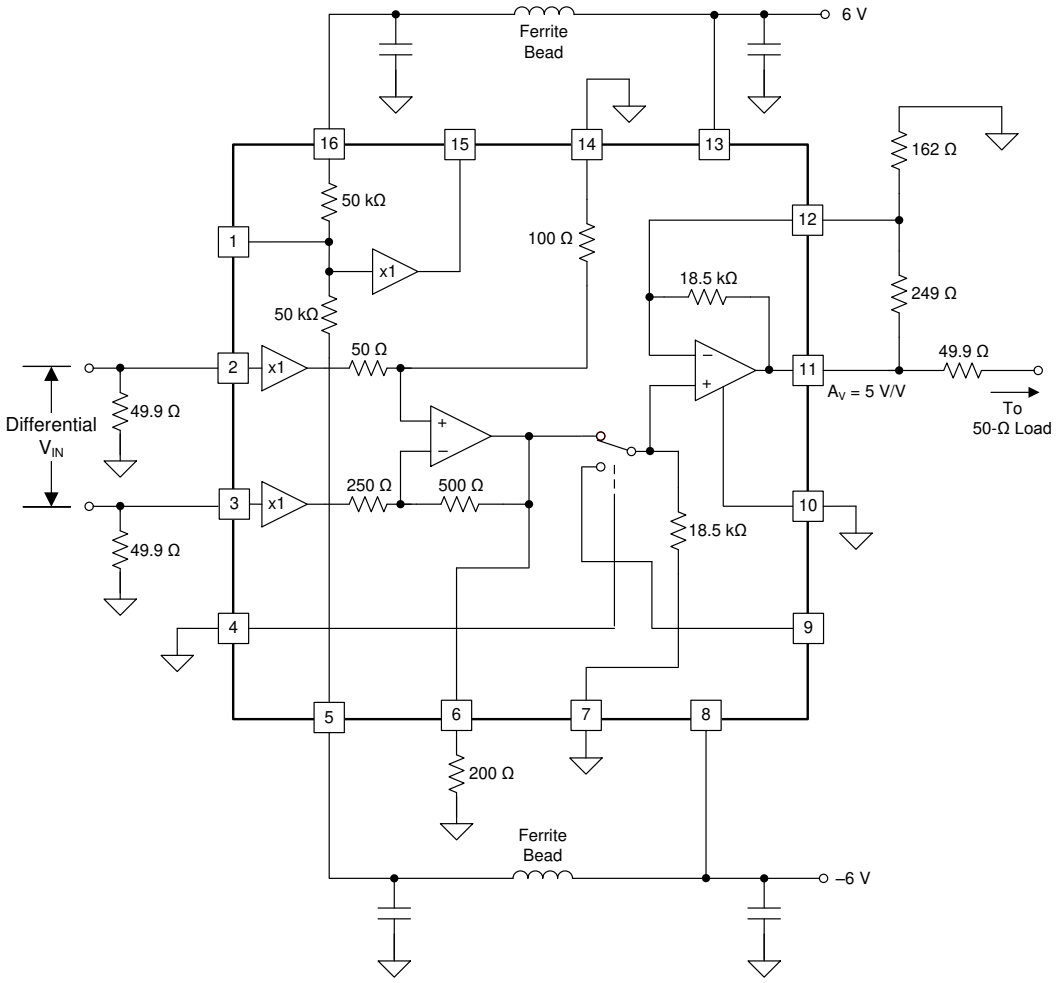


図 8-15. Differential to Single-Ended, Gain of 5 V/V Configuration

This configuration shows the test circuit used to generate Frequency Response vs Output Voltage. Some of the key features in this basic configuration include:

1. The power supplies are brought into the OPS first, then back to the input stage through a π-filter comprised of a ferrite bead and local decoupling capacitors on –VCC2 and +VCC2 (pins 5 and 16, respectively). See the *セクション 10* section for more information.
2. The two logic lines are grounded. This logic configuration (with pin 7 grounded) selects the internal path from the D2S to OPS, and enables the OPS.
3. The external I/O pins of the midscale buffer are left floating.
4. The VREF pin is grounded, thus setting the D2S output common-mode voltage at VO1 (pin 6) to ground.
5. The D2S external output is loaded with a 200 Ω resistor to ground. Lighter loading on the VO1 pin (versus the 100 Ω used to characterize the D2S only) results in increased frequency response peaking. Heavier loading degrades the D2S distortion performance.

6. The external OPS input at VIN+ (pin 9) is left floating. However, VIN+ is internally tied to ground by the internal 18.5 kΩ resistor.
7. The feedback resistor in the OPS is set to the parallel combination of the external 249 Ω resistor and the internal 18.5 kΩ resistor. This 245.7 Ω total R_F with the 162 Ω R_G resistor results in a gain of approximately 2.5 V/V (7.98 dB) in the OPS.
8. The input D2S provides a gain of 2 V/V (6 dB), and along with the 2.5 V/V (7.98 dB) from the OPS, results in an overall gain of 5 V/V (13.98 dB) with > 600 MHz of SSBW (see Frequency Response vs Output Voltage).

8.4.1.2 Internal Connection With Adjustable Common-Mode Output Voltage

The simplest modification to this starting configuration is using the midscale buffer to drive the VREF pin with either a dc or ac source into VMID_IN (pin 1), shown in 図 8-16.

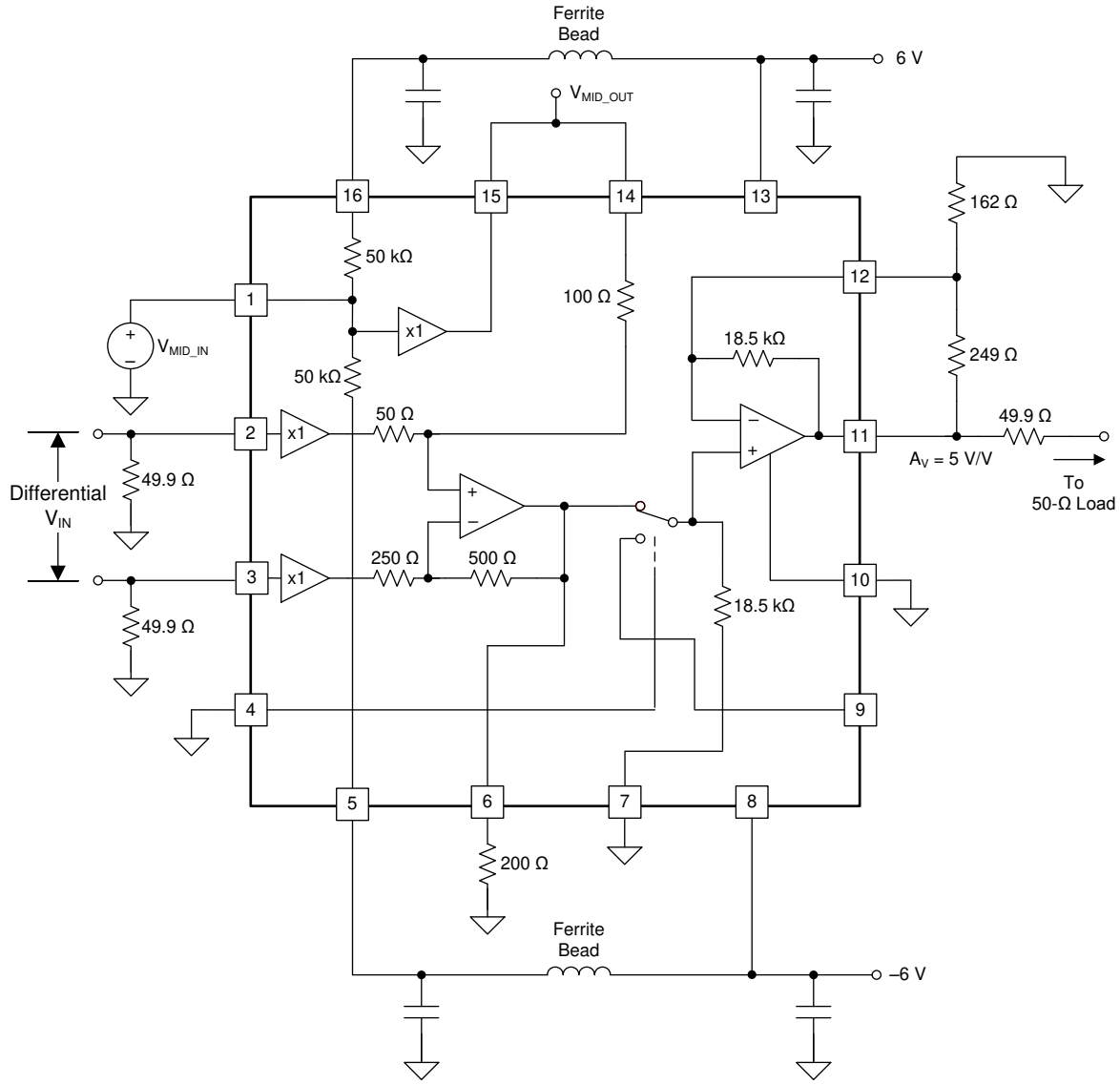


図 8-16. Differential to Single-Ended, Gain of 5 V/V Configuration With VREF Driven by the Midscale Buffer

The VREF input is used to offset the output of the D2S that is then amplified by the OPS. Correct the total dc offset at the output of the OPS by adjusting the voltage at VMID_IN (pin 1). Use the on-chip midscale buffer as a low-impedance source to drive the correction voltage to the VREF pin. A wideband small-signal source can also be summed into this path with a gain of 1 V/V to the D2S output pin. Frequency Response vs Output Voltage shows the midscale buffer to have an extremely flat response through 100 MHz for < 100 mV_{PP}swings, while 1 V_{PP} is supported through 20 MHz with a flat response.

From this point on, the diagrams are simplified to not show the power-supply elements. However, the supplies are required by any application, as described in the *セクション 9* section.

8.4.1.3 External Connection

In the configuration shown in 図 8-17, the bias to PATHSEL (pin 4) is changed in order to select the external input of the OPS. The external D2S output drives a low insertion loss, third-order Bessel filter. The filter in this example is designed with a low frequency insertion loss of 1.55 dB and f_{-3dB} = 50 MHz, and results in an additional insertion loss of 1 dB at 30 MHz. The OPS gain is slightly increased to recover the filter loss, in order to give an input to output gain of 5 V/V. Using an interstage filter between the D2S and the OPS improves the step response by reducing the overshoot. The filter in this example has a relatively low cutoff frequency but if the application requires it, use a filter with a higher cutoff frequency.

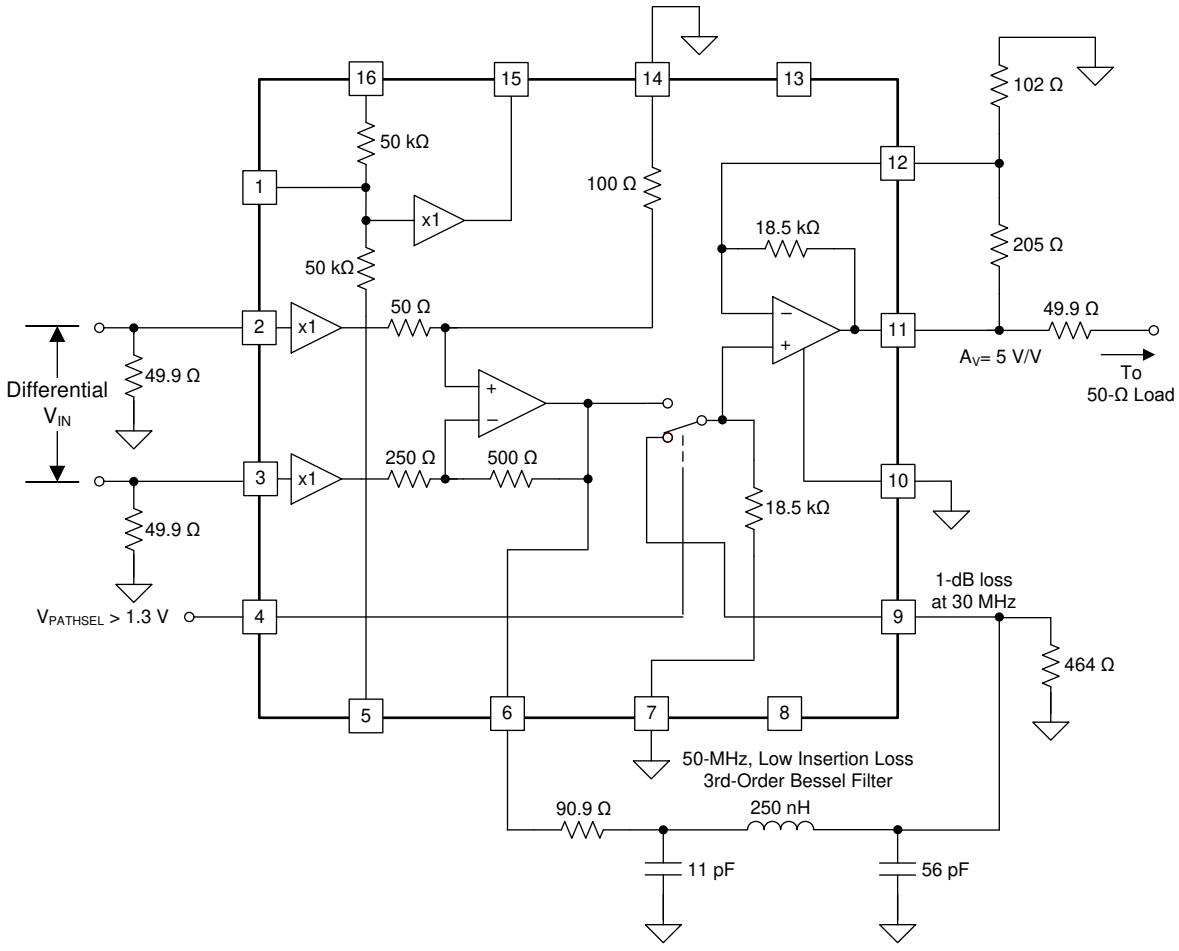


図 8-17. External Path Configuration With Interstage Low-Pass Filter

8.4.2 Dual-Output Mode

The D2S is also used to directly drive a doubly-terminated line, as shown in 図 8-18. In addition, the OPS amplifies the internal D2S output by 5 V/V. The internal path to the OPS is selected with PATHSEL (pin 4) at ground, and the OPS gain is increased to 5 V/V. A 2 V_{PP} output at VO1 produces a 10 V_{PP} output at VOUT (pin 11). This 10 V_{PP} swing requires higher supply operation to provide sufficient headroom in the OPS output stage in order to preserve signal integrity. A power supply of ±7.5 V provides adequate headroom.

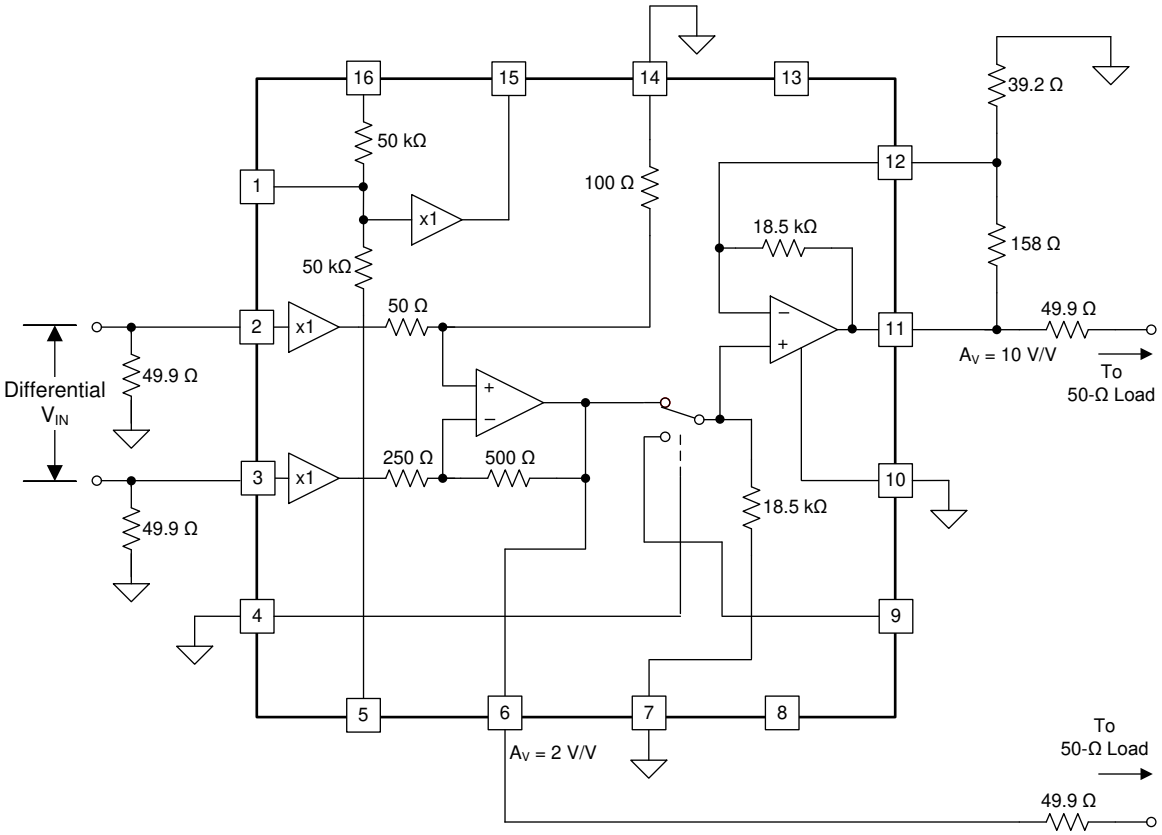


図 8-18. Dual-Output Mode

A simple modification to the circuit in 図 8-18 is to disable the OPS. The D2S output at VO1 can then be used either directly or through a filter to an even higher power driver, such as the ±15 V THS3091.

8.4.3 Differential I/O Voltage Mode

Having two amplifiers available also allows a simple differential I/O implementation with independent output common-mode control, as shown in 図 8-19. In this configuration, the D2S provides one side of the differential output, while simultaneously driving the OPS configured in an inverting gain of –1 V/V to provide the differential output on the other side. The output at VMID_OUT (pin 15) biases the external noninverting input, VIN+ (pin 9). This circuit configuration places the differential input to the output filter at a common-mode voltage, V_{MID_OUT}.

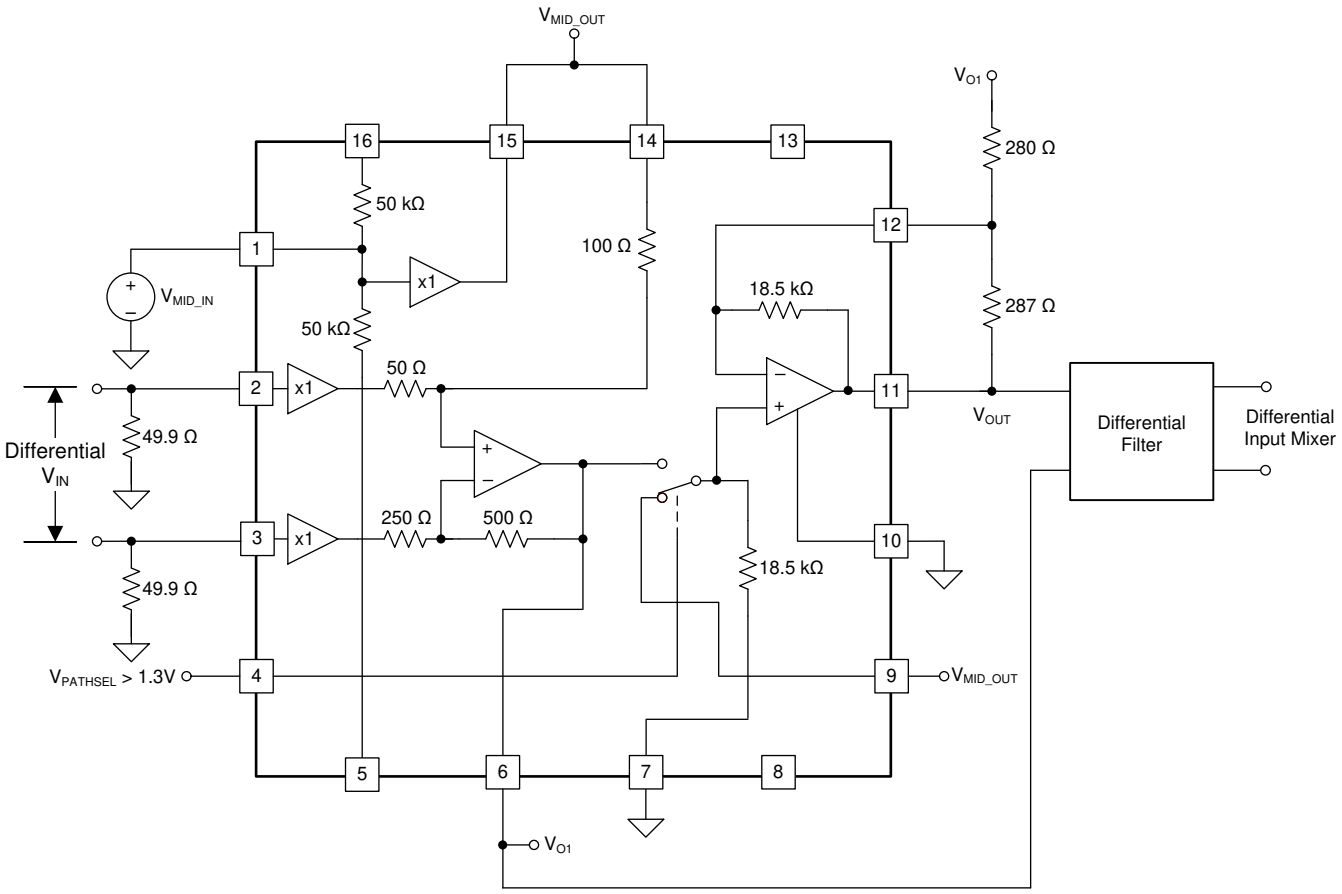


図 8-19. Differential I/O Configuration With Independent Output Common-Mode Voltage Control

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Typical Applications

The five example designs presented show a good, but not comprehensive, range of the possible solutions that the THS3215 provides. Numerous more configurations are clearly possible to the creative designer.

9.1.1.1 High-Frequency, High-Voltage, Dual-Output Line Driver for AWGs

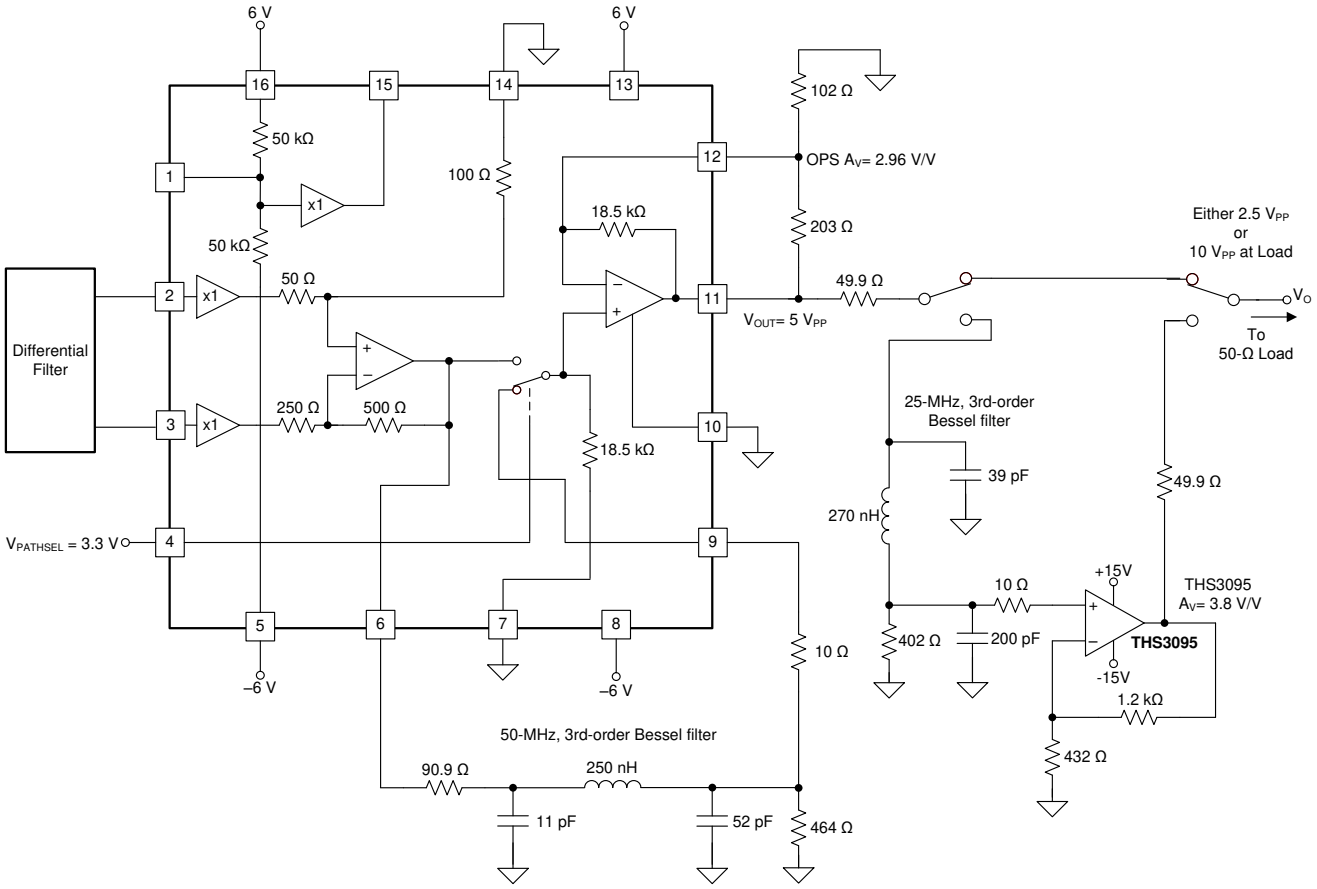


図 9-1. Dual-Channel Design: 5 V_{PP} at THS3215 Output and 20 V_{PP} at THS3095 Output

9.1.1.1.1 Design Requirements

For this design example, use the parameters listed in 表 9-1 as the input parameters.

表 9-1. Dual-Output Design Specifications

DESIGN PARAMETER	EXAMPLE VALUE
High-frequency, THS3215 channel	5 V_{PP}, 50 MHz bandwidth
High-voltage, THS3095 channel	20 V_{PP}, 25 MHz bandwidth

9.1.1.1.2 Detailed Design Procedure

The THS3215 is well suited for high-speed, low-distortion arbitrary waveform generator (AWG) applications commonly used in laboratory equipment. In this typical application, a high-speed, complementary-current-output DAC is used to drive the D2S. The OPS of the THS3215 easily drives a 50 MHz, 2.5 V_{PP} signal into a matched 50 Ω load. When a larger output signal is required, consider using the THS3095 as the final driver stage.

A passive RLC filter is commonly used on DAC outputs to reduce the high-frequency content in the DAC steps. The filtering between the DAC output and the input to the D2S reduces higher-order DAC harmonics from feeding into the internal OPS path when the external input path is selected. Feedthrough between the internal and external OPS paths increases with increasing frequency; however, the input filter rolls off the DAC harmonics before the harmonics couple to VOUT (pin 10) through the deselected OPS signal path. 図 9-2 shows an example of a doubly-terminated differential filter from the DAC to the THS3215 D2S inputs at +IN (pin 2) and –IN (pin 3). The DAC is modeled as two, fixed, 10 mA currents and a differential, ac-current source. The 10 mA dc midscale currents set up the average common-mode voltage at the DAC outputs and D2S inputs at 10 mA × 25 Ω = 0.25 V_{CM}. The total voltage swing on each DAC output is 0 V to 0.5 V.

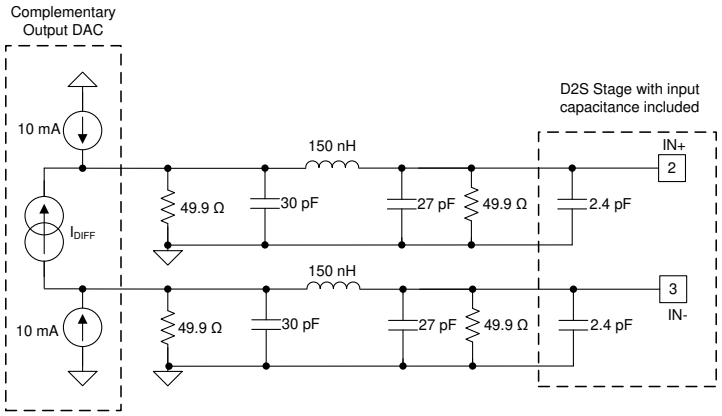


図 9-2. 105 MHz Butterworth Filter Between DAC and D2S Inputs

Some of the guidelines to consider in this filter design are:

1. The filter cutoff is adjusted to hit a standard value in the standard high-frequency, chip inductors kits.
2. The required filter output capacitance is reduced from the design value of 29.4 pF to 27 pF to account for the D2S input capacitance of 2.4 pF, as reported in the *D2S Electrical Characteristics* table.
3. The capacitor at the DAC output pins must also be reduced by the expected DAC output pin capacitance. The DAC output capacitance is often specified as 5 pF, but is usually much lower. Contact the DAC manufacturer for an accurate value.

図 9-3 shows the TINA-simulated filter response for the input-stage filter. The low-frequency 34 dBΩ gain is due to the 50 Ω differential resistance at the DAC output terminals. At 200 MHz, this filter is down 17 dB from the 50 Ω level; it is also very flat through 50 MHz.

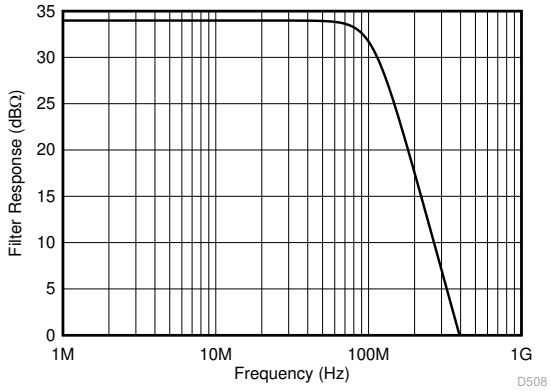


図 9-3. Simulated, Differential-Input Filter Response

In the example design of 図 9-1, a 50 MHz, third-order Bessel filter is placed between the D2S output and the external OPS input. Another 25 MHz, third-order Bessel filter is placed at the input of a very-high output-swing THS3095 stage. A double-pole, double-throw (DPDT) relay selects the THS3095 path when the internal OPS path is selected in the THS3215. 図 9-1 shows this design. The key operational considerations in this design include:

1. When the external input OPS path is selected, the 2 V_{PP} maximum D2S output swing experiences a 1.55 dB insertion loss from the interstage filter between VO1 (pin 6) and VIN+ (pin 9). A standard value inductor is used and the 464 Ω termination accounts for the internal 18.5 kΩ element. The 10 Ω resistor at VIN+ isolates the OPS input from the 52 pF filter capacitor. To recover the insertion loss and produce a maximum 5 V_{PP} output, the OPS gain is set to 2.96 V/V. When the interstage filter path is selected, the two DPDT relays pass the OPS output on directly from the 49.9 Ω output matching resistor to V_O. Disable the THS3095 to conserve power.
2. To deliver 20 V_{PP} at the V_O output, select the THS3095 path. Select the internal OPS path to bypass the 50 MHz filter (1.55 dB insertion loss) in order to give a maximum 5.9 V_{PP} output at VOUT (pin 11). The two DPDT relays switch position, and the 49.9 Ω at the OPS output becomes part of the 25 MHz, third-order Bessel filter into the THS3095 stage. This filter has a 1 dB insertion loss requiring a gain of 3.8 V/V in the THS3095 to deliver 20 V_{PP} from the OPS output.
3. Frequency Response of the 5 V_{PP} and 20 V_{PP} Channels and Harmonic Distortion Performance of the 5 V_{PP} and 20 V_{PP} Channels show the frequency response and harmonic distortion performance of the dual output-voltage system. The frequency response is normalized to 0 dB to make bandwidth comparisons easier.

9.1.1.1.3 Application Curves

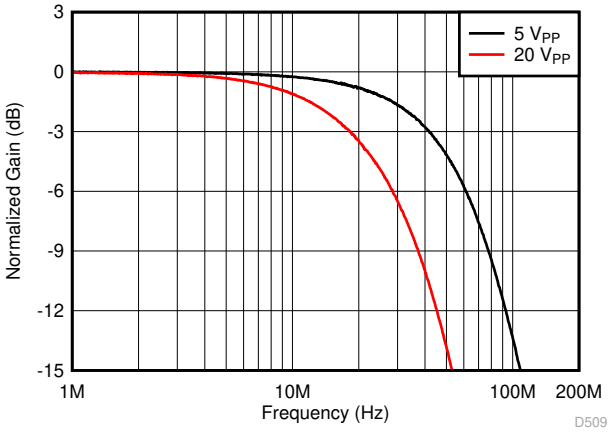


図 9-4. Frequency Response of the 5 V_{PP} and 20 V_{PP} Channels

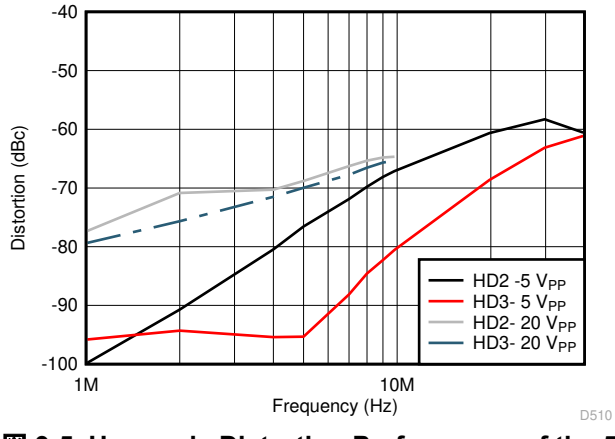


図 9-5. Harmonic Distortion Performance of the 5 V_{PP} and 20 V_{PP} Channels

9.1.1.2 High-Voltage Pulse-Generator

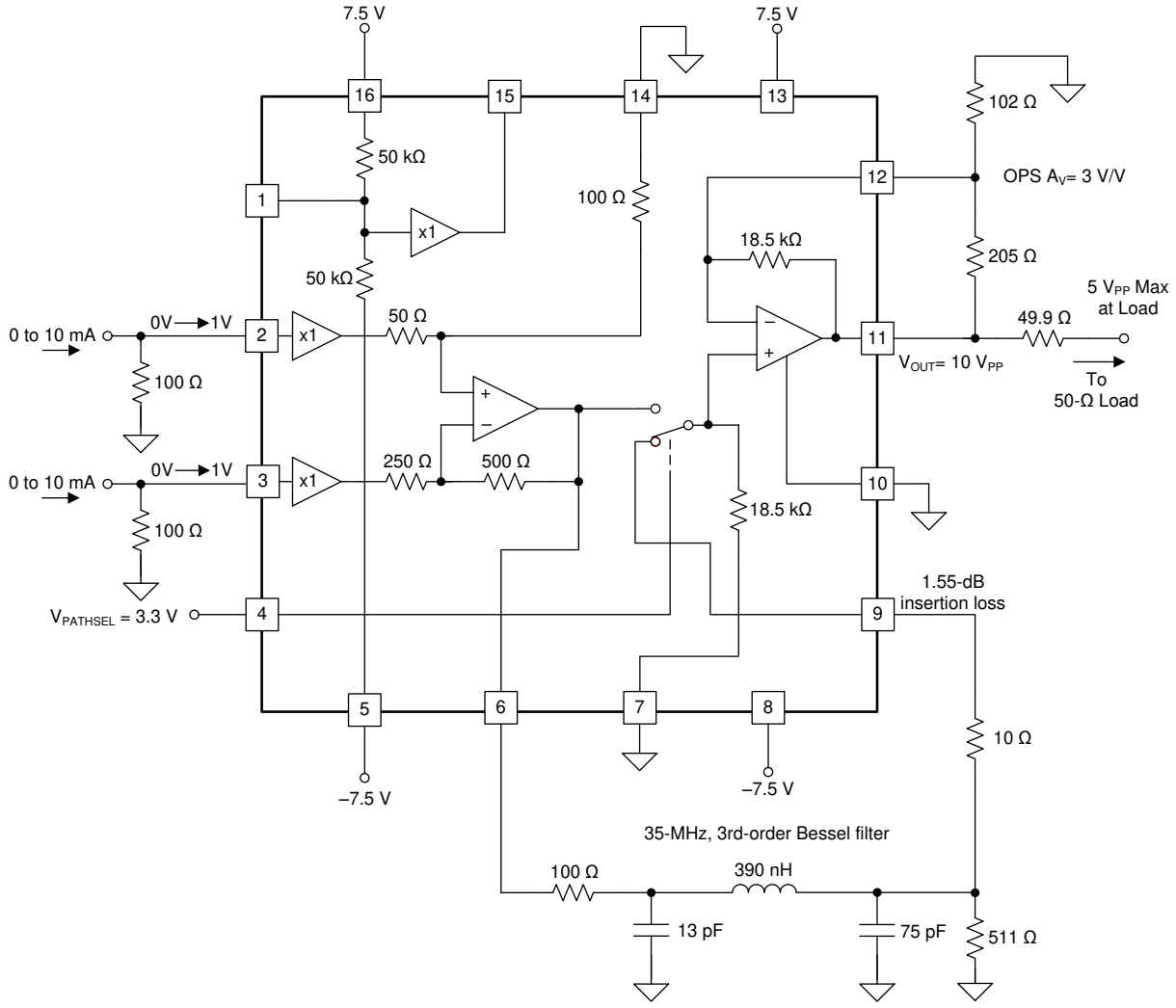


図 9-6. Driving a 10 V_{PP} Pulse Output into a 100 Ω Load With a 35 MHz External Interstage Bessel Filter

9.1.1.2.1 Design Requirements

To design a high-voltage, high-speed pulse generator with minimum overshoot, use the parameters listed in 表 9-1 as the input parameters.

表 9-2. Pulse-Generator Specifications

DESIGN PARAMETER	EXAMPLE VALUE
Power supply	±7.5 V
Pulse frequency	5 MHz
Pulse output voltage	10 V_{PP}

9.1.1.2.2 Detailed Design Procedure

図 9-6 shows an example design using the THS3215 to deliver a 10 V_{PP} maximum voltage from a DAC input, and includes an example external, third-order, interstage Bessel filter. Some of the salient considerations for this design include:

1. Termination resistance at the D2S inputs is increased to reduce DAC output current. This example is intended to be used with a current-sourcing DAC with an output compliance voltage of at least 1 V on a 0.5 V common-mode voltage. The 10-mA, single-ended, DAC tail current produces a 0 V to 1 V swing on each 100 Ω termination. The resulting 2 V_{PP} differential DAC signal produces a higher SNR signal at the THS3215 inputs.
2. The midscale buffer is not used. VREF (pin 14) is grounded to set the inputs to a 4-V_{PP} ground-centered maximum output swing at VO1 (pin 6). The external input to the OPS is selected by setting PATHSEL (pin 4) to 3.3 V (anything over 1.3 V is adequate, or tie this pin to +V_{CC} for fixed, external-path operation).
3. The interstage Bessel filter is –0.3 dB flat through 12 MHz, with only 1.55 dB of insertion loss. The filter is designed to be low insertion-loss with relatively high resistor values. The filter uses standard inductor values. The capacitors are also standard-value, and slightly off from the exact filter solution. The final resistor to ground is designed for 500 Ω, but increased here to a standard 511 Ω externally to account for the internal 18.5 kΩ resistor on the external OPS input pin to GND. To isolate the last 75 pF filter capacitor from the OPS input stage, a 10 Ω series resistor is added close to the VIN+ (pin 9) input.
4. The filter adds 1.55 dB of insertion loss that is recovered, to achieve a 10 V_{PP} maximum output by designing the OPS for a gain of 3 V/V. Looking at 表 8-6, this gain setting requires the 205 Ω external R_F and 102 Ω R_G to ground for best operation.
5. For 10 V_{PP} maximum output, the ±7.5 V supplies shown in 図 9-6 give adequate headroom in the OPS output stage. The operating maximum supply of 15.8 V requires a 5% tolerance on these ±7.5 V supplies.
6. The Bessel filter gives a very low overshoot full-scale output step-response, as shown in the 5 MHz, ±5 V square wave of Pulse Response of the System With the Interstage Bessel Filter. The frequency response of the system is shown in Frequency Response of the System With the Interstage Bessel Filter.

9.1.1.2.3 Application Curves

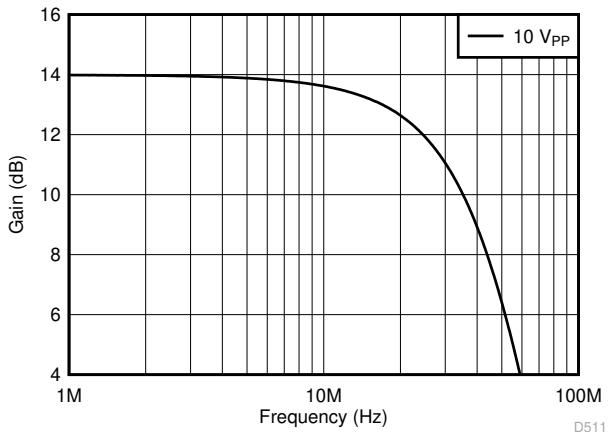


図 9-7. Frequency Response of the System With the Interstage Bessel Filter

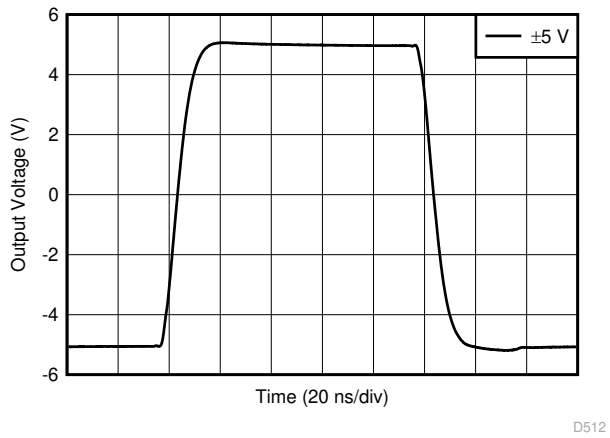


図 9-8. Pulse Response of the System With the Interstage Bessel Filter

9.1.1.3 Single-Supply, AC-Coupled, Piezo Element Driver

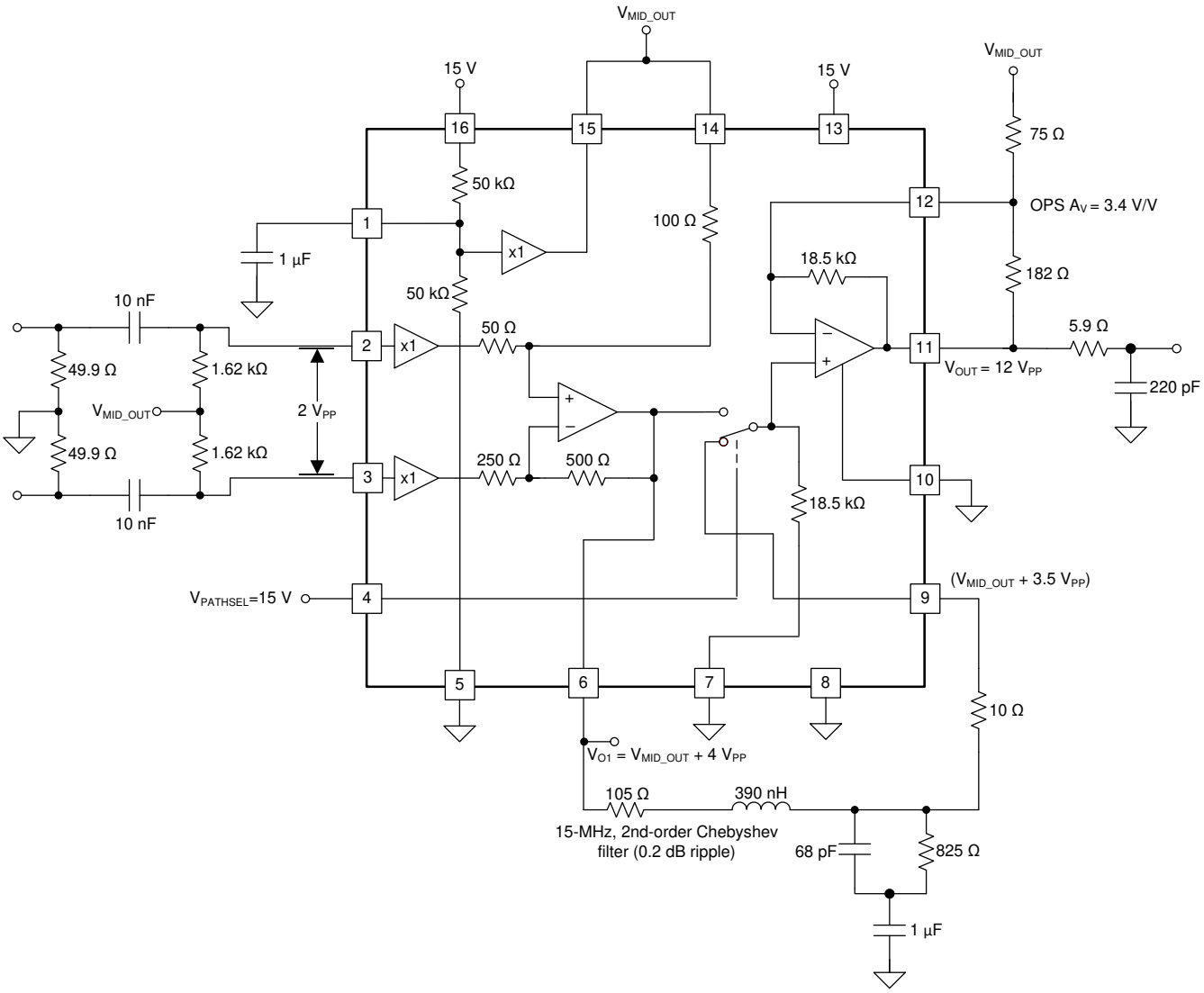


図 9-9. Single-Supply, Heavy Capacitive-Load Driving

9.1.1.3.1 Detailed Design Procedure

The very-high peak output current and slew rate of the THS3215 OPS make it particularly suitable for driving heavy capacitive loads, such as the piezo elements used in continuous wave (CW) applications that require high-amplitude, sinusoidal-type excitations. The driver is quickly disabled during the receive time when the output transmit and receive switch is moved to receive mode. 図 9-9 shows an example design using the internal midscale buffer to bias all the stages to midsupply on a single 15 V design. There are many elements to this example that also apply to any single-supply application. The key points here are:

1. The differential DAC input signal is ac-coupled to the D2S input, and the termination resistors are scaled up and biased to midsupply using the output of the midscale buffer, VMID_OUT (pin 15). The 10-nF blocking capacitors before the 1.62 kΩ termination resistors set the high-pass pole at 10 kHz.
2. The internal divider resistors of the midscale buffer are decoupled using a 1 µF capacitor on VMID_IN (pin 1). Use of the capacitor improves both noise and PSRR through the reference buffer stage. In turn, the noise injected by the bias source is reduced at the various places the buffer output is used.

3. V_{MID_OUT} is also applied to the VREF input (pin 14) to hold the D2S output centered on the single 15 V supply. There is minimal dc current into VREF because the D2S input buffers operate at the same common-mode voltage, V_{MID_OUT}.
4. The D2S output is dc biased at midsupply and delivers two times the differential swing applied at its inputs. Assuming 2 V_{PP} at the D2S inputs implies 4 V_{PP} at the D2S output pins. Lower input swings are supported with the gain in the OPS adjusted to meet the desired output maximum.
5. The filter in 図 9-9 is a 0.2 dB ripple, second-order Chebyshev filter at 15 MHz. For example, if the desired maximum frequency is 12 MHz, this filter attenuates the HD2 and HD3 out of the D2S by approximately 3 dB and 5 dB, respectively. Increased attenuation can be provided with higher-order filters, but this simple filter does a good job of band-limiting the high-frequency noise from the D2S outputs before the noise gets into the OPS.
6. The dc bias voltage at VO1 (pin 6) drives a small dc current into the 18.5 kΩ resistor to ground at the OPS external input, VIN+ (pin 9). The error voltage due to the bias current level-shifts the dc voltage at the OPS noninverting input through the 105 Ω filter resistor. This offset is amplified by the OPS gain because the R_G element is referenced to the V_{MID} output with a dc gain of 3.4 V/V.
7. The logic lines are still referenced to ground in this single-supply application. The external path to the OPS is selected by connecting PATHSEL (pin 4) to $+V_{CC}$. DISABLE (pin 10) is grounded in this example in order to hold the OPS on. If the disable feature is required by the application, drive DISABLE (pin 10) using a standard logic control driver. Note that the midscale buffer output still drives R_G and R_F to midsupply in this configuration with the OPS disabled.
8. To operate at midsupply, ac-couple the R_G element to ground through a capacitor. 図 9-9 shows the midscale buffer driving R_G, thus eliminating the need for an added capacitor. Use a blocking capacitor to move the dc gain to 1 V/V. The voltage on the external, noninverting input of the OPS sets the dc operating point. Use a blocking capacitor to lighten the load on the midscale buffer output and eliminate the bias on R_G when the OPS is disabled.
9. Piezo element drivers operate in a relatively low-frequency range; therefore, the OPS R_F is scaled up even further than the values suggested in 表 8-6. An increased R_F allows R_G to also be scaled up, thereby reducing the load on the midscale buffer, and allow a lower series output resistor to be used into the 220 pF capacitive load.
10. The peak charging current into the capacitive load occurs at the peak dV/dT point. Assuming a 12 MHz sinusoid at 12 V_{PP} requires a peak output current from the OPS of 6 $V_{PEAK} \times 2\pi \times 12$ MHz × 220 pF = 100 mA. This result is slightly lesser than the rated minimum peak output current of the OPS.

Using a very low series resistor limits the waveform distortion due to the I × R drop at the peak charging point around the sinusoidal zero crossing. The 100 mA through 5.9 Ω causes a 0.59 V peak drop to the load capacitance around zero crossing. The voltage drop across the series output resistor increases the apparent third harmonic distortion at the capacitive load. HD2 vs Load Capacitance and HD3 vs Load Capacitance show 10 V_{PP} distortion sweeps into various capacitor loads. The results shown in these figures are for the OPS only because the results set the harmonic distortion performance in this example.

9.1.1.4 Output Common-Mode Control Using the Midscale Buffer as a Level Shifter

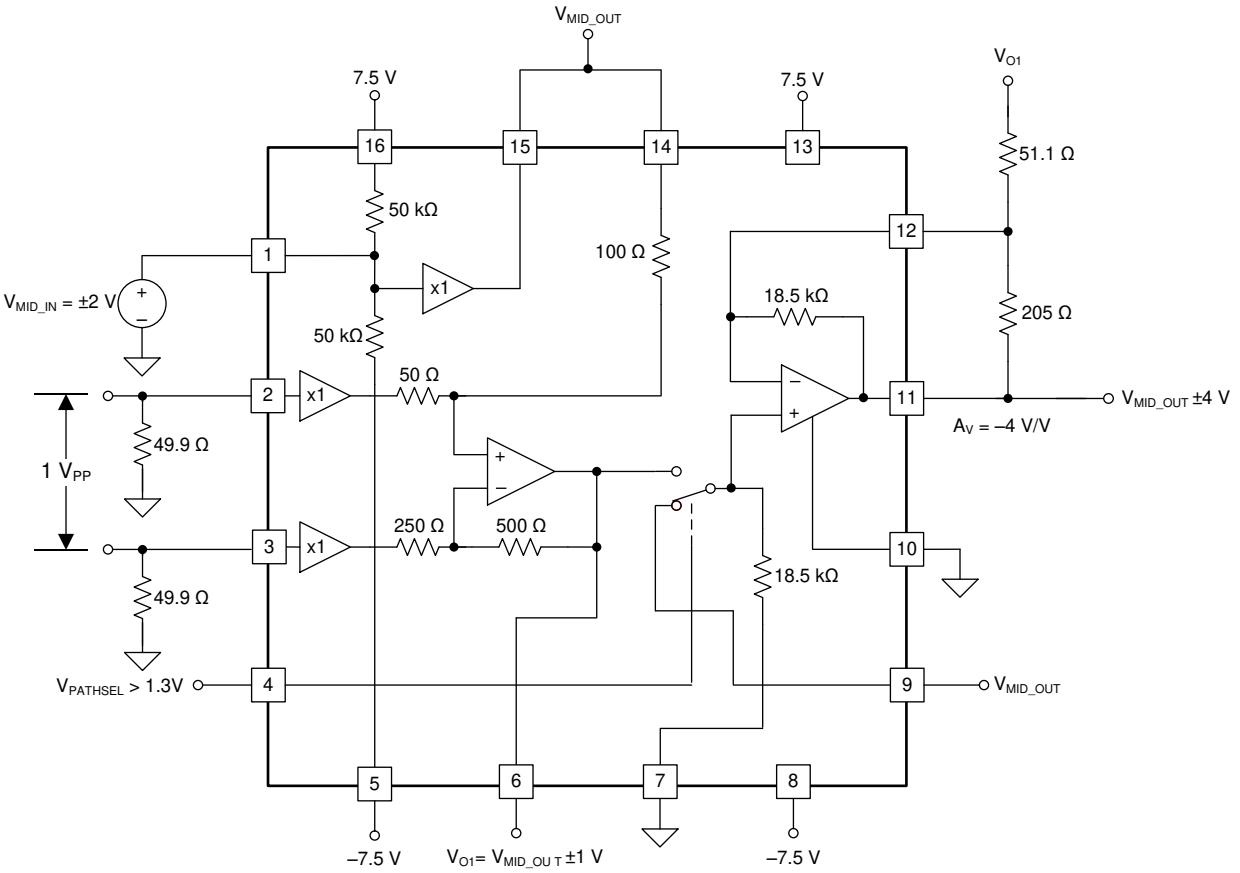


図 9-10. Adding an Output DC Offset Using the Midscale Buffer

9.1.1.4.1 Detailed Design Procedure

An easy way to insert a dc offset into the signal channel (without sacrificing any of the DAC dynamic range) is to apply the desired offset at VMID_IN (pin 1) and use it to bias VREF (pin 14) and VIN+ (pin 9). An example is shown in 図 9-10. This example shows a relatively low maximum differential input of 1 V_{PP} on any compliance voltage required by the DAC. Other configuration options include:

1. The D2S output is offset using a dc input at VMID_IN. Although shown here as ±2 V, the dc range expands to ±3.5 V when using ±7.5 V supplies.
2. Connect VMID_OUT (pin 15) to the VREF input to place the D2S output at the dc offset voltage along with a gain of 2 V/V version of the differential input voltage. The stated range of ±2 V, along with the ±0.5 V out of the upper input buffer, requires a peak output current from VMID_OUT of 2.5 V / 150 Ω = 16.7 mA. This value is well below the rated minimum linear output current of 40 mA for the midscale buffer.
3. The dc offset voltage is then applied to the external OPS non-inverting input, VIN+. Connecting the circuit in this manner results in no additional dc gain for the dc offset between the D2S and OPS outputs, while continuing to retain the signal gain of the OPS configured as an inverting amplifier. The values of R_F and R_G in this application example are derived from 表 8-3. The OPS is setup for a gain of –4 V/V in this example. Using the resistor values from 表 8-3 results in the widest bandwidth for the OPS; however, the R_G = 51.1 Ω resistor presents a heavy load to the D2S output. In such cases, the OPS external resistors can be scaled up to reduce the D2S output load, but at the expense of reduced OPS bandwidth.
4. No filtering is shown in this example; however, introducing filtering in the OPS R_G path is certainly possible. In such cases, the R_G element is also the filter termination resistor. Filtering adds insertion loss that can be recovered by adjusting the OPS gain setting.

9.1.1.5 Differential I/O Driver With independent Common-Mode Control

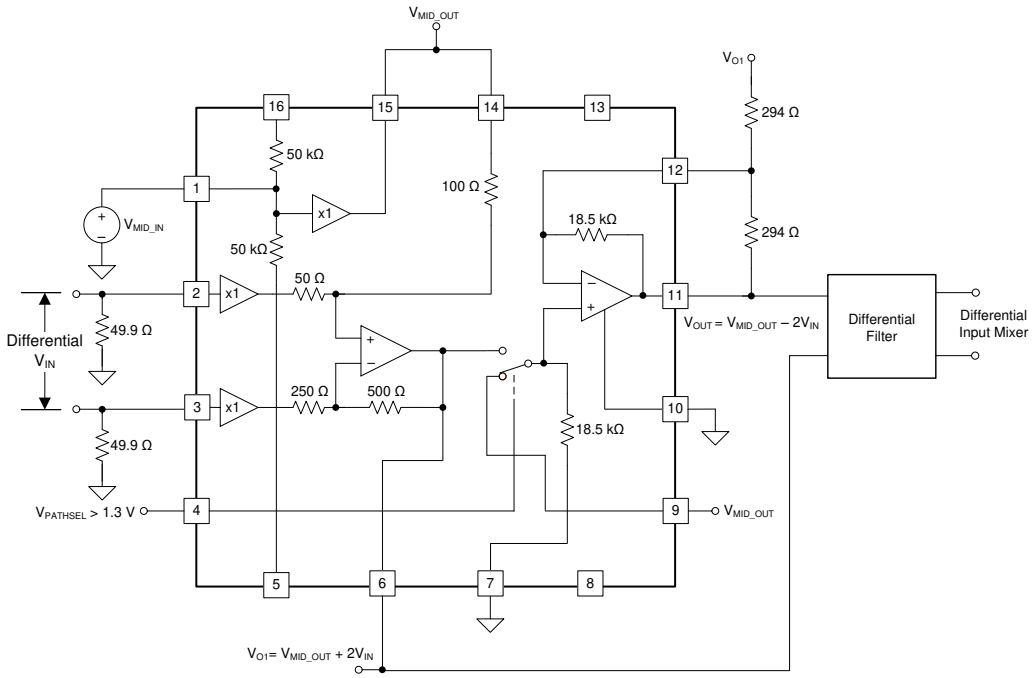


図 9-11. Differential I/O with Common-Mode Control

9.1.1.5.1 Detailed Design Procedure

Certain applications require the differential DAC output voltage to be translated from one common-mode (compliance) level to a differential output at a different common-mode level. The THS3215 performs voltage-level translation directly using the very flexible blocks provided internally. 図 9-11 shows an example of such an application, where the differential gain is always 4 V/V. The differential gain is fine-tuned down by setting the insertion loss in the differential post-filter. The considerations critical to this application include:

1. The input is dc-coupled with the appropriate termination impedance required by the DAC. Use a high-frequency, antialiasing filter at the input to limit DAC feedthrough in the deselected OPS internal input.
2. The output common-mode control is set with the voltage applied to the VMID buffer input at VMID_IN (pin 1). The circuit is configured so that the output at VMID_OUT (pin 15) drives both VREF (pin 14), in order to set the D2S dc output voltage, and VIN+ (pin 9).
3. The D2S output available at VO1 (pin 6) provides one side of the differential-output, and is dc-biased at V_{MID_OUT}. VO1 also drives the R_G resistor for the OPS in an inverting gain of –1 V/V. The dc bias level at the R_G input and the VIN+ input of the OPS are the same voltage; therefore, no level shift through the OPS occurs. The OPS outputs an inverted version of the D2S output signal at the same common-mode voltage (V_{MID_OUT}). The wideband, differential signal with independent output common-mode voltage control can now be applied to a differential filter and on to the next stage.
4. Make sure that the differential filter has only differential resistors and capacitors. Termination resistors to ground level-shift the input common-mode voltage, while differential resistors transfer V_{MID_OUT} directly through the filter as a common-mode input to the mixer.
5. If the desired V_{MID_OUT} + differential signal combined clips in the OPS or D2S, offset the supplies to gain headroom. For instance, if a 5 V output common-mode voltage is required with a 10 V_{PP} differential signal, the OPS and D2S must deliver 2.5 V to 7.5 V output swings. The D2S has the higher headroom requirement at 1.5 V (maximum). Operating the THS3215 with –5 V and 10 V supplies stays within the rated maximum of 15.8 V total supply range, and provide adequate headroom for the positive offset swing requirement. Note that the logic lines are still referenced to GND by pin 7. Tie PATHSEL (pin 4) to $+V_{CC}$ to hold this design in the external path mode required.

10 Power Supply Recommendations

The THS3215 typically operates on balanced, split supplies. The specifications and characterization plots use ±6 V in most cases. The full operating range for the THS3215 spans ±4 V to ±7.9 V. The input and output stages have separate supply pins that are isolated internally.

The recommended external supply configuration brings $\pm V_{CC}$ into the output stage first, then back to the input stage connections through a π-filter comprised of ferrite beads and added decoupling capacitors at +VCC2 (pin 16) and –VCC2 (pin 5). 図 10-1 shows an example decoupling configuration. This same circuit configuration was used to characterize the D2S + OPS performance in Frequency Response vs Output Voltage to HD3 vs Supply Voltage.

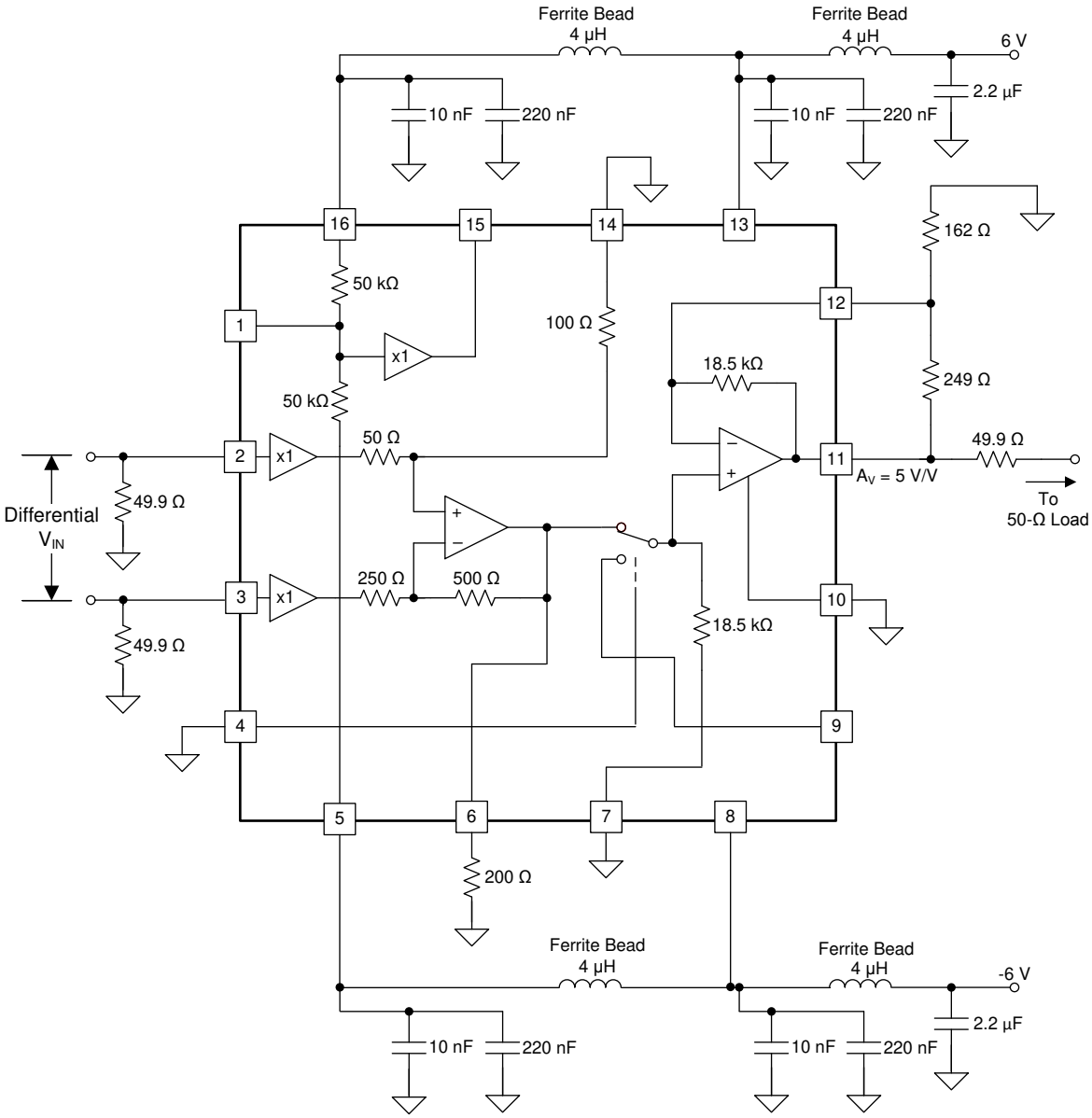


図 10-1. Recommended Power-Supply Configuration

The ferrite bead acts to break the feedback loop from the output stage load currents that re-enter the D2S and midscale buffer stages. Operate the two positive supply pins and the two negative supply pins at the same voltage. Using separate sources on the two pins risks forward-biasing the on-chip parallel diodes that connect the two supply inputs together. +VCC1 (pin 13) and +VCC2 (pin 16) have two parallel diodes that are off if the voltage at the two pins are equal. The same is true for –VCC1 (pin 8) and –VCC2 (pin 5).

The THS3215 provides considerable flexibility in the supply voltage settings. The overriding consideration is always satisfying the required headroom to the supplies on all the I/O paths. The logic controls on PATHSEL (pin 4) and DISABLE (pin 10) are intended to operate ground referenced regardless of supplies used. The ground connection on pin 7 is used to set the reference.

Power savings are certainly possible by operating with only the minimum required supplies for the intended swings at each of the pins. For instance, consider an example design operating with a current-sinking DAC with the input common-mode voltage at 3 V, with an output swing at the D2S output of ±1 V. Looking at just the D2S under these conditions, the minimum positive supply is 3 V_{CM} + the maximum input headroom of 1.5 V to the positive supply + the input signal swing of 0.25 V, resulting in a minimum 4.75 V supply for this operation. The ±1 V output at VO1 (pin 6) along with the D2S output headroom sets the minimum negative supply voltage. The maximum 1.5 V headroom gives a possible minimum negative supply of –2.75 V. However, the minimum operating total of 8 V increases the negative supply to –3.5 V.

If the ±1 V swing is then amplified by the OPS, the output swing and headroom requirements set the minimum operating supply. For instance, if the OPS is operating at a gain of 2.5 V/V, the ±2.5 V output requires a maximum headroom of 1.6 V to either supply. Achieving a 1.6 V headroom requires a minimum balanced supply of ±4.1 V. However, the input stage overrides the positive side because the required minimum is 4.75 V, while the negative increases to –4.1 V. This example of absolute minimum supplies saves power. Using a typical 35-mA quiescent current for all stages, going to the minimum 8.5 V total across the device, uses 310 mW of quiescent power versus the 420 mW if a simple ±6 V supply is applied. However, ac performance degrades with the lower headroom. For more power-sensitive applications, consider adjusting the supplies to the minimum required on each side.

10.1 Thermal Considerations

The internal power for the THS3215 is a combination of its quiescent power and load power. The quiescent power is simply the total supply voltage times the supply current. This current is trimmed to reduce power dissipation variation and minimize variations in the ac performance. At a ±7.5 V supply, the maximum supply current of 36.5 mA dissipates 548 mW of quiescent power. The worst-case load power occurs if the output is at ½ the single-sided supply voltage driving a dc load. Placing a ±3.75 V dc output into 100 Ω adds another 37.5 mA × 3.75 V = 140 mW of internal power. This total of approximately 688 mW of internal dissipation requires the thermal pad be connected to a good heat-spreading ground plane to hold the internal junction temperatures below the rated maximum of 150°C.

The thermal impedance is approximately 45 °C/W with the thermal pad connected. For 688 mW of internal power dissipation there is a 31°C (approximate) rise in the junction temperature from ambient. Designing for the intended 85°C maximum ambient temperature results in a maximum junction temperature of 116°C.

11 Layout

11.1 Layout Guidelines

High-speed amplifier designs require careful attention to board layout in order to achieve the performance specified in the data sheets. Poor layout techniques can lead to increased parasitics from the board and external components resulting in suboptimal performance, and also instability in the form of oscillations. The THS3215 evaluation module (EVM) serves as a good reference for proper, high-speed layout methodology. The EVM includes numerous extra elements needed for lab characterization, and also additional features that are useful in certain applications. These additional components can be eliminated on the end system if not required by the application. General suggestions for the design and layout of high-speed, signal-path solutions include:

1. Minimize parasitic capacitance to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and input pins can cause instability. To reduce unwanted capacitance, open a window around the signal I/O pins on all of the ground and power planes around those pins. On other areas of the board, continuous ground and power planes are preferred for signal routing, with matched impedance traces for longer runs.
2. Use high-quality, high-frequency decoupling capacitors (0.1 µF) on the ground plane at the device power pins. Higher value capacitors (2.2 µF) are required, but can be placed further from the device power pins and shared among devices. For best high-frequency decoupling, consider X2Y supply-decoupling capacitors that offer a much higher self-resonance frequency over standard capacitors. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. Follow the power-supply guidelines recommended in the *セクション 10* section.
3. Careful selection and placement of external components preserve the high-frequency performance of the THS3215. Use low-reactance type resistors. Surface-mount resistors work best, and allow a tighter overall layout. Keep the printed circuit board (PCB) trace length as short as possible. Never use wire-bound type resistors in a high-frequency application. The output pin and inverting input pins are the most sensitive to parasitic capacitance; therefore, always position the feedback and series output resistors, if any, as close as possible to the inverting input pins and output pins. Place other network components, such as input termination resistors, close to the gain-setting resistors.
4. When using differential signal routing over any appreciable distance, use microstrip layout techniques with matched impedance traces. On differential lines, like those on the D2S inputs, match the routing in order to minimize common-mode noise effects and improve HD2 performance.
5. The input summing junction of the OPS is very sensitive to parasitic capacitance. Connect the R_G element into the summing junction with minimal trace length to the device-pin side of the resistor. The other side of R_G can have more trace length to source or ground, if needed; however, a very-short, low-inductance connection is preferred. For best results, do not socket a high-speed device such as the THS3215. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network that makes it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the THS3215 directly onto the board.

11.2 Layout Example

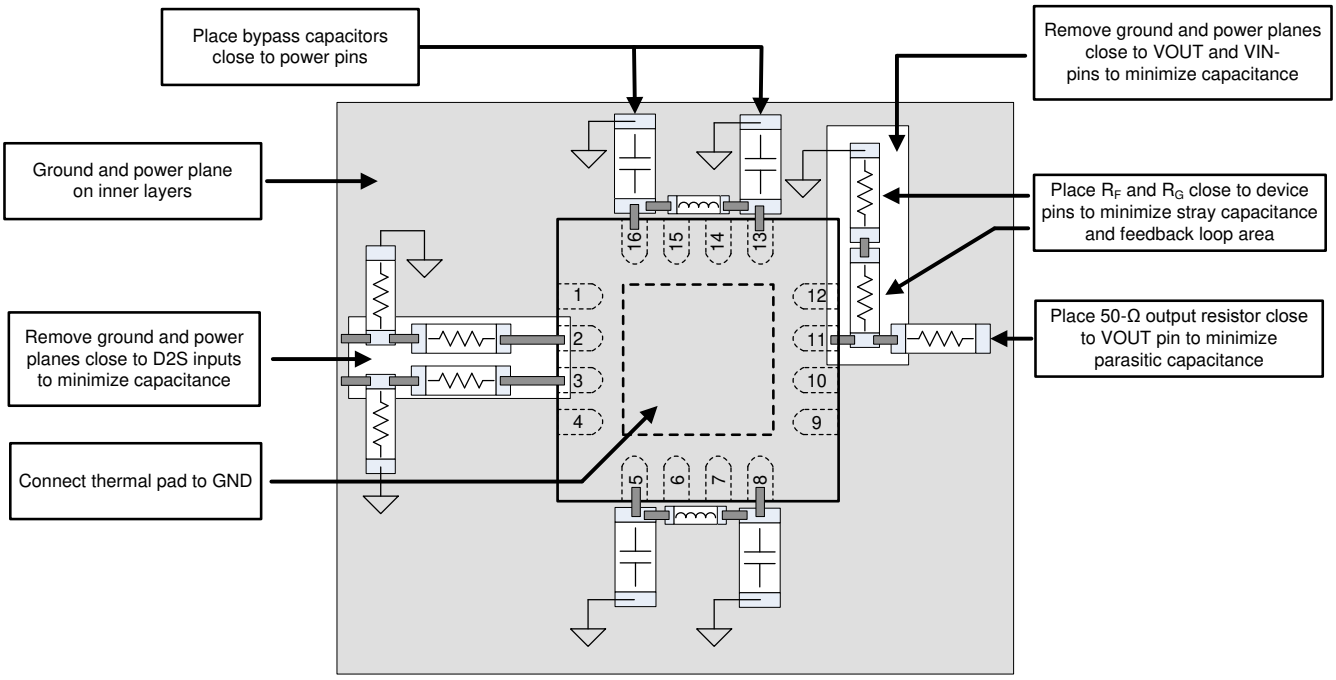


図 11-1. Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

The THS3215 TINA model is available on the THS3215 product folder, under the *Tools and software* tab. After downloading, open the model, right-click on a model symbol, and select *Enter Macro* to see the list of modeled parameters.

Note

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *OPA695 Ultra-Wideband, Current-Feedback Operational Amplifier With Disable* data sheet
- Texas Instruments, *THS3215EVM and THS3217EVM* user's guide
- Texas Instruments, *Voltage Feedback Vs Current Feedback Op Amps* application report
- Texas Instruments, *Current Feedback Amplifier Analysis and Compensation* application report
- Texas Instruments, *Current Feedback Amplifiers: Review, Stability Analysis, and Applications* application note
- Texas Instruments, *Stabilizing Current-Feedback Op Amps While Optimizing Circuit Performance* application report

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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12.5 Trademarks

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12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THS3215IRGVR	Active	Production	VQFN (RGV) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS3215 IRGV
THS3215IRGVR.A	Active	Production	VQFN (RGV) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS3215 IRGV
THS3215IRGVT	Active	Production	VQFN (RGV) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS3215 IRGV
THS3215IRGVT.A	Active	Production	VQFN (RGV) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS3215 IRGV

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

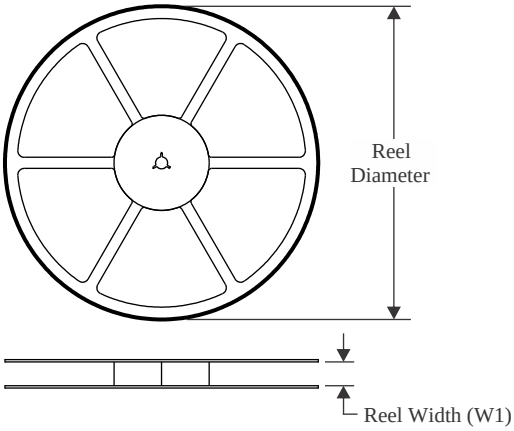
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

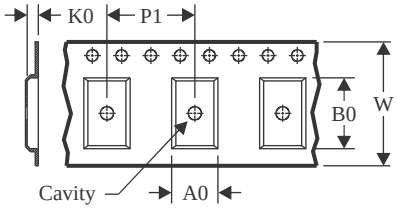
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

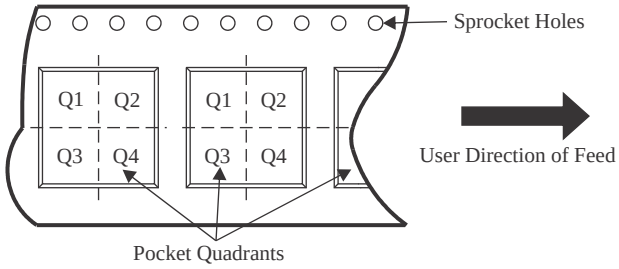


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

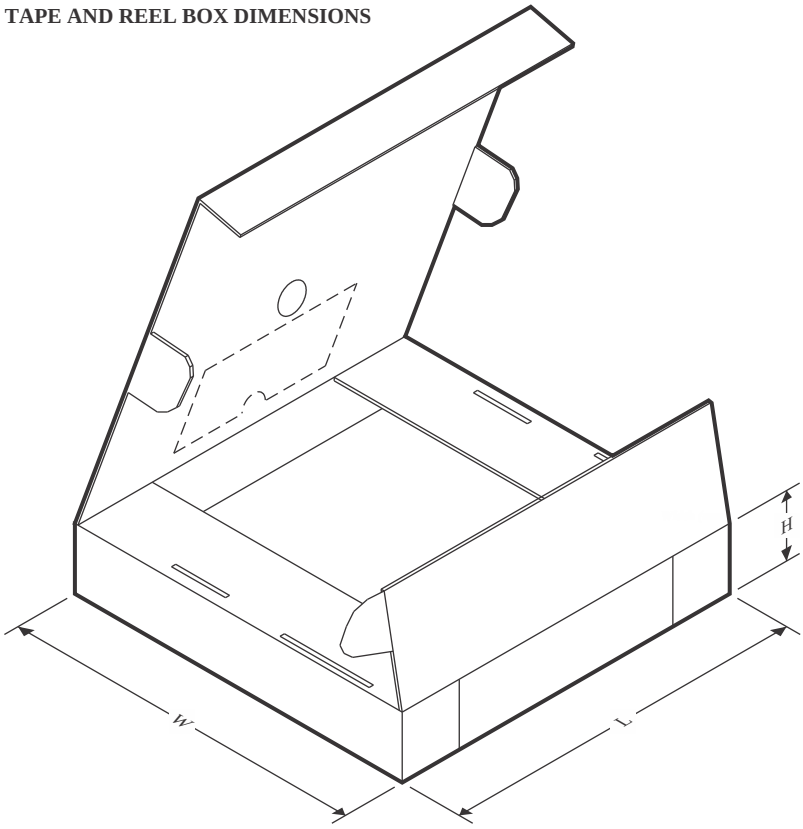
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS3215IRGVR	VQFN	RGV	16	2500	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
THS3215IRGVT	VQFN	RGV	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS3215IRGVR	VQFN	RGV	16	2500	346.0	346.0	33.0
THS3215IRGVT	VQFN	RGV	16	250	210.0	185.0	35.0

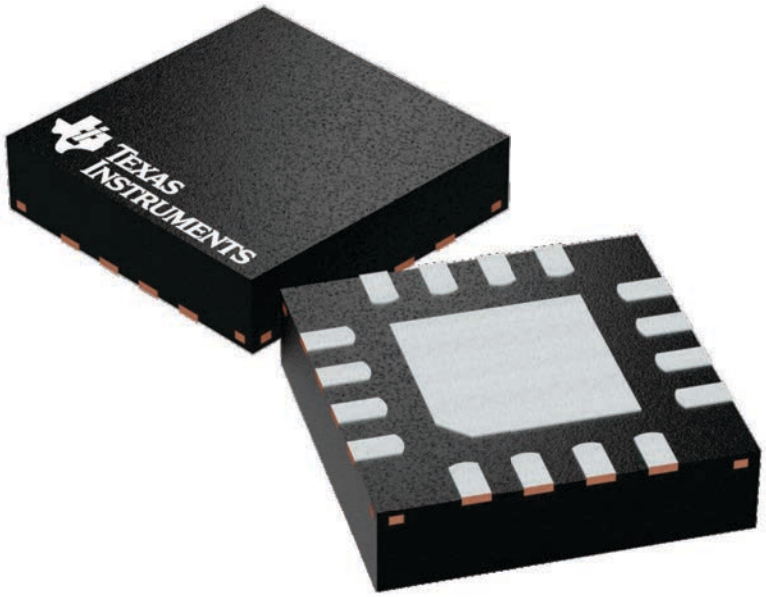
GENERIC PACKAGE VIEW

RGV 16

VQFN - 1 mm max height

4 x 4, 0.65 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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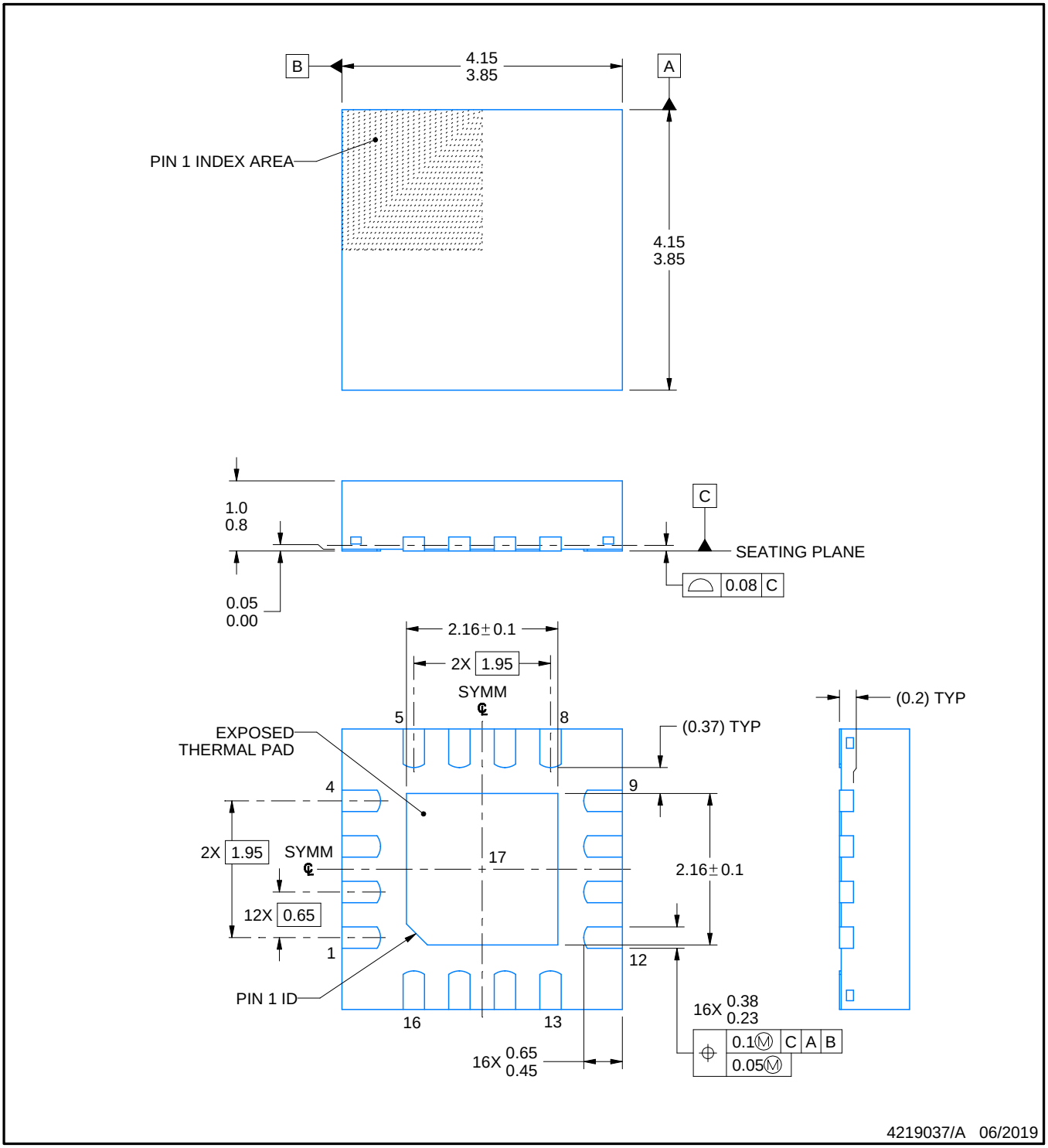
RGV0016A

PACKAGE OUTLINE

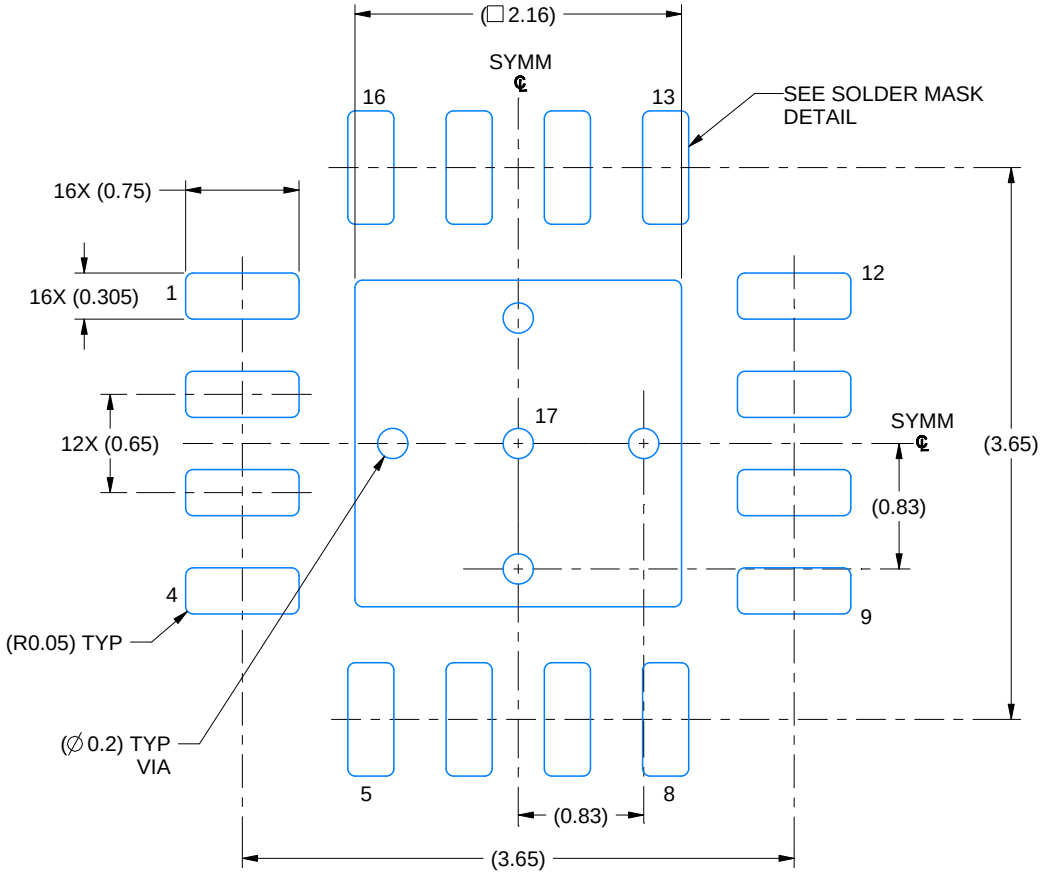
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

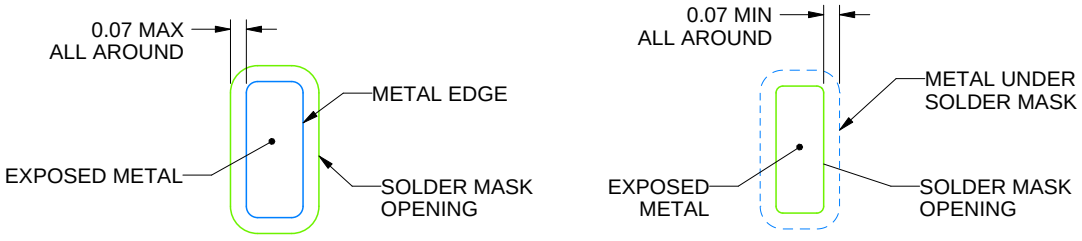


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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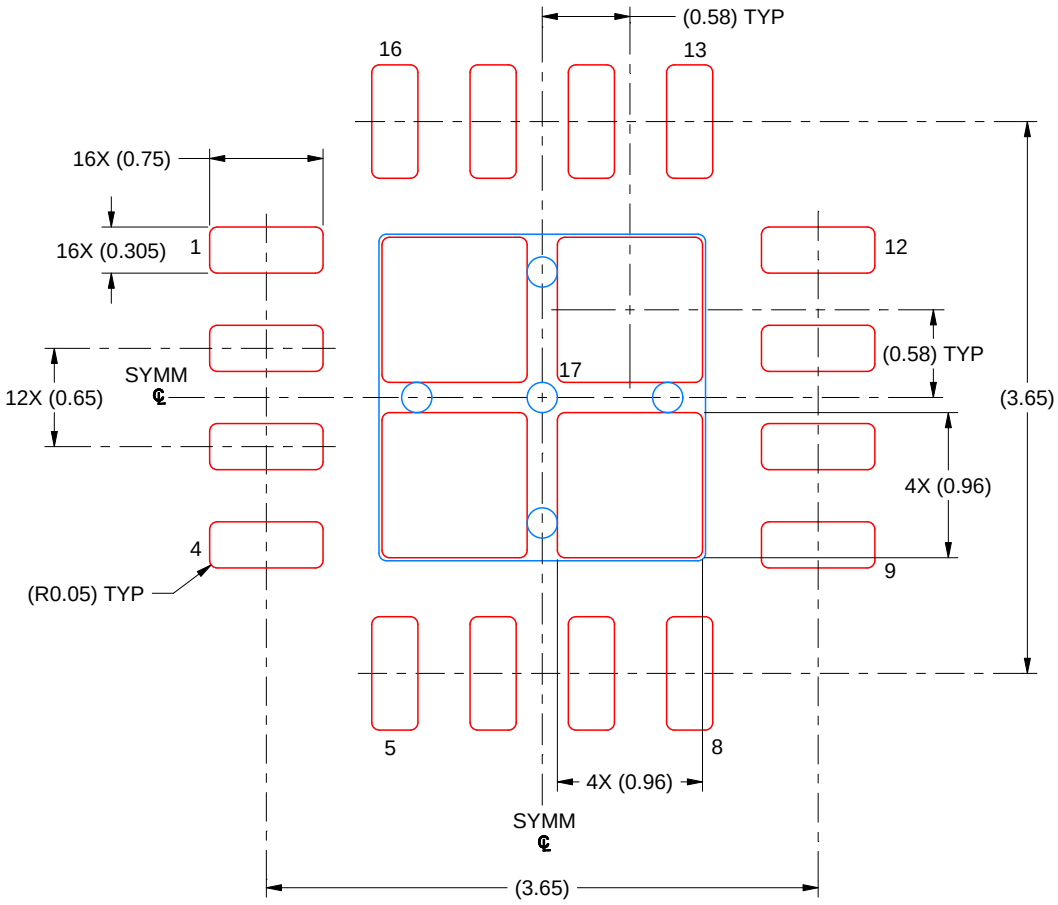
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 17
79% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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