

THVD1454 120Ω のスイッチ可能終端およびスルー・レート制御を内蔵した 3V~5.5V、半二重 RS-485 トランシーバ

1 特長

- TIA/EIA-485A 規格の要件を満たすか、それを上回る性能
- 3V~5.5V の電源電圧
- 5V 電源で 2.1V を超える差動出力により PROFIBUS に準拠
- 半二重 RS-422/RS-485
- ピンで制御されるオンチップ 120Ω 終端抵抗をバスのピン間に配置
- 最大データ・レートを構成可能
 - SLR = High: 500kbps
 - SLR = Low またはフローティング: 20Mbps
- バス I/O 保護
 - ±16kV HBM ESD
 - ±8kV IEC 61000-4-2 接触放電
 - ±15kV IEC 61000-4-2 エアギャップ放電
 - ±4kV IEC 61000-4-4 高速過渡バースト
 - ±16V のバス・フォルト保護 (バス・ピンの絶対最大電圧)
- 工業用拡張温度範囲に対応: -40°C~125°C
- 低い消費電力
 - シャットダウン時消費電流: 5μA 未満
 - 動作中の静止電流: 3mA 未満
- グリッチなしの電源オン/オフによるホット・プラグイン機能
- 開放、短絡、アイドル・バスのフェイルセーフ
- 1/8 単位負荷 (最大 256 のバス・ノード)
- 小型で省スペースの熱効率の高い 10 ピン VSON パッケージ (3mm × 3mm)

2 アプリケーション

- ファクトリ・オートメーション / 制御
- ビル・オートメーション
- モーター・ドライブ
- PD (パワー・デリバリー)
- 産業用輸送
- HVAC システム
- スマート・メーター

3 概要

THVD1454 は、産業用アプリケーション向けのフレキシブルな半二重 RS-485 トランシーバです。このデバイスには、オンチップの 120Ω 終端抵抗や、ドライバ出力スルーレート制御などの機能があります。どちらの機能もピンで制御できます。これにより、このデバイスは、任意のネットワークで、どのようなノード位置 (終端ノードまたは中間ノード) でも、低速または高速で使用できます。最終製品の設計者は、共通のプリント基板 (PCB) を設計し、さまざまなアプリケーションの要求に合わせたソフトウェアで PCB を構成できるようになりました。これにより、顧客向けに設計と認定に必要な時間を短縮できます。

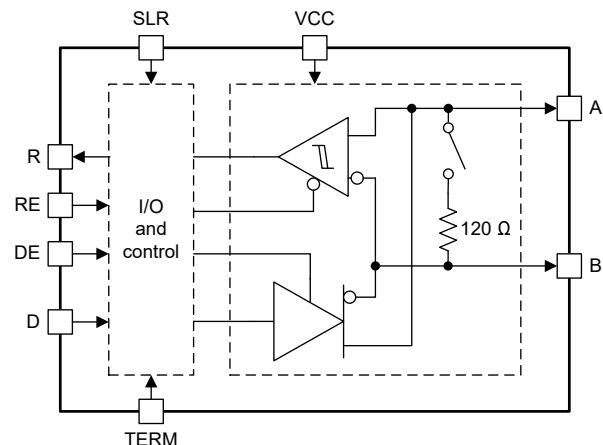
バスのピンは高レベルの IEC 接触放電 ESD への耐性があるため、システム・レベルでの追加保護部品が不要になります。このデバイスは 3V~5.5V の単一電源で動作します。同相電圧範囲が広く、バスのピンでの入力レークが小さいため、このデバイスは長いケーブルを使用するマルチポイントのアプリケーションに適しています。

THVD1454 は、省スペースで熱効率の高い 10-VSON パッケージ (3mm × 3mm) で供給されます。このデバイスは、-40°C~125°C の周囲温度での動作が規定されています。

パッケージ情報

| 部品番号 | パッケージ (1) | パッケージ・サイズ (2) |
|----------|-----------|---------------|
| THVD1454 | VSON (10) | 3mm × 3mm |

- (1) 完全な部品番号については、このデータシートの末尾にある注文情報を参照してください。
- (2) パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



アプリケーション概略図



Table of Contents

| | | | |
|--|----|--|----|
| 1 特長 | 1 | 8.1 Overview..... | 14 |
| 2 アプリケーション | 1 | 8.2 Functional Block Diagrams..... | 14 |
| 3 概要 | 1 | 8.3 Feature Description..... | 14 |
| 4 Revision History | 2 | 8.4 Device Functional Modes..... | 14 |
| 5 Pin Configuration and Functions | 3 | 9 Application Information Disclaimer | 17 |
| 6 Specifications | 4 | 9.1 Application Information..... | 17 |
| 6.1 Absolute Maximum Ratings..... | 4 | 9.2 Typical Application..... | 17 |
| 6.2 ESD Ratings | 4 | 9.3 Power Supply Recommendations..... | 23 |
| 6.3 ESD Ratings [IEC]..... | 4 | 9.4 Layout..... | 23 |
| 6.4 Recommended Operating Conditions..... | 5 | 10 Device and Documentation Support | 24 |
| 6.5 Thermal Information..... | 5 | 10.1 Device Support..... | 24 |
| 6.6 Power Dissipation..... | 5 | 10.2 ドキュメントの更新通知を受け取る方法..... | 24 |
| 6.7 Electrical Characteristics..... | 6 | 10.3 サポート・リソース..... | 24 |
| 6.8 Switching Characteristics_500 kbps..... | 8 | 10.4 Trademarks..... | 24 |
| 6.9 Switching Characteristics_20 Mbps..... | 9 | 10.5 静電気放電に関する注意事項..... | 24 |
| 6.10 Switching Characteristics_Termination resistor..... | 9 | 10.6 用語集..... | 24 |
| 6.11 Typical Characteristics..... | 10 | 11 Mechanical, Packaging, and Orderable Information | 24 |
| 7 Parameter Measurement Information | 12 | | |
| 8 Detailed Description | 14 | | |

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| Changes from Revision * (January 2023) to Revision A (July 2023) | Page |
|---|-------------|
| • データシートのステータスを「事前情報」から「量産データ」に変更 | 1 |

5 Pin Configuration and Functions

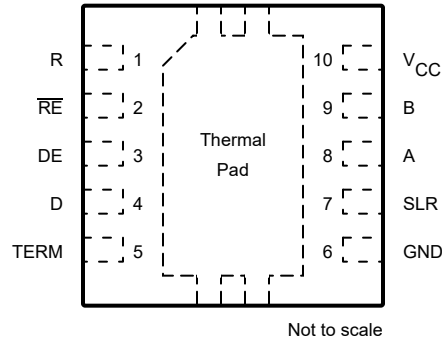


图 5-1. VSON (DRC) Package, 10-Pins (Top View)

表 5-1. Pin Functions

| PIN | | TYPE | DESCRIPTION |
|-----------------|-----|------------------|--|
| NAME | NO. | | |
| R | 1 | Digital output | Logic output RS-485 data |
| RE | 2 | Digital input | Receiver enable/disable. Internal pull-up. Receiver disabled by default |
| DE | 3 | Digital input | Driver enable/disable. Internal pull-down. Driver disabled by default |
| D | 4 | Digital input | Logic input RS485 data. Internal pull-up. Drives the bus high by default if driver is enabled |
| TERM | 5 | Digital input | 120 Ω on-chip termination control for A/B pins. Internal pull-down. Termination across A/B is disabled by default |
| GND | 6 | GND | Ground |
| SLR | 7 | Digital input | Slew rate control. Internal pull-down, default 20 Mbps operation. Logic high SLR enables slow speed (500 kbps) |
| A | 8 | Bus input/output | RS-485 bus pin. This pin is non-inverting driver output or non-inverting receiver input |
| B | 9 | Bus input/output | RS-485 bus pin. This pin is inverting driver output or inverting receiver input |
| V _{CC} | 10 | Power | 3 V to 5.5 V supply |
| Thermal Pad | | -- | Connect to GND for optimal thermal and electrical performance |

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾ ⁽²⁾

| | | MIN | MAX | UNIT |
|--------------------------|---|------|-----|------|
| Supply voltage | V _{CC} | -0.5 | 7 | V |
| Bus voltage | Voltage at any bus pin (A or B) with respect to GND | -16 | 16 | V |
| Differential bus voltage | (A-B) or (B-A) with termination enabled | -6 | 6 | V |
| Input voltage | Range at any logic pin (D, DE, SLR, TERM, or RE) | -0.3 | 5.7 | V |
| Receiver output current | I _O | -24 | 24 | mA |
| Storage temperature | T _{stg} | -65 | 150 | °C |

- Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- All voltage values, except differential I/O bus voltages, are with respect to ground terminal.

6.2 ESD Ratings

| | | | VALUE | UNIT | |
|--------------------|-------------------------|--|---------------------------------------|---------|---|
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/ JEDEC JS-001 ⁽¹⁾ | Bus terminals (A, B) and GND | ±16,000 | V |
| | | | All pins except bus terminals and GND | ±4,000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±1,500 | V | |

- JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings [IEC]

| | | | | VALUE | UNIT |
|--------------------|--|--------------------------------------|-----------------------|---------|------|
| V _(ESD) | Electrostatic discharge, on chip termination ON or OFF | Contact discharge, per IEC 61000-4-2 | Bus terminals and GND | ±8,000 | V |
| | | Air-gap discharge, per IEC 61000-4-2 | Bus terminals and GND | ±15,000 | |
| V _(EFT) | Electrical fast transient | Per IEC 61000-4-4 | Bus terminals | ±4,000 | V |

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|-------------------------------|--|-----------------------|-----|-----|------|
| V _{CC} | Supply voltage | 3 | | 5.5 | V |
| V _I | Input voltage at any bus terminal (separately or common mode) ⁽¹⁾ | -7 | | 12 | V |
| V _{IH} | High-level input voltage (D, DE, RE, TERM, SLR inputs) | 2 | | 5.5 | V |
| V _{IL} | Low-level input voltage (D, DE, RE, TERM, SLR inputs) | 0 | | 0.8 | V |
| I _O | Output current, driver | -60 | | 60 | mA |
| I _{OR} | Output current, receiver | -8 | | 8 | mA |
| R _L | Differential load resistance | 54 | 60 | | Ω |
| 1/t _{UI} | Signaling rate | SLR = V _{IO} | | 500 | kbps |
| | | SLR = GND or floating | | 20 | Mbps |
| T _A ⁽²⁾ | Operating ambient temperature | -40 | | 125 | °C |
| T _J ⁽²⁾ | Junction temperature | -40 | | 150 | °C |

- (1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.
(2) Operation is specified for internal (junction) temperatures upto 150°C. Self-heating due to internal power dissipation should be considered for each application. Maximum junction temperature is internally limited by the thermal shut-down (TSD) circuit which disables the driver outputs when the junction temperature reaches typical 170°C.

6.5 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | THVD1454 | UNIT |
|-------------------------------|--|------------|------|
| | | DRC (VSON) | |
| | | 10 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 48.6 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 54 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 21.9 | °C/W |
| ψ _{JT} | Junction-to-top characterization parameter | 1.1 | °C/W |
| ψ _{JB} | Junction-to-board characterization parameter | 21.9 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | 6.7 | °C/W |

- (1) For more information about traditional and new thermalmetrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.6 Power Dissipation

| PARAMETER | | TEST CONDITIONS | | Typical | Max | UNIT | |
|----------------|---|---|---------|----------|-----|------|----|
| P _D | Driver and receiver enabled, V _{CC} = 5.5 V, T _A = 125 °C, D = square wave 50% duty | Unterminated, TERM = L | SLR = H | 500 kbps | 185 | 210 | mW |
| | | | SLR = L | 20Mbps | 310 | 340 | |
| | | TERM = H, With 120 Ω load between A/B inputs | SLR = H | 500 kbps | 316 | 360 | mW |
| | | | SLR = L | 20Mbps | 396 | 430 | |

6.7 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of $V_{CC} = 5\text{ V}$, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|---------------------------|---|--|-----------------------------|----------------|------|---------------|---------------|
| Driver | | | | | | | |
| $ V_{OD} $ | Driver differential output voltage magnitude | $R_L = 60\ \Omega, -7\text{ V} \leq V_{\text{test}} \leq 12\text{ V}$ (See 7-1) | 1.5 | 3.3 | | V | |
| | | $R_L = 60\ \Omega, -7\text{ V} \leq V_{\text{test}} \leq 12\text{ V}, 4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ (See 7-1) | 2.1 | 3.3 | | V | |
| | | $R_L = 100\ \Omega$ (See 7-2) | 2 | 4 | | V | |
| | | $R_L = 54\ \Omega, 4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ (See 7-2) | 2.1 | 3.3 | | V | |
| | | $R_L = 54\ \Omega$ (See 7-2) | 1.5 | 3.3 | | V | |
| $\Delta V_{OD} $ | Change in magnitude of differential output voltage | $R_L = 54\ \Omega$ or $100\ \Omega$ (See 7-2) | -50 | | 50 | mV | |
| V_{OC} | Common-mode output voltage | $R_L = 54\ \Omega$ or $100\ \Omega$ (See 7-2) | | $V_{CC}/2$ | 3 | V | |
| $\Delta V_{OC(SS)}$ | Change in steady-state common-mode output voltage | $R_L = 54\ \Omega$ or $100\ \Omega$ (See 7-2) | -50 | | 50 | mV | |
| I_{OS} | Short-circuit output current | $DE = V_{IO}, -7\text{ V} \leq (V_A \text{ or } V_B) \leq 12\text{ V}$, or A shorted to B | -250 | | 250 | mA | |
| Receiver | | | | | | | |
| I_I | Bus input current (termination disabled) | $DE = 0\text{ V}, V_{CC} = 0\text{ V}$ or 5.5 V | $V_I = 12\text{ V}$ | 85 | 110 | μA | |
| | | | $V_I = -7\text{ V}$ | -100 | -70 | μA | |
| I_{RXT} | Receiver bus input leakage current with termination enabled | $DE = 0\text{ V}, V_{CC} = 5.5\text{ V}, \text{TERM} = V_{CC}$ | $V_I = -7$ to 12 V | | -300 | 300 | μA |
| V_{TH+} | Positive-going input threshold voltage ⁽¹⁾ | Over common-mode range of -7 V to 12 V | | -85 | -45 | mV | |
| V_{TH-} | Negative-going input threshold voltage ⁽¹⁾ | | -200 | -150 | mV | | |
| V_{HYS} | Input hysteresis | | 30 | 50 | mV | | |
| $C_{A,B}$ | Input differential capacitance | Measured between A and B, $f = 1\text{ MHz}$ | | 20 | | pF | |
| V_{OH} | Output high voltage | $I_{OH} = -8\text{ mA}$ | $V_{CC} - 0.4$ | $V_{CC} - 0.2$ | | V | |
| V_{OL} | Output low voltage | $I_{OL} = 8\text{ mA}$ | | 0.2 | 0.4 | V | |
| I_{OZ} | Output high-impedance current, R pin | $V_O = 0\text{ V}$ or $V_{CC}, RE = V_{CC}$ | -2 | | 2 | μA | |
| Logic | | | | | | | |
| I_{IN} | Input current (D, RE, DE, SLR, TERM) | $3\text{ V} \leq V_{CC} \leq 5.5\text{ V}, 0\text{ V} \leq V_{IN} \leq V_{CC}$ | -5 | | 5 | μA | |
| Thermal Protection | | | | | | | |
| T_{SHDN} | Thermal shutdown threshold | Temperature rising | 150 | 170 | | °C | |
| T_{HYS} | Thermal shutdown hysteresis | | | 15 | | °C | |
| Supply | | | | | | | |
| UV_{VCC} (rising) | Rising under-voltage threshold on V_{CC} | | | 2.5 | 2.7 | V | |
| UV_{VCC} (falling) | Falling under-voltage threshold on V_{CC} | | 2 | 2.1 | | V | |
| $UV_{VCC(hys)}$ | Hysteresis on under-voltage of V_{CC} | | | 400 | | mV | |

6.7 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of $V_{CC} = 5\text{ V}$, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------------|---|---|---|-----|-----|---------------|
| I_{CC} | Supply current (quiescent), $V_{CC} = 4.5\text{ V to }5.5\text{ V}$, TERM = Floating or low, SLR = X | Driver and receiver enabled | $\overline{RE} = 0\text{ V}$, $DE = V_{CC}$, No load | 1.5 | 3 | mA |
| | | Driver enabled, receiver disabled | $\overline{RE} = V_{CC}$, $DE = V_{CC}$, No load | 1.3 | 2.5 | mA |
| | | Driver disabled, receiver enabled | $\overline{RE} = 0\text{ V}$, $DE = 0\text{ V}$, No load | 0.8 | 1.2 | mA |
| | | Driver and receiver disabled | $\overline{RE} = V_{CC}$, $DE = 0\text{ V}$, D = open, No load | 0.2 | 8 | μA |
| I_{CC} | Supply current (quiescent), $V_{CC} = 3\text{ V to }3.6\text{ V}$, TERM = Floating or low, SLR = X | Driver and receiver enabled | $\overline{RE} = 0\text{ V}$, $DE = V_{CC}$, No load | 1.4 | 2 | mA |
| | | Driver enabled, receiver disabled | $\overline{RE} = V_{CC}$, $DE = V_{CC}$, No load | 1 | 1.5 | mA |
| | | Driver disabled, receiver enabled | $\overline{RE} = 0\text{ V}$, $DE = 0\text{ V}$, No load | 0.7 | 1 | mA |
| | | Driver and receiver disabled | $\overline{RE} = V_{CC}$, $DE = 0\text{ V}$, D = open, No load | 0.2 | 8 | μA |
| I_{CCDT} | Supply current in driver termination mode | Driver enabled, receiver disabled with termination ON | $\overline{RE} = V_{CC}$, $DE = V_{IO}$, TERM = V_{CC} | 39 | 48 | mA |
| I_{CCRT} | Supply current in receiver termination mode | Receiver enabled and driver disabled, with termination ON | $\overline{RE} = \text{GND}$, $DE = 0\text{ V}$, TERM = V_{CC} | 1 | 1.3 | mA |
| I_{CCT} | Supply current in device disabled, termination enabled mode | Driver and Receiver disabled, termination ON | $\overline{RE} = V_{CC}$, $DE = 0\text{ V}$, TERM = V_{CC} | 200 | 350 | μA |
| On-Chip termination resistor | | | | | | |
| R_{TERM} | 120 Ω termination across receiver output A/B terminals | $DE = \text{GND}$, TERM = V_{CC} , $V_{AB} = 2\text{ V}$, $V_B = -7\text{ V}$, 0 V , 10 V See 7-9 | 102 | 120 | 138 | Ω |

(1) $V_{\text{TH+}}$ is specified to be at least V_{HYS} higher than $V_{\text{TH-}}$.

6.8 Switching Characteristics_500 kbps

500-kbps (with $SLR = V_{CC}$) over recommended operating conditions. All typical values are at 25°C and supply voltage of $V_{CC} = 5\text{ V}$, unless otherwise noted. ⁽¹⁾

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|--------------------------|------------------------------------|--|--|-------------------------|------|------|---------------|
| Driver | | | | | | | |
| t_r, t_f | Differential output rise/fall time | $R_L = 54\ \Omega, C_L = 50\ \text{pF}$ See 7-3 | $V_{CC} = 3\text{ to }3.6\text{ V}$, Typical at 3.3V | 200 | 250 | 600 | ns |
| | | | $V_{CC} = 4.5\text{ to }5.5\text{ V}$, Typical at 5 V | 220 | 270 | 600 | ns |
| t_{PHL}, t_{PLH} | Propagation delay | | $V_{CC} = 3\text{ to }3.6\text{ V}$, Typical at 3.3V | | 260 | 500 | ns |
| | | | $V_{CC} = 4.5\text{ to }5.5\text{ V}$, Typical at 5 V | | 260 | 450 | ns |
| $t_{SK(P)}$ | Pulse skew, $ t_{PHL} - t_{PLH} $ | | $V_{CC} = 3\text{ to }3.6\text{ V}$, Typical at 3.3V | | 2 | 15 | ns |
| | | | $V_{CC} = 4.5\text{ to }5.5\text{ V}$, Typical at 5 V | | 2 | 15 | ns |
| t_{PHZ}, t_{PLZ} | Disable time | $\overline{RE} = X$ | | | 80 | 200 | ns |
| t_{PZH}, t_{PZL} | Enable time | $\overline{RE} = 0\text{ V}$ | See 7-4 and 7-5 | | 200 | 650 | ns |
| | | $\overline{RE} = V_{CC}$ | | | 6 | 11 | μs |
| Receiver | | | | | | | |
| t_r, t_f | Output rise/fall time | $C_L = 15\ \text{pF}$ | See 7-6 | | 5 | 20 | ns |
| t_{PHL}, t_{PLH} | Propagation delay | | | | 620 | 1200 | ns |
| $t_{SK(P)}$ | Pulse skew, $ t_{PHL} - t_{PLH} $ | | | | 10 | 40 | ns |
| t_{PHZ}, t_{PLZ} | Disable time | $DE = X$ | See 7-7 | | 20 | 60 | ns |
| $t_{PZH(1)}$ | Enable time | $DE = V_{CC}$ | | 80 | 155 | ns | |
| $t_{PZL(1)}$ | Enable time | $DE = V_{CC}$ | | 650 | 1250 | ns | |
| $t_{PZH(2)}, t_{PZL(2)}$ | Enable time | $DE = 0\text{ V}$ | | See 7-8 | 7 | 12 | μs |

(1) A, B are RX input, Y/Z are driver output terminals in Full duplex mode

6.9 Switching Characteristics_20 Mbps

20-Mbps (SLR = GND) over recommended operating conditions. All typical values are at 25°C and supply voltage of $V_{CC} = 5$ V. (1)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|--------------------------|------------------------------------|---|---|-----|-----|---------------|------|
| Driver | | | | | | | |
| t_r, t_f | Differential output rise/fall time | $R_L = 54 \Omega, C_L = 50 \text{ pF}$ See 7-3 | $V_{CC} = 3 \text{ to } 3.6 \text{ V}$, Typical at 3.3 V | 5 | 9 | 15 | ns |
| | | | $V_{CC} = 4.5 \text{ to } 5.5 \text{ V}$, Typical at 5 V | 4.5 | 8 | 15 | ns |
| t_{PHL}, t_{PLH} | Propagation delay | | $V_{CC} = 3 \text{ to } 3.6 \text{ V}$, Typical at 3.3 V | 14 | 22 | 50 | ns |
| | | | $V_{CC} = 4.5 \text{ to } 5.5 \text{ V}$, Typical at 5 V | 9 | 20 | 40 | ns |
| $t_{SK(P)}$ | Pulse skew, $ t_{PHL} - t_{PLH} $ | | $V_{CC} = 3 \text{ to } 3.6 \text{ V}$, Typical at 3.3 V | | 1 | 3.5 | ns |
| | | | $V_{CC} = 4.5 \text{ to } 5.5 \text{ V}$, Typical at 5 V | | 1 | 3.5 | ns |
| t_{PHZ}, t_{PLZ} | Disable time | $\overline{RE} = X$ | | 25 | 50 | ns | |
| t_{PZH}, t_{PZL} | Enable time | $\overline{RE} = 0 \text{ V}$ | See 7-4 and 7-5 | 30 | 70 | ns | |
| | | $\overline{RE} = V_{CC}$ | | 6 | 11 | μs | |
| Receiver | | | | | | | |
| t_r, t_f | Output rise/fall time | $C_L = 15 \text{ pF}$ | See 7-6 | | 5 | 10 | ns |
| t_{PHL}, t_{PLH} | Propagation delay | | | | 30 | 72 | ns |
| $t_{SK(P)}$ | Pulse skew, $ t_{PHL} - t_{PLH} $ | | | | | 6 | ns |
| t_{PHZ}, t_{PLZ} | Disable time | $DE = X$ | See 7-7 | 20 | 58 | ns | |
| $t_{PZH(1)}, t_{PZL(1)}$ | Enable time | $DE = V_{CC}$ | | 80 | 155 | ns | |
| $t_{PZH(2)}, t_{PZL(2)}$ | Enable time | $DE = 0 \text{ V}$ | See 7-8 | 6 | 11 | μs | |

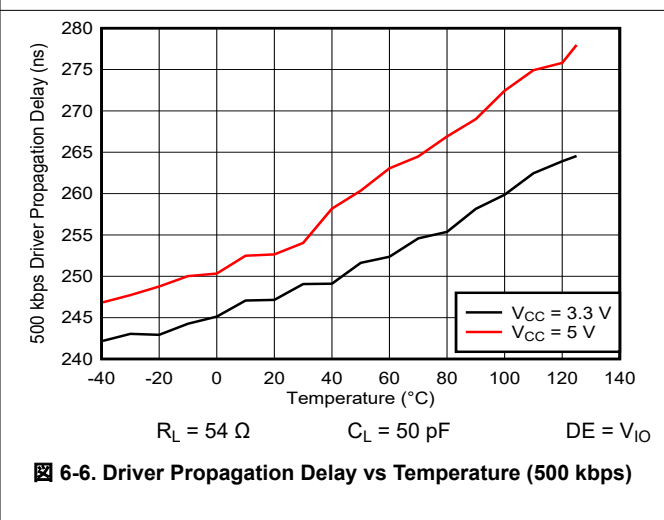
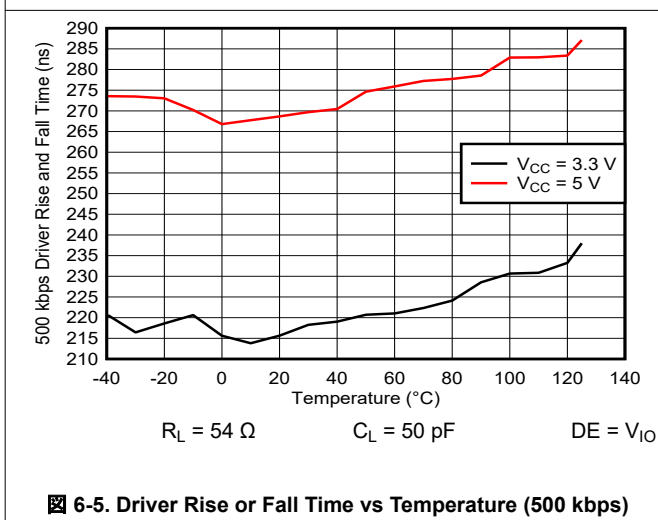
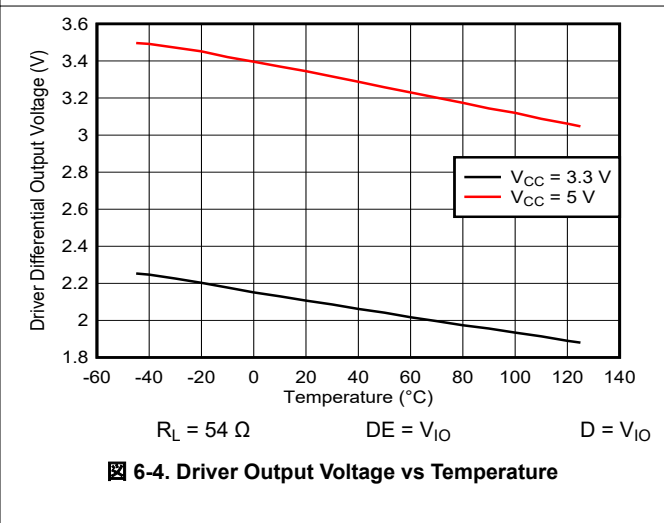
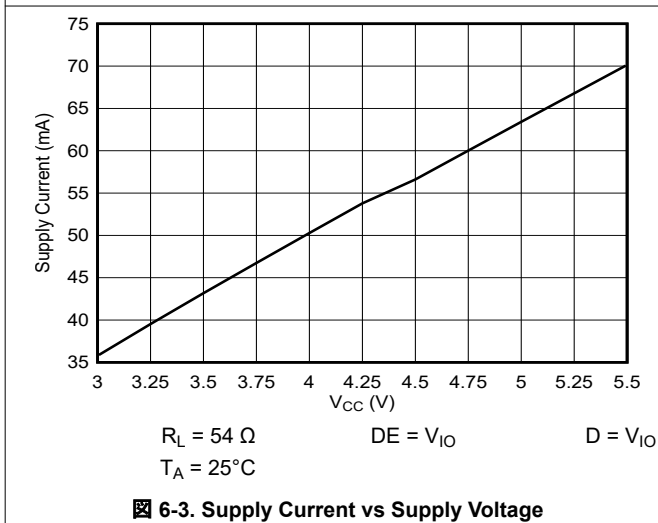
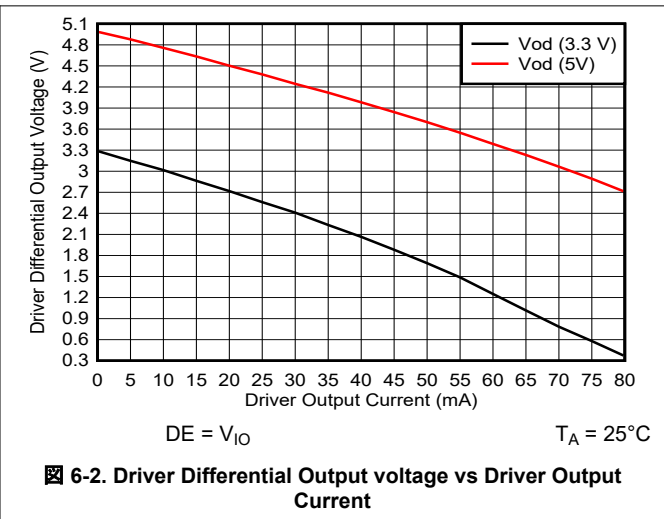
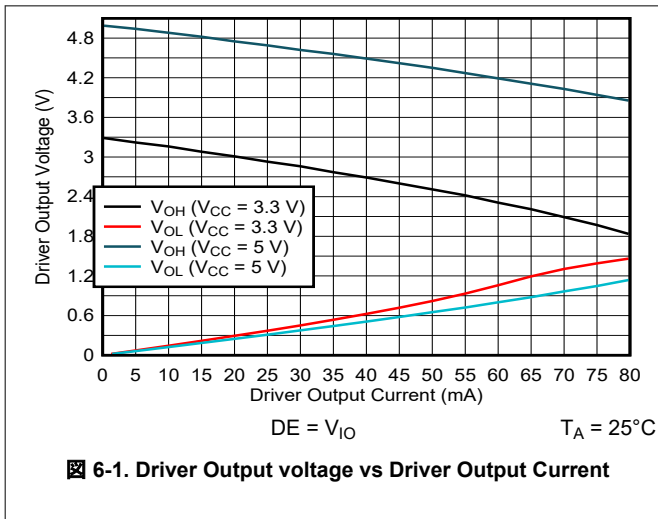
(1) A, B are RX input, Y/Z are driver output terminals in Full duplex mode.

6.10 Switching Characteristics_Termination resistor

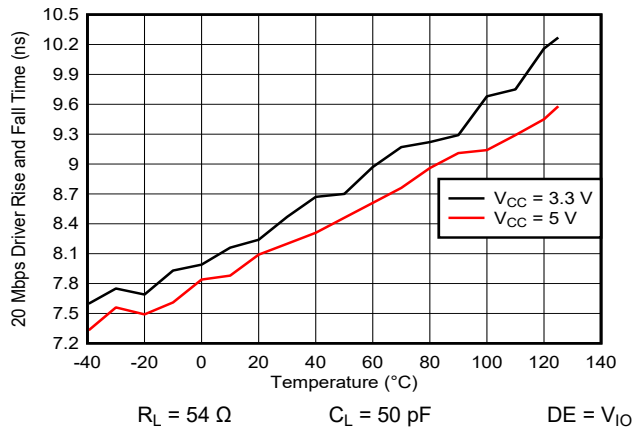
Parameters over recommended operating conditions. All typical values are at 25°C and supply voltage of $V_{CC} = 5 \text{ V}$, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|-----------|------------------------------------|---|--|-----|-----|-----|---------------|
| t_{TEN} | Termination resistor turn-on time | $\overline{RE} = V_{CC}, V_{AB} = 2 \text{ V}, V_B = 0 \text{ V}$; See 7-9 | | | 1.5 | 12 | μs |
| t_{TZ} | Termination resistor turn-off time | $\overline{RE} = V_{CC}, V_{AB} = 2 \text{ V}, V_B = 0 \text{ V}$; See 7-9 | | | 4.6 | 7.2 | μs |

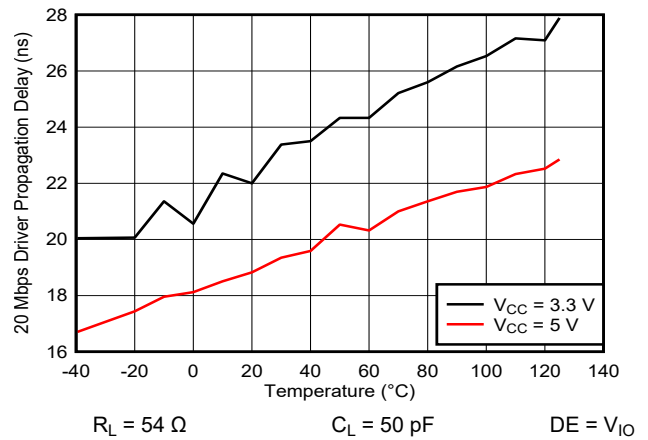
6.11 Typical Characteristics



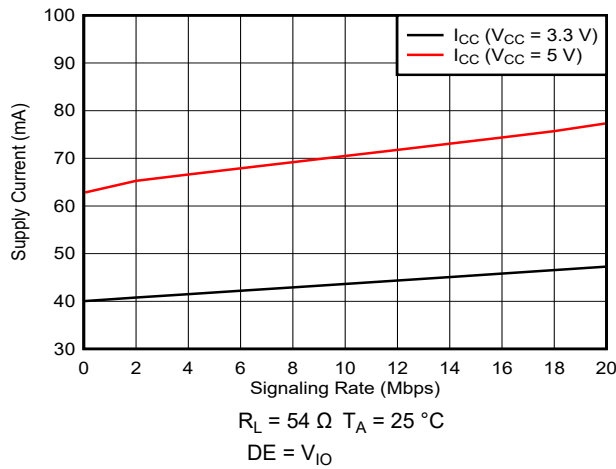
6.11 Typical Characteristics (continued)



6-7. Driver Rise or Fall Time vs Temperature (20 Mbps)

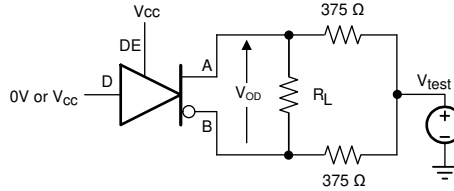


6-8. Driver Propagation Delay vs Temperature (20 Mbps)

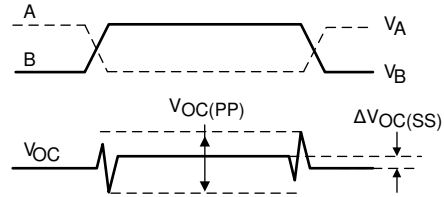
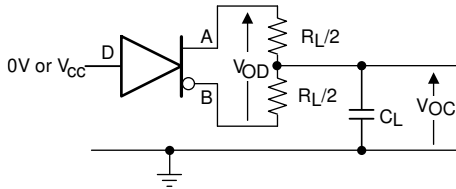


6-9. Supply Current vs Signal Rate (20 Mbps)

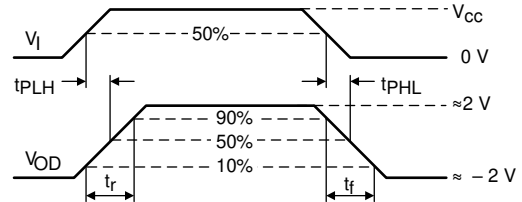
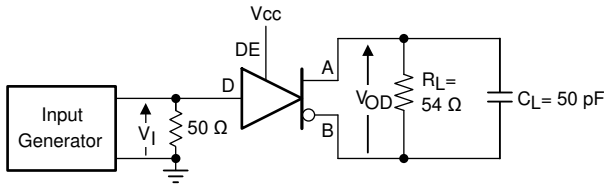
7 Parameter Measurement Information



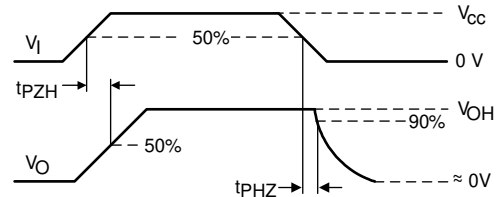
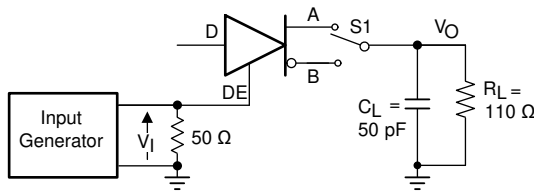
7-1. Measurement of Driver Differential Output Voltage With Common-Mode Load



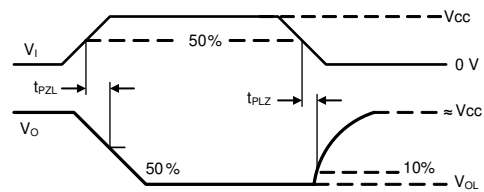
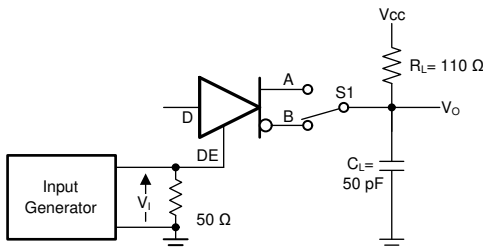
7-2. Measurement of Driver Differential and Common-Mode Output With RS-485 Load



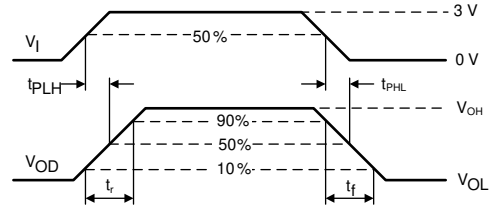
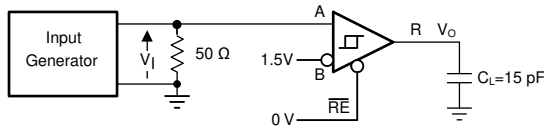
7-3. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays



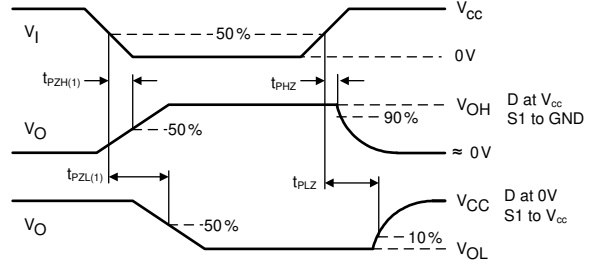
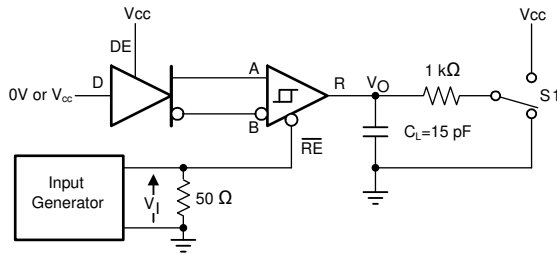
7-4. Measurement of Driver Enable and Disable Times With Active High Output and Pull-Down Load



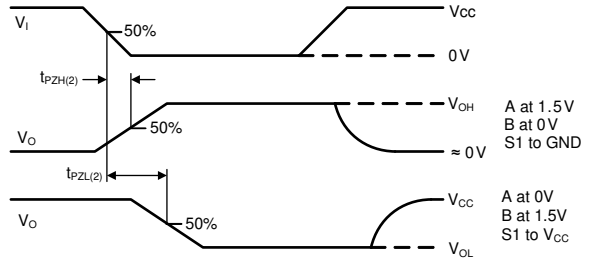
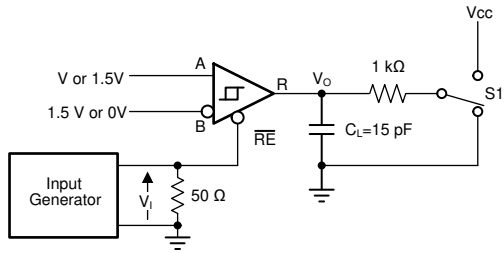
7-5. Measurement of Driver Enable and Disable Times With Active Low Output and Pull-up Load



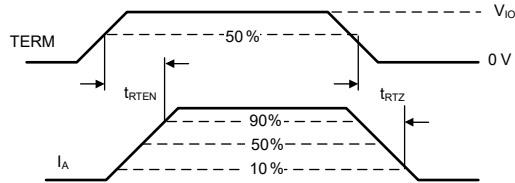
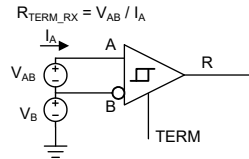
7-6. Measurement of Receiver Output Rise and Fall Times and Propagation Delays



7-7. Measurement of Receiver Enable/Disable Times With Driver Enabled



7-8. Measurement of Receiver Enable Times With Driver Disabled



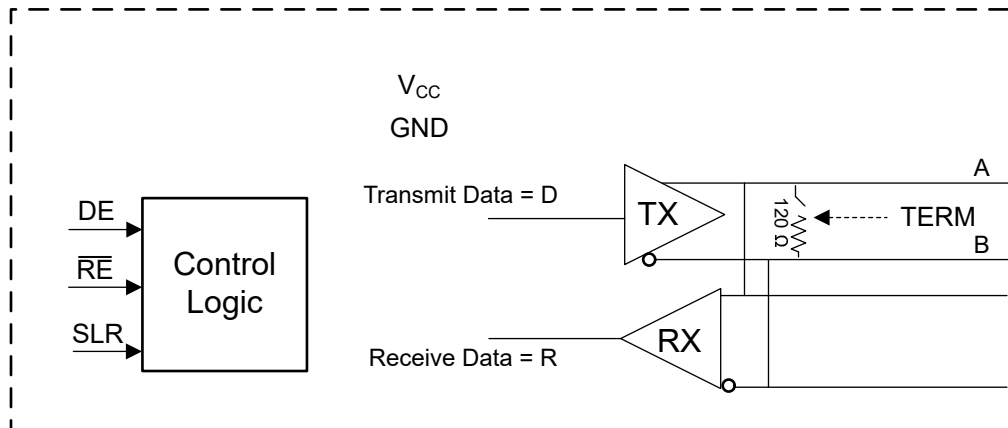
7-9. Measurement of enable and disable times of bus terminal termination resistor

8 Detailed Description

8.1 Overview

The THVD1454 is a flexible half duplex RS-485 transceiver. The device has slew rate control pin SLR which can be used to set the device in maximum 20 Mbps mode or slew rate limited 500 kbps mode. THVD1454 also has on-chip 120 Ω termination resistor across bus terminals A/B which is controlled using TERM pin.

8.2 Functional Block Diagrams



8.3 Feature Description

The THVD1454 operates from 3 V to 5.5 V bus supply. Internal ESD protection circuits on bus pins protect the transceiver against Electrostatic Discharges (ESD) according to IEC 61000-4-2 of up to ± 8 kV (Contact Discharge), ± 15 kV (Air Gap Discharge) and against electrical fast transients (EFT) according to IEC 61000-4-4 of up to ± 4 kV.

8.4 Device Functional Modes

When the driver enable pin, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this condition, the differential output voltage defined as $V_{OD} = V_A - V_B$ is positive. When D is low, the output states reverse, B turns high, A becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition, the logic state at D is irrelevant. The DE pin has an internal pull-down resistor to ground; thus, when left open, the driver is disabled (high-impedance) by default. The D pin has an internal pull-up resistor to V_{CC} , thus, when left open while the driver is enabled, output A turns high and B turns low.

表 8-1. Driver Function Table

| INPUT | ENABLE | OUTPUTS | | FUNCTION |
|-------|--------|---------|---|------------------------------------|
| | | A | B | |
| H | H | H | L | Actively drive bus high |
| L | H | L | H | Actively drive bus low |
| X | L | Z | Z | Driver disabled |
| X | OPEN | Z | Z | Driver disabled by default |
| OPEN | H | H | L | Actively drive bus high by default |

When the receiver enable pin, \overline{RE} , is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A - V_B$ is positive and higher than the positive input threshold, V_{TH+} , the receiver output, R, turns high. When V_{ID} is negative and lower than the negative input threshold, V_{TH-} , the receiver output, R, turns low. If V_{ID} is between V_{TH+} and V_{TH-} , the output is indeterminate.

When \overline{RE} is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go fail safe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

表 8-2. Receiver Function Table

| DIFFERENTIAL INPUT | ENABLE | OUTPUT | FUNCTION |
|------------------------------|-----------------|--------|------------------------------|
| $V_{ID} = V_A - V_B$ | \overline{RE} | R | |
| $V_{TH+} < V_{ID}$ | L | H | Receive valid bus high |
| $V_{TH-} < V_{ID} < V_{TH+}$ | L | ? | Indeterminate bus state |
| $V_{ID} < V_{TH-}$ | L | L | Receive valid bus low |
| X | H | Z | Receiver disabled |
| X | OPEN | Z | Receiver disabled by default |
| Open-circuit bus | L | H | Fail-safe high output |
| Short-circuit bus | L | H | Fail-safe high output |
| Idle (terminated) bus | L | H | Fail-safe high output |

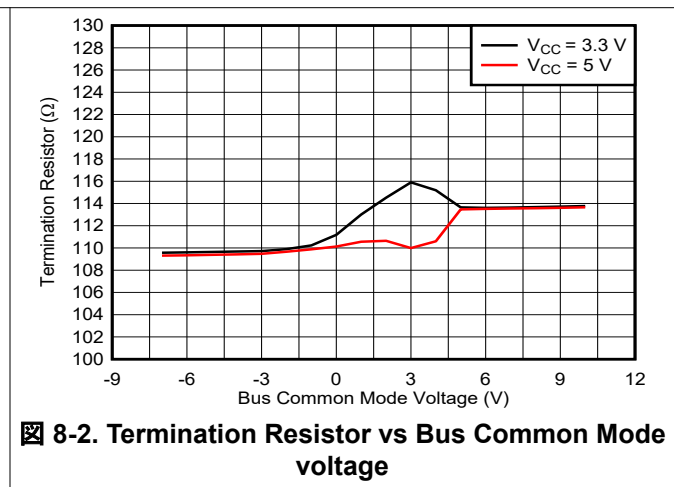
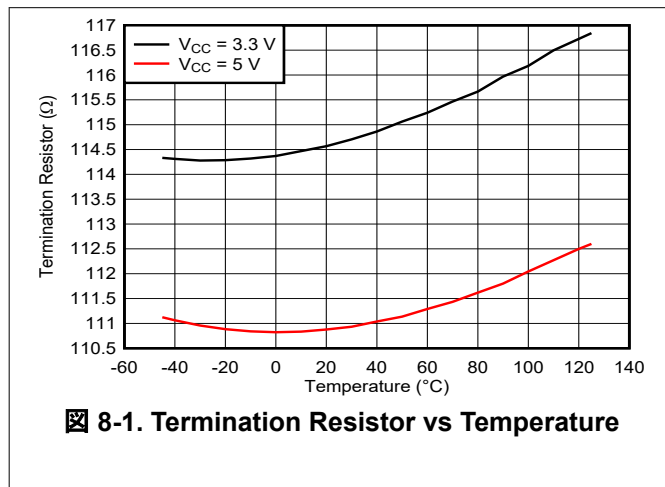
8.4.1 On-Chip Switchable Termination

THVD1454 has integrated termination resistor of nominal 120 Ω across A/B bus terminals. Termination resistor is enabled or disabled using the TERM pin described in 表 8-3.

表 8-3. On-chip termination function table

| Signal state | Function | Comments |
|------------------------|---------------------------------------|------------------------------------|
| TERM = V_{CC} | 120 Ω enabled between A and B | |
| TERM = GND or floating | 120 Ω disabled between A and B | Termination is disabled by default |

On-chip 120 Ω termination resistor variation with temperature and across common mode voltage is shown in 图 8-1 and 图 8-2.



THVD1454 on-chip termination resistor has been designed so the termination block offers a resistive load to the bus, and does not alter the magnitude or phase of the bus signals from DC to 20Mbps signaling. See 图 8-3 and 图 8-4 with the bus voltage swept from -6 V to +6 V. Current into the bus changes linearly in both conditions of termination ON or OFF.

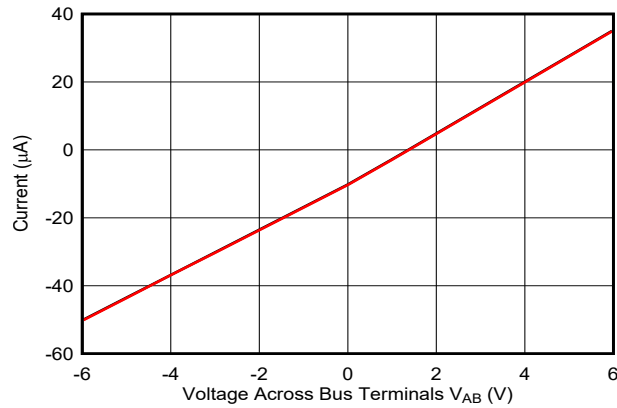


图 8-3. Voltage vs Current Across AB Bus Pins with Termination OFF

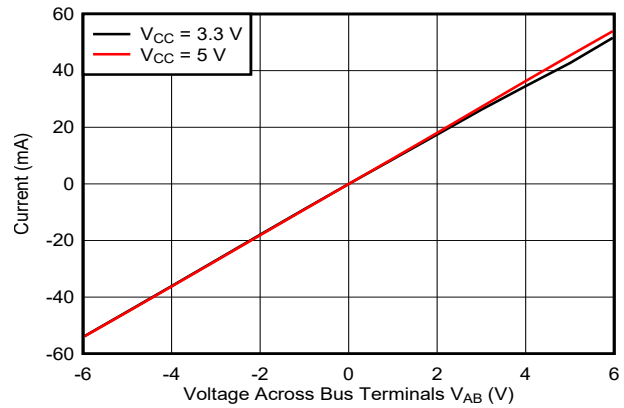


图 8-4. Voltage vs Current Across AB Bus Pins with Termination ON

8.4.2 Operational Data rate

THVD1454 can be used in slow speed or fast speed RS-485 networks by configuring Slew rate control (SLR) pin. 表 8-4 describes slew rate control function.

表 8-4. Slew rate control function table

| Signal state | Driver | Receiver | Comment |
|-----------------------|--------------------------------------|--------------------------------------|--|
| SLR = V_{CC} | Maximum speed of operation = 500kbps | Maximum speed of operation = 500kbps | Active high slew rate limiting applied on driver output and glitch filter in receiver path enabled |
| SLR = GND or floating | Maximum speed of operation = 20Mbps | Maximum speed of operation = 20Mbps | Slew rate limiting on driver output disabled and glitch filter in receiver path disabled |

Receiver path in the slow speed mode (500kbps) provides additional noise filtering. To attenuate noise frequency noise pulses from the bus which can be wrongly interpreted as valid data, SLR = V_{CC} enables a low pass filter to filter out pulses with frequency higher than typical 800 kHz.

8.4.3 Protection Features

THVD1454 has in-built protection features such as supply undervoltage, bus short circuit and thermal shutdown.

Supply undervoltage protection is present on V_{CC} supply. This maintains the bus output and receiver logic output in known driven state when the supply is above the rising undervoltage threshold. 表 8-5 describes the device behavior in various scenarios of supply levels.

表 8-5. Supply Function Table

| V_{CC} | Driver Output | Receiver Output | Termination across bus pins AB |
|------------------------------|-------------------------------|---------------------------------------|--------------------------------|
| > $UV_{VCC}(\text{rising})$ | Determined by DE and D inputs | Determined by \overline{RE} and A-B | Determined by TERM pin |
| < $UV_{VCC}(\text{falling})$ | High impedance | Undetermined | OFF |

Bus terminals are protected against high voltage short circuit events up to ± 16 V. Additionally, bus short circuit current is limited to 250 mA. In events like bus contention when multiple drivers are driving the bus simultaneously, the current through the bus terminals is internally limited. If the power dissipation makes the junction temperature cross 150°C , thermal shutdown is activated which disables the driver and receiver and reduces the on-chip power dissipation. The device is enabled once the junction temperature falls by the thermal shutdown hysteresis as specified in electrical parameter section of the data sheet.

9 Application Information Disclaimer

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The THVD1454 is a flexible RS-485 transceiver used for asynchronous data transmissions. The driver and receiver enable pins, slew rate control, and termination control pins allow the device to be applicable for various point-to-point, multipoint or multidrop network configurations.

9.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T , whose value matches the characteristic impedance, Z_0 , of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length. [Figure 9-1](#) shows two end nodes terminated, while remaining nodes unterminated. THVD1454 can be designed in all node designs. TERM pin allows configuring the nodes for end nodes and middle nodes in the network.

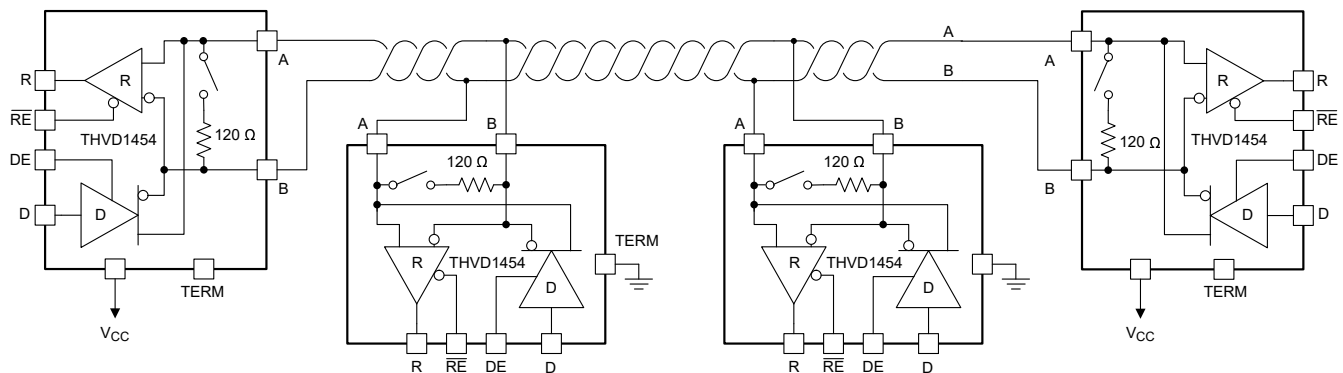


Figure 9-1. Typical Half Duplex RS-485 Network With all Nodes Using THVD1454

9.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

9.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the shorter the cable length; and conversely, the lower the data rate, the longer the cable length. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 300 kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5% or 10%.

9.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in 式 1.

$$L_{(\text{STUB})} \leq 0.1 \times t_r \times v \times c \quad (1)$$

where:

- t_r is the 10/90 rise time of the driver
- c is the speed of light (3×10^8 m/s)
- v is the signal velocity of the cable or trace as a factor of c

THVD1454 can be used in both slow speed and high speed networks with SLR pin configurability. Slew rate limiting makes the driver output rise or fall time slower so that stub lengths can be increased.

9.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to driver 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 kΩ. Because the THVD1454 consists of 1/8 UL transceivers, connecting up to 256 transceivers to the bus is possible.

9.2.1.4 Receiver Failsafe

The differential receiver of the THVD1454 is *failsafe* to invalid bus states caused by the following:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

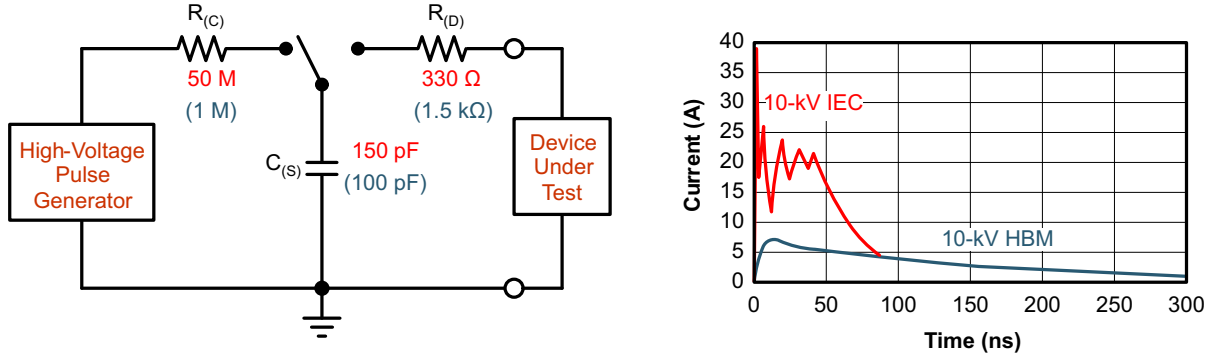
In any of these cases, the differential receiver outputs a failsafe logic high state so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds such that the *input indeterminate* range does not include zero volts differential. To comply with the RS-422 and RS-485 standards, the receiver output must output a high when the differential input V_{ID} is more positive than 200 mV, and must output a low when V_{ID} is more negative than -200 mV. The receiver parameters which determine the failsafe performance are V_{TH+} , V_{TH-} , and V_{HYS} (the separation between V_{TH+} and V_{TH-}). As shown in the 表 8-2, differential signals more negative than -200 mV always causes a low receiver output, and differential signals more positive than 200 mV always causes a high receiver output.

When the differential input signal is close to zero, it is still above the V_{TH+} threshold, and the receiver output is high. Only when the differential input is more than V_{HYS} below V_{TH+} does the receiver output transition to a low state. Therefore, the noise immunity of the receiver inputs during a bus fault conditions includes the receiver hysteresis value, V_{HYS} , as well as the value of V_{TH+} .

9.2.1.5 Transient Protection

The bus pins of the THVD1454 transceiver family include on-chip ESD protection against ± 16 -kV HBM and ± 8 -kV IEC 61000-4-2 contact discharge. The International Electrotechnical Commission (IEC) ESD test is far more severe than the HBM ESD test. The 50% higher charge capacitance, $C_{(S)}$, and 78% lower discharge resistance, $R_{(D)}$, of the IEC model produce significantly higher discharge currents than the HBM model.



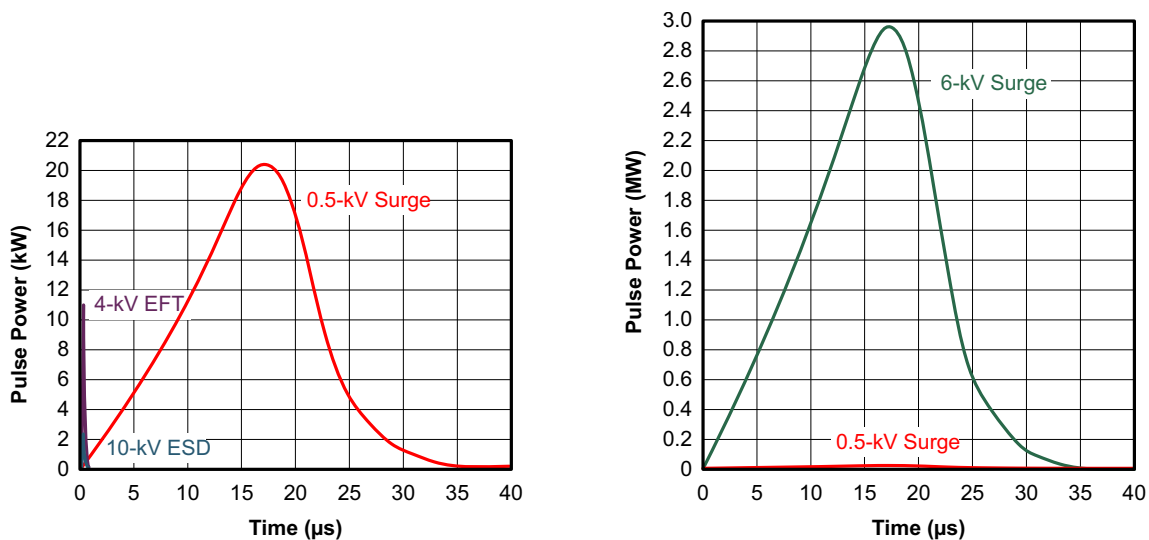
9-2. HBM and IEC ESD Models and Currents in Comparison (HBM Values in Parenthesis)

The on-chip implementation of IEC ESD protection significantly increases the robustness of equipment. Common discharge events occur because of human contact with connectors and cables. Designers may choose to implement protection against longer duration transients, typically referred to as surge transients.


EFTs are generally caused by relay-contact bounce or the interruption of inductive loads. Surge transients often result from lightning strikes (direct strike or an indirect strike which induce voltages and currents), or the switching of power systems, including load changes and short circuit switching. These transients are often encountered in industrial environments, such as factory automation and power-grid systems.

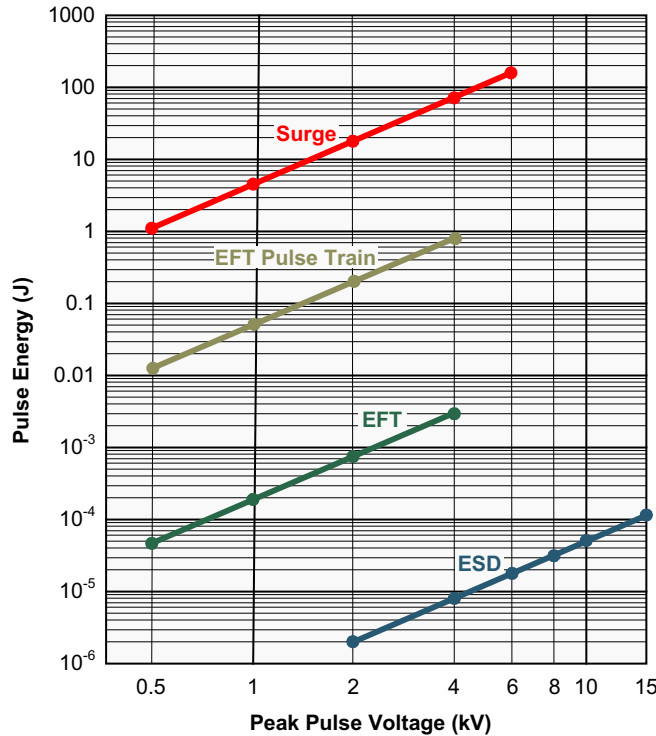
9-3 compares the pulse-power of the EFT and surge transients with the power caused by an IEC ESD transient. The left side of the diagram shows the relative pulse-power for a 0.5-kV surge transient and 4-kV EFT transient, both of which exceed the 10-kV ESD transient visible in the lower-left corner. 500-V surge transients are representative of events that may occur in factory environments in industrial and process automation.

The right side of the diagram shows the pulse-power of a 6-kV surge transient, relative to the same 0.5-kV surge transient. 6-kV surge transients may occur in power generation and power-grid systems.



9-3. Power Comparison of ESD, EFT, and Surge Transients

For surge transients, high-energy content is characterized by long pulse duration and slow decaying pulse power. The electrical energy of a transient that is dumped into the internal protection cells of a transceiver is converted into thermal energy, which heats and destroys the protection cells, thus destroying the transceiver.  9-4 shows the large differences in transient energies for single ESD, EFT, surge transients, and an EFT pulse train that is commonly applied during compliance testing.



 9-4. Comparison of Transient Energies

9.2.2 Detailed Design Procedure

To protect bus nodes against high-energy transients, the implementation of external transient protection devices is necessary. 图 9-5 suggests a protection circuit against 1 kV surge (IEC 61000-4-5) transients. 表 9-1 shows the associated bill of materials.

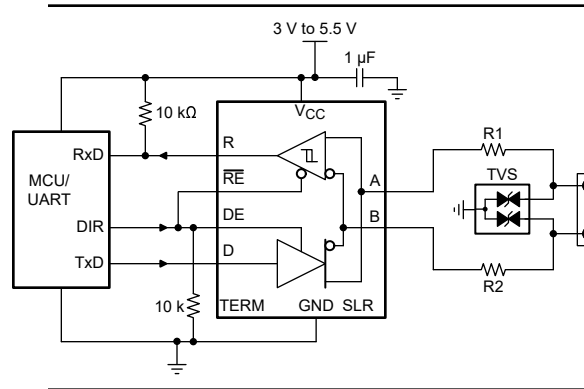


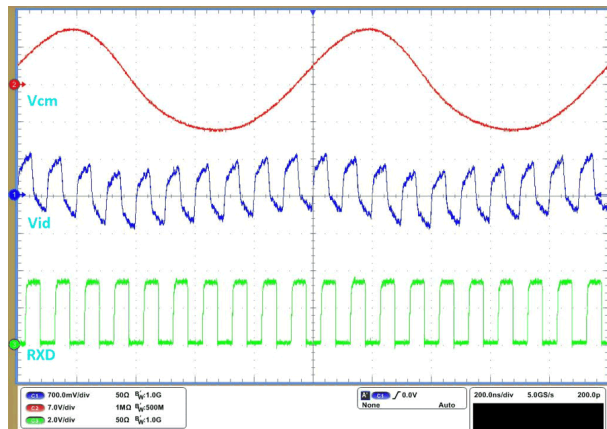
图 9-5. Transient Protection Against Surge Transients for THVD1454

表 9-1. Bill of Materials

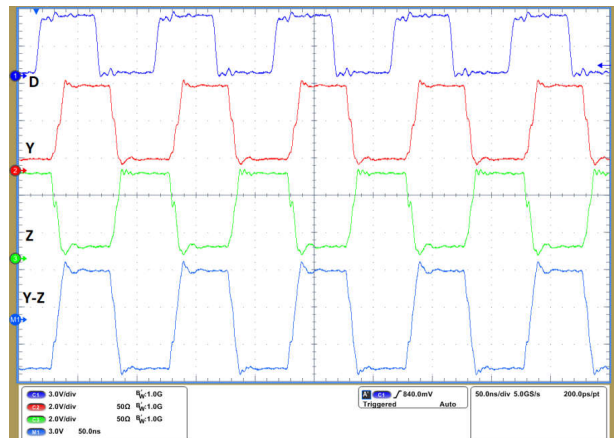
| DEVICE | FUNCTION | ORDER NUMBER | MANUFACTURER ⁽¹⁾ |
|--------|--|--------------------|-----------------------------|
| XCVR | RS-485 transceiver | THVD1454 | TI |
| R1 | 10-Ω, pulse-proof thick-film resistor | CRCW0603010RJNEAHP | Vishay |
| R2 | | | |
| TVS | Bidirectional 400-W transient suppressor | CDSOT23-SM712 | Bourns |

(1) See the [Third Part Disclaimer](#).

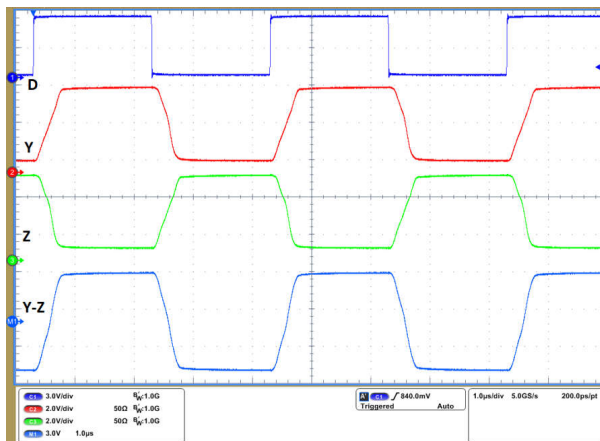
9.2.3 Application Curves



9-6. Receiver Waveforms at 20 Mbps, with Common Mode Moving at 1 Mhz



9-7. Driver Waveforms at 20 Mbps with Termination Enabled



9-8. Driver Waveforms at 500 kbps with Termination Enabled

9.3 Power Supply Recommendations

For reliable operation at all data rates and supply voltages, V_{CC} supply should be decoupled with a 1 μF ceramic capacitor located as close to the supply pin as possible. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes.

9.4 Layout

9.4.1 Layout Guidelines

Robust and reliable bus node design often requires the use of external transient protection devices in order to protect against surge transients that may occur in industrial environments. Since these transients have a wide frequency bandwidth (from approximately 3 MHz to 300 MHz), high-frequency layout techniques should be applied during PCB design.

1. Place the protection circuitry close to the bus connector to prevent noise transients from propagating across the board.
2. Use V_{CC} and ground planes to provide low inductance. Note that high-frequency currents tend to follow the path of least impedance and not the path of least resistance.
3. Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
4. Apply at least 1 μF decoupling capacitors as close as possible to the V_{CC} pin of the transceiver, UART and/or controller ICs on the board.
5. Use at least two vias for V_{CC} and ground connections of decoupling capacitors and protection devices to minimize effective via inductance.
6. Use 1-k Ω to 10-k Ω pull-up and pull-down resistors for logic lines to limit noise currents in these lines during transient events.
7. Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
8. While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1 mA.

9.4.2 Layout Example

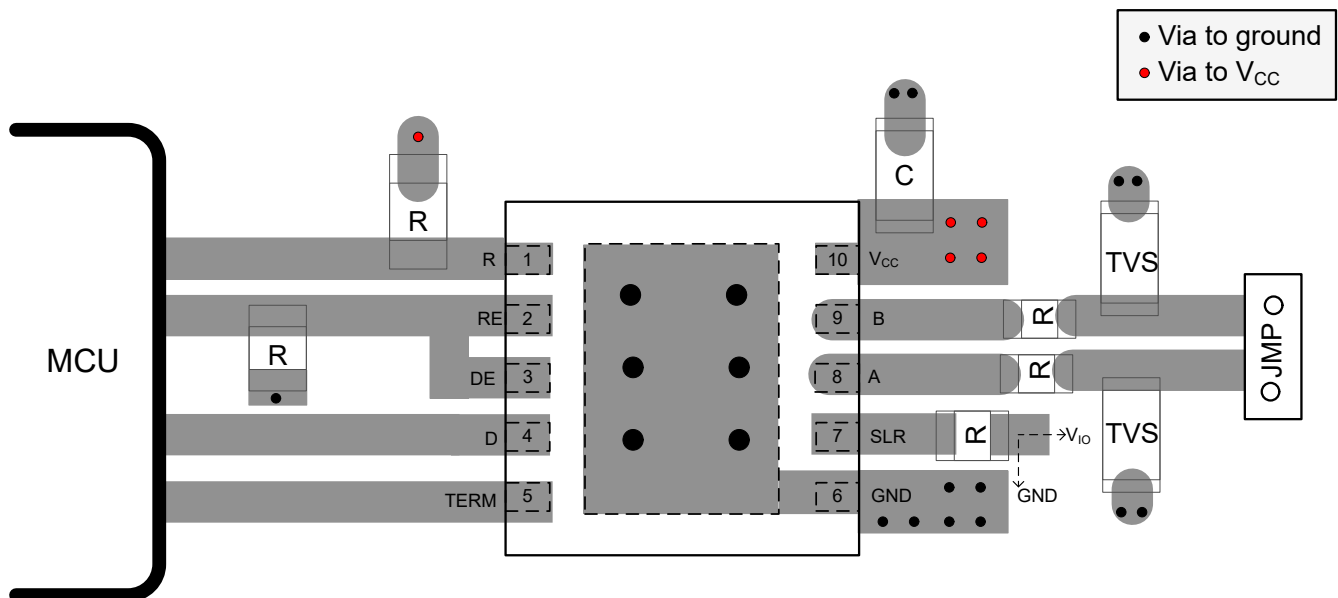


图 9-9. Layout Example for THVD1454 in VSON-10 Package

10 Device and Documentation Support

10.1 Device Support

10.1.1 サード・パーティ製品に関する免責事項

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10.2 ドキュメントの更新通知を受け取る方法

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10.3 サポート・リソース

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10.5 静電気放電に関する注意事項



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10.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| THVD1454DRCR | Active | Production | VSON (DRC) 10 | 5000 LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 1454 |
| THVD1454DRCR.A | Active | Production | VSON (DRC) 10 | 5000 LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 1454 |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

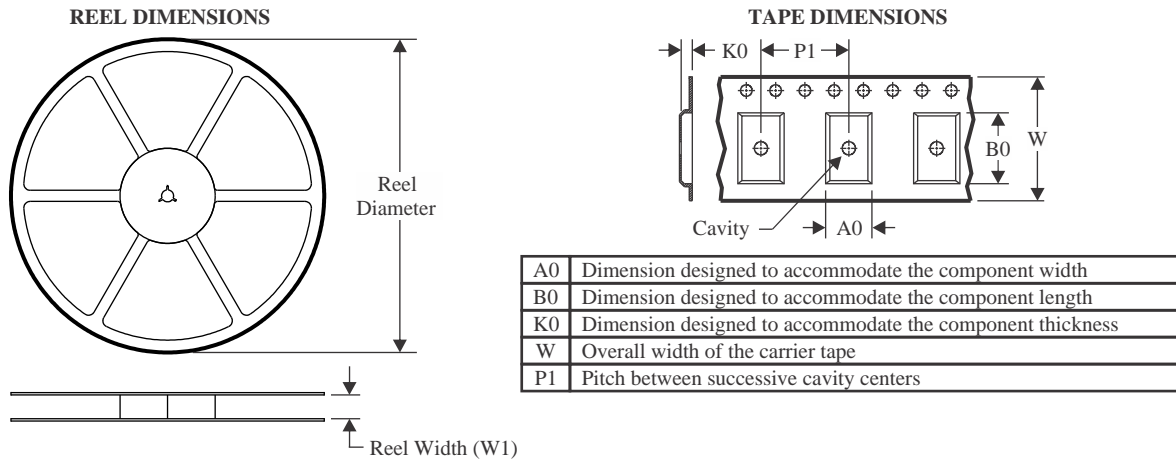
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| THVD1454DRCR | VSON | DRC | 10 | 5000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| THVD1454DRCR | VSON | DRC | 10 | 5000 | 367.0 | 367.0 | 35.0 |

GENERIC PACKAGE VIEW

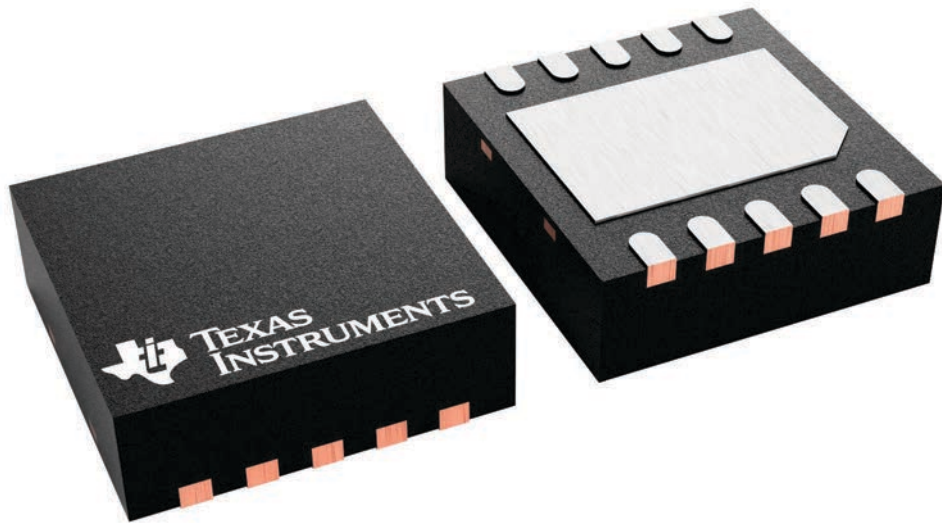
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



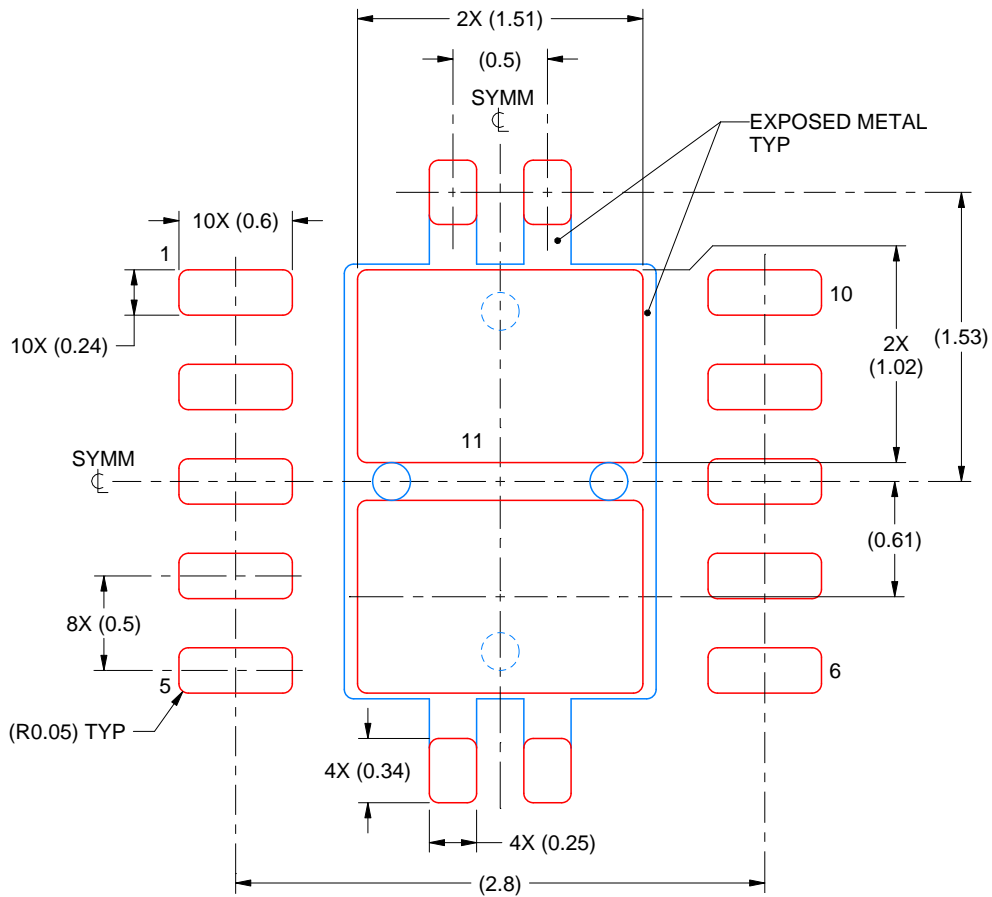
4226193/A

EXAMPLE STENCIL DESIGN

DRC0010V

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4226575/A 02/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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