TEXAS INSTRUMENTS

THVD1510, THVD1512
THVD1550, THVD1551, THVD1552

JAJSDS3C – SEPTEMBER 2017 – REVISED DECEMBER 2018

THVD15xx ±18kV IEC ESD保護の5V RS-485トランシーバ

1 特長

- TIA/EIA-485A規格の要件を満たすか、それを上回る性能
- 電源電圧: 4.5V～5.5V
- バスI/O保護を内蔵
  - ±30kV HBM ESD
  - ±18kV IEC 61000-4-2 ESD接触放電
  - ±25kV IEC 61000-4-2 ESD空中放電
  - ±4kV IEC 61000-4-4電気的高速過渡
- 拡張動作同相電圧: ±15V
- 低EMIで500kbpsおよび50Mbpsのデータレート
- 拡張温度範囲: －40℃～125℃
- レシーバの大きなヒステリシスによるノイズ除去
- 低消費電力
  - 低いスタンバイ時消費電流: 1μA未満
  - 動作時電流: 1mA未満
- グリッチなしの電源オン/オフによるホット・プラグイン能力
- オープン、短絡、アイドル・バスのフェイルセーフ
- 1/8ユニット負荷オプション(最大256のバス・ノード)
- 小型のVSSOPパッケージによるボード・スペースの削減、またはSOICによりドロップイン互換を実現

2 アプリケーション

- モータ制御
- ファクトリ・オートメーション/制御
- グリッド・インフラ
- ビルディング・オートメーション
- HVACシステム
- ビデオ監視
- プロセス分析
- 通信インフラ

3 概要

THVD15xxは、過酷な産業環境で動作するように設計されたノイズ耐性の高いRS-485/RS-422トランシーバ・ファミリです。このデバイスのバス・ピンは、高レベルのIEC電気的高速過渡(EFT)およびIEC静電放電(ESD)事象に対する耐性があるため、システム・レベルの保護部品を追加する必要がありません。

各デバイスは単一5V電源で動作します。このファミリのデバイスは同相電圧範囲が広いため、長いケーブルを使用するマルチポイント・アプリケーションに最適です。

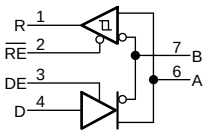
THVD15xxファミリのデバイスは、スペースの制約があるアプリケーション向けに小型のVSSOPパッケージで供給されています。このデバイスは、－40℃～125℃の周囲自由通気温度範囲で仕様が規定されています。

製品情報(1)

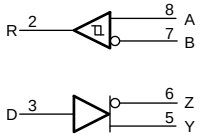
型番	パッケージ	本体サイズ(公称)
THVD1510	VSSOP (8)	3.00mm×3.00mm
THVD1550	SOIC (8)	4.90mm×3.91mm
THVD1551	VSSOP (8)	3.00mm×3.00mm
THVD1512	VSSOP (10)	3.00mm×3.00mm
THVD1552	VSSOP (10)	3.00mm×3.00mm
	SOIC (14)	8.65mm×3.91mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

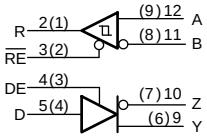
THVD1510およびTHVD1550の概略回路図



THVD1551の概略回路図



THVD1512およびTHVD1552の概略回路図



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目次

4 改訂履歴

Revision B (July 2018) から **Revision C** に変更 **Page**

- Changed the Description of pins 13 and 14 in the *Pin Functions* table for THVD1512, THVD1552 D package ... 5

Revision A (January 2018) から **Revision B** に変更 **Page**

- Added T_{SD} to the *Electrical Characteristics* table ... 8

2017年9月発行のものから更新 **Page**

- Changed the Machine model (MM) value From: ±400 To: ±200 in the *ESD Ratings* ... 6
- Changed the V_{OH} MIN value From: 2.4 V To: 4 V in the *Electrical Characteristics* table ... 8

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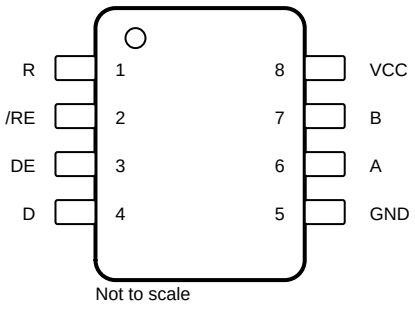
5 Device Comparison Table

PART NUMBER	DUPLEX	ENABLES	SIGNALING RATE	NODES
THVD1512	Full	DE, $\overline{RE}$	up to 500 kbps	256
THVD1510	Half	DE, $\overline{RE}$		
THVD1552	Full	DE, $\overline{RE}$	up to 50 Mbps	196
THVD1551	Full	None		
THVD1550	Half	DE, $\overline{RE}$		

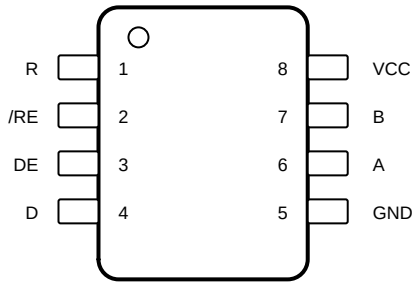
6 Pin Configuration and Functions

THVD1510, THVD1550 Devices
8-Pin D Package (SOIC)
Top View



Not to scale

THVD1510, THVD1550 Devices
8-Pin DGK Package (VSSOP)
Top View



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Pin Functions

PIN			I/O	DESCRIPTION
NAME	D	DGK		
A	6	6	Bus input/output	Bus I/O port, A (complementary to B)
B	7	7	Bus input/output	Bus I/O port, B (complementary to A)
D	4	4	Digital input	Driver data input
DE	3	3	Digital input	Driver enable, active high (2 MΩ internal pull-down)
GND	5	5	Ground	Device ground
R	1	1	Digital output	Receive data output
V_{CC}	8	8	Power	5-V supply
$\overline{RE}$	2	2	Digital input	Receiver enable, active low (2 MΩ internal pull-up)

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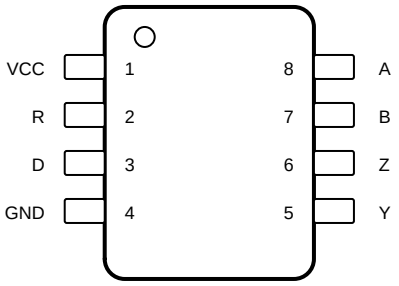
THVD1551 Device
8-Pin DGK Package (VSSOP)
Top View



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Pin Functions

PIN		I/O	DESCRIPTION
NAME	DGK		
A	8	Bus input	Bus input, A (complementary to B)
B	7	Bus input	Bus input, B (complementary to A)
D	3	Digital input	Driver data input
GND	4	Ground	Device ground
R	2	Digital output	Receive data output
V_{CC}	1	Power	5-V supply
Y	5	Bus output	Bus output, Y (complementary to Z)
Z	6	Bus output	Bus output, Z (complementary to Y)

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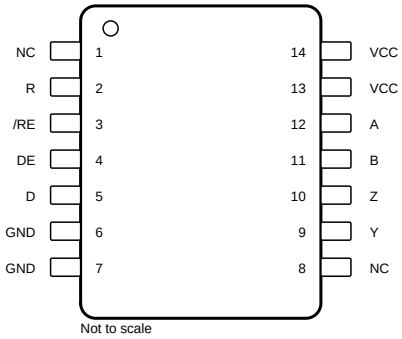
THVD1552 Device
14-Pin D Package (SOIC)
Top View



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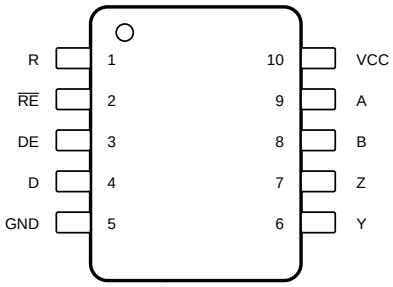
THVD1512, THVD1552 Devices
10-Pin DGS Package (VSSOP)
Top View



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Pin Functions

PIN			I/O	DESCRIPTION
NAME	D	DGS		
A	12	9	Bus input	Bus input, A (complementary to B)
B	11	8	Bus input	Bus input, B (complementary to A)
D	5	4	Digital input	Driver data input
DE	4	3	Digital input	Driver enable, active high (2 MΩ internal pull-down)
GND	6, 7 (1)	5	Ground	Device ground
NC	1, 8	—	—	Internally not connected
R	2	1	Digital output	Receive data output
V_{CC}	—	10	Power	5-V supply.
	13, 14	—	Power	5-V supply. These pins are not connected together internally, so power must be applied to both.
Y	9	6	Bus output	Bus output, Y (Complementary to Z)
Z	10	7	Bus output	Bus output, Z (Complementary to Y)
$\overline{RE}$	3	2	Digital input	Receiver enable, active low (2 MΩ internal pull-up)

(1) These pins are internally connected

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	V_{CC}	–0.5	7	V
Bus voltage	Range at any bus pin (A, B, Y, or Z) as differential or common-mode with respect to GND	–18	18	V
Input voltage	Range at any logic pin (D, DE, or $\overline{RE}$)	–0.3	5.7	V
Receiver output current	I_O	–24	24	mA
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Contact discharge, per IEC 61000-4-2	Bus terminals and GND	±18,000	V
		Air-gap discharge, per IEC 61000-4-2	Bus terminals and GND	±25,000	
		Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Bus terminals and GND	±30,000	
			All pins except Bus terminals and GND	±8,000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1,500	
		Machine model (MM), per JEDEC JESD22-A115-A		±200	
$V_{(EFT)}$	Electrical fast transient	Per IEC 61000-4-4	Bus terminals	±4,000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5		5.5	V
V_I	Input voltage at any bus terminal (1)		-15		15	V
V_{IH}	High-level input voltage (driver, driver enable, and receiver enable inputs)		2		V_{CC}	V
V_{IL}	Low-level input voltage (driver, driver enable, and receiver enable inputs)		0		0.8	V
V_{ID}	Differential input voltage		-15		15	V
I_O	Output current, driver		-60		60	mA
I_{OR}	Output current, receiver		-8		8	mA
R_L	Differential load resistance		54			Ω
$1/t_{UI}$	Signaling rate	THVD1510, THVD1512			500	kbps
		THVD1550, THVD1551, THVD1552			50	Mbps
T_A	Operating ambient temperature		-40		125	°C
T_J	Junction temperature		-40		150	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

7.4 Thermal Information

THERMAL METRIC (1)		THVD1510 THVD1550	THVD1552	THVD1510 THVD1550 THVD1551	THVD1512 THVD1552	UNIT
		D (SOIC)	D (SOIC)	DGK (VSSOP)	DGS (VSSOP)	
		8 PINS	14 PINS	8 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	112.4	88.0	151.7	151.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	62.7	45.4	62.8	59.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62.0	44.1	81.3	81.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	15.4	11.3	7.8	6.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	61.3	43.7	79.8	79.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Power Dissipation

PARAMETER		TEST CONDITIONS			VALUE	UNIT
PD	Driver and receiver enabled, V_{CC} = 5.5 V, T_A = 125 °C, 50% duty cycle square wave at signaling rate	Unterminated R_L = 300 Ω, C_L = 50 pF (driver)	THVD151x	500 kbps	210	mW
			THVD155x	50 Mbps	350	
		RS-422 load R_L = 100 Ω, C_L = 50 pF (driver)	THVD151x	500 kbps	220	mW
			THVD155x	50 Mbps	330	
		RS-485 load R_L = 54 Ω, C_L = 50 pF (driver)	THVD151x	500 kbps	250	mW
			THVD155x	50 Mbps	340	

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7.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
Driver								
$\|V_{OD}\|$	Driver differential output voltage magnitude	R_L = 60 Ω, -15 V ≤ V_{test} ≤ 15 V, (See 図 11)			1.5	2.7		V
		R_L = 100 Ω (See 図 12)			2	3		V
		R_L = 54 Ω (See 図 12)			1.5	2.7		V
$\Delta\|V_{OD}\|$	Change in differential output voltage	R_L = 54 Ω (See 図 12)			–200		200	mV
V_{OC}	Common-mode output voltage				1	V_{CC}/2	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage				–200		200	mV
I_{OS}	Short-circuit output current	DE = V_{CC}, -15 V ≤ V_O ≤ 15V			–250		250	mA
Receiver								
I_I	Bus input current	DE = 0 V, V_{CC} = 0 V or 5.5 V	THVD151x	V_I = 12 V		75	125	µA
				V_I = 15 V		95	156	
				V_I = -7 V	-100	-40		
				V_I = -15 V	-215	-85		
			THVD155x	V_I = 12 V		115	160	
				V_I = 15 V		150	200	
				V_I = -7 V	-130	-75		
				V_I = -15 V	-280	-180		
Receiver								
V_{TH+}	Positive-going input threshold voltage	Over common-mode range of - 7 V to +12 V			See(1)	–85	–20	mV
V_{TH-}	Negative-going input threshold voltage				–200	–135	See(1)	mV
V_{HYS}	Input hysteresis					50		mV
V_{TH+}	Positive-going input threshold voltage	Over common-mode range of ± 15 V			See(1)	–85	–20	mV
V_{TH-}	Negative-going input threshold voltage				–220	–135	See(1)	mV
V_{HYS}	Input hysteresis					50		mV
V_{OH}	Output high voltage	I_{OH} = -8 mA			4	V_{CC} - 0.3		V
V_{OL}	Output low voltage	I_{OL} = 8 mA				0.2	0.4	V
I_{OZ}	Output high-impedance current	V_O = 0 V or V_{CC}, $\overline{RE}$ = V_{CC}			-1		1	µA
Logic								
I_{IN}	Input current (D, DE, $\overline{RE}$)	4.5 V ≤ V_{CC} ≤ 5.5 V, 0 V ≤ V_{IN} ≤ V_{CC}			–5	0	5	µA
Supply								
I_{CC}	Supply current (quiescent)	Driver and receiver enabled		$\overline{RE}$ = 0 V, DE = V_{CC}, No load		700	1000	µA
		Driver enabled, receiver disabled		$\overline{RE}$ = V_{CC}, DE = V_{CC}, No load		400	620	µA
		Driver disabled, receiver enabled		$\overline{RE}$ = 0 V, DE = 0 V, No load		400	630	µA
		Driver and receiver disabled		$\overline{RE}$ = V_{CC}, DE = 0 V, D = open, No load		0.1	1	µA
T_{SD}	Thermal shutdown temperature					170		°C

(1) Under any specific conditions, V_{TH+} is specified to be at least V_{HYS} higher than $V_{TH–}$.

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7.7 Switching Characteristics

500-kbps devices (THVD1510, THVD1512) over recommended operating conditions

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
t_r, t_f	Differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF	See 図 13	300	400	600	ns
t_{PHL}, t_{PLH}	Propagation delay				350	500	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL} - t_{PLH}\|$					15	ns
t_{PHZ}, t_{PLZ}	Disable time (THVD1510, THVD1512)		See 図 14 and 図 15		110	200	ns
t_{PZH}, t_{PZL}	Enable time (THVD1510, THVD1512)	$\overline{RE}$ = 0 V			100	500	ns
		$\overline{RE}$ = V_{CC}			2	4	µs
Receiver							
t_r, t_f	Differential output rise/fall time	C_L = 15 pF	See 図 16		15	25	ns
t_{PHL}, t_{PLH}	Propagation delay				50	60	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL} - t_{PLH}\|$					10	ns
t_{PHZ}, t_{PLZ}	Disable time (THVD1510, THVD1512)				30	40	ns
$t_{PZH(1)}$, $t_{PZL(1)}$, $t_{PZH(2)}$, $t_{PZL(2)}$	Enable time (THVD1510, THVD1512)	DE = V_{CC}	See 図 17		60	100	ns
		DE = 0 V	See 図 18		3	8	µs

7.8 Switching Characteristics

50-Mbps devices (THVD1550, THVD1551, THVD1552) over recommended operating conditions

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
t_r, t_f	Differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF	See 図 13	1	2	6	ns
t_{PHL}, t_{PLH}	Propagation delay			5	10	16	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL} - t_{PLH}\|$					3.5	ns
t_{PHZ}, t_{PLZ}	Disable time (THVD1550, THVD1552)		See 図 14 and 図 15		10	22	ns
t_{PZH}, t_{PZL}	Enable time (THVD1550, THVD1552)	$\overline{RE}$ = 0 V			10	22	ns
		$\overline{RE}$ = V_{CC}			2	4	µs
Receiver							
t_r, t_f	Differential output rise/fall time	C_L = 15 pF	See 図 16	1	3	6	ns
t_{PHL}, t_{PLH}	Propagation delay				30	45	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL} - t_{PLH}\|$					2	ns
t_{PHZ}, t_{PLZ}	Disable time (THVD1550, THVD1552)				8	18	ns
$t_{PZH(1)}$, $t_{PZL(1)}$, $t_{PZH(2)}$, $t_{PZL(2)}$	Enable time (THVD1550, THVD1552)	DE = V_{CC}	See 図 17		55	90	ns
		DE = 0 V	See 図 18		3	8	µs

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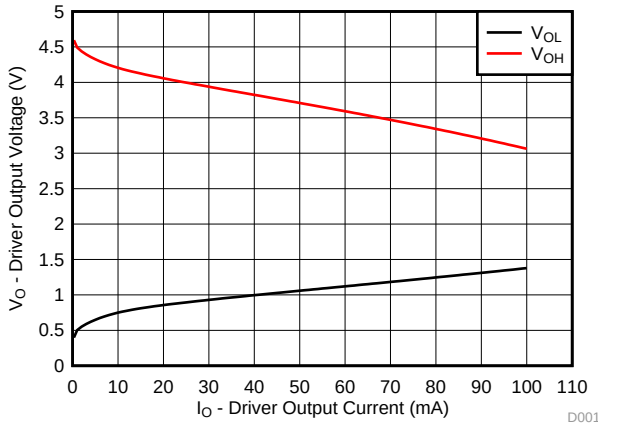
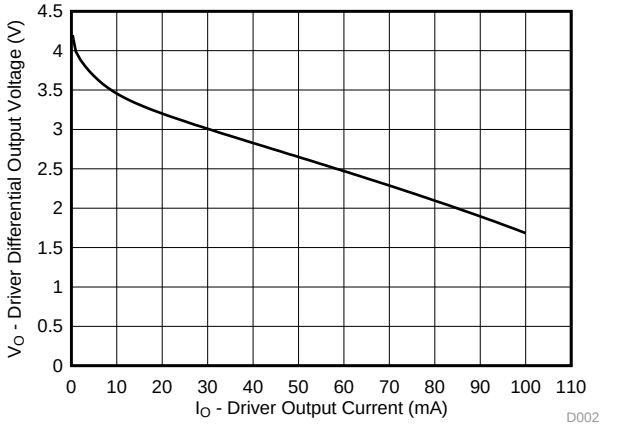
7.9 Typical Characteristics



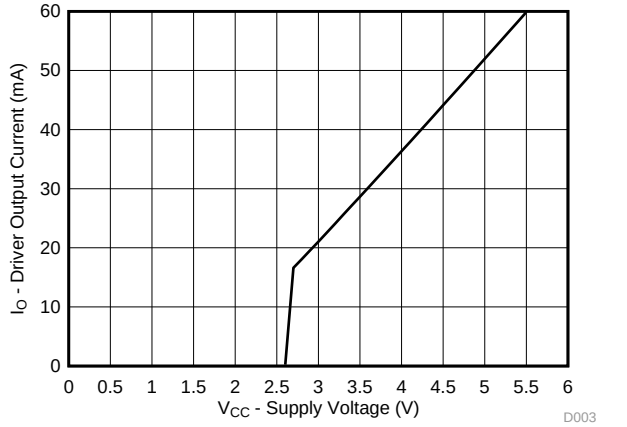
V_{CC} = 5 V　　DE = V_{CC}　　D = 0 V

図 1. Driver Output Voltage vs Driver Output Current



V_{CC} = 5 V　　DE = V_{CC}　　D = 0 V

図 2. Driver Differential Output Voltage vs Driver Output



T_A = 25°C　　R_L = 54 Ω　　D = V_{CC}
DE = V_{CC}

図 3. Driver Output Current vs Supply Voltage

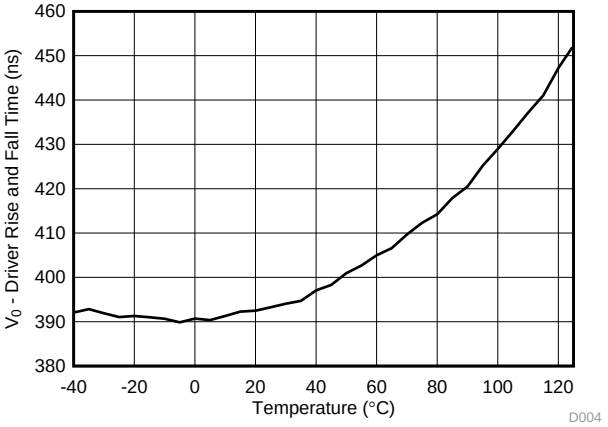


図 4. THVD1510 Driver Rise or Fall Time vs Temperature

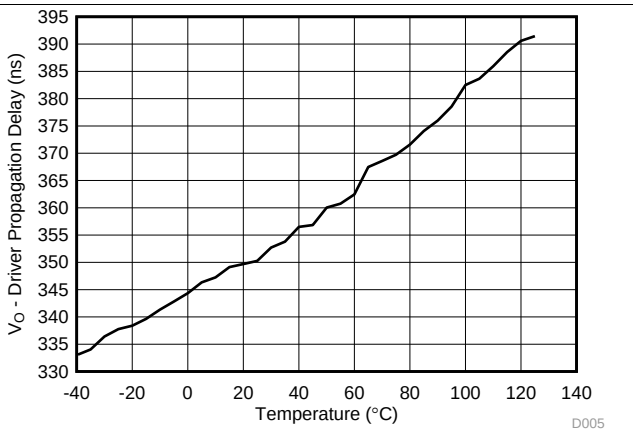


図 5. THVD1510 Driver Propagation Delay vs Temperature

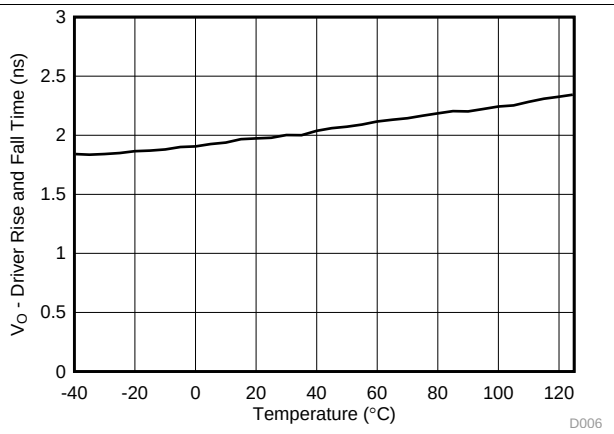


図 6. THVD1550 Driver Rise or Fall Time vs Temperature

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Typical Characteristics (continued)

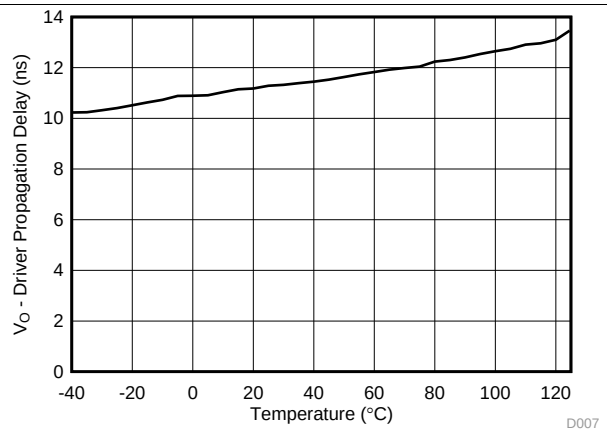
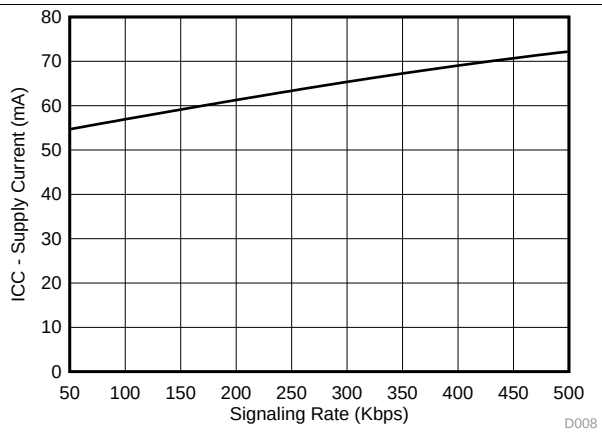
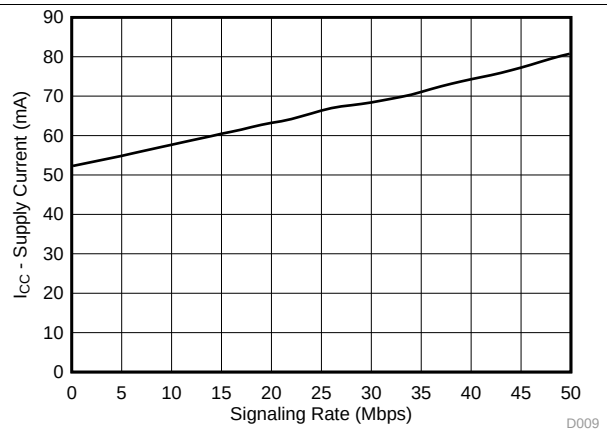


図 7. THVD1550 Driver Propagation Delay vs Temperature



R_L = 54 Ω

図 8. THVD1510 Supply Current vs Signal Rate



R_L = 54 Ω

図 9. THVD1550 Supply Current vs Signal Rate

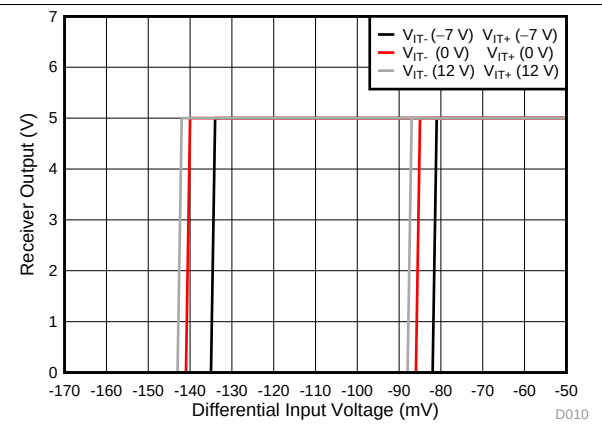


図 10. Receiver Output vs Input

8 Parameter Measurement Information

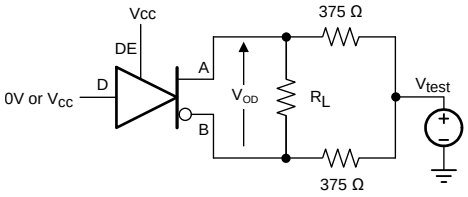


図 11. Measurement of Driver Differential Output Voltage With Common-Mode Load

図 12. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

Parameter Measurement Information (continued)

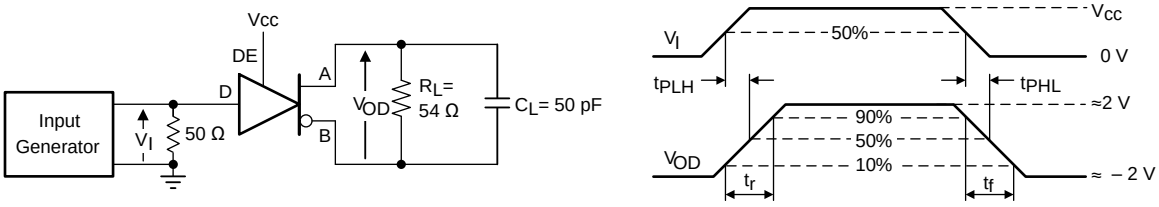


図 13. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays

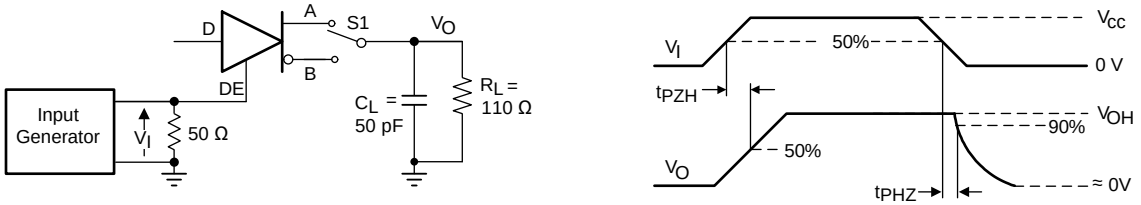


図 14. Measurement of Driver Enable and Disable Times With Active High Output and Pull-Down Load

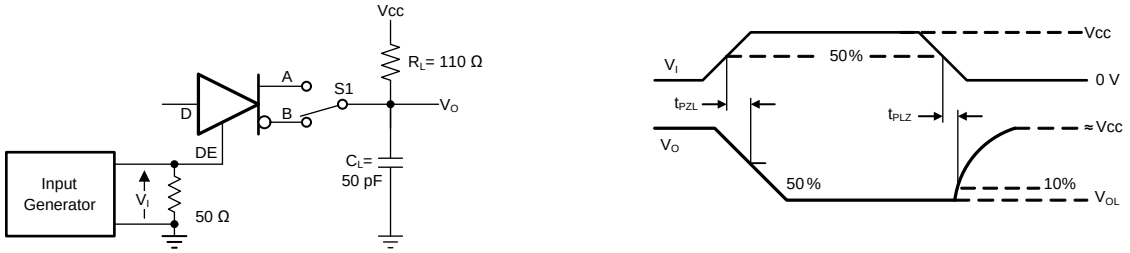


図 15. Measurement of Driver Enable and Disable Times With Active Low Output and Pull-up Load

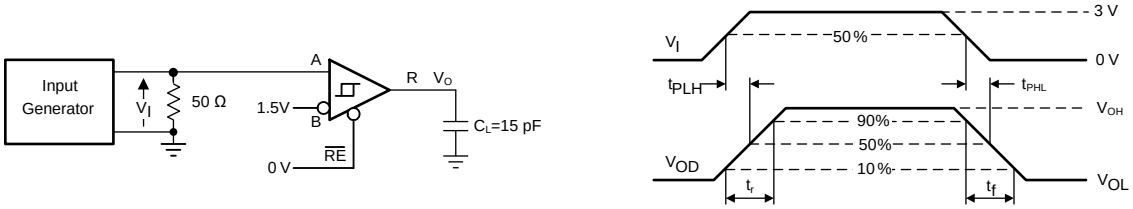


図 16. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

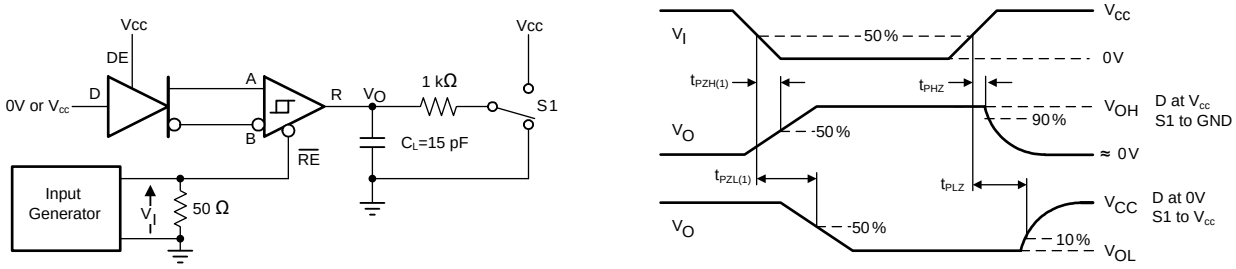


図 17. Measurement of Receiver Enable/Disable Times With Driver Enabled

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Parameter Measurement Information (continued)

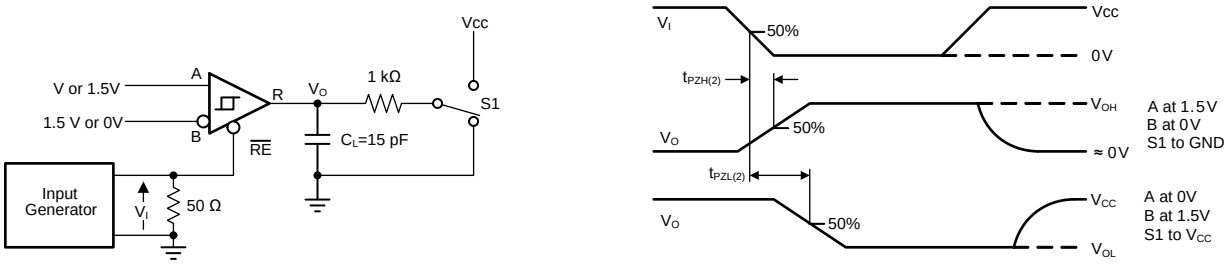

図 18. Measurement of Receiver Enable Times With Driver Disabled

9 Detailed Description

9.1 Overview

THVD1510 and THVD1550 are low-power, half-duplex RS-485 transceivers available in two speed grades suitable for data transmission up to 500 kbps and 50 Mbps respectively.

THVD1551 is fully enabled with no external enabling pins. THVD1512 and THVD1552 have active-high driver enables and active-low receiver enables. A standby current of less than 1 µA can be achieved by disabling both driver and receiver.

9.2 Functional Block Diagrams

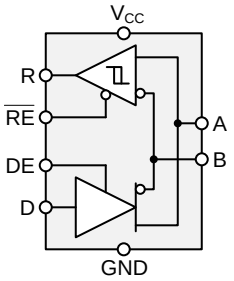

図 19. THVD1510 and THVD1550

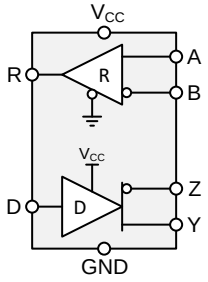

図 20. THVD1551

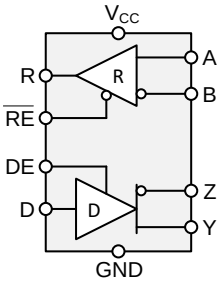

図 21. THVD1512 and THVD1552

9.3 Feature Description

Internal ESD protection circuits of the THVD15xx protect the transceivers against electrostatic discharges (ESD) according to IEC 61000-4-2 of up to ±18 kV and against electrical fast transients (EFT) according to IEC 61000-4-4 of up to ±4 kV. With careful system design, one could achieve ±4 kV EFT Criterion A (no data loss when transient noise is present).

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Feature Description (continued)

The THVD15xx device family provides internal biasing of the receiver input thresholds in combination with large input-threshold hysteresis. The receiver output remains logic high under a bus-idle or bus-short conditions without the need for external failsafe biasing resistors. Device operation is specified over a wide ambient temperature range from –40°C to 125°C.

9.4 Device Functional Modes

9.4.1 Device Functional Modes for THVD1510 and THVD1550

When the driver enable pin, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case the differential output voltage defined as $V_{OD} = V_A – V_B$ is positive. When D is low, the output states reverse: B turns high, A becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pull-down resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pull-up resistor to V_{CC}, thus, when left open while the driver is enabled, output A turns high and B turns low.

表 1. Driver Function Table for THVD1510 and THVD1550

INPUT	ENABLE	OUTPUTS		FUNCTION
D	DE	A	B	
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus high by default

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A – V_B$ is higher than the positive input threshold, V_{TH+}, the receiver output, R, turns high. When V_{ID} is lower than the negative input threshold, V_{TH-}, the receiver output, R, turns low. If V_{ID} is between V_{TH+} and V_{TH-} the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted to one another (short-circuit), or the bus is not actively driven (idle bus).

表 2. Receiver Function Table for THVD1510 and THVD1550

DIFFERENTIAL INPUT	ENABLE	OUTPUT	FUNCTION
$V_{ID} = V_A – V_B$	$\overline{RE}$	R	
$V_{TH+} < V_{ID}$	L	H	Receive valid bus high
$V_{TH-} < V_{ID} < V_{TH+}$	L	?	Indeterminate bus state
$V_{ID} < V_{TH-}$	L	L	Receive valid bus low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

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9.4.2 Device Functional Modes for THVD1551

For this device, the driver and receiver are fully enabled, thus the differential outputs Y and Z follow the logic states at data input D at all times. A logic high at D causes Y to turn high and Z to turn low. In this case, the differential output voltage defined as $V_{OD} = V_Y – V_Z$ is positive. When D is low, the output states reverse: Z turns high, Y becomes low, and VOD is negative. The D pin has an internal pull-up resistor to V_{CC}, thus, when left open while the driver is enabled, output Y turns high and Z turns low.

表 3. Driver Function Table for THVD1551

INPUT	OUTPUTS		FUNCTIONS
D	Y	Z	
H	H	L	Actively drive bus high
L	L	H	Actively drive bus low
OPEN	H	L	Actively drive bus high by default

When the differential input voltage defined as $V_{ID} = V_A – V_B$ is higher than the positive input threshold, V_{TH+}, the receiver output, R, turns high. When V_{ID} is less than the negative input threshold, $V_{TH–}$, the receiver output, R, turns low. If V_{ID} is between V_{TH+} and $V_{TH–}$ the output is indeterminate. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted to one another (short-circuit), or the bus is not actively driven (idle bus).

表 4. Receiver Function Table for THVD1551

DIFFERENTIAL INPUT	OUTPUT	FUNCTION
$V_{ID} = V_A – V_B$	R	
$V_{TH+} < V_{ID}$	H	Receive valid bus high
$V_{TH-} < V_{ID} < V_{TH+}$	?	Indeterminate bus state
$V_{ID} < V_{TH-}$	L	Receive valid bus low
Open-circuit bus	H	Fail-safe high output
Short-circuit bus	H	Fail-safe high output
Idle (terminated) bus	H	Fail-safe high output

9.4.3 Device Functional Modes for THVD1512 and THVD1552

When the driver enable pin, DE, is logic high, the differential outputs Y and Z follow the logic states at data input D. A logic high at D causes Y to turn high and Z to turn low. In this case the differential output voltage defined as $V_{OD} = V_Y – V_Z$ is positive. When D is low, the output states reverse: Z turns high, Y becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pull-down resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pull-up resistor to V_{CC}, thus, when left open while the driver is enabled, output Y turns high and Z turns low.

表 5. Driver Function Table for THVD1512 and THVD1552

INPUT	ENABLE	OUTPUTS		FUNCTION
D	DE	Y	Z	
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus high by default

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When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A - V_B$ is higher than the positive input threshold, V_{TH+}, the receiver output, R, turns high. When V_{ID} is lower than the negative input threshold, V_{TH-}, the receiver output, R, turns low. If V_{ID} is between V_{TH+} and V_{TH-} the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted to one another (short-circuit), or the bus is not actively driven (idle bus).

表 6. Receiver Function Table for THVD1512 and THVD1552

DIFFERENTIAL INPUT	ENABLE	OUTPUT	FUNCTION
$V_{ID} = V_A - V_B$	$\overline{RE}$	R	
$V_{TH+} < V_{ID}$	L	H	Receive valid bus high
$V_{TH-} < V_{ID} < V_{TH+}$	L	?	Indeterminate bus state
$V_{ID} < V_{TH-}$	L	L	Receive valid bus low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

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10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The THVD15xx family consists of half-duplex and full-duplex RS-485 transceivers commonly used for asynchronous data transmissions. For half-duplex devices, the driver and receiver enable pins allow for the configuration of different operating modes. Full-duplex implementation requires two signal pairs (four wires), and allows each node to transmit data on one pair while simultaneously receiving data on the other pair.

10.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T, whose value matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, generally allows for higher data rates over longer cable length.

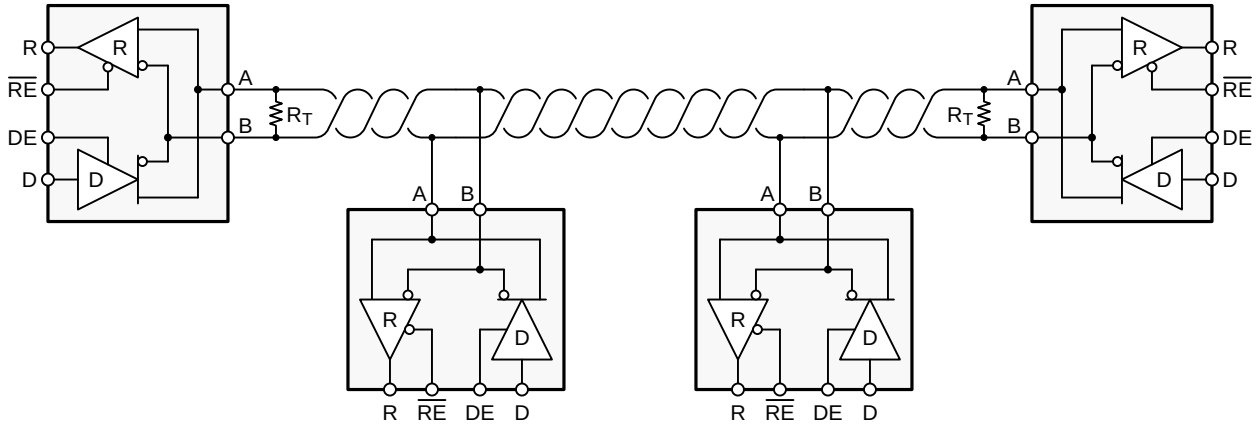

図 22. Typical RS-485 Network With Half-Duplex Transceivers

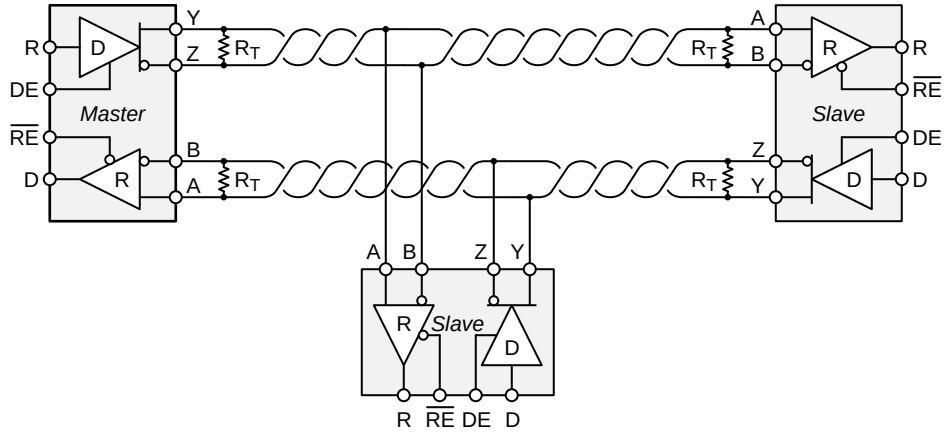

図 23. Typical RS-485 Network With Full-Duplex Transceivers

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Typical Application (continued)

10.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

10.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the shorter the cable length; and conversely, the lower the data rate, the longer the cable length. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 250 kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

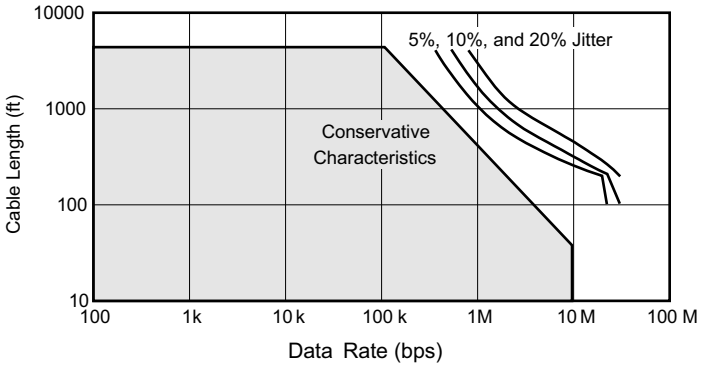

図 24. Cable Length vs Data Rate Characteristic

Even higher data rates are achievable (that is, 50 Mbps for the THVD1550, THVD1551 and THVD1552) in cases where the interconnect is short enough (or has suitably low attenuation at signal frequencies) to not degrade the data.

10.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections of varying phase as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in 式 1.

$$L_{(STUB)} \leq 0.1 \times t_r \times v \times c \quad (1)$$

where

- t_r is the 10/90 rise time of the driver
- c is the speed of light (3×10^8 m/s)
- v is the signal velocity of the cable or trace as a factor of c

10.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to drive 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 kΩ. Because the THVD15xx family consists of 1/8 UL transceivers, connecting up to 256 receivers to the bus is possible.

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Typical Application (continued)

10.2.1.4 Receiver Failsafe

The differential receivers of the THVD15xx family are failsafe to invalid bus states caused by the following:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver will output a failsafe logic high state so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds such that the input indeterminate range does not include zero volts differential. In order to comply with the RS-422 and RS-485 standards, the receiver output must output a high when the differential input V_{ID} is more positive than 200 mV, and must output a low when V_{ID} is more negative than –200 mV. The receiver parameters which determine the failsafe performance are V_{TH+}, $V_{TH–}$, and V_{HYS} (the separation between V_{TH+} and $V_{TH–}$). As shown in the Electrical Characteristics table, differential signals more negative than –200 mV will always cause a low receiver output, and differential signals more positive than 200 mV will always cause a high receiver output.

When the differential input signal is close to zero, it is still above the V_{TH+} threshold, and the receiver output will be high. Only when the differential input is more than V_{HYS} below V_{TH+} will the receiver output transition to a low state. Therefore, the noise immunity of the receiver inputs during a bus fault conditions includes the receiver hysteresis value, V_{hys}, as well as the value of V_{TH+}.

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Typical Application (continued)

10.2.1.5 Transient Protection

The bus pins of the THVD15xx transceiver family include on-chip ESD protection against ±30-kV HBM and ±18-kV IEC 61000-4-2 contact discharge. The International Electrotechnical Commission (IEC) ESD test is far more severe than the HBM ESD test. The 50% higher charge capacitance, $C_{(S)}$, and 78% lower discharge resistance, $R_{(D)}$, of the IEC model produce significantly higher discharge currents than the HBM model. As stated in the IEC 61000-4-2 standard, contact discharge is the preferred transient protection test method.

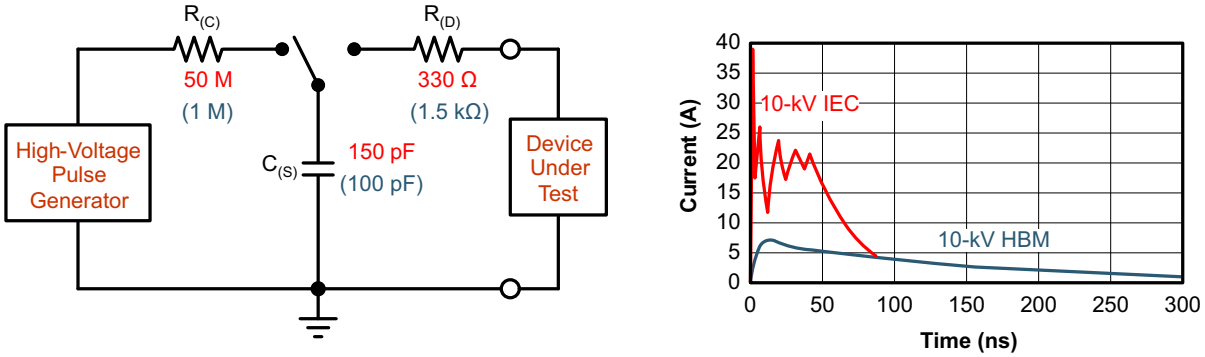

図 25. HBM and IEC ESD Models and Currents in Comparison (HBM Values in Parenthesis)

The on-chip implementation of IEC ESD protection significantly increases the robustness of equipment. Common discharge events occur because of human contact with connectors and cables. Designers may choose to implement protection against longer duration transients, typically referred to as surge transients.

EFTs are generally caused by relay-contact bounce or the interruption of inductive loads. Surge transients often result from lightning strikes (direct strike or an indirect strike which induce voltages and currents), or the switching of power systems, including load changes and short circuit switching. These transients are often encountered in industrial environments, such as factory automation and power-grid systems.

図 26 compares the pulse power of the EFT and surge transients with the power caused by an IEC ESD transient. The left-hand diagram shows the relative pulse-power for a 0.5-kV surge transient and 4-kV EFT transient, both of which dwarf the 10-kV ESD transient visible in the lower-left corner. 500-V surge transients are representative of events that may occur in factory environments in industrial and process automation.

The right-hand diagram shows the pulse-power of a 6-kV surge transient, relative to the same 0.5-kV surge transient. 6-kV surge transients are most likely to occur in power generation and power-grid systems.

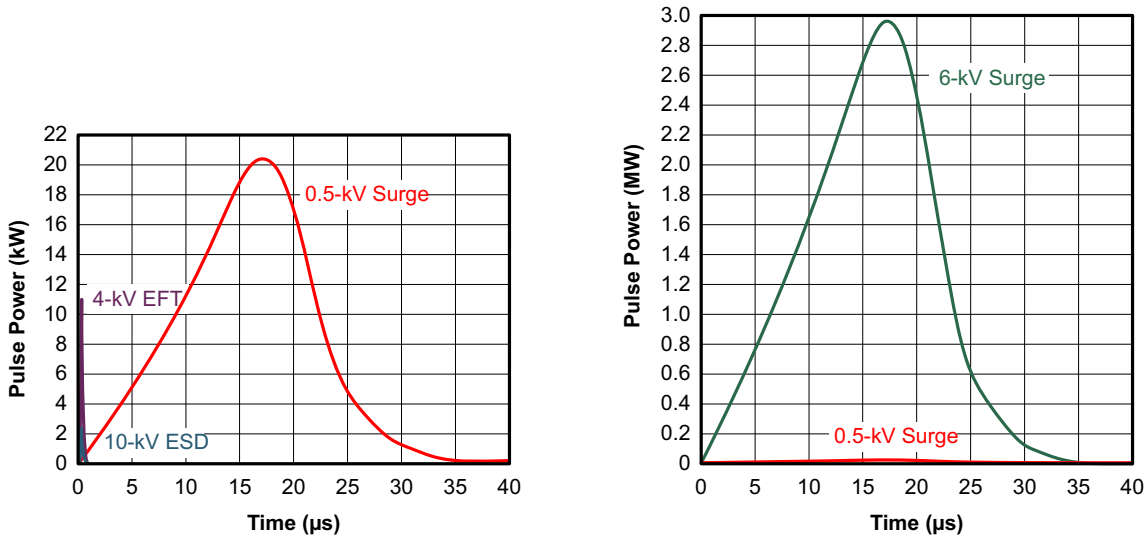

図 26. Power Comparison of ESD, EFT, and Surge Transients

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Typical Application (continued)

In the case of surge transients, high-energy content is characterized by long pulse duration and slow decaying pulse power. The electrical energy of a transient that is dumped into the internal protection cells of a transceiver is converted into thermal energy, which heats and destroys the protection cells, thus destroying the transceiver. 図 27 shows the large differences in transient energies for single ESD, EFT, surge transients, and an EFT pulse train that is commonly applied during compliance testing.

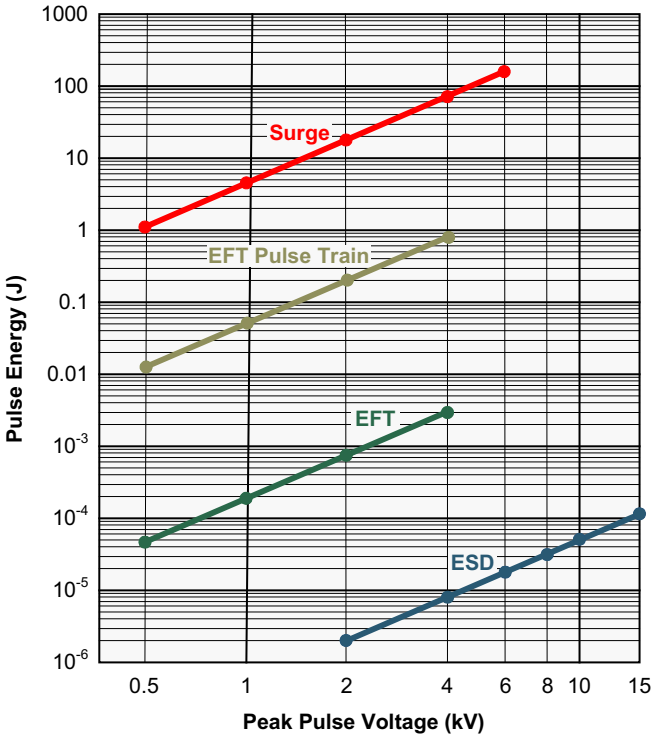

図 27. Comparison of Transient Energies

10.2.2 Detailed Design Procedure

図 28 and 図 29 suggest a protection circuit against 1 kV surge (IEC 61000-4-5) transients. 表 7 shows the associated bill of materials.

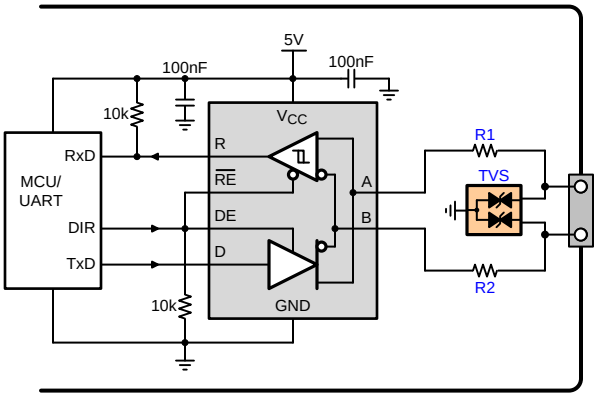

図 28. Transient Protection Against Surge Transients for Half-Duplex Devices

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Typical Application (continued)

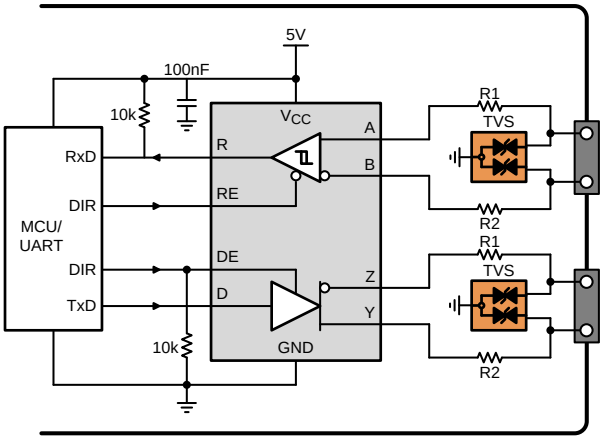

図 29. Transient Protection Against Surge Transients for Full-Duplex Devices

表 7. Bill of Materials

DEVICE	FUNCTION	ORDER NUMBER	MANUFACTURER
XCVR	5-V, RS-485 transceiver	THVD15xx	TI
R1	10-Ω, pulse-proof thick-film resistor	CRCW0603010RJNEAHP	Vishay
R2			
TVS	Bidirectional 400-W transient suppressor	CDSOT23-SM712	Bourns

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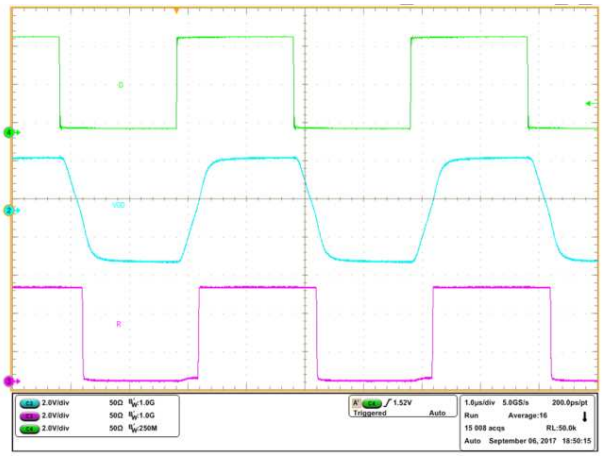
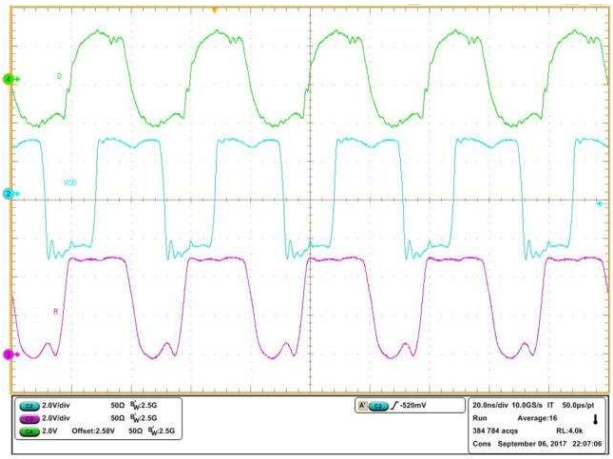
10.2.3 Application Curves



500 kbps

図 30. THVD1510 Waveforms with 60-Ω Termination



50 Mbps

図 31. THVD1550 Waveforms with 60-Ω Termination

11 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with a 100 nF ceramic capacitor located as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes.

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12 Layout

12.1 Layout Guidelines

Robust and reliable bus node design often requires the use of external transient protection devices in order to protect against surge transients that may occur in industrial environments. Since these transients have a wide frequency bandwidth (from approximately 3 MHz to 300 MHz), high-frequency layout techniques should be applied during PCB design.

1. Place the protection circuitry close to the bus connector to prevent noise transients from propagating across the board.
2. Use V_{CC} and ground planes to provide low inductance. Note that high-frequency currents tend to follow the path of least impedance and not the path of least resistance.
3. Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
4. Apply 100-nF to 220-nF decoupling capacitors as close as possible to the V_{CC} pins of transceiver, UART and/or controller ICs on the board.
5. Use at least two vias for V_{CC} and ground connections of decoupling capacitors and protection devices to minimize effective via inductance.
6. Use 1-kΩ to 10-kΩ pullup and pulldown resistors for enable lines to limit noise currents in these lines during transient events.
7. Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
8. While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1 mA.

12.2 Layout Example

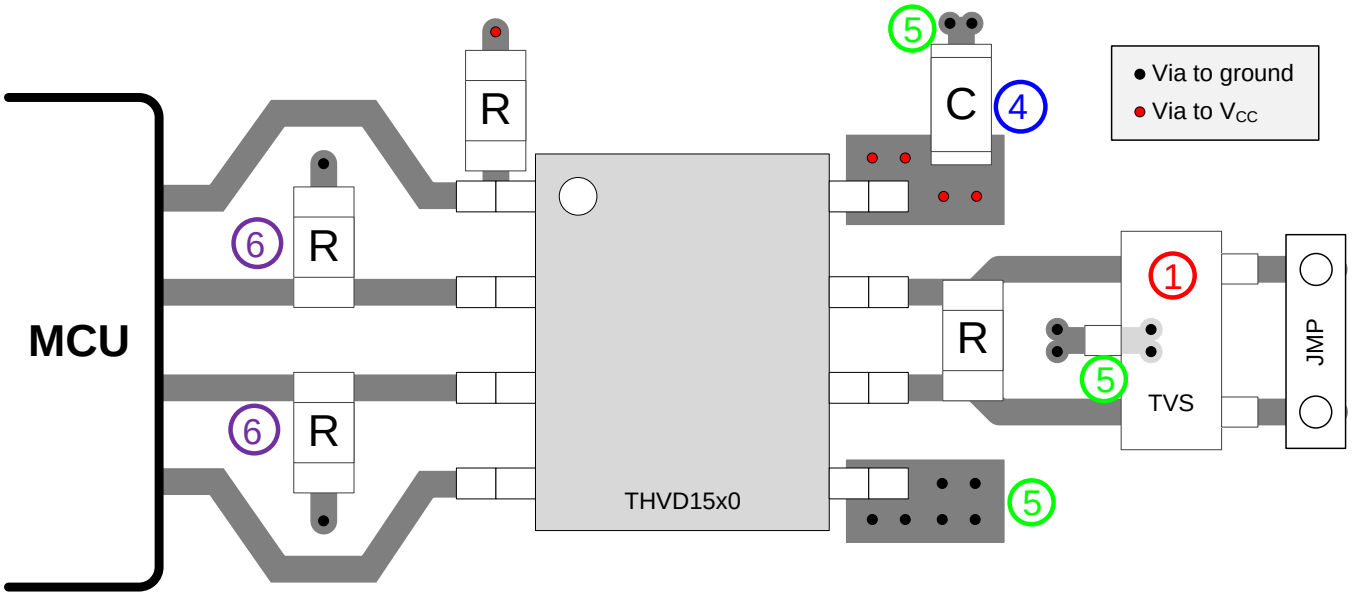

図 32. Half-Duplex Layout Example

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13 デバイスおよびドキュメントのサポート

13.1 デバイス・サポート

13.2 デベロッパー・ネットワークの製品に関する免責事項

デベロッパー・ネットワークの製品またはサービスに関するTIの出版物は、単独またはTIの製品、サービスと一緒に提供される場合に関係なく、デベロッパー・ネットワークの製品またはサービスの適合性に関する是認、デベロッパー・ネットワークの製品またはサービスの是認の表明を意味するものではありません。

13.3 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびご注文へのクイック・アクセスが含まれます。

表 8. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
THVD1510	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
THVD1512	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
THVD1550	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
THVD1551	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
THVD1552	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

13.4 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comで、お使いのデバイスの製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」ボタンをクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

13.5 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E (Engineer-to-Engineer) コミュニティ。*** エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。

設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

13.6 商標

E2E is a trademark of Texas Instruments.

13.7 静電気放電に関する注意事項

これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

13.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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14 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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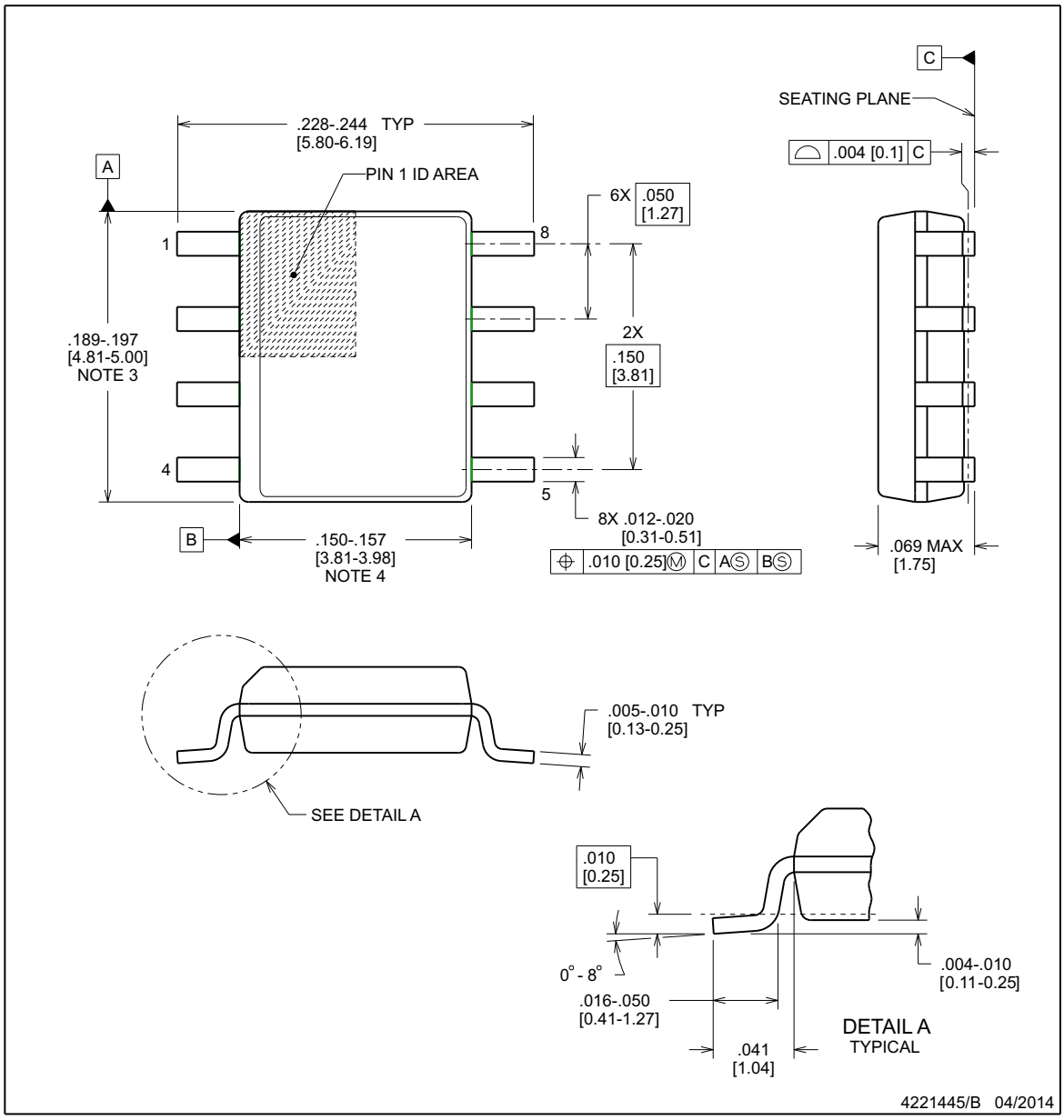
PACKAGE OUTLINE

D0008B

SOIC - 1.75 mm max height

SOIC



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15], per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

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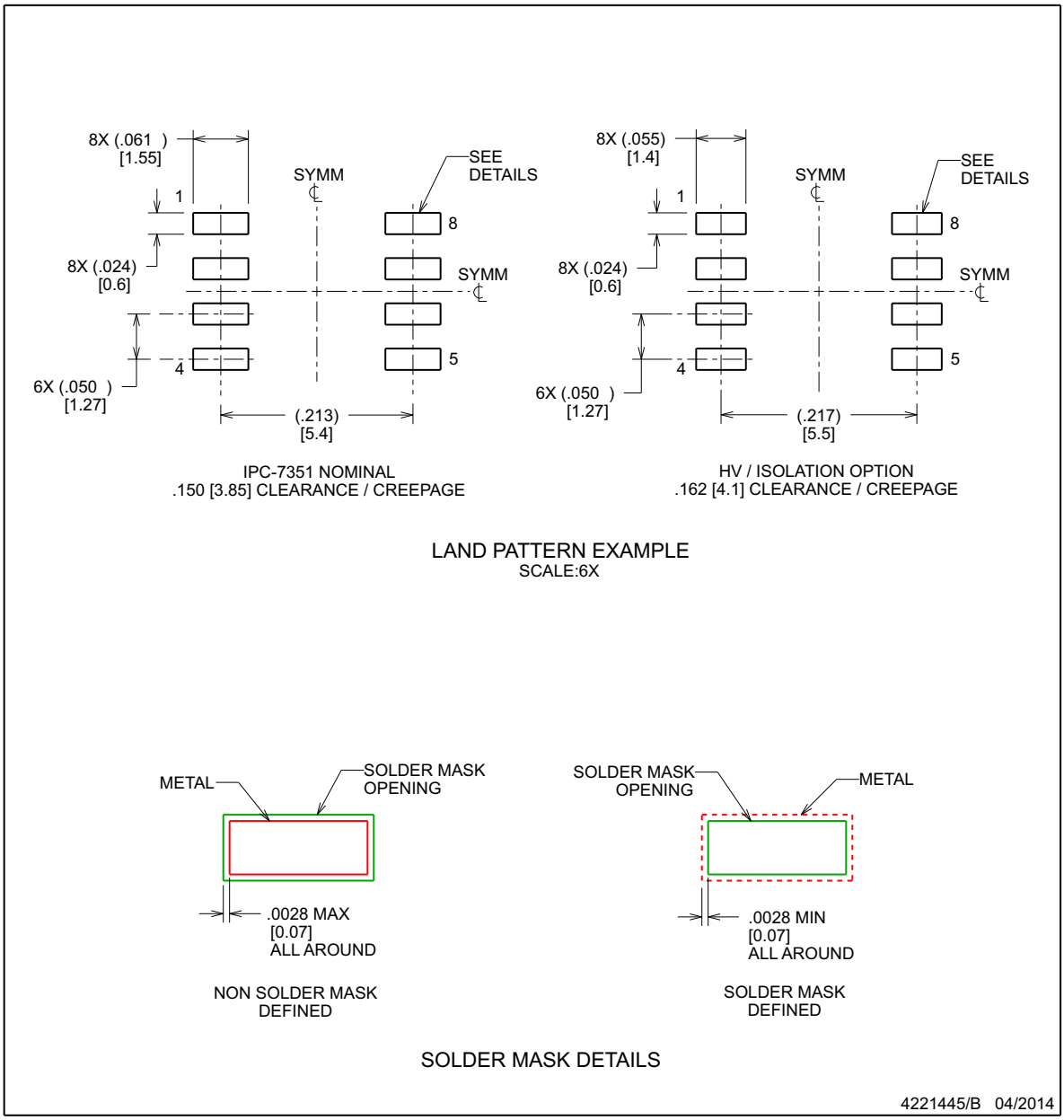
EXAMPLE BOARD LAYOUT

D0008B

SOIC - 1.75 mm max height

SOIC



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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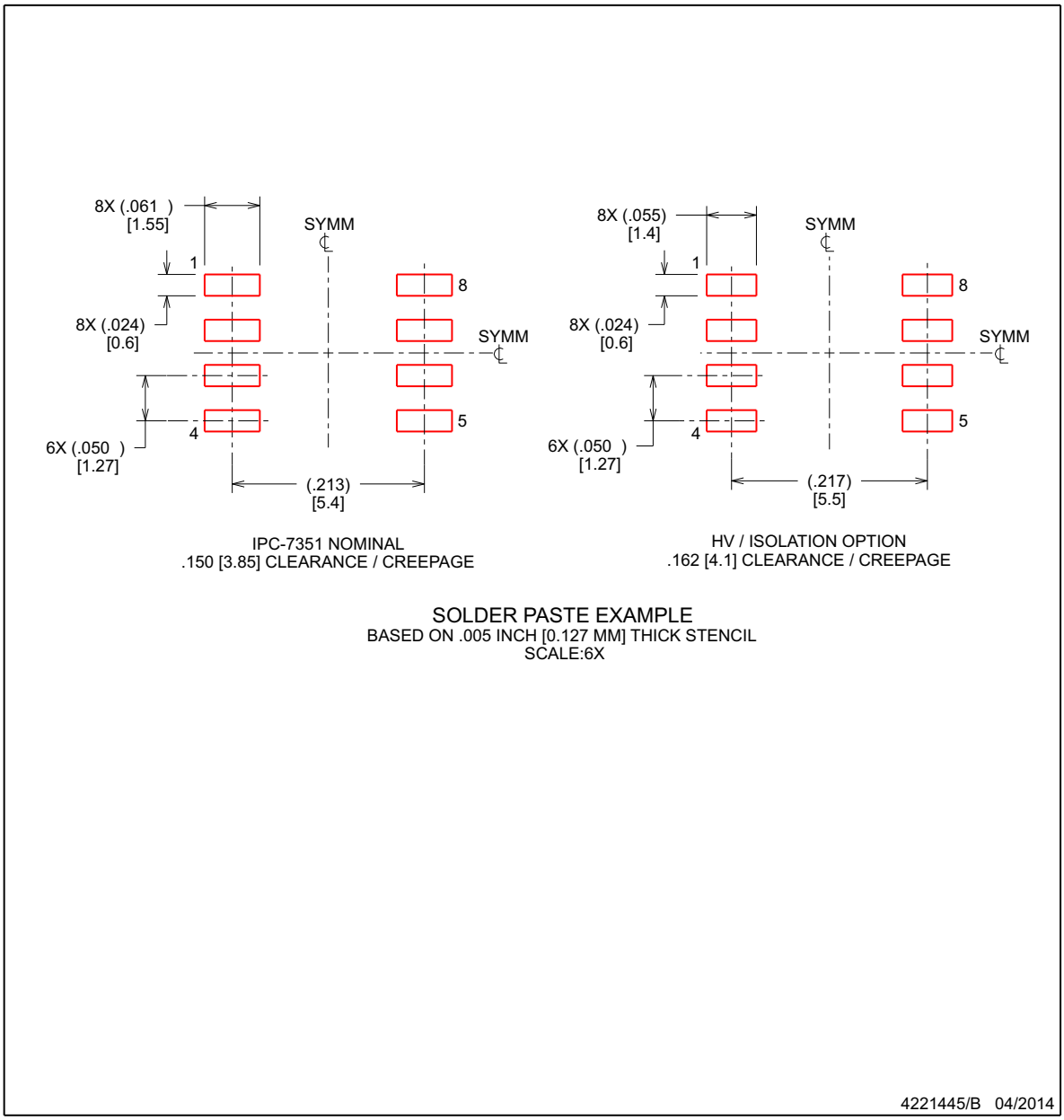
EXAMPLE STENCIL DESIGN

D0008B — **SOIC - 1.75 mm max height**

SOIC



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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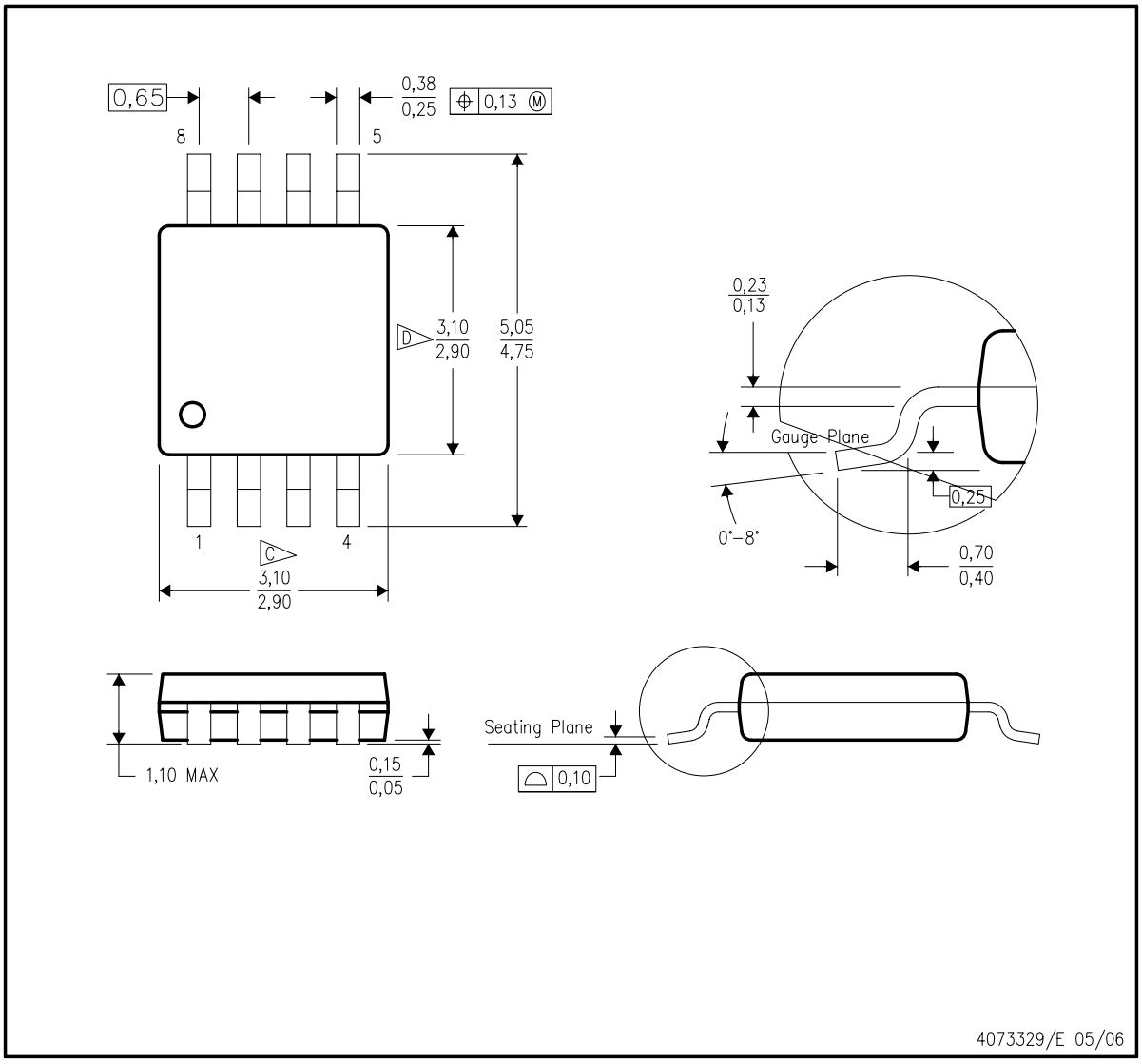
MECHANICAL DATA

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

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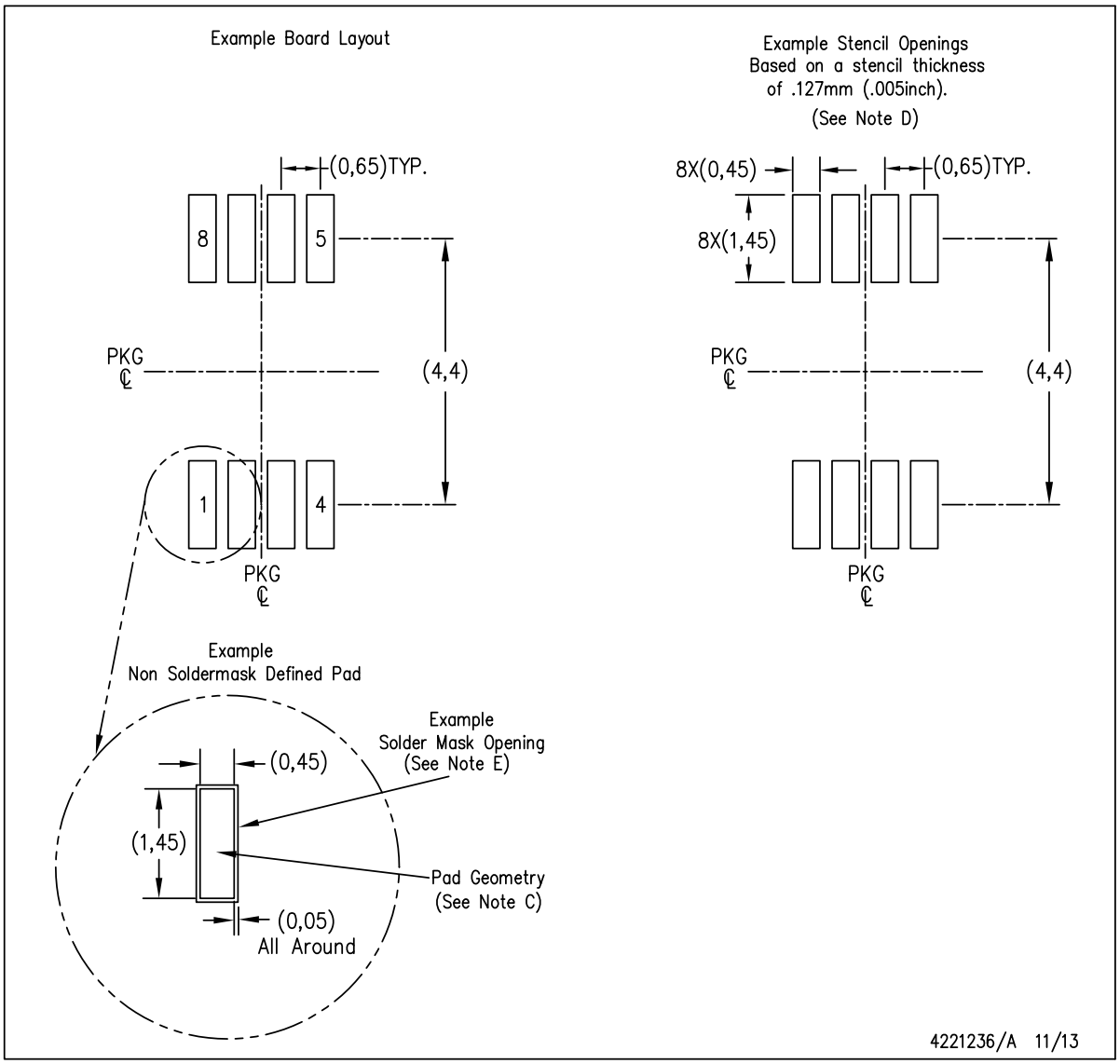
LAND PATTERN DATA

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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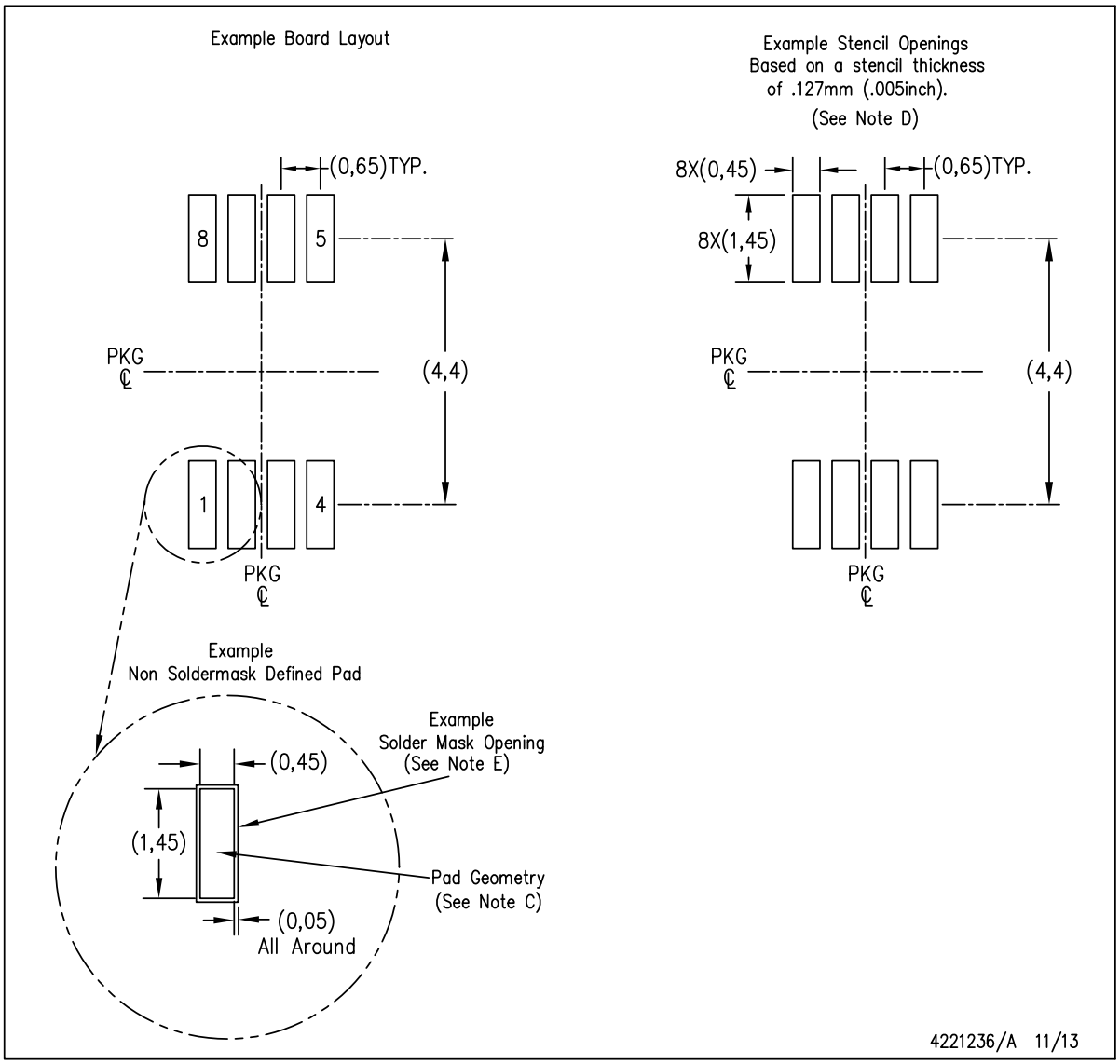
LAND PATTERN DATA

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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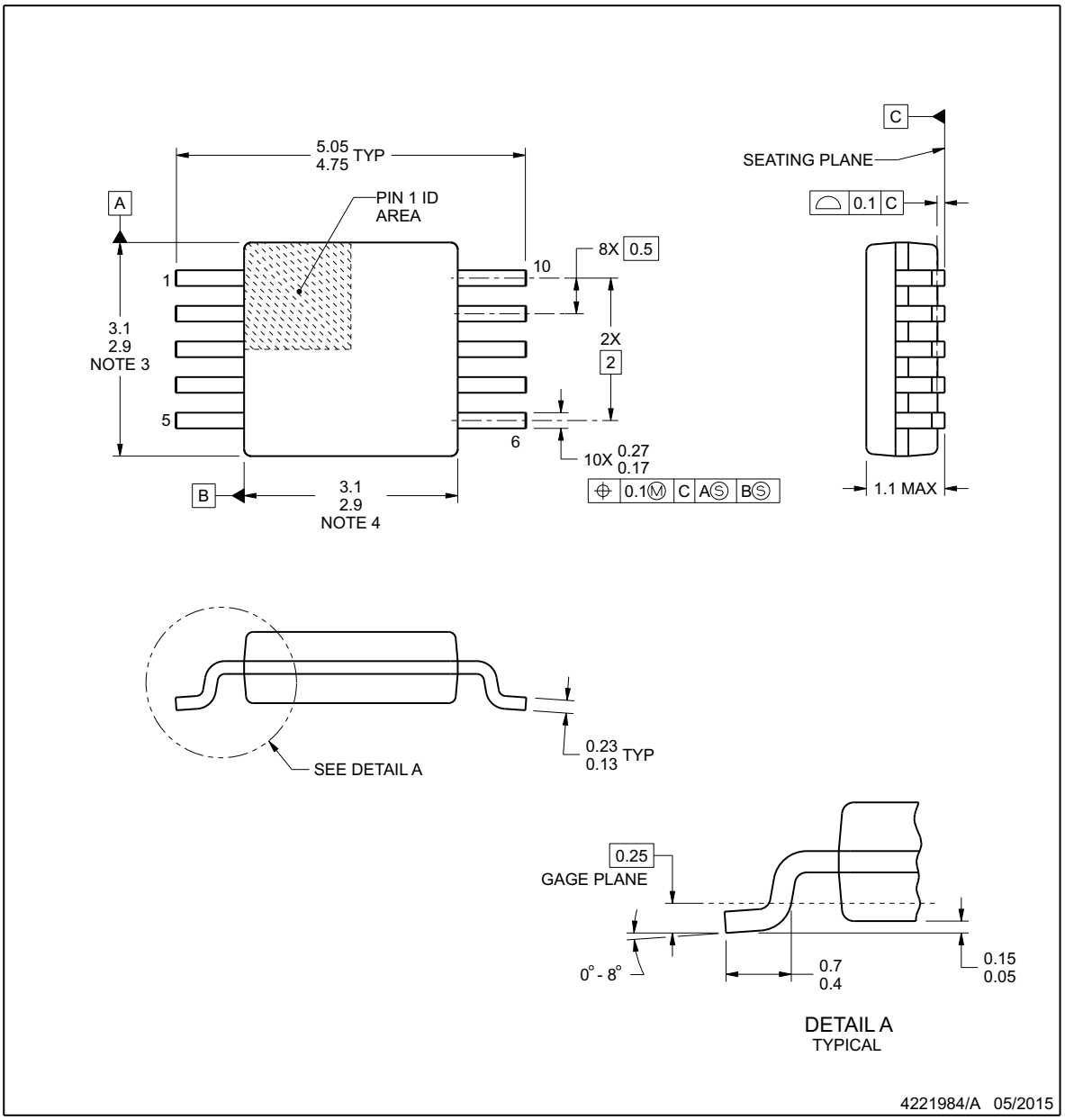
PACKAGE OUTLINE

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

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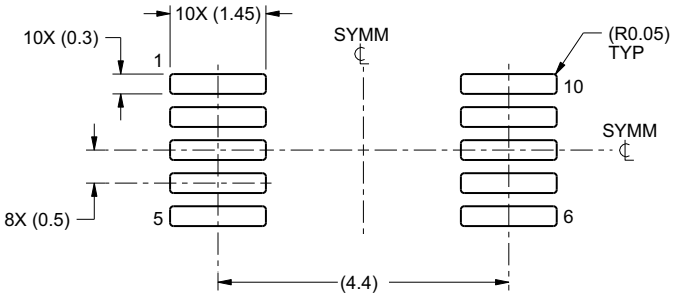
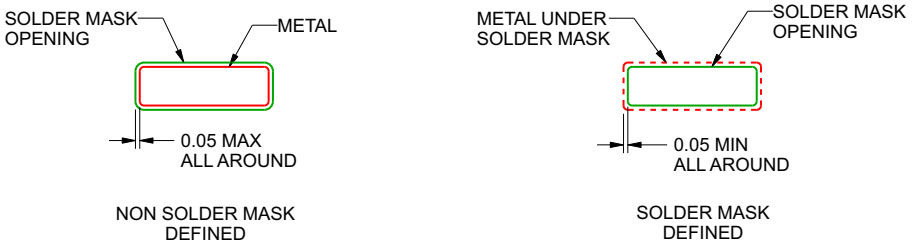
EXAMPLE BOARD LAYOUT

DGS0010A — **VSSOP - 1.1 mm max height**

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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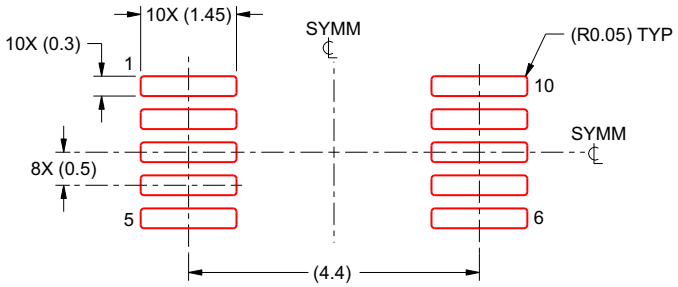
EXAMPLE STENCIL DESIGN

DGS0010A — **VSSOP - 1.1 mm max height**

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THVD1510D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VD1510
THVD1510D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VD1510
THVD1510DGK	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1510
THVD1510DGK.A	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1510
THVD1510DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1510
THVD1510DGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1510
THVD1510DGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1510
THVD1510DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VD1510
THVD1510DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VD1510
THVD1512DGS	Active	Production	VSSOP (DGS) | 10	80 | TUBE	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1512
THVD1512DGS.A	Active	Production	VSSOP (DGS) | 10	80 | TUBE	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1512
THVD1512DGSR	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 125	1512
THVD1512DGSR.A	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1512
THVD1512DGSR.B	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1512
THVD1550D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VD1550
THVD1550D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VD1550
THVD1550DGK	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1550
THVD1550DGK.A	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1550
THVD1550DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1550
THVD1550DGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1550
THVD1550DGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1550
THVD1550DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VD1550
THVD1550DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VD1550
THVD1550DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VD1550
THVD1550DRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VD1550
THVD1551DGK	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1551
THVD1551DGK.A	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1551

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THVD1551DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1551
THVD1551DGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1551
THVD1551DGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1551
THVD1552D	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1552
THVD1552D.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1552
THVD1552DGS	Active	Production	VSSOP (DGS) | 10	80 | TUBE	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1552
THVD1552DGS.A	Active	Production	VSSOP (DGS) | 10	80 | TUBE	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1552
THVD1552DGS.B	Active	Production	VSSOP (DGS) | 10	80 | TUBE	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1552
THVD1552DGSR	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 125	1552
THVD1552DGSR.A	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1552
THVD1552DGSR.B	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1552
THVD1552DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1552
THVD1552DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1552

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

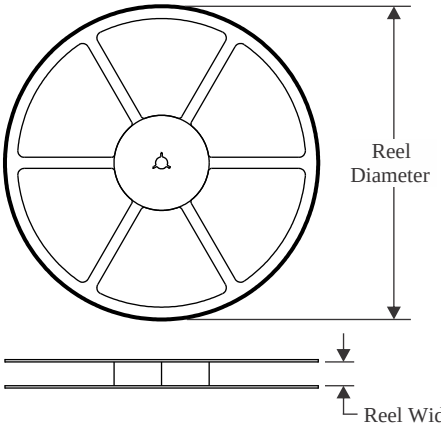
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

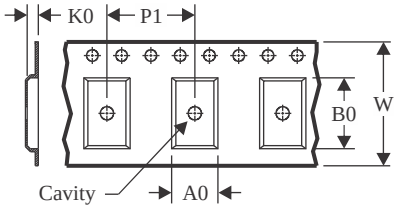
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

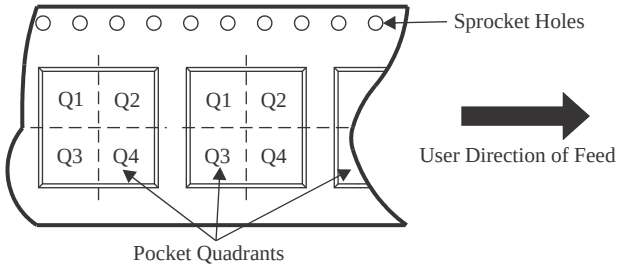


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

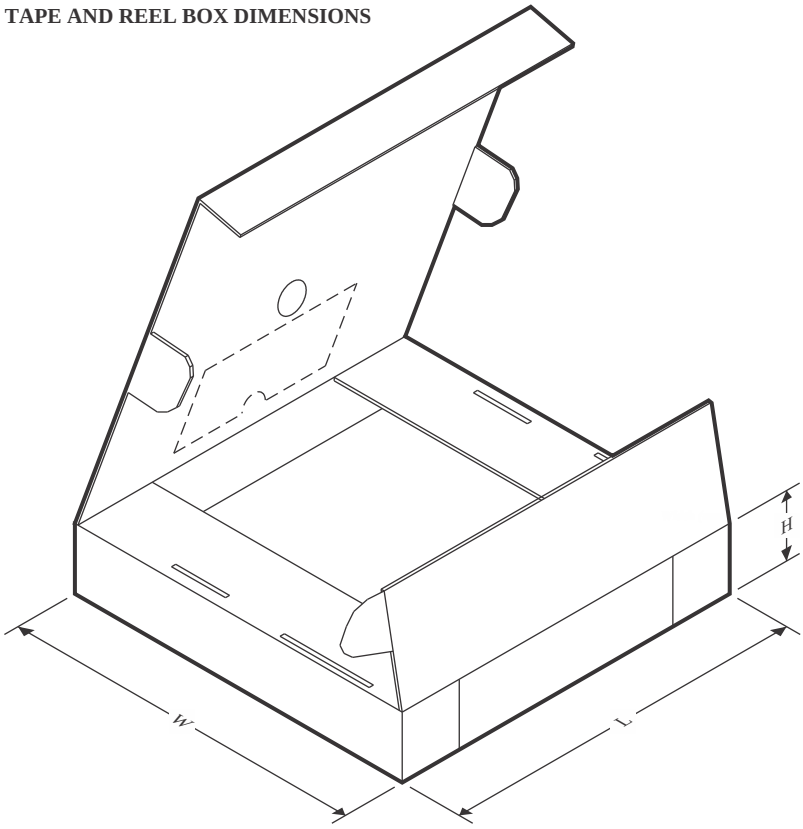
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THVD1510DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THVD1510DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THVD1512DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
THVD1550DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THVD1550DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THVD1550DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THVD1551DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THVD1551DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THVD1552DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
THVD1552DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

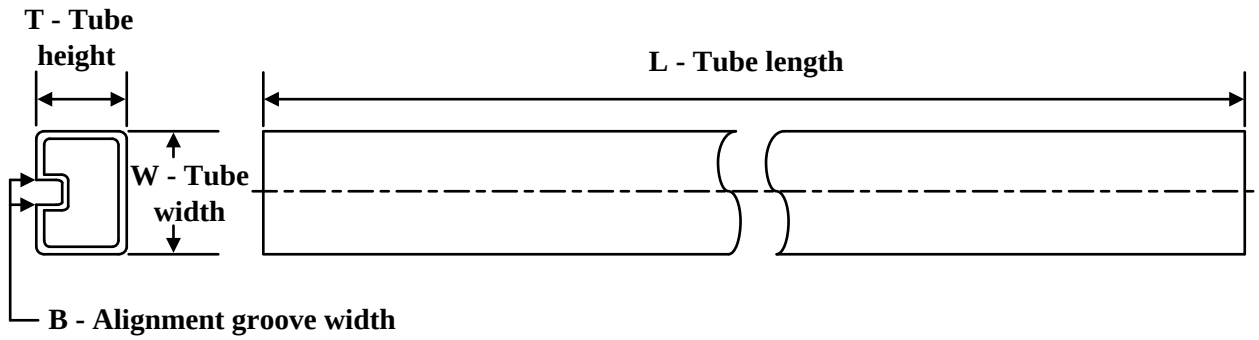
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THVD1510DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
THVD1510DR	SOIC	D	8	2500	353.0	353.0	32.0
THVD1512DGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
THVD1550DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
THVD1550DR	SOIC	D	8	2500	353.0	353.0	32.0
THVD1550DRG4	SOIC	D	8	2500	353.0	353.0	32.0
THVD1551DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
THVD1551DGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
THVD1552DGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
THVD1552DR	SOIC	D	14	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
THVD1510D	D	SOIC	8	75	507	8	3940	4.32
THVD1510D.A	D	SOIC	8	75	507	8	3940	4.32
THVD1510DGK	DGK	VSSOP	8	80	330	6.55	500	2.88
THVD1510DGK.A	DGK	VSSOP	8	80	330	6.55	500	2.88
THVD1512DGS	DGS	VSSOP	10	80	330	6.55	500	2.88
THVD1512DGS.A	DGS	VSSOP	10	80	330	6.55	500	2.88
THVD1550D	D	SOIC	8	75	507	8	3940	4.32
THVD1550D.A	D	SOIC	8	75	507	8	3940	4.32
THVD1550DGK	DGK	VSSOP	8	80	330	6.55	500	2.88
THVD1550DGK.A	DGK	VSSOP	8	80	330	6.55	500	2.88
THVD1551DGK	DGK	VSSOP	8	80	274	6.55	500	2.88
THVD1551DGK.A	DGK	VSSOP	8	80	274	6.55	500	2.88
THVD1552D	D	SOIC	14	50	507	8	3940	4.32
THVD1552D.A	D	SOIC	14	50	507	8	3940	4.32
THVD1552DGS	DGS	VSSOP	10	80	330	6.55	500	2.88
THVD1552DGS.A	DGS	VSSOP	10	80	330	6.55	500	2.88
THVD1552DGS.B	DGS	VSSOP	10	80	330	6.55	500	2.88

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