TL06xx 低消費電力、JFET 入力オペアンプ

1 特長

- 超低消費電力
- 標準消費電流:200µA (アンプ 1 個あたり)
- 広い同相範囲と差動電圧範囲
- 低い入力バイアスとオフセット電流
- 同相入力電圧範囲に V_{CC+} を含む
- 出力短絡保護
- 高い入力インピーダンス:JFET 入力段
- 内部周波数補償
- ラッチアップ・フリーの動作
- 高いスルーレート:3.5V/µs (標準値)
- MIL-PRF-38535 準拠の製品については、特に記述のない限り、すべてのパラメータはテスト済みです。その他のすべての製品については、量産プロセスにすべてのパラメータのテストが含まれているとは限りません。

2 アプリケーション

- タブレット
- 白物家電
- パーソナル・エレクトロニクス
- コンピュータ

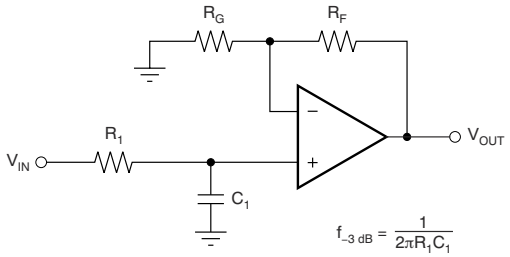
3 概要

TL06x (TL061、TL062、TL064) ファミリの業界標準オペアンプは、TL07x および TL08x ファミリのオペアンプと同様に低消費電力です。これらのデバイスは、高い入力インピーダンス、広い帯域幅、高いスルーレート、低い入力オフセットと入力バイアス電流を特長として、コスト重視のアプリケーションに優れた価値を提供します。高い ESD (1.5kV、HBM)、内蔵された EMI および RF フィルタ、広い動作温度範囲により、TL06x デバイスは、過酷で環境条件が厳しいアプリケーションで使用できます。

製品情報

部品番号	チャネル数	パッケージ (1)	パッケージ・サイズ (2)
TL061x	シングル	D (SOIC、8)	4.90mm × 6.00mm
		P (PDIP、8)	9.59mm × 7.94mm
		PS (SO、8)	6.20mm × 7.80mm
TL062x	デュアル	D (SOIC、8)	4.90mm × 6.00mm
		P (PDIP、8)	9.59mm × 7.94mm
		PS (SO、8)	6.20mm × 7.80mm
		JG (CDIP、8)	9.58mm × 7.62mm
		PW (TSSOP、8)	3.00mm × 6.40mm
		FK (LCCC、20)	8.89mm × 8.80mm
TL064x	クワッド	D (SOIC、14)	8.65mm × 6.00mm
		J (CDIP、14)	19.4mm × 7.90mm
		N (PDIP、14)	19.31mm × 7.94mm
		NS (SO、14)	10.20mm × 7.80mm
		PW (TSSOP、14)	5.00mm × 6.40mm
		W (CFP、14)	21.78mm × 9.21mm
		FK (LCCC、20)	8.89mm × 8.80mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ・サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR_1C_1}\right)$$

単極ローパス・フィルタ

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision M (June 2023) to Revision N (August 2023) — **Page**

- Added typical specification for Unity-Gain Bandwidth in *Electrical Characteristics for TL06xM* ... 10
- Changed Equivalent Input Noise Voltage vs Frequency curve in *Typical Characteristics* section ... 11

Changes from Revision L (May 2015) to Revision M (June 2023) — **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新 ... 1
- 「製品情報」をパッケージ・サイズとチャネル数で更新し、チャネル数に基づいてパッケージの順序を変更 ... 1
- Updated TL061 pinout diagram in *Pin Configuration and Functions* ... 4
- Changed Charged Device Model (CDM) ESD from 2 kV to 1.5 kV in *ESD Ratings* ... 6
- Added table note for input bias current and input offset current on *Electrical Characteristics for TL06xC and TL06xxC* ... 8
- Added table note for input bias current and input offset current on *Electrical Characteristics for TL06xxC and TL06xI* ... 9
- Changed name of *Electrical Characteristics for TL06xM and TL064M* to *Electrical Characteristics for TL06xM* ... 10
- Added table note for input bias current and input offset current on *Electrical Characteristics for TL06xM* ... 10
- Changed typical input voltage noise density at 1 kHz from 42 nV/√Hz to 30 nV/√Hz ... 10
- Updated description in *Overview* ... 15
- Updated image in *Functional Block Diagram* ... 15

Changes from Revision K (January 2014) to Revision L (May 2015) — **Page**

- 「アプリケーション」を追加 ... 1
- 「ピン構成および機能」セクション、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 ... 1

Changes from Revision J (September 2004) to Revision K (January 2014) — **Page**

- 新しいテキサス・インスツルメンツのデータシート・フォーマットにドキュメントを更新 - 仕様変更なし。 ... 1

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- 「注文情報」表を削除。 1
- 「特長」を「軍事に関する免責事項」で更新。 1

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5 Pin Configuration and Functions

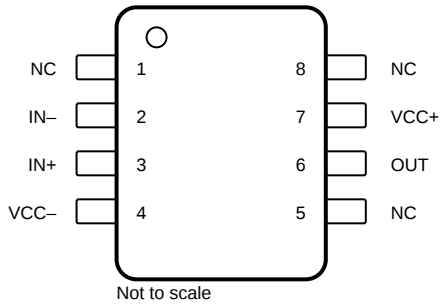


図 5-1. TL061x D, P, and PS Package, 8-Pin SOIC, PDIP, and SO (Top View)

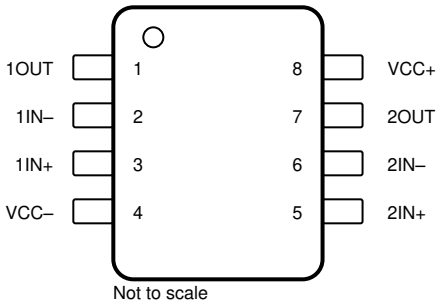


図 5-2. TL062x D, JG, P, PS, and PW Package, 8-Pin SOIC, CDIP, PDIP, SO, and TSSOP (Top View)

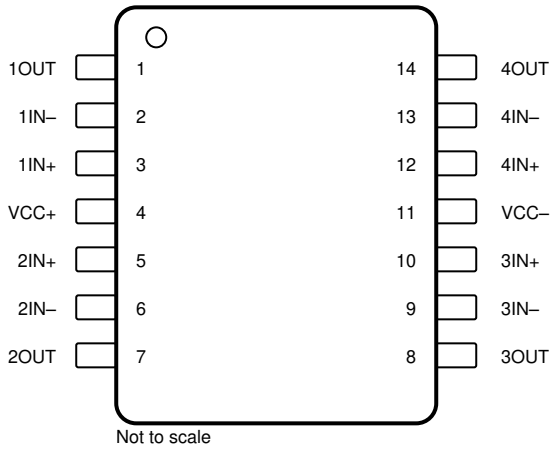


図 5-3. TL064x D, J, N, NS, PW, and W Package, 14-Pin SOIC, CDIP, PDIP, SO, TSSOP and CFP (Top View)

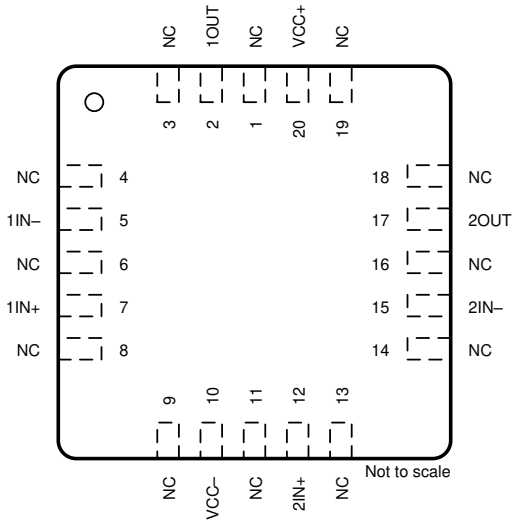


図 5-4. TL062 FK Package, 20-Pin LCCC (Top View)

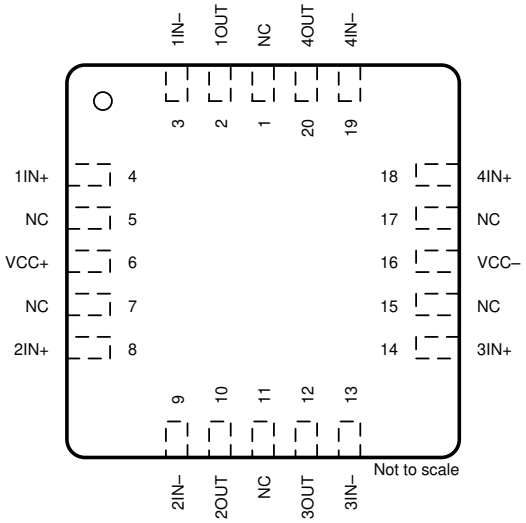


図 5-5. TL064 FK Package, 20-Pin LCCC (Top View)

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表 5-1. Pin Functions

PIN						TYPE[1]	DESCRIPTION
NAME	TL061	TL062		TL064			
	D, P, PS	D, JG, P, PS, PW	FK	D, J, N, NS, PW, W	FK		
1IN–	—	2	5	2	3	I	Negative input
1IN+	—	3	7	3	4	I	Positive input
1OUT	—	1	2	1	2	O	Output
2IN–	—	6	15	6	9	I	Negative input
2IN+	—	5	12	5	8	I	Positive input
2OUT	—	7	17	7	10	O	Output
3IN–	—	—	—	9	13	I	Negative input
3IN+	—	—	—	10	14	I	Positive input
3OUT	—	—	—	8	12	O	Output
4IN–	—	—	—	13	19	I	Negative input
4IN+	—	—	—	12	18	I	Positive input
4OUT	—	—	—	14	20	O	Output
IN–	2	—	—	—	—	I	Negative input
IN+	3	—	—	—	—	I	Positive input
NC	8	—	1	—	1	—	Do not connect
			3				
			4		5		
			6				
			8		7		
			9				
			11		11		
			13				
			14		15		
			16				
			18		17		
			19				
OFFSET N1	1	—	—	—	—	—	Input offset adjustment
OFFSET N2	5	—	—	—	—	—	Input offset adjustment
OUT	6	—	—	—	—	O	Output
$V_{CC–}$	4	4	10	11	16	—	Power supply
V_{CC+}	7	8	20	4	6	—	Power supply

(1) I = input, O = output

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC+}	Supply voltage(2)			18	V
V_{CC-}				–18	
V_{ID}	Differential input voltage(3)			±30	V
V_I	Input voltage(2) (4)			±15	V
	Duration of output short circuit(5)		Unlimited		
T_J	Operating virtual junction temperature			150	°C
	Case temperature for 60 seconds	FK package		260	°C
	Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds	J, JG, U, or W package		300	°C
	Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	D, N, NS, P, PS, or PW package		260	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
(3) Differential voltages are at IN+, with respect to IN−.
(4) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
(5) The output may be shorted to ground or to either supply. Temperature or supply voltages must be limited so that the dissipation rating is not exceeded.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC+}	Supply voltage		5	15	V
V_{CC-}	Supply voltage		–5	–15	V
V_{CM}	Common-mode voltage		V_{CC-} + 4	V_{CC+} – 4	V
T_A	Ambient temperature	TL06xM	–55	125	°C
		TL06xQ	–40	125	
		TL06xI	–40	85	
		TL06xC	0	70	

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6.4 Thermal Information (TL061)

THERMAL METRIC[1]		TL061		UNIT
		D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2] [3]	97	85	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance[4] [5]	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} – T_A)/R_{\theta JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.
(4) Maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JC}$, and T_C. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} – T_C) / R_{\theta JC}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(5) The package thermal impedance is calculated in accordance with MIL-STD-883.

6.5 Thermal Information (TL062)

THERMAL METRIC[1]		TL062						UNIT
		D (SOIC)	P (PDIP)	PS (SO)	PW (TSSOP)	FK (LCCC)	JG (CDIP)	
		8 PINS	8 PINS	8 PINS	8 PINS	20 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2] [3]	97	85	95	149	—	—	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance[4] [5]	—	—	—	—	5.61	14.5	°C/W

6.6 Thermal Information (TL064)

THERMAL METRIC[1]		TL064								UNIT
		D (SOIC)	N (PDIP)	NS (SO)	PS (SO)	PW (TSSOP)	FK (LCCC)	J (CDIP)	W (CFP)	
		14 PINS	14 PINS	14 PINS	8 PINS	14 PINS	20 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2] [3]	86	80	76	95	113	—	—	—	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance[2] [3]	—	—	—	—	—	5.61	15.05	14.65	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JC}$, and T_C. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} – T_C) / R_{\theta JC}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(3) The package thermal impedance is calculated in accordance with MIL-STD-883.

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6.7 Electrical Characteristics for TL06xC and TL06xxC

$V_{CC±}$ = ±15 V, R_L = 10 kΩ to (V_{CC+} + V_{CC-}) / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		TL061C, TL062C, TL064C			TL061AC, TL062AC, TL064AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	T_A = 25°C		3	15		3	6	mV
			T_A = Full range			20			7.5	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω, T_A = Full range			10			10		μV/°C
I_{IO} [3]	Input offset current	V_O = 0	T_A = 25°C		5	200		5	100	pA
			T_A = Full range			5			3	nA
I_{IB} [3]	Input bias current[2]	V_O = 0	T_A = 25°C		30	400		30	200	pA
			T_A = Full range			10			7	nA
V_{ICR}	Common-mode input voltage range	T_A = 25°C		±11	–12 to 15		±11	–12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ, T_A = 25°C		±10	±13.5		±10	±13.5		V
		R_L ≥ 10 kΩ, T_A = Full range		±10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ	T_A = 25°C	3	6		4	6		V/mV
			T_A = Full range	3			4			
B_1	Unity-gain bandwidth	R_L = 10 kΩ, T_A = 25°C			1			1		MHz
r_i	Input resistance	T_A = 25°C			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω, T_A = 25°C		70	86		80	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC±}/\Delta V_{IO}$)	V_{CC} = ±9 V to ±15 V, V_O = 0, R_S = 50 Ω, T_A = 25°C		70	95		80	95		dB
P_D	Total power dissipation (each amplifier)	V_O = 0, No load, T_A = 25°C			6	7.5		6	7.5	mW
I_{CC}	Supply current (each amplifier)	V_O = 0, No load, T_A = 25°C			200	250		200	250	μA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100, T_A = 25°C			120			120		dB

(1) All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for T_A is 0°C to 70°C for TL06xC, TL06xAC, and TL06xBC and –40°C to 85°C for TL06xI.
(2) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in 図 6-12. Pulse techniques are used to maintain the junction temperature as close to the ambient temperature as possible.
(3) Specified by design and characterization; not production tested.

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6.8 Electrical Characteristics for TL06xxC and TL06xI

$V_{CC±}$ = ±15 V, R_L = 10 kΩ to (V_{CC+} + $V_{CC–}$) / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		TL061BC, TL062BC, TL064BC			TL061I, TL062I, TL064I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	T_A = 25°C		2	3		3	6	mV
			T_A = Full range			5			9	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω, T_A = Full range			10			10		μV/°C
I_{IO} (3)	Input offset current	V_O = 0	T_A = 25°C		5	100		5	100	pA
			T_A = Full range			3			10	nA
I_{IB} (3)	Input bias current(2)	V_O = 0	T_A = 25°C		30	200		30	200	pA
			T_A = Full range			7			20	nA
V_{ICR}	Common-mode input voltage range	T_A = 25°C		±11	–12 to 15		±11	–12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ, T_A = 25°C		±10	±13.5		±10	±13.5		V
		R_L ≥ 10 kΩ, T_A = Full range		±10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ	T_A = 25°C	4	6		4	6		V/mV
			T_A = Full range	4			4			
B_1	Unity-gain bandwidth	R_L = 10 kΩ, T_A = 25°C			1			1		MHz
r_i	Input resistance	T_A = 25°C			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω, T_A = 25°C		80	86		80	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC±}/\Delta V_{IO}$)	V_{CC} = ±9 V to ±15 V, V_O = 0, R_S = 50 Ω, T_A = 25°C		80	95		80	95		dB
P_D	Total power dissipation (each amplifier)	V_O = 0, No load, T_A = 25°C			6	7.5		6	7.5	mW
I_{CC}	Supply current (each amplifier)	V_O = 0, No load, T_A = 25°C			200	250		200	250	μA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100, T_A = 25°C			120			120		dB

(1) All characteristics are measured under open-loop conditions with zero common-mode input voltage, unless otherwise specified. Full range for T_A is 0°C to 70°C for TL06xC, TL06xAC, and TL06xBC and –40°C to 85°C for TL06xI.
(2) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in 図 6-12. Pulse techniques are used to maintain the junction temperature as close to the ambient temperature as possible.
(3) Assured by design and characterization; not production tested.

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6.9 Electrical Characteristics for TL06xM

$V_{CC±}$ = ±15 V, R_L = 10 kΩ to (V_{CC+} + $V_{CC–}$) / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS[2]		TL061M, TL062M			TL064M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	T_A = 25°C		3	6		3	9	mV
			T_A = –55°C to 125°C			9			15	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω, T_A = –55°C to 125°C			10			10		µV/°C
I_{IO} [4]	Input offset current	V_O = 0	T_A = 25°C		5	100		5	100	pA
			T_A = –55°C			20[1]			20[1]	nA
			T_A = 125°C			20			20	
I_{IB} [4]	Input bias current[3]	V_O = 0	T_A = 25°C		30	200		30	200	pA
			T_A = –55°C			50[1]			50[1]	nA
			T_A = 125°C			50			50	
V_{ICR}	Common-mode input voltage range	T_A = 25°C		±11	–12 to 15		±11	–12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ, T_A = 25°C		±10	±13.5		±10	±13.5		V
		R_L ≥ 10 kΩ, T_A = –55°C to 125°C		±10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ	T_A = 25°C	4	6		4	6		V/mV
			T_A = –55°C to 125°C	4			4			
B_1	Unity-gain bandwidth	R_L = 10 kΩ, T_A = 25°C			1			1		MHz
r_i	Input resistance	T_A = 25°C			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω, T_A = 25°C		80	86		80	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC±}/\Delta V_{IO}$)	V_{CC} = ±9 V to ±15 V, V_O = 0, R_S = 50 Ω, T_A = 25°C		80	95		80	95		dB
P_D	Total power dissipation (each amplifier)	V_O = 0, No load, T_A = 25°C			6	7.5		6	7.5	mW
I_{CC}	Supply current (each amplifier)	V_O = 0, No load, T_A = 25°C			200	250		200	250	µA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100, T_A = 25°C			120			120		dB

(1) This parameter is not production tested.
(2) All characteristics are measured under open-loop conditions, with zero common-mode voltage, unless otherwise specified.
(3) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in 図 6-12. Pulse techniques are used to maintain the junction temperature as close to the ambient temperature as possible.
(4) Specified by design and characterization; not production tested.

6.10 Operating Characteristics

$V_{CC±}$ = ±15 V, T_A= 25°C, R_L = 10 kΩ to (V_{CC+} + $V_{CC–}$) / 2

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain[1]	V_I = 10 V, R_L = 10 kΩ,	C_L = 100 pF, see 図 7-1	1.5	3.5		V/µs
t_r	Rise-time	V_I = 20 V, R_L = 10 kΩ,	C_L = 100 pF, see 図 7-1		0.2		µs
	Overshoot factor				10%		
V_n	Equivalent input noise voltage	R_S = 20 Ω	f = 1 kHz		30		nV/√Hz

(1) Slew rate at –55°C to 125°C is 0.7 V/µs min.

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Typical Characteristics

Data at high and low temperatures are applicable only within the specified operating free-air temperature ranges of the various devices.

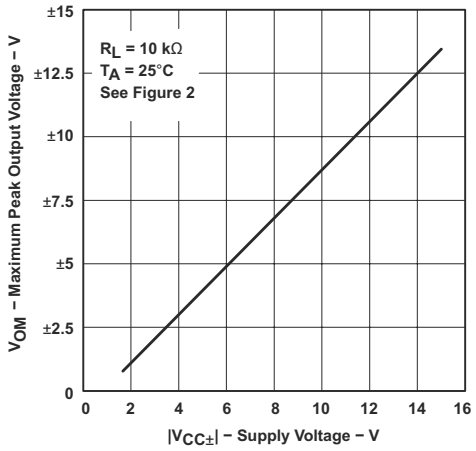


図 6-1. Maximum Peak Output Voltage vs Supply Voltage

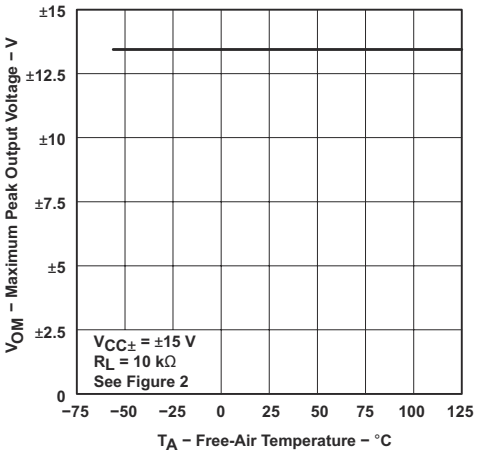


図 6-2. Maximum Peak Output Voltage vs Free-Air Temperature

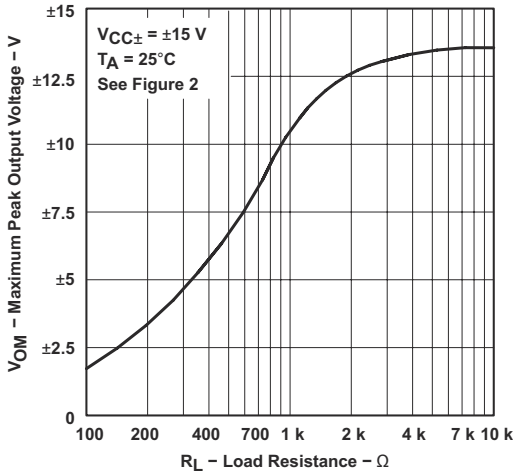


図 6-3. Maximum Peak Output Voltage vs Load Resistance

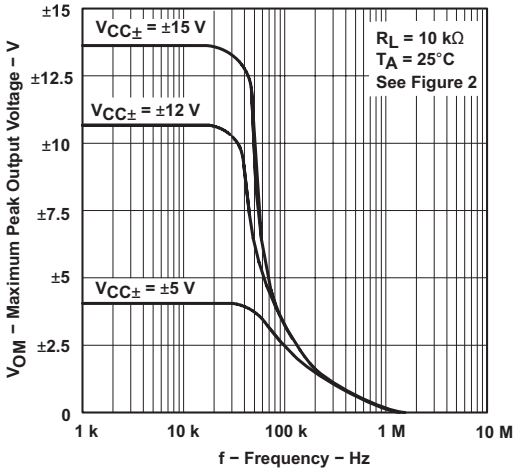


図 6-4. Maximum Peak Output Voltage vs Frequency

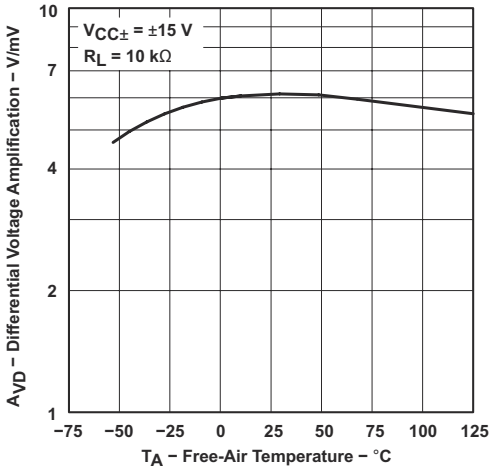


図 6-5. Differential Voltage Amplification vs Free-Air Temperature

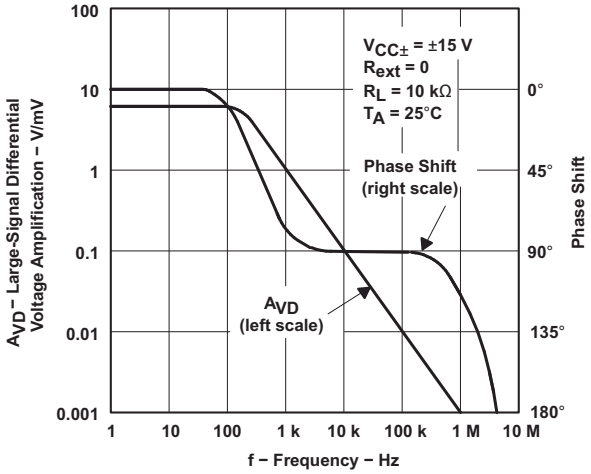


図 6-6. Large-Signal Differential Voltage Amplification and Phase Shift vs Frequency

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Typical Characteristics (continued)

Data at high and low temperatures are applicable only within the specified operating free-air temperature ranges of the various devices.

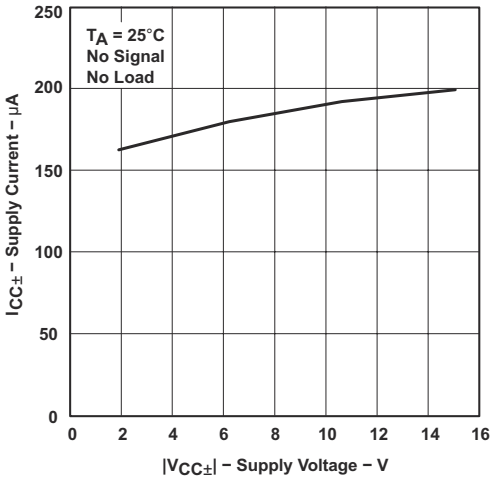


図 6-7. Supply Current vs Supply Voltage

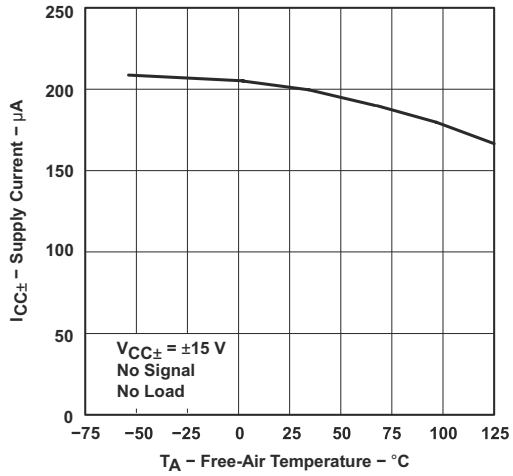


図 6-8. Supply Current vs Free-Air Temperature

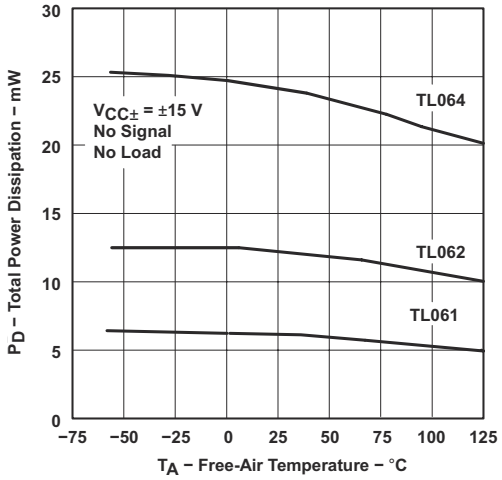


図 6-9. Total Power Dissipation vs Free-Air Temperature

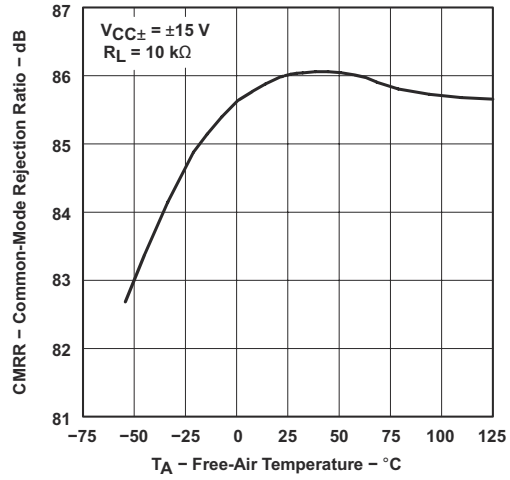


図 6-10. All Except TL06_C Common-Mode Rejection Ratio vs Free-Air Temperature

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Typical Characteristics (continued)

Data at high and low temperatures are applicable only within the specified operating free-air temperature ranges of the various devices.

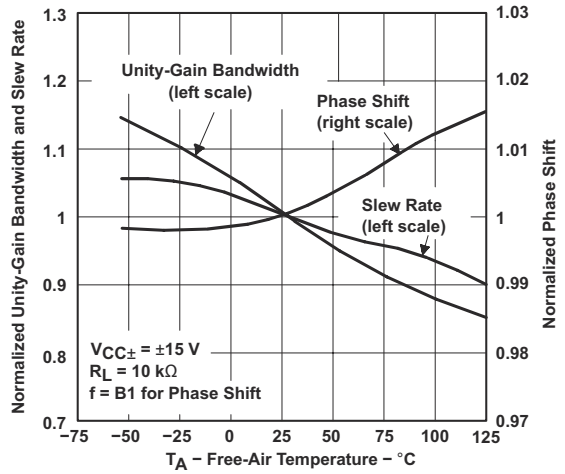


図 6-11. Normalized Unity-Gain Bandwidth, Slew Rate, and Phase Shift vs Free-Air Temperature

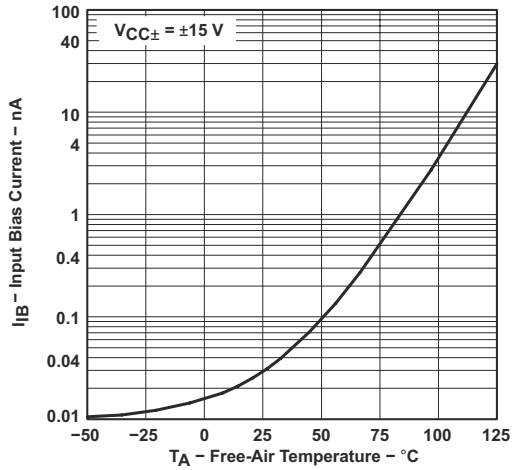


図 6-12. Input Bias Current vs Free-Air Temperature

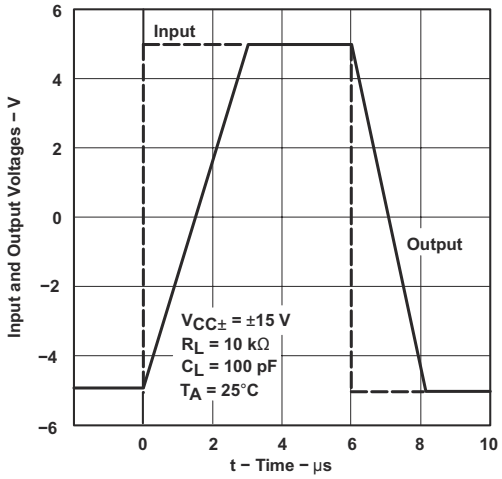


図 6-13. Voltage-Follower Large-Signal Pulse Response vs Time

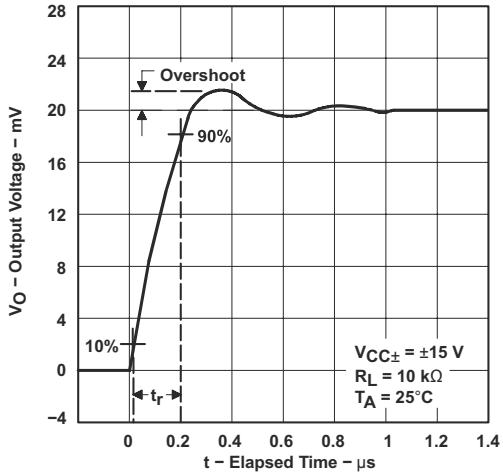


図 6-14. Output Voltage vs Elapsed Time

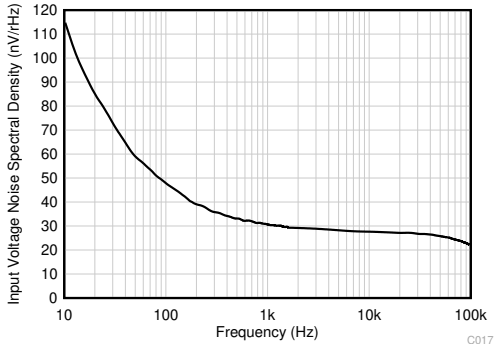


図 6-15. Equivalent Input Noise Voltage vs Frequency

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7 Parameter Measurement Information

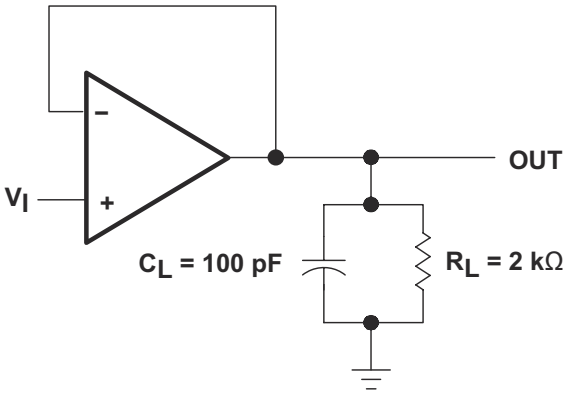


図 7-1. Unity-Gain Amplifier

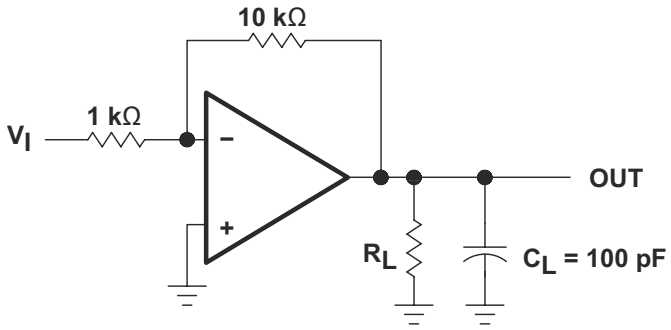


図 7-2. Gain-of-10 Inverting Amplifier

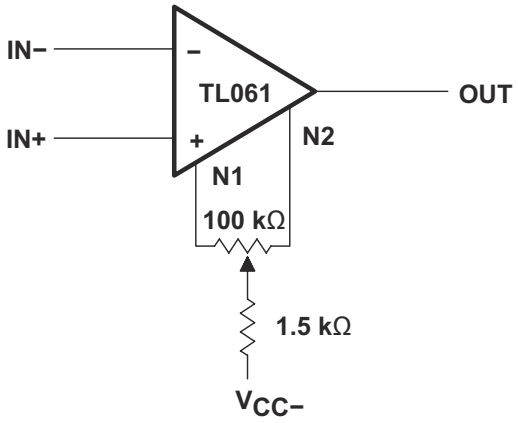


図 7-3. Input Offset-Voltage Null Circuit

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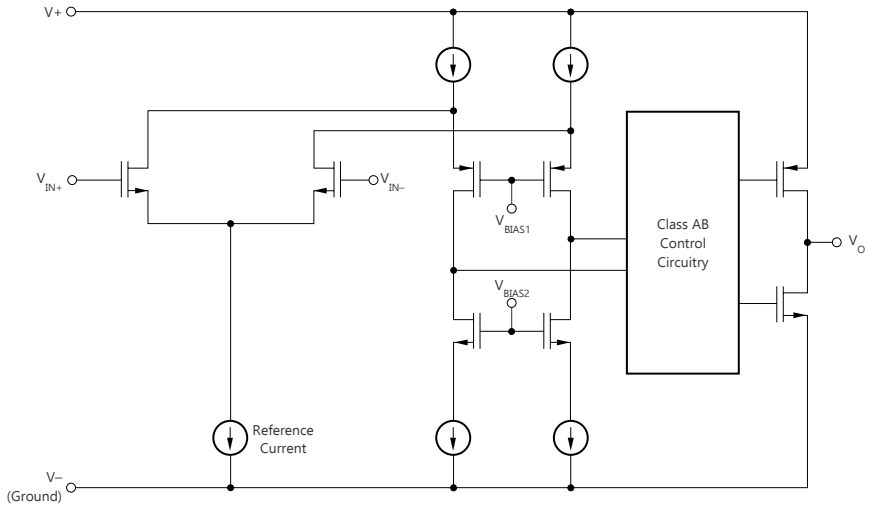
8 Detailed Description

8.1 Overview

The TL06x (TL061, TL062, and TL064) family of industry-standard operational amplifiers (op amps) mirror the TL07x and TL08x family of op amps with lower power consumption. These devices provide outstanding value for cost-sensitive applications, featuring high input impedance, wide bandwidth, high slew rate, and low input offset and input bias currents. High ESD (1.5 kV, HBM), integrated EMI and RF filters, and wide temperature operation enable the TL06x devices to be used in rugged and environmentally-demanding applications.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from −40°C to 85°C, and the M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Common-Mode Rejection Ratio

The common-mode rejection ratio (CMRR) of an amplifier is a measure of how well the device rejects unwanted input signals common to both input leads. It is found by taking the ratio of the change in input offset voltage to the change in the input voltage and converting to decibels. Ideally the CMRR is infinite, but in practice, amplifiers are designed to have it as high as possible. The CMRR of this device is 86 dB.

8.3.2 Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. These devices have a 3.5-V/µs slew rate.

8.4 Device Functional Modes

These devices are powered on when the supply is connected. This device can be operated as a single supply operational amplifier or dual supply amplifier depending on the application.

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9 Applications and Implementation

注

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9.1 Application Information

The TL06x series of operational amplifiers can be used in countless applications. The few applications in this section show principles used in all applications of these parts.

9.2 Typical Applications

9.2.1 Inverting Amplifier Application

A typical application for an operational amplifier in an inverting amplifier. This amplifier takes a positive voltage on the input, and makes it a negative voltage of the same magnitude. In the same manner, it also makes negative voltages positive.

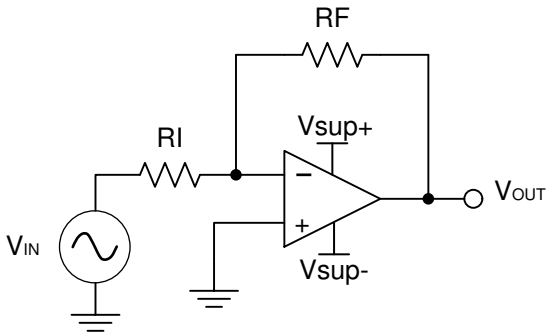


図 9-1. Schematic for Inverting Amplifier Application

9.2.1.1 Design Requirements

The supply voltage must be chosen such that it is larger than the input voltage range and output range. For instance, this application will scale a signal of ±0.5 V to ±1.8 V. Setting the supply at ±12 V is sufficient to accommodate this application.

9.2.1.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier:

$$A_V = \frac{VOUT}{VIN} \quad (1)$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \quad (2)$$

Once the desired gain is determined, choose a value for RI or RF. Choose a value in the kΩ range to limit currents in the amplifier circuit to the mA range. This example will choose 10 kΩ for RI which means 36 kΩ will be used for RF. This was determined by Equation 3.

$$A_V = -\frac{RF}{RI} \quad (3)$$

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9.2.1.3 Application Curve

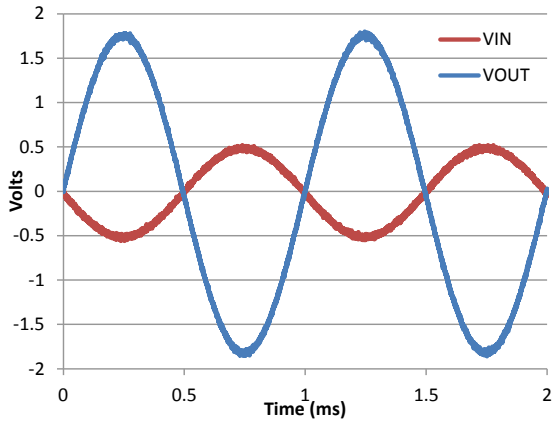


図 9-2. Input and Output Voltages of the Inverting Amplifier

9.3 System Examples

9.3.1 General Applications

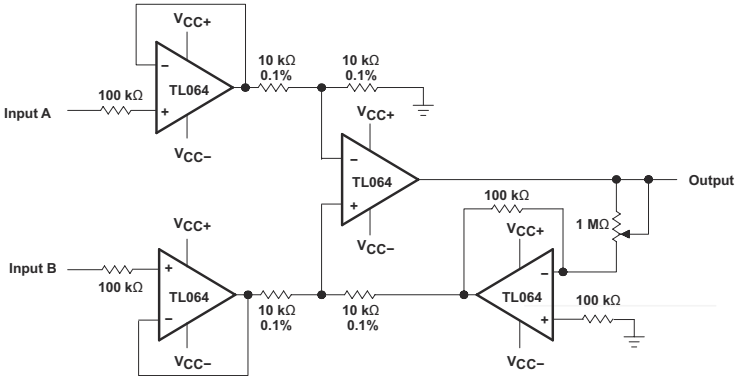


図 9-3. Instrumentation Amplifier

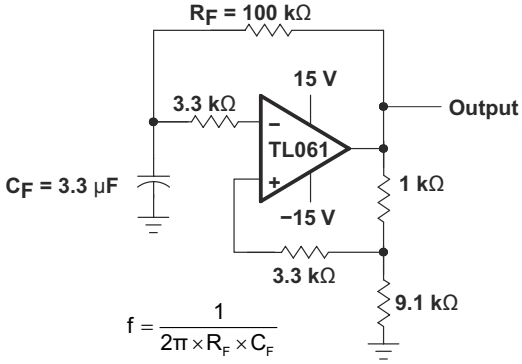


図 9-4. 0.5-Hz Square-Wave Oscillator

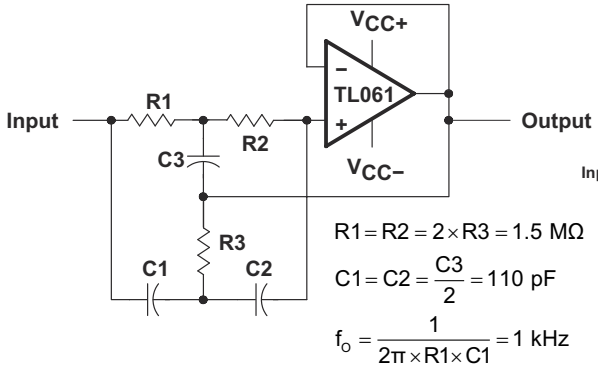


図 9-5. High-Q Notch Filter

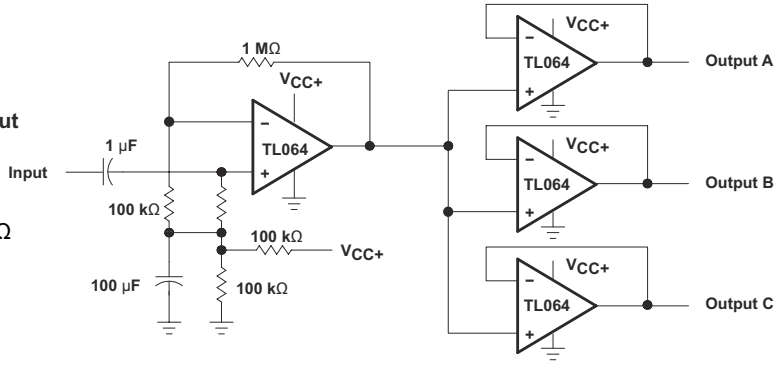


図 9-6. Audio-Distribution Amplifier

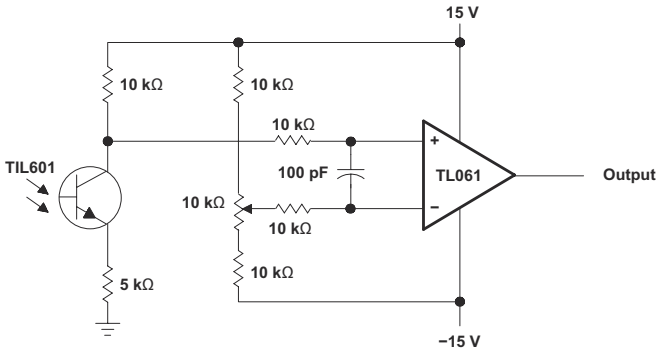


図 9-7. Low-Level Light Detector Preamplifier

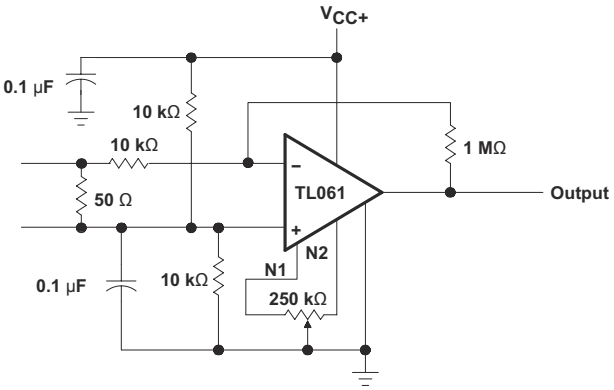


図 9-8. AC Amplifier

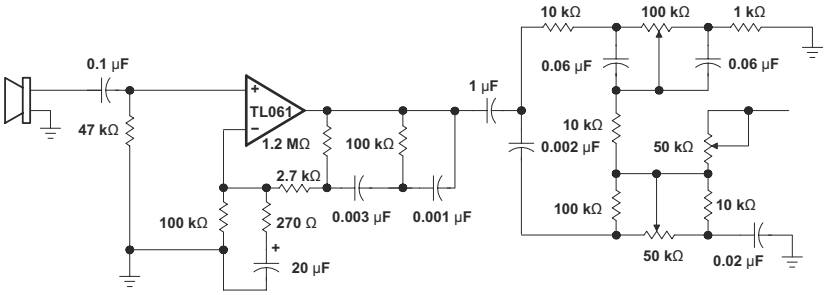


図 9-9. Microphone Preamplifier With Tone Control

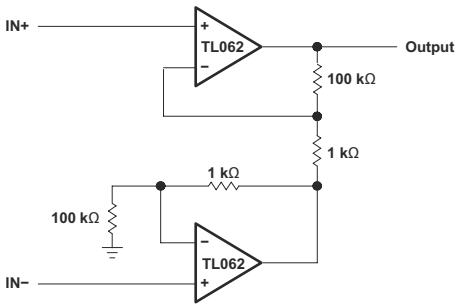


図 9-10. Instrumentation Amplifier

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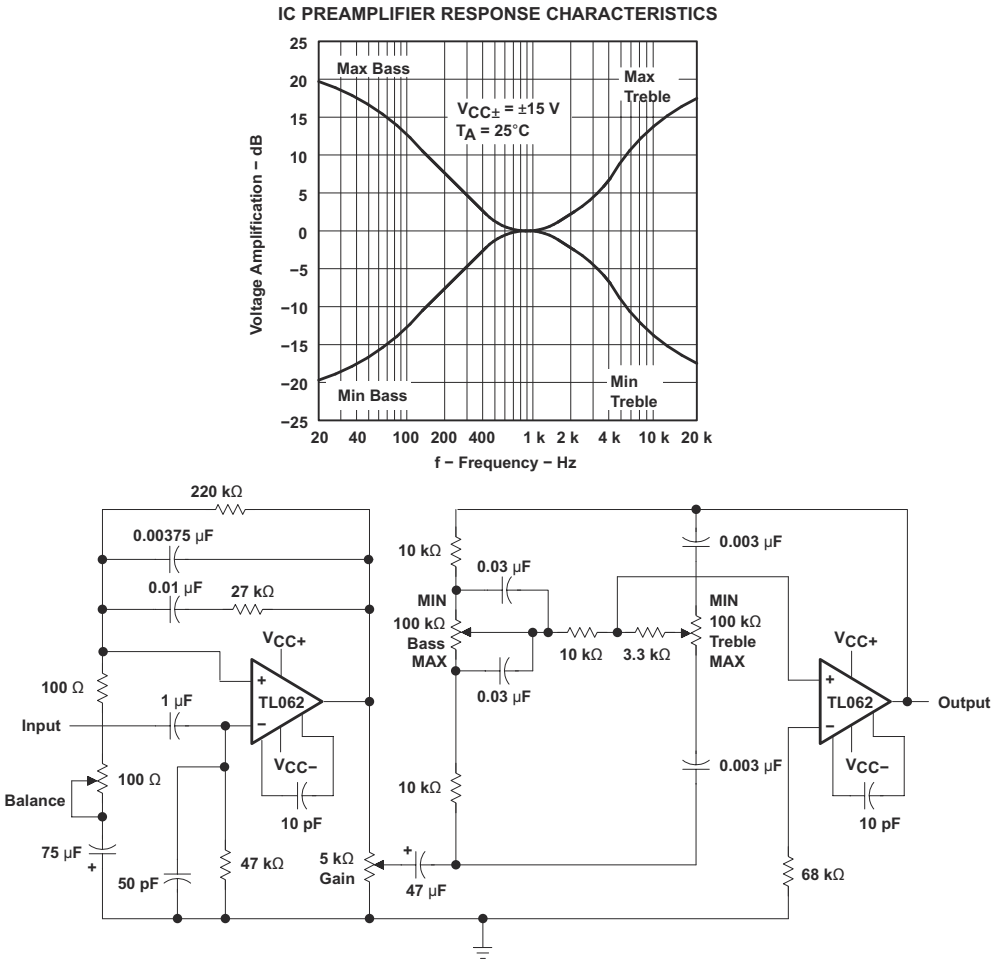


図 9-11. IC Preamplifier

9.4 Power Supply Recommendations

> **注意**
>
> Supply voltages larger than 36 V for a single supply, or outside the range of ±18 V for a dual supply can permanently damage the device (see the *Absolute Maximum Ratings*).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout* section.

9.5 Layout

9.5.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, refer to *Circuit Board Layout Techniques*.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in *Layout Examples*.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

9.5.2 Layout Examples

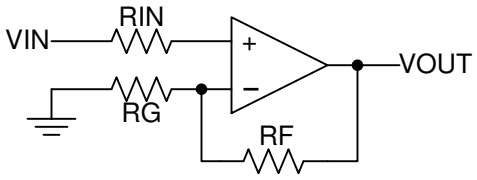


図 9-12. Operational Amplifier Schematic for Noninverting Configuration

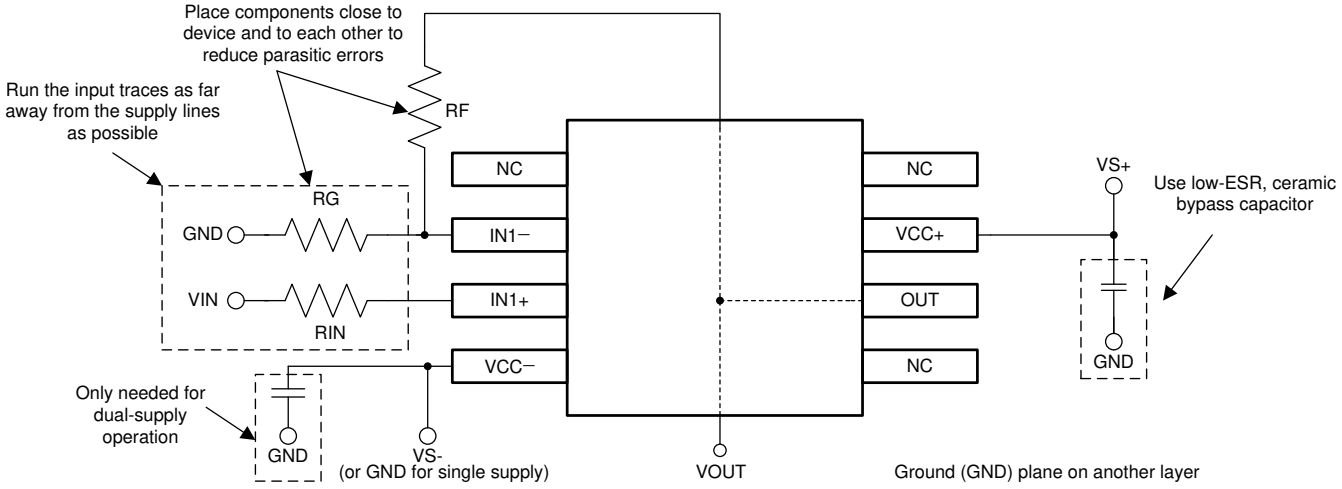


図 9-13. Operational Amplifier Board Layout for Noninverting Configuration

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10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Circuit Board Layout Techniques* chapter extracts

10.2 サポート・リソース

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10.4 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
81023022A	LIFEBUY	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	81023022A TL062MFKB	
8102302PA	ACTIVE	CDIP	JG	8	50	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102302PA TL062M	Samples
81023032A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	81023032A TL064MFKB	Samples
8102303CA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102303CA TL064MJB	Samples
8102303DA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102303DA TL064MWB	Samples
TL061ACD	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	061AC	
TL061ACDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	061AC	Samples
TL061ACP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL061ACP	Samples
TL061BCP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL061BCP	Samples
TL061BCPE4	ACTIVE	PDIP	P	8	50	TBD	Call TI	Call TI	0 to 70		Samples
TL061CD	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL061C	
TL061CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL061C	Samples
TL061CP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL061CP	Samples
TL061CPSR	LIFEBUY	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T061	
TL061ID	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL061I	
TL061IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL061I	Samples
TL061IDRG4	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 85		Samples
TL061IP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TL061IP	Samples
TL061IPE4	ACTIVE	PDIP	P	8	50	TBD	Call TI	Call TI	-40 to 85		Samples
TL062ACD	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	062AC	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL062ACDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	062AC	Samples
TL062ACDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	062AC	Samples
TL062ACP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL062ACP	Samples
TL062ACPSR	LIFEBUY	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T062A	
TL062BCD	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	062BC	
TL062BCDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	062BC	Samples
TL062BCP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL062BCP	Samples
TL062CD	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL062C	
TL062CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL062C	Samples
TL062CDRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL062C	Samples
TL062CDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL062C	Samples
TL062CP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL062CP	Samples
TL062CPE4	ACTIVE	PDIP	P	8	50	TBD	Call TI	Call TI	0 to 70		Samples
TL062CPS	LIFEBUY	SO	PS	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T062	
TL062CPSR	LIFEBUY	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T062	
TL062CPW	LIFEBUY	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T062	
TL062CPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T062	Samples
TL062CPWRG4	LIFEBUY	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T062	
TL062ID	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL062I	
TL062IDG4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL062I	
TL062IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL062I	Samples
TL062IP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TL062IP	Samples
TL062IPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z062	Samples
TL062IPWRG4	ACTIVE	TSSOP	PW	8	2000	TBD	Call TI	Call TI	-40 to 85		Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL062MFKB	LIFEBUY	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	81023022A TL062MFKB	
TL062MJG	ACTIVE	CDIP	JG	8	50	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	TL062MJG	Samples
TL062MJGB	ACTIVE	CDIP	JG	8	50	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102302PA TL062M	Samples
TL064ACD	LIFEBUY	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL064AC	
TL064ACDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL064AC	Samples
TL064ACN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL064ACN	Samples
TL064BCD	LIFEBUY	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL064BC	
TL064BCDG4	LIFEBUY	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL064BC	
TL064BCDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL064BC	Samples
TL064BCN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL064BCN	Samples
TL064CD	LIFEBUY	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL064C	
TL064CDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL064C	Samples
TL064CN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL064CN	Samples
TL064CNSR	LIFEBUY	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL064	
TL064CPW	LIFEBUY	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T064	
TL064CPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T064	Samples
TL064ID	LIFEBUY	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL064I	
TL064IDG4	LIFEBUY	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL064I	
TL064IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	TL064I	Samples
TL064IDRG4	LIFEBUY	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL064I	
TL064IN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TL064IN	Samples
TL064INE4	ACTIVE	PDIP	N	14	25	TBD	Call TI	Call TI	-40 to 85		Samples
TL064INS	LIFEBUY	SO	NS	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL064I	
TL064INSR	LIFEBUY	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL064I	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL064IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z064	Samples
TL064MFKB	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	81023032A TL064MFKB	Samples
TL064MJ	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	TL064MJ	Samples
TL064MJB	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102303CA TL064MJB	Samples
TL064MWB	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102303DA TL064MWB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TL062, TL062M, TL064, TL064M :

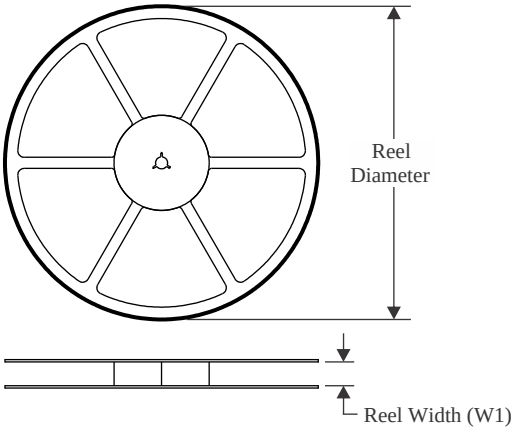
- Catalog : TL062, TL064
- Military : TL062M, TL064M

NOTE: Qualified Version Definitions:

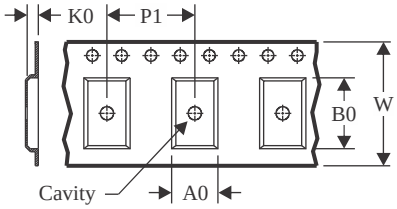
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

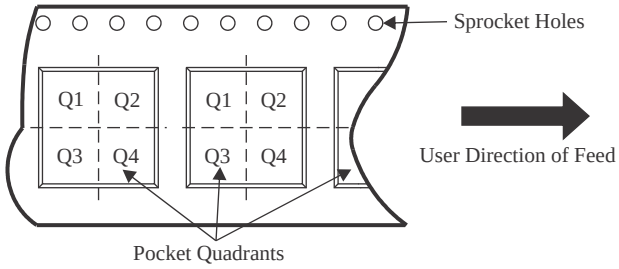


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

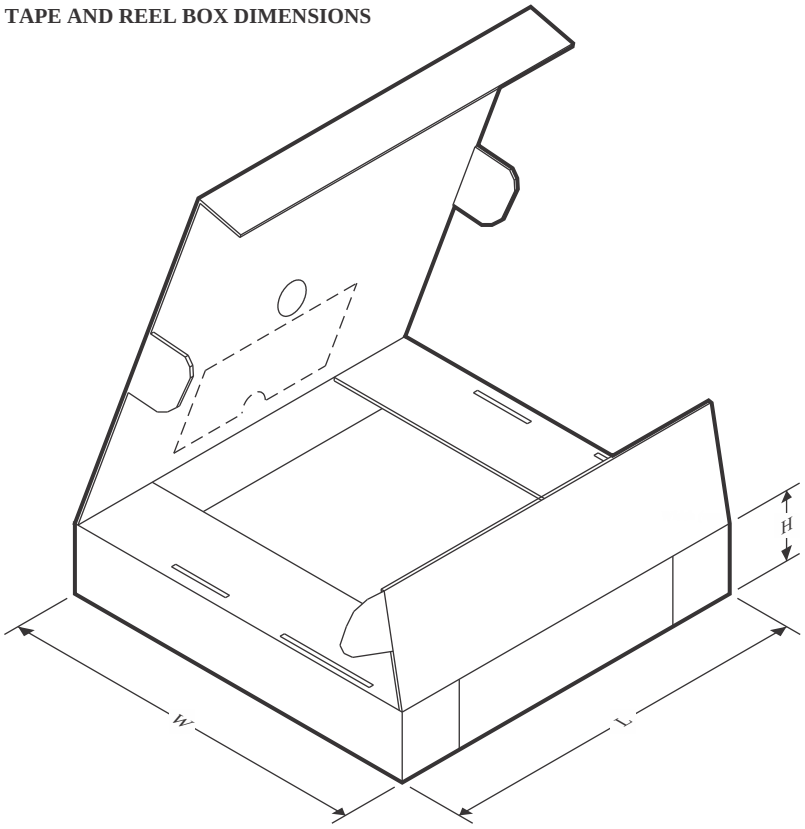


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL061ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL061CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL061CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TL061IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL062ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL062ACPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TL062BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL062CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL062CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TL062CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL062CPWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL062IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL062IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL064ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL064BCDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL064CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL064CNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TL064CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL064IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL064IDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL064INSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TL064IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

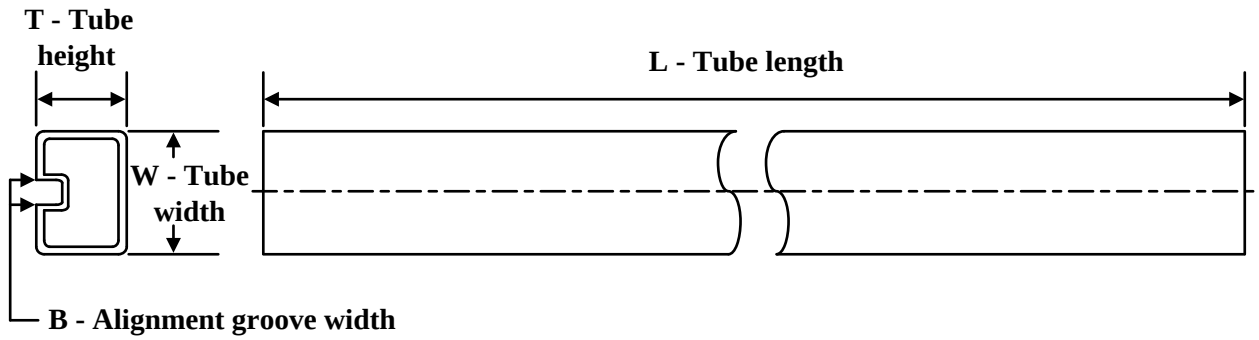


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL061ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL061CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL061CPSR	SO	PS	8	2000	356.0	356.0	35.0
TL061IDR	SOIC	D	8	2500	340.5	338.1	20.6
TL062ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL062ACPSR	SO	PS	8	2000	356.0	356.0	35.0
TL062BCDR	SOIC	D	8	2500	340.5	338.1	20.6
TL062CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL062CPSR	SO	PS	8	2000	356.0	356.0	35.0
TL062CPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
TL062CPWRG4	TSSOP	PW	8	2000	356.0	356.0	35.0
TL062IDR	SOIC	D	8	2500	340.5	338.1	20.6
TL062IPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
TL064ACDR	SOIC	D	14	2500	356.0	356.0	35.0
TL064BCDR	SOIC	D	14	2500	356.0	356.0	35.0
TL064CDR	SOIC	D	14	2500	356.0	356.0	35.0
TL064CNSR	SO	NS	14	2000	367.0	367.0	38.0
TL064CPWR	TSSOP	PW	14	2000	356.0	356.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL064IDR	SOIC	D	14	2500	356.0	356.0	35.0
TL064IDRG4	SOIC	D	14	2500	356.0	356.0	35.0
TL064INSR	SO	NS	14	2000	356.0	356.0	35.0
TL064IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

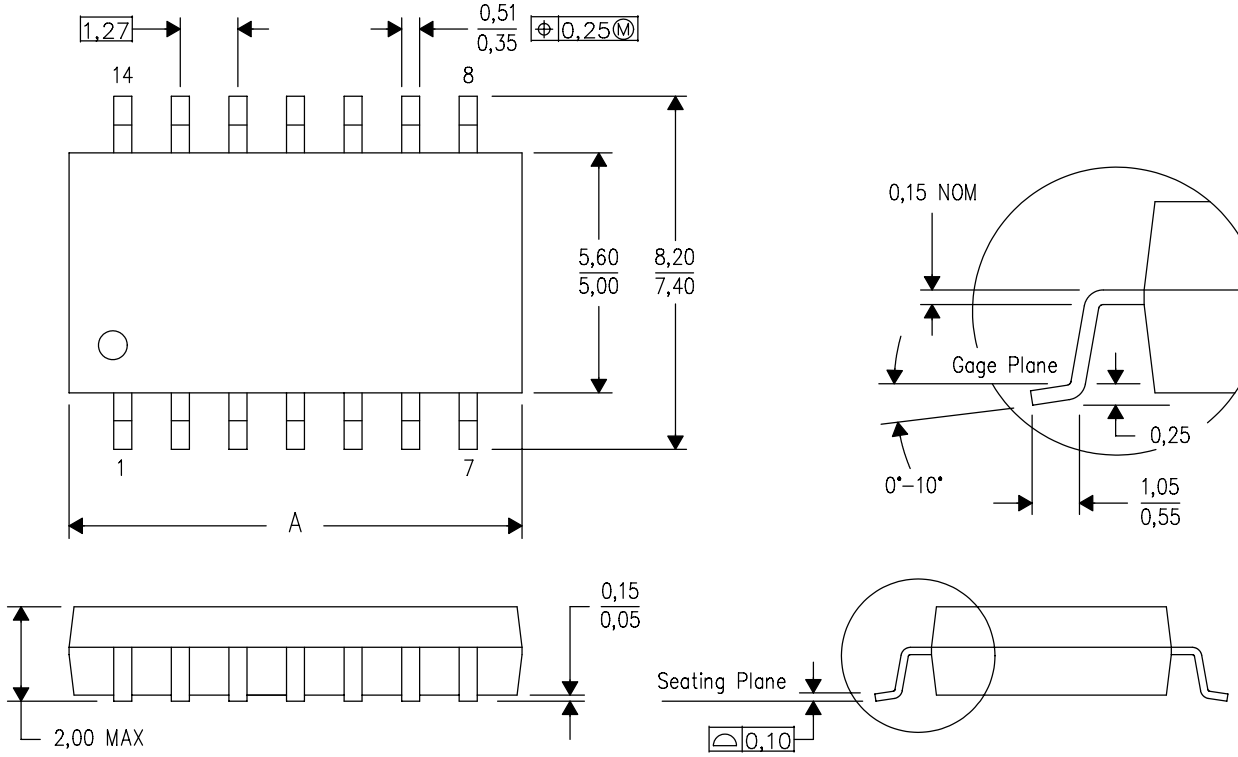
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
81023022A	FK	LCCC	20	55	506.98	12.06	2030	NA
81023032A	FK	LCCC	20	55	506.98	12.06	2030	NA
8102303DA	W	CFP	14	25	506.98	26.16	6220	NA
TL061ACD	D	SOIC	8	75	507	8	3940	4.32
TL061ACP	P	PDIP	8	50	506	13.97	11230	4.32
TL061BCP	P	PDIP	8	50	506	13.97	11230	4.32
TL061CD	D	SOIC	8	75	506.6	8	3940	4.32
TL061CD	D	SOIC	8	75	507	8	3940	4.32
TL061CP	P	PDIP	8	50	506	13.97	11230	4.32
TL061ID	D	SOIC	8	75	506.6	8	3940	4.32
TL061ID	D	SOIC	8	75	507	8	3940	4.32
TL061IP	P	PDIP	8	50	506	13.97	11230	4.32
TL062ACD	D	SOIC	8	75	507	8	3940	4.32
TL062ACP	P	PDIP	8	50	506	13.97	11230	4.32
TL062BCD	D	SOIC	8	75	507	8	3940	4.32
TL062BCP	P	PDIP	8	50	506	13.97	11230	4.32
TL062CD	D	SOIC	8	75	507	8	3940	4.32
TL062CD	D	SOIC	8	75	506.6	8	3940	4.32
TL062CP	P	PDIP	8	50	506	13.97	11230	4.32
TL062CPS	PS	SOP	8	80	530	10.5	4000	4.1
TL062CPW	PW	TSSOP	8	150	530	10.2	3600	3.5
TL062ID	D	SOIC	8	75	507	8	3940	4.32
TL062ID	D	SOIC	8	75	506.6	8	3940	4.32
TL062IDG4	D	SOIC	8	75	507	8	3940	4.32
TL062IDG4	D	SOIC	8	75	506.6	8	3940	4.32
TL062IP	P	PDIP	8	50	506	13.97	11230	4.32
TL062MFKB	FK	LCCC	20	55	506.98	12.06	2030	NA
TL064ACD	D	SOIC	14	50	506.6	8	3940	4.32
TL064ACN	N	PDIP	14	25	506	13.97	11230	4.32

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL064BCD	D	SOIC	14	50	506.6	8	3940	4.32
TL064BCDG4	D	SOIC	14	50	506.6	8	3940	4.32
TL064BCN	N	PDIP	14	25	506	13.97	11230	4.32
TL064CD	D	SOIC	14	50	506.6	8	3940	4.32
TL064CN	N	PDIP	14	25	506	13.97	11230	4.32
TL064CPW	PW	TSSOP	14	90	530	10.2	3600	3.5
TL064ID	D	SOIC	14	50	506.6	8	3940	4.32
TL064IDG4	D	SOIC	14	50	506.6	8	3940	4.32
TL064IN	N	PDIP	14	25	506	13.97	11230	4.32
TL064INS	NS	SOP	14	50	530	10.5	4000	4.1
TL064MFKB	FK	LCCC	20	55	506.98	12.06	2030	NA
TL064MWB	W	CFP	14	25	506.98	26.16	6220	NA

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

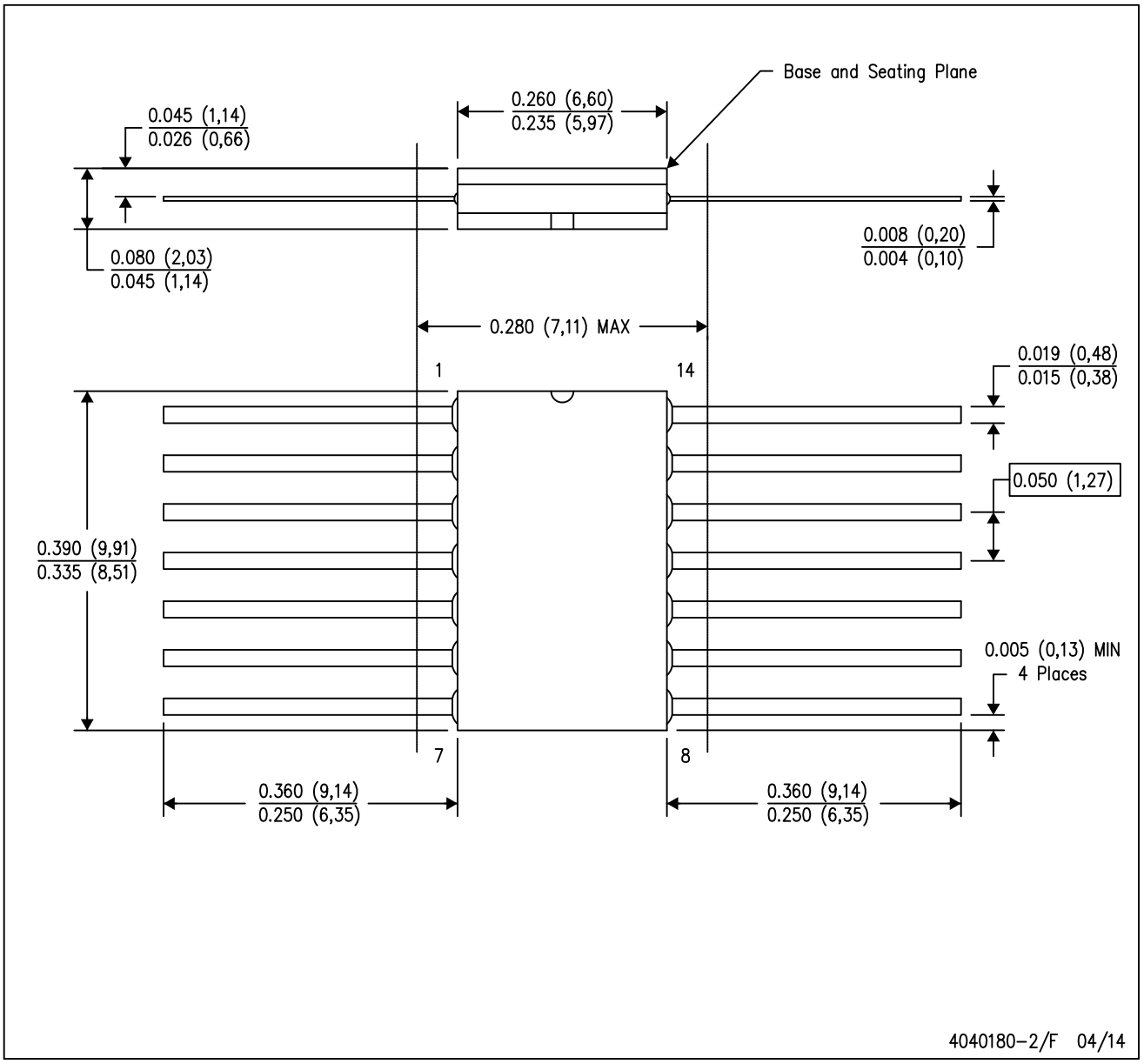


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R–GDFP–F14) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

GENERIC PACKAGE VIEW

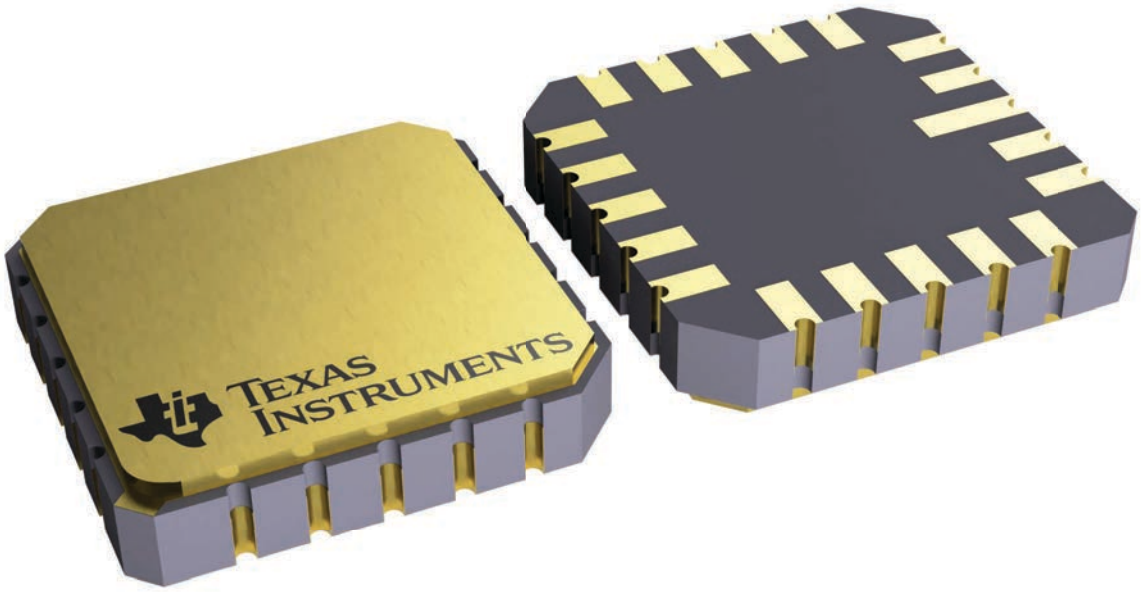
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

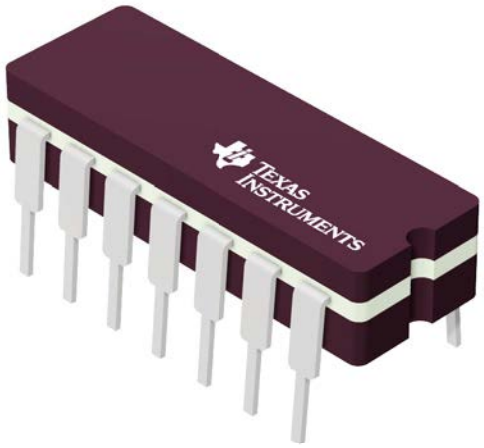


4229370VA\

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

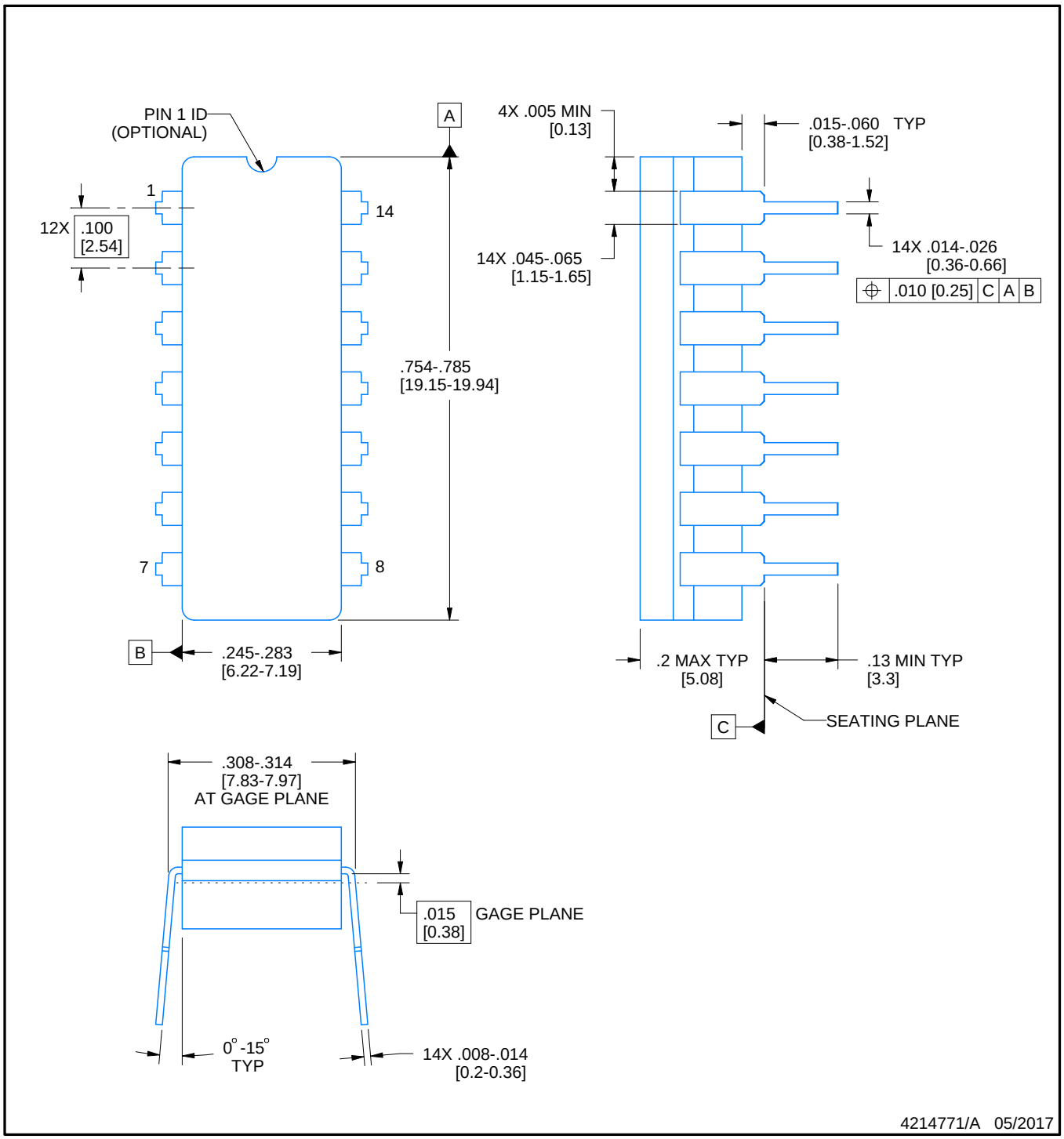


PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

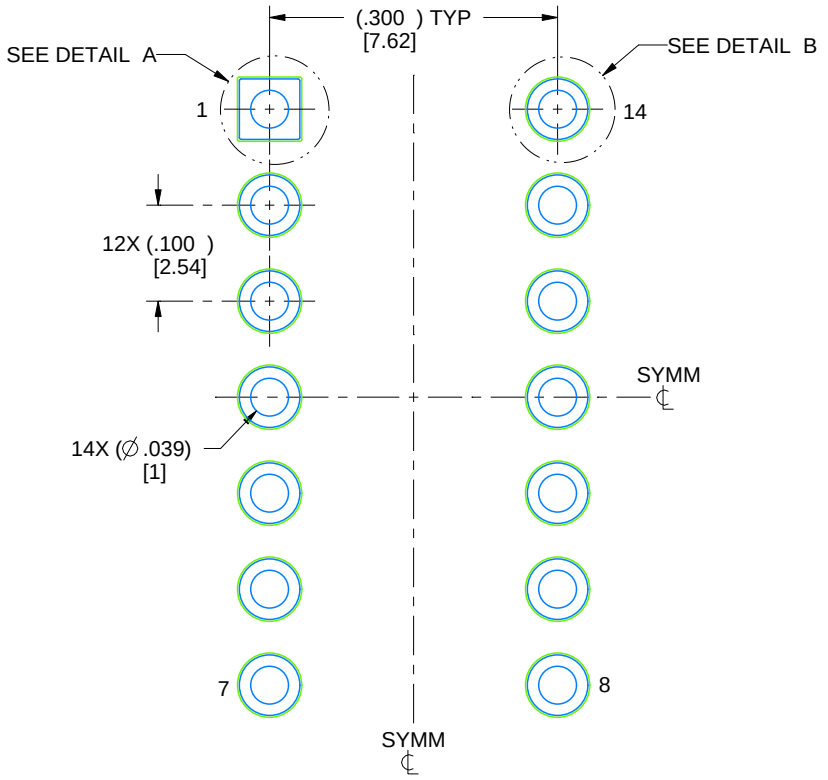
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

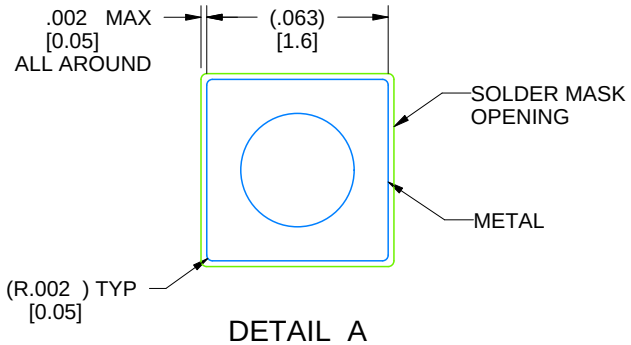
J0014A

CDIP - 5.08 mm max height

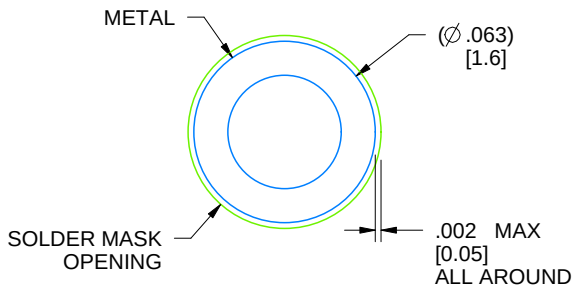
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



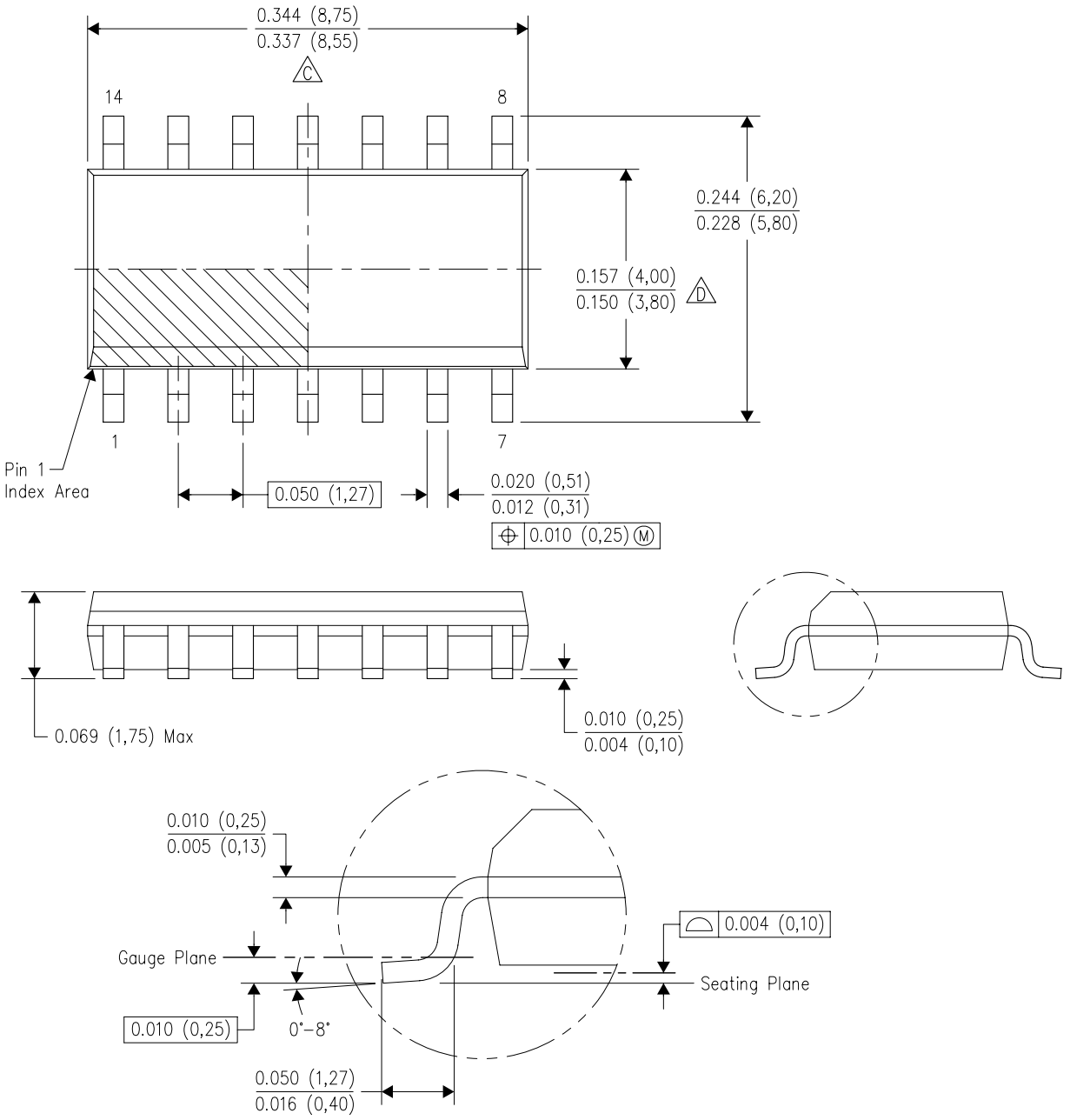
DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

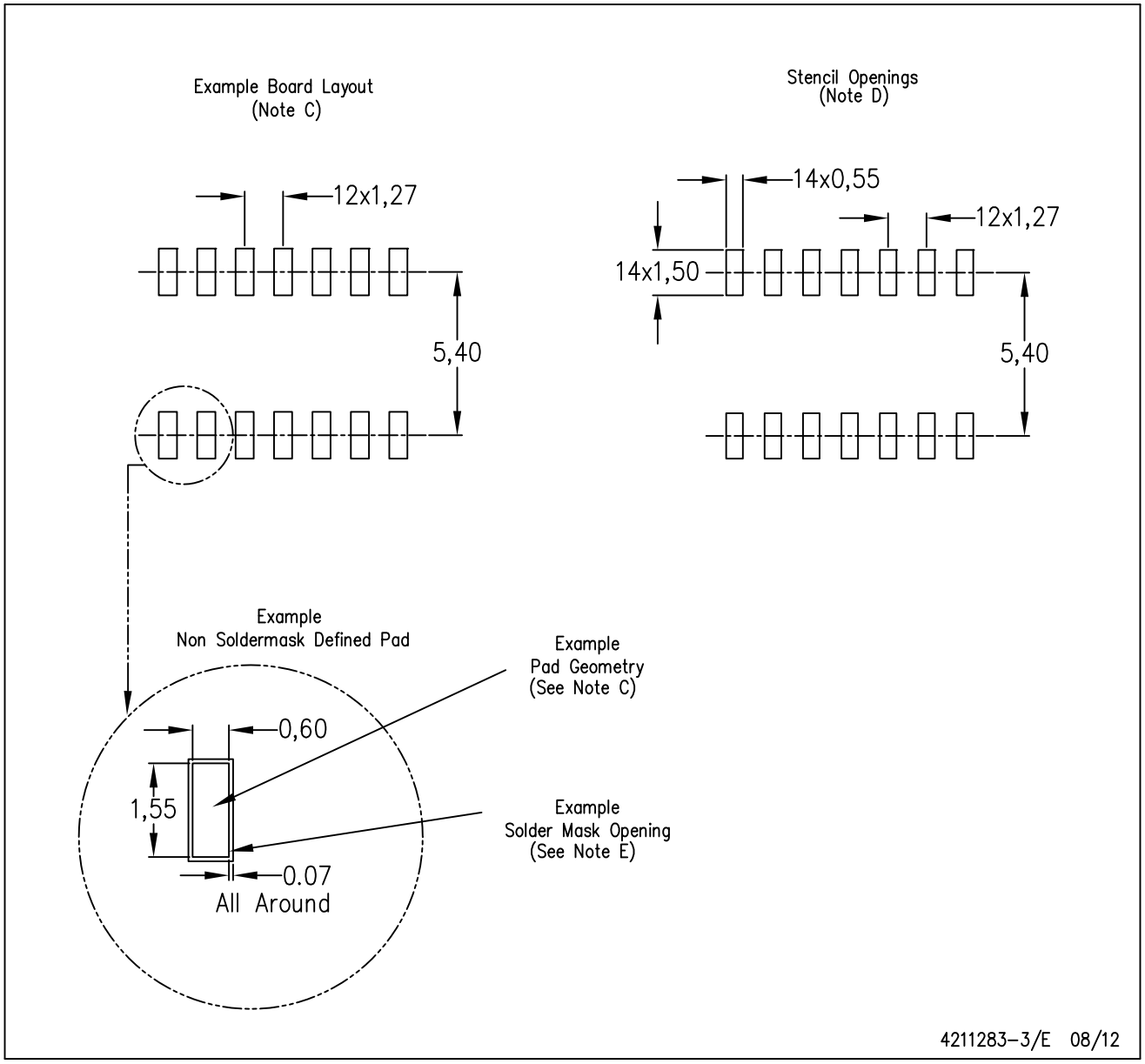
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

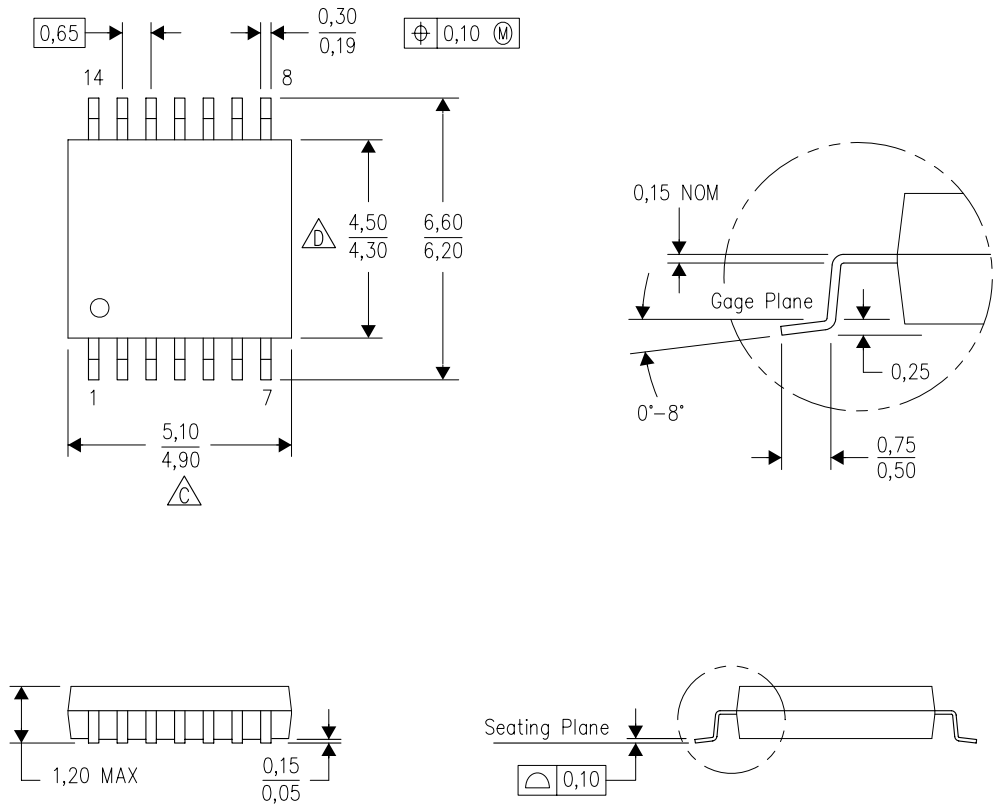
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



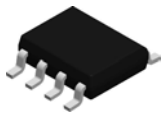
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

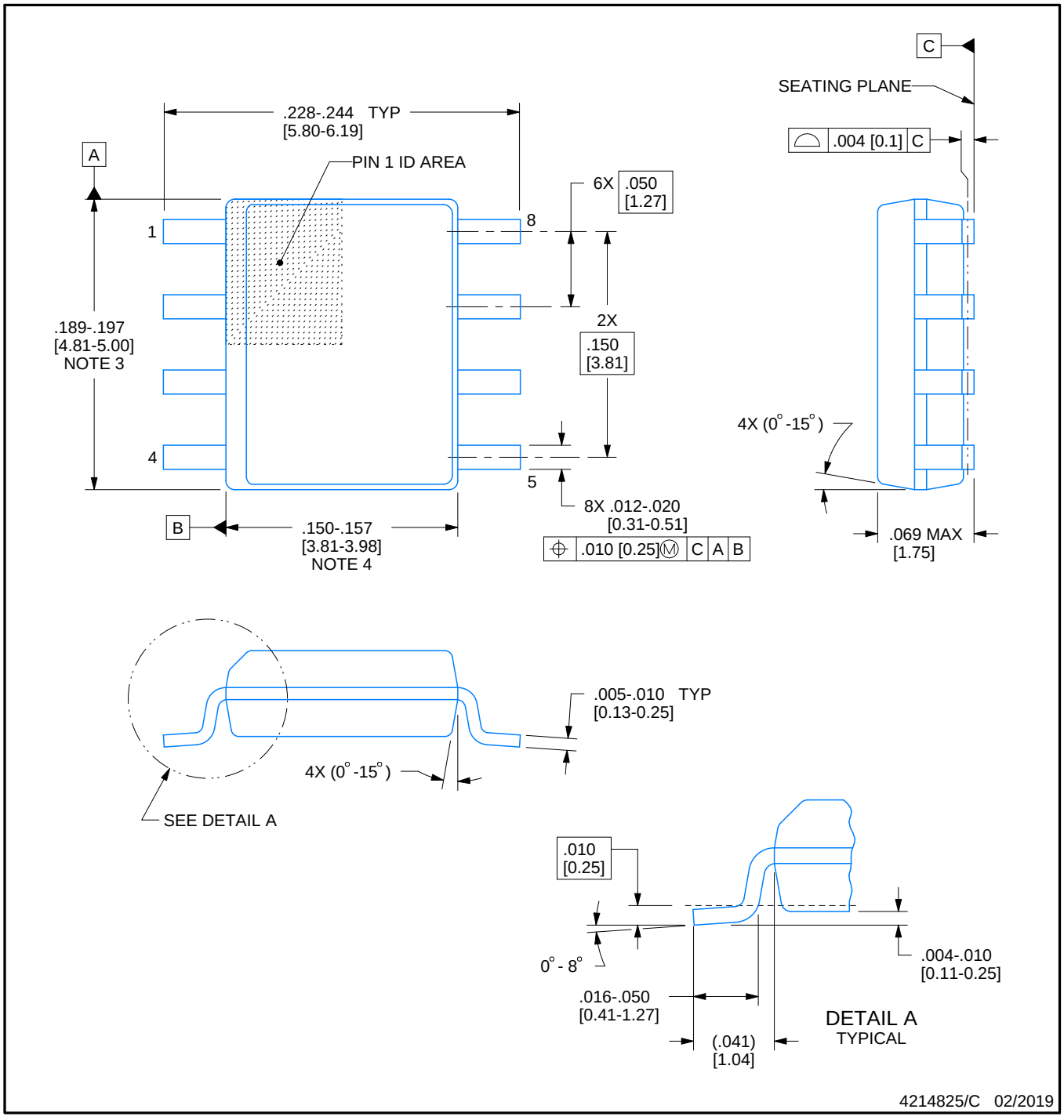


PACKAGE OUTLINE

D0008A

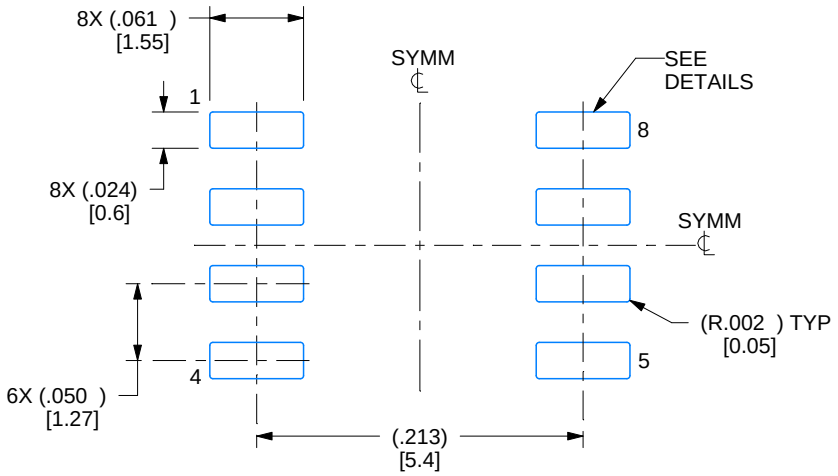
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

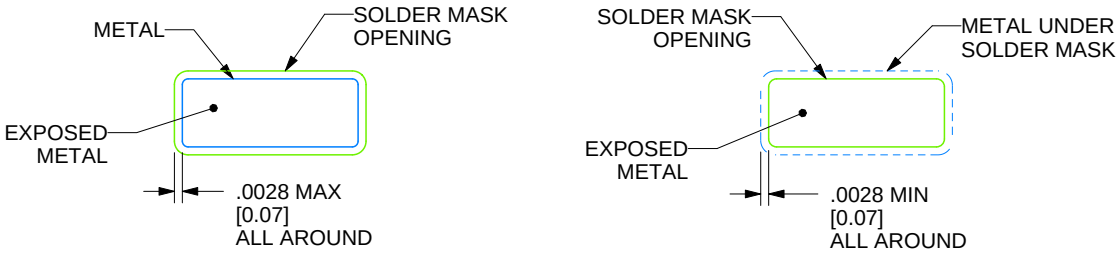


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

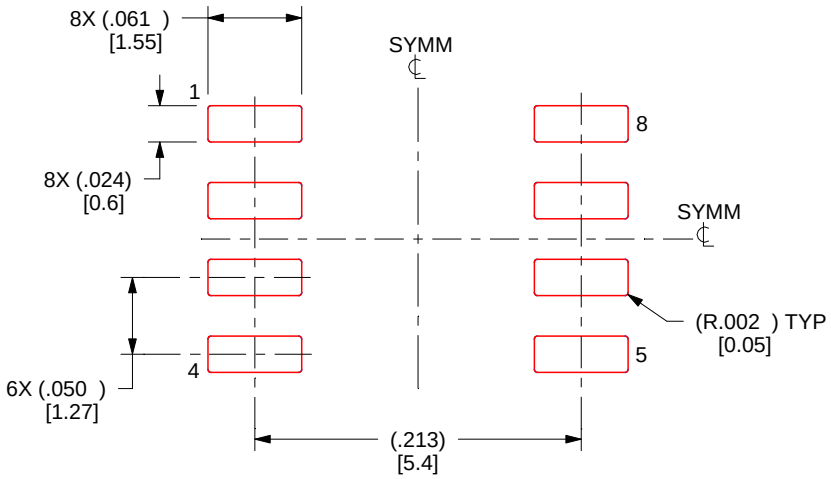
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

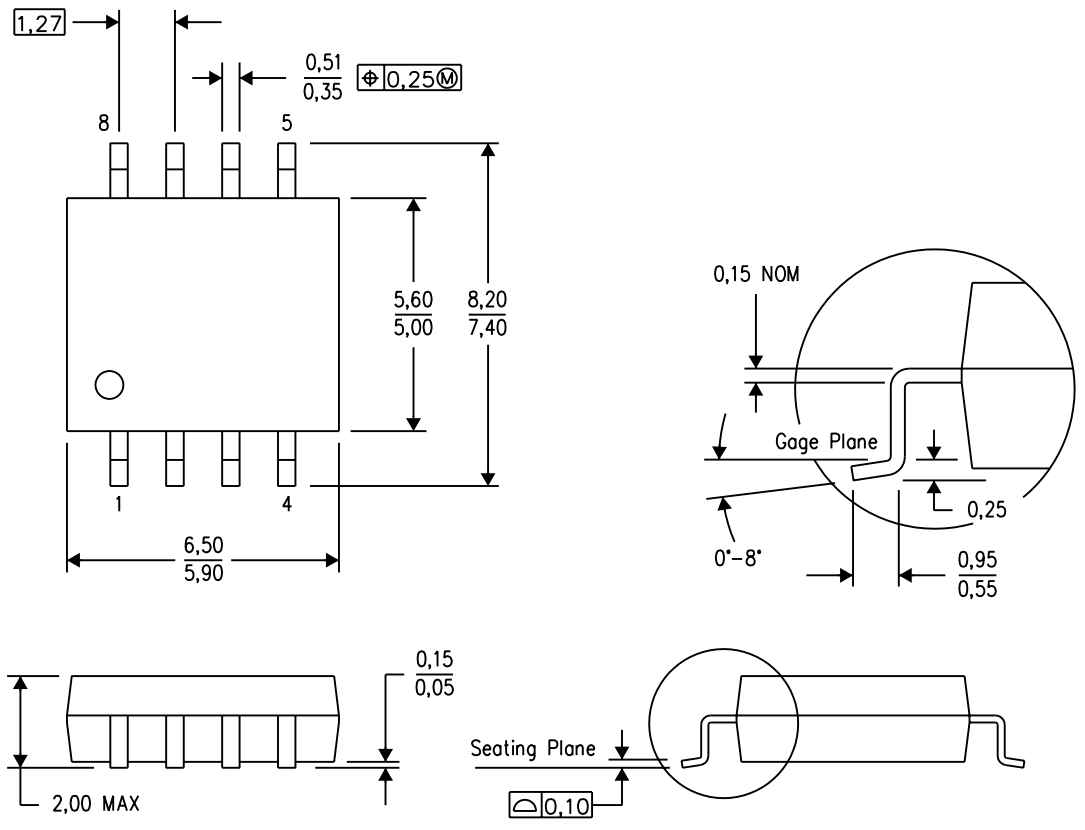
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

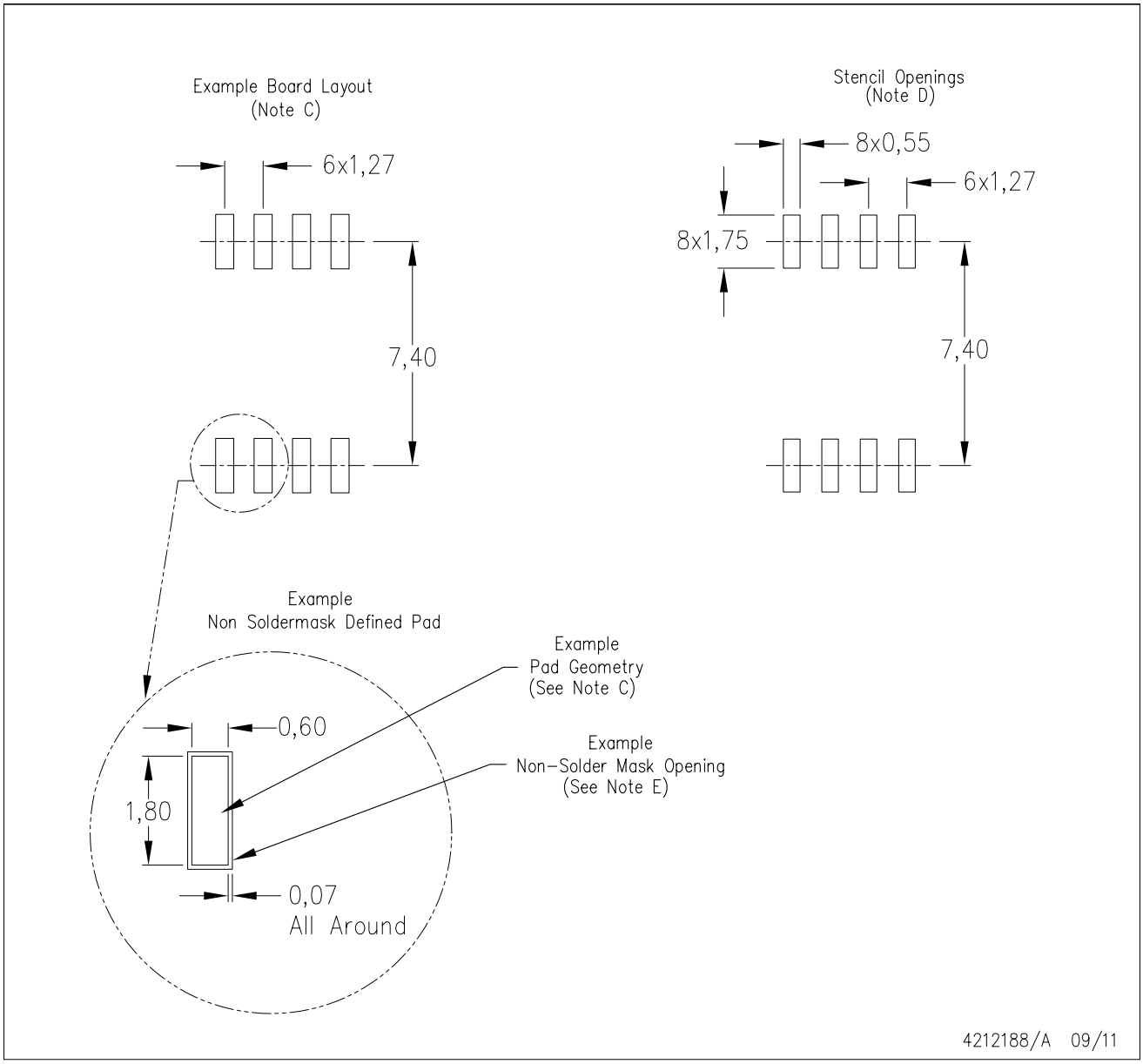
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

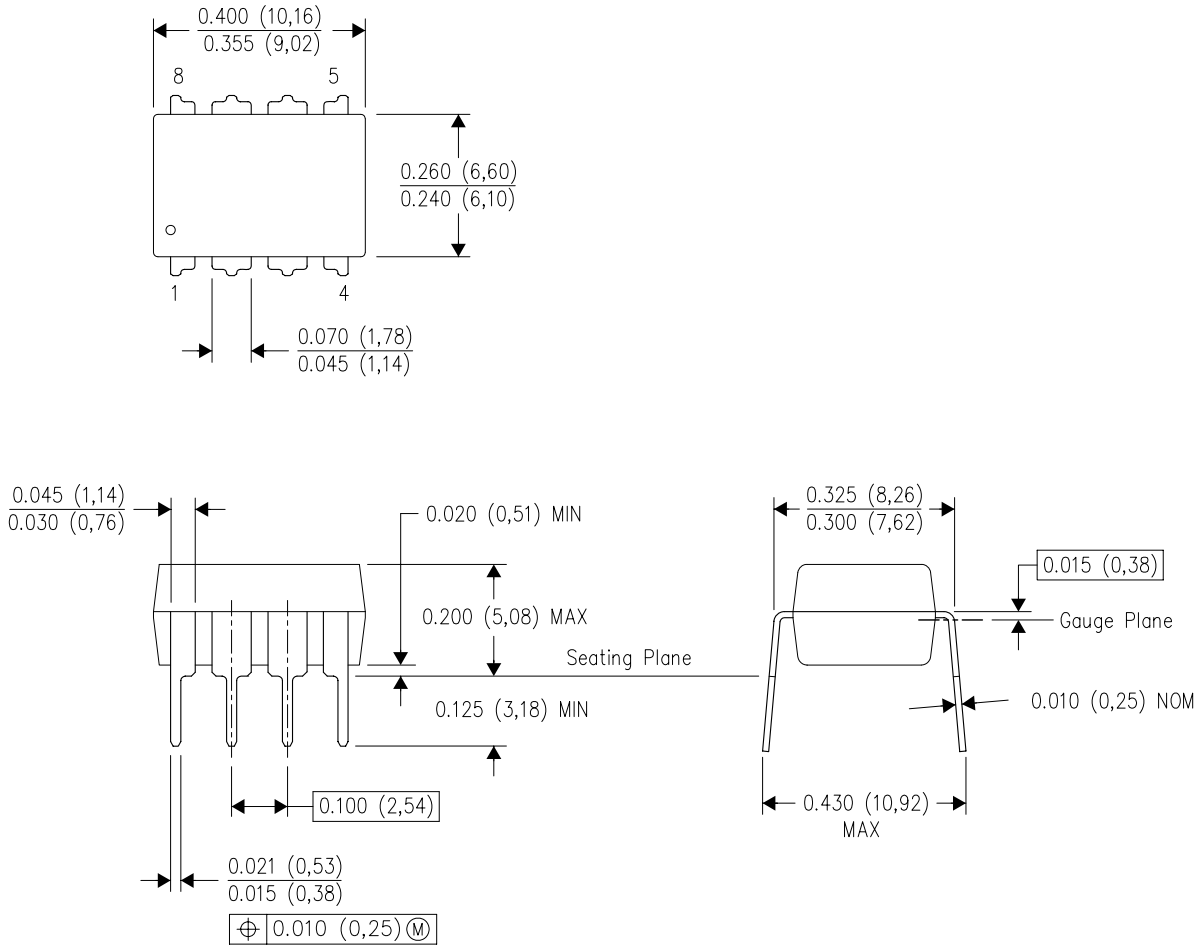
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

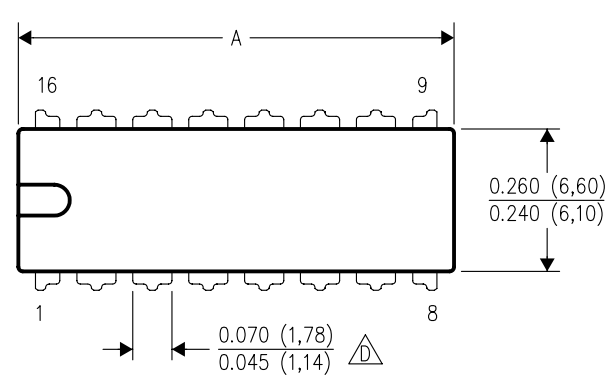


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

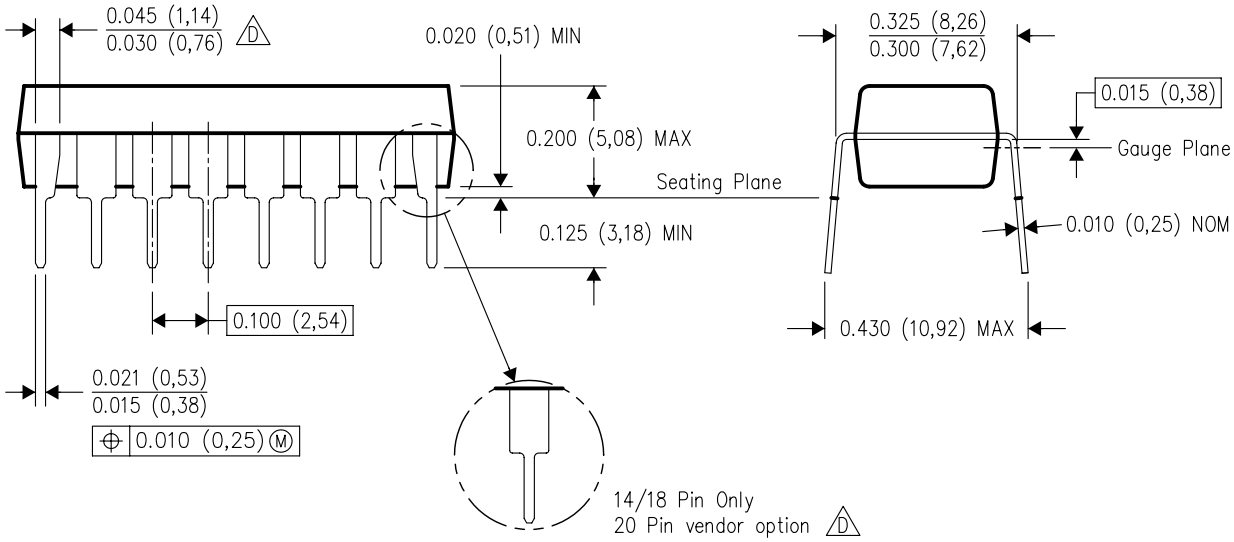
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

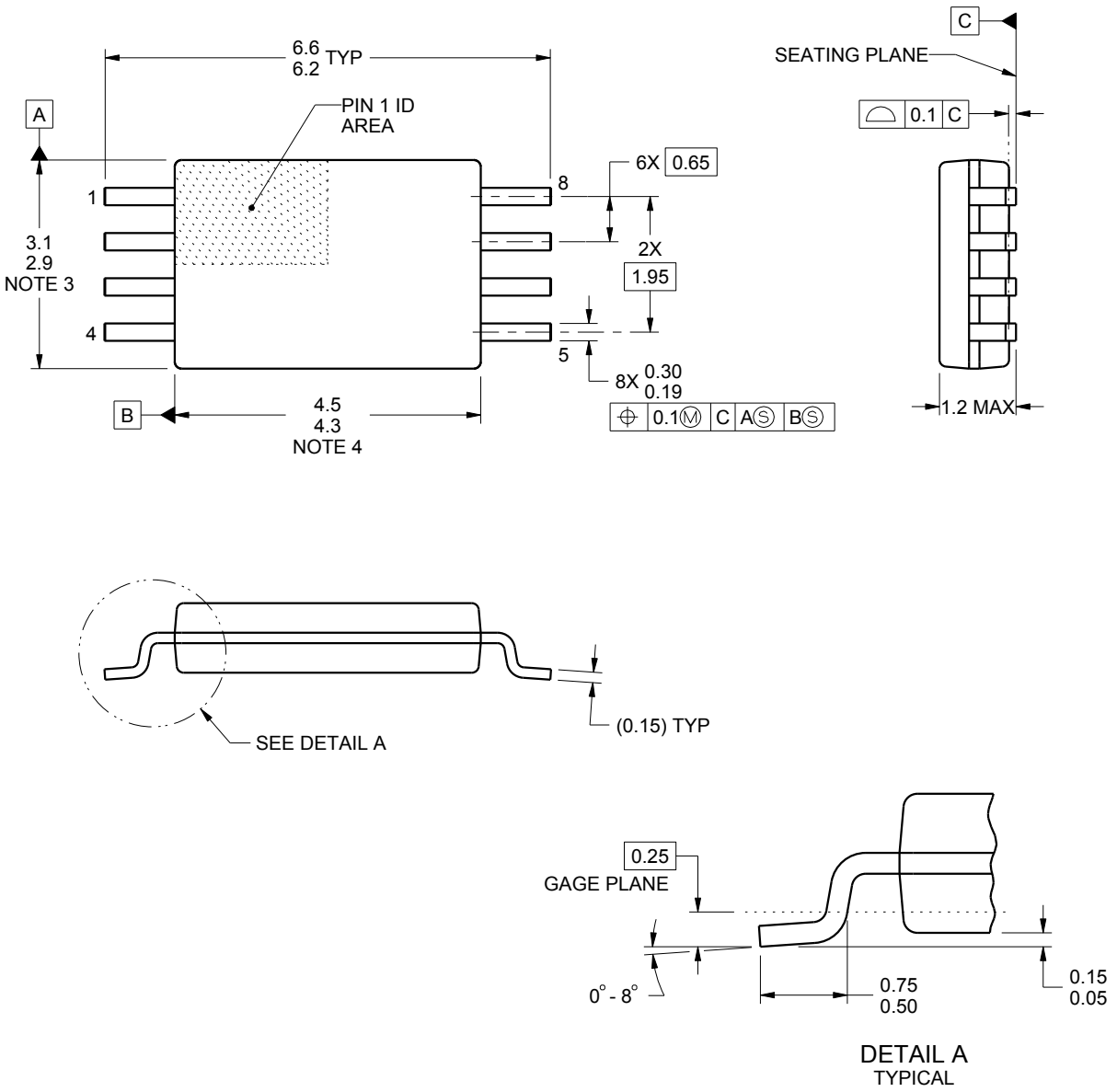
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

PW0008A

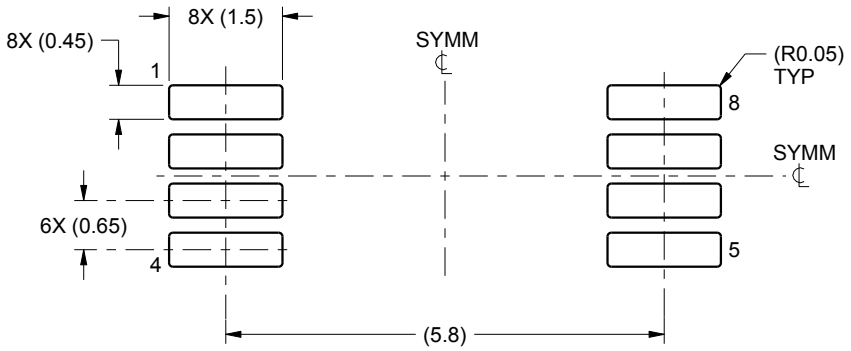
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

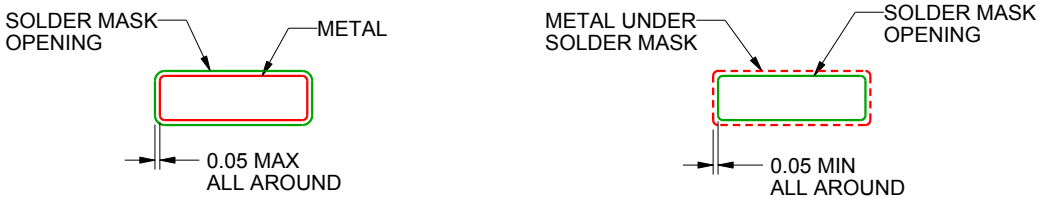


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

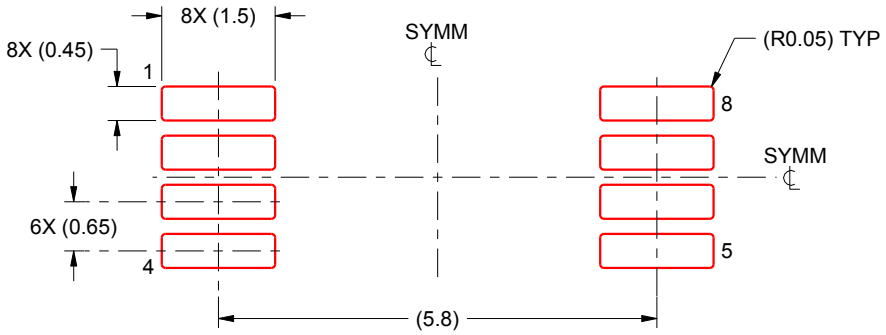


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

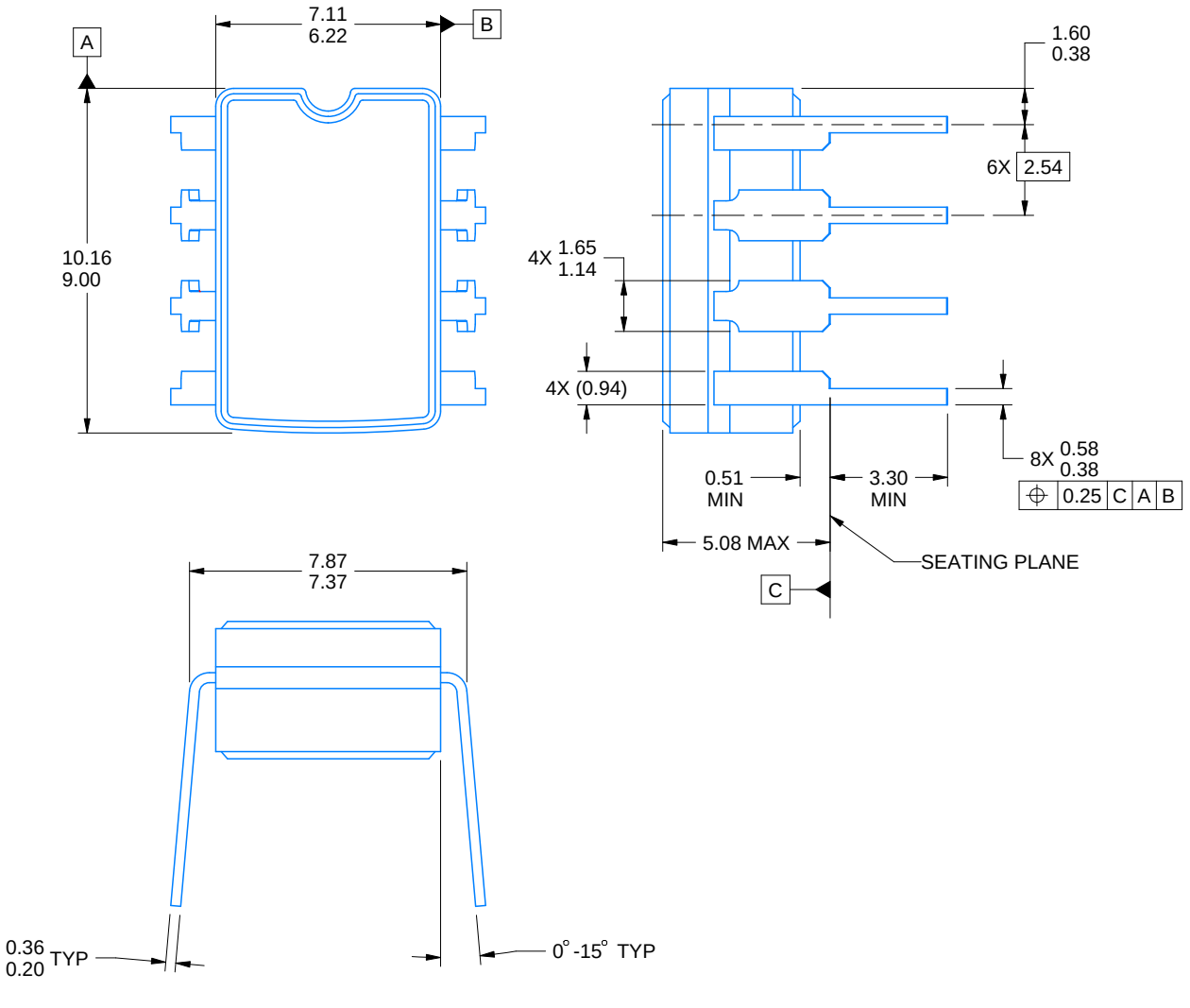
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



4230036/A 09/2023

NOTES:

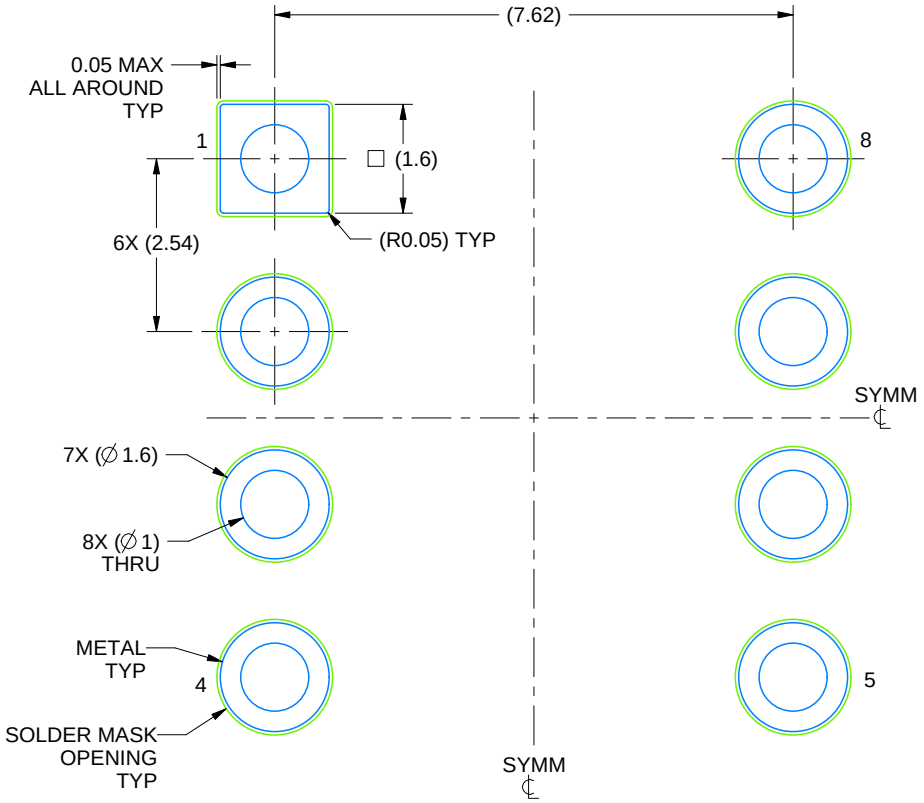
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package can be hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification.
5. Falls within MIL STD 1835 GDIP1-T8

EXAMPLE BOARD LAYOUT

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



LAND PATTERN EXAMPLE
NON SOLDER MASK DEFINED
SCALE: 9X

4230036/A 09/2023

重要なお知らせと免責事項

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