TL331B、TL391B および TL331 シングル コンパレータ

1 特長

- 新しい TL331B および TL391B
- B バージョンの仕様を改善
  - 最大定格:最大 38V
  - ESD 定格 (HBM):2 kV
  - 優れた逆電圧性能
  - 低入力オフセット:0.37 mV
  - 低い入力バイアス電流:3.5nA
  - 低消費電流:430μA
  - 1μsec の短い応答時間
  - ピン配置が異なる TL391B
- TL331 をそのまま置き換えることができる改良された代替品 TL331B を提供
- 同相入力電圧範囲にグランドを含む
- 差動入力電圧範囲が最大定格電源電圧と同じ:±38V
- 低い出力飽和電圧
- TTL、MOS、CMOS 互換出力

2 アプリケーション

- ロボット掃除機
- 単相 UPS
- サーバー PSU
- コードレス電動工具
- ワイヤレス・インフラ
- 家電製品
- ビル・オートメーション
- ファクトリ・オートメーション / 制御
- モータ・ドライブ
- インフォテインメント / クラスタ

3 概要

TL331B および TL391B デバイスは、業界標準の TL331 コンパレータの次世代バージョンです。これらの次世代デバイスは、コスト重視のアプリケーション向けに非常に手頃な価格で提供しています。小さいオフセット電圧、高い電源電圧への対応、小さい消費電流、小さい入力バイアス電流、小さい伝搬遅延、優れた 2kV の ESD 性能などの特長と、そのまま置き換えることができる利便性を兼ね備えています。TL331B は、TL331I と TL331K の両方のバージョンをそのまま置き換えることができる改良された代替品です。一方 TL391B は、競合デバイスを置き換えるために TL331B のピン配置を変更したデバイスです。

デュアル電源でも、2 つの電源間の差分が 2V～36V の範囲内であり、VCC が入力同相電圧より 1.5V 以上高ければ、動作可能です。電流ドレインは、電源電圧に依存しません。出力を他のオープン コレクタ出力に接続し、ワイヤード AND 関係を構築できます。

製品情報

部品番号 (1)	パッケージ	本体サイズ (公称)(2)
TL331、 TL331B、 TL391B	SOT-23 (5)	2.90mm × 1.60mm

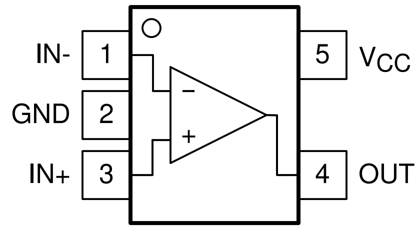
(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。

ファミリ比較表

仕様	TL331B TL391B	TL331I	TL331K	単位
電源電圧	2～36	2～36	2～36	V
総消費電流 (5V～最大値 36V)	0.43	0.7	0.7	mA
温度範囲	-40～125	-40～85	-40～105	℃
静電気放電 (HBM)	2000	1000	1000	V
オフセット電圧 (全温度範囲での最大値)	±4	±9	±9	mV
入力バイアス電流 (代表値 / 最大値)	3.5 / 25	25 / 250	25 / 250	nA
応答時間 (代表値)	1	1.3	1.3	μsec

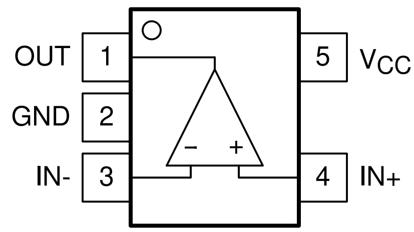
Table of Contents

4 Pin Configuration and Functions



Note reversed inputs compared to similar common pinout

図 4-1. TL331, TL331B DBV Package, 5-Pin SOT-23, Top View



Note reversed inputs compared to similar common pinout

図 4-2. TL391B DBV Package, 5-Pin SOT-23, Top View

Pin Functions

PIN			TYPE	DESCRIPTION
	TL331, TL331B	TL391B		
NAME	NO.	NO.		
IN+	3	4	I	Positive Input
IN–	1	3	I	Negative Input
OUT	4	1	O	Open Collector/Drain Output
V_{CC}	5	5	—	Power Supply Input
GND	2	2	—	Ground

5 Specifications

5.1 Absolute Maximum Ratings, TL331 and TL331K

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
V_{CC}	Supply voltage[(2)]	0	36	V
V_{ID}	Differential input voltage[(3)]	–36	36	V
V_I	Input voltage range (either input)	–0.3	36	V
V_O	Output voltage	0	36	V
I_O	Output current	0	20	mA
	Duration of output short-circuit to ground[(4)]	Unlimited		
I_{IK}	Input current[(5)]		–50	mA
T_J	Operating virtual junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the network ground.
(3) Differential voltages are at IN+ with respect to IN–.
(4) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.
(5) Input current flows thorough parasitic diode to ground and will turn on parasitic transistors that will increase ICC and may cause output to be incorrect. Normal operation resumes when input current is removed.

5.2 Absolute Maximum Ratings, TL331B and TL391B

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
V_{CC}	Supply voltage[(2)]	-0.3	38	V
V_{ID}	Differential input voltage[(3)]	–38	38	V
V_I	Input voltage range (either input)	–0.3	38	V
V_O	Output voltage	-0.3	38	V
I_O	Output current		20	mA
	Duration of output short-circuit to ground[(4)]	Unlimited		
I_{IK}	Input current[(5)]		–50	mA
T_J	Operating virtual junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the network ground.
(3) Differential voltages are at IN+ with respect to IN–.
(4) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.
(5) Input current flows thorough parasitic diode to ground and will turn on parasitic transistors that will increase ICC and may cause output to be incorrect. Normal operation resumes when input current is removed.

5.3 ESD Ratings - TL331B and TL391B

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[(2)]	±750	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.4 ESD Ratings, TL331 and TL331K

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[(2)]	±750	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.5 Recommended Operating Conditions, TL331B and TL391B

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2	36	V
T_J	Junction temperature	–40	125	°C

5.6 Recommended Operating Conditions, TL331 and TL331K

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2	36	V
T_J	Junction temperature, TL331	–40	85	°C
T_J	Junction temperature, TL331K	–40	105	°C

5.7 Thermal Information

THERMAL METRIC[(1)]		TL331x, TL391x	UNIT
		DBV (SOT-23)	
		5 PINS	
$R_{θJA}$	Junction-to-ambient thermal resistance	211.7	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	133.6	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	79.9	°C/W
$Ψ_{JT}$	Junction-to-top characterization parameter	56.4	°C/W
$Ψ_{JB}$	Junction-to-board characterization parameter	79.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* report.

5.8 Electrical Characteristics, TL331B and TL391B

V_S = 5V, V_{CM} = (V–) ; T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_S = 5 to 36V	–2.5	±0.37	2.5	mV
		V_S = 5 to 36V, T_A = –40°C to +125°C	–4		4	
I_B	Input bias current			–3.5	–25	nA
		T_A = –40°C to +125°C			–50	nA
I_{OS}	Input offset current		–10	±0.5	10	nA
		T_A = –40°C to +125°C	–25		25	nA
V_{CM}	Input voltage range	V_S = 3 to 36V	(V–) – 0.1		(V+) – 1.5	V
		V_S = 3 to 36V, T_A = –40°C to +125°C	(V–) – 0.05		(V+) – 2.0	V
A_{VD}	Large signal differential voltage amplification	V_S = 15V, V_O = 1.4V to 11.4V; R_L ≥ 15k to (V+)	50	200		V/mV
V_{OL}	Low level output Voltage {swing from (V–)}	I_{SINK} ≤ 4mA, V_{ID} = -1V		110	400	mV
		I_{SINK} ≤ 4mA, V_{ID} = -1V T_A = –40°C to +125°C			550	mV
I_{OH-LKG}	High-level output leakage current	(V+) = V_O = 5V; V_{ID} = 1V		0.1	20	nA
I_{OH-LKG}	High-level output leakage current	(V+) = V_O = 36V; V_{ID} = 1V; T_A = –40°C to +125°C			1000	nA
I_{OL}	Low level output current	V_{OL} = 1.5V; V_{ID} = -1V; V_S = 5V	6	18		mA
I_Q	Quiescent current	V_S = 5V, no load		210	330	µA
		V_S = 36V, no load, T_A = –40°C to +125°C		275	430	µA

5.9 Switching Characteristics, TL331B and TL391B

V_S = 5V, V_{O_PULLUP} = 5V, V_{CM} = V_S/2, C_L = 15pF, R_L = 5.1k Ohm, T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{response}$	Propagation delay time, high-to-low; Small scale input signal (1)	Input overdrive = 5mV, Input step = 100mV		1000		ns
$t_{response}$	Propagation delay time, high-to-low; TTL input signal (1)	TTL input with V_{ref} = 1.4V		300		ns

(1) High-to-low and low-to-high refers to the transition at the input.

5.10 Electrical Characteristics, TL331 and TL331K

at specified free-air temperature, V_{CC} = 5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)	T_A (3)	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{CC} = 5V to 30V, V_O = 1.4V, $V_{IC} = V_{IC(min)}$	25°C		2	5	mV
			Full range			9	
I_{IO}	Input offset current	V_O = 1.4V	25°C		5	50	nA
			Full range			250	
I_{IB}	Input bias current	V_O = 1.4V	25°C		–25	–250	nA
			Full range			–400	
V_{ICR}	Common-mode input voltage range(2)		Full range	0 to V_{CC} – 1.5			V
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15V, V_O = 1.4V to 11.4V, R_L ≥ 15 kΩ to V_{CC}	25°C	50	200		V/mV
I_{OH}	High-level output current	V_{OH} = 5V, V_{ID} = 1V	25°C		0.1	50	nA
		V_{OH} = 30V, V_{ID} = 1V	Full range			1	μA
V_{OL}	Low-level output voltage	I_{OL} = 4mA, V_{ID} = –1V	25°C		150	400	mV
			Full range			700	
I_{OL}	Low-level output current	V_{OL} = 1.5V, V_{ID} = –1V	25°C	6			mA
I_{CC}	Supply current	R_L = ∞, V_{CC} = 5V	25°C		0.4	0.7	mA

(1) All characteristics are measured with zero common-mode input voltage, unless otherwise specified.
(2) The voltage at either input or common-mode must not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V_{CC+} – 1.5V, but either or both inputs can go to 30V without damage.
(3) Full range T_A is –40°C to +85°C for I-suffix devices and –40°C to +105°C for K-suffix devices.

5.11 Switching Characteristics, TL331 and TL331K

V_{CC} = 5V, T_A = 25°C

PARAMETER	TEST CONDITIONS		TYP	UNIT
Response time	R_L connected to 5V through 5.1kΩ, C_L = 15pF(1) (2)	100mV input step with 5mV overdrive	1.3	μs
		TTL-level input step	0.3	

(1) C_L includes probe and jig capacitance.
(2) The response time specified is the interval between the input step function and the instant when the output crosses 1.4V.

5.12 Typical Characteristics

T_A = 25°C, V_S = 5V, R_{PULLUP} = 5.1k, C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

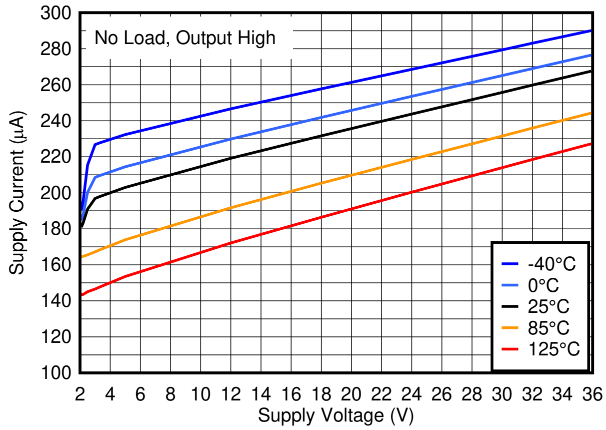


図 5-1. Supply Current vs. Supply Voltage

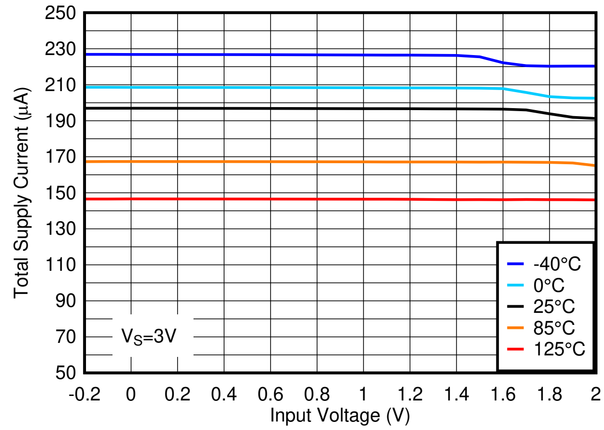


図 5-2. Total Supply Current vs. Input Voltage at 3V

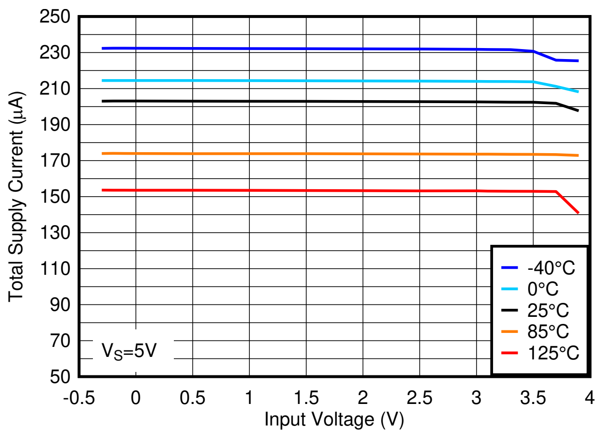


図 5-3. Total Supply Current vs. Input Voltage at 3.3V

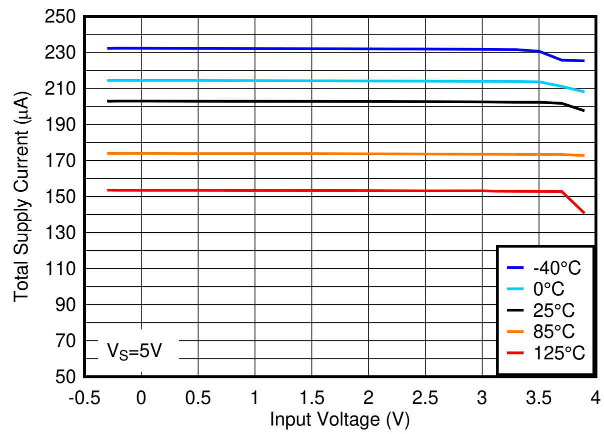


図 5-4. Total Supply Current vs. Input Voltage at 5V

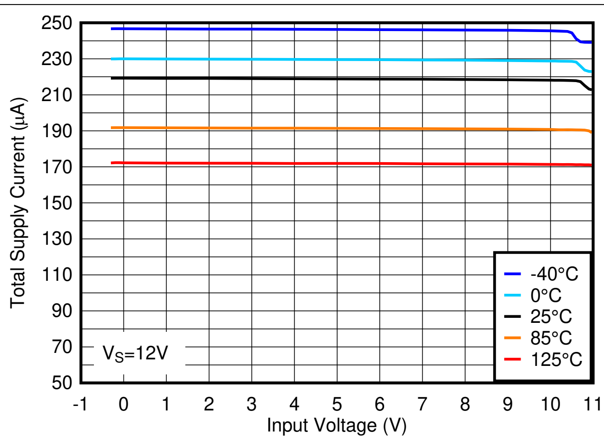


図 5-5. Total Supply Current vs. Input Voltage at 12V

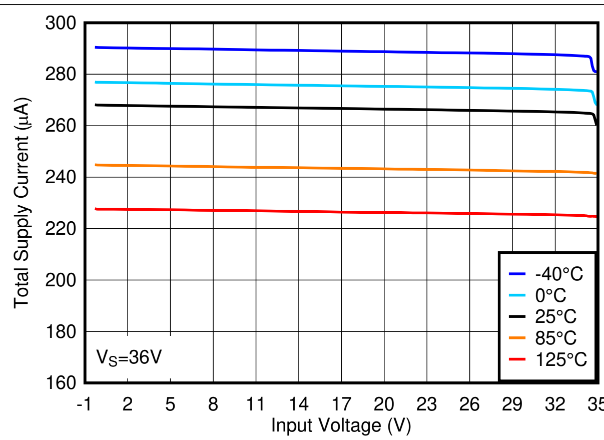


図 5-6. Total Supply Current vs. Input Voltage at 36V

5.12 Typical Characteristics (continued)

T_A = 25°C, V_S = 5V, R_{PULLUP} = 5.1k, C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

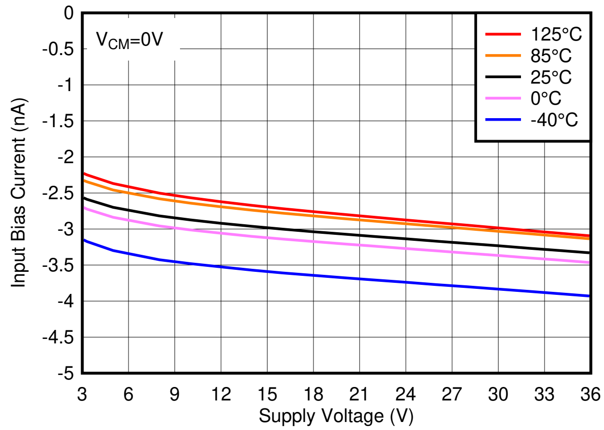


図 5-7. Input Bias Current vs. Supply Voltage

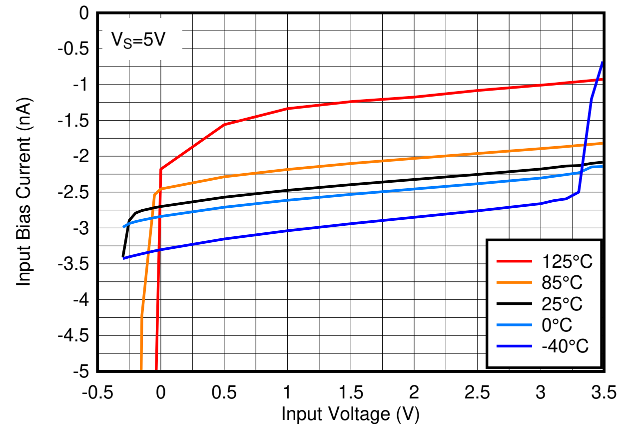


図 5-8. Input Bias Current vs. Input Voltage at 5V

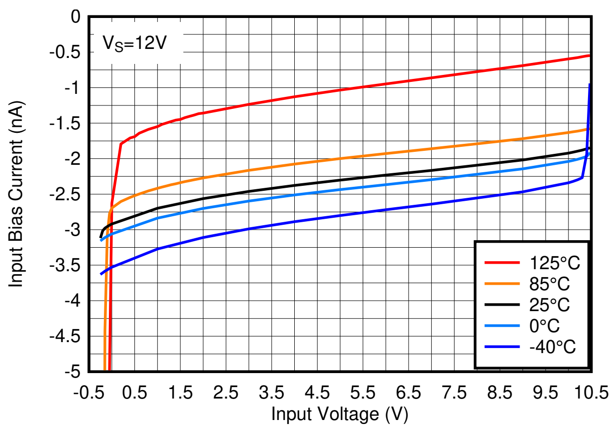


図 5-9. Input Bias Current vs. Input Voltage at 12V

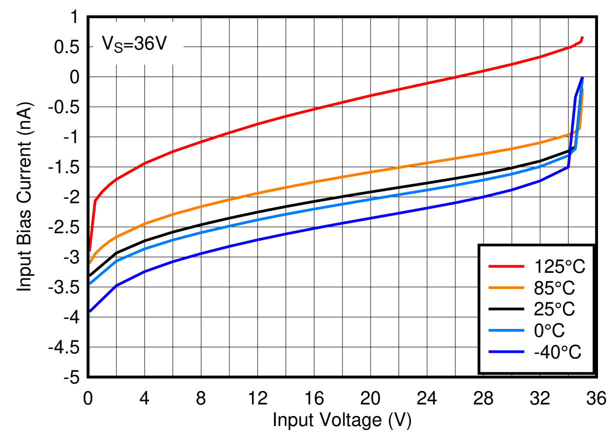


図 5-10. Input Bias Current vs. Input Voltage at 36V

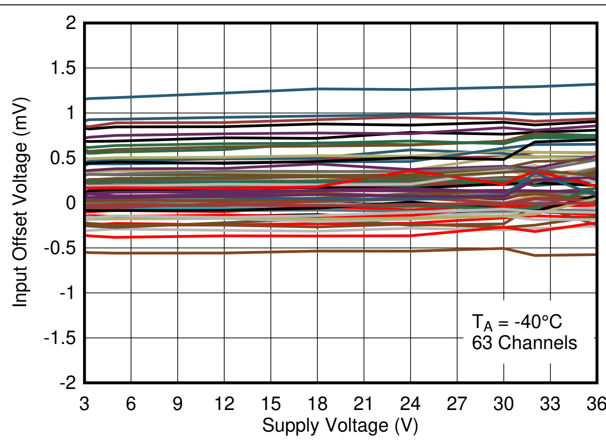


図 5-11. Input Offset Voltage vs. Supply Voltage at -40°C

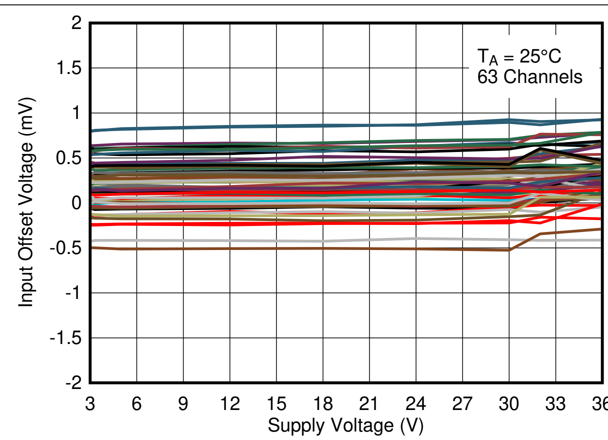


図 5-12. Input Offset Voltage vs. Supply Voltage at 25°C

5.12 Typical Characteristics (continued)

T_A = 25°C, V_S = 5V, R_{PULLUP} = 5.1k, C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

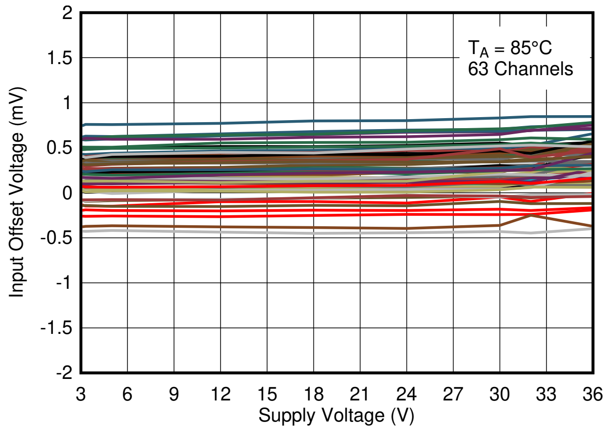


図 5-13. Input Offset Voltage vs. Supply Voltage at 85°C

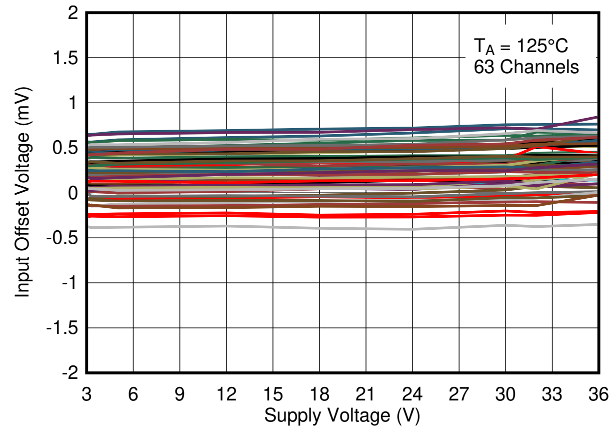


図 5-14. Input Offset Voltage vs. Supply Voltage at 125°C

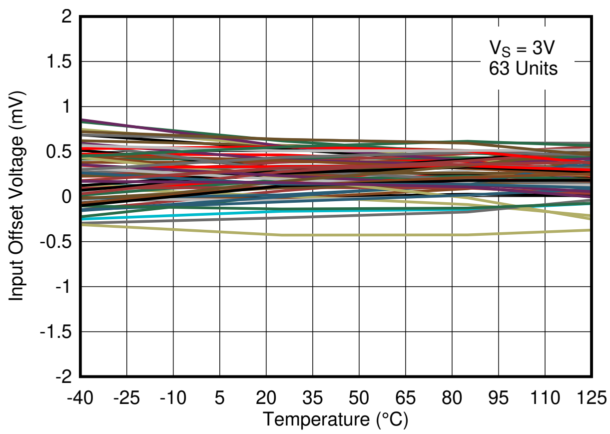


図 5-15. Input Offset Voltage vs. Temperature at 3V

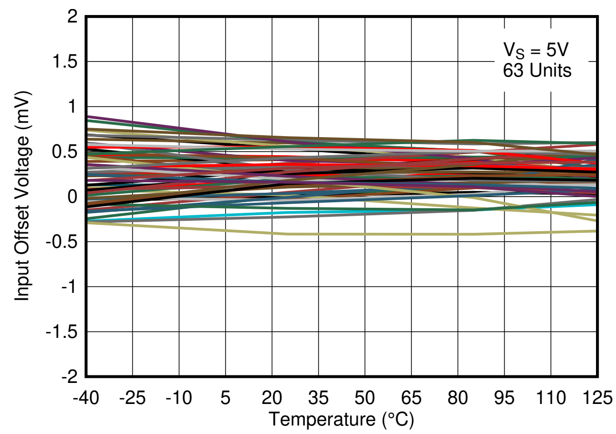


図 5-16. Input Offset Voltage vs. Temperature at 5V

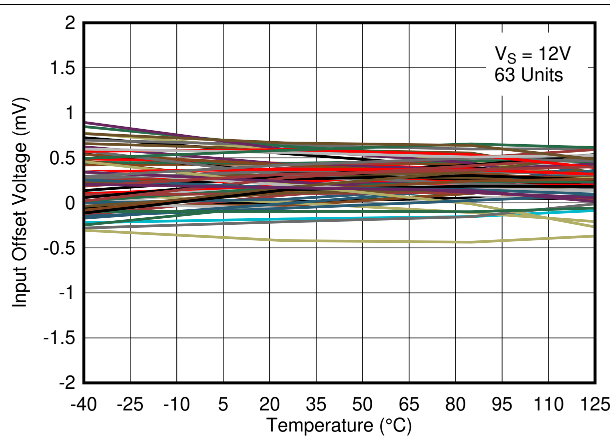


図 5-17. Input Offset Voltage vs. Temperature at 12V

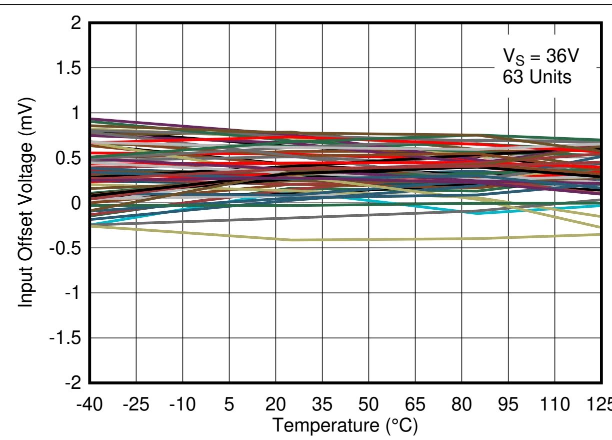


図 5-18. Input Offset Voltage vs. Temperature at 36V

5.12 Typical Characteristics (continued)

T_A = 25°C, V_S = 5V, R_{PULLUP} = 5.1k, C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

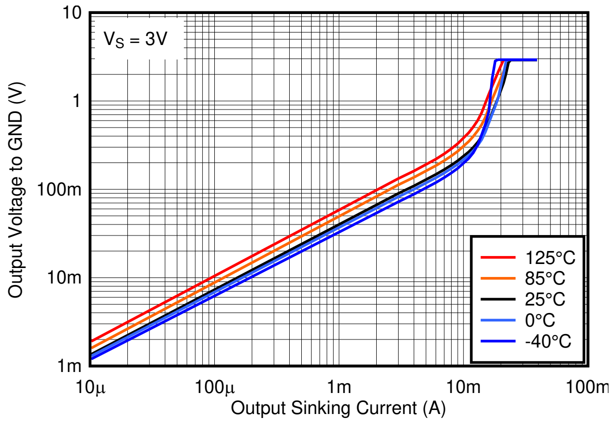


図 5-19. Output Low Voltage vs. Output Sinking Current at 3V

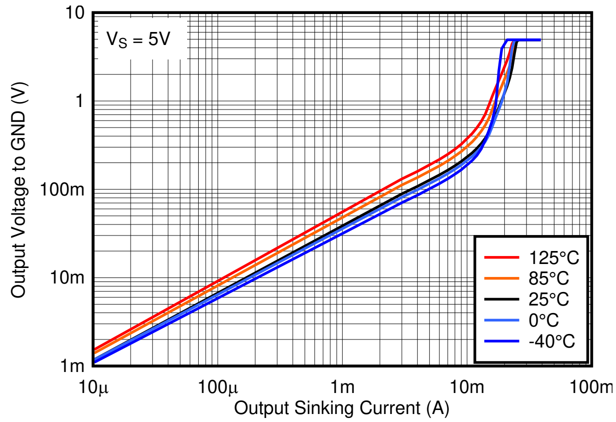


図 5-20. Output Low Voltage vs. Output Sinking Current at 5V

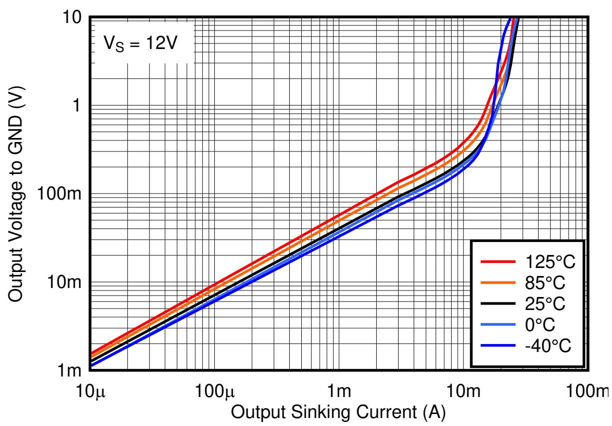


図 5-21. Output Low Voltage vs. Output Sinking Current at 12V

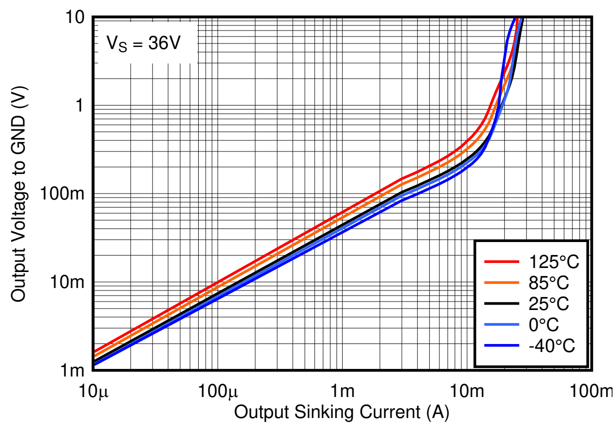


図 5-22. Output Low Voltage vs.Output Sinking Current at 36V

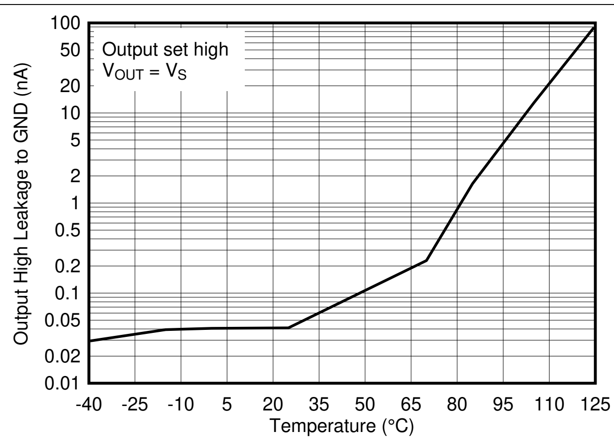


図 5-23. Output High Leakage Current vs.Temperature at 5V

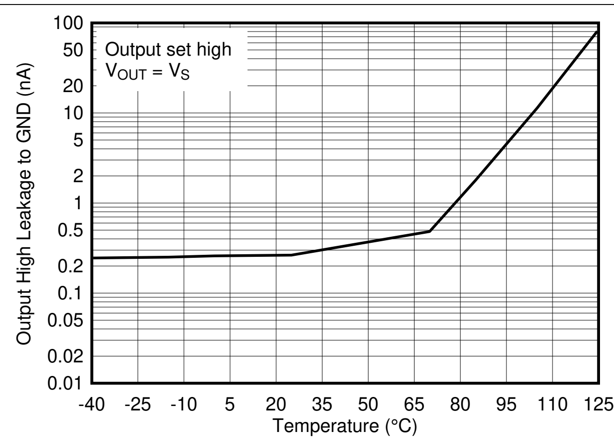


図 5-24. Output High Leakage Current vs. Temperature at 36V

5.12 Typical Characteristics (continued)

T_A = 25°C, V_S = 5V, R_{PULLUP} = 5.1k, C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

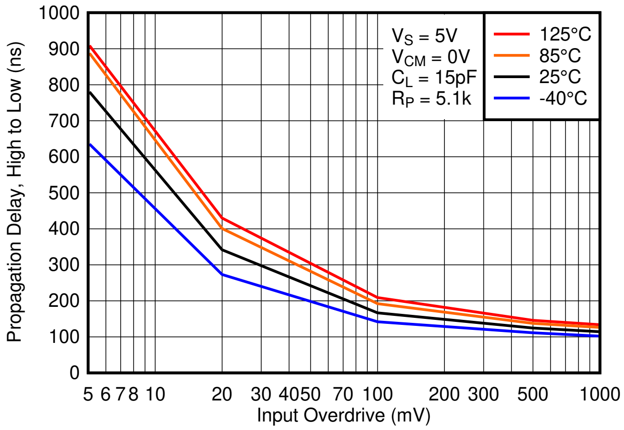


図 5-25. High to Low Propagation Delay vs. Input Overdrive Voltage, 5V

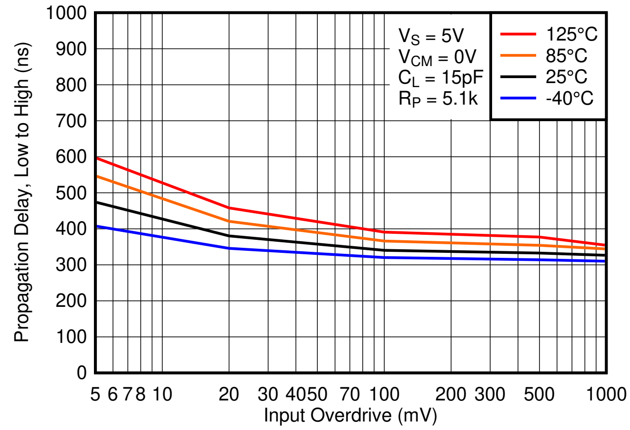


図 5-26. Low to High Propagation Delay vs. Input Overdrive Voltage, 5V

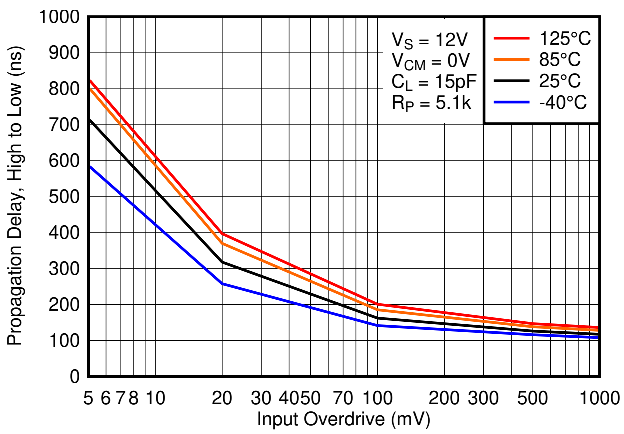


図 5-27. High to Low Propagation Delay vs. Input Overdrive Voltage, 12V

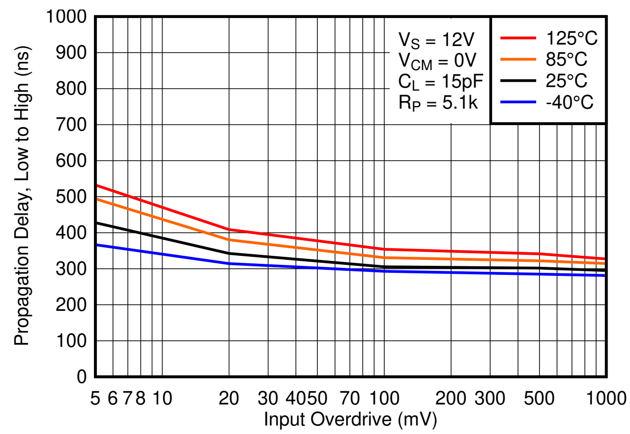


図 5-28. Low to High Propagation Delay vs. Input Overdrive Voltage, 12V

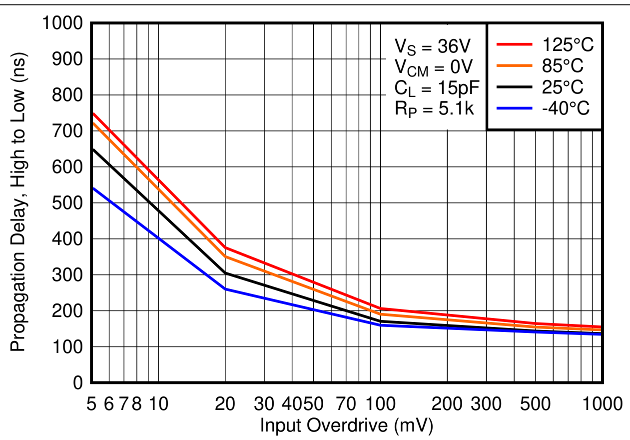


図 5-29. High to Low Propagation Delay vs. Input Overdrive Voltage, 36V

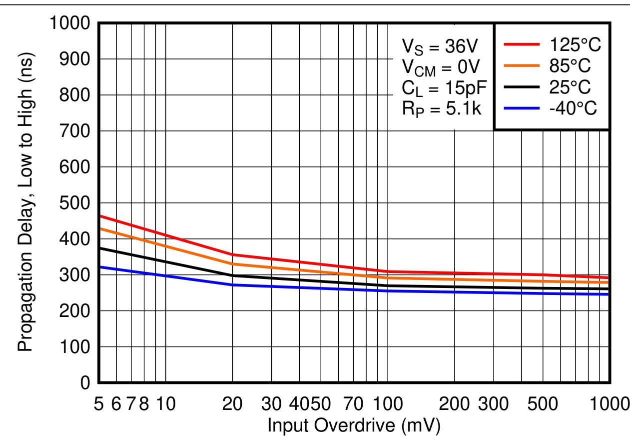


図 5-30. Low to High Propagation Delay vs. Input Overdrive Voltage, 36V

5.12 Typical Characteristics (continued)

T_A = 25°C, V_S = 5V, R_{PULLUP} = 5.1k, C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

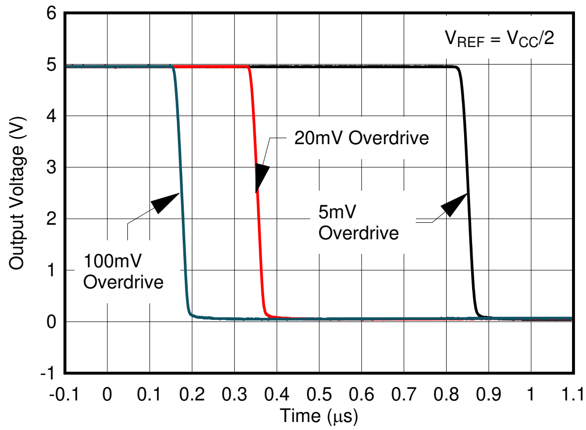


図 5-31. Response Time for Various Overdrives, High-to-Low Transition

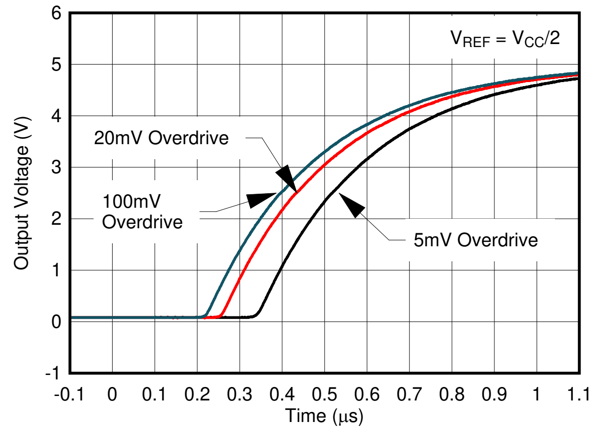


図 5-32. Response Time for Various Overdrives, Low-to-High Transition

6 Detailed Description

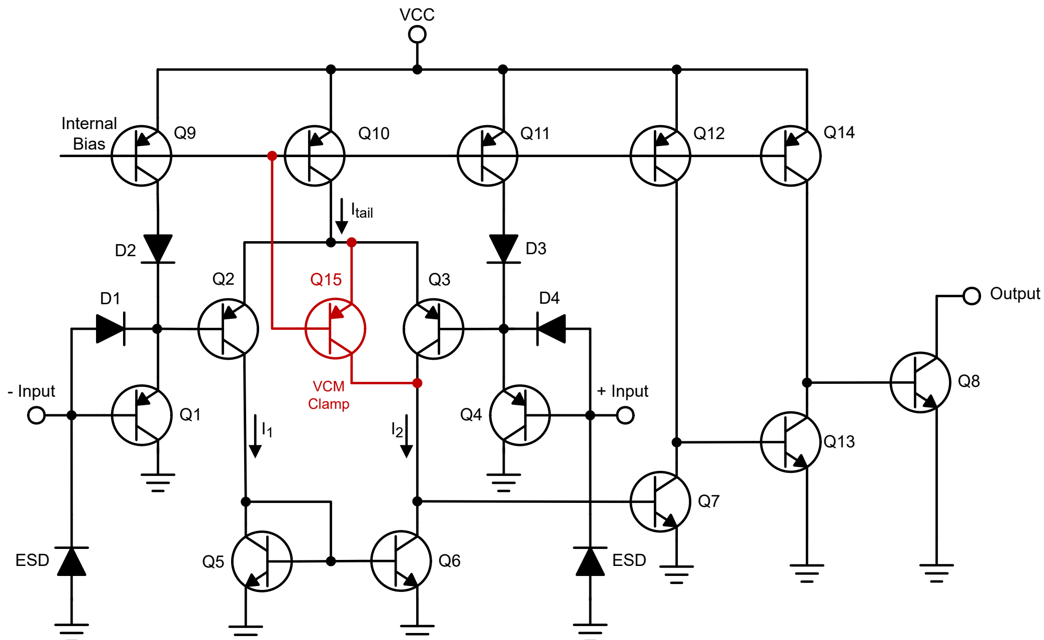
6.1 Overview

The TL331 family is a single comparator with the ability to operate up to 36V on the supply pin. This standard device has proven ubiquity and versatility across a wide range of applications. This is due to its very wide supply voltages range (2V to 36V), low Iq, and fast response.

The open-collector output allows the user to configure the output's logic low voltage (V_{OL}) and can be utilized to enable the comparator to be used in AND functionality.

The TL331B and TL391B are performance upgrades to standard TL331 using the latest process technologies allowing for lower offset voltages, lower input bias and supply currents and faster response time over an extended temperature range. The TL331B can drop-in replace the "I" or "K" versions of TL331. The TL391B is an alternate pinout for replacing competitive devices.

6.2 Functional Block Diagram



6.3 Feature Description

TL331x family consists of a PNP Darlington pair input, allowing the device to operate with very high gain and fast response with minimal input bias current. The input Darlington pair creates a limit on the input common mode voltage capability, allowing TL331x to accurately function from ground to V_{CC} – 1.5V differential input. In later revisions, a clamp was added around Q3 to mimic the outside-of-input voltage range behavior of the original classic silicon.

The output consists of an open collector NPN (pull-down or low side) transistor. The output NPN will sink current when the negative input voltage is higher than the positive input voltage and the offset voltage. The VOL is resistive and will scale with the output current. Please see the "Output Low Voltage vs. Output Sinking Current" graphs in Typical Characteristics for V_{OL} values with respect to the output current.

6.4 Device Functional Modes

6.4.1 Voltage Comparison

The TL331x operates solely as a voltage comparator, comparing the differential voltage between the positive and negative pins and outputting a logic low or high impedance (logic high with pull-up) based on the input differential polarity.

7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

TL331x will typically be used to compare a single signal to a reference or two signals against each other. Many users take advantage of the open drain output to drive the comparison logic output to a logic voltage level to an MCU or logic device. The wide supply range and high voltage capability makes TL331x optimal for level shifting to a higher or lower voltage.

7.2 Typical Application

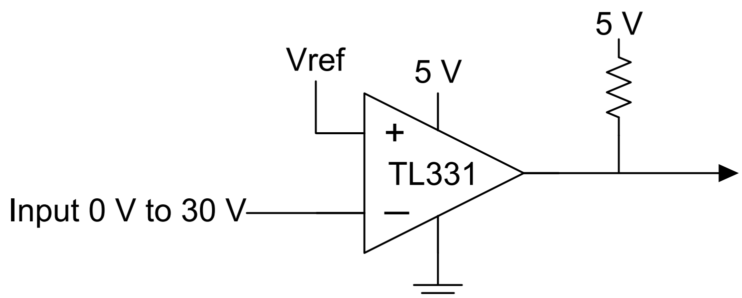


図 7-1. Typical Application Schematic

7.2.1 Design Requirements

For this design example, use the parameters listed in 表 7-1 as the input parameters.

表 7-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	0V to V_{CC} – 1.5V
Supply Voltage	2V to 36V
Logic Supply Voltage (R_{PULLUP} Voltage)	2V to 36V
Output Current (V_{LOGIC}/R_{PULLUP})	1μA to 4mA
Input Overdrive Voltage	100mV
Reference Voltage	2.5V
Load Capacitance (C_L)	15pF

7.2.2 Detailed Design Procedure

When using TL331x in a general comparator application, determine the following:

- Input voltage range
- Minimum overdrive voltage
- Output and drive current
- Response time

7.2.2.1 Input Voltage Range

When choosing the input voltage range, the input common mode voltage range (V_{ICR}) must be taken in to account. If temperature operation is above or below 25°C the V_{ICR} can range from 0V to V_{CC} – 1.5V. This limits the input voltage range to as high as V_{CC} – 1.5V and as low as 0V. Operation outside of this range can yield incorrect comparisons.

Below is a list of input voltage situation and their outcomes:

1. When both IN- and IN+ are both within the common mode range:
   a. If IN- is higher than IN+ and the offset voltage, the output is low and the output transistor is sinking current
   b. If IN- is lower than IN+ and the offset voltage, the output is high impedance and the output transistor is not conducting
2. When IN- is higher than common mode and IN+ is within common mode, the output is low and the output transistor is sinking current
3. When IN+ is higher than common mode and IN- is within common mode, the output is high impedance and the output transistor is not conducting
4. When IN- and IN+ are both higher than common mode, please see the *Both Inputs Above Input Range Behavior* section of the LM339 Family Application Note (SNOAA35).

7.2.2.2 Minimum Overdrive Voltage

Overdrive Voltage is the differential voltage produced between the positive and negative inputs of the comparator over the offset voltage (V_{IO}). To make an accurate comparison the Overdrive Voltage (V_{OD}) should be higher than the input offset voltage (V_{IO}). Overdrive voltage can also determine the response time of the comparator, with the response time decreasing with increasing overdrive. 図 7-2 and 図 7-3 show positive and negative response times with respect to overdrive voltage.

7.2.2.3 Output and Drive Current

Output current is determined by the load/pull-up resistance and logic/pull-up voltage. The output current produces a output low voltage (V_{OL}) from the comparator. In which V_{OL} is proportional to the output current. Use *Output Low Voltage vs Output Current (I_{OL})* to determine V_{OL} based on the output current.

The output current can also effect the transient response. More is explained in the next section.

7.2.2.4 Response Time

Response time is a function of input over drive. See *セクション 7.2.3* for typical response times. The rise and fall times can be determined by the load capacitance (C_L), load/pullup resistance (R_{PULLUP}), and equivalent collector-emitter resistance (R_{CE}).

- The rise time (τ_R) is approximately $\tau_R \sim R_{PULLUP} \times C_L$
- The fall time (τ_F) is approximately $\tau_F \sim R_{CE} \times C_L$
  – R_{CE} can be determined by taking the slope of *Output Low Voltage vs Output Current (I_{OL})* in its linear region at the desired temperature, or by dividing the V_{OL} by I_{out}

7.2.3 Application Curves

The following curves were generated with 5V on V_{CC} and V_{Logic}, R_{PULLUP} = 5.1kΩ, and 50pF scope probe.

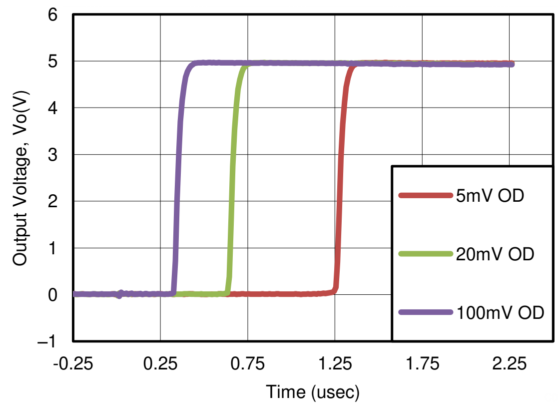


図 7-2. Response Time for Various Overdrives (Positive Transition)

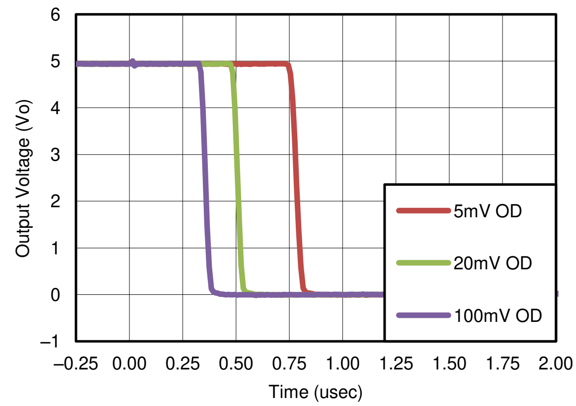


図 7-3. Response Time for Various Overdrives (Negative Transition)

7.2.4 ESD Protection

The "B" and TiB versions add dedicated ESD protections on all the pins for improved ESD performance. Please see Application Note SNOAA35 for more information.

7.2.5 Power Supply Recommendations

For fast response and comparison applications with noisy or AC inputs, it is recommended to use a bypass capacitor on the supply pin to reject any variation on the supply voltage. This variation can eat into the comparator's input common mode range and create an inaccurate comparison.

7.2.6 Layout

7.2.6.1 Layout Guidelines

For accurate comparator applications without hysteresis it is important maintain a stable power supply with minimized noise and glitches, which can affect the high level input common mode voltage range. To achieve this, it is best to add a bypass capacitor between the supply voltage and ground. This should be implemented on the positive power supply and negative supply (if available). If a negative supply is not being used, do not put a capacitor between the IC's GND pin and system ground.

7.2.6.2 Layout Example

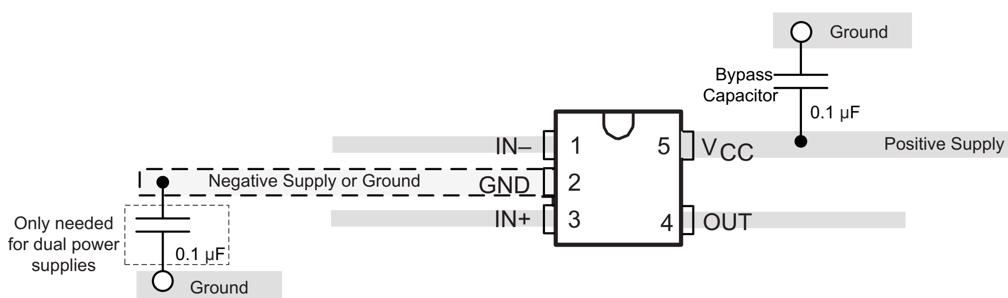


図 7-4. TL331 Layout Example

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

Application Design Guidelines for LM339, LM393, TL331 Family Comparators - SNOAA35

Analog Engineers Circuit Cookbook: Amplifiers (See Comparators section) - SLYY137

Precision Design, Comparator with Hysteresis Reference Design- TIDU020

Window comparator circuit - SBOA221

Reference Design, Window Comparator Reference Design- TIPD178

Comparator with and without hysteresis circuit - SBOA219

Inverting comparator with hysteresis circuit - SNOA997

Non-Inverting Comparator With Hysteresis Circuit - SBOA313

Zero crossing detection using comparator circuit - SNOA999

PWM generator circuit - SBOA212

How to Implement Comparators for Improving Performance of Rotary Encoder in Industrial Drive Applications - SNOAA41

A Quad of Independently Func Comparators - SNOA654

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

8.4 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

8.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision K (September 2023) to Revision L (November 2024) **Page**

Changes from Revision J (November 2020) to Revision K (September 2023) **Page**

Changes from Revision I (August 2020) to Revision J (November 2020) **Page**

Changes from Revision H (April 2020) to Revision I (August 2020) **Page**

Changes from Revision G (January 2015) to Revision H (April 2020) **Page**

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、テキサス・インスツルメンツの販売条件、または ti.com やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL331BIDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	331B
TL331BIDBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	331B
TL331BIDBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	331B
TL331BIDBVRG4.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	331B
TL331IDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(T1I8, T1IG, T1IL, T1IS)
TL331IDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(T1I8, T1IG, T1IL, T1IS)
TL331IDBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(T1I8, T1IG, T1IL, T1IU)
TL331IDBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(T1I8, T1IG, T1IL, T1IU)
TL331IDBVT.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(T1I8, T1IG, T1IL, T1IU)
TL331KDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 105	(T1K8, T1KG, T1KJ, T1KL)
TL331KDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	(T1K8, T1KG, T1KJ, T1KL)
TL331KDBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	(T1K8, T1KG, T1KJ, T1KL)
TL331KDBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	(T1K8, T1KG, T1KJ, T1KL)
TL331KDBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	(T1K8, T1KG, T1KJ, T1KL)
TL331KDBVT.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	(T1K8, T1KG, T1KJ, T1KL)
TL391BIDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	391B
TL391BIDBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	391B

(1) **Status:** For more details on status, see our product life cycle.

[2] **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

[3] **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[4] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TL331, TL331B, TL391B :

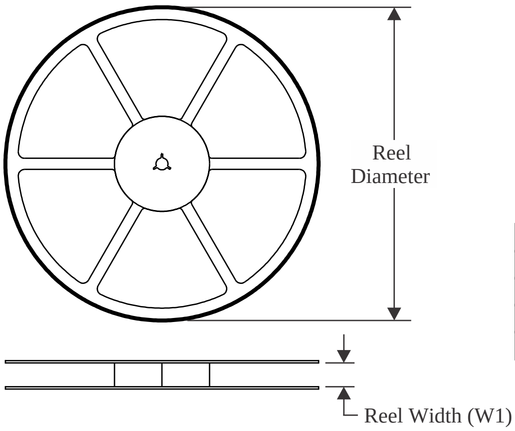
- Automotive : TL331-Q1, TL331B-Q1, TL391B-Q1
- Enhanced Product : TL331-EP

NOTE: Qualified Version Definitions:

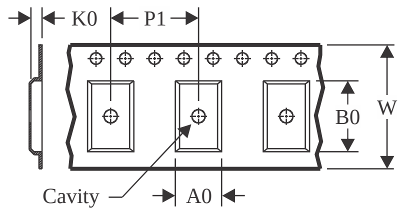
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

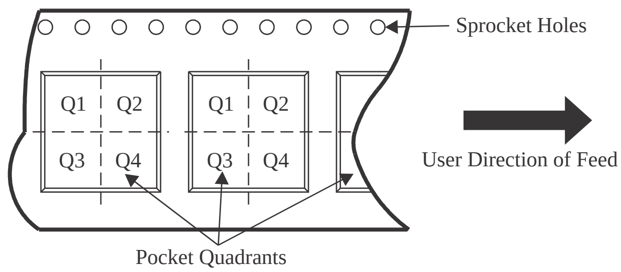


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

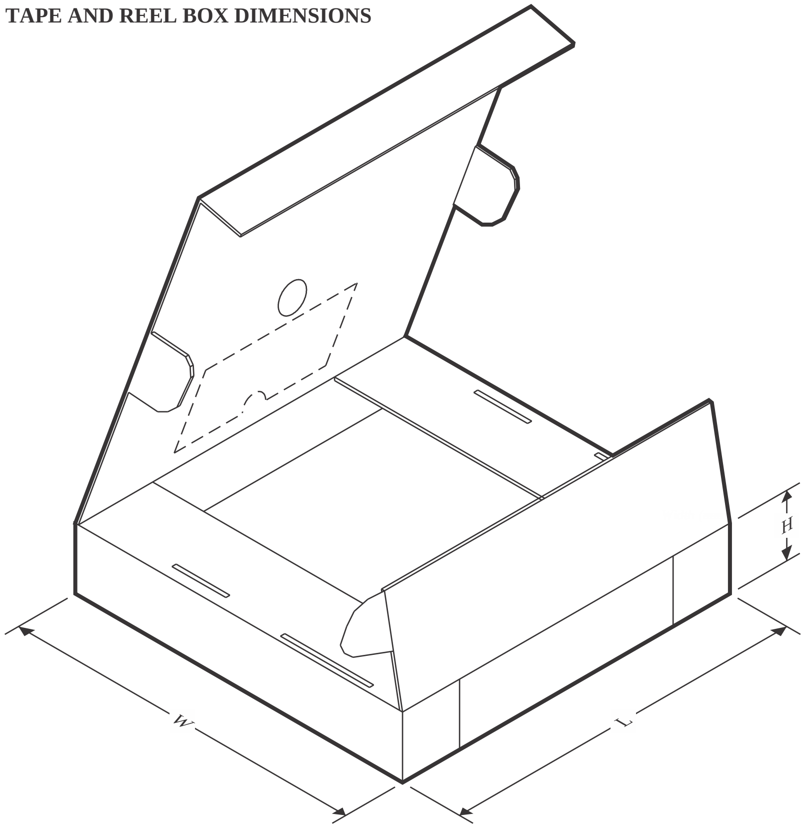
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

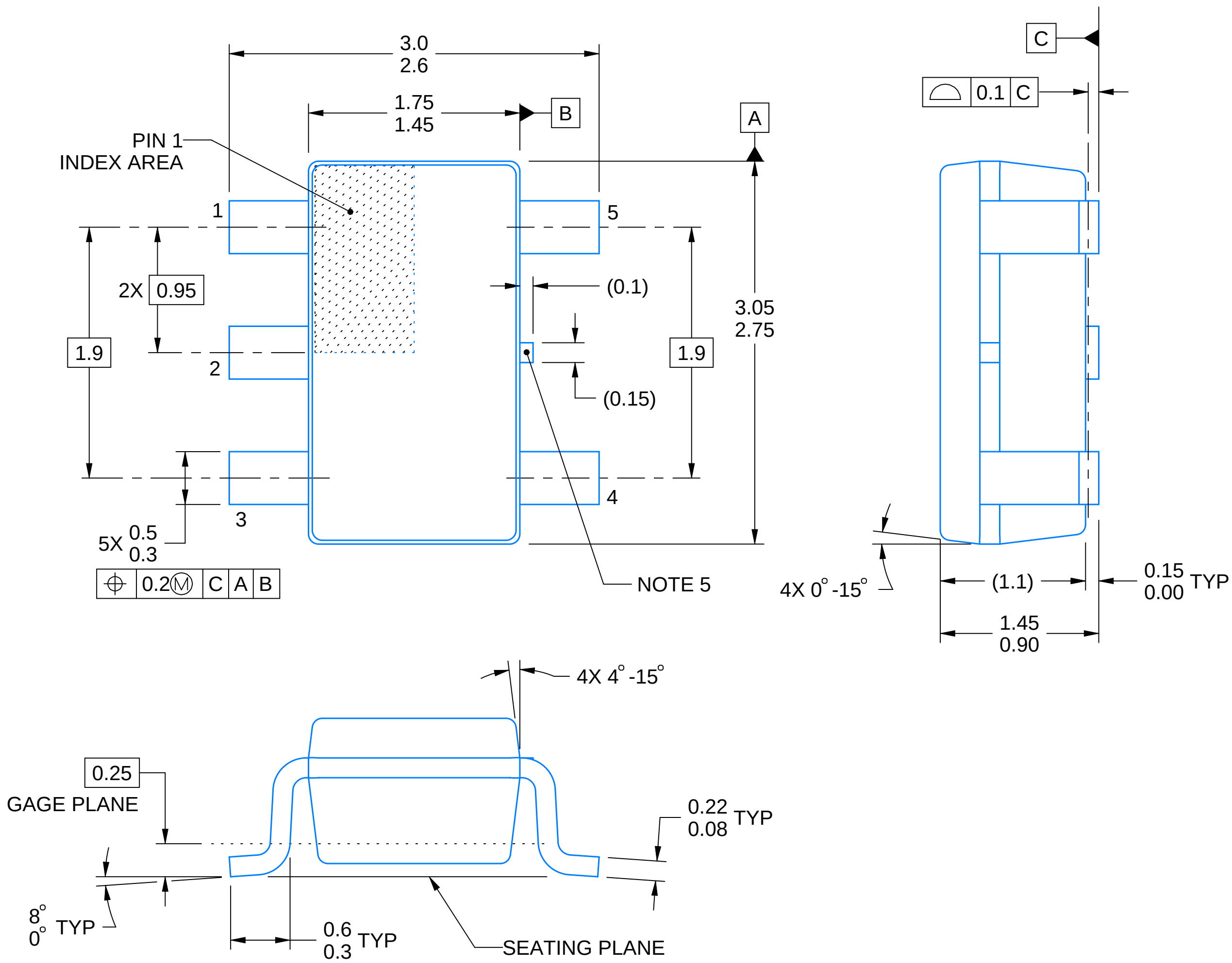
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL331BIDBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL331BIDBVRG4	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL331IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL331IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL331IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL331IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL331KDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL331KDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL331KDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL391BIDBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

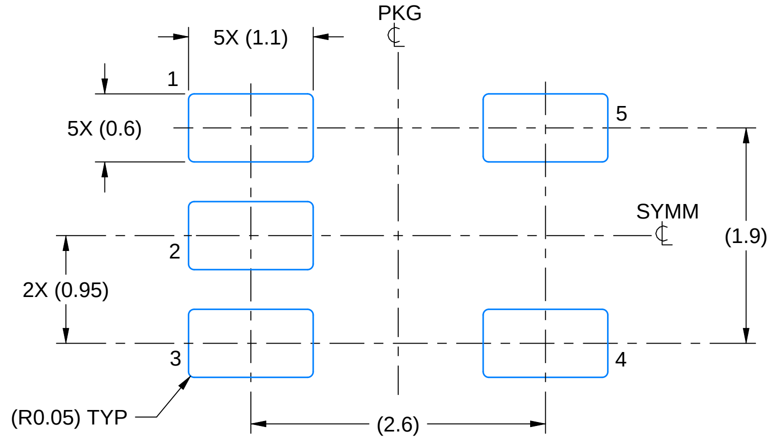
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL331BIDBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TL331BIDBVRG4	SOT-23	DBV	5	3000	210.0	185.0	35.0
TL331IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TL331IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TL331IDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TL331IDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TL331KDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TL331KDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TL331KDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TL391BIDBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0



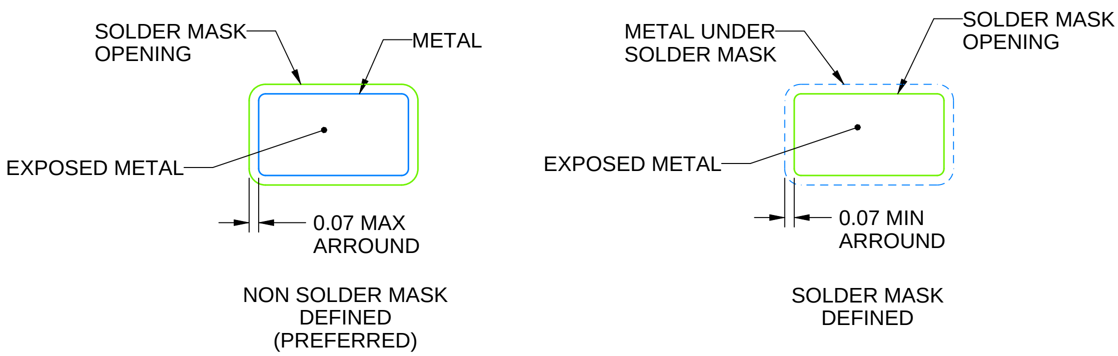
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

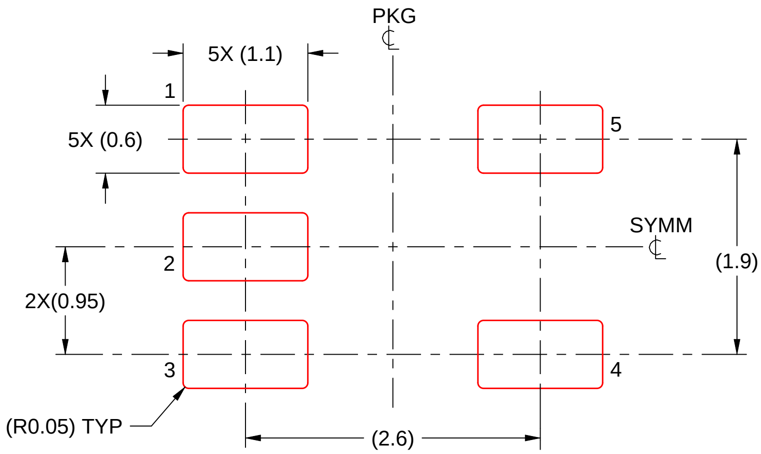


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項