TL3474, TL3474A High-Slew-Rate, Single-Supply Operational Amplifiers

1 Features

- Low offset: 3mV (max) for A-grade
- Wide gain-bandwidth product: 4.5MHz
- Wide-range single-supply operation: 4V to 36V
- Wide input common-mode range includes ground (V_{CC-})
- Output short-circuit protection
- Alternative to MC33074/A and MC34074/A

2 Applications

- Multiplexed data-acquisition systems
- Test and measurement equipment
- ADC driver amplifiers
- SAR ADC reference buffers
- Programmable logic controllers
- Low-side current sensing

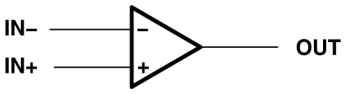
3 Description

Quality, low-cost, bipolar fabrication with remarkable design concepts is employed for the TL3474 and TL3474A operational amplifiers. These devices offer 4.5MHz of gain-bandwidth product. Although the TL3474 and TL3474A can be operated from split supplies, these devices are designed for single-supply operation because the common-mode input voltage range includes ground potential (V_{CC-}). These devices exhibit high input resistance, low input offset voltage, and high gain. The low-cost TL3474 is a good alternative to the MC34074/A and MC33074/A operational amplifiers.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TL3474	D (SOIC, 14)	8.65mm × 6.00mm
	PW (TSSOP, 14)	5.00mm × 6.40mm
	N (PDIP, 14)	19.30mm × 9.40mm

(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Symbol (Each Amplifier)

Table of Contents

4 Pin Configuration and Functions

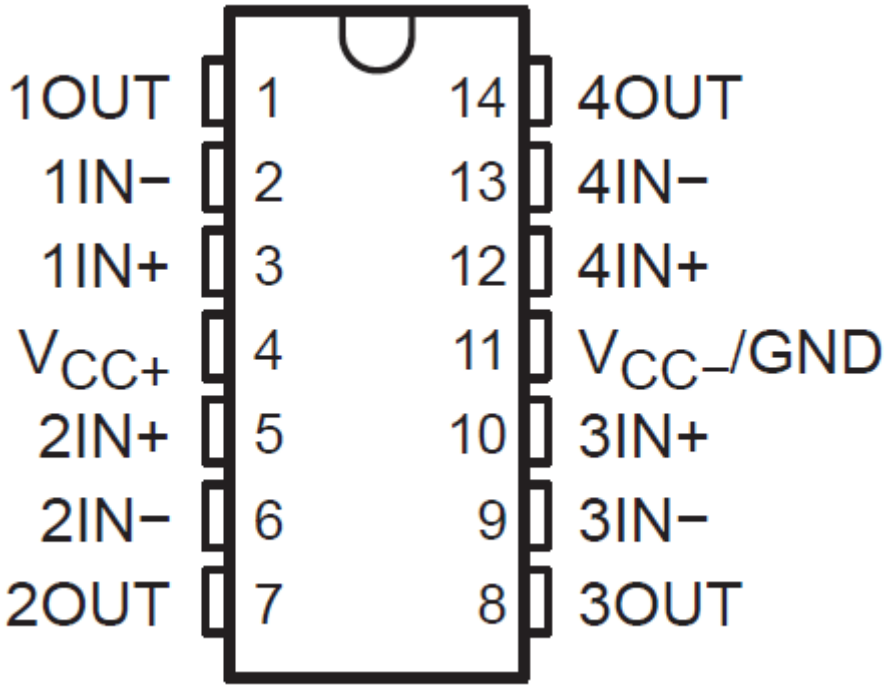


Figure 4-1. D, N, or PW Package
Top View

Table 4-1. Pin Functions: TL3474

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
1OUT	1	O	Output channel 1
1IN–	2	I	Inverting input channel 1
1IN+	3	I	Non inverting input channel 1
VCC+	4	—	Positive Input supply voltage
2IN+	5	I	Non inverting input channel 2
2IN–	6	I	Inverting input channel 2
2OUT	7	O	Output channel 2
3OUT	8	O	Output channel 3
3IN–	9	I	Inverting input channel 3
3IN+	10	I	Non inverting input channel 3
VCC– / GND	11	—	Negative Input supply voltage or Ground
4IN+	12	I	Non inverting input channel 4
4IN–	13	I	Inverting input channel 4
4OUT	14	O	Output channel 4

(1) I = input and O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
	Supply voltage(2)	V_{CC+}		18	V
		V_{CC-}		–18	
V_{ID}	Differential input voltage(3)		–36	36	V
V_I	Input voltage	Any input	V_{CC-}	V_{CC+}	
I_I	Input current	Each input	–1	1	mA
I_O	Output current		–80	80	mA
	Total current into V_{CC+}			80	mA
	Total current out of V_{CC-}			80	mA
	Duration of short-circuit current at (or below) 25°C(4)			Unlimited	
θ_{JA}	Package thermal impedance(5) (6)	D package		86	°C/W
		N package		80	
		PW package		113	
T_J	Operating virtual junction temperature			150	°C
	Lead temperature 1.6mm (1/16 inch) from case for 10 seconds			260	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}/GND.
(3) Differential voltages are at the noninverting input with respect to the inverting input. Excessive input current can flow when the input is less than V_{CC-}− 0.3V.
(4) The output can be shorted to either supply. Limit temperature and supply voltages so that the maximum dissipation rating is not exceeded.
(5) Maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.

5.2 Recommended Operating Conditions

			MIN	MAX	UNIT
$V_{CC\pm}$	Supply voltage		4	36	V
V_{IC}	Common-mode input voltage	V_{CC} = 5V	0	2.8	V
		$V_{CC\pm}$ = ±15V	−15	12.8	
T_A	Operating free-air temperature	TL3474C, TL3474AC	0	70	°C
		TL3474I, TL3474AI	−40	105	

5.3 Electrical Characteristics

at specified free-air temperature, $V_{CC\pm}$ = ±15V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	TL3474			TL3474A			UNIT
					MIN	TYP(1)	MAX	MIN	TYP†	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50Ω	V_{CC} = 5V	25°C		1.5	10		1.5	3	mV
			V_{CC} = ±15V	25°C		1.0	10		1.0	3	
				Full range(2)			12			5	
a_{VIO}	Temperature coefficient of input offset voltage		V_{CC} = ±15V	Full range(2)		10			10		µV/°C
I_{IO}	Input offset current		V_{CC} = ±15V	25°C		0.01	75		0.01	75	nA
				Full range(2)			300			0.01	
I_{IB}	Input bias current		V_{CC} = ±15V	25°C		0.01	500		0.01	500	nA
				Full range(2)			700			0.01	
V_{ICR}	Common-mode input voltage range	R_S = 50Ω		25°C		−15 to 12.8			−15 to 12.8		V
				Full range(2)		−15 to 12.8			−15 to 12.8		
V_{OH}	High-level output voltage	V_{CC+} = 5V, V_{CC-} = 0, R_L = 2kΩ		25°C	3.7	4.8		3.7	4.8		V
		R_L = 10kΩ		25°C	13.6	14.8		13.6	14.8		
		R_L = 2kΩ		Full range(2)	13.4			13.4			
V_{OL}	Low-level output voltage	V_{CC+} = 5V, V_{CC-} = 0, R_L = 2kΩ		25°C		0.005	0.3		0.005	0.3	V
		R_L = 10kΩ		25°C		−14.8	−14.3		−14.8	−14.3	
		R_L = 2kΩ		Full range(2)			−13.5			−13.5	
A_{VD}	Large-signal differential voltage amplification	V_O = ±10V, R_L = 2kΩ		25°C	25	100		25	100		V/mV
				Full range(2)	20			20			
I_{OS}	Short-circuit output current	Source: V_{ID} = 1V,	V_O = 0	25°C	−10	−75		−10	−75		mA
		Sink: V_{ID} = −1V,	V_O = 0		20	75		20	27		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}(min),	R_S = 50Ω	25°C	65	97		80	97		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±13.5V to ±16.5V, R_S = 100Ω		25°C	70	97		70	97		dB
I_{CC}	Supply current (per channel)	V_O = 0	No load	25°C		0.56	4.5		0.56	4.5	mA
				Full range(2)			5.5			5.5	
		V_{CC+} = 5V, V_O = 2.5V, V_{CC-} = 0, No load		25°C			4.5			4.5	

(1) All typical values are at T_A = 25°C.
(2) Full range is 0°C to 70°C for the TL3474C, TL3474AC devices and −40°C to 105°C for the TL3474I, TL3474AI devices.

5.4 Operating Characteristics

$V_{CC±}$ = ±15V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TL3474			TL3474A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	V_I = −10V to 10V, R_L = 2kΩ, C_L = 300pF	A_V = 1	8	10		8	10		V/µs
SR−	Negative slew rate		A_V = −1		13			13		
	Small Signal Slew-Rate	V_I= −0.1V to 0.1V			0.5			0.5		V/µs
t_s	Settling time	A_{VD} = −1, 10V step	To 0.1%		2			2		µs
			To 0.01%		2.5			2.5		
V_n	Equivalent input noise voltage	f = 1kHz,	R_S = 100Ω		10.8			10.8		nV/√Hz
I_n	Equivalent input noise current	f = 1kHz			2			2		fA/√Hz
THD	Total harmonic distortion	$V_{O(PP)}$ = 2V to 20V, R_L = 2kΩ, A_{VD} = 10, f = 10kHz			0.02			0.02		%
GBW	Gain-bandwidth product	f =100 kHz			4.5			4.5		MHz
BW	Power bandwidth	$V_{O(PP)}$ = 20V, R_L = 2kΩ, A_{VD} = 1, THD = 5.0%			85			85		kHz
φ_m	Phase margin	R_L = 2kΩ,	C_L = 0		70			70		deg
		R_L = 2kΩ,	C_L = 300pF		50			50		
	Gain margin	R_L = 2kΩ,	C_L = 0		12			12		dB
		R_L = 2kΩ,	C_L = 300pF		4			4		
r_i	Differential input resistance	V_{IC} = 0			540			540		GΩ
C_i	Input capacitance	V_{IC} = 0			10			10		pF
	Channel separation	f = 10kHz			101			101		dB
z_o	Open-loop output impedance	f = 1MHz,	A_V = 1		525			525		Ω

5.5 Typical Characteristics

T_A = 25°C (unless otherwise noted)

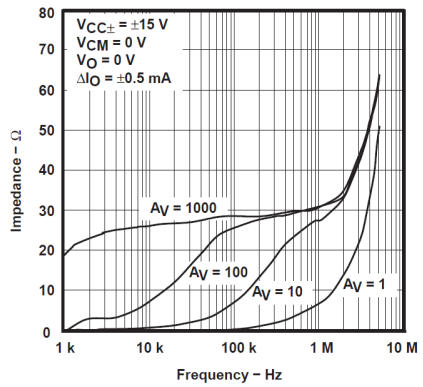


Figure 5-1. Output Impedance vs Frequency, Old Die

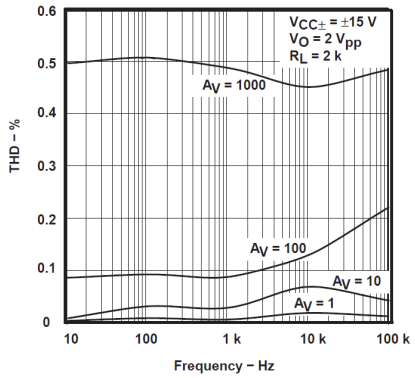


Figure 5-2. Total Harmonic Distortion vs Frequency, Old Die

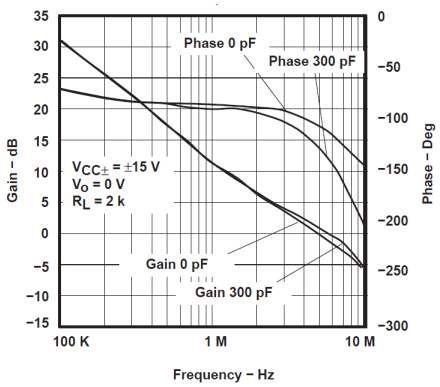


Figure 5-3. Gain and Phase vs Frequency, Old Die

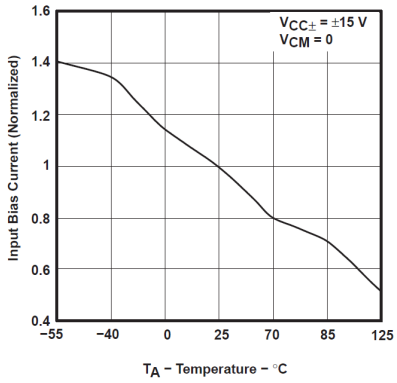


Figure 5-4. Normalized Input Bias Current vs Temperature, Old Die

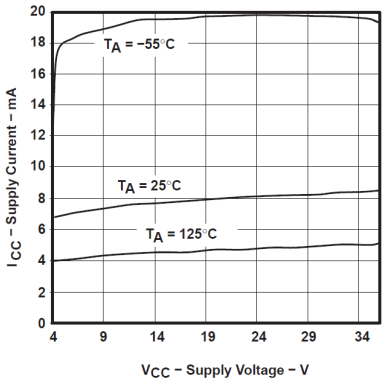


Figure 5-5. Supply Current vs Supply Voltage, Old Die

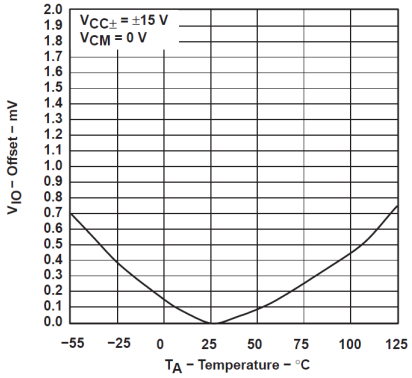


Figure 5-6. Offset Voltage Drift vs Temperature, Old Die

5.5 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

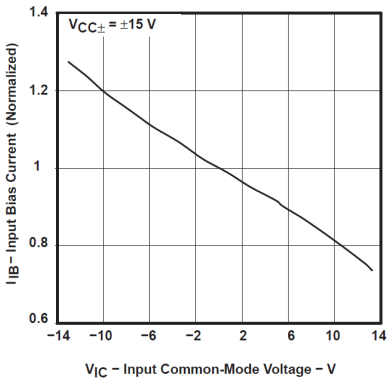


Figure 5-7. Normalized Input Bias Current vs Input Common-Mode Voltage, Old Die

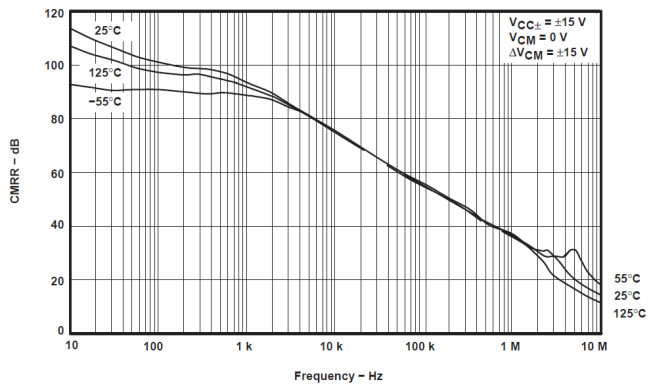
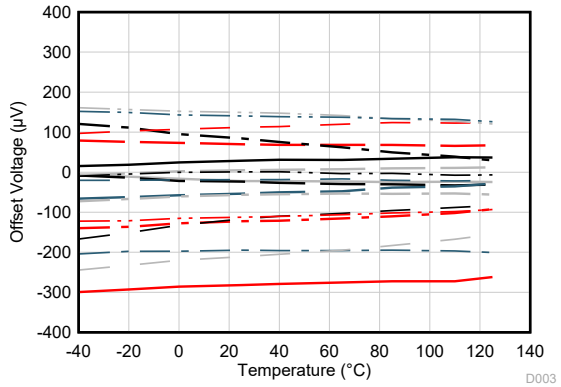
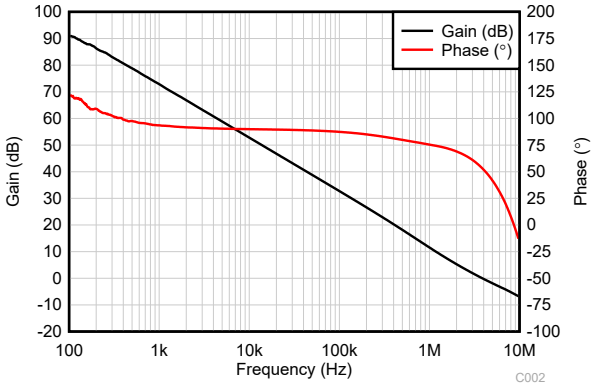


Figure 5-8. Common-Mode Rejection vs Frequency, Old Die



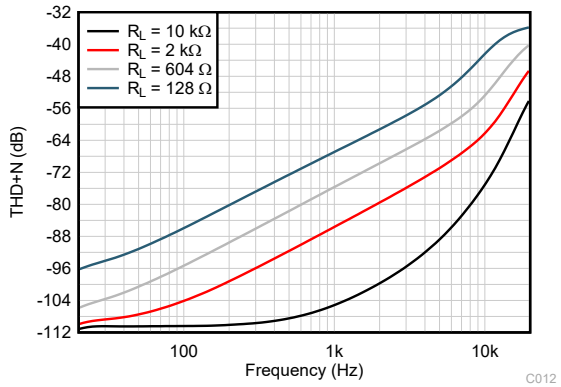
V_{CM} = V–

Figure 5-9. Offset Voltage vs Temperature, New Die



C_L = 20pF

Figure 5-10. Open-Loop Gain and Phase vs Frequency, New Die



BW = 80kHz, V_{OUT} = 1V_{RMS}

Figure 5-11. THD+N Ratio vs Frequency, New Die

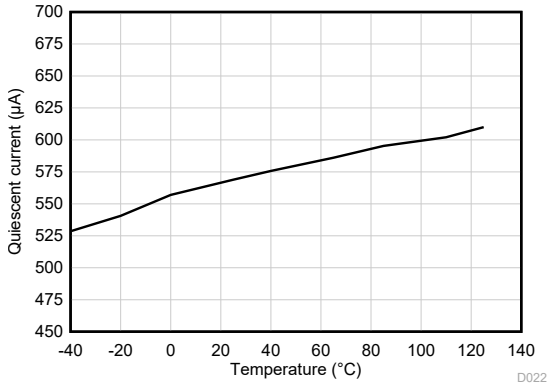


Figure 5-12. Quiescent Current vs Temperature, New Die

5.5 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

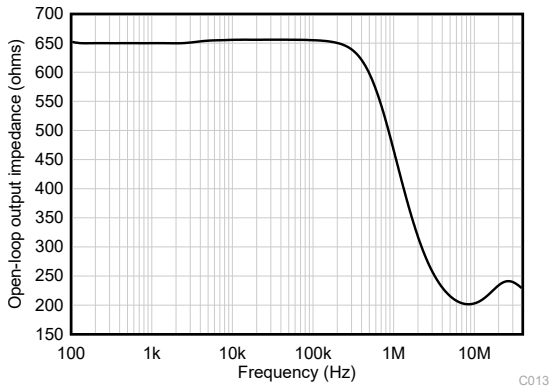


Figure 5-13. Open-Loop Output Impedance vs Frequency, New Die

5.6 Old Die to New Die Transition

As of the publication of revision C of this datasheet, Texas Instruments has moved manufacturing of the die for TL3474 to a modern fabrication site. The two different die are referred to in this document as “old” (previous fabrication site) and “new” die (current fabrication site). The die origin can be separated from the “Chip Source Origin” (CSO) parameter in the shipping information. The old die CSO is “SHE”, for the new die the CSO is “RFB”. The old die information is maintained in this datasheet for comparison purposes, but all new manufacturing has moved to the new die.

6 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop designs are listed below.

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

6.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

6.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (July 2003) to Revision C (June 2026)	Page
• Changed datasheet structure and organization. Added, updated, or renamed the following sections: Features, Applications, Description, Absolute Maximum Ratings, Recommended Operating Conditions, Old Die to New Die Transition, Device and Documentation Support; Mechanical, Packaging, and Ordering Information	1
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Changed Wide gain bandwidth product from 4MHz to 4.5MHz	1
• Deleted High slew rate: 13V/µs	1
• Deleted Fast settling time 1.1µs to 0.1%	1
• Deleted Low total harmonic distortion 0.02%	1
• Deleted Large-capacitance drive capability: 10,000 pF	1
• Updated the *Packaging Information* table in the *Description* section	1
• Changed Input offset current typical value for TL3474A max from 6nA to 0.01nA	5
• Changed Input bias current typical value for TL3474A max from 100nA to 0.01nA	5
• Changed High level output voltage typical values from 4V to 4.8V and 14V to 14.8V	5
• Changed Low level output voltage typical value from 0.1V to 0.005V	5
• Changed Supply current typical value from 3.5mA to 0.56mA	5
• Changed Short-circuit output current typical values from −34mA to −75mA and from 27mA to 75mA	5
• Deleted Supply current typical values at full range and VCC 5V conditions	5
• Changed Setting time from 1.1µs to 2µs	6
• Changed Equivalent input noise voltage from 49nV/√Hz to 10.8nV/√Hz	6

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL3474ACD	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	0 to 70	TL3474A
TL3474ACDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL3474A
TL3474ACDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL3474A
TL3474ACN	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL3474ACN
TL3474ACN.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL3474ACN
TL3474ACPW	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	0 to 70	T3474A
TL3474ACPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T3474A
TL3474ACPWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T3474A
TL3474AID	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 105	TL3474AI
TL3474AIDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	TL3474AI
TL3474AIDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	TL3474AI
TL3474AIDRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	TL3474AI
TL3474AIDRG4.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	TL3474AI
TL3474AIN	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	TL3474AIN
TL3474AIN.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	TL3474AIN
TL3474AIPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z3474A
TL3474AIPWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z3474A
TL3474CD	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	0 to 70	TL3474C
TL3474CDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL3474C
TL3474CDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL3474C
TL3474CN	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL3474CN
TL3474CN.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL3474CN
TL3474CPW	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	0 to 70	T3474
TL3474CPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	T3474
TL3474CPWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T3474
TL3474ID	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 105	TL3474I
TL3474IDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	TL3474I
TL3474IDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	TL3474I
TL3474IN	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	TL3474IN

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL3474IN.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	TL3474IN
TL3474IPW	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	-40 to 105	Z3474
TL3474IPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 105	Z3474
TL3474IPWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z3474

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

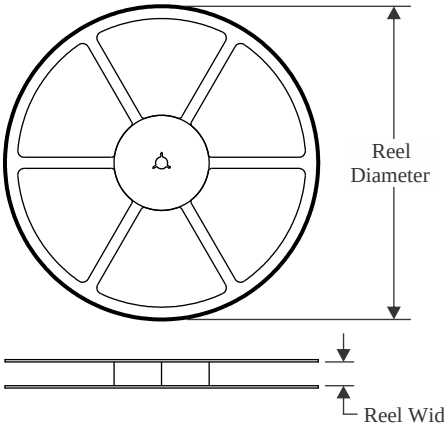
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

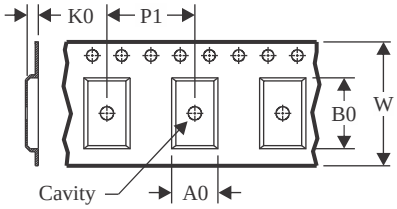
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

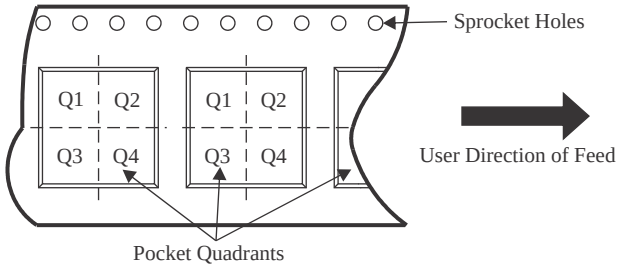


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

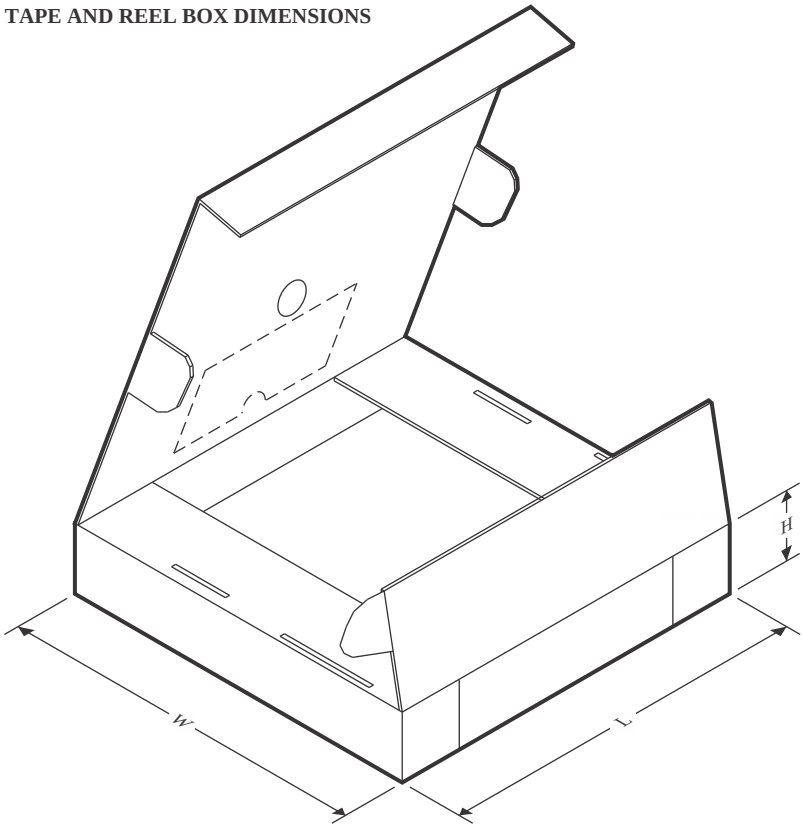
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL3474ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL3474ACPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL3474ACPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL3474AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL3474AIDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL3474AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL3474AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL3474CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL3474CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL3474IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL3474IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

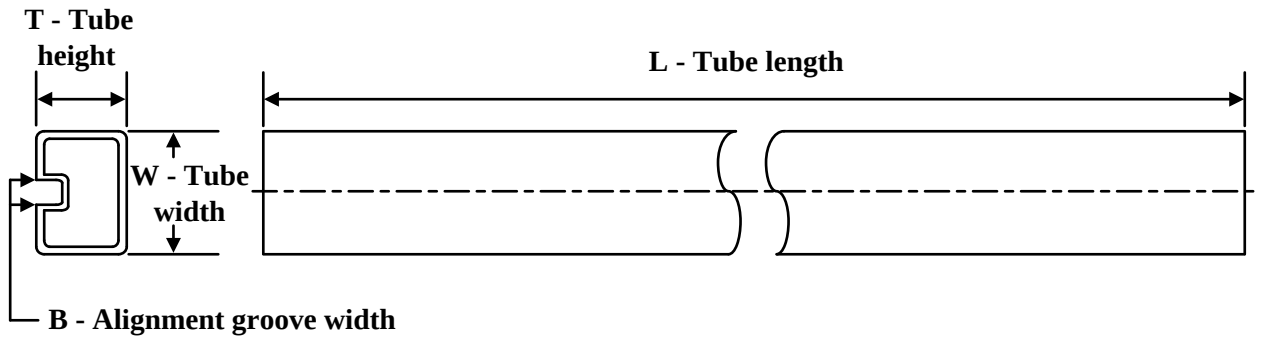
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

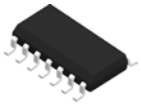
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL3474ACDR	SOIC	D	14	2500	340.5	336.1	32.0
TL3474ACPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TL3474ACPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TL3474AIDR	SOIC	D	14	2500	353.0	353.0	32.0
TL3474AIDRG4	SOIC	D	14	2500	353.0	353.0	32.0
TL3474AIPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TL3474AIPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TL3474CDR	SOIC	D	14	2500	353.0	353.0	32.0
TL3474CPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TL3474IDR	SOIC	D	14	2500	353.0	353.0	32.0
TL3474IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL3474ACN	N	PDIP	14	25	506	13.97	11230	4.32
TL3474ACN.A	N	PDIP	14	25	506	13.97	11230	4.32
TL3474AIN	N	PDIP	14	25	506	13.97	11230	4.32
TL3474AIN.A	N	PDIP	14	25	506	13.97	11230	4.32
TL3474CN	N	PDIP	14	25	506	13.97	11230	4.32
TL3474CN.A	N	PDIP	14	25	506	13.97	11230	4.32
TL3474IN	N	PDIP	14	25	506	13.97	11230	4.32
TL3474IN.A	N	PDIP	14	25	506	13.97	11230	4.32

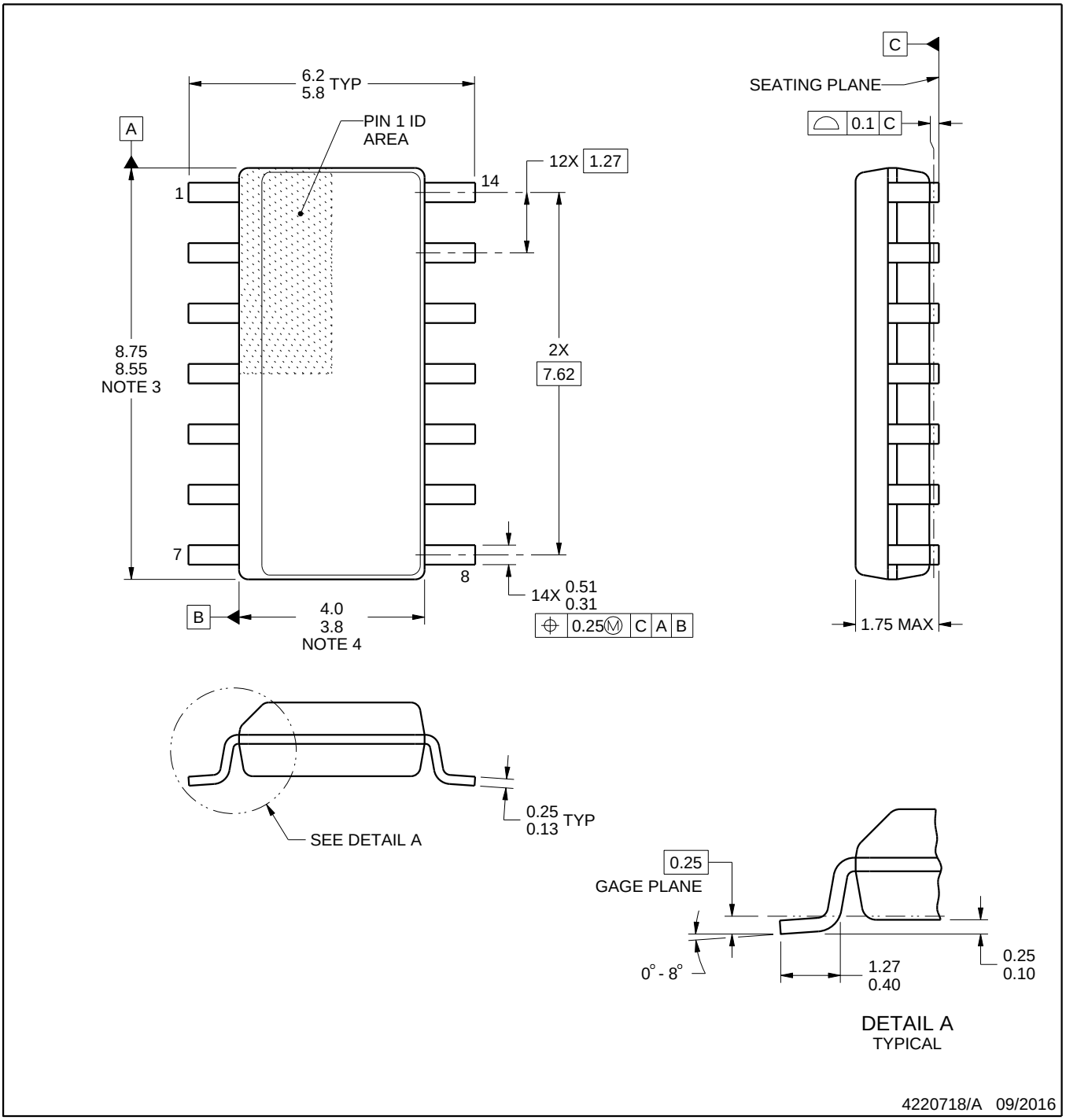


PACKAGE OUTLINE

D0014A

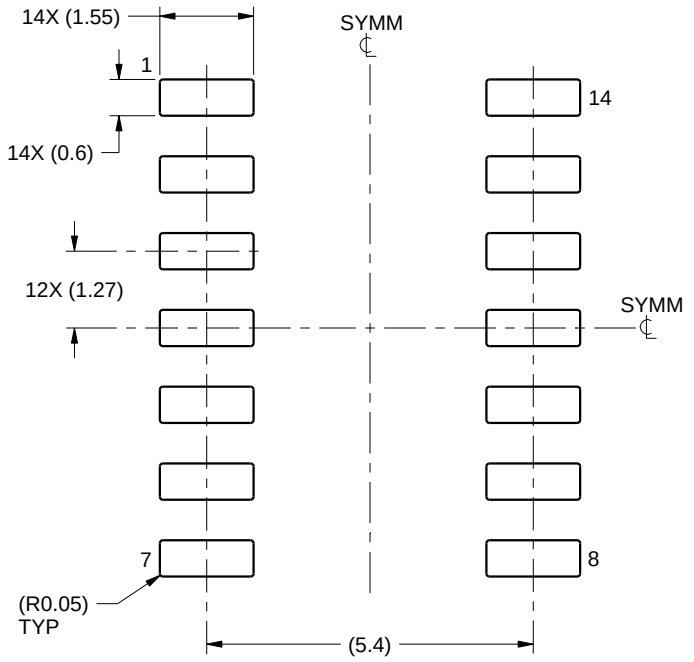
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

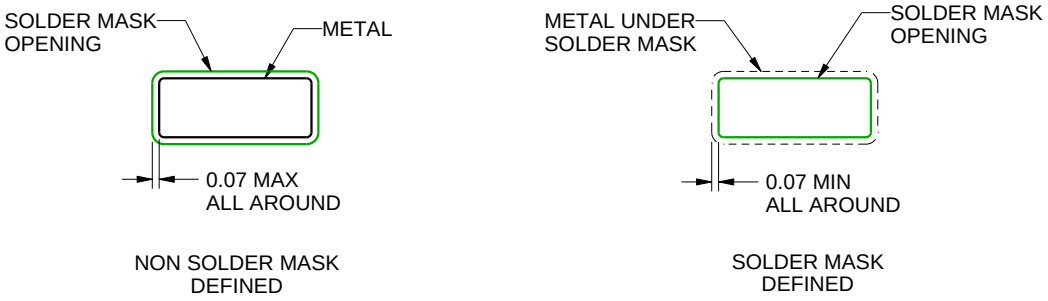


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

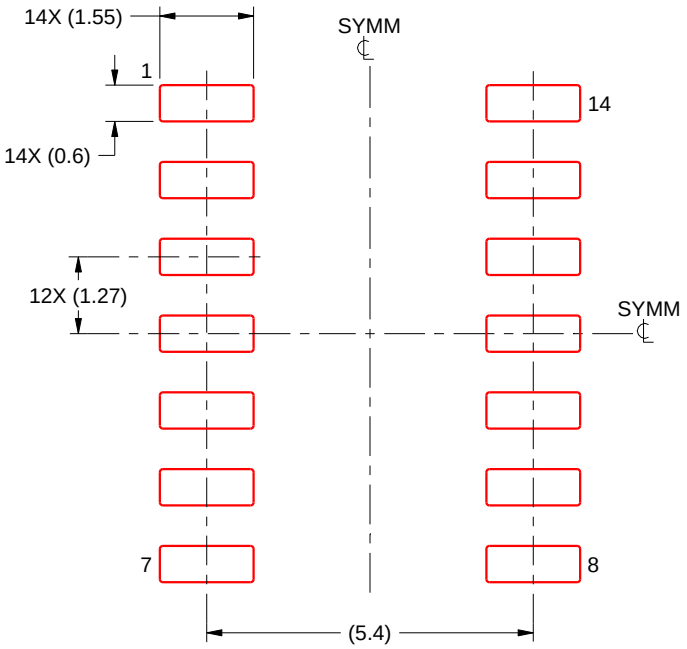
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

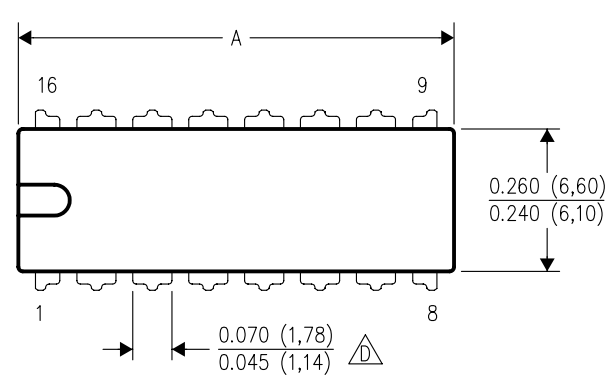
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

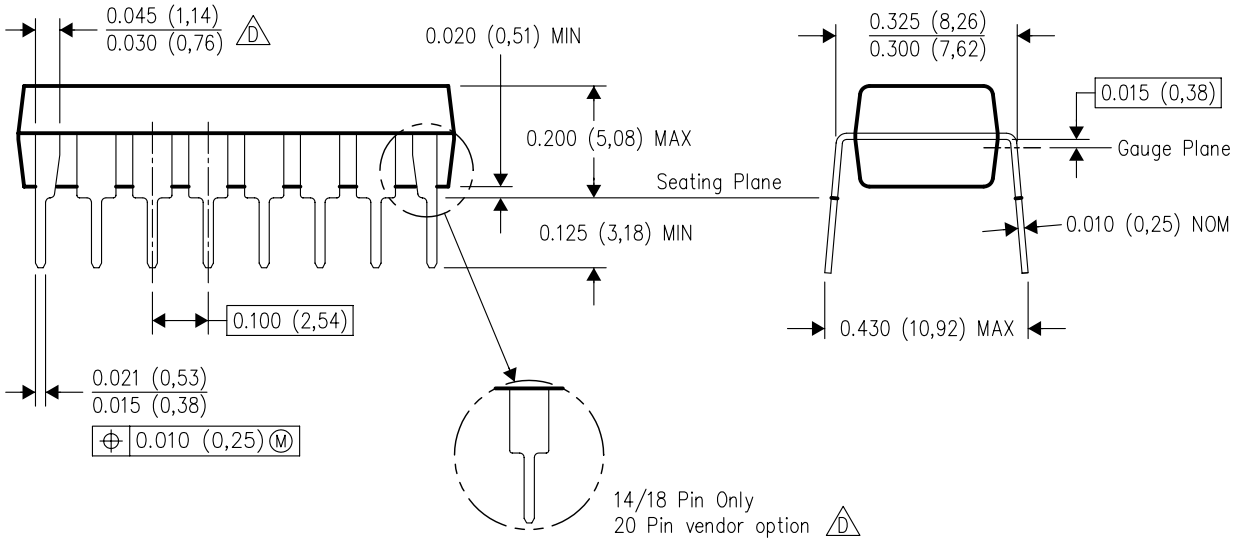
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

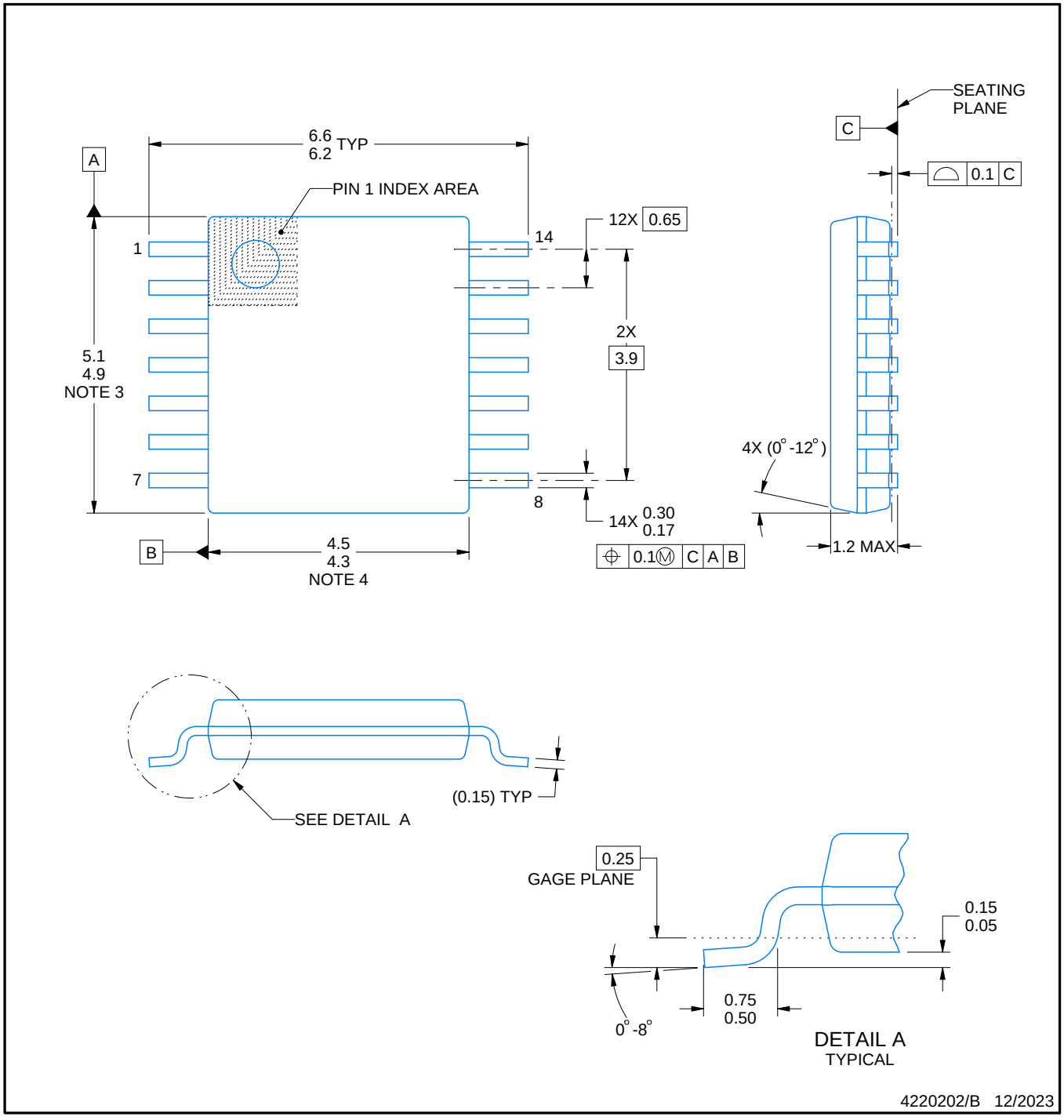
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

PW0014A

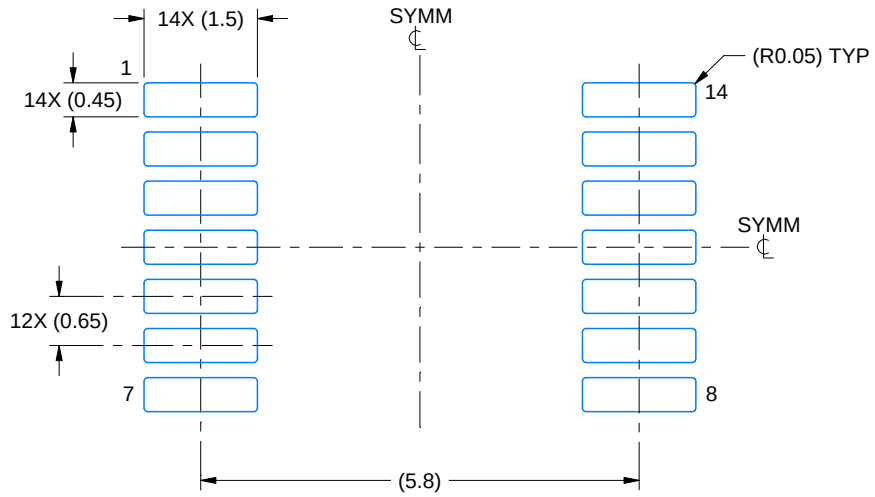
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

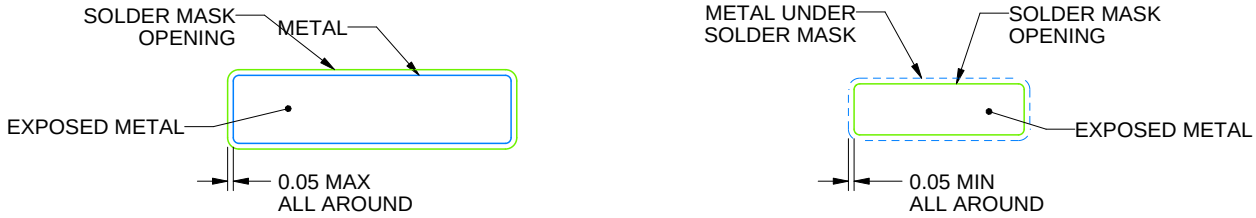


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

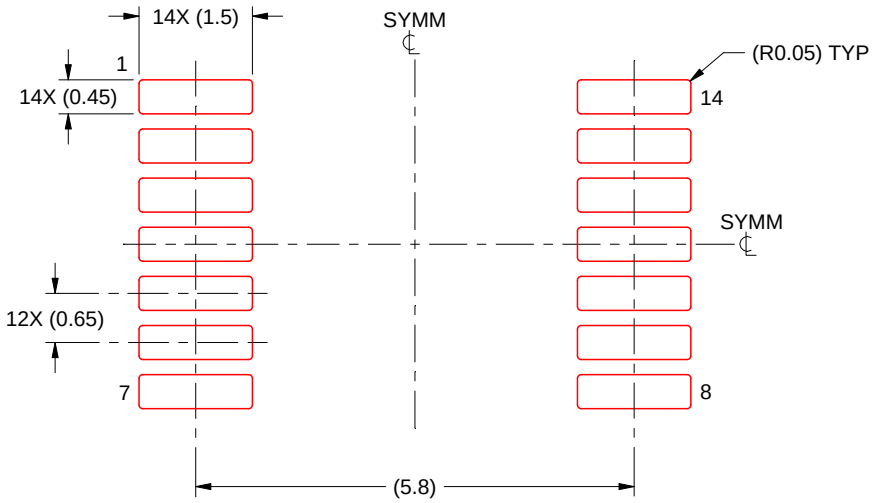


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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