TEXAS INSTRUMENTS
TL7702B, TL7705B, TL7733B
JAJSKL2O – SEPTEMBER 1989 – REVISED DECEMBER 2020

TL7702B、TL7733B、TL7705B 電源電圧監視 IC

1 特長

- パワーオン・リセット (POR) ジェネレータ
- 電圧低下後の自動リセット生成
- V_{CC} 1V 以上で規定された $\overline{\text{RESET}}$ 出力
- 高精度電圧センサ
- 温度補償付き電圧リファレンス
- 正論理および負論理のリセット出力
- 外部で調整可能なパルス幅

2 アプリケーション

- ワイヤレス通信システム
- ファクトリ・オートメーション
- ビル・オートメーション
- サーバー
- ノート PC およびデスクトップ PC
- STB および DVR

3 概要

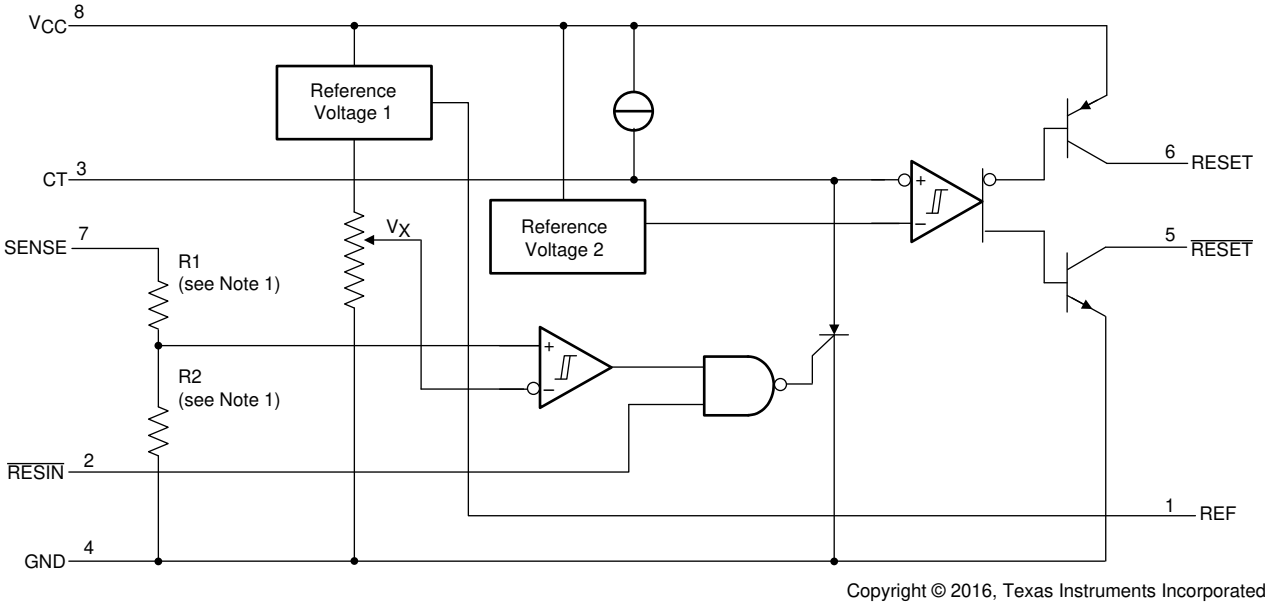
TL7702B、TL7705B、TL7733B は、マイクロコンピュータおよびマイクロプロセッサ・システムでリセット・コントローラとして使用するように設計された、電源電圧監視 IC です。この電源電圧監視 IC は、SENSE 入力の低電圧状態について電源を監視します。通常動作中に低電圧状態が発生すると、$\overline{\text{RESET}}$ および RESET 出力がアクティブになります。

TL7702BC、TL7705BC、TL7733BC は、0℃～70℃での動作が規定されています。TL7702BI、TL7705BI、TL7733BI は、-40℃～85℃での動作が規定されています。TL7705BQ は、-40℃～125℃での動作が規定されています。

デバイス情報(1)

部品番号	パッケージ	本体サイズ (公称)
TL77xxBD	SOIC (8)	4.90mm × 3.91mm
TL77xxBP	PDIP (8)	9.81mm × 6.35mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



機能ブロック図

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4 Revision History

Changes from Revision N (September 2016) to Revision O (December 2020) **Page**

- 文書全体にわたって表、図、相互参照の採番方法を更新 ... 1
- Corrected the $\overline{\text{RESIN}}$ pin description ... 3
- Corrected the I_{CC} parameter units from µA to mA in Electrical Characteristics Table ... 6

Changes from Revision M (May 2003) to Revision N (September 2016) **Page**

- 「*ESD 定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加。 ... 1
- 「*注文情報*」表を削除 (データシートの末尾にある POA を参照) ... 1
- Deleted Lead temperature row ... 4
- Changed $R_{\theta JA}$ for D (SOIC) from 97 to 109.2 and for P (PDIP) from 85 to 51.4 ... 5

5 Pin Configuration and Functions

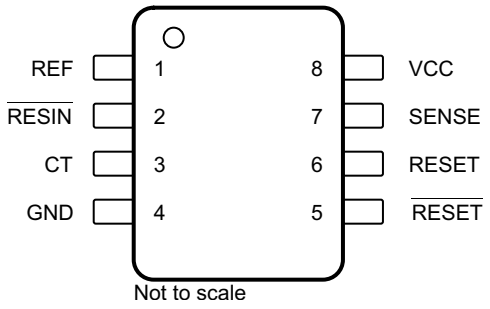


図 5-1. D or P Package 8-Pin SOIC or PDIP Top View

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CT	3	O	Timing capacitor input. The timing capacitor determines the time delay that the reset outputs remain active after the voltage at the SENSE input exceeds the positive-going threshold value.
GND	4	—	Ground
REF	1	O	Reference voltage. See *セクション 6.5* for reference voltage output and specification.
RESET	6	O	Active high reset. See 図 6-1 for RESET function and timing.
$\overline{\text{RESET}}$	5	O	Active low reset. See 図 6-1 for $\overline{\text{RESET}}$ function and timing.
$\overline{\text{RESIN}}$	2	I	Reset input. When the Reset Input is low, the RESET output goes high and the $\overline{\text{RESET}}$ goes low. When the Reset Input is high, the RESET and $\overline{\text{RESET}}$ outputs are allowed to trigger based on the SENSE voltage.
SENSE	7	I	Sense input. Voltage input to be supervised. See 図 6-1 for SENSE function and timing.
VCC	8	—	Supply voltage. See *セクション 6.3* for recommended voltage input range.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage(2), V_{CC}			20	V
Input voltage, V_I	$\overline{RESIN}$	–0.3	20	V
	SENSE	–0.3	20	
High-level output current, I_{OH} (RESET)			–30	mA
Low-level output current, I_{OL} ($\overline{RESET}$)			30	mA
Operating virtual junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		3.6	18	V
V_{IH}	High-level input voltage	$\overline{RESIN}$	2	18	V
V_{IL}	Low-level input voltage	$\overline{RESIN}$	0	0.8	V
V_I	Input voltage	SENSE	0	18	V
I_{OH}	High-level output current	RESET		–20	mA
I_{OL}	Low-level output current	$\overline{RESET}$		20	mA
T_A	Operating free-air temperature	TL77xxBC	0	70	°C
		TL77xxBI	–40	85	
		TL7705BQ	–40	125	

6.4 Thermal Information

THERMAL METRIC[1] [2]		TL77xxB		UNIT
		D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	109.2	51.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56	40.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.9	28.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.4	17.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	49.4	28.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

(2) Maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} – T_A) / R_{\theta JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

6.5 Electrical Characteristics: TL77xxBC, TL77xxBI, and TL7705BQ

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage, RESET		I_{OH} = –16 mA	V_{CC} – 1.5			V
V_{OL}	Low-level output voltage, $\overline{\text{RESET}}$		I_{OL} = 16 mA			0.4	V
V_{REF}	Reference voltage, REF		I_{ref} = –500 µA, T_A = 25°C	2.48	2.53	2.58	V
$V_{IT–}$	Negative-going input threshold voltage at SENSE input	TL7702B	T_A = 25°C	2.505	2.53	2.555	V
		TL7705B		4.5	4.55	4.6	
		TL7733B		3.03	3.08	3.13	
		TL7702B	T_A = full range(2)	2.48	2.53	2.58	
		TL7705B		4.45	4.55	4.65	
		TL7733B		3	3.08	3.16	
V_{HYS}	Hysteresis, SENSE ($V_{IT+} – V_{IT–}$)	TL7702B	V_{CC} = 3.6 V to 18 V, T_A = 25°C		10		mV
		TL7705B			30		
		TL7733B			10		
V_{RES}	Power-up reset voltage(3)		I_{OL} at $\overline{\text{RESET}}$ = 2 mA, T_A = 25°C			1	V
I_I	Input current	$\overline{\text{RESIN}}$	V_I = 0.4 V to V_{CC}			–10	µA
		SENSE, TL7702B	V_I = V_{REF} to 18 V		–0.1	–2	
I_{OH}	High-level output current, $\overline{\text{RESET}}$		V_O = 18 V, see 図 7-1			50	µA
I_{OL}	Low-level output current, RESET		V_O = 0 V, see 図 7-1			–50	µA
I_{CC}	Supply current		V_{SENSE} = 15 V, $\overline{\text{RESIN}}$ ≥ 2 V		1.8	3	mA
			V_{CC} = 18 V, T_A = full range(2)			3.5	

(1) All electrical characteristics are measured with 0.1-µF capacitors connected at REF, CT, and VCC to GND.
(2) Full range is 0°C to 70°C for the C-suffix devices, –40°C to 85°C for the I-suffix devices, and –40°C to 125°C for the Q-suffix device.
(3) This is the lowest voltage at which $\overline{\text{RESET}}$ becomes active.

6.6 Switching Characteristics: TL77xxBC, TL77xxBI, and TL7705BQ

V_{CC} = 5 V, C_T open, T_A = 25°C, over operating free-air temperature range (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time from low-level to high-level output	$\overline{\text{RESIN}}$	RESET	See , 図 6-1 図 6-2, 図 7-1		270	500	ns
t_{PHL}	Propagation delay time from high-level to low-level output	$\overline{\text{RESIN}}$	$\overline{\text{RESET}}$	See 図 6-1, 図 6-2, 図 7-2		270	500	ns
t_w	Effective pulse duration	$\overline{\text{RESIN}}$		See 図 7-3,図 7-4		150		ns
		SENSE				100		
t_r	Rise time		RESET	See 図 6-1, 図 7-1, 図 7-2			75	ns
			$\overline{\text{RESET}}$			75	150	
t_f	Fall time		RESET	See 図 6-1, 図 7-1, 図 7-2		150	200	ns
			$\overline{\text{RESET}}$				50	

6.7 Timing Diagrams

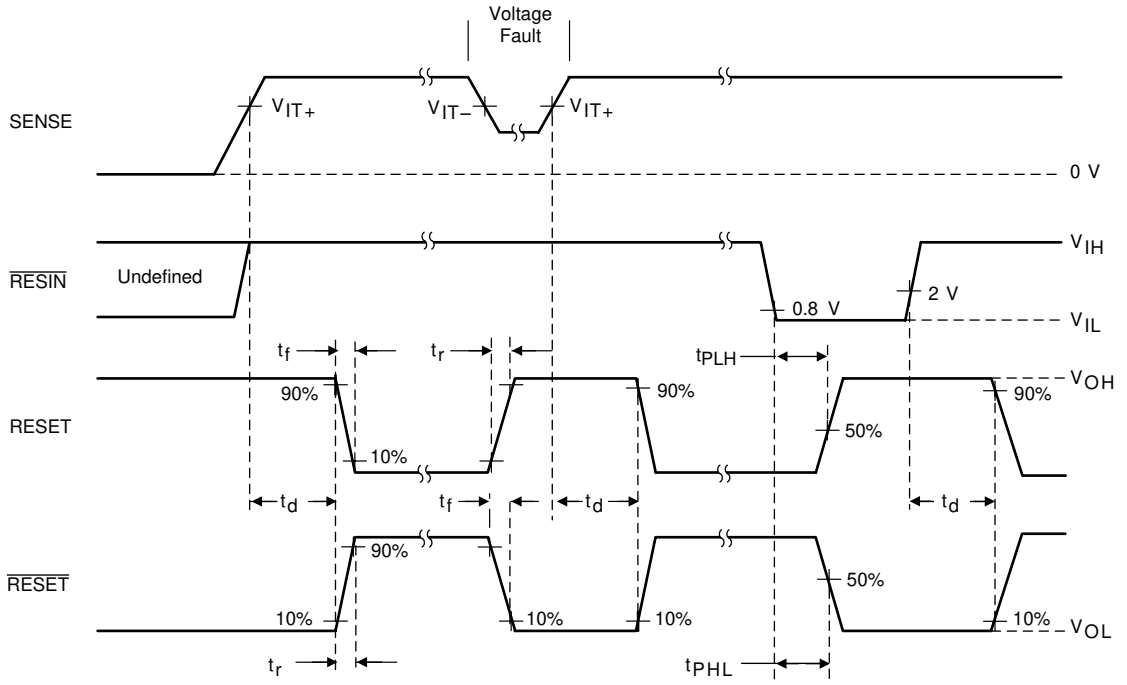


図 6-1. TL7702B, TL7705B, and TL7733B Timing Diagram

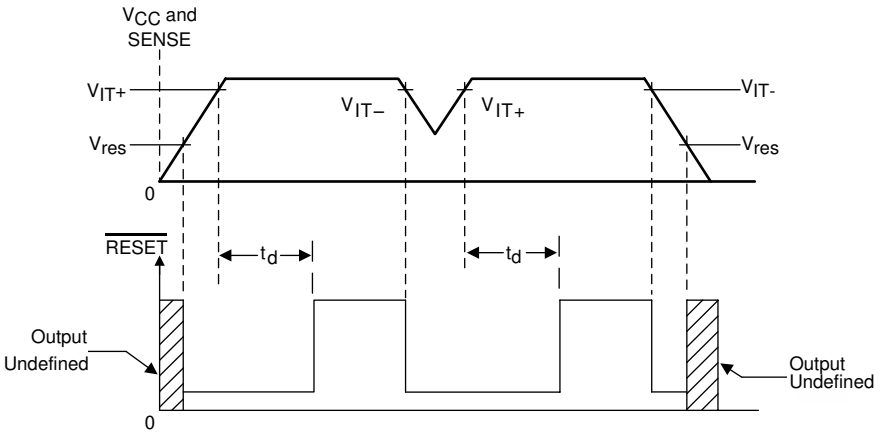


図 6-2. V_{IT} and V_{RES} Timing Diagram

6.8 Typical Characteristics

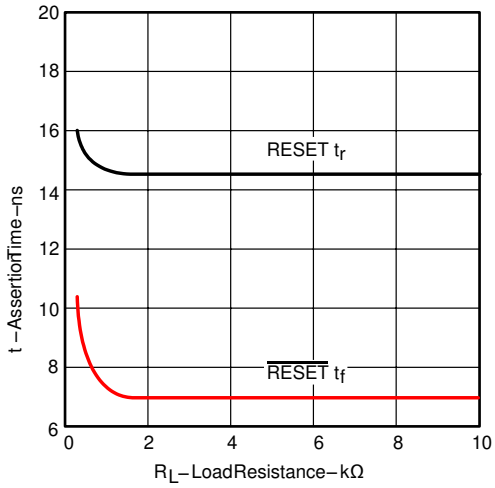


図 6-3. Assertion Time vs Load Resistance

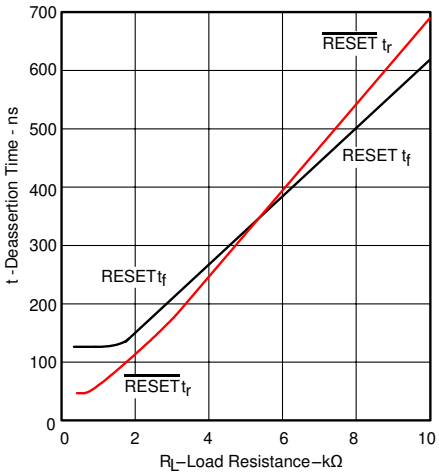


図 6-4. Deassertion Time vs Load Resistance

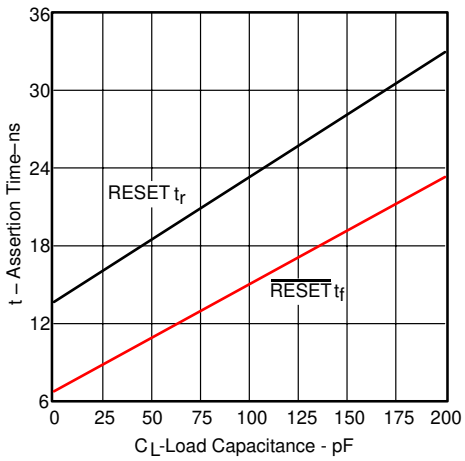


図 6-5. Assertion Time vs Load Capacitance

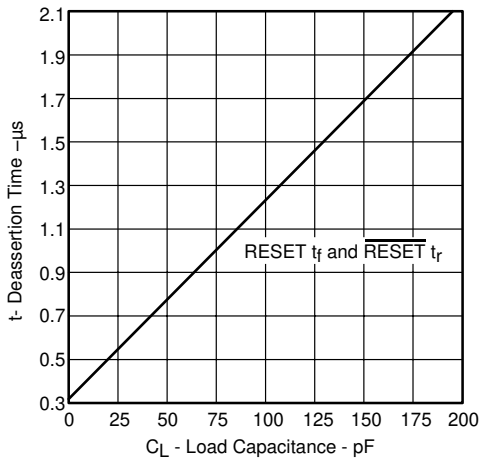
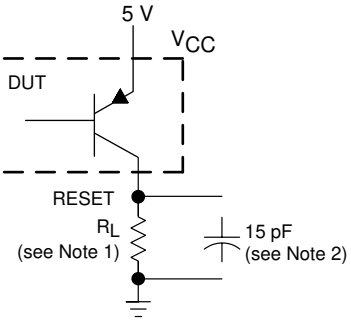


図 6-6. Deassertion Time vs Load Capacitance

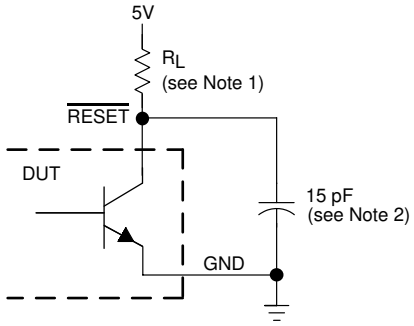
7 Parameter Measurement Information



RESET OUTPUT CONFIGURATION

A. For I_{OL} and I_{OH}, R_L = 10 kΩ. For all switching characteristics, R_L = 511 Ω.
B. This figure includes jig and probe capacitance.

図 7-1. RESET Output Configuration



$\overline{\text{RESET}}$ OUTPUT CONFIGURATION

A. For I_{OL} and I_{OH}, R_L = 10 kΩ. For all switching characteristics, R_L = 511 Ω.
B. This figure includes jig and probe capacitance.

図 7-2. $\overline{\text{RESET}}$ Output Configuration

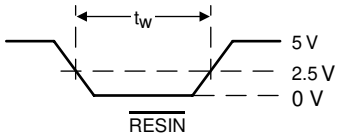


図 7-3. Input Pulse Definition RESIN

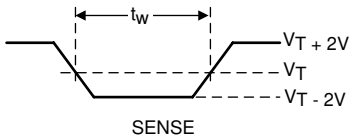


図 7-4. Input Pulse Definition SENSE

8 Detailed Description

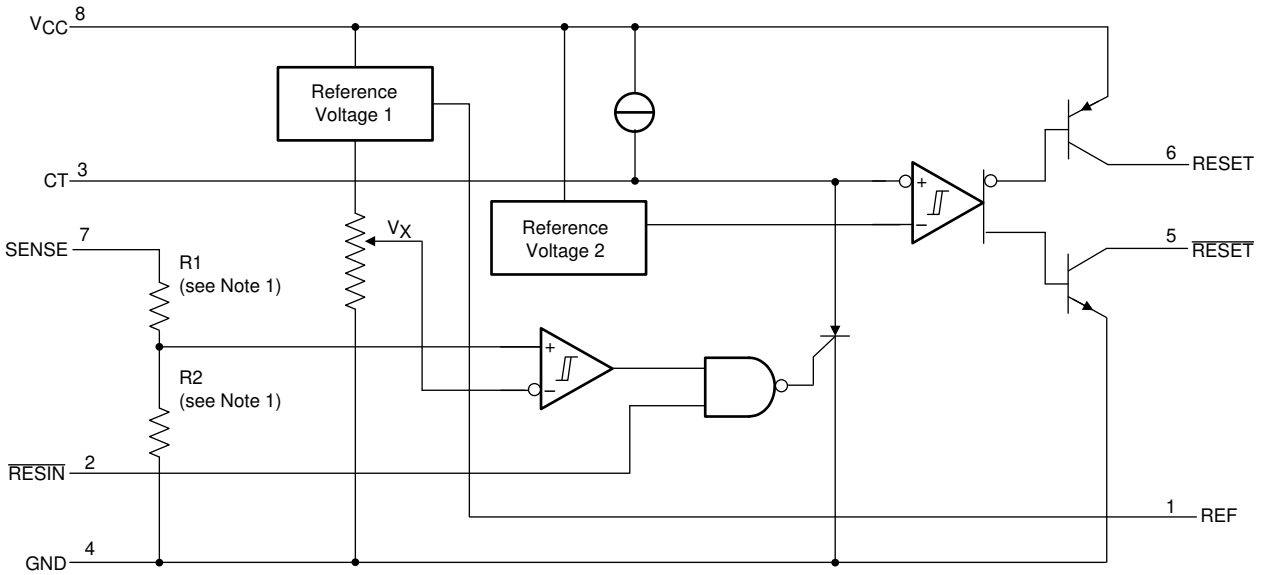
8.1 Overview

The TL7702B, TL7705B, and TL7733B are integrated-circuit supply-voltage supervisors designed for use as reset controllers in microcomputer and microprocessor systems. The supply-voltage supervisor monitors the supply for undervoltage conditions at the SENSE input. During power up, the $\overline{\text{RESET}}$ output becomes active (low) when V_{CC} attains a value approaching 1 V. As V_{CC} approaches 3 V (assuming that SENSE is above V_{T+}), the delay-timer function activates a time delay, after which outputs $\overline{\text{RESET}}$ and RESET go inactive (high and low, respectively). When an undervoltage condition occurs during normal operation, outputs $\overline{\text{RESET}}$ and RESET go active. To ensure that a complete reset occurs, the reset outputs remain active for a time delay after the voltage at the SENSE input exceeds the positive-going threshold value. The time delay is determined by the value of the external capacitor C_T : $t_d \approx 2.6 \times 10^4 \times C_T$, where C_T is in farads (F) and t_d is in seconds (s).

An external capacitor (typically 0.1 μF) must be connected to REF to reduce the influence of fast transients in the supply voltage.

8.2 Functional Block Diagram

The functional block diagram is shown for illustrative purposes only; the actual circuit includes a trimming network to adjust the reference voltage and sense-comparator trip point.



8.3 Feature Description

8.3.1 Wide Supply-Voltage Range

The TL77xxB family operates using a wide supply voltage from 3.6 V to 18 V.

8.3.2 Adjustable Pulse Duration

The CT pin enables the ability to set a user-defined time delay in order to ensure that the fault condition is recognized. The external capacitor charges based on an internal current source until the voltage at the CT pin exceeds that of the internal reference voltage.

The time delay is determined by the value of the external capacitor C_T : $t_d \approx 2.6 \times 10^4 \times C_T$, where C_T is in farads (F) and t_d is in seconds (s).

The current source to charge the timing capacitor varies ±15%. Reference Voltage 2 is approximately 1.8 V and varies approximately ±5%. Once the timing capacitor charges, it discharges to about 0.6 V, not completely to 0 V.

8.4 Device Functional Modes

図 8-1 displays how the RESET and $\overline{\text{RESET}}$ output pins respond to the change in the the SENSE and $\overline{\text{RESIN}}$ input pins. When the $\overline{\text{RESIN}}$ pin is high, the RESET outputs are able to respond to a drop in the supply voltage at the SENSE pin. When the RESIN pin is low, the RESET and $\overline{\text{RESET}}$ pins are set HIGH and LOW respectively.

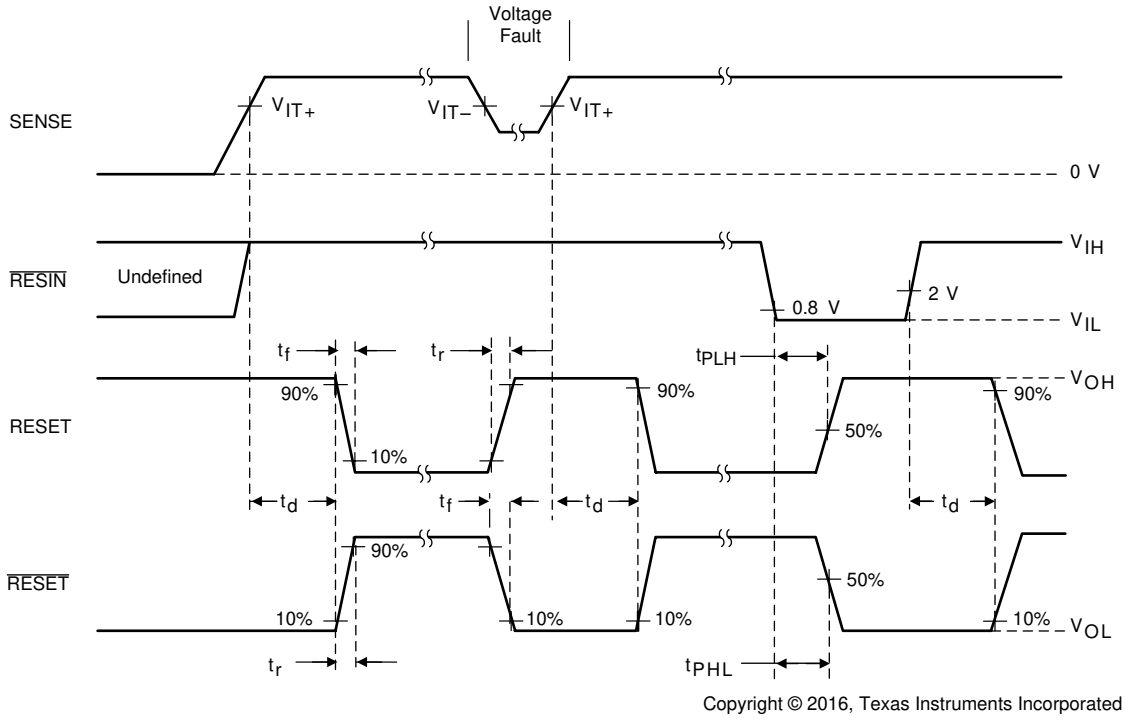


図 8-1. TL77xxB RESET and $\overline{\text{RESET}}$ Response and Timing

9 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。また、お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

図 9-1 shows an application where the TL7705B device is being used to sense the voltage supply for a microcontroller that is supplied with 5 V. If the voltage supply drops below the threshold voltage, the $\overline{\text{RESET}}$ pin is pulled LOW, signaling the microcontroller to reset.

9.2 Typical Application

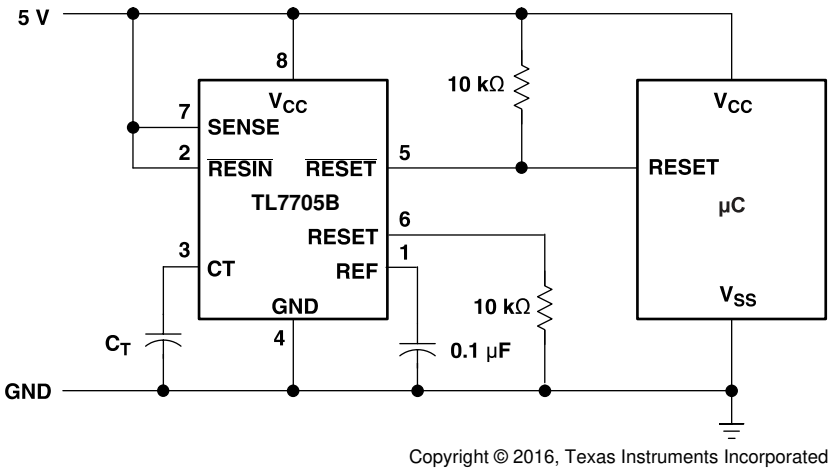


図 9-1. Reset Controller Schematic for a Microprocessor

9.2.1 Design Requirements

The external components required include the decoupling capacitor for the REF pin and the timing capacitor for the CT pin. Additionally, because the $\overline{\text{RESET}}$ output is open collector, a pullup resistor is required to ensure the correct HIGH level for the microcontroller RESET pin.

9.2.2 Detailed Design Procedure

TI recommends pullup and pulldown resistors of 10 kΩ.

To achieve a 2.6 ms time delay, use C_T = 0.1 μF.

Both outputs of the TL770xB must be terminated with similar value resistors, even when only one is being used. This prevents unwanted plateauing in either output waveform during switching, which may be interpreted as an undefined state or delay system reset

9.2.3 Application Curve

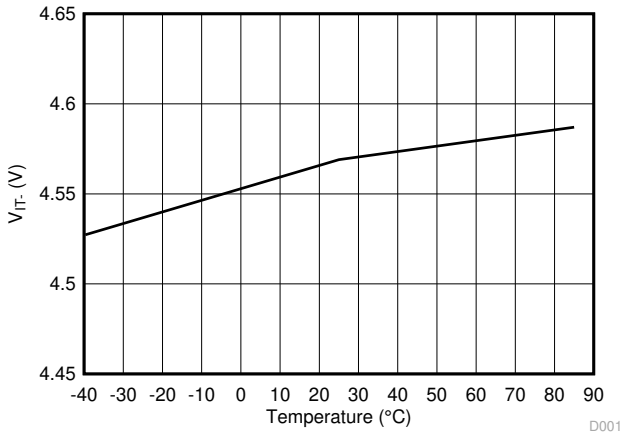


図 9-2. TL7705B Threshold Voltage vs Temperature

10 Power Supply Recommendations

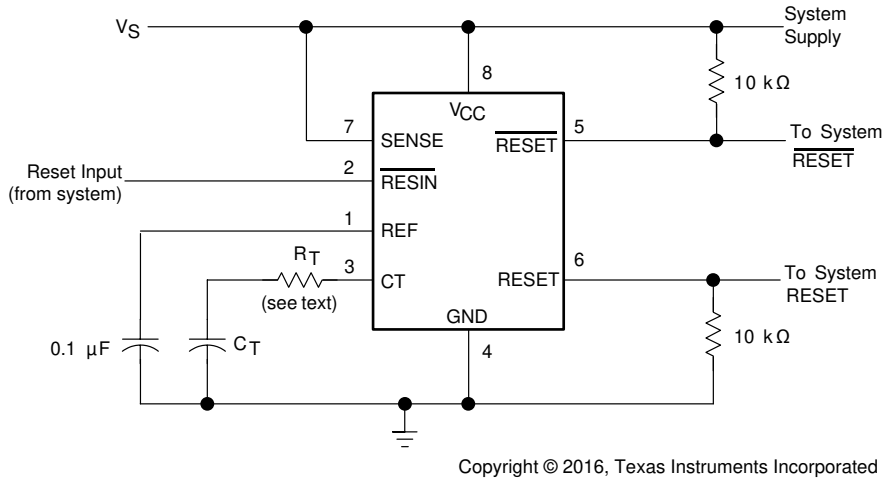


図 10-1. System Reset Controller With Undervoltage Sensing

When the TL770xB SENSE terminal is used to monitor V_{CC}, TI recommends a current-limiting resistor in series with C_T. During normal operation, the timing capacitor is charged by the onboard current source to approximately V_{CC} or an internal voltage clamp (≈7.1-V Zener), whichever is less. When the circuit then is subjected to an undervoltage condition during which V_{CC} is rapidly slewed down, the voltage on CT exceeds that on V_{CC}. This forward biases a secondary path internally, which falsely activates the outputs. A fault is indicated when V_{CC} drops below $V_{(CT)}$, not when V_{SENSE} falls below $V_{T–}$.

Adding the external resistor, R_T, prevents false triggering. Its value is calculated as follows:

$$(V_{(CT)} – V_{T-}) / R_T \quad (1)$$

where

- $V_{(CT)} = V_{CC}$ or 7.1 V, whichever is less
- $V_{T–} = 4.55$ V (nom)
- R_T = value of series resistor required

For $V_{CC} = 5$ V

$$(5 – 4.55) / R_T < 1 \text{ mA} \quad (2)$$

Therefore,

$$R_T > 450\ \Omega \quad (3)$$

Using a 20%-tolerance resistor, R_T should be greater than 560 Ω.

Adding this series resistor changes the duration of the reset pulse by no more than 10%. R_T extends the discharge of C_T, but also skews the $V_{(CT)}$ threshold. These effects tend to cancel one another. The precise percentage change can be derived theoretically, but the equation is complicated by this interaction and is dependent upon the duration of the supply-voltage fault condition.

Both outputs of the TL770xB must be terminated with similar value resistors, even when only one is being used. This prevents unwanted plateauing in either output waveform during switching, which may be interpreted as an undefined state or delay system reset.

11 Layout

11.1 Layout Guidelines

図 11-1 shows an example layout for the TL7705B device. As the $\overline{\text{RESET}}$ and RESET pins are open collector outputs, place pullup and pulldown resistors on the $\overline{\text{RESET}}$ and RESET pins respectively. A capacitor must be placed on the REF pin to stabilize the reference. This can help to prevent false triggering if noise couples into the reference.

11.2 Layout Example

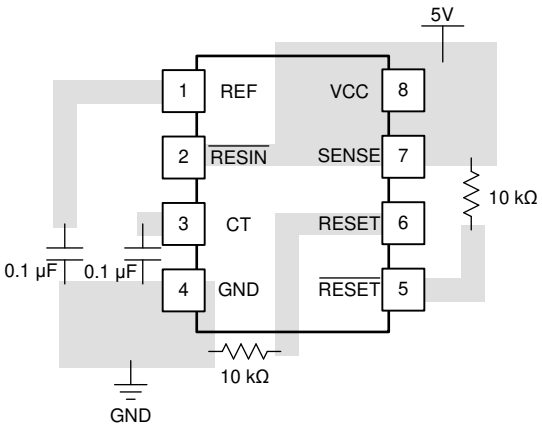


図 11-1. TL7705B Layout Example

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 12-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TL7702B	Click here	Click here	Click here	Click here	Click here
TL7705B	Click here	Click here	Click here	Click here	Click here
TL7733B	Click here	Click here	Click here	Click here	Click here

12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。*「更新の通知を受け取る」をクリック*して登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

12.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

12.6 用語集

TI 用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL7702BCD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	7702BC
TL7702BCD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	7702BC
TL7702BCDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	7702BC
TL7702BCDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	7702BC
TL7702BCP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL7702BCP
TL7702BCP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL7702BCP
TL7702BID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	7702BI
TL7702BID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	7702BI
TL7702BIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	7702BI
TL7702BIDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	7702BI
TL7702BIP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL7702BIP
TL7702BIP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL7702BIP
TL7705BCD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	7705BC
TL7705BCD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	7705BC
TL7705BCDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	7705BC
TL7705BCDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	7705BC
TL7705BCP	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL7705BCP
TL7705BCP.A	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL7705BCP
TL7705BID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	7705BI
TL7705BID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	7705BI
TL7705BIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	7705BI
TL7705BIDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	7705BI
TL7705BIP	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL7705BIP
TL7705BIP.A	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL7705BIP
TL7705BQD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7705BQ
TL7705BQD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7705BQ
TL7705BQDG4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7705BQ
TL7705BQDG4.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7705BQ
TL7705BQDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7705BQ

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL7705BQDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7705BQ
TL7705BQDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7705BQ
TL7705BQDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7705BQ
TL7733BCD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	7733BC
TL7733BCD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	7733BC
TL7733BCDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	7733BC
TL7733BCDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	7733BC
TL7733BCP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL7733BCP
TL7733BCP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL7733BCP
TL7733BID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	7733BI
TL7733BID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	7733BI
TL7733BIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	7733BI
TL7733BIDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	7733BI

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

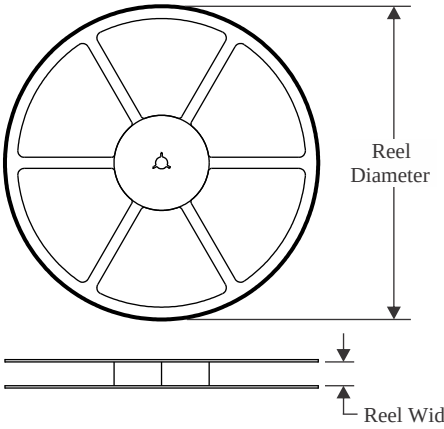
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

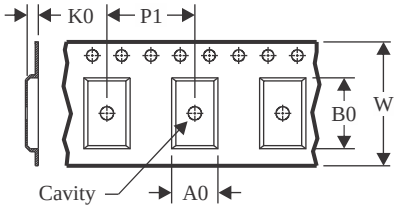
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

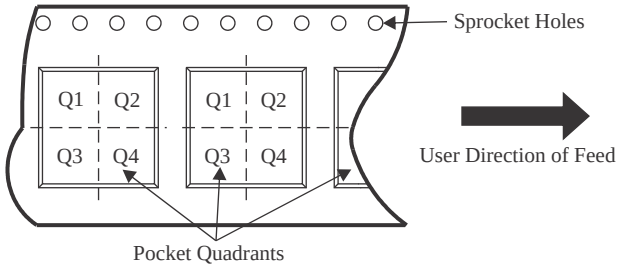


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

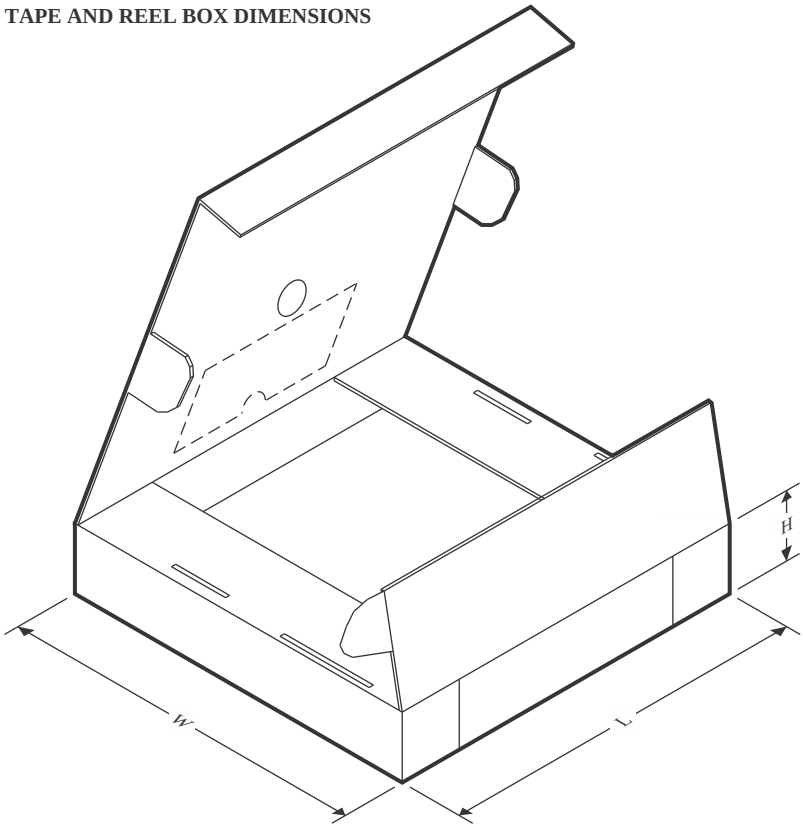
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL7702BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7702BIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7705BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7705BIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7705BQDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7705BQDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7733BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7733BIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

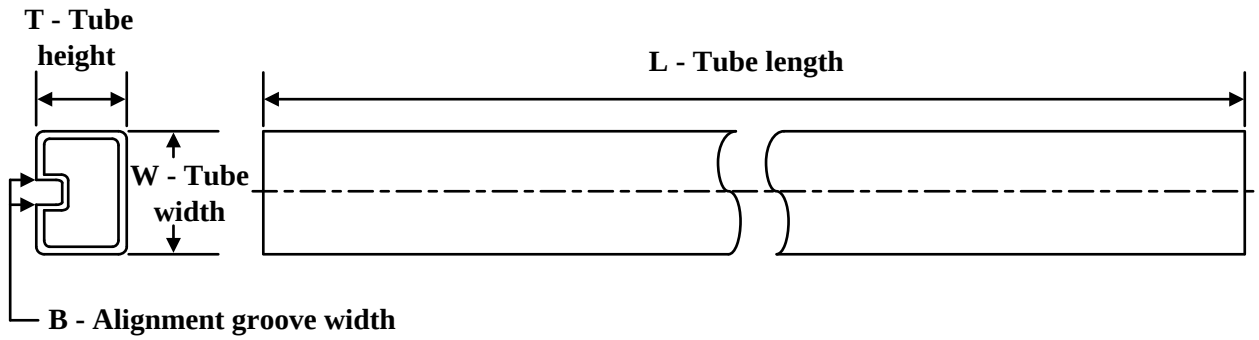
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

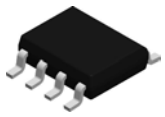
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL7702BCDR	SOIC	D	8	2500	353.0	353.0	32.0
TL7702BIDR	SOIC	D	8	2500	353.0	353.0	32.0
TL7705BCDR	SOIC	D	8	2500	353.0	353.0	32.0
TL7705BIDR	SOIC	D	8	2500	353.0	353.0	32.0
TL7705BQDR	SOIC	D	8	2500	350.0	350.0	43.0
TL7705BQDRG4	SOIC	D	8	2500	350.0	350.0	43.0
TL7733BCDR	SOIC	D	8	2500	353.0	353.0	32.0
TL7733BIDR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL7702BCD	D	SOIC	8	75	507	8	3940	4.32
TL7702BCD.A	D	SOIC	8	75	507	8	3940	4.32
TL7702BCP	P	PDIP	8	50	506	13.97	11230	4.32
TL7702BCP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL7702BID	D	SOIC	8	75	507	8	3940	4.32
TL7702BID.A	D	SOIC	8	75	507	8	3940	4.32
TL7702BIP	P	PDIP	8	50	506	13.97	11230	4.32
TL7702BIP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL7705BCD	D	SOIC	8	75	507	8	3940	4.32
TL7705BCD.A	D	SOIC	8	75	507	8	3940	4.32
TL7705BCP	P	PDIP	8	50	506	13.97	11230	4.32
TL7705BCP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL7705BID	D	SOIC	8	75	507	8	3940	4.32
TL7705BID.A	D	SOIC	8	75	507	8	3940	4.32
TL7705BIP	P	PDIP	8	50	506	13.97	11230	4.32
TL7705BIP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL7705BQD	D	SOIC	8	75	505.46	6.76	3810	4
TL7705BQD.A	D	SOIC	8	75	505.46	6.76	3810	4
TL7705BQDG4	D	SOIC	8	75	505.46	6.76	3810	4
TL7705BQDG4.A	D	SOIC	8	75	505.46	6.76	3810	4
TL7733BCD	D	SOIC	8	75	507	8	3940	4.32
TL7733BCD.A	D	SOIC	8	75	507	8	3940	4.32
TL7733BCP	P	PDIP	8	50	506	13.97	11230	4.32
TL7733BCP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL7733BID	D	SOIC	8	75	507	8	3940	4.32
TL7733BID.A	D	SOIC	8	75	507	8	3940	4.32

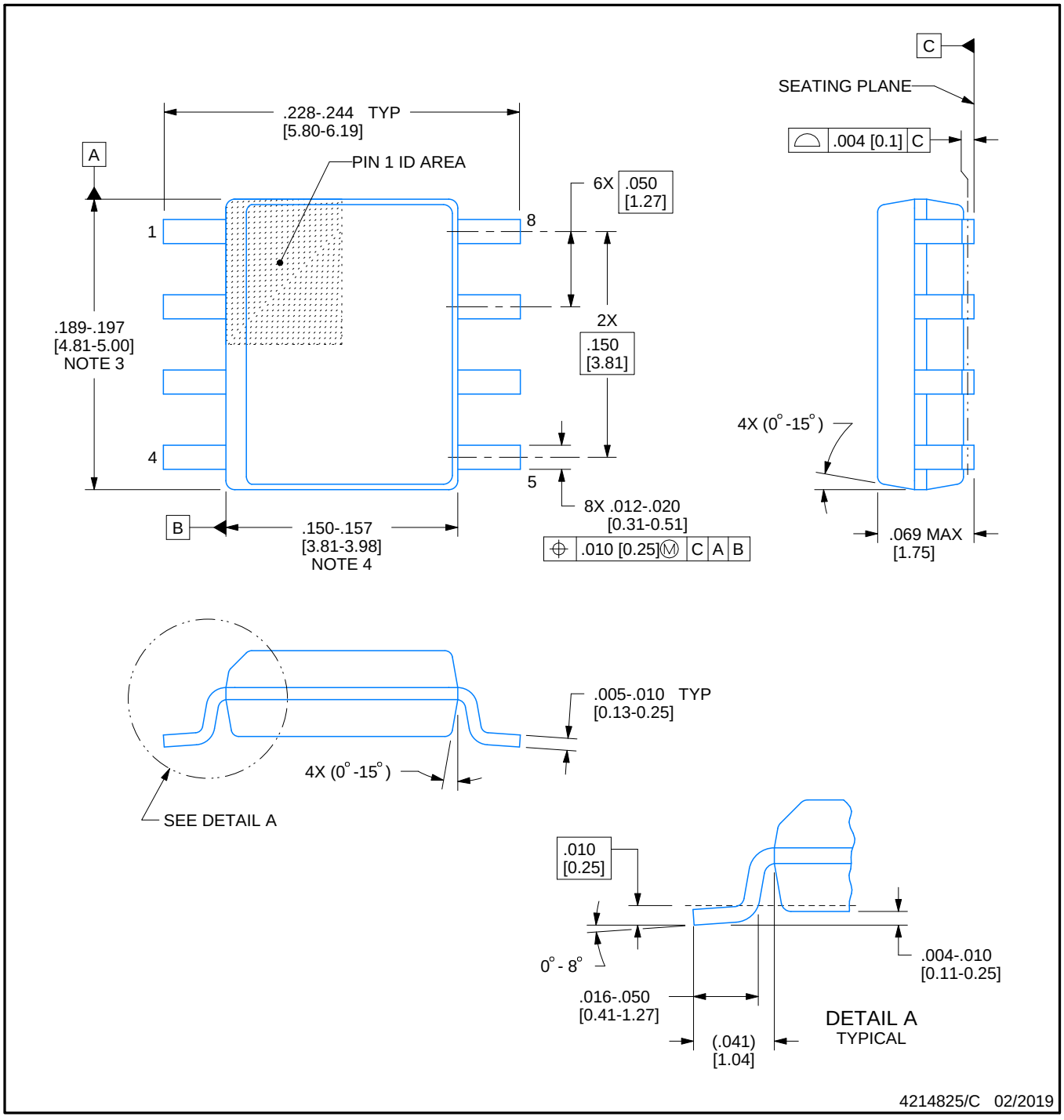


PACKAGE OUTLINE

D0008A

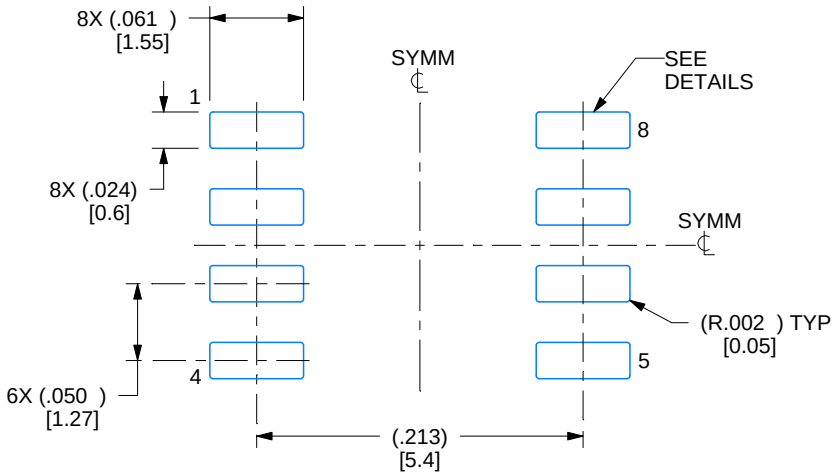
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

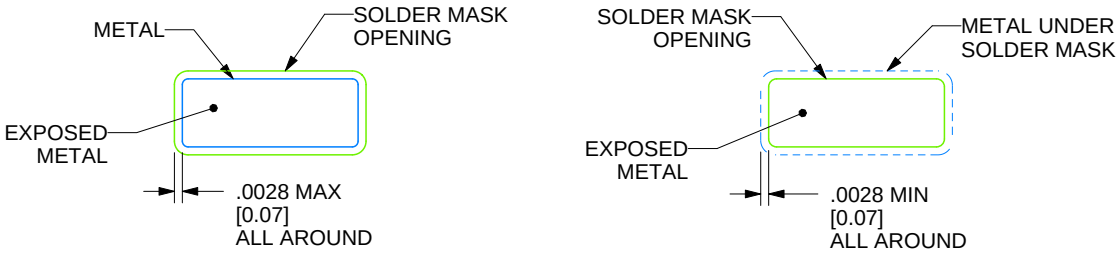


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

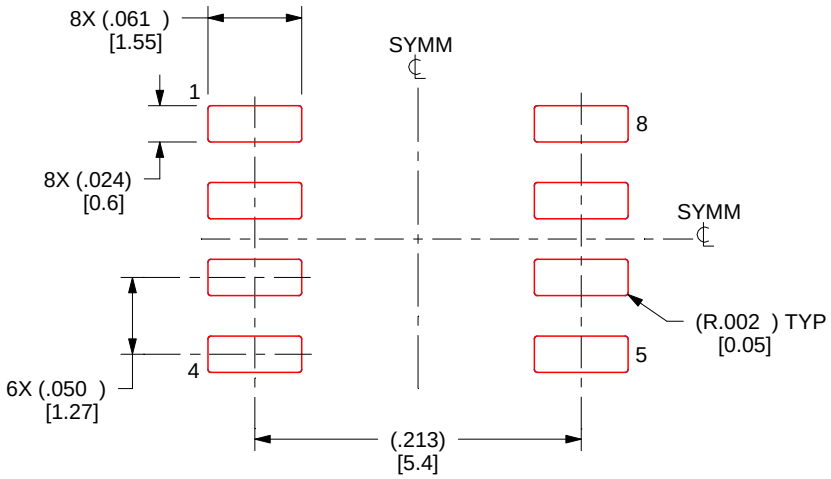
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



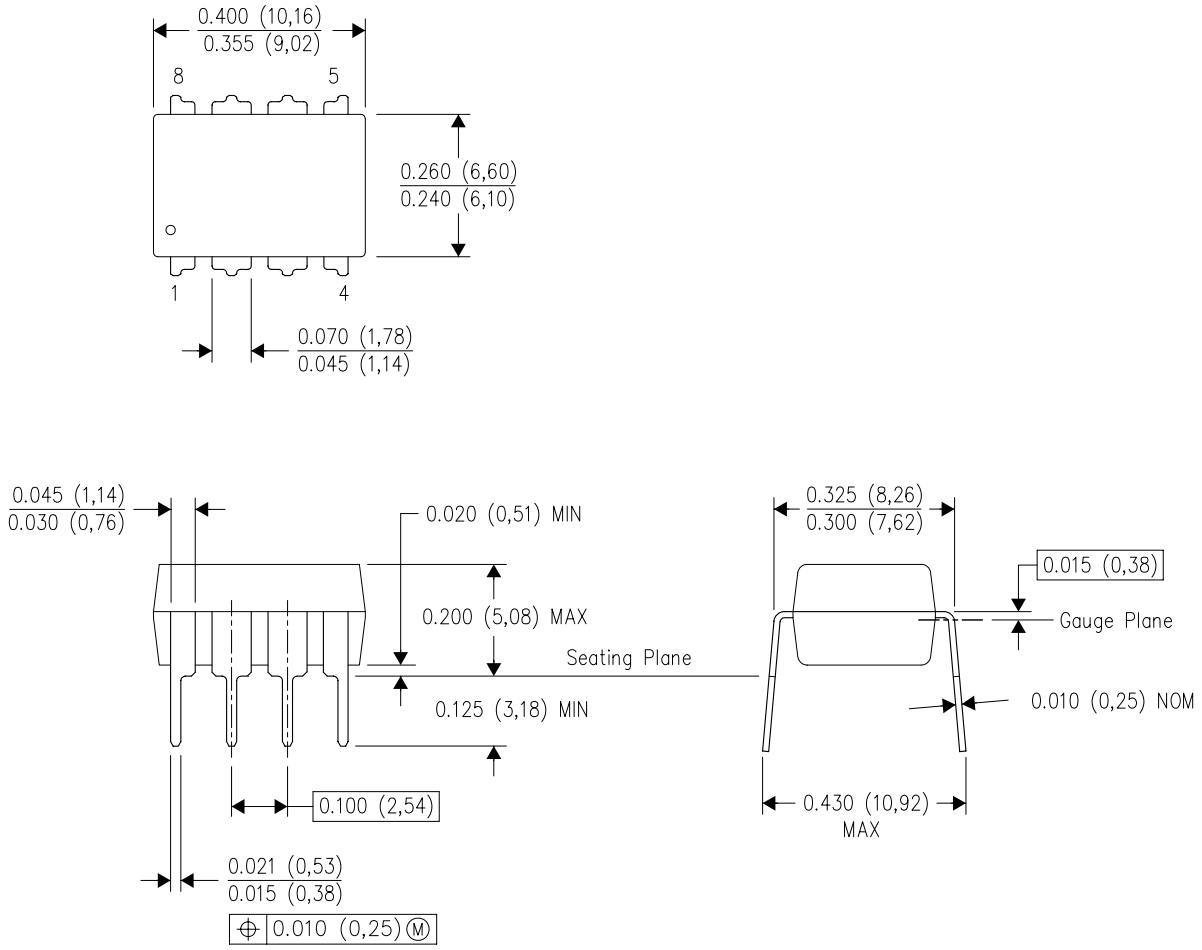
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

重要なお知らせと免責事項

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最終更新日：2025 年 10 月