

## TLC227x-Q1 先進のレール・ツー・レール LinCMOS™ オペアンプ

### 1 特長

- 車載アプリケーション向けに AEC-Q100 認定済み
  - 温度グレード 1: -40°C ~ 125°C, T<sub>A</sub>
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能 (TLC2272-Q1)
  - 機能安全システムの設計に役立つ資料を利用可能 (TLC2272A-Q1)
- 出力シングに両方の電源レールを含む
- 低いノイズ: f = 1kHz 時に 9nV/√Hz (標準値)
- 低い入力バイアス電流: 1pA (標準値)
- 単一電源と分割電源での動作を完全に規定
- 同相入力電圧範囲に負のレールを含む
- 高ゲイン帯域幅: 2.2MHz (標準値)
- 高いスルーレート: 3.6V/μs (標準値)
- 低い入力オフセット電圧: 950μV 以下 (T<sub>A</sub> = 25°C)
- マクロモデル内蔵

### 2 アプリケーション

- ボディ・コントロール・モジュール
- バッテリー・マネージメント・システム
- カー・オーディオ
- DC/DC コンバータ
- 電動パワー・ステアリング
- エンジン制御ユニット
- ガソリン・エンジン
- インストルメント・クラス
- インバータおよびモータ制御
- オンボード・チャージャ
- テレマティクス制御ユニット
- トランスミッション制御
- 白物家電 (冷蔵庫、洗濯機)

### 3 概要

TLC227x-Q1 はデュアルおよびクワッド LinCMOS™ オペアンプです。どちらのデバイスも、単一および分割電源アプリケーションで広いダイナミック・レンジが得られるレール・ツー・レールの出力特性を示します。TLC227x-Q1 ファミリーは 2MHz の帯域幅と 3V/μs のスルーレートを実現しており、高速アプリケーションに適しています。これらのデバイスは既存の CMOS オペアンプと同等の AC 性能を備えながら、ノイズ、入力オフセット電圧、消費電力の点で CMOS オペアンプより優れています。TLC227x-Q1 のノイズ電圧は 9nV/√Hz で、競合ソリューションの半分です。

TLC227x-Q1 は入力インピーダンスが高く、ノイズが低いいため、圧電性トランスデューサなど高インピーダンスのソース用の小信号コンディショニングに最適です。さらに、単一

または分割電源でレール・ツー・レール出力が可能なため、このファミリーは A/D コンバータ (ADC) と接続するための優れた選択肢です。

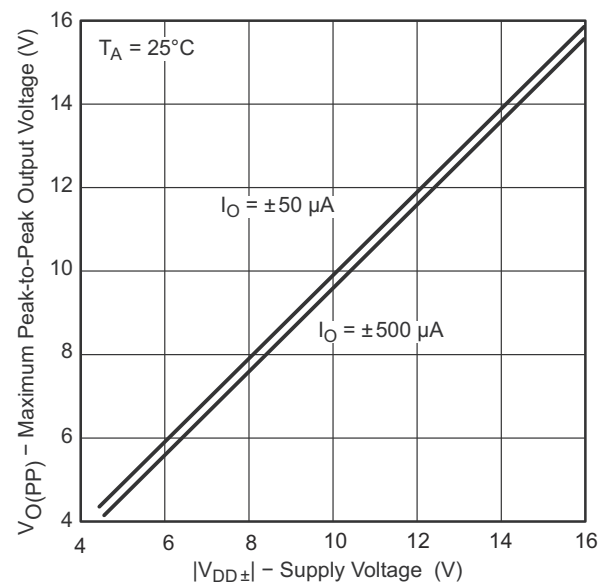
高精度のアプリケーション向けには、最大入力オフセット電圧 950μV の TLC227xA-Q1 ファミリーが利用可能です。このファミリーは 5V および ±5V で完全に動作が規定されています。

これらのデバイスは広い出力ダイナミック・レンジ、小さいノイズ電圧、小さい入力オフセット電圧を実現しています。これらの拡張機能セットから、TLC227x-Q1 は広範なアプリケーションで使用可能です。より高い出力駆動能力と広い入力電圧範囲を必要とするアプリケーションについては、TLV2432-Q1 と TLV2442-Q1 を参照してください。TLC227x-Q1 ファミリーのすべてのパラメータのおかげで、これらのデバイスはほとんどの車載アプリケーションに適用可能です。

#### パッケージ情報

部品番号	パッケージ <sup>(1)</sup>	本体サイズ (公称)
TLC2272-Q1, TLC2272A-Q1	SOIC (8)	4.90mm × 3.91mm
	TSSOP (8)	3.00mm × 4.40mm
TLC2274-Q1, TLC2274A-Q1	SOIC (14)	8.65mm × 3.91mm
	TSSOP (14)	5.00mm × 4.40mm

- (1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



最大ピーク・ツー・ピーク出力電圧と電源電圧との関係



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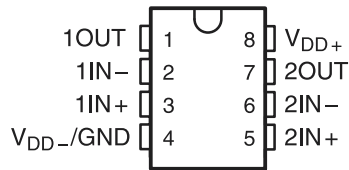
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## 4 Revision History

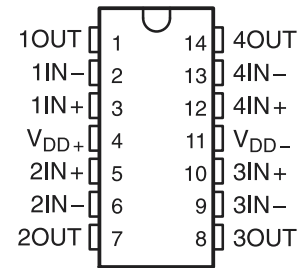
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

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• 「ピン構成および機能」セクション、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加.....	1
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## 5 Pin Configuration and Functions



**图 5-1. TLC2272-Q1 and TLC2272A-Q1:  
D (8-Pin SOIC) or PW (8-Pin TSSOP)  
Packages, Top View**



**图 5-2. TLC2274-Q1 and TLC2274A-Q1:  
D (14-Pin SOIC) or PW (14-Pin TSSOP)  
Packages, Top View**

**表 5-1. Pin Functions**

NAME	PIN NO.		TYPE	DESCRIPTION
	TLC2272-Q1, TLC2272A-Q1	TLC2274-Q1, TLC2274A-Q1		
1IN+	3	3	Input	Noninverting input, channel 1
1IN-	2	2	Input	Inverting input, channel 1
1OUT	1	1	Output	Output, channel 1
2IN+	5	5	Input	Noninverting input, channel 2
2IN-	6	6	Input	Inverting input, channel 2
2OUT	7	7	Output	Output, channel 2
3IN+	—	10	Input	Noninverting input, channel 3
3IN-	—	9	Input	Inverting input, channel 3
3OUT	—	8	Output	Output, channel 3
4IN+	—	12	Input	Noninverting input, channel 4
4IN-	—	13	Input	Inverting input, channel 4
4OUT	—	14	Output	Output, channel 4
V <sub>DD+</sub>	8	4	Input	Positive (highest) supply
V <sub>DD-</sub>	4	11	Input	Negative (lowest) supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

	MIN	MAX	UNIT
Supply voltage, $V_{DD+}$ <sup>(2)</sup>		8	V
$V_{DD-}$ <sup>(2)</sup>	-8		V
Differential input voltage, $V_{ID}$ <sup>(3)</sup>		±16	V
Input voltage, $V_I$ (any input) <sup>(2)</sup>	$V_{DD-} - 0.3$	$V_{DD+}$	V
Input current, $I_I$ (any input)		±5	mA
Output current, $I_O$		±50	mA
Total current into $V_{DD+}$		±50	mA
Total current out of $V_{DD-}$		±50	mA
Duration of short-circuit current at (or below) 25°C <sup>(4)</sup>	Unlimited		
Operating free-air temperature range, $T_A$	-40	125	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or PW package		260
Storage temperature, $T_{stg}$	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under [セクション 6.3](#). Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to the midpoint between  $V_{DD+}$  and  $V_{DD-}$ .
- (3) Differential voltages are at  $IN+$  with respect to  $IN-$ . Excessive current will flow if input is brought below  $V_{DD-} - 0.3$  V.
- (4) The output can be shorted to either supply. Temperature or supply voltages must be limited so that the maximum dissipation rating is not exceeded.

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup> HBM ESD classification level 2	±2000
		Charged-device model (CDM), per AEC Q100-011 CDM ESD classification level C6	±1000

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{DD±}$	Supply voltage	±2.2	±8	V
$V_I$	Input voltage	$V_{DD-}$	$V_{DD+} - 1.5$	V
$V_{IC}$	Common-mode input voltage	$V_{DD-}$	$V_{DD+} - 1.5$	V
$T_A$	Operating free-air temperature	-40	125	°C

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TLC2272-Q1, TLC2272A-Q1		TLC2274-Q1, TLC2274A-Q1		UNIT
		D (SOIC)	PW (TSSOP)	D (SOIC)	PW (TSSOP)	
		8 PINS	8 PINS	14 PINS	14 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	115.6	175.8	83.8	111.6	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	61.8	58.8	43.2	41.2	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	55.9	104.3	38.4	54.7	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	14.3	5.9	9.4	3.9	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	55.4	102.3	38.1	53.9	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	—	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

## 6.5 Electrical Characteristics: V<sub>DD</sub> = 5 V (TLC2272-Q1 and TLC2272A-Q1)

at specified free-air temperature, V<sub>DD</sub> = 5 V; T<sub>A</sub> = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V <sub>IO</sub>	Input offset voltage	V <sub>IC</sub> = 0 V, V <sub>DD±</sub> = ±2.5 V, V <sub>O</sub> = 0 V, R <sub>S</sub> = 50 Ω	TLC2272-Q1	T <sub>A</sub> = 25°C	300	2500	μV
			TLC2272A-Q1		300	950	
			TLC2272-Q1	Full Range <sup>(1)</sup>		3000	
			TLC2272A-Q1		1500		
α <sub>VIO</sub>	Temperature coefficient of input offset voltage	V <sub>IC</sub> = 0 V, V <sub>DD±</sub> = ±2.5 V, V <sub>O</sub> = 0 V, R <sub>S</sub> = 50 Ω			2		μV/°C
	Input offset voltage long-term drift <sup>(2)</sup>	V <sub>IC</sub> = 0 V, V <sub>DD±</sub> = ±2.5 V, V <sub>O</sub> = 0 V, R <sub>S</sub> = 50 Ω			0.002		μV/mo
I <sub>IO</sub>	Input offset current	V <sub>IC</sub> = 0 V, V <sub>DD±</sub> = ±2.5 V, V <sub>O</sub> = 0 V, R <sub>S</sub> = 50 Ω	T <sub>A</sub> = 25°C	0.5	60	pA	
			Full Range <sup>(1)</sup>		800		
I <sub>IB</sub>	Input bias current	V <sub>IC</sub> = 0 V, V <sub>DD±</sub> = ±2.5 V, V <sub>O</sub> = 0 V, R <sub>S</sub> = 50 Ω	T <sub>A</sub> = 25°C	1	60	pA	
			Full Range <sup>(1)</sup>		800		
V <sub>ICR</sub>	Common-mode input voltage	R <sub>S</sub> = 50 Ω;  V <sub>IO</sub>   ≤ 5 mV	T <sub>A</sub> = 25°C	-0.3	2.5	4	V
			Full Range <sup>(1)</sup>	0	2.5	3.5	
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -200 μA	I <sub>OH</sub> = -20 μA		4.99		V
			T <sub>A</sub> = 25°C	4.85	4.93		
			Full Range <sup>(1)</sup>	4.85			
			T <sub>A</sub> = 25°C	4.25	4.65		
V <sub>OL</sub>	Low-level output voltage	V <sub>IC</sub> = 2.5 V	I <sub>OL</sub> = 50 μA		0.01		V
			I <sub>OL</sub> = 500 μA	T <sub>A</sub> = 25°C	0.09	0.15	
				Full Range <sup>(1)</sup>		0.15	
			I <sub>OL</sub> = 5 mA	T <sub>A</sub> = 25°C	0.9	1.5	
Full Range <sup>(1)</sup>		1.5					
A <sub>VD</sub>	Large-signal differential voltage amplification	V <sub>IC</sub> = 2.5 V, V <sub>O</sub> = 1 V to 4 V	R <sub>L</sub> = 10 kΩ <sup>(3)</sup>	T <sub>A</sub> = 25°C	10	35	V/mV
			R <sub>L</sub> = 1 MΩ <sup>(3)</sup>	Full Range <sup>(1)</sup>	10		
					175		
r <sub>id</sub>	Differential input resistance				10 <sup>12</sup>		Ω
r <sub>i</sub>	Common-mode input resistance				10 <sup>12</sup>		Ω
c <sub>i</sub>	Common-mode input capacitance	f = 10 kHz, P package			8		pF
z <sub>o</sub>	Closed-loop output impedance	f = 1 MHz, A <sub>v</sub> = 10			140		Ω
CMRR	Common-mode rejection ratio	V <sub>IC</sub> = 0 V to 2.7 V, V <sub>O</sub> = 2.5 V, R <sub>S</sub> = 50 Ω	T <sub>A</sub> = 25°C	70	75	dB	
			Full Range <sup>(1)</sup>	70			
k <sub>SVR</sub>	Supply-voltage rejection ratio (ΔV <sub>DD</sub> / ΔV <sub>IO</sub> )	V <sub>DD</sub> = 4.4 V to 16 V, V <sub>IC</sub> = V <sub>DD</sub> / 2, no load	T <sub>A</sub> = 25°C	80	95	dB	
			Full Range <sup>(1)</sup>	80			

## 6.5 Electrical Characteristics: $V_{DD} = 5\text{ V}$ (TLC2272-Q1 and TLC2272A-Q1) (continued)

at specified free-air temperature,  $V_{DD} = 5\text{ V}$ ;  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{DD}$	Supply current	$V_O = 2.5\text{ V}$ , no load	$T_A = 25^\circ\text{C}$		2.2	3	mA
			Full Range <sup>(1)</sup>				
SR	Slew rate at unity gain	$V_O = 0.5\text{ V}$ to $2.5\text{ V}$ , $R_L = 10\text{ k}\Omega$ <sup>(3)</sup> , $C_L = 100\text{ pF}$ <sup>(3)</sup>	$T_A = 25^\circ\text{C}$		2.3	3.6	V/ $\mu\text{s}$
			Full Range <sup>(1)</sup>		1.7		
$V_n$	Equivalent input noise voltage		$f = 10\text{ Hz}$			50	nV/ $\sqrt{\text{Hz}}$
			$f = 1\text{ kHz}$			9	
$V_{NPP}$	Peak-to-peak equivalent input noise voltage		$f = 0.1\text{ Hz}$ to $1\text{ Hz}$			1	$\mu\text{V}$
			$f = 0.1\text{ Hz}$ to $10\text{ Hz}$			1.4	
$I_n$	Equivalent input noise current				0.6	fA/ $\sqrt{\text{Hz}}$	
THD+N	Total harmonic distortion + noise	$V_O = 0.5\text{ V}$ to $2.5\text{ V}$ , $f = 20\text{ kHz}$ , $R_L = 10\text{ k}\Omega$ <sup>(3)</sup>	$A_V = 1$		0.0013%		
			$A_V = 10$		0.004%		
			$A_V = 100$		0.03%		
	Gain-bandwidth product	$f = 10\text{ kHz}$ , $R_L = 10\text{ k}\Omega$ <sup>(3)</sup> , $C_L = 100\text{ pF}$ <sup>(3)</sup>			2.18	MHz	
$B_{OM}$	Maximum output-swing bandwidth	$V_{O(PP)} = 2\text{ V}$ , $A_V = 1$ , $R_L = 10\text{ k}\Omega$ <sup>(3)</sup> , $C_L = 100\text{ pF}$ <sup>(3)</sup>			1	MHz	
$t_s$	Settling time	$A_V = -1$ , $R_L = 10\text{ k}\Omega$ <sup>(3)</sup> , Step = $0.5\text{ V}$ to $2.5\text{ V}$ , $C_L = 100\text{ pF}$ <sup>(3)</sup>	To 0.1%		1.5	$\mu\text{s}$	
			To 0.01%		2.6		
$\phi_m$	Phase margin at unity gain	$R_L = 10\text{ k}\Omega$ <sup>(3)</sup> , $C_L = 100\text{ pF}$ <sup>(3)</sup>			50°		
	Gain margin	$R_L = 10\text{ k}\Omega$ <sup>(3)</sup> , $C_L = 100\text{ pF}$ <sup>(3)</sup>			10	dB	

(1)  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ .

(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.

(3) Referenced to 0 V.

## 6.6 Electrical Characteristics: $V_{DD\pm} = \pm 5\text{ V}$ (TLC2272-Q1 and TLC2272A-Q1)

at specified free-air temperature,  $V_{DD\pm} = \pm 5\text{ V}$ ;  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
$V_{IO}$	Input offset voltage	$V_{IC} = 0\text{ V}$ , $V_O = 0\text{ V}$ , $R_S = 50\ \Omega$	TLC2272-Q1	$T_A = 25^\circ\text{C}$	300	2500	$\mu\text{V}$	
			TLC2272A-Q1		300	950		
			TLC2272-Q1	Full Range <sup>(1)</sup>				3000
			TLC2272A-Q1					1500
$\alpha_{VIO}$	Temperature coefficient of input offset voltage	$V_{IC} = 0\text{ V}$ , $V_O = 0\text{ V}$ , $R_S = 50\ \Omega$			2	$\mu\text{V}/^\circ\text{C}$		
	Input offset voltage long-term drift <sup>(2)</sup>	$V_{IC} = 0\text{ V}$ , $V_O = 0\text{ V}$ , $R_S = 50\ \Omega$			0.002	$\mu\text{V}/\text{mo}$		
$I_{IO}$	Input offset current	$V_{IC} = 0\text{ V}$ , $V_O = 0\text{ V}$ , $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$		0.5	60	pA	
			Full Range <sup>(1)</sup>			800		
$I_{IB}$	Input bias current	$V_{IC} = 0\text{ V}$ , $V_O = 0\text{ V}$ , $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$		1	60	pA	
			Full Range <sup>(1)</sup>			800		
$V_{ICR}$	Common-mode input voltage	$R_S = 50\ \Omega$ ; $ V_{IO}  \leq 5\text{ mV}$	$T_A = 25^\circ\text{C}$		-5.3	0	4	V
			Full Range <sup>(1)</sup>		-5	0	3.5	
$V_{OM+}$	Maximum positive peak output voltage		$I_O = -20\ \mu\text{A}$		4.99		V	
			$I_O = -200\ \mu\text{A}$	$T_A = 25^\circ\text{C}$	4.85	4.93		
				Full Range <sup>(1)</sup>	4.85			
			$I_O = -1\text{ mA}$	$T_A = 25^\circ\text{C}$	4.25	4.65		
Full Range <sup>(1)</sup>	4.25							
$V_{OM-}$	Maximum negative peak output voltage	$V_{IC} = 0\text{ V}$	$I_O = 50\ \mu\text{A}$		-4.99		V	
			$I_O = 500\ \mu\text{A}$	$T_A = 25^\circ\text{C}$	-4.85	-4.91		
				Full Range <sup>(1)</sup>	-4.85			
			$I_O = 5\text{ mA}$	$T_A = 25^\circ\text{C}$	-3.5	-4.1		
Full Range <sup>(1)</sup>	-3.5							

## 6.6 Electrical Characteristics: $V_{DD\pm} = \pm 5\text{ V}$ (TLC2272-Q1 and TLC2272A-Q1) (continued)

at specified free-air temperature,  $V_{DD\pm} = \pm 5\text{ V}$ ;  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$A_{VD}$	Large-signal differential voltage amplification	$V_O = \pm 4\text{ V}$	$R_L = 10\text{ k}\Omega$	$T_A = 25^\circ\text{C}$	20	50	V/mV
				Full Range <sup>(1)</sup>	20		
			$R_L = 1\text{ M}\Omega$			300	
$r_{id}$	Differential input resistance				$10^{12}$		$\Omega$
$r_i$	Common-mode input resistance				$10^{12}$		$\Omega$
$c_i$	Common-mode input capacitance	$f = 10\text{ kHz}$ , P package			8		pF
$Z_o$	Closed-loop output impedance	$f = 1\text{ MHz}$ , $A_V = 10$			130		$\Omega$
CMRR	Common-mode rejection ratio	$V_{IC} = -5\text{ V to } 2.7\text{ V}$ , $V_O = 0\text{ V}$ , $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$	75	80	dB	
			Full Range <sup>(1)</sup>	75			
$k_{SVR}$	Supply-voltage rejection ratio ( $\Delta V_{DD} / \Delta V_{IO}$ )	$V_{DD+} = 2.2\text{ V to } \pm 8\text{ V}$ , $V_{IC} = 0\text{ V}$ , no load	$T_A = 25^\circ\text{C}$	80	95	dB	
			Full Range <sup>(1)</sup>	80			
$I_{DD}$	Supply current	$V_O = 0\text{ V}$ , no load	$T_A = 25^\circ\text{C}$		2.4	3	mA
			Full Range <sup>(1)</sup>				
SR	Slew rate at unity gain	$V_O = \pm 2.3\text{ V}$ , $R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$	$T_A = 25^\circ\text{C}$	2.3	3.6	V/ $\mu\text{s}$	
			Full Range <sup>(1)</sup>	1.7			
$V_n$	Equivalent input noise voltage	$f = 10\text{ Hz}$			50	nV/ $\sqrt{\text{Hz}}$	
		$f = 1\text{ kHz}$			9		
$V_{NPP}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to } 1\text{ Hz}$			1	$\mu\text{V}$	
		$f = 0.1\text{ Hz to } 10\text{ Hz}$			1.4		
$I_n$	Equivalent input noise current				0.6	fA/ $\sqrt{\text{Hz}}$	
THD+N	Total harmonic distortion + noise	$V_O = \pm 2.3$ , $f = 20\text{ kHz}$ , $R_L = 10\text{ k}\Omega$	$A_V = 1$		0.0011%		
			$A_V = 10$		0.004%		
			$A_V = 100$		0.03%		
	Gain-bandwidth product	$f = 10\text{ kHz}$ , $R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$			2.25	MHz	
$B_{OM}$	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6\text{ V}$ , $A_V = 1$ , $R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$			0.54	MHz	
$t_s$	Settling time	$A_V = -1$ , $R_L = 10\text{ k}\Omega$ , Step = $-2.3\text{ V to } 2.3\text{ V}$ , $C_L = 100\text{ pF}$	To 0.1%		1.5	$\mu\text{s}$	
			To 0.01%		3.2		
$\Phi_m$	Phase margin at unity gain	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$			52°		
	Gain margin	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$			10	dB	

(1)  $T_A = -40^\circ\text{C to } 125^\circ\text{C}$ .

(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.

## 6.7 Electrical Characteristics: $V_{DD} = 5\text{ V}$ (TLC2274-Q1 and TLC2274A-Q1)

at specified free-air temperature,  $V_{DD} = 5\text{ V}$ ;  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{IO}$	Input offset voltage	$V_{IC} = 0\text{ V}$ , $V_{DD\pm} = \pm 2.5\text{ V}$ , $V_O = 0\text{ V}$ , $R_S = 50\ \Omega$	TLC2274-Q1	$T_A = 25^\circ\text{C}$	300	2500	$\mu\text{V}$
			TLC2274A-Q1		300	950	
			TLC2274-Q1	Full Range <sup>(1)</sup>		3000	
			TLC2274A-Q1		1500		
$\alpha_{VIO}$	Temperature coefficient of input offset voltage	$V_{IC} = 0\text{ V}$ , $V_{DD\pm} = \pm 2.5\text{ V}$ , $V_O = 0\text{ V}$ , $R_S = 50\ \Omega$			2		$\mu\text{V}/^\circ\text{C}$
	Input offset voltage long-term drift <sup>(2)</sup>	$V_{IC} = 0\text{ V}$ , $V_{DD\pm} = \pm 2.5\text{ V}$ , $V_O = 0\text{ V}$ , $R_S = 50\ \Omega$			0.002		$\mu\text{V}/\text{mo}$
$I_{IO}$	Input offset current	$V_{IC} = 0\text{ V}$ , $V_{DD\pm} = \pm 2.5\text{ V}$ , $V_O = 0\text{ V}$ , $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$	0.5	60	$\text{pA}$	
			Full Range <sup>(1)</sup>		800		
$I_{IB}$	Input bias current	$V_{IC} = 0\text{ V}$ , $V_{DD\pm} = \pm 2.5\text{ V}$ , $V_O = 0\text{ V}$ , $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$	1	60	$\text{pA}$	
			Full Range <sup>(1)</sup>		800		
$V_{ICR}$	Common-mode input voltage	$R_S = 50\ \Omega$ ; $ V_{IO}  \leq 5\text{ mV}$	$T_A = 25^\circ\text{C}$	-0.3	2.5	4	V
			Full Range <sup>(1)</sup>	0	2.5	3.5	
$V_{OH}$	High-level output voltage	$I_{OH} = -20\ \mu\text{A}$ $I_{OH} = -200\ \mu\text{A}$ $I_{OH} = -1\text{ mA}$	$T_A = 25^\circ\text{C}$	4.85	4.93	V	
			Full Range <sup>(1)</sup>	4.85			
			$T_A = 25^\circ\text{C}$	4.25	4.65		
			Full Range <sup>(1)</sup>	4.25			
$V_{OL}$	Low-level output voltage	$V_{IC} = 2.5\text{ V}$	$I_{OL} = 50\ \mu\text{A}$		0.01	V	
			$I_{OL} = 500\ \mu\text{A}$	$T_A = 25^\circ\text{C}$	0.09		0.15
				Full Range <sup>(1)</sup>			0.15
			$I_{OL} = 5\text{ mA}$	$T_A = 25^\circ\text{C}$	0.9		1.5
Full Range <sup>(1)</sup>		1.5					
$A_{VD}$	Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}$ , $V_O = 1\text{ V to }4\text{ V}$	$R_L = 10\text{ k}\Omega^{(3)}$	$T_A = 25^\circ\text{C}$	10	35	V/mV
			$R_L = 1\text{ M}\Omega^{(3)}$	Full Range <sup>(1)</sup>	10		
						175	
$r_{id}$	Differential input resistance				$10^{12}$	$\Omega$	
$r_i$	Common-mode input resistance				$10^{12}$	$\Omega$	
$c_i$	Common-mode input capacitance	$f = 10\text{ kHz}$ , P package			8	pF	
$z_o$	Closed-loop output impedance	$f = 1\text{ MHz}$ , $A_V = 10$			140	$\Omega$	
CMRR	Common-mode rejection ratio	$V_{IC} = 0\text{ V to }2.7\text{ V}$ , $V_O = 2.5\text{ V}$ , $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$	70	75	dB	
			Full Range <sup>(1)</sup>	70			
$k_{SVR}$	Supply-voltage rejection ratio ( $\Delta V_{DD} / \Delta V_{IO}$ )	$V_{DD} = 4.4\text{ V to }16\text{ V}$ , $V_{IC} = V_{DD} / 2$ , no load	$T_A = 25^\circ\text{C}$	80	95	dB	
			Full Range <sup>(1)</sup>	80			
$I_{DD}$	Supply current	$V_O = 2.5\text{ V}$ , no load	$T_A = 25^\circ\text{C}$	4.4	6	mA	
			Full Range <sup>(1)</sup>		6		
SR	Slew rate at unity gain	$V_O = 0.5\text{ V to }2.5\text{ V}$ , $R_L = 10\text{ k}\Omega^{(3)}$ , $C_L = 100\text{ pF}^{(3)}$	$T_A = 25^\circ\text{C}$	2.3	3.6	V/ $\mu\text{s}$	
			Full Range <sup>(1)</sup>	1.7			
$V_n$	Equivalent input noise voltage	$f = 10\text{ Hz}$ $f = 1\text{ kHz}$		50		nV/ $\sqrt{\text{Hz}}$	
				9			
$V_{NPP}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$		1		$\mu\text{V}$	
		$f = 0.1\text{ Hz to }10\text{ Hz}$		1.4			
$I_n$	Equivalent input noise current			0.6		fA/ $\sqrt{\text{Hz}}$	
THD+N	Total harmonic distortion + noise	$V_O = 0.5\text{ V to }2.5\text{ V}$ , $f = 20\text{ kHz}$ , $R_L = 10\text{ k}\Omega^{(3)}$	$A_V = 1$		0.0013%		
			$A_V = 10$		0.004%		
			$A_V = 100$		0.03%		
	Gain-bandwidth product	$f = 10\text{ kHz}$ , $R_L = 10\text{ k}\Omega^{(3)}$ , $C_L = 100\text{ pF}^{(3)}$			2.18	MHz	
$B_{OM}$	Maximum output-swing bandwidth	$V_{O(PP)} = 2\text{ V}$ , $A_V = 1$ , $R_L = 10\text{ k}\Omega^{(3)}$ , $C_L = 100\text{ pF}^{(3)}$			1	MHz	



## 6.7 Electrical Characteristics: $V_{DD} = 5\text{ V}$ (TLC2274-Q1 and TLC2274A-Q1) (continued)

at specified free-air temperature,  $V_{DD} = 5\text{ V}$ ;  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_s$	Settling time	$A_V = -1$ , $R_L = 10\text{ k}\Omega^{(3)}$ , Step = 0.5 V to 2.5 V, $C_L = 100\text{ pF}^{(3)}$	To 0.1%		1.5		$\mu\text{s}$
			To 0.01%		2.6		
$\phi_m$	Phase margin at unity gain	$R_L = 10\text{ k}\Omega^{(3)}$ , $C_L = 100\text{ pF}^{(3)}$			50°		
	Gain margin	$R_L = 10\text{ k}\Omega^{(3)}$ , $C_L = 100\text{ pF}^{(3)}$			10		dB

- $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ .
- Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.
- Referenced to 0 V.

## 6.8 Electrical Characteristics: $V_{DD\pm} = \pm 5\text{ V}$ (TLC2274-Q1 and TLC2274A-Q1)

at specified free-air temperature,  $V_{DD\pm} = \pm 5\text{ V}$ ;  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
$V_{IO}$	Input offset voltage	$V_{IC} = 0\text{ V}$ , $V_O = 0\text{ V}$ , $R_S = 50\ \Omega$	TLC2274-Q1	$T_A = 25^\circ\text{C}$	300	2500	$\mu\text{V}$	
			TLC2274A-Q1		300	950		
			TLC2274-Q1	Full Range <sup>(1)</sup>		3000		
			TLC2274A-Q1			1500		
$\alpha_{VIO}$	Temperature coefficient of input offset voltage	$V_{IC} = 0\text{ V}$ , $V_O = 0\text{ V}$ , $R_S = 50\ \Omega$			2		$\mu\text{V}/^\circ\text{C}$	
	Input offset voltage long-term drift <sup>(2)</sup>	$V_{IC} = 0\text{ V}$ , $V_O = 0\text{ V}$ , $R_S = 50\ \Omega$			0.002		$\mu\text{V}/\text{mo}$	
$I_{IO}$	Input offset current	$V_{IC} = 0\text{ V}$ , $V_O = 0\text{ V}$ , $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$		0.5	60	pA	
			Full Range <sup>(1)</sup>			800		
$I_{IB}$	Input bias current	$V_{IC} = 0\text{ V}$ , $V_O = 0\text{ V}$ , $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$		1	60	pA	
			Full Range <sup>(1)</sup>			800		
$V_{ICR}$	Common-mode input voltage	$R_S = 50\ \Omega$ ; $ V_{IO}  \leq 5\text{ mV}$	$T_A = 25^\circ\text{C}$		-5.3	0	4	V
			Full Range <sup>(1)</sup>		-5	0	3.5	
$V_{OM+}$	Maximum positive peak output voltage	$I_O = -20\ \mu\text{A}$	$T_A = 25^\circ\text{C}$		4.85	4.93	V	
			Full Range <sup>(1)</sup>		4.85			
			$T_A = 25^\circ\text{C}$		4.25	4.65		
			Full Range <sup>(1)</sup>		4.25			
$V_{OM-}$	Maximum negative peak output voltage	$V_{IC} = 0\text{ V}$	$I_O = 50\ \mu\text{A}$			-4.99	V	
			$I_O = 500\ \mu\text{A}$	$T_A = 25^\circ\text{C}$		-4.85		-4.91
				Full Range <sup>(1)</sup>		-4.85		
			$I_O = 5\text{ mA}$	$T_A = 25^\circ\text{C}$		-3.5		-4.1
Full Range <sup>(1)</sup>		-3.5						
$A_{VD}$	Large-signal differential voltage amplification	$V_O = \pm 4\text{ V}$	$R_L = 10\text{ k}\Omega$	$T_A = 25^\circ\text{C}$	20	50	V/mV	
				Full Range <sup>(1)</sup>	20			
			$R_L = 1\text{ M}\Omega$		300			
$r_{id}$	Differential input resistance				$10^{12}$		$\Omega$	
$r_i$	Common-mode input resistance				$10^{12}$		$\Omega$	
$c_i$	Common-mode input capacitance	$f = 10\text{ kHz}$ , P package			8		pF	
$z_o$	Closed-loop output impedance	$f = 1\text{ MHz}$ , $A_V = 10$			130		$\Omega$	
CMRR	Common-mode rejection ratio	$V_{IC} = -5\text{ V}$ to $2.7\text{ V}$ , $V_O = 0\text{ V}$ , $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$		75	80	dB	
			Full Range <sup>(1)</sup>		75			
$k_{SVR}$	Supply-voltage rejection ratio ( $\Delta V_{DD} / \Delta V_{IO}$ )	$V_{DD+} = 2.2\text{ V}$ to $\pm 8\text{ V}$ , $V_{IC} = 0\text{ V}$ , no load	$T_A = 25^\circ\text{C}$		80	95	dB	
			Full Range <sup>(1)</sup>		80			
$I_{DD}$	Supply current	$V_O = 0\text{ V}$ , no load	$T_A = 25^\circ\text{C}$		4.8	6	mA	
			Full Range <sup>(1)</sup>			6		

## 6.8 Electrical Characteristics: $V_{DD\pm} = \pm 5\text{ V}$ (TLC2274-Q1 and TLC2274A-Q1) (continued)

at specified free-air temperature,  $V_{DD\pm} = \pm 5\text{ V}$ ;  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_O = \pm 2.3\text{ V}$ , $R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$	$T_A = 25^\circ\text{C}$	2.3	3.6		V/ $\mu\text{s}$
			Full Range <sup>(1)</sup>	1.7			
$V_n$	Equivalent input noise voltage		$f = 10\text{ Hz}$		50		nV/ $\sqrt{\text{Hz}}$
			$f = 1\text{ kHz}$		9		
$V_{NPP}$	Peak-to-peak equivalent input noise voltage		$f = 0.1\text{ Hz to }1\text{ Hz}$		1		$\mu\text{V}$
			$f = 0.1\text{ Hz to }10\text{ Hz}$		1.4		
$I_n$	Equivalent input noise current				0.6		fA/ $\sqrt{\text{Hz}}$
THD+N	Total harmonic distortion + noise	$V_O = \pm 2.3$ , $f = 20\text{ kHz}$ , $R_L = 10\text{ k}\Omega$	$A_V = 1$		0.0011%		
			$A_V = 10$		0.004%		
			$A_V = 100$		0.03%		
	Gain-bandwidth product	$f = 10\text{ kHz}$ , $R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$			2.25		MHz
$B_{OM}$	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6\text{ V}$ , $A_V = 1$ , $R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$			0.54		MHz
$t_s$	Settling time	$A_V = -1$ , $R_L = 10\text{ k}\Omega$ , Step = $-2.3\text{ V to }2.3\text{ V}$ , $C_L = 100\text{ pF}$	To 0.1%		1.5		$\mu\text{s}$
			To 0.01%		3.2		
$\phi_m$	Phase margin at unity gain	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$			52°		
	Gain margin	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$			10		dB

(1)  $T_A = -40^\circ\text{C to }125^\circ\text{C}$ .

(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.

## 6.9 Typical Characteristics

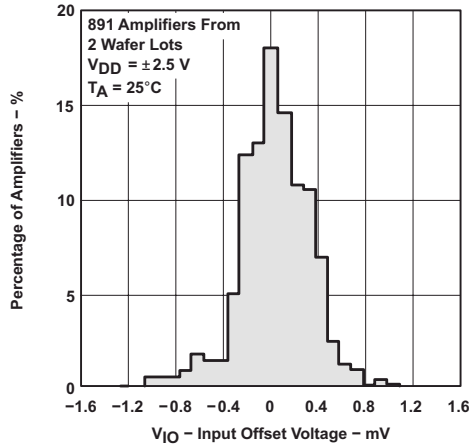
**表 6-1. Table of Graphs**

			FIGURE <sup>(1)</sup>
$V_{IO}$	Input offset voltage	Distribution	1, 2, 3, 4
		vs Common-mode voltage	5, 6
$\alpha_{VIO}$	Input offset voltage temperature coefficient	Distribution	7, 8, 9, 10 <sup>(2)</sup>
$I_{IB} / I_{IO}$	Input bias and input offset current	vs Free-air temperature	11 <sup>(2)</sup>
$V_I$	Input voltage	vs Supply voltage	12
		vs Free-air temperature	13 <sup>(2)</sup>
$V_{OH}$	High-level output voltage	vs High-level output current	14 <sup>(2)</sup>
$V_{OL}$	Low-level output voltage	vs Low-level output current	15, 16 <sup>(2)</sup>
$V_{OM+}$	Maximum positive peak output voltage	vs Output current	17 <sup>(2)</sup>
$V_{OM-}$	Maximum negative peak output voltage	vs Output current	18 <sup>(2)</sup>
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	19
$I_{OS}$	Short-circuit output current	vs Supply voltage	20
		vs Free-air temperature	21 <sup>(2)</sup>
$V_O$	Output voltage	vs Differential input voltage	22, 23
$A_{VD}$	Large-signal differential voltage amplification	vs Load resistance	24
	Large-signal differential voltage amplification and phase margin	vs Frequency	25, 26
	Large-signal differential voltage amplification	vs Free-air temperature	27 <sup>(2)</sup> , 28 <sup>(2)</sup>
$Z_0$	Output impedance	vs Frequency	29, 30
CMRR	Common-mode rejection ratio	vs Frequency	31
		vs Free-air temperature	32
$k_{SVR}$	Supply-voltage rejection ratio	vs Frequency	33, 34
		vs Free-air temperature	35 <sup>(2)</sup>
$I_{DD}$	Supply current	vs Supply voltage	36 <sup>(2)</sup> , 37 <sup>(2)</sup>
		vs Free-air temperature	38 <sup>(2)</sup> , 39 <sup>(2)</sup>
SR	Slew rate	vs Load Capacitance	40
		vs Free-air temperature	41 <sup>(2)</sup>
$V_O$	Inverting large-signal pulse response		42, 43
	Voltage-follower large-signal pulse response		44, 45
	Inverting small-signal pulse response		46, 47
	Voltage-follower small-signal pulse response		48, 49
$V_n$	Equivalent input noise voltage	vs Frequency	50, 51
	Noise voltage over a 10-second period		52
	Integrated noise voltage	vs Frequency	53
THD+N	Total harmonic distortion + noise	vs Frequency	54
	Gain-bandwidth product	vs Supply voltage	55
		vs Free-air temperature	56 <sup>(2)</sup>
$\Phi_m$	Phase margin	vs Load capacitance	57
	Gain margin	vs Load capacitance	58

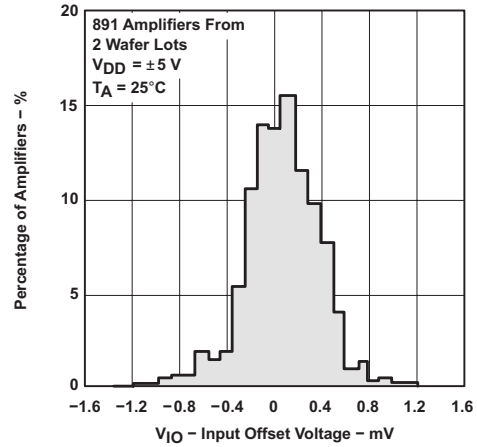
(1) For all graphs where  $V_{DD} = 5\text{ V}$ , all loads are referenced to 2.5 V.

(2) Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

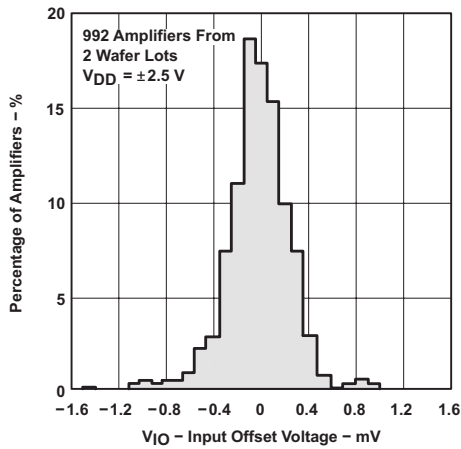
## 6.9 Typical Characteristics (continued)



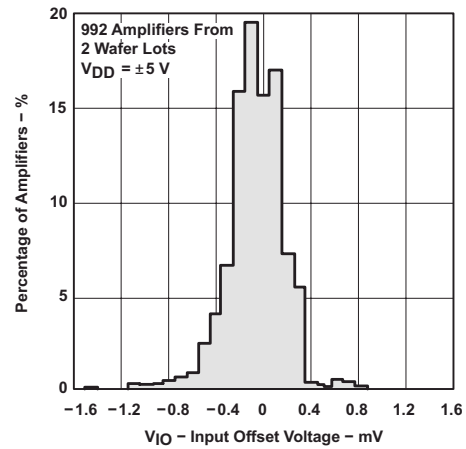
6-1. Distribution of TLC2272-Q1 Input Offset Voltage



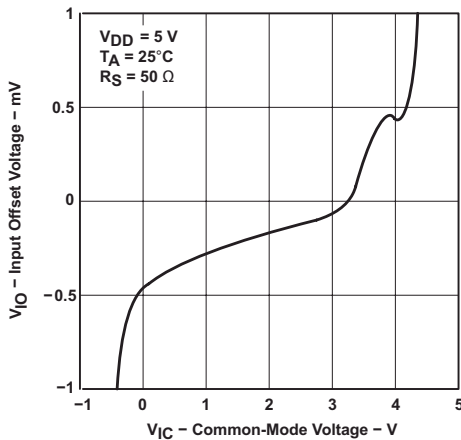
6-2. Distribution of TLC2272-Q1 Input Offset Voltage



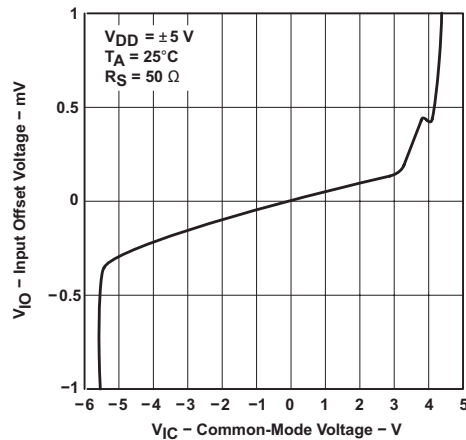
6-3. Distribution of TLC2274-Q1 Input Offset Voltage



6-4. Distribution of TLC2274-Q1 Input Offset Voltage

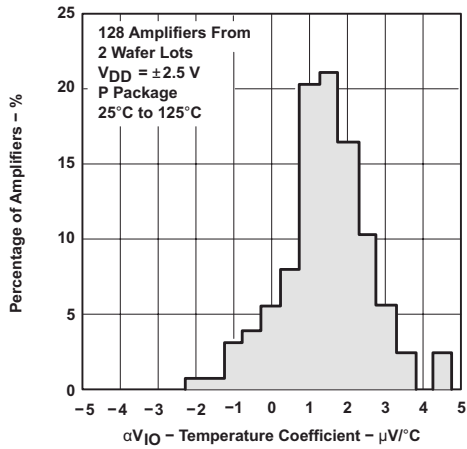


6-5. Input Offset Voltage vs Common-Mode Voltage

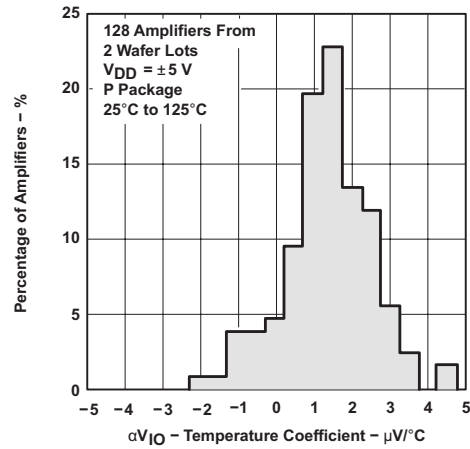


6-6. Input Offset Voltage vs Common-Mode Voltage

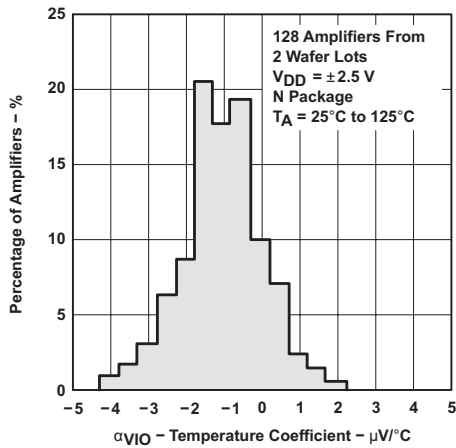
## 6.9 Typical Characteristics (continued)




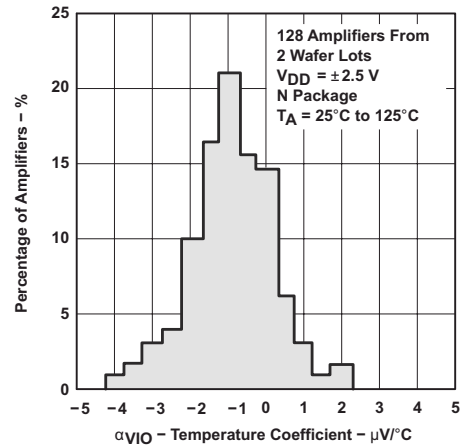

**6-7. Distribution of TLC2272-Q1 vs Input Offset Voltage Temperature Coefficient**




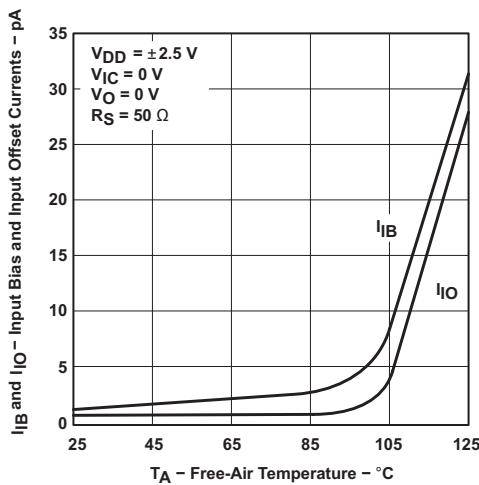

**6-8. Distribution of TLC2272-Q1 vs Input Offset Voltage Temperature Coefficient**



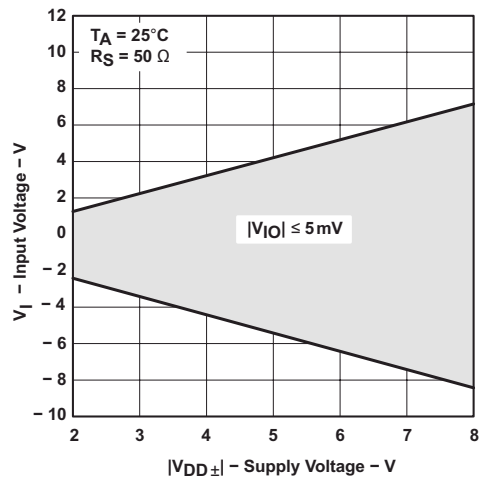

**6-9. Distribution of TLC2274-Q1 vs Input Offset Voltage Temperature Coefficient**




**6-10. Distribution of TLC2274-Q1 vs Input Offset Voltage Temperature Coefficient**




**6-11. Input Bias and Input Offset Current vs Free-Air Temperature**




**6-12. Input Voltage vs Supply Voltage**

## 6.9 Typical Characteristics (continued)

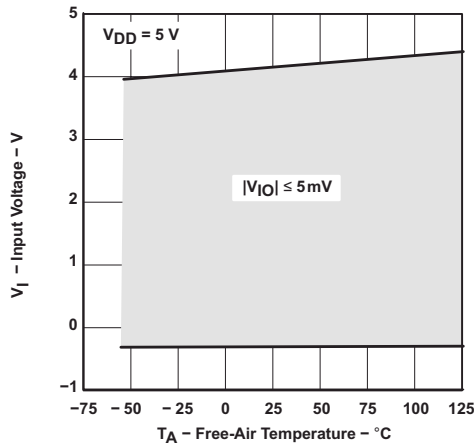


FIG 6-13. Input Voltage vs Free-Air Temperature

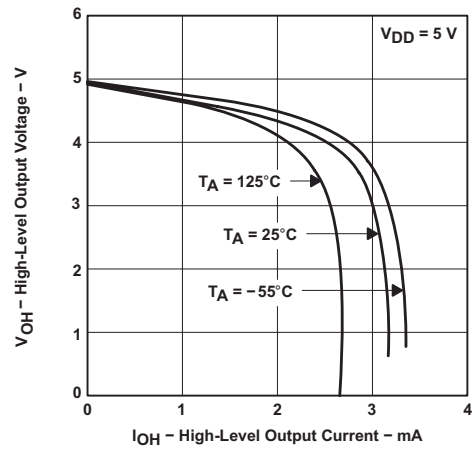


FIG 6-14. High-Level Output Voltage vs High-Level Output Current

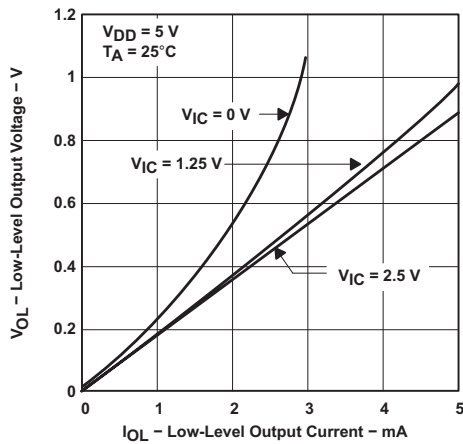


FIG 6-15. Low-Level Output Voltage vs Low-Level Output Current

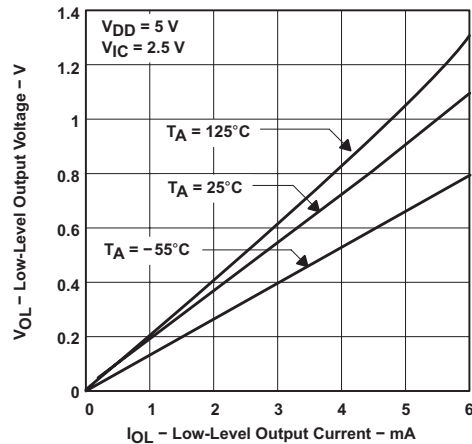


FIG 6-16. Low-Level Output Voltage vs Low-Level Output Current

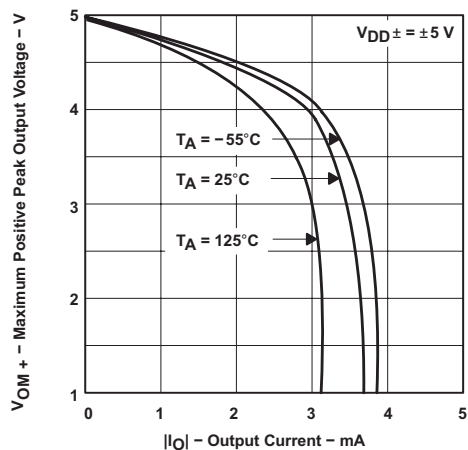


FIG 6-17. Maximum Positive Peak Output Voltage vs Output Current

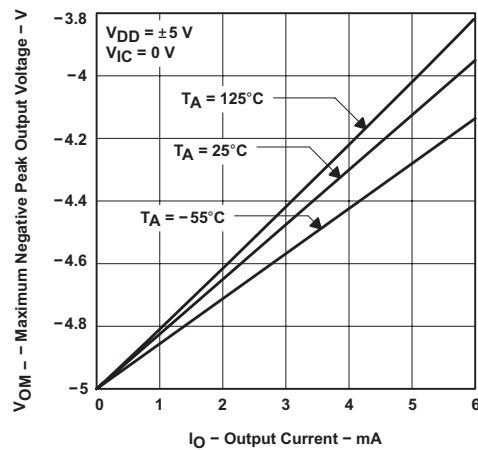
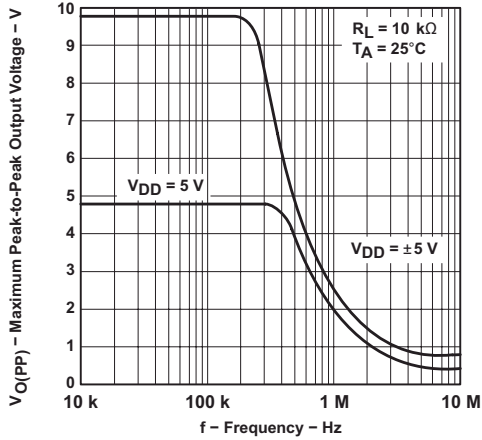
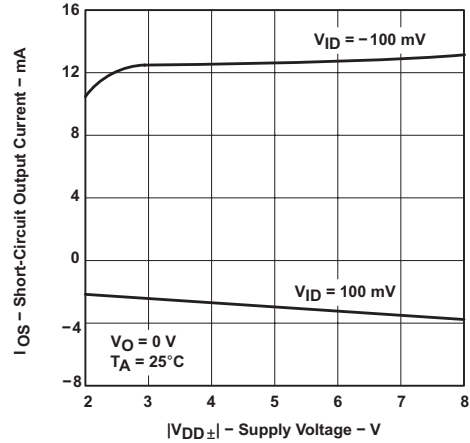


FIG 6-18. Maximum Positive Peak Output Voltage vs Output Current

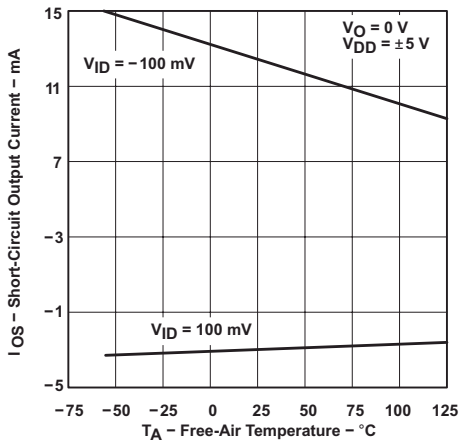
## 6.9 Typical Characteristics (continued)



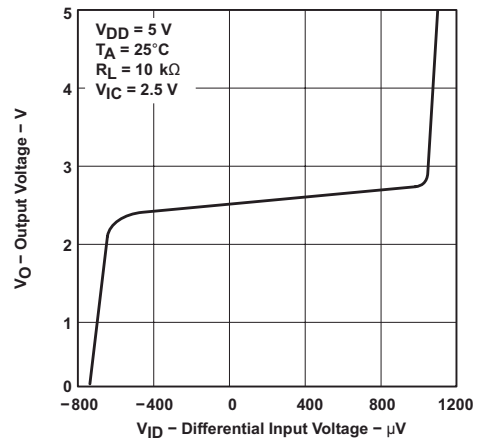
6-19. Maximum Peak-to-Peak Output Voltage vs Frequency



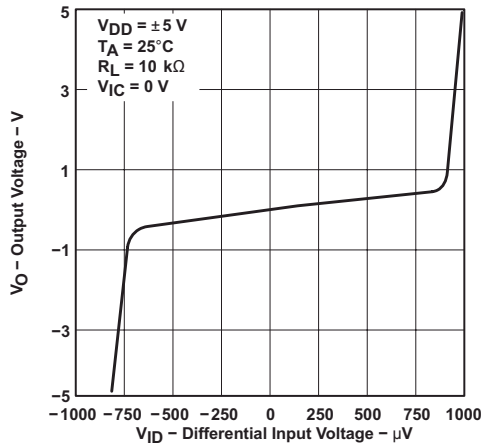
6-20. Short-Circuit Output Current vs Supply Voltage



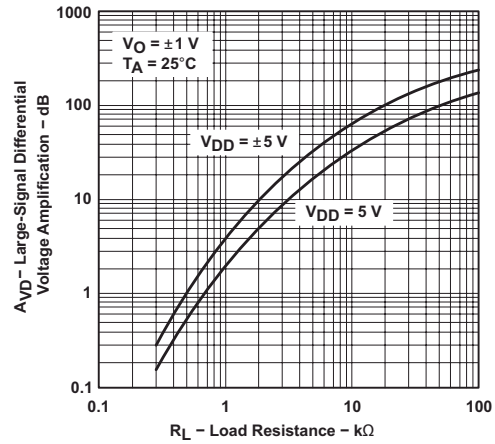
6-21. Short-Circuit Output Current vs Free-Air Temperature



6-22. Output Voltage vs Differential Input Voltage

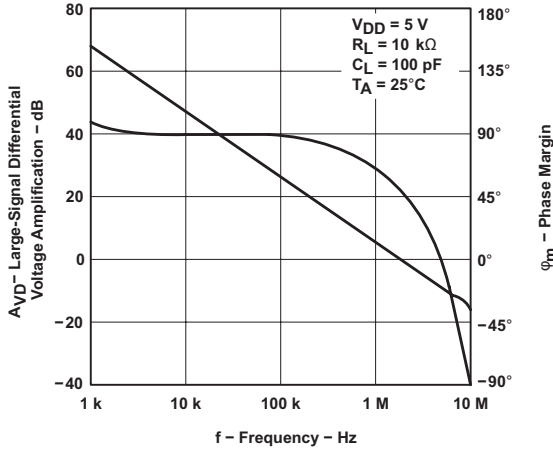


6-23. Output Voltage vs Differential Input Voltage

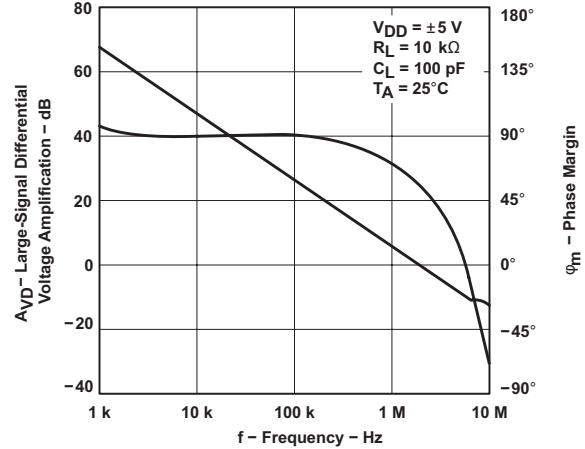


6-24. Large-Signal Differential Voltage Amplification vs Load Resistance

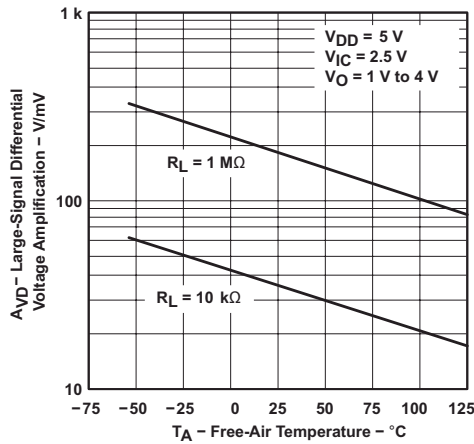
### 6.9 Typical Characteristics (continued)



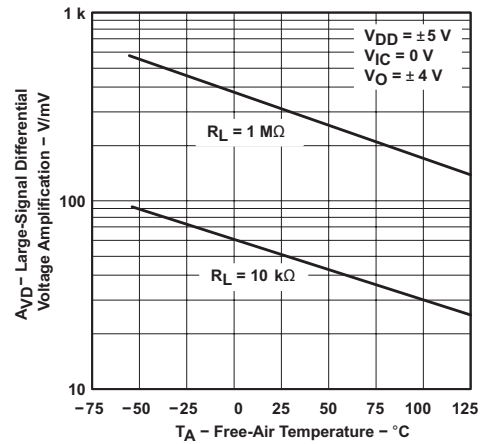
6-25. Large-Signal Differential Voltage Amplification and Phase Margin vs Frequency



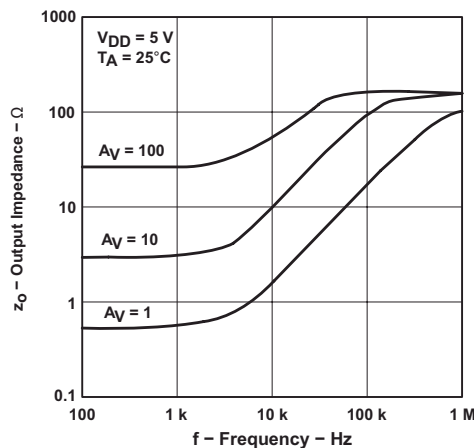
6-26. Large-Signal Differential Voltage Amplification and Phase Margin vs Frequency



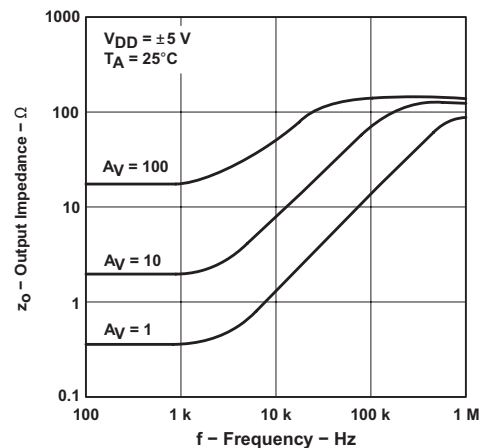
6-27. Large-Signal Differential Voltage Amplification vs Free-Air Temperature



6-28. Large-Signal Differential Voltage Amplification vs Free-Air Temperature



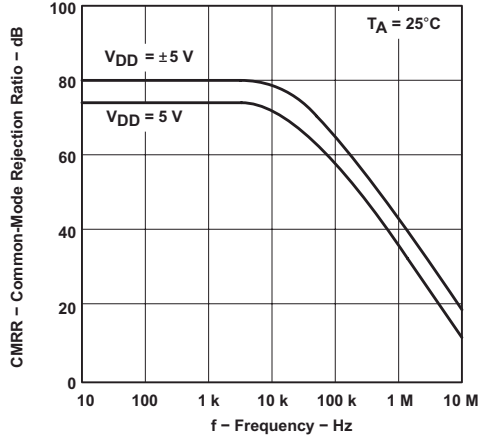
6-29. Output Impedance vs Frequency



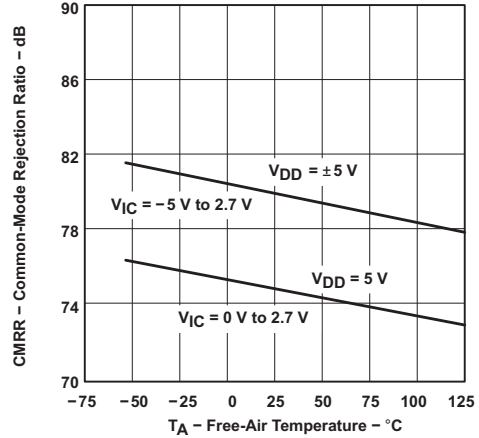
6-30. Output Impedance vs Frequency



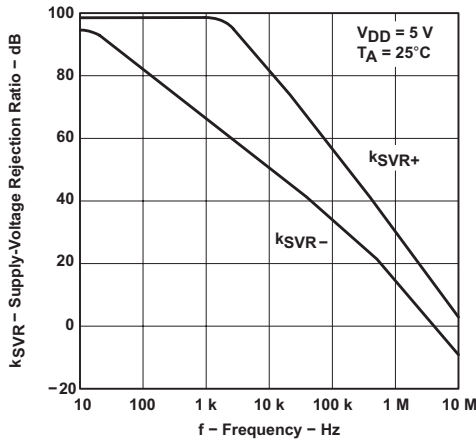
### 6.9 Typical Characteristics (continued)



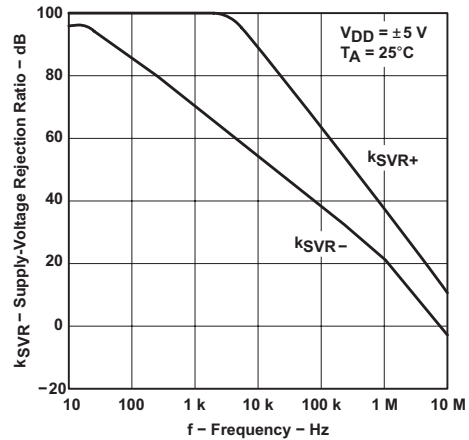
6-31. Common-Mode Rejection Ratio vs Frequency



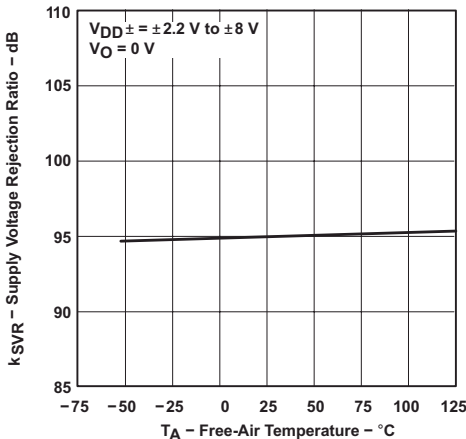
6-32. Common-Mode Rejection Ratio vs Free-Air Temperature



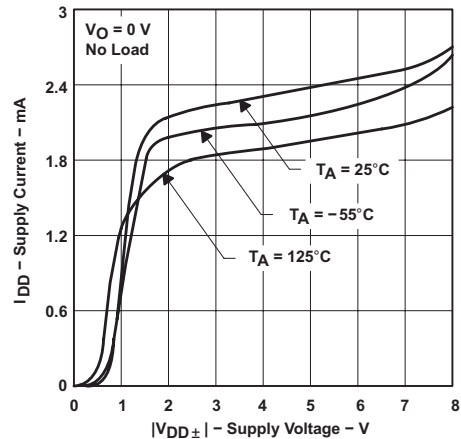
6-33. Supply-Voltage Rejection Ratio vs Frequency



6-34. Supply-Voltage Rejection Ratio vs Frequency

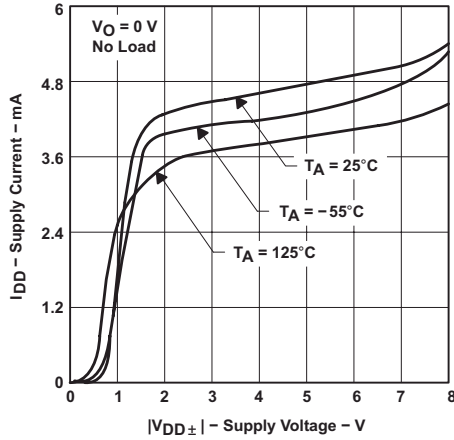


6-35. Supply-Voltage Rejection Ratio vs Free-Air Temperature

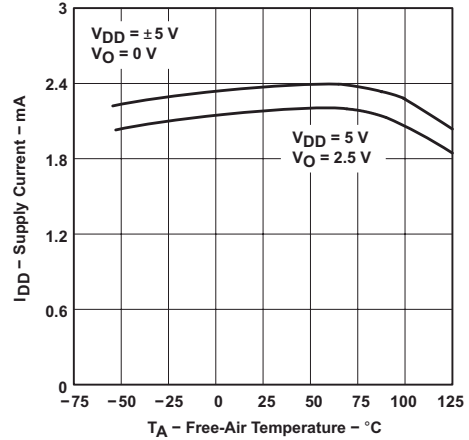


6-36. TLC2272-Q1 Supply Current vs Supply Voltage

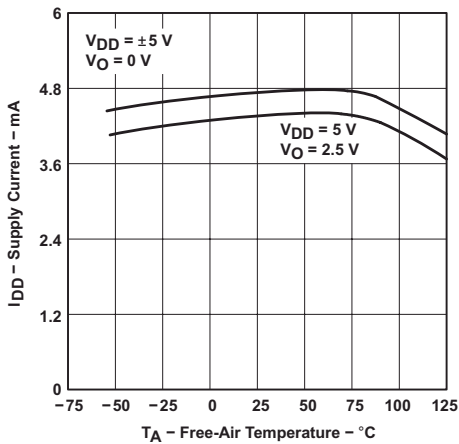
### 6.9 Typical Characteristics (continued)



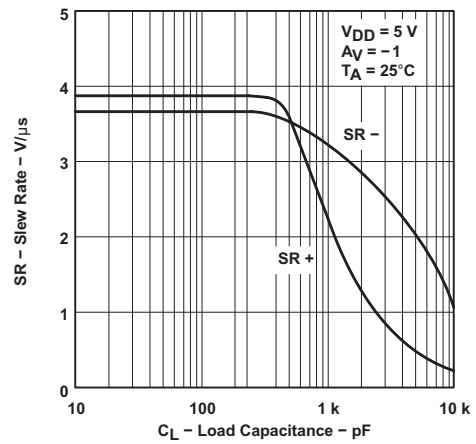
6-37. TLC2274-Q1 Supply Current vs Supply Voltage



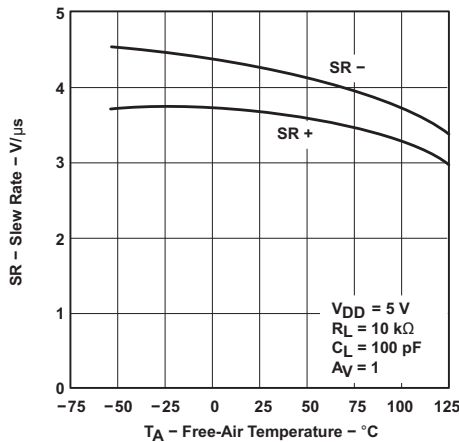
6-38. TLC2272-Q1 Supply Current vs Free-Air Temperature



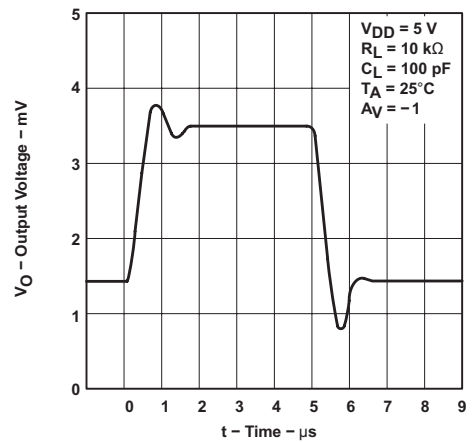
6-39. TLC2274-Q1 Supply Current vs Free-Air Temperature



6-40. Slew Rate vs Load Capacitance

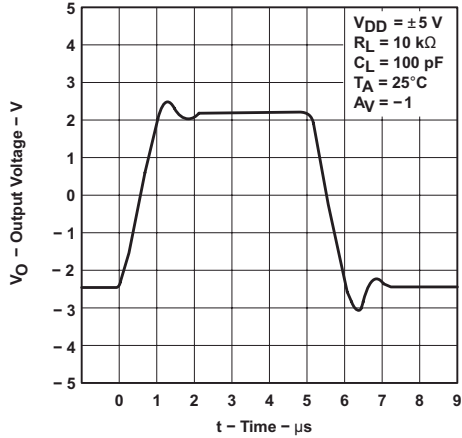


6-41. Slew Rate vs Free-Air Temperature

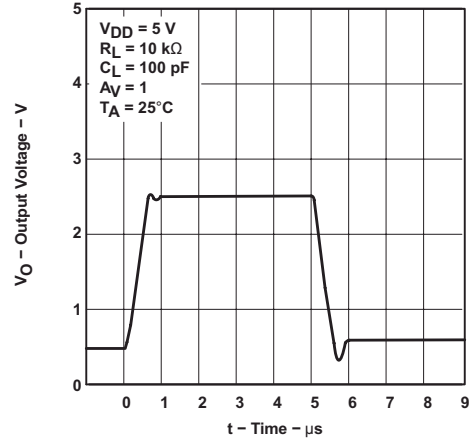


6-42. Inverting Large-Signal Pulse Response

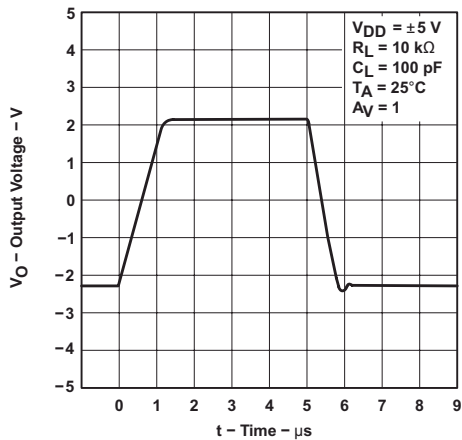
## 6.9 Typical Characteristics (continued)



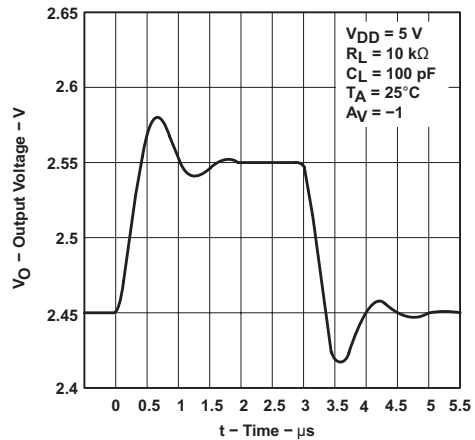
6-43. Inverting Large-Signal Pulse Response



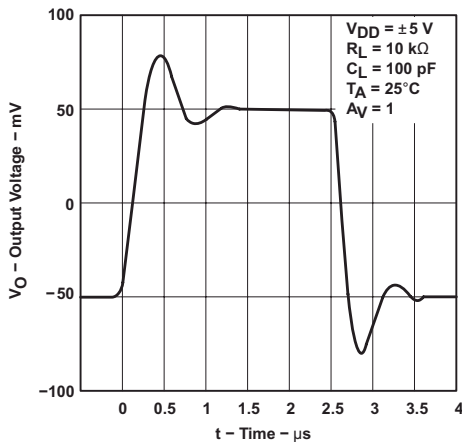
6-44. Voltage-Follower Large-Signal Pulse Response



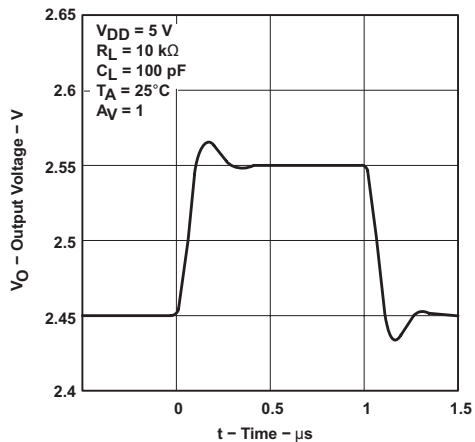
6-45. Voltage-Follower Large-Signal Pulse Response



6-46. Inverting Small-Signal Pulse Response

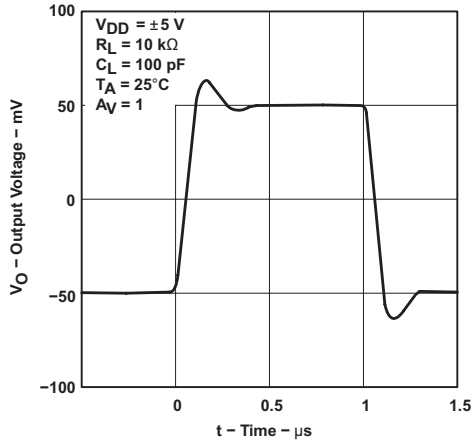


6-47. Inverting Small-Signal Pulse Response

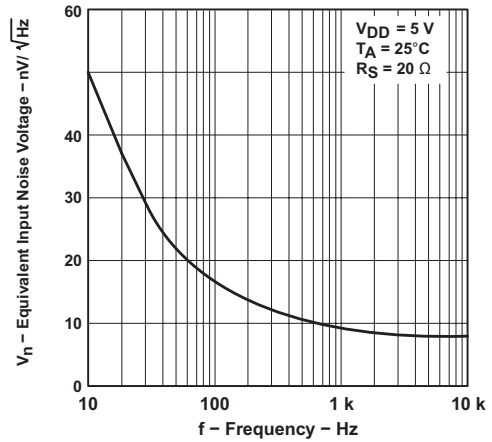


6-48. Voltage-Follower Small-Signal Pulse Response

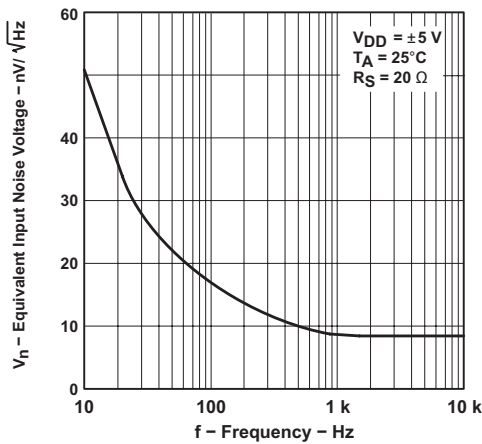
## 6.9 Typical Characteristics (continued)



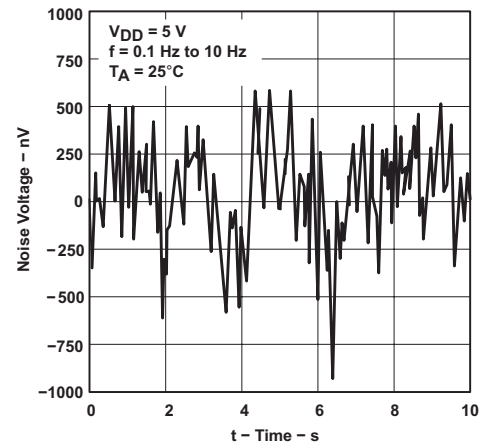
6-49. Voltage-Follower Small-Signal Pulse Response



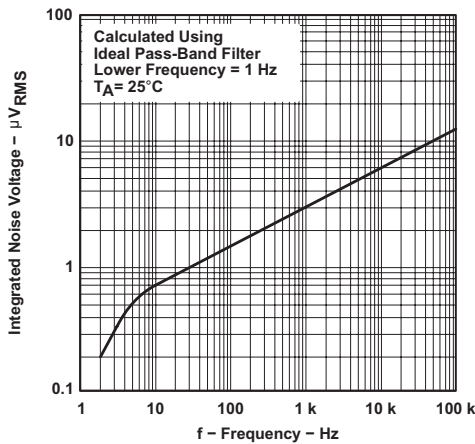
6-50. Equivalent Input Noise Voltage vs Frequency



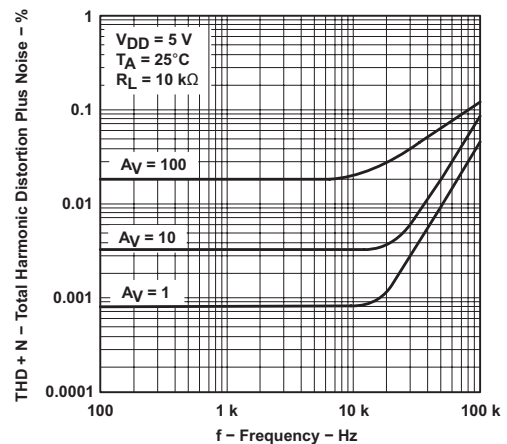
6-51. Equivalent Input Noise Voltage vs Frequency



6-52. Noise Voltage Over a 10 Second Period

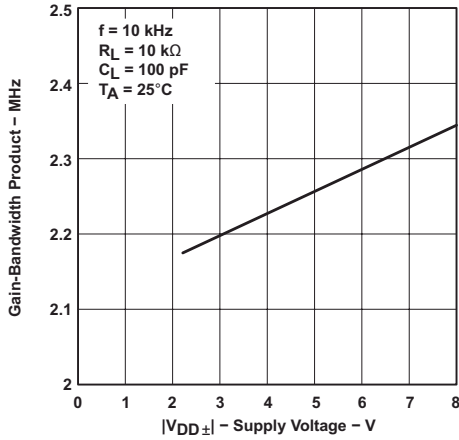


6-53. Integrated Noise Voltage vs Frequency

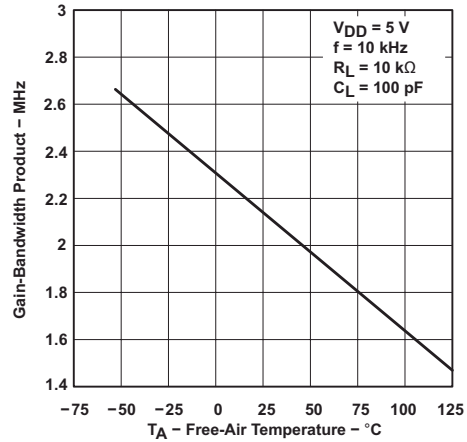


6-54. Total Harmonic Distortion + Noise vs Frequency

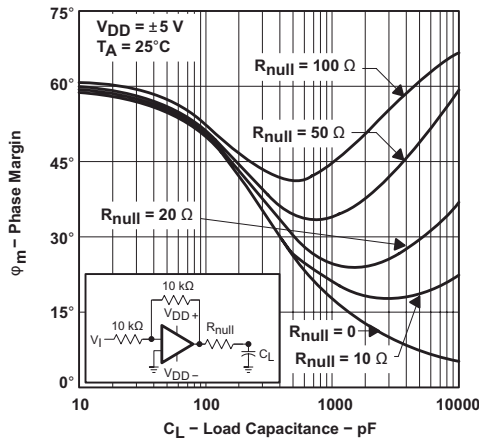
### 6.9 Typical Characteristics (continued)



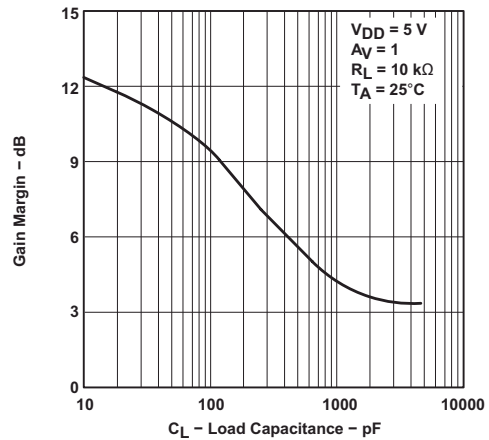
**6-55. Gain-Bandwidth Product vs Supply Voltage**



**6-56. Gain-Bandwidth Product vs Free-Air Temperature**



**6-57. Phase Margin vs Load Capacitance**



**6-58. Gain Margin vs Load Capacitance**

## 7 Detailed Description

### 7.1 Overview

The TLC227x-Q1 devices are a rail-to-rail output operational amplifiers. These devices operate from a 4.4-V to 16-V single supply and a  $\pm 2.2\text{-V}$   $\pm 8\text{-V}$  dual supply, are unity-gain stable, and are an excellent choice for a wide range of general-purpose applications.

### 7.2 Functional Block Diagram

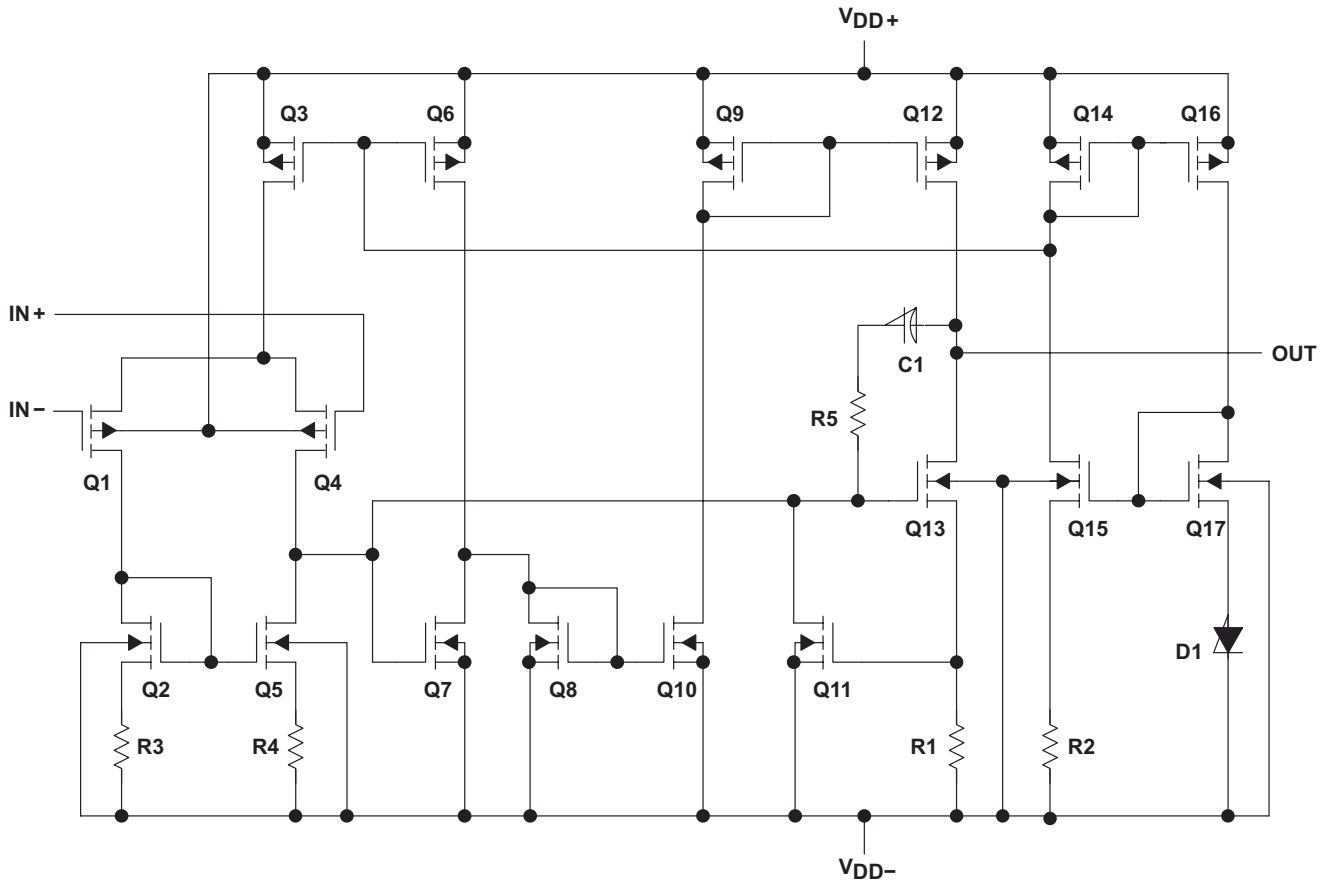


表 7-1. Actual Device Component Count<sup>(1)</sup>

COMPONENT	TLC2272-Q1	TLC2274-Q1
Transistors	38	76
Resistors	26	52
Diodes	9	18
Capacitors	3	6

(1) Includes both amplifiers and all ESD, bias, and trim circuitry.

### 7.3 Feature Description

The TLC227x-Q1 family features 2-MHz bandwidth and voltage noise of  $9\text{ nV}/\sqrt{\text{Hz}}$  with performance rated from 4.4 V to 16 V across an automotive temperature range ( $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ). LinMOS is a great choice for a wide range of audio, automotive, industrial, and instrumentation applications.

### 7.4 Device Functional Modes

The TLC227x-Q1 family of devices is powered on when the supply is connected. The device can operate with single or dual supply, depending on the application. The device is in full performance after the supply is greater than the recommended value.

## 8 Application and Implementation

### 注

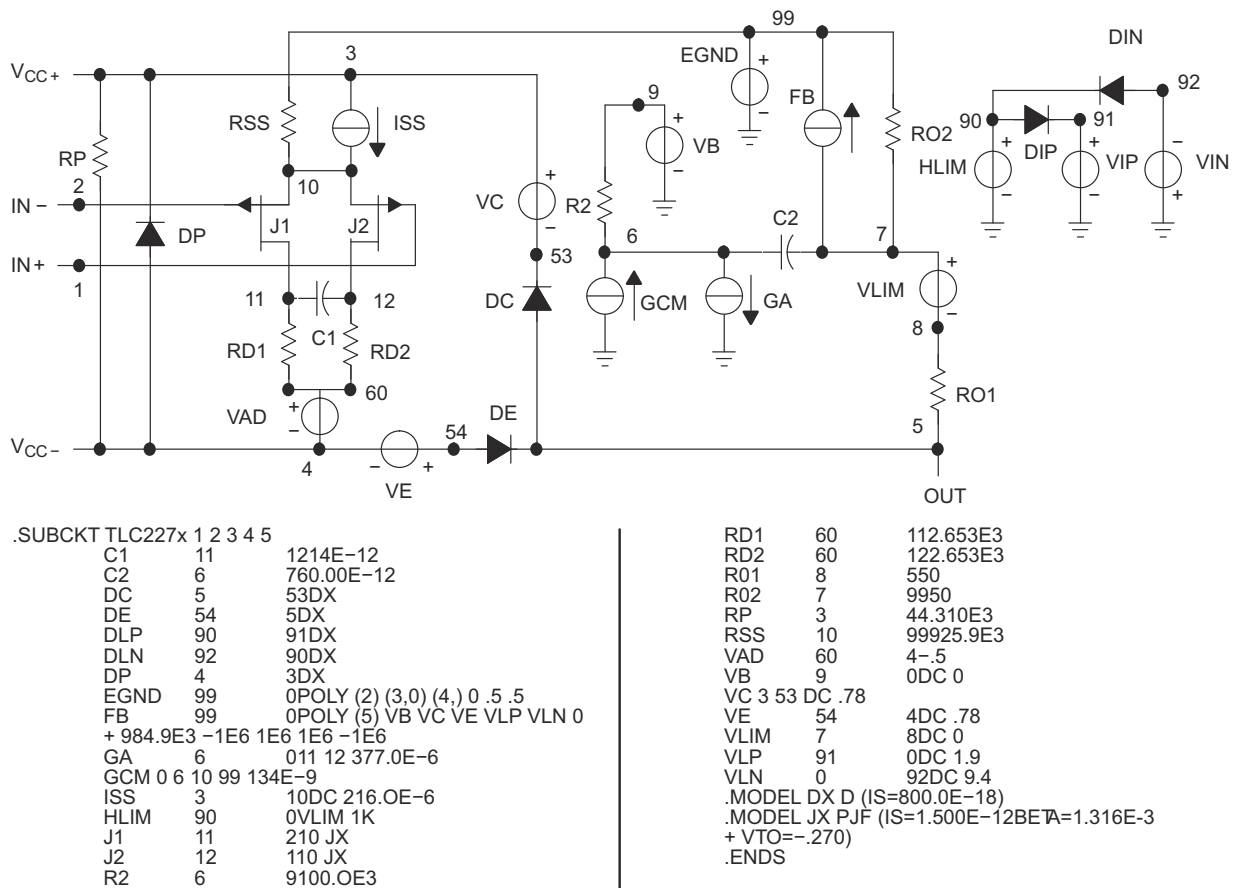
以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 8.1 Application Information

#### 8.1.1 Macromodel Information

Macromodel information provided was derived using MicroSim Parts, the model generation software used with PSpice®. The Boyle macromodel (see also [セクション 9.2.1](#)) and subcircuit in [図 8-1](#) were generated using the TLC227x typical electrical and operating characteristics at  $T_A = 25^\circ\text{C}$ . Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit



**図 8-1. Boyle Macromodels and Subcircuit**

## 8.2 Typical Application

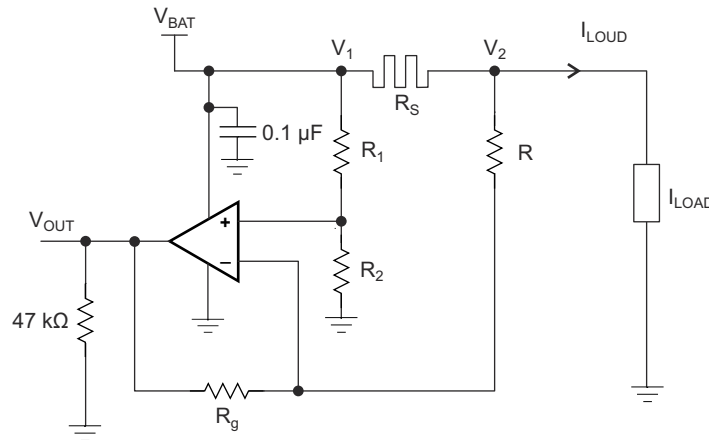


图 8-2. High-Side Current Monitor Equivalent Schematic (Each Amplifier)

### 8.2.1 Design Requirements

For this design example, use these parameters listed in 表 8-1 as the input parameters.

表 8-1. Design Parameters

PARAMETER		VALUE
V <sub>BAT</sub>	Battery voltage	12 V
R <sub>SENSE</sub>	Sense resistor	0.1 Ω
I <sub>LOAD</sub>	Load current	0 A to 10 A
	Operational amplifier	Set in differential configuration with gain = 10

### 8.2.2 Detailed Design Procedure

This circuit is designed for measuring the high-side current in automotive body control modules with a 12-V battery or similar applications. The operational amplifier is set as differential with an external resistor network.

#### 8.2.2.1 Differential Amplifier Equations

式 1 和 式 2 are used to calculate V<sub>OUT</sub>.

$$V_{OUT} = \frac{R_g}{R} \left( \frac{\frac{R}{R_g} - \frac{R_1}{R_2}}{1 + \frac{R_1}{R_2}} \times \frac{V_1 + V_2}{2} + \frac{1 + \frac{1}{2} \left( \frac{R_1}{R_2} + \frac{R}{R_g} \right)}{1 + \frac{R_1}{R_2}} (V_1 - V_2) \right) \quad (1)$$

$$V_{OUT} = \frac{R_g}{R} \left( \frac{\frac{R}{R_g} - \frac{R_1}{R_2}}{1 + \frac{R_1}{R_2}} \times V_{BAT} + \frac{1 + \frac{1}{2} \left( \frac{R_1}{R_2} + \frac{R}{R_g} \right)}{1 + \frac{R_1}{R_2}} \times R_S \times I_{LOAD} \right) \quad (2)$$

In an ideal case, 式 3 then calculates R<sub>1</sub> = R and R<sub>2</sub> = R<sub>g</sub>, and V<sub>OUT</sub>:

$$V_{OUT} = \frac{R_g}{R} \times R_S \times I_{LOAD} \quad (3)$$



However, the resistors have tolerances; therefore, the resistors cannot be perfectly matched.

$$R_1 = R \pm \Delta R_1$$

$$R_2 = R_2 \pm \Delta R_2$$

$$R = R \pm \Delta R$$

$$R_g = R_g \pm \Delta R_g$$

$$\text{Tol} = \frac{\Delta R}{R} \tag{4}$$

式 5 shows that by developing the equations and neglecting the second order, the worst case is when the tolerances add up:

$$V_{\text{OUT}} = \pm (4 \text{ Tol}) \frac{R_g}{R + R_g} \times V_{\text{BAT}} + \left( 1 \pm 2 \text{ Tol} \left( 1 + \frac{2R}{R + R_g} \right) \right) \frac{R_g}{R} \times R_S \times I_{\text{LOAD}} \tag{5}$$

where

- Tol = 0.01 for 1%
- Tol = 0.001 for 0.1%

If the resistors are perfectly matched, then Tol = 0 and 式 6 calculates  $V_{\text{OUT}}$ :

$$V_{\text{OUT}} = \frac{R_g}{R} \times R_S \times I_{\text{LOAD}} \tag{6}$$

The highest error is from the common mode:

$$4 (\text{Tol}) \frac{R_g}{R + R_g} \times V_{\text{BAT}} \tag{7}$$

Gain of 10,  $R_g / R = 10$ , and Tol = 1%:

$$\text{Common mode error} = ((4 \times 0.01) / 1.1) \times 12 \text{ V} = 0.436 \text{ V}$$

Gain of 10 and Tol = 0.1%:

$$\text{Common mode error} = 43.6 \text{ mV}$$

The resistors were chosen from 2% batches.

$R_1$  and R 12 k $\Omega$

$R_2$  and  $R_g$  120 k $\Omega$

$$\text{Ideal Gain} = 120 / 12 = 10$$

The measured value of the resistors:

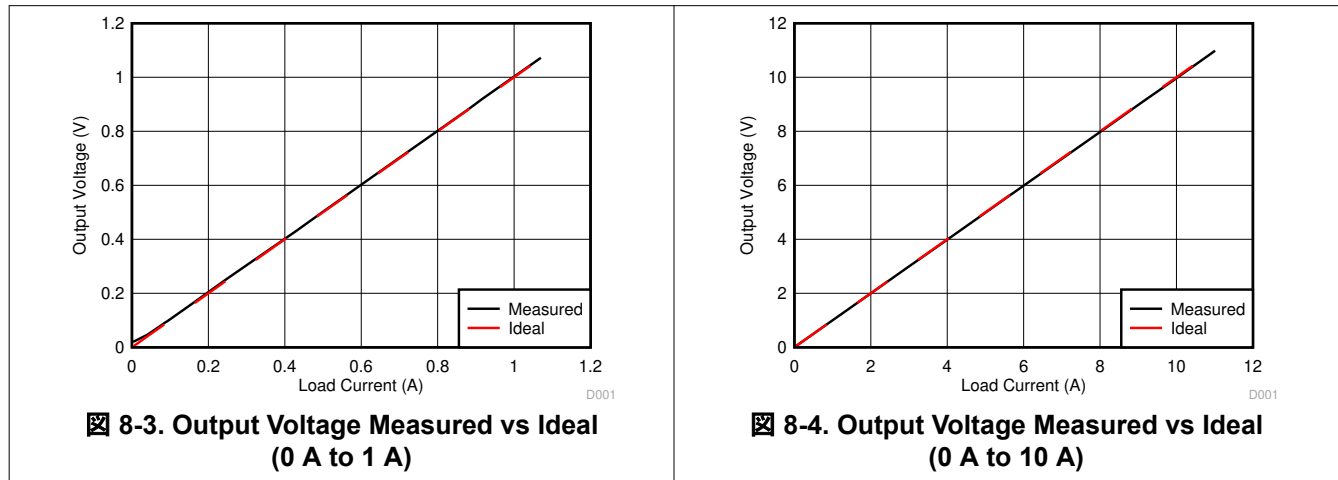
$$R_1 = 11.835 \text{ k}\Omega$$

$$R = 11.85 \text{ k}\Omega$$

$$R_2 = 117.92 \text{ k}\Omega$$

$$R_g = 118.07 \text{ k}\Omega$$

### 8.2.3 Application Curves



### 8.3 Power Supply Recommendations

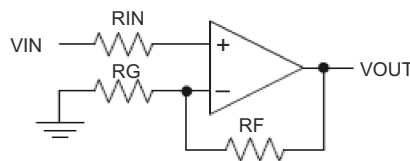
Supply voltage is 4.4 V to 16 V for single supply and  $\pm 2.2$  V to  $\pm 8$  V for dual. In the high-side sensing application, the supply is connected to a 12-V battery.

### 8.4 Layout

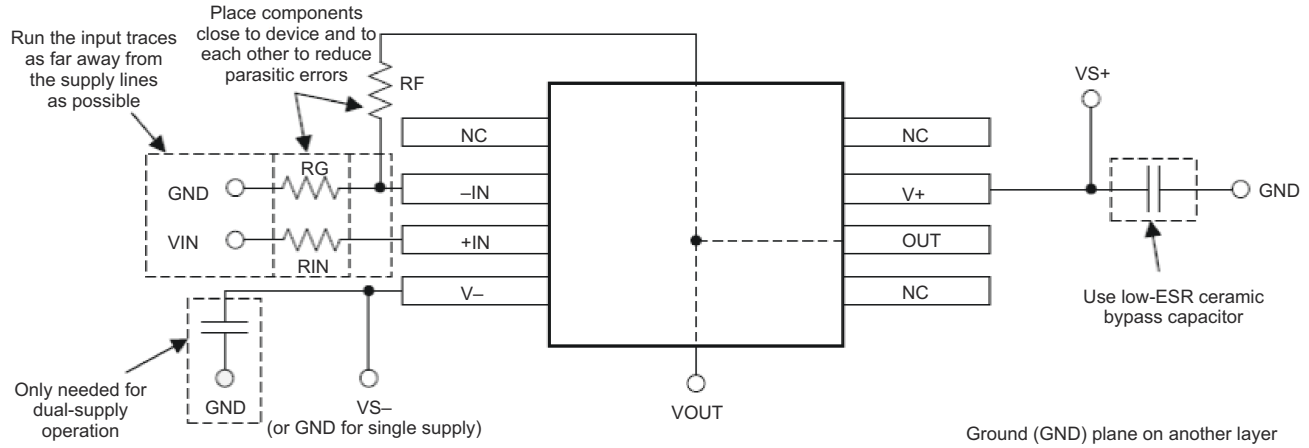
#### 8.4.1 Layout Guidelines

The TLC227x-Q1 is a wideband amplifier. To realize the full operational performance of the device, good high frequency printed-circuit-board (PCB) layout practices are required. Low-loss 0.1- $\mu$ F bypass capacitors must be connected between each supply pin and ground as close to the device as possible. The bypass capacitor traces must be designed for minimum inductance.

#### 8.4.2 Layout Example



**Figure 8-5. Schematic Representation**



 **8-6. Operational Amplifier Board Layout for Noninverting Configuration**

## 9 Device and Documentation Support

### 9.1 Device Support

#### 9.1.1 Development Support

##### 9.1.1.1 PSpice® for TI

PSpice® for TI は、アナログ回路の性能評価に役立つ設計およびシミュレーション環境です。レイアウトと製造に移る前に、サブシステムの設計とプロトタイプ・ソリューションを作成することで、開発コストを削減し、市場投入までの期間を短縮できます。

##### 9.1.1.2 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a [free download](#) from the [Design tools and simulation](#) web page, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

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#### 注

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the [TINA-TI™ software folder](#).

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## 9.2 Documentation Support

### 9.2.1 Related Documentation

For related documentation see the following:

- G.R. Boyle, D.O. Pederson, B.M. Cohn, J.E. Solomon (Dec. 1974). *Macromodeling of Integrated Circuit Operational Amplifiers*. IEEE Journal of Solid-State Circuits, Volume 9, Issue 6, pages 353–364. Retrieved from <https://ieeexplore.ieee.org/document/1050528>

### 9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.4 サポート・リソース

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## 9.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC2272AQDRG4Q1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272AQ	<a href="#">Samples</a>
TLC2272AQDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272AQ	<a href="#">Samples</a>
TLC2272AQPWRG4Q1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272AQ	<a href="#">Samples</a>
TLC2272AQPWRQ1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272AQ	<a href="#">Samples</a>
TLC2272QDRG4Q1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272Q1	<a href="#">Samples</a>
TLC2272QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272Q1	<a href="#">Samples</a>
TLC2272QPWRG4Q1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272Q1	<a href="#">Samples</a>
TLC2272QPWRQ1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272Q1	<a href="#">Samples</a>
TLC2274AQDRG4Q1	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2274AQ1	<a href="#">Samples</a>
TLC2274AQDRQ1	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2274AQ1	<a href="#">Samples</a>
TLC2274AQPWRG4Q1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2274AQ1	<a href="#">Samples</a>
TLC2274AQPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2274AQ1	<a href="#">Samples</a>
TLC2274QDRG4Q1	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 125	2274Q1	
TLC2274QDRQ1	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 125	2274Q1	
TLC2274QPWRG4Q1	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 125	2274Q1	
TLC2274QPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2274Q1	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TLC2272-Q1, TLC2272A-Q1, TLC2274-Q1, TLC2274A-Q1 :**

- Catalog : [TLC2272](#), [TLC2272A](#), [TLC2274](#), [TLC2274A](#)
- Enhanced Product : [TLC2272A-EP](#), [TLC2274-EP](#), [TLC2274A-EP](#)
- Military : [TLC2272M](#), [TLC2272AM](#), [TLC2274M](#), [TLC2274AM](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

- Military - QML certified for Military and Defense Applications



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC2272AQPWRG4Q1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC2272AQPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC2272QPWRG4Q1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC2272QPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC2274AQPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC2274AQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC2274QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC2272AQPWRG4Q1	TSSOP	PW	8	2000	356.0	356.0	35.0
TLC2272AQPWRQ1	TSSOP	PW	8	2000	356.0	356.0	35.0
TLC2272QPWRG4Q1	TSSOP	PW	8	2000	356.0	356.0	35.0
TLC2272QPWRQ1	TSSOP	PW	8	2000	356.0	356.0	35.0
TLC2274AQPWRG4Q1	TSSOP	PW	14	2000	356.0	356.0	35.0
TLC2274AQPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0
TLC2274QPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0



D (R-PDSO-G14)

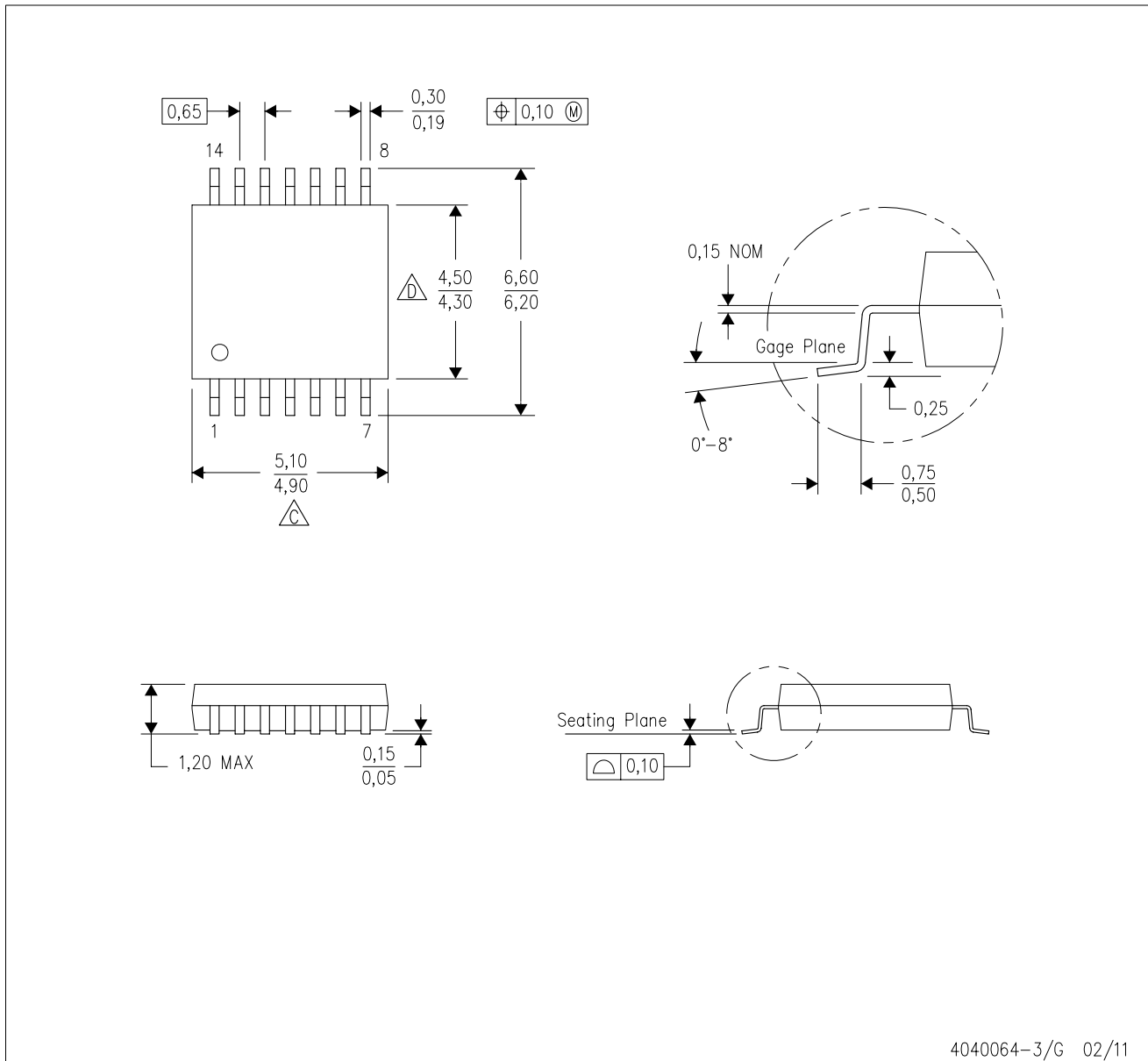
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



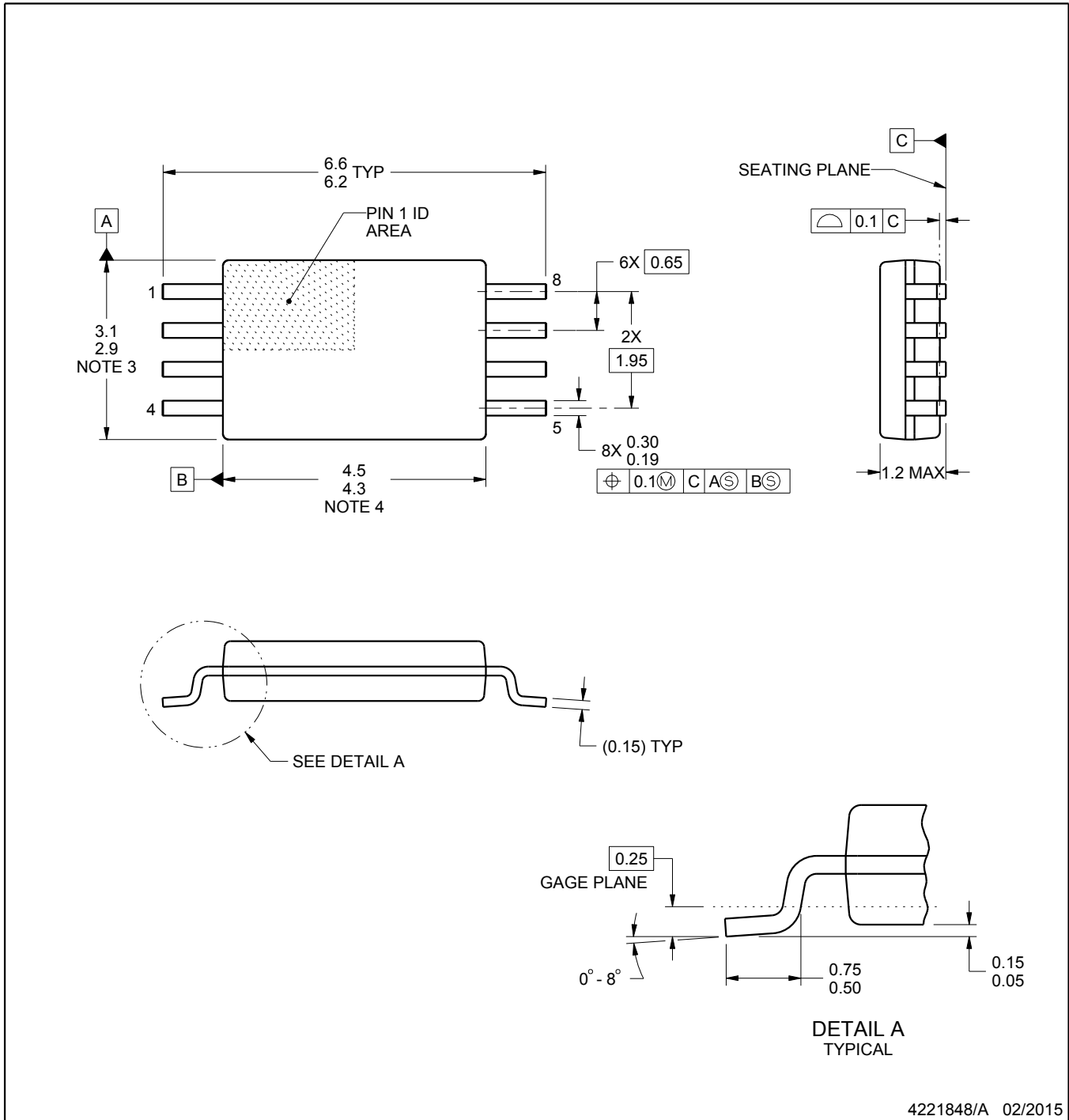
PW0008A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

### NOTES:

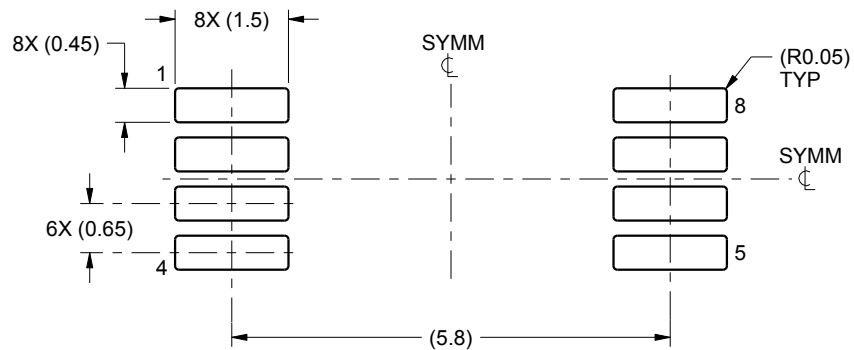
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

# EXAMPLE BOARD LAYOUT

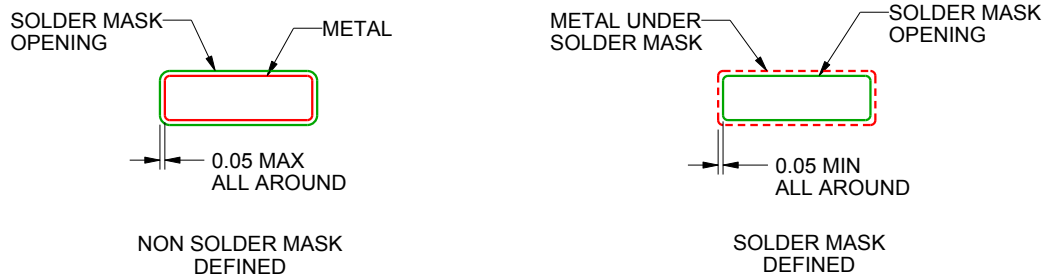
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

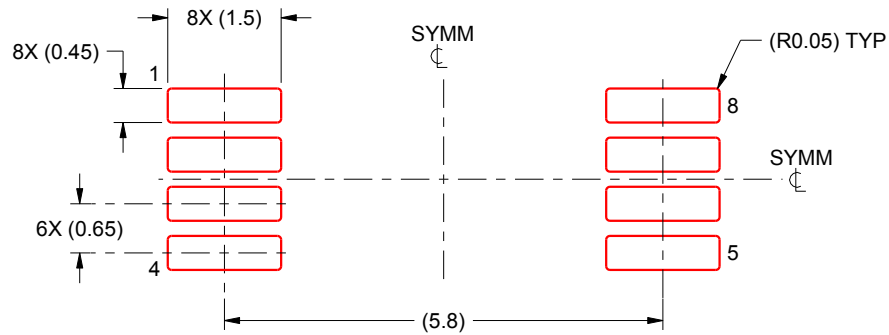
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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