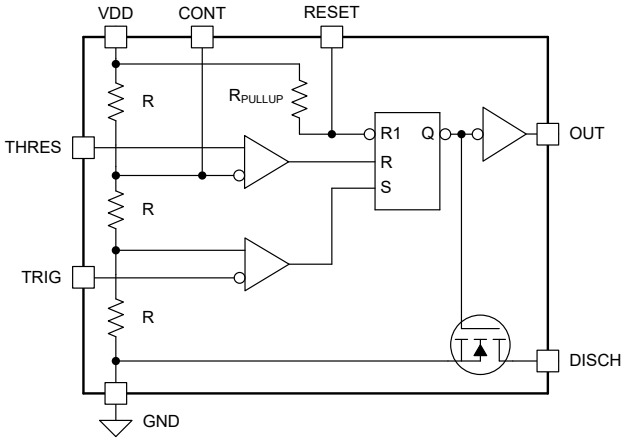
TLC3555-Q1 車載高速 CMOS トランシーバ

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
  - 温度グレード 1:-40℃～+125℃、T_A
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 超低消費電力
  - V_{DD} = 5V で 1mA (標準値)
- 最大 3MHz の非安定動作
- レール ツー レールにスイング可能な CMOS 出力
- 高い出力電流能力
  - 200mA (シンク)
  - 50mA (ソース)
- 出力は CMOS、TTL、MOS と完全互換
- RESET から V_{DD} へのプルアップを内蔵
- 既知の状態へのパワーオン リセット
- サーマル シャットダウン保護内蔵
- 1.5V～18V の単一電源動作

2 アプリケーション

- 車載ライティング
- 自動車向けインストルメント クラスタ
- テレマティクス
- パルス生成
- シーケンシャル タイミング
- 時間遅延の生成
- パルス幅変調
- パルス位置変調
- MOSFET ゲートドライブ



概略回路図

3 概要

TLC3555-Q1 は、テキサス・インスツルメンツの CMOS プロセスを利用して製造されたモノリシック タイミング回路です。このタイマは、CMOS、TTL、MOS ロジックと完全互換であり、3MHz まで、さらにはそれを超える周波数でも動作します。TLC3555-Q1 は、性能と機能の両方の観点から既存の TLC555-Q1 を改良したものであり、より厳格な仕様許容誤差に加え、サーマル シャットダウンやパワーオン リセットなどの追加機能も備えています。

TLC3555-Q1 のトリガ、スレッショルド、リセットのロジックは、TLC555-Q1 と同じ真理値表に従います。リセット ピン (RESET) を High に設定すると標準的な動作になり、リセット ピンを Low に設定すると、フリップ フロップがリセットされて、出力が強制的に Low になります。TLC3555-Q1 は、RESET から VDD への内部プルアップ抵抗を備えているため、受動部品数を減らし、基板面積を削減できます。

伝搬遅延時間が短く、立ち上がりおよび立ち下がり時間が短いため、TLC3555-Q1 は、NE555 や TLC555-Q1 など従来のタイマよりも高い周波数の非安定動作をサポートしています。TLC3555-Q1 は、電源電圧が 15V の場合、テキサス・インスツルメンツの従来型非安定テスト回路で 3.1MHz のクリーンな方形波を実現します。TLC3555-Q1 を発振器として使用し、出力と入力を互いに接続すると、7.2MHz の発振周波数が得られます。高い周波数での応答は、回路の寄生成分が支配的です。TLC555-Q1 とピン互換の D パッケージに加えて、TLC3555-Q1 は DDF パッケージでも供給されるため、寄生成分を低減しながら簡潔な実装が可能です。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
TLC3555-Q1	D (SOIC、8)	4.9mm × 6.0mm
	DDF (SOT-23-THIN、8)(3)	2.9 mm × 2.8mm

(1) 詳細については、セクション 10 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。
(3) 事前情報 (量産データではありません)。

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4 Pin Configuration and Functions

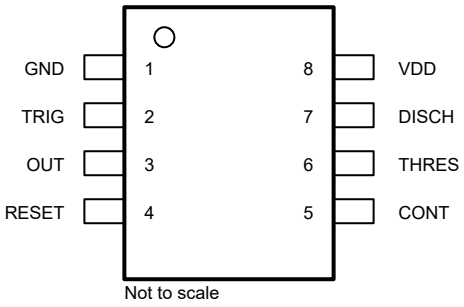


図 4-1. D Package, 8-Pin SOIC, and DDF (Preview) Package, 8-Pin SOT-23-THIN (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
CONT	5	Input/Output	Controls comparator thresholds. Outputs 2/3 V_{DD} by default, or can be driven externally
DISCH	7	Output	Open collector output to discharge timing capacitor
GND	1	Power	Ground reference voltage
OUT	3	Output	Timer output signal
RESET	4	Input	Active low reset input forces output and discharge low
THRES	6	Input	End of timing input. THRES > CONT sets output low and discharge low
TRIG	2	Input	Start of timing input. TRIG < 1/2 CONT sets output high and discharge open
VDD	8	Power	Input supply voltage, 1.5V to 18V

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{DD}	Supply voltage (2)	–0.3	20	V
	Input voltage on TRIG, THRES, CONT, RESET pins	–0.3	V_{DD} + 0.3	V
I_{OL}	Sink current, discharge or output		225	mA
I_{OH}	Source current, output		60	mA
T_A	Operating free-air temperature	–55	125	°C
T_J	Junction temperature	–55	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to network GND.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	1.5		18	V
T_A	Operating free-air temperature	–40		125	°C

5.4 Thermal Information

THERMAL METRICS(1)		TLC3555-Q1		UNIT
		8 PINS		
		D (SOIC)	DDF (SOT-23-THIN)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	138.9	211.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78.8	118.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	87.9	112.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	23.2	15.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	86.9	111.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

at T_A = 25°C and V_{DD} = 5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{I(THRES)}$	Threshold voltage	V_{DD} = 1.5V		0.95	1.0	1.05	V
			–40°C to +125°C	0.8	1.0	1.15	
		V_{DD} = 3.3V		2.1	2.2	2.3	
			–40°C to +125°C	2	2.2	2.4	
		V_{DD} = 5V		3.28	3.33	3.38	
			–40°C to +125°C	3.2	3.33	3.46	
		V_{DD} = 12V		7.92	8	8.08	
			–40°C to +125°C	7.7	8	8.3	
		V_{DD} = 15V		9.9	10	10.1	
			–40°C to +125°C	9.6	10	10.4	
$I_{I(THRES)}$	Threshold current	V_{DD} = 1.5V to 15V			10		pA
			–40°C to +125°C		1000		
$V_{I(TRIG)}$	Trigger voltage	V_{DD} = 1.5V		0.48	0.5	0.52	V
			–40°C to +125°C	0.42	0.5	0.58	
		V_{DD} = 3.3V		1.06	1.1	1.14	
			–40°C to +125°C	1	1.1	1.2	
		V_{DD} = 5V		1.64	1.67	1.70	
			–40°C to +125°C	1.6	1.67	1.75	
		V_{DD} = 12V		3.95	4	4.05	
			–40°C to +125°C	3.85	4	4.15	
		V_{DD} = 15V		4.94	5	5.06	
			–40°C to +125°C	4.8	5	5.2	
$I_{I(TRIG)}$	Trigger current	V_{DD} = 1.5V to 15V			10		pA
			–40°C to +125°C		1000		
$V_{I(RESET)}$	Reset voltage	V_{DD} = 1.5V		0.35	0.6	0.8	V
			–40°C to +125°C	0.3	0.6	1	
		V_{DD} = 3.3V		0.5	0.77	1.05	
			–40°C to +125°C	0.4	0.77	1.2	
		V_{DD} = 5V		0.65	0.86	1.3	
			–40°C to +125°C	0.5	0.86	1.4	
		V_{DD} = 12V		0.67	0.89	1.3	
			–40°C to +125°C	0.5	0.89	1.4	
		V_{DD} = 15V		0.67	0.89	1.3	
			–40°C to +125°C	0.5	0.89	1.4	
$I_{I(RESET)}$	Reset current	V_{DD} = 1.5V to 15V, RESET = V_{DD}			10		pA
			–40°C to +125°C		1000		
		V_{DD} = 1.5V, RESET = 0V			1.8		µA
			–40°C to +125°C		1.9		
		V_{DD} = 3.3V, RESET = 0V			3.9		
			–40°C to +125°C		4		
		V_{DD} = 5V, RESET = 0V			5.9		
			–40°C to +125°C		6		
		V_{DD} = 12V, RESET = 0V			14.2		
			–40°C to +125°C		14.4		
		V_{DD} = 15V, RESET = 0V			17.8		
			–40°C to +125°C		18		
$V_{I(CONT)}$	Control voltage	Open circuit, expressed as a percentage of supply voltage			66.7		%

5.5 Electrical Characteristics (続き)

at T_A = 25°C and V_{DD} = 5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Discharge switch on-stage voltage	I_{OL} = 1mA, V_{DD} = 1.5V to 15V			0.025	0.2	V
			–40°C to +125°C		0.03	0.25	
		I_{OL} = 10mA, V_{DD} = 3.3V to 15V			0.08	0.3	
			–40°C to +125°C		0.28	0.35	
		I_{OL} = 100mA, V_{DD} = 5V to 15V			0.82	1.5	
			–40°C to +125°C		1.3	1.7	
	Discharge switch off-stage current	V_{DD} = 1.5V to 15V			0.01		nA
			–40°C to +125°C (3)		70		
V_{OH}	High-level output voltage	I_{OH} = –1mA, V_{DD} = 1.5V		1.05	1.29		V
			–40°C to +125°C	1.05	1.25		
		I_{OH} = –1mA, V_{DD} = 3.3V		2.9	3.25		
			–40°C to +125°C	2.9	3.1		
		I_{OH} = –1mA, V_{DD} = 5V		4.67	4.91		
			–40°C to +125°C	4.6	4.88		
		I_{OH} = –10mA, V_{DD} = 5V		4.2	4.58		
			–40°C to +125°C	4.09	4.35		
		I_{OH} = –10mA, V_{DD} = 12V		11.2	11.54		
			–40°C to +125°C	11	11.4		
		I_{OH} = –10mA, V_{DD} = 15V		14.2	14.54		
			–40°C to +125°C	14	14.2		
		I_{OH} = –50mA, V_{DD} = 15V		10.5	11.5		
			–40°C to +125°C (4)		9		
V_{OL}	Low-level output voltage	I_{OL} = 1mA, 1.5V			0.1	0.25	V
			–40°C to +125°C		0.2	0.35	
		I_{OL} = 1mA, 3.3V			0.09	0.25	
			–40°C to +125°C		0.2	0.35	
		I_{OL} = 1mA, V_{DD} = 5V to 15V			0.08	0.2	
			–40°C to +125°C		0.2	0.35	
		I_{OL} = 10mA, V_{DD} = 3.3V			0.25	0.3	
			–40°C to +125°C		0.3	0.4	
		I_{OL} = 10mA, V_{DD} = 5V to 15V			0.17	0.3	
			–40°C to +125°C		0.25	0.4	
		I_{OL} = 100mA, V_{DD} = 5V to 15V (4)			2.11	2.8	
			–40°C to +125°C		2.5	3.2	
		I_{OL} = 200mA, V_{DD} = 15V (4)			5	6	
			–40°C to +125°C		7		
C_I	Trigger, threshold capacitance (each pin)				2.1		pF
C_{PD}	Power dissipation capacitance (1) (2)				50		pF

5.5 Electrical Characteristics (続き)

at T_A = 25°C and V_{DD} = 5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_Q	Quiescent current	V_{DD} = 1.5V			150	200	μA
			–40°C to +125°C		180	285	
		V_{DD} = 3.3V			180	250	
			–40°C to +125°C		210	330	
		V_{DD} = 5V			200	270	
			–40°C to +125°C		240	365	
		V_{DD} = 12V			240	310	
			–40°C to +125°C		290	425	
		V_{DD} = 15V			260	330	
			–40°C to +125°C		310	465	

(1) C_{PD} is used to determine the dynamic power consumption.
(2) $P_D = V_{DD}^2 f_o(C_{PD} + C_L)$ where f_o = output frequency, C_L = output load capacitance, V_{DD} = supply voltage.
(3) Leakage increases with temperature, approximately doubling in magnitude with each 10°C rise in temperature. Value specified for Full Range is measured at T_A = 125°C.
(4) Sustained operation at this output current results in self-heating that can cause the device to go into protective thermal shutdown, depending on the supply voltage and ambient temperature. Limit operation at high output current to only short durations, such as transient events.

5.6 Switching Characteristics

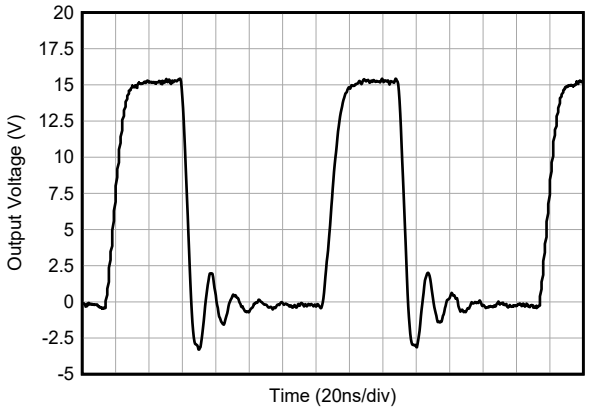
at T_A = 25°C and V_{DD} = 5V (unless otherwise noted); characteristic values are specified by design, characterization, or both

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Temperature sensitivity of timing internal	T_A = –40°C to +125°C, C_T = 0.1μF, R_A = R_B = 1kΩ to 100kΩ (2)			75		ppm/°C
	Supply voltage sensitivity of timing interval	V+ = 3.3V to 15V, C_T = 0.1μF, R_A = R_B = 1kΩ to 100kΩ			0.17		%/V
t_r	Output pulse rise time	R_L = 10MΩ, C_L = 10pF			7.8		ns
t_f	Output pulse fall time	R_L = 10MΩ, C_L = 10pF			4.7		ns
f_{max}	Maximum frequency, astable mode (1)	R_A = 470Ω, R_B = 200Ω, C_T = 200pF		2.6	3		MHz
			V_{DD} = 15V		3.1		
		Free-running oscillator, THRES = TRIG = OUT			7.2		
t_{PD}	Trigger propagation delay	Rising	V_{DD} = 3.3V		85		ns
			V_{DD} = 5V		75		
			V_{DD} = 15V		60		
		Falling	V_{DD} = 3.3V		70		
			V_{DD} = 5V		50		
			V_{DD} = 15V		50		

(1) This measurement is significantly impacted by board parasitics.
(2) Calculated as $(f_{125°C} – f_{–40°C}) / (\Delta T_A \times f_{25°C}) \times 10^6$ where f_T = output frequency at temperature T, and T_A = –40°C to +125°C.

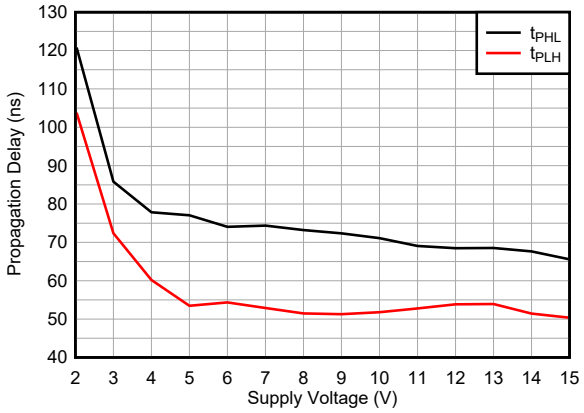
5.7 Typical Characteristics

at T_A = 25°C and V_{DD} = 5V (unless otherwise noted)



TRIG, THRES, and OUT shorted together in this test, such that f_{max} ≅ 7.2MHz

図 5-1. Output Voltage vs Time as Free-Running Oscillator



TRIG and THRES shorted together in this test; take effects of load resistance on t_{PH} and t_{PL} into account separately

図 5-2. Propagation Delay to Discharge Output vs Supply Voltage

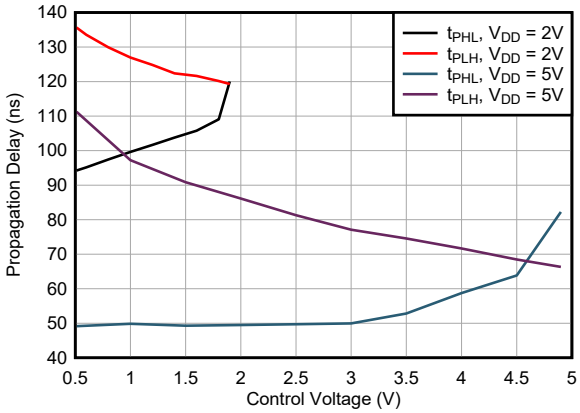


図 5-3. Propagation Delay vs Control Voltage

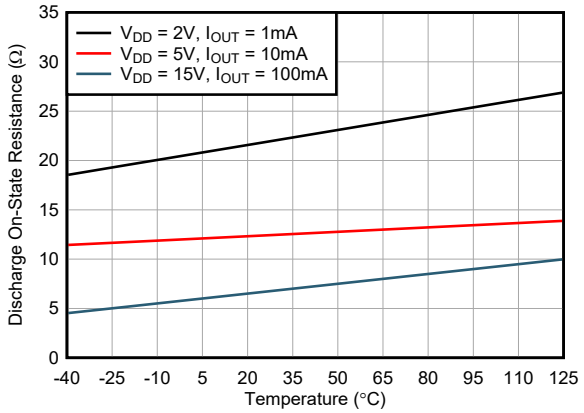


図 5-4. Discharge Switch On-State Resistance vs Ambient Temperature

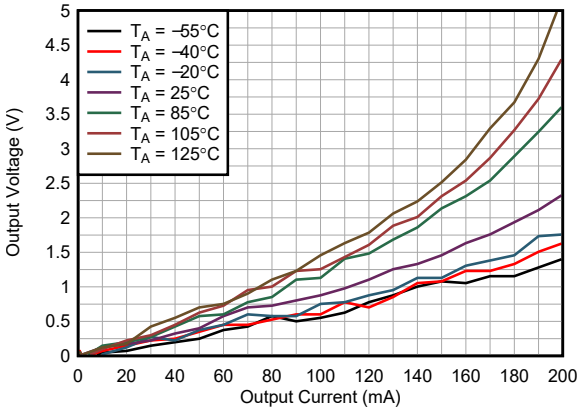
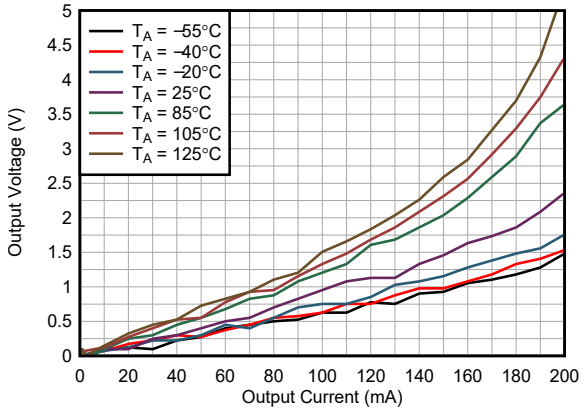


図 5-5. Output Voltage vs Output Current, Sinking



V_{DD} = 15V

図 5-6. Output Voltage vs Output Current, Sinking

5.7 Typical Characteristics (continued)

at T_A = 25°C and V_{DD} = 5V (unless otherwise noted)

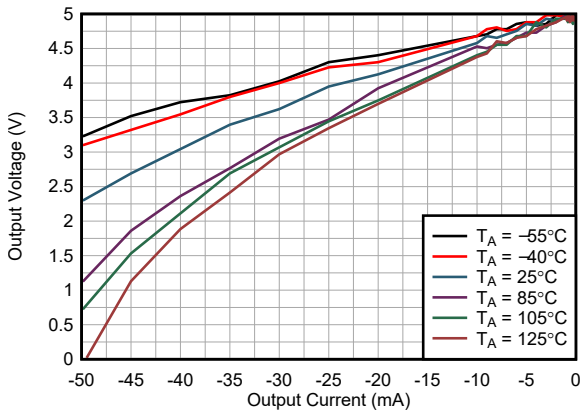
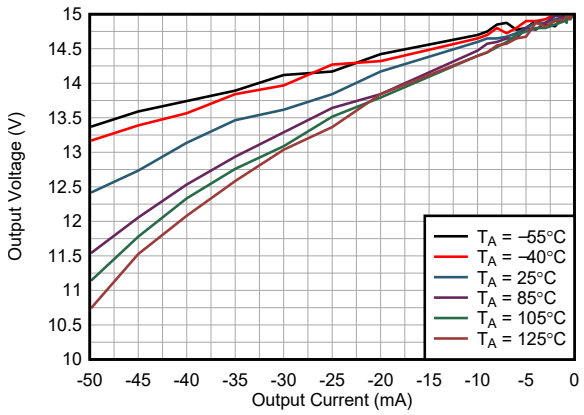


図 5-7. Output Voltage vs Output Current, Sourcing



V_{DD} = 15V

図 5-8. Output Voltage vs Output Current, Sourcing

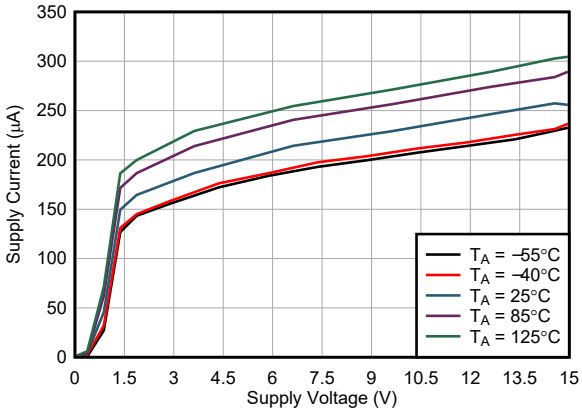


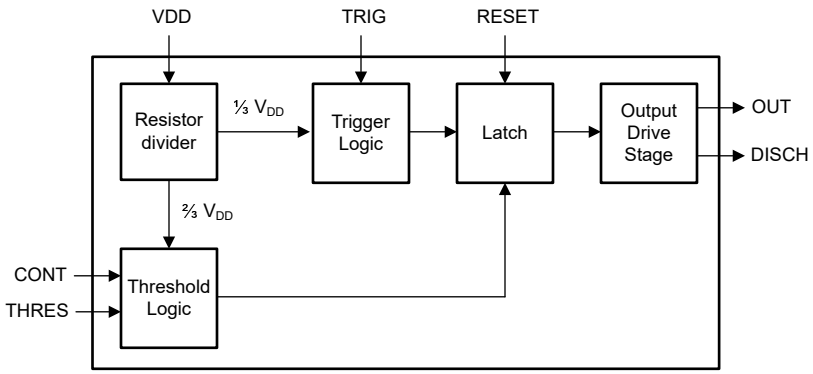
図 5-9. Supply Current vs Supply Voltage

6 Detailed Description

6.1 Overview

The TLC3555-Q1 next-generation timer is useful for both general-purpose and precise timing applications, with astable mode periods from 325ns to hours, and frequencies to 3MHz or even beyond. In nearly all cases, the tolerances of the passive components used to implement the application circuit contribute more error than the TLC3555-Q1 tolerance. The improved precision of the TLC3555-Q1 as compared to previous-generation timers provides a performance benefit to the trigger and threshold tolerances when using the same grade of passive components, or can enable similar end tolerances while using lower-grade passives for a cost benefit.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Monostable Operation

For monostable operation, connect the TLC3555-Q1 as in 図 6-1. If the output is low, application of a negative-going pulse to the trigger (TRIG) sets the internal flip-flop, drives the output high, and turns off DISCH. Capacitor C_T charges through R_A until the voltage across the capacitor reaches the threshold voltage of the threshold (THRES) input. If TRIG returns to a high level, the output of the threshold comparator resets the flip-flop, drives the output low, and discharges C_T through DISCH.

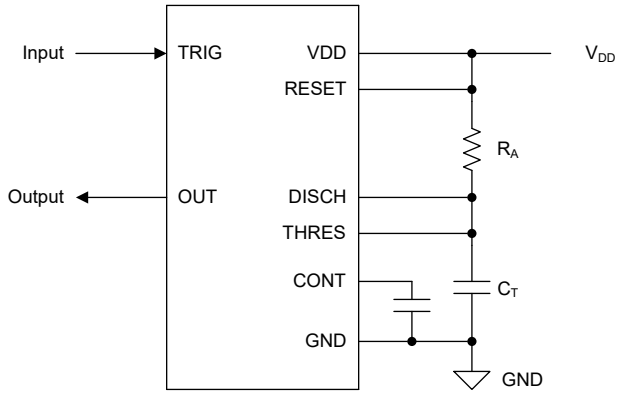
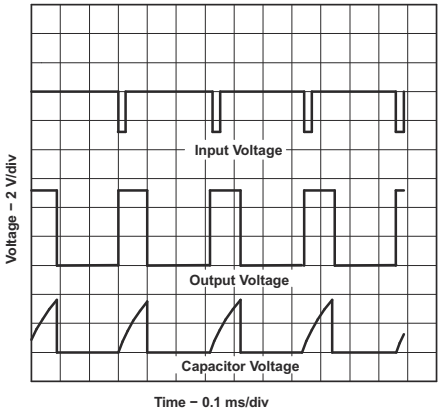


図 6-1. Circuit for Monostable Operation

Monostable operation initiates when the TRIG voltage is less than the trigger threshold. After initialization, the sequence ends only if TRIG is high for at least 500ns before the end of the timing interval. When the trigger is grounded, the comparator storage time can be as long as 500ns, which limits the minimum monostable pulse width to 500ns. As a result of the threshold level and saturation voltage of the discharge transistor, the output pulse duration is approximately $t_w = 1.1 \times R_A \times C_T$. 図 6-3 is a plot of the nominal pulse width for various values of R_A and C_T. The threshold levels and charge rates are directly proportional to the supply voltage (V_{DD}). As a

result, the timing interval is independent of the supply voltage if the supply voltage is constant during the time interval.

Apply a negative-going trigger pulse simultaneously to RESET and TRIG during the timing interval to discharge C_T and reinitiate the cycle, commencing on the positive edge of the reset pulse. The output is held low for as long as the reset pulse is low.



R_A = 9.1kΩ C_T = 0.01µF

図 6-2. Typical Monostable Waveforms

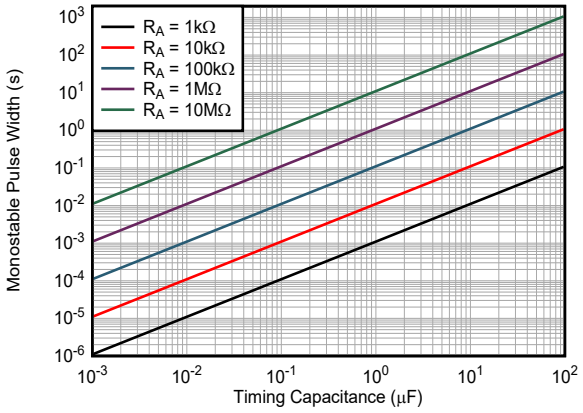


図 6-3. Simulated Output Pulse Width vs Capacitance

6.3.2 Astable Operation

図 6-4 shows that adding a second resistor (R_B) to the circuit and connecting the trigger input to the threshold input causes the timer to self-trigger and run as a multivibrator. The C_T capacitor charges through R_A and R_B and then only discharges through R_B. As a result, the values of R_A and R_B control the duty cycle. D_B is optional and typically used only when a duty cycle below 50% is required, as the diode bypasses R_B to allow faster charging of C_T.

This astable connection results in the C_T capacitor charging and discharging between the threshold-voltage level (≅ 0.67 × V_{DD}) and the trigger-voltage level (≅ 0.33 × V_{DD}). Driving the CONT pin externally shifts the threshold-voltage and trigger-voltage levels to V_{CONT} and 0.5 × V_{CONT}, respectively. As in the monostable circuit, charge and discharge times (and as a result, the frequency and duty cycle) are independent of the supply voltage.

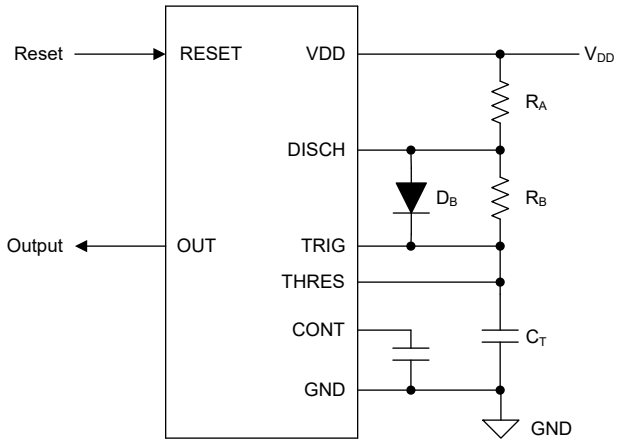
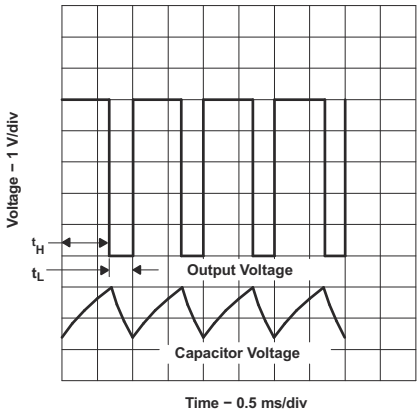


図 6-4. Circuit for Astable Operation



R_A = 5kΩ R_B = 3kΩ C_T = 0.15µF

図 6-5. Typical Astable Waveforms

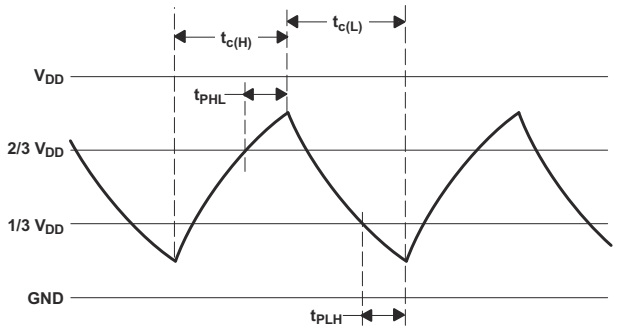


図 6-6. Trigger and Threshold Voltage Waveform

図 6-6 shows typical waveforms generated during astable operation. The output high-level duration (t_H) and low-level duration t_L can be calculated as follows:

$$t_H = 0.693 \times (R_A + R_B) \times C_T \quad (1)$$

$$t_L = 0.693 \times R_B \times C_T \quad (2)$$

Other useful relationships for period, frequency, and driver-referred and waveform-referred duty cycle are shown as follows:

$$T = t_H + t_L = 0.693 \times (R_A + 2R_B) \times C_T \quad (3)$$

$$f = \frac{1}{T} \cong \frac{1.44}{(R_A + 2R_B) \times C_T} \quad (4)$$

$$\text{Output driver duty cycle} = \frac{t_L}{T} = \frac{R_B}{R_A + 2R_B} \quad (5)$$

$$\text{Output waveform duty cycle} = \frac{t_H}{T} = 1 - \frac{R_B}{R_A + 2R_B} = \frac{R_A + R_B}{R_A + 2R_B} \quad (6)$$

These equations do not account for any propagation delay times from the TRIG and THRES inputs to DISCH output. These delay times add directly to the period and overcharge the capacitor, creating differences between calculated and actual values that increase with frequency. In addition, the discharge on-state resistance r_{on} during the discharge event contributes another source of timing error in the calculation when R_B is very low. The following equations provide better agreement with measured values. 式 7 and 式 8 represent the actual low and high times when used at higher frequencies (at 100kHz and beyond) because propagation delay and discharge on resistance is added to the formulas. The value of C_T includes both the nominal or deliberate timing capacitance, as well as parasitic capacitance on the PCB. Decoupling capacitance on CONT also affects the duty cycle, with an error contribution that depends on the capacitor leakage resistance. For additional discussion, see the *Design low-duty-cycle timer circuits* article.

$$t_{c(H)} = C_T \times (R_A + R_B) \times \ln\left(3 - e^{\left(\frac{-t_{PD\ rising}}{C_T \times (R_B + r_{on})}\right)}\right) + t_{PD\ falling} \quad (7)$$

$$t_{c(L)} = C_T \times (R_B + r_{on}) \times \ln\left(3 - e^{\left(\frac{-t_{PD\ falling}}{C_T \times (R_A + R_B)}\right)}\right) + t_{PD\ rising} \quad (8)$$

These equations and those given earlier are similar in that a time constant is multiplied by the logarithm of a number or function. The limit values of the logarithmic terms must be between ln(2) at low frequencies, and ln(3) at extremely high frequencies. For a duty cycle close to 50%, an appropriate constant for the logarithmic terms can be substituted with good results. Output waveform duty cycles less than 50% require that $t_{c(H)}$ / $t_{c(L)}$ < 1 and possibly that $R_A \leq r_{on}$. These conditions can be difficult to obtain. D_B can be used to reduce the effective R_B during the capacitor charging event, but has a nonlinear response. If using D_B, verify performance through simulation and bench evaluation before selecting final timing component values.

図 6-7 and 図 6-8 show the nominal free-running frequency associated with various combinations of C_T and R_A + 2 × R_B for a 66% duty cycle (such that R_A = R_B). The values of r_{on}, $t_{PD\ falling}$ and $t_{PD\ rising}$ vary according to the device supply voltage and temperature. Tolerances of R_A, R_B, and C_T also contribute variation. The difference of simulation results calculated using the simplified and detailed equations becomes apparent by 100kHz, with approximately 2.15% error at V_{DD} = 15V and 2.6% error at V_{DD} = 5V. This error manifests as nonlinearity in the following curves. For applications where sub-1% error is required, use 式 7 and 式 8 for frequencies greater than 10kHz at V_{DD} = 5V, or greater than 30kHz at V_{DD} = 15V.

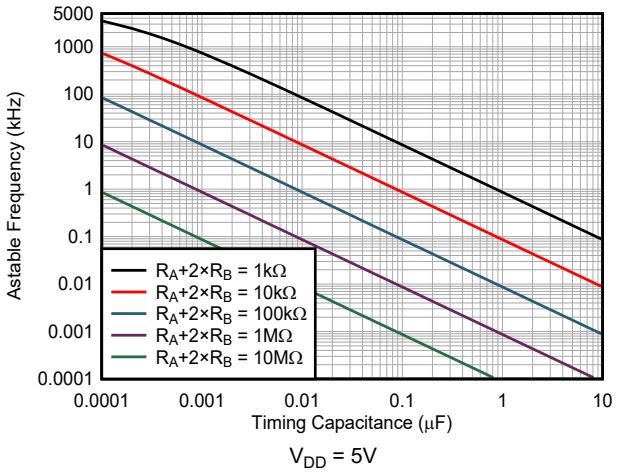


図 6-7. Simulated Astable Frequency

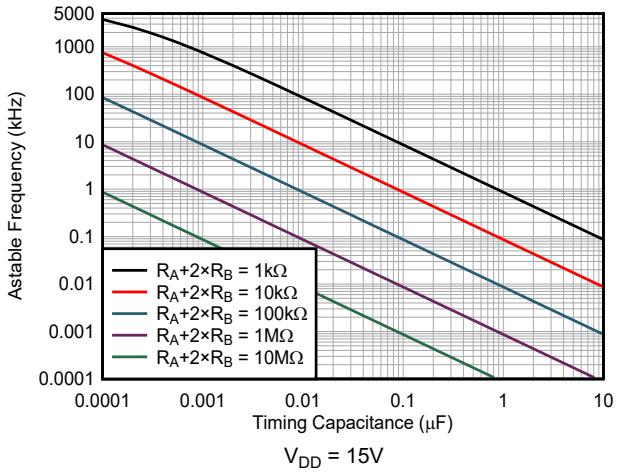


図 6-8. Simulated Astable Frequency

6.3.3 Power-on Reset

The TLC3555-Q1 includes a power-on reset feature, which holds the output high-impedance until the power-up is complete and the output flip-flop state machine has achieved a valid state. Previous generations of 555 timers lacked this feature, meaning the output state as the power supply ramped was unpredictable. The power-on reset of the TLC3555-Q1 asserts to hold the output in a high-impedance (Hi-Z) state during the ramp event. After the supply voltage has reached the minimum threshold, the power-on reset is released, and the state machine and logic table described in 表 6-1 apply. The RESET pin of the TLC3555-Q1 includes a weak pullup resistance to V_{DD}, so if the RESET pin is not driven externally, the device exits the reset state after the power-on reset event is complete. The device then enters whatever state is dictated by the values of THRES, TRIG, and CONT.

6.3.4 Thermal Shutdown

The TLC3555-Q1 is capable of sourcing and sinking more current than previous CMOS-based 555 timers, such as the TLC555-Q1. To help protect the device from overstress due to self-heating, the TLC3555-Q1 includes a thermal shutdown feature. If the junction temperature rises beyond the shutdown limit, a thermal event is asserted and the output enters a high-impedance state, similar to a power-on reset. The device exits the shutdown state after the junction temperature has sufficiently reduced.

In the event of a very fast, extremely high-current transient, the die temperature can rise too quickly for the thermal shutdown feature to activate in time. If a load at the output is capable of pulling more current than the absolute maximum current rating of the device output, use a resistor in series with the output to limit the maximum current of the device.

6.4 Device Functional Modes

表 6-1 lists the device functional modes. While the TLC3555-Q1 features a weak internal pullup resistor to V_{DD}, the pullup can be overpowered by coupled noise due to a fast transient signal edge or noisy circuit environment. To improve reliability, use an external pullup resistor to V_{DD} (if using the RESET functionality), or short the RESET pin directly to V_{DD} (if the RESET functionality is not used).

表 6-1. Function Table

RESET	TRIGGER VOLTAGE(1)	THRESHOLD VOLTAGE(1)	OUTPUT	DISCHARGE SWITCH
Low	Irrelevant	Irrelevant	Low	On
High	< 1/3 V_{CC}	Irrelevant	High	Off
High	> 1/3 V_{CC}	> 2/3 V_{CC}	Low	On
High	> 1/3 V_{CC}	< 2/3 V_{CC}	As previously established	

(1) Voltage levels shown are nominal.

7 Application and Implementation

注

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7.1 Application Information

The TLC3555-Q1 timer device uses resistor and capacitor charging delay to provide a programmable time delay or operating frequency. The TLC3555-Q1 can directly drop-in or upgrade most 555 timer applications. The reduced propagation delays and tighter tolerances of the TLC3555-Q1 can lead to slightly discrepant results when directly replacing legacy CMOS timers for high-frequency astable and monostable applications. Assess board-level parasitics before selecting final values for timing components. While the TLC3555-Q1 output sinking current rating is comparable to a bipolar timer, the sourcing limit must be respected and considered when the TLC3555-Q1 is used as a drop-in replacement for a bipolar 555 timer.

The following section presents a simplified discussion of the design process for some unique applications of the TLC3555-Q1.

7.2 Typical Applications

7.2.1 Missing-Pulse Detector

The circuit shown in 図 7-1 can be used to detect a missing pulse or abnormally long spacing between consecutive pulses in a train of pulses. The timing interval of the monostable circuit is triggered continuously by the input pulse train as long as the pulse spacing is less than the timing interval. A longer pulse spacing, missing pulse, or terminated pulse train permits the timing interval to be completed, thereby generating an output pulse, as in 図 7-2.

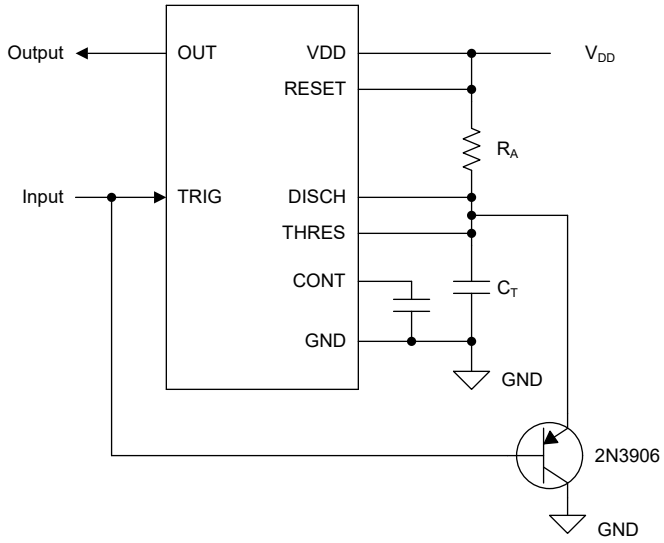

図 7-1. Circuit for Missing-Pulse Detector

7.2.1.1 Design Requirements

Input fault (missing pulses) must be input high. An input stuck low condition cannot be detected because the timing capacitor (C_T) remains discharged.

7.2.1.2 Detailed Design Procedure

Select R_A and C_T so that $R_A \times C_T$ > the maximum normal input high time.

7.2.1.3 Application Curve

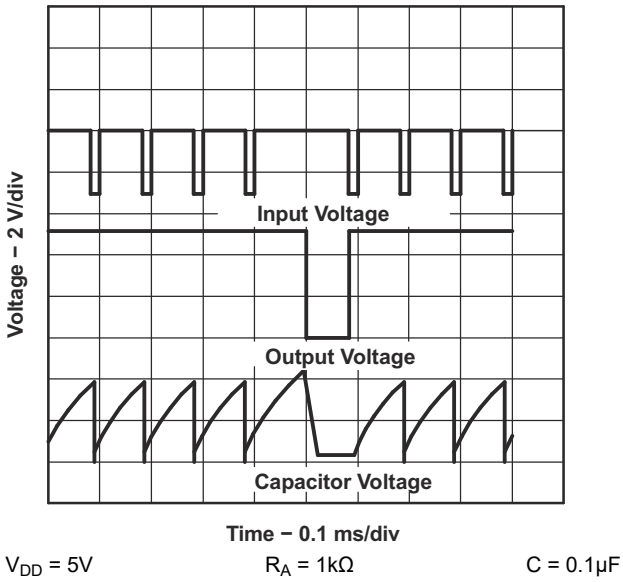

図 7-2. Application Waveform

7.2.2 Pulse-Width Modulation

To modify timer operation, apply an external voltage (or current) to CONT to modulate the internal threshold and trigger voltages. 図 7-3 shows a circuit for pulse-width modulation. A continuous input pulse train triggers the monostable circuit, and a control signal modulates the threshold voltage. 図 7-4 shows the resulting duty cycle versus control voltage transfer function. Attempting to run under 10% duty cycle can result in inconsistent output pulses. Attempting to run close to 100% duty cycle results in frequency division by 2, then 3, then 4.

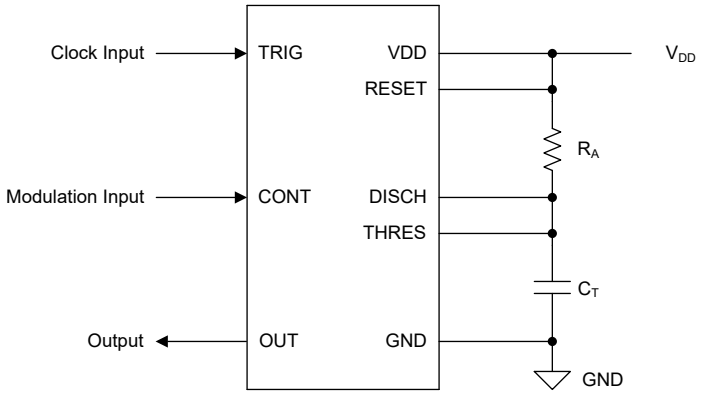

図 7-3. Circuit for Pulse-Width Modulation

7.2.2.1 Design Requirements

The clock input must have V_{OL} and V_{OH} levels that are less than and greater than 1/3 V_{DD}, respectively. Clock input V_{OL} time must be less than minimum output high time; therefore, a high (positive) duty cycle clock is recommended. The minimum recommended modulation voltage is 1V, as a lower CONT voltage can increase threshold comparator propagation delay and storage time. The application must be tolerant of a nonlinear transfer function; the relationship between modulation input and pulse duration is not linear because the capacitor charge is RC-based with an negative exponential curve.

The modulating signal can be directly or capacitively coupled to CONT. For direct coupling, consider the effects of modulation source voltage and impedance on the bias of the timer.

7.2.2.2 Detailed Design Procedure

Select R_A and C_T so that $R_A \times C_T$ is same as or less than the clock input period. 図 7-4 shows the nonlinear relationship between control voltage and output duty cycle. The duty cycle is a function of the control voltage and clock period relative to the $R_A \times C_T$ time constant.

7.2.2.3 Application Curve

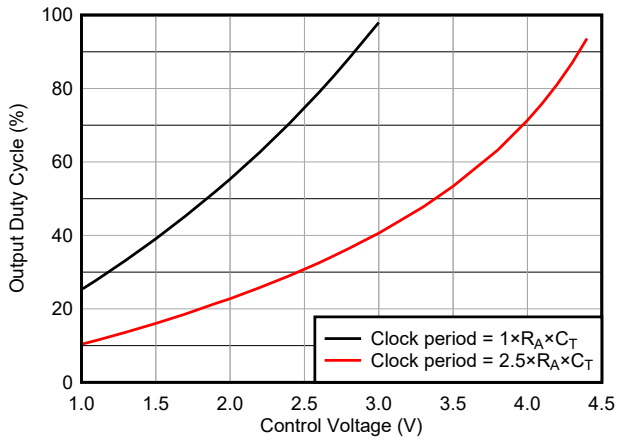

図 7-4. Application Waveform

7.3 Power Supply Recommendations

The TLC3555-Q1 requires a voltage supply from 1.5V to 18V. Adequate power supply bypassing is required to protect associated circuitry. The minimum recommended decoupling capacitance value is 0.1µF, preferably in parallel with a 1µF electrolytic. Place the bypass capacitors as close as possible to the TLC3555-Q1 and minimize the trace length. During a start-up condition, keep the supply ramp below 1V/µs for proper functionality of the power-on reset feature.

7.4 Layout

7.4.1 Layout Guidelines

Standard best practices for PCB layout apply to routing the TLC3555-Q1. A 0.1µF decoupling capacitor, preferably in parallel with a 1µF electrolytic bulk decoupling capacitor, must be placed as close as possible to the TLC3555-Q1 supply pins. The capacitor used for the time delay must be placed as close to the discharge pin as possible. A ground plane on the bottom layer can provide better noise immunity and signal integrity.

For circuits operating at or in excess of 100kHz, parasitic capacitance can significantly impact circuit performance and must be carefully controlled. Increase space between adjacent traces where possible, cut out power and ground planes above and below critical traces, and minimize the use of vias on critical traces. Shorter traces have less capacitance due to capacitance per unit length, so minimize component-to-component trace lengths for the timing resistor (or resistors) and timing capacitor. Simulate, calculate, or manually measure board capacitance before selecting a timing capacitor value because the effective timing capacitance C_T is the sum of the deliberate timing capacitance and parasitic capacitance. Be aware that the timing capacitor value as measured at the frequency of interest can differ from the nominal value; confirm with an LCR meter.

7.4.2 Layout Example

図 7-5 and 図 7-6 show the basic layout for monostable and astable applications. Use C0G (NP0) capacitors to improve stability and repeatability.

- C_T – C0G (NP0) ceramic timing capacitance, based on time delay calculations
- C1 – C0G (NP0) ceramic bypass capacitor for control voltage pin, 0.1µF
- C2 – C0G (NP0) ceramic bypass capacitor for supply pin, 0.1µF
- C3 – electrolytic bypass capacitor for supply pin, 1µF
- R_A – timing resistor, based on time delay calculations
- R_B – timing resistor (astable mode), based on time delay calculations

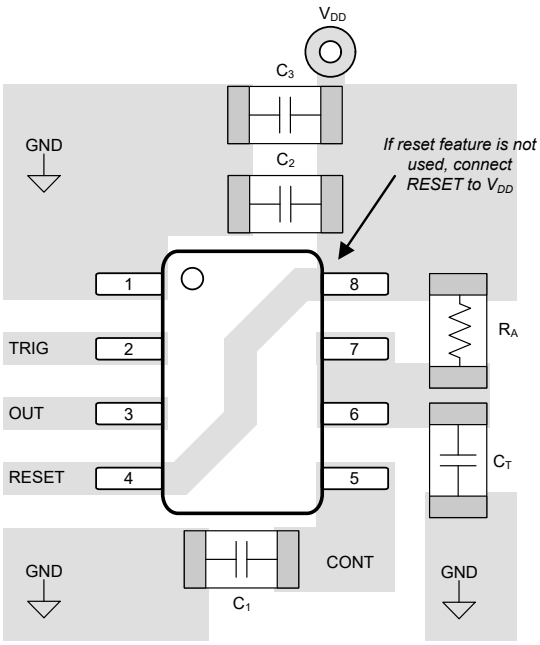

図 7-5. Recommended Layout, Monostable Configuration

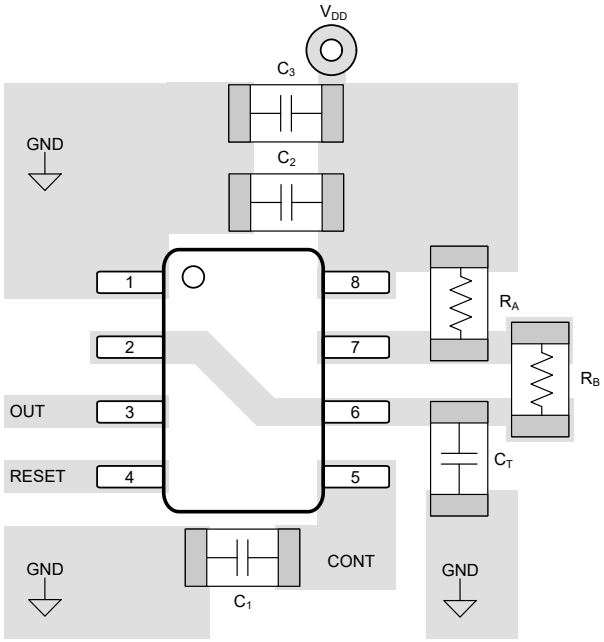

図 7-6. Recommended Layout, Astable Configuration

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TLC3555EVM* evaluation module
- Texas Instruments, *TLC555-Q1 Used as a Positive and Negative Charge Pump* application note
- Texas Instruments, *EMC Compatible Automotive LED Rear Lamp With Sequential-Turn Animation Reference Design*
- Texas Instruments, *Precision PWM Dimming LED Driver Reference Design for Automotive Lighting*

8.2 ドキュメントの更新通知を受け取る方法

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8.3 サポート・リソース

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8.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (July 2024) to Revision A (October 2024)	Page
• DDF パッケージのステータスをプレビューから事前情報 (サンプルありのプレビュー) に変更	1
• Added thermal metrics for DDF package in *Thermal Information*	3
• Added *TLC3555EVM* reference to *Related Documentation*	19

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC3555QDRQ1	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3555Q
TLC3555QDRQ1.A	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3555Q
XTL3555QDDFRQ1	Active	Preproduction	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
XTL3555QDDFRQ1.A	Active	Preproduction	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

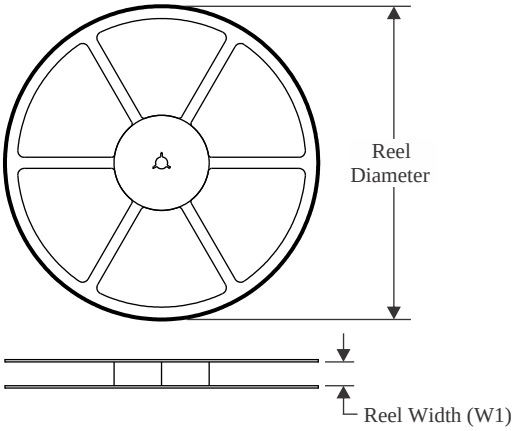
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

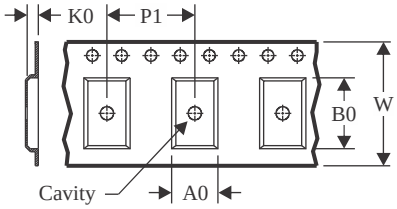
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

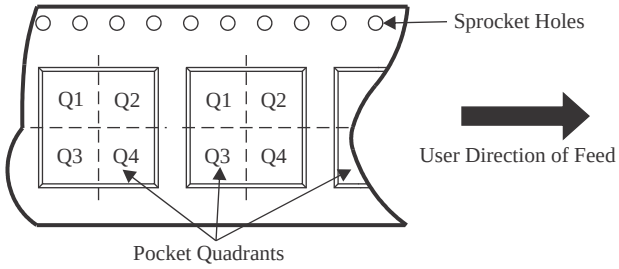


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

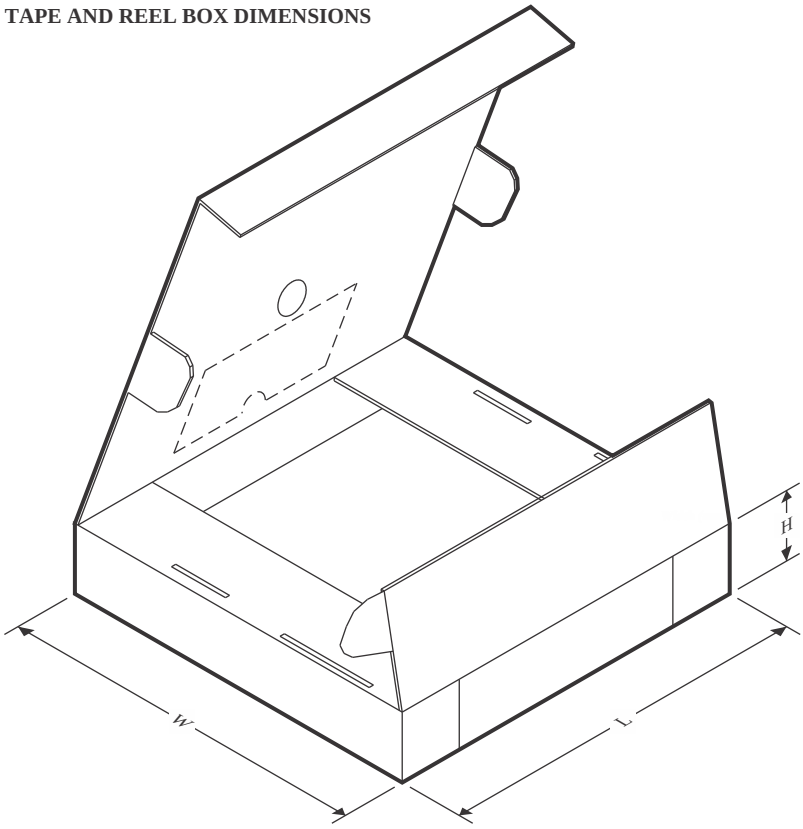
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC3555QDRQ1	SOIC	D	8	3000	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

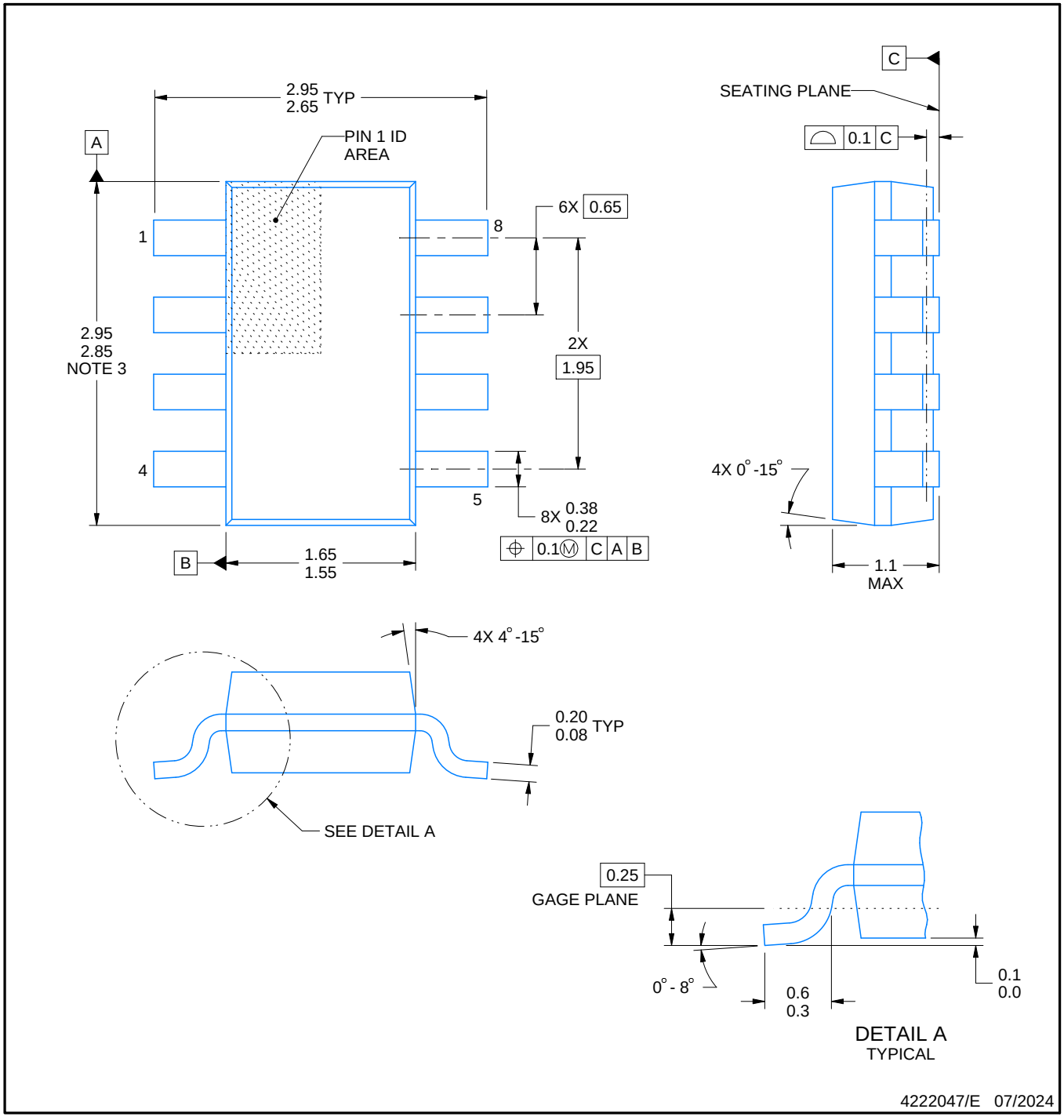
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC3555QDRQ1	SOIC	D	8	3000	340.5	336.1	25.0

PACKAGE OUTLINE

DDF0008A

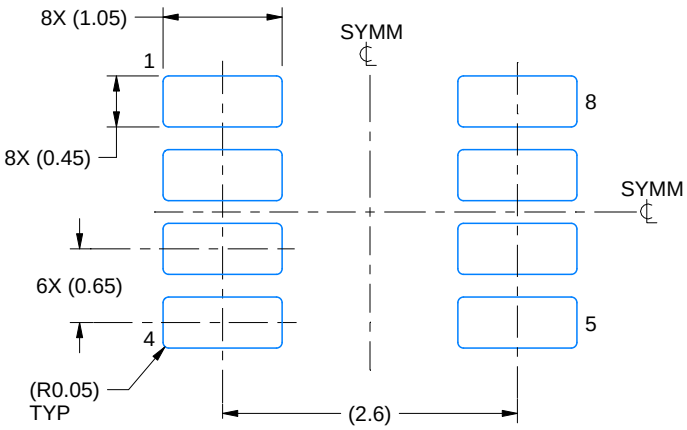
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

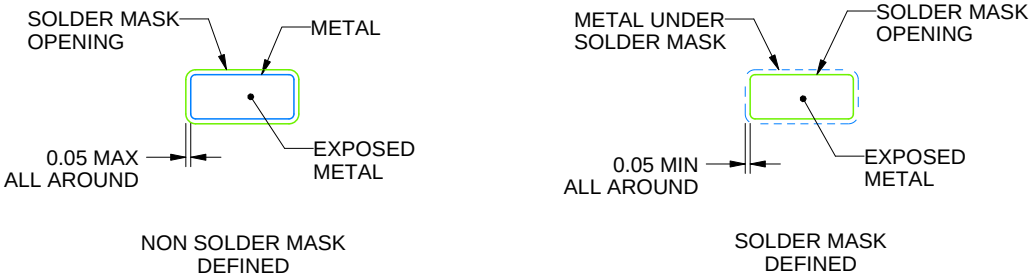


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

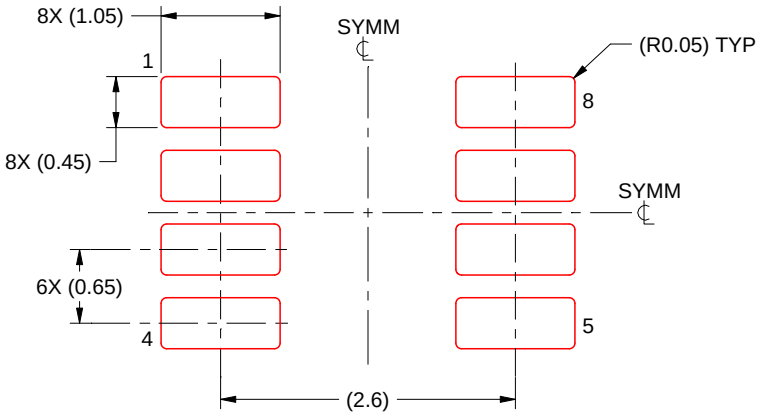
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

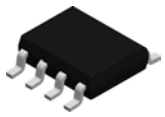


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

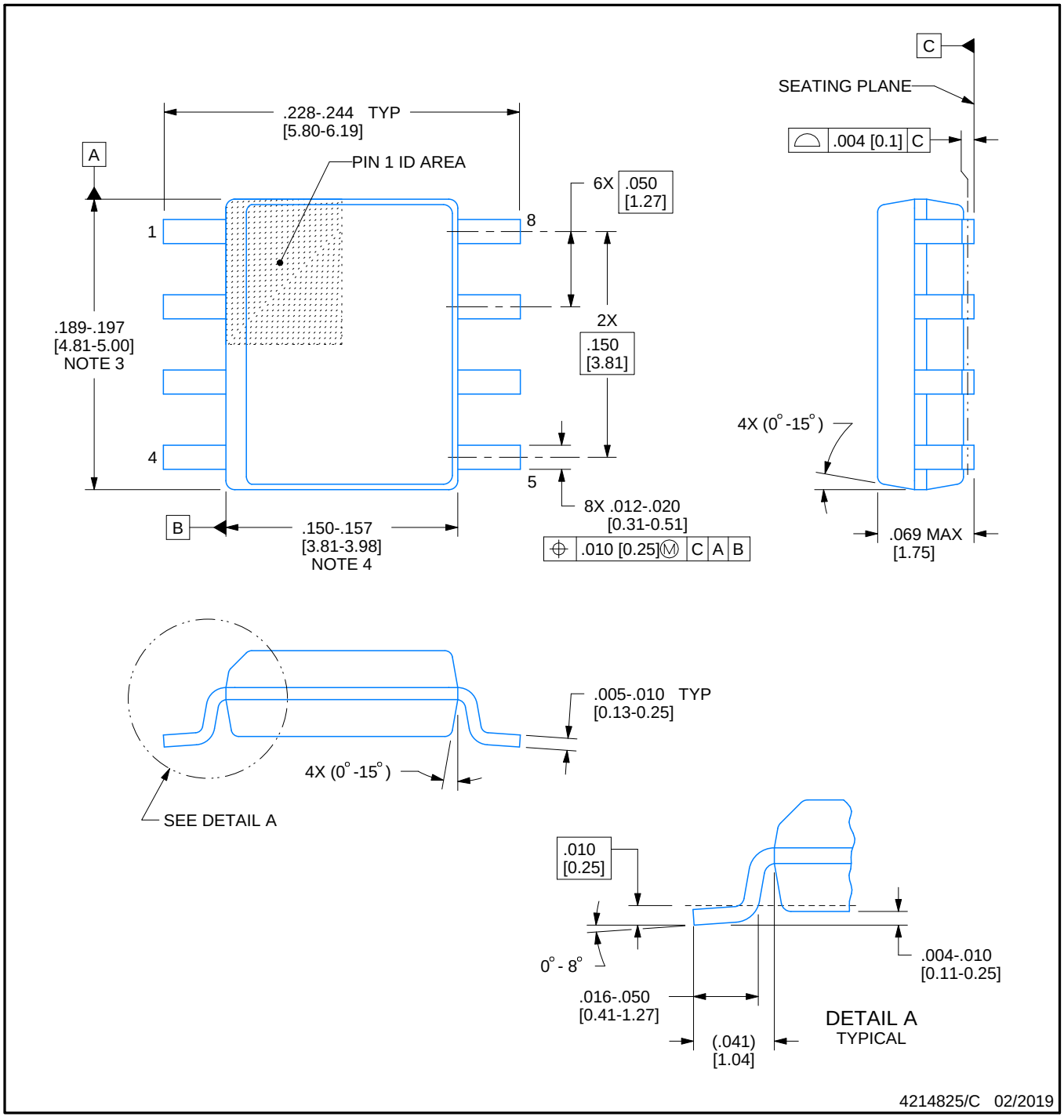


PACKAGE OUTLINE

D0008A

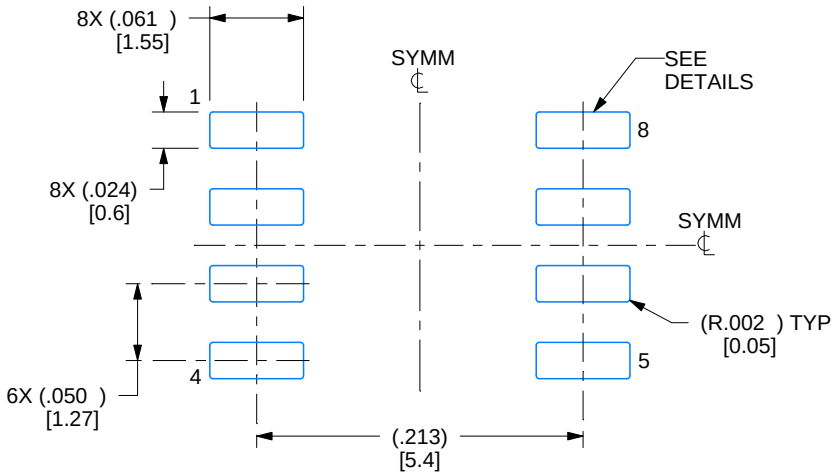
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

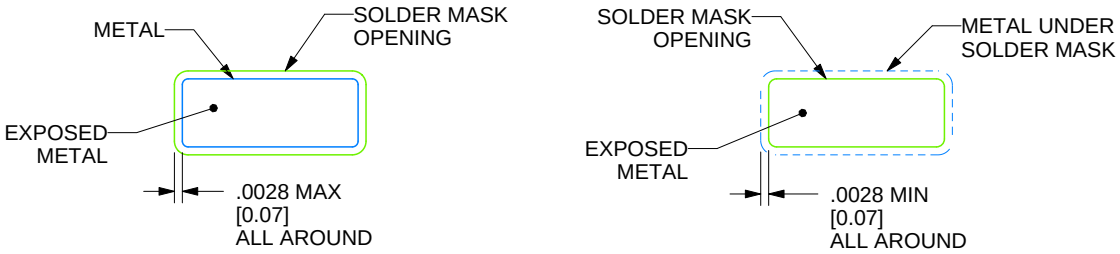


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

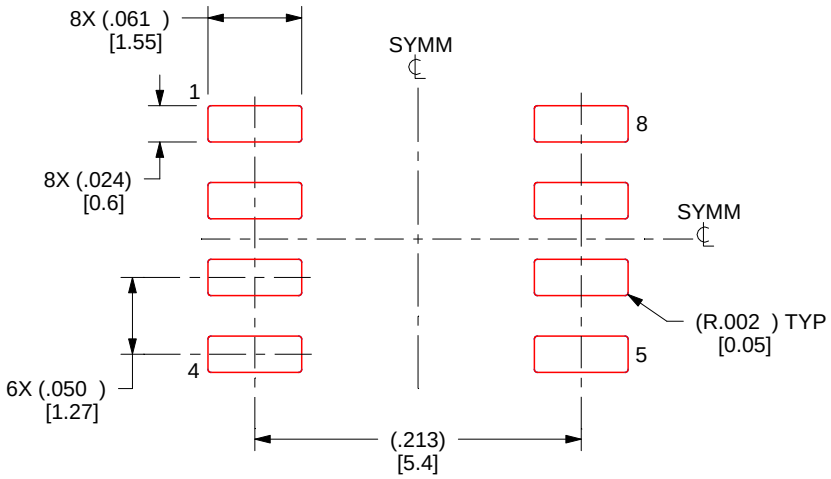
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月