参考資料

TEXAS INSTRUMENTS

TLC6C5912 12チャネル・シフト・レジスタLEDドライバ

1 特長

- 3V～ 5.5Vの広いV_{CC}範囲
- 出力最大定格40V
- 12個のパワーDMOSトランジスタにより、
  V_{CC} = 5Vで50mAの連続電流を出力、
  または1ms未満の単一パルス期間および50mA$_r$
  未満の平均電流で200mAのPWM電流を出力
- サーマル・シャットダウン保護機能
- 拡張カスケードにより複数のステージが可能
- 単一の入力ですべてのレジスタをクリア
- 低消費電力
- 低速なスイッチング時間(tおよびt_f)により、EMIを大幅に低減
- 20ピンのTSSOP-PWパッケージ

2 アプリケーション

- 家電機器用ディスプレイ・パネル
- エレベータ用ディスプレイ・パネル
- PLC用機能インジケータ
- 7セグメント・ディスプレイ

3 概要

TLC6C5912は、モノリシックで中程度の電圧、低電流出力の12ビット・シフト・レジスタで、LEDなど、比較的中程度の負荷電力を必要とするシステムで使用するよう設計されています。

このデバイスには、12ビットのシリアル・イン、パラレル・アウトのシフト・レジスタが内蔵されており、12ビットのDタイプ・ストレージ・レジスタへデータを供給します。データはシフト・レジスタとストレージ・レジスタを経由して、それぞれシフト・レジスタ・クロック(SRCK)とレジスタ・クロック(RCK)の立ち上がりエッジで転送されます。ストレージ・レジスタは、シフト・レジスタ・クリア($\overline{CLR}$)がHIGHのとき、出力バッファへデータを転送します。$\overline{CLR}$がLOWになると、デバイス内のすべてのレジスタがクリアされます。出力イネーブル($\overline{G}$)をHIGHに保持すると、出力バッファのすべてのデータがLOWに保持され、すべてのドレイン出力がオフになります。$\overline{G}$をLOWに保持すると、ストレージ・レジスタのデータが出力バッファへ透過的になります。

このデバイスには、12ビットのシリアル・イン、パラレル・アウトのシフト・レジスタが内蔵されており、12ビットのDタイプ・ストレージ・レジスタへデータを供給します。シフト・レジスタとストレージ・レジスタの両方に、それぞれ独立したクロックが供給されます。

出力はローサイドのオープン・ドレインDMOSトランジスタで、出力定格は40Vです。V_{CC} = 5Vのとき、50mAの連続シンク電流、または1ms未満の単一パルス期間および50mA未満の平均電流で200mAのPWM電流を出力します。デバイスにはサーマル・シャットダウン保護が内蔵されており、人体モデルを使用したテストで2000V、マシン・モデルでは200VまでのESD保護を提供します。

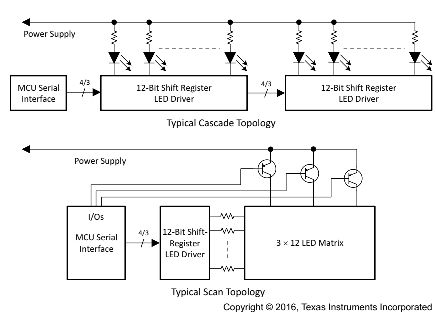
TLC6C5912の特性は、−40°C～105°Cの周辺温度範囲での動作についてのものです。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TLC6C5912	TSSOP (20)	6.50mm×4.40mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

代表的なアプリケーションの回路図



English Data Sheet: SLIS180

目次

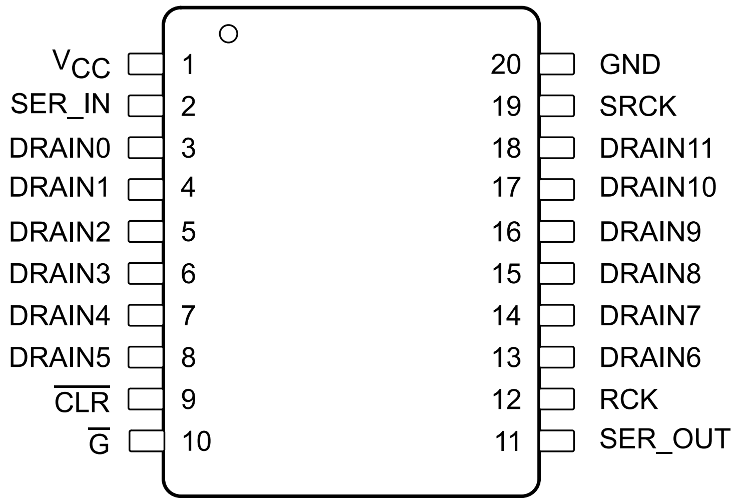
4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

日付	改訂内容	注
2016年5月	*	初版

5 Pin Configuration and Functions

PW Package
20-Pin TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{\text{CLR}}$	9	I	**Shift register clear, active-low:** $\overline{\text{CLR}}$ is the signal used to clear all the registers. The storage register transfers data to the output buffer when shift register clear $\overline{\text{CLR}}$ is high. Driving $\overline{\text{CLR}}$ is low clears all the registers in the device.
DRAIN0	3	O	**Open-drain output:** DRAIN0 to DRAIN11 are the LED current-sink channels. These pins connect to the LED cathodes, and they can survive up to 40-V LED supply voltage.
DRAIN1	4	O	
DRAIN2	5	O	
DRAIN3	6	O	
DRAIN4	7	O	
DRAIN5	8	O	
DRAIN6	13	O	
DRAIN7	14	O	
DRAIN8	15	O	
DRAIN9	16	O	
DRAIN10	17	O	
DRAIN11	18	O	
$\overline{\text{G}}$	10	I	**Output enable, active-low:** $\overline{\text{G}}$ is the LED channel enable and disable input pin. Having $\overline{\text{G}}$ low enables all drain channels according to the output-latch register content. When high, all channels are off.
GND	20	—	**Power ground:** GND is the ground reference pin for the device. This pin must connect to the ground plane on the PCB.
RCK	12	I	**Register clock:** RCK is the storage register clock. The data in each shift register stage transfers to the storage register at the rising edge of RCK. Data in the storage register appears at the output whenever the output enable $\overline{\text{G}}$ input signal is high.
SER IN	2	I	**Serial-data input:** SER IN is the serial data input. Data on SER IN loads into the internal register on each rising edge of SRCK.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
SER OUT	11	O	**Serial-data output:** SER OUT is the serial data output of the 12−bit serial shift register. The purpose of this pin is to cascade several devices on the serial bus. By connecting the SER OUT pin to the SER IN input of the next device on the serial bus to cascade, the data transfers to the next device on the falling edge of SRCK. This can improve the cascade application reliability, as it can avoid the issue that the second device receives SRCK and data input at the same rising edge of SRCK.
SRCK	19	I	**Shift-register clock:** SRCK is the serial clock input. On each rising SRCK edge, data transfers from SER IN to the internal serial shift registers.
V_{CC}	1	I	**Power supply:** V_{CC} is the power supply pin voltage for the device. TI recommends adding a 0.1 μF ceramic capacitor close to the pin.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Logic supply voltage		8	V
V_I	Logic input-voltage	–0.3	8	V
V_{DS}	Power DMOS drain-to-source voltage		42	V
	Continuous total dissipation	See *Thermal Information*		
	Operating ambient temperature (Top)		105	°C
T_J	Operating junction temperature	–40	125	°C
T_{stg}	Storage temperature	–55	165	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	3	5.5	V
V_{IH}	High-level input voltage	2.4		V
V_{IL}	Low-level input voltage		0.7	V
t_{su}	Setup time, SER IN high before SRCK↑	15		ns
t_h	Hold time, SER IN high after SRCK↑	15		ns
t_w	Pulse duration	40		ns
T_A	Operating ambient temperature	–40	105	°C

6.4 Thermal Information

THERMAL METRIC(1)		TLC6C5912 PW (TSSOP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	114.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	44.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	60.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	DRAIN0 to DRAIN11, drain-to-source voltage					40	V
V_{OH}	High-level output voltage, SER OUT	I_{OH} = –20 µA	V_{CC} = 5 V	4.9	4.99		V
		I_{OH} = –4 mA		4.5	4.69		
V_{OL}	Low-level output voltage, SER OUT	I_{OH} = 20 µA	V_{CC} = 5 V		0.001	0.01	V
		I_{OH} = 4 mA			0.25	0.4	
I_{IH}	High-level input current	V_{CC} = 5 V, V_I = V_{CC}			0.2		µA
I_{IL}	Low-level input current	V_{CC} = 5 V, V_I = 0			–0.2		µA
I_{CC}	Logic supply current	V_{CC} = 5 V, No clock signal	All outputs off		0.1	1	µA
			All outputs on		130	170	
$I_{CC(FRQ)}$	Logic supply current at frequency	f_{SRCK} = 5 MHz, C_L = 30 pF, all outputs on			300		µA
I_{DSX}	Off-state drain current	V_{DS} = 30 V, V_{CC} = 5 V				0.1	µA
		V_{DS} = 30 V, T_C = 125°C, V_{CC} = 5 V			0.15	0.3	
$r_{DS(on)}$	Static drain-source on-state resistance	I_D = 20 mA, V_{CC} = 5 V, T_A = 25°C, single channel ON		6	7.4	8.6	Ω
		I_D = 20 mA, V_{CC} = 5 V, T_A = 25°C, all channels ON		6.7	8.9	9.6	
		I_D = 20 mA, V_{CC} = 3.3 V, T_A = 25°C, single channel ON		7.9	9.3	11.2	
		I_D = 20 mA, V_{CC} = 3.3 V, T_A = 25°C, all channels ON		8.7	10.6	12.3	
		I_D = 20 mA, V_{CC} = 5 V, T_A = 105°C, single channel ON		9.1	11.2	12.9	
		I_D = 20 mA, V_{CC} = 5 V, T_A = 105°C, all channels ON		10.3	13	14.5	
		I_D = 20 mA, V_{CC} = 3.3 V, T_A = 105°C, single channel ON		11.6	13.7	16.4	
		I_D = 20 mA, V_{CC} = 3.3 V, T_A = 105°C, all channels ON		12.8	15.6	18.2	
$T_{SHUTDOWN}$	Thermal shutdown trip point			150	175	200	°C
t_{HYS}	Hysteresis				15		°C

6.6 Switching Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from $\overline{G}$	C_L = 30 pF, I_D = 48 mA		210		ns
t_{PHL}	Propagation delay time, high-to-low-level output from $\overline{G}$			75		ns
t_r	Rise time, drain output			250		ns
t_f	Fall time, drain output			200		ns
t_{pd}	Propagation delay time, SRCK↓ to SEROUT	C_L = 30 pF, I_D = 48 mA		35		ns
t_{or}	SEROUT rise time (10% to 90%)	C_L = 30 pF		20		ns
t_{of}	SEROUT fall time (90% to 10%)	C_L = 30 pF		20		ns

Switching Characteristics (continued)

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(SRCK)}$	Serial clock frequency	C_L = 30 pF, I_D = 20 mA			10	MHz
t_{SRCK_WH}	SRCK pulse duration, high		30			ns
t_{SRCK_WL}	SRCK pulse duration, low		30			ns

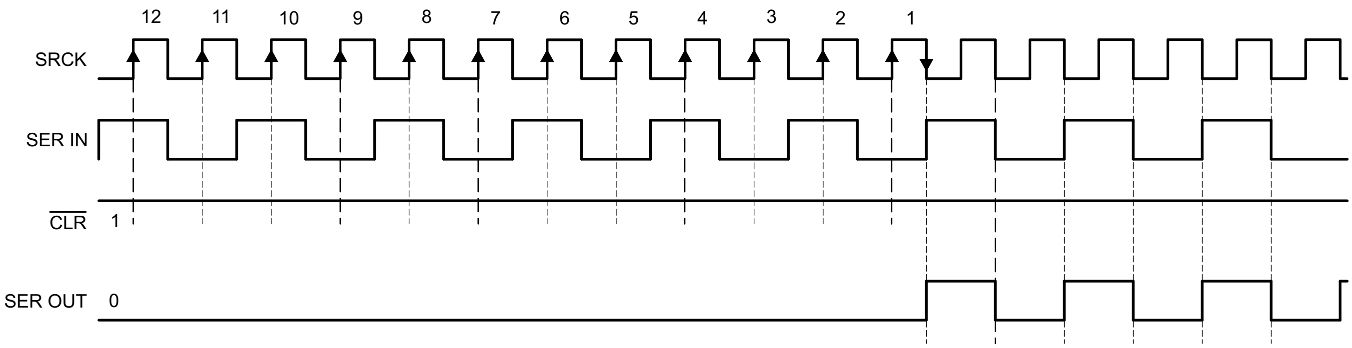


Figure 1. SER IN to SER OUT Waveform

Figure 1 shows the SER IN to SER OUT waveform. The output signal appears on the falling edge of the shift register clock (SRCK) because there is a phase inverter at SER OUT (see Figure 2). As a result, it takes seven and a half periods of SRCK for data to transfer from SER IN to SER OUT.

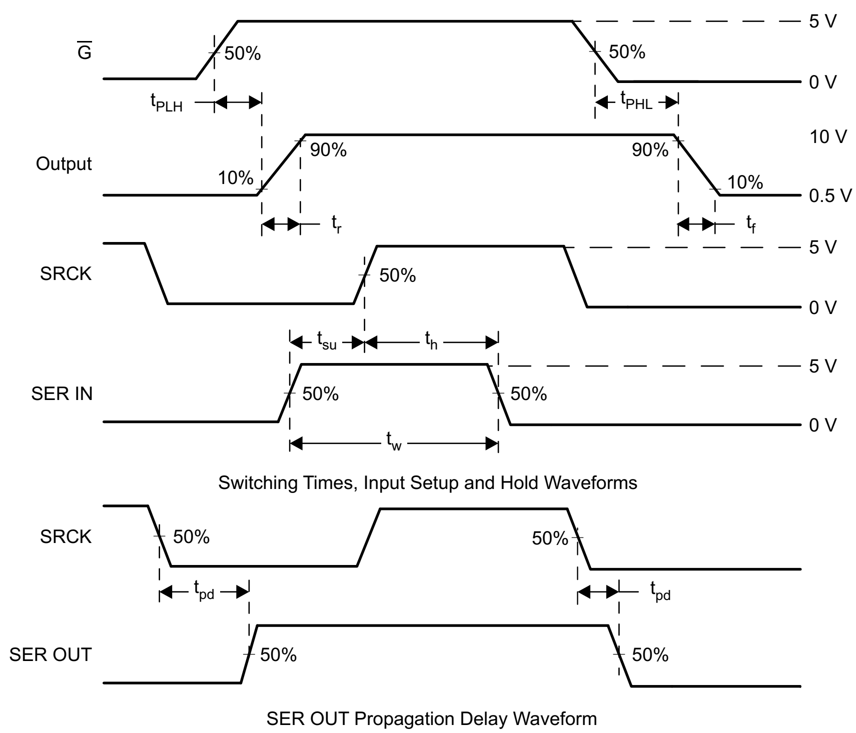
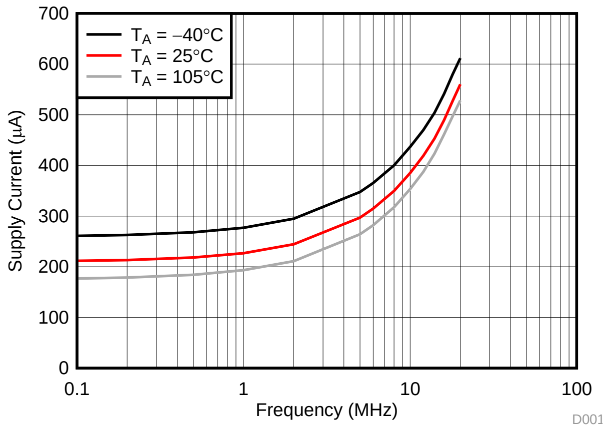


Figure 2. Switching Times and Voltage Waveforms

Figure 2 shows the switching times and voltage waveforms. Tests for all these parameters took place using the test circuit shown in Figure 12.

6.7 Typical Characteristics

Conditions for Figure 5 and Figure 6: Single channel on; conditions for Figure 7, Figure 8, and Figure 9: All channels on.



V_{CC} = 5 V

Figure 3. Supply Current vs Frequency

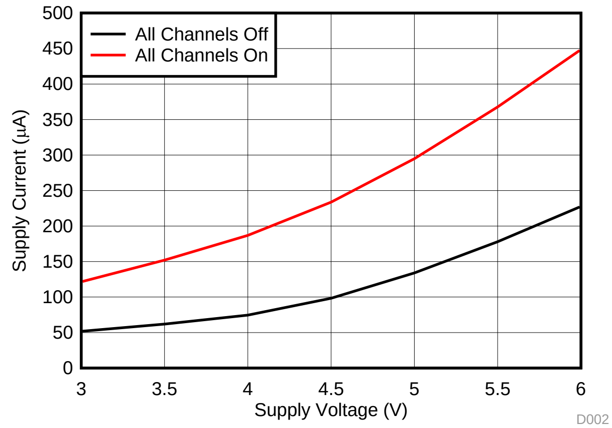
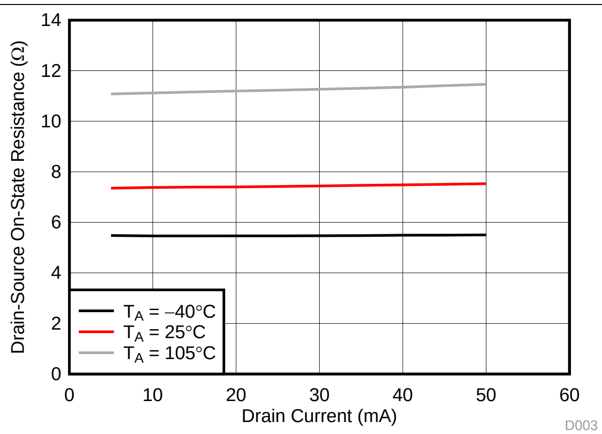
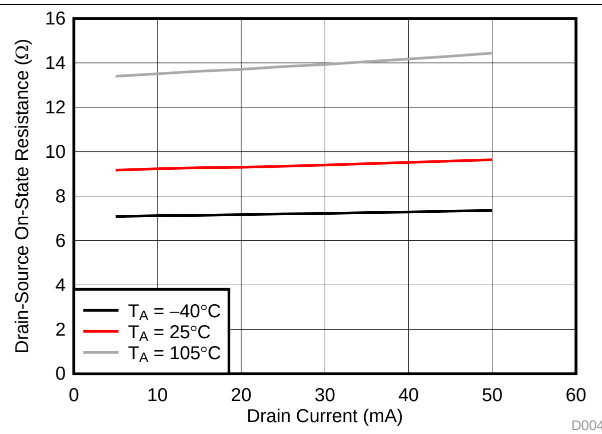


Figure 4. Supply Current vs Supply Voltage



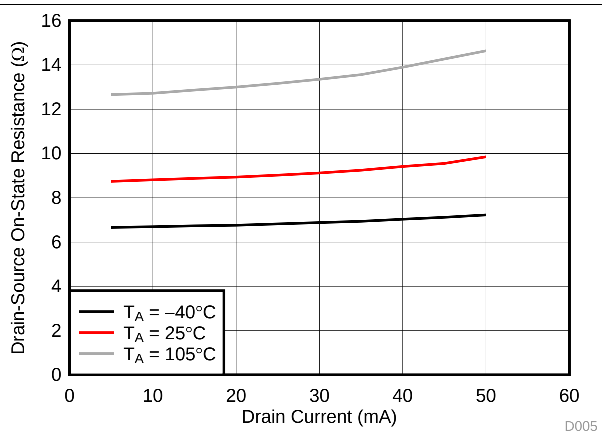
V_{CC} = 5 V

Figure 5. Drain-to-Source On-State Resistance vs Drain Current (Single Channel On)



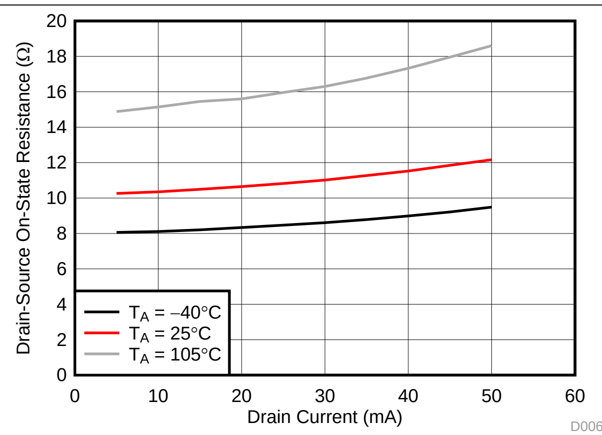
V_{CC} = 3.3 V

Figure 6. Drain-to-Source On-State Resistance vs Drain Current (Single Channel On)



V_{CC} = 5 V

Figure 7. Drain-to-Source On-State Resistance vs Drain Current (All Channels On)

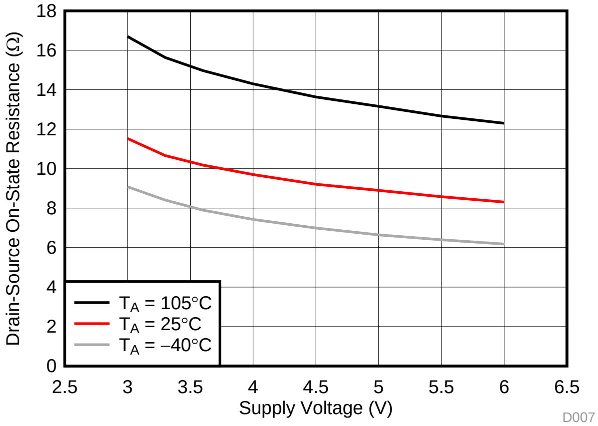


V_{CC} = 3.3 V

Figure 8. Drain-to-Source On-State Resistance vs Drain Current (All Channels On)

Typical Characteristics (continued)

Conditions for Figure 5 and Figure 6: Single channel on; conditions for Figure 7, Figure 8, and Figure 9: All channels on.



$I_{(ds)}$ = 20 mA

Figure 9. Drain-to-Source On-State Resistance vs Supply Voltage

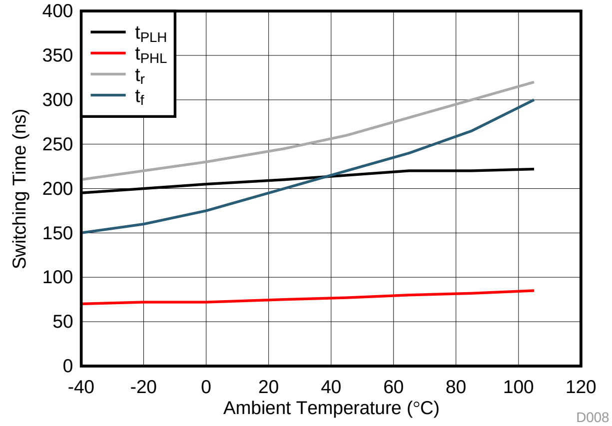
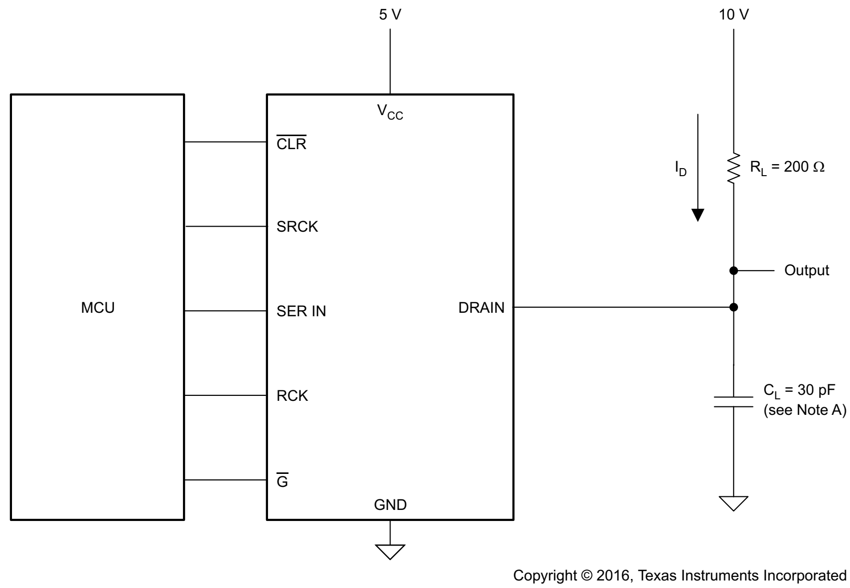


Figure 10. Switching Time vs Ambient Temperature

7 Parameter Measurement Information



A. C_L includes probe and jig capacitance.

Figure 11. Resistive-Load Test Circuit

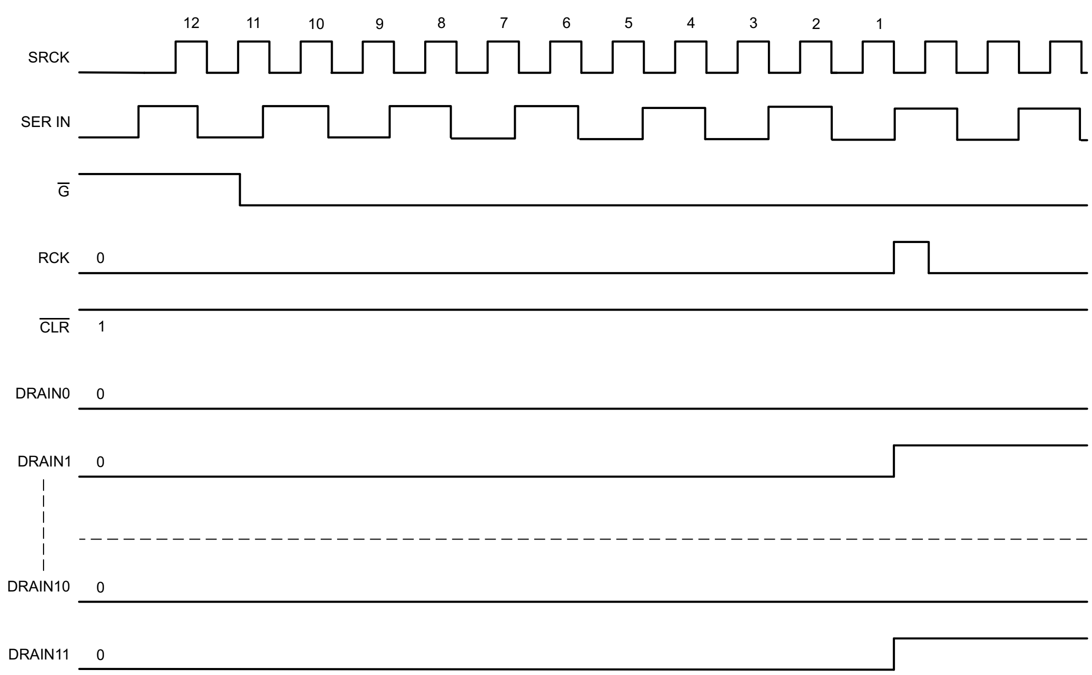


Figure 12. Voltage Waveforms

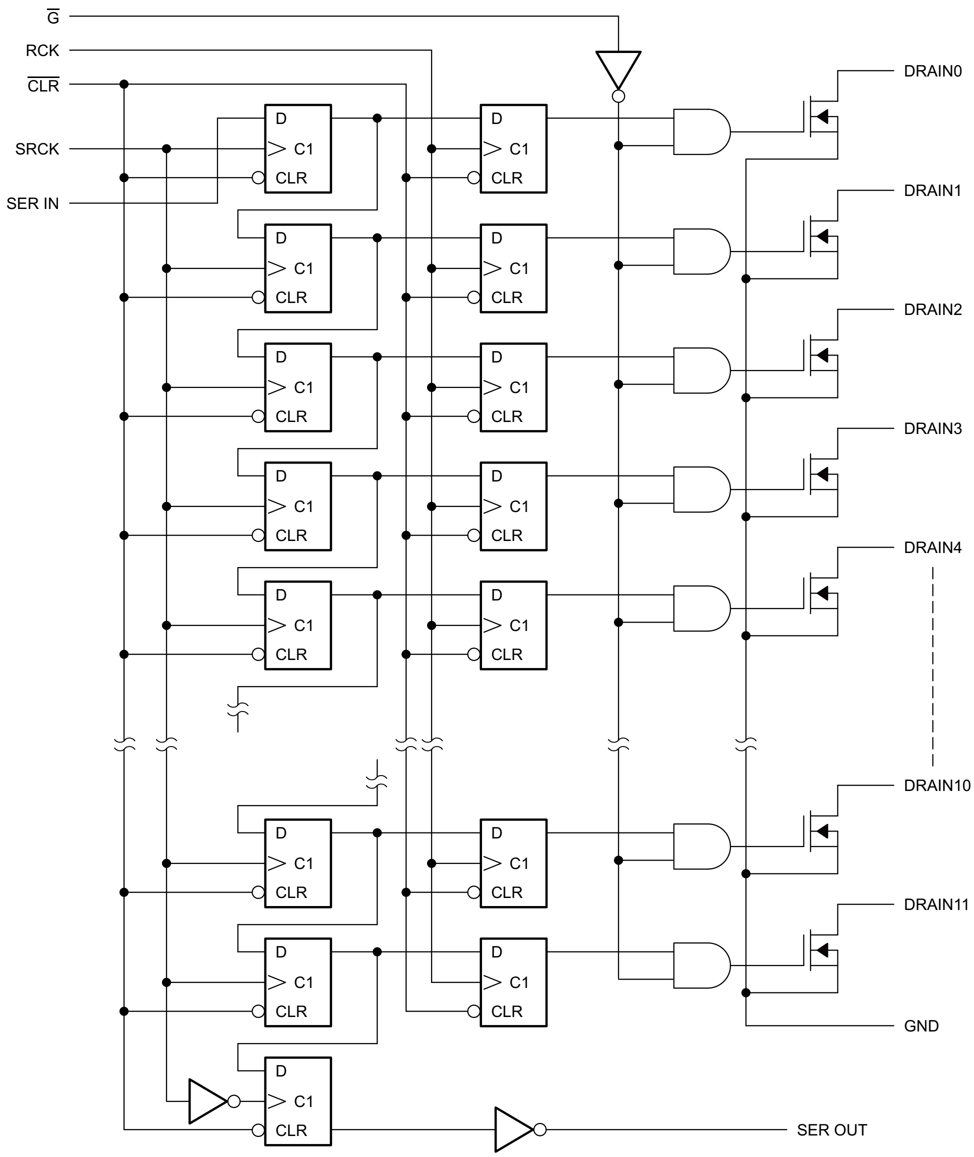
Figure 11 and Figure 12 show the resistive-load test circuit and voltage waveforms. One can see from Figure 12 that with G held low and CLR held high, the status of each drain changes on the rising edge of the register clock, indicating the transfer of data to the output buffers at that time.

8 Detailed Description

8.1 Overview

The TLC6C5912 device is a monolithic, medium-voltage, low current 12-bit shift register designed to drive relatively moderate load power such LEDs. The device contains a 12-bit serial-in, parallel-out shift register that feeds a 12-bit D-type storage register. Thermal shutdown protection is also built-into the device.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 175°C (typical). The thermal shutdown forces the device to have an open state when the junction temperature exceeds the thermal trip threshold. Once the junction temperature decreases to less than 160°C (typical), the device begins to operate again.

Feature Description (continued)

8.3.2 Serial-In Interface

The TLC6C598 device contains an 8-bit serial-in, parallel out shift register that feeds an 8-bit D-type storage register. Data transfer through both the shift and storage registers on the rising edge of the shift register clock (SRCK) and the register clock (RCK), respectively. The storage transfers data to the output buffer when shift register clear (CLR) is high.

8.3.3 Clear Register

A logic low on $\overline{\text{CLR}}$ clears all registers in the device. TI suggests clearing the device during power up or initialization.

8.3.4 Cascade Through SER OUT

By connecting the SER OUT pin to the SER IN input of the next device on the serial bus to cascade, the data transfers to the next device on the falling edge of SRCK. This can improve the cascade application reliability, as it can avoid that the second device receives SRCK and data input at the same rising edge of SRCK.

8.3.5 Output Control

Holding the output enable (G) high holds all data in the output buffers low, and all drain outputs are off. Holding G low makes data from the storage register transparent to the output buffers. When data in the output buffers is low, the DMOS transistor outputs are off. When data is high, the DMOS transistor outputs are capable of sink-current. This pin also be used for global PWM dimming.

8.4 Device Functional Modes

8.4.1 Operation With V_{CC} < 3 V

This device works normally during 3 V ≤ V_{CC} ≤ 5.5 V, when operation voltage is lower than 3 V. The behavior of device cannot be ensured, including communication interface and current capability.

8.4.2 Operation With 5.5 V ≤ V_{CC} ≤ 8 V

The device works normally during this voltage range, but reliability issues may occurs while the device works for a long time in this voltage range.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TLC6C5912 device is a serial-in, parallel-out, power logic 8-bit shift register with low-side open-drain DMOS output rating of 40 V and 50-mA continuous sink-current capabilities when V_{CC}= 5 V. The device is designed to drive resistive loads and is particularly well-suited as an interface between a microcontroller and LEDs or lamps. The device also provides up to 2000 V of ESD protection when tested using the human body model and 200 V when using the machine model.

9.2 Typical Application

Figure 13 shows a typical cascade application circuit with two TLC6C5912 chips configured to cascade topology. The MCU generates all the input signals.

Typical Application (continued)

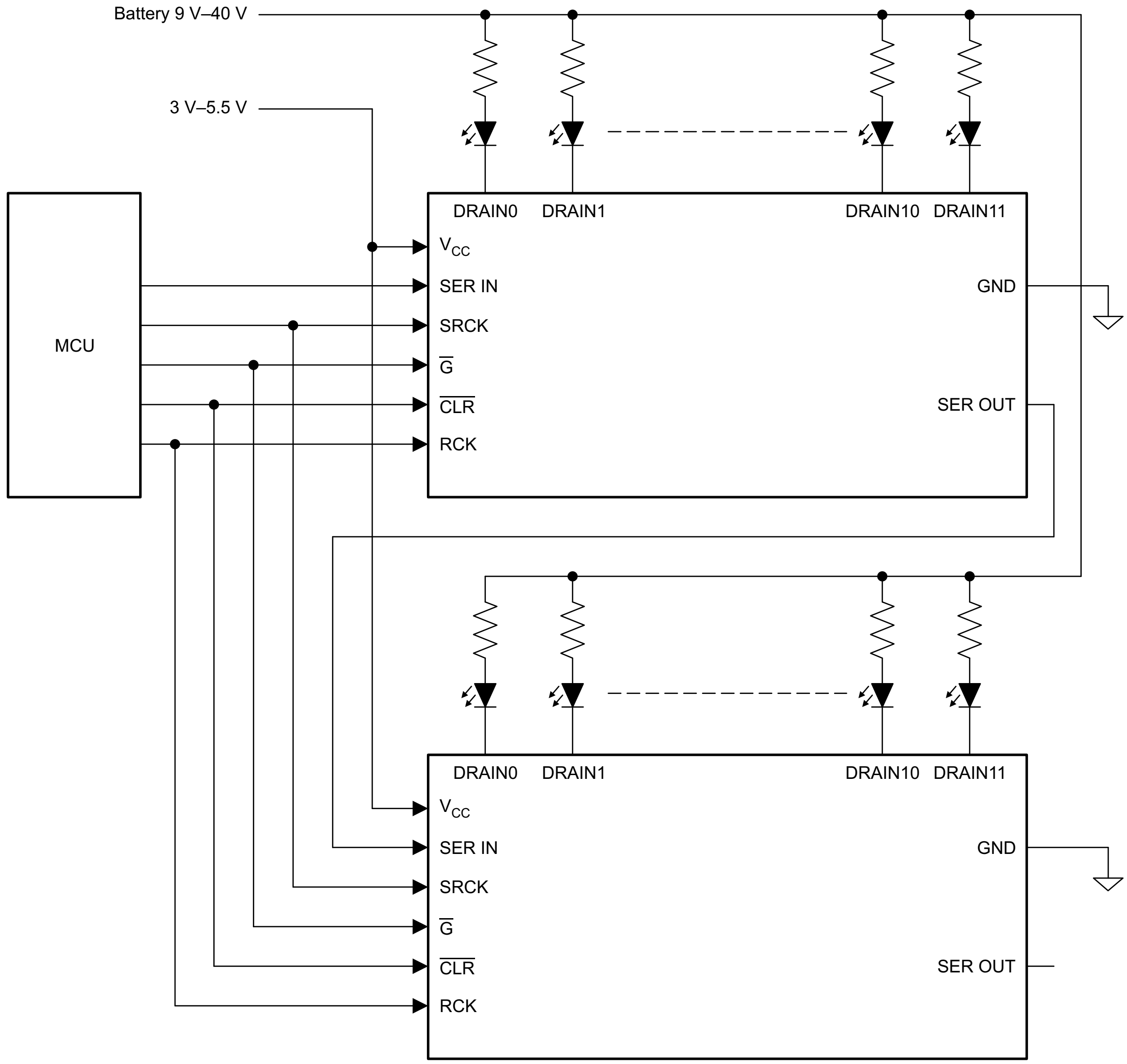


Figure 13. Typical Application Circuit

9.2.1 Design Requirements

Table 1 lists the parameters for this design example.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Vbattery	9 V to 40 V
V_{CC} _ 1	3.3 V
I(D0), I(D1), I(D2), I(D3) , I(D4), I(D5), I(D6), I(D7), I(D8), I(D9), I(D10), I(D11)	30 mA
V_{CC} _ 2	5 V
I(D12), I(D13), I(D14), I(D15) , I(D16), I(D17), I(D18), I(D19), I(D20), I(D21), I(D122), I(D23)	50 mA

9.2.2 Detailed Design Procedure

To begin the design process, the designer must decide on a few parameters:

- Vsupply: LED supply voltage
- VDx: LED forward voltage
- I: LED current

After determining the parameters, calculate the resistor in series with LED using Equation 1.

$$Rx = (Vsupply – VDx) / I \tag{1}$$

9.2.3 Application Curve

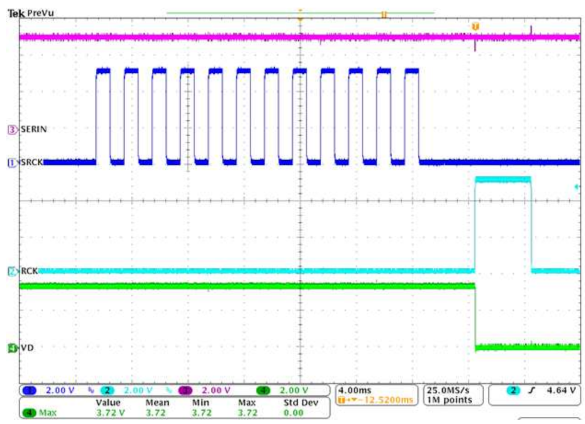


Figure 14. TLC6C5912 Application Waveform

10 Power Supply Recommendations

The TLC6C5912 device is designed to operate from an input voltage supply range from 3 V to 5.5 V. This input supply should be well regulated. TI recommends placing the ceramic bypass capacitors near the V_{CC} pin.

11 Layout

11.1 Layout Guidelines

There are no special layout requirement for the digital signal pins. The only requirement is placing the ceramic bypass capacitors near the corresponding pin.

Maximize the copper coverage on the PCB to increase the thermal conductivity of the board. The major heat-flow path from the package to the ambient is through the cooper on the PCB. Maximizing the copper coverage is extremely important when the design does not include heat sinks attached to the PCB on the other side of the package.

- Add as many thermal vias as possible directly under the package ground pad to optimize the thermal conductivity of the board.
- All thermal vias should be either plated shut or plugged and capped on both sides of the board to prevent solder voids. To ensure reliability and performance, the solder coverage should be at least 85%.

11.2 Layout Example

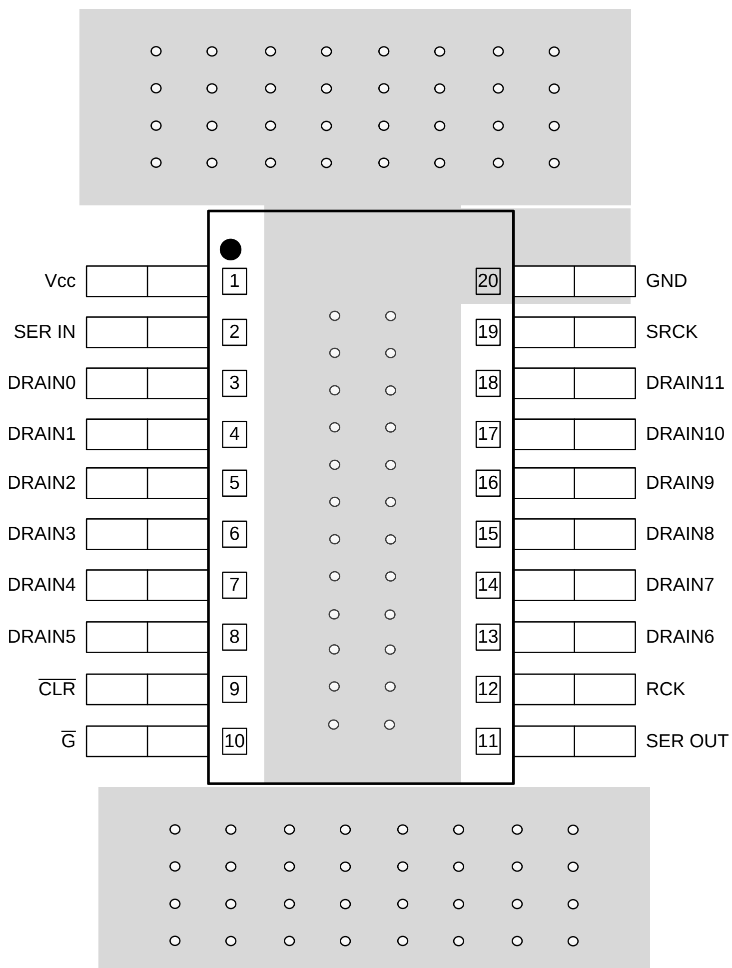


Figure 15. Layout Recommendation

12 デバイスおよびドキュメントのサポート

12.1 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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12.2 商標

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12.3 静電気放電に関する注意事項

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12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC6C5912PWR	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	6C5912I
TLC6C5912PWR.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	6C5912I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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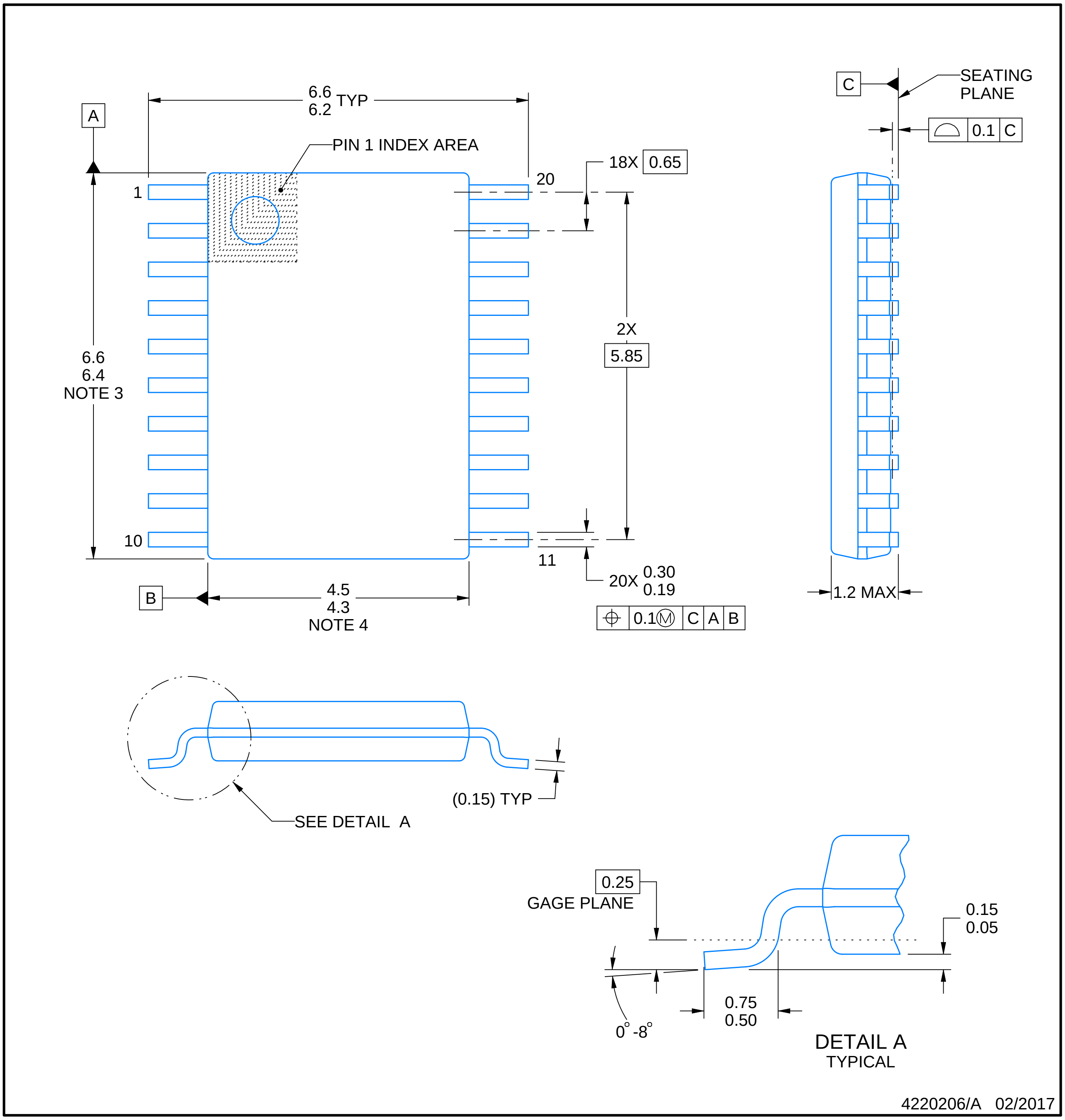
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLC6C5912 :

- Automotive : TLC6C5912-Q1

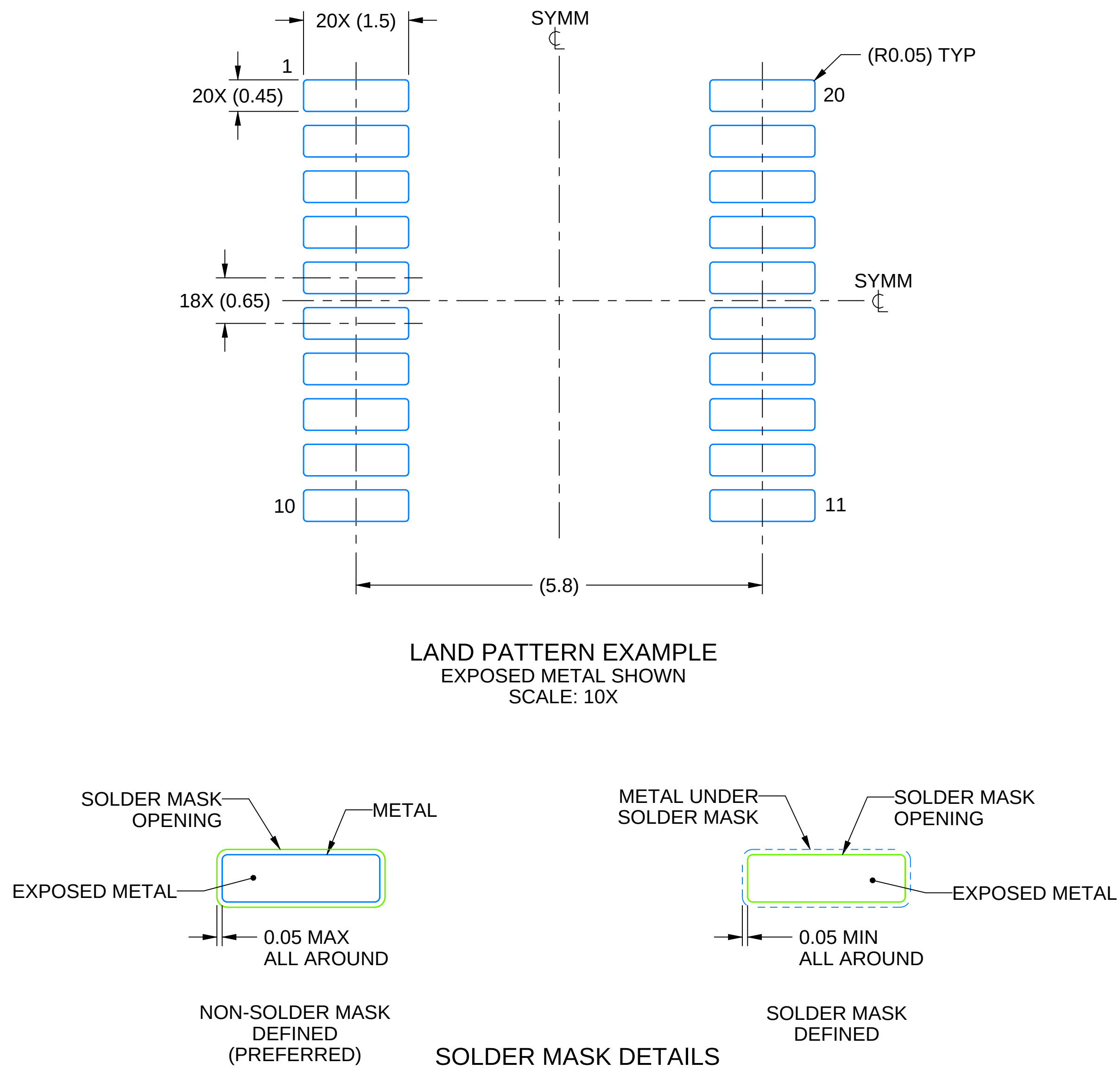
NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects



NOTES:

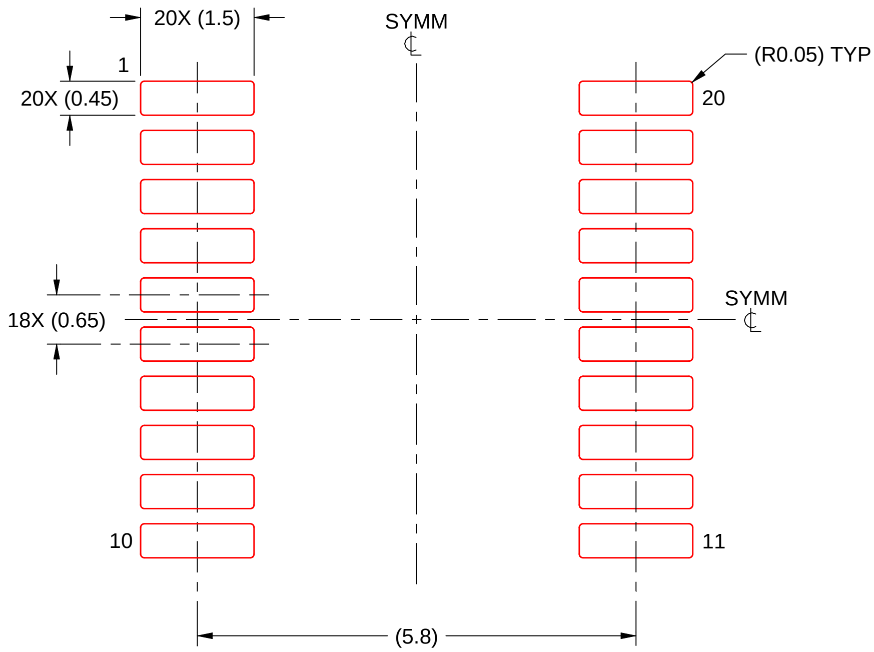
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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