TEXAS INSTRUMENTS

TLV1701-Q1, TLV1702-Q1, TLV1704-Q1

JAJSE11B – NOVEMBER 2015 – REVISED SEPTEMBER 2017

TLV170x-Q1 2.2V～36V、マイクロパワー・コンパレータ

1 特長

- **車載アプリケーション用に認定済み**
- **以下の結果でAEC Q100認定済み**
  - デバイス温度グレード 1: 動作時周囲温度 –40℃～+125°C
  - デバイスHBM ESD分類レベル3A (TLV1701-Q1)
  - デバイスHBM ESD分類レベル1C (TLV1702-Q1、TLV1704-Q1)
  - デバイスCDM ESD分類レベルC5
- **電源電圧範囲**: 2.2V～36Vまたは±1.1V～±18V
- **低い静止電流**: コンパレータあたり55µA
- **入力同相範囲に両レールを含む**
- **短い伝搬遅延**: 560ns
- **低い入力オフセット電圧**: 300µV
- **オープン・コレクタ出力**:
  - 電源電圧に関係なく負電源を最大36V上回る
- **工業用温度範囲**: －40℃～＋125℃
- **小型パッケージ**:
  - シングル: SOT23-5
  - デュアル: VSSOP-8
  - クワッド: TSSOP-14

2 アプリケーション

- **過電圧および低電圧検出器**
- **ウィンドウ・コンパレータ**
- **過電流検出器**
- **ゼロクロス検出器**
- **システム監視**:
  - 白物家電
  - オートモーティブ(車載)
  - 医療用

3 概要

TLV1701-Q1 (シングル)、TLV1702-Q1 (デュアル)、およびTLV1704-Q1 (クワッド)デバイスは、広い電源電圧範囲、レール・ツー・レール入力、低い静止電流、短い伝搬遅延時間を実現しています。こうした機能を業界標準の超小型パッケージで提供することから、これらのデバイスは市販の汎用コンパレータでは最高水準のものとなっています。

オープン・コレクタ出力により、TLV170x-Q1の電源電圧に関係なく、負電源を最大36V上回る電圧レールまで出力を引き上げることができます。

このデバイスはマイクロパワー・コンパレータです。低入力オフセット電圧、低入力バイアス電流、低消費電流、オープン・コレクタ設定により、TLV170x-Q1デバイスには、単純な電圧検出からシングル・リレーの駆動まで、ほぼすべてのアプリケーションに対応する柔軟性があります。

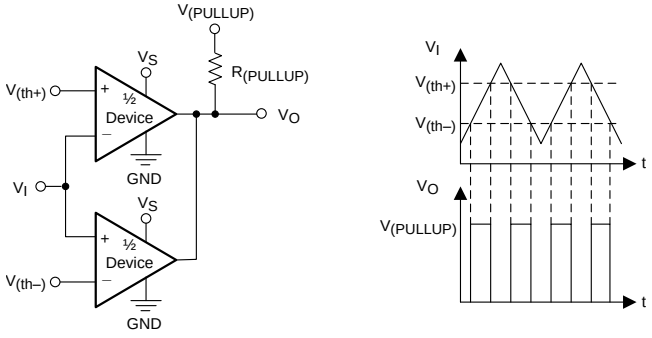
このデバイスは、－40℃～＋125℃の拡張工業用温度範囲で仕様が規定されています。

製品情報(1)

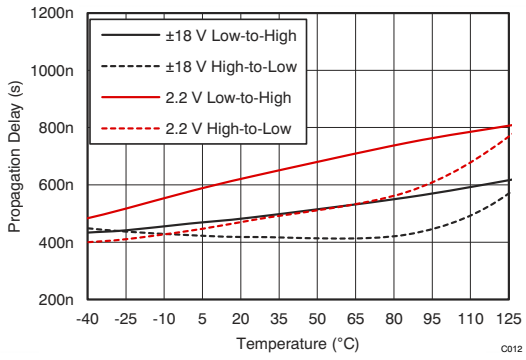
型番	パッケージ	本体サイズ(公称)
TLV1701-Q1	SOT-23 (5)	1.60mm×2.90mm
TLV1702-Q1	VSSOP (8)	3.00mm×3.00mm
TLV1704-Q1	TSSOP (14)	4.40mm×5.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。

ウィンドウ・コンパレータとしてのTLV1702-Q1



安定した伝搬遅延 対 温度



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (December 2015) から Revision B に変更 **Page**

- TLV1701-Q1デバイスをデータシートに追加 ... 1
- Added TLV1701-Q1 to ESD table and specified the ESD ratings under each device ... 5

2015年11月発行のものから更新 **Page**

- TLV1704-Q1デバイスをデータシートに追加 ... 1

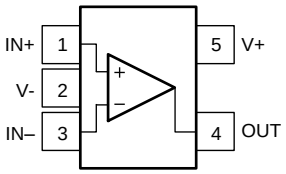
5 Device Comparison Table

Table 1. Related Products

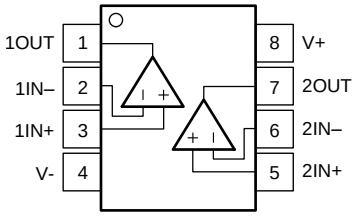
DEVICE	FEATURES
TLC3702-Q1	Push-pull, 20-µA, 20-mA drive
TLC3704-Q1	
TLV3012-Q1	Push-pull, 5-µA, integrated 1.242-V reference
TLV3501-Q1	Push-Pull, 3.2 mA, 4.5-ns propagation delay
TLV3502-Q1	
TLV3701-Q1	Push-pull, 560-nA, reverse battery to 16 V
TLV3702-Q1	
REF50xx-Q1	Series reference, 0.1% tolerance, 8 ppm/°C
TL4050xx-Q1	Shunt reference, 0.1% tolerance, 50 ppm/°C
TLVH431-Q1	Adjustable Shunt Reference, 1.24 V to 18 V

6 Pin Configuration and Functions

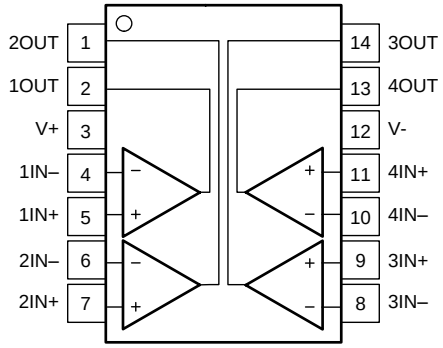
TLV1701-Q1 DBV Package
5-Pin SOT-23
Top View



TLV1702-Q1 DGK Package
8-Pin VSSOP
Top View



TLV1704-Q1 PW Package
14-Pin TSSOP
Top View



Pin Functions

PIN				I/O	DESCRIPTION
NAME	TLV1701-Q1 DBV	TLV1702-Q1 DGK	TLV1704-Q1 PW		
IN+	1	—	—	I	Noninverting input
1IN+	—	3	5	I	Noninverting input, channel 1
2IN+	—	5	7	I	Noninverting input, channel 2
3IN+	—	—	9	I	Noninverting input, channel 3
4IN+	—	—	11	I	Noninverting input, channel 4
IN–	3	—	—	I	Inverting input
1IN–	—	2	4	I	Inverting input, channel 1
2IN–	—	6	6	I	Inverting input, channel 2
3IN–	—	—	8	I	Inverting input, channel 3
4IN–	—	—	10	I	Inverting input, channel 4
OUT	4	—	—	O	Output
1OUT	—	1	2	O	Output, channel 1
2OUT	—	7	1	O	Output, channel 2
3OUT	—	—	14	O	Output, channel 3
4OUT	—	—	13	O	Output, channel 4
V+	5	8	3	—	Positive (highest) power supply
V–	2	4	12	—	Negative (lowest) power supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage			40 (±20)	V
Signal input pins	Voltage(2)	(V_S–) – 0.5	(V_S+) + 0.5	V
	Current(2)		±10	mA
Output short-circuit(3)		Continuous		mA
Operating temperature		–55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to ground; one comparator per package.

7.2 ESD Ratings

			VALUE	UNIT
TLV1701-Q1				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	
TLV1702-Q1				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±1000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	
TLV1704-Q1				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±1000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage V_S = (V_S+) – (V_S–)	2.2 (±1.1)		36 (±18)	V
Specified temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TLV1701-Q1 DBV (SOT-23) 5 PINS	TLV1702-Q1 DGK (VSSOP) 8 PINS	TLV1704-Q1 PW (TSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	233.1	199	128.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	156.4	89.5	56.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60.6	120.4	69.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	35.7	22	9.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	59.7	118.7	69.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

at T_A = 25°C, V_S = 2.2 V to 36 V, C_L = 15 pF, R_{PULLUP} = 5.1 kΩ, V_{CM} = V_S / 2, and V_S = V_{PULLUP} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	T_A = 25°C, V_S = 2.2 V		±0.5	±3.5	mV
		T_A = 25°C, V_S = 36 V		±0.3	±2.5	mV
		T_A = –40°C to +125°C			±5.5	mV
		T_A = 25°C, V_S = 36 V, TLV1701-Q1 Only		±0.4	±3.2	
		T_A = –40°C to +125°C, TLV1701-Q1 Only			±6.3	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C		±4	±20	µV/°C
PSRR	Power-supply rejection ratio	T_A = 25°C		15	100	µV/V
		T_A = –40°C to +125°C		20		µV/V
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	T_A = –40°C to +125°C	(V–)		(V+)	V
INPUT BIAS CURRENT						
I_B	Input bias current	T_A = 25°C		5	15	nA
		T_A = –40°C to +125°C			20	nA
I_{OS}	Input offset current			0.5		nA
C_{LOAD}	Capacitive load drive		See *Typical Characteristics*			
OUTPUT						
V_O	Voltage output swing from rail	I_O ≤ 4 mA, input overdrive = 100 mV, V_S = 36 V			900	mV
		I_O = 0 mA, input overdrive = 100 mV, V_S = 36 V			600	mV
I_{SC}	Short circuit sink current			20		mA
	Output leakage current	V_{IN+} > $V_{IN–}$		70		nA
POWER SUPPLY						
V_S	Specified voltage range		2.2		36	V
I_Q	Quiescent current (per channel)	I_O = 0 A		55	75	µA
		I_O = 0 A, T_A = –40°C to +125°C			100	µA

7.6 Switching Characteristics

at T_A = 25°C, V_S = +2.2 V to +36 V, C_L = 15 pF, R_{PULLUP} = 5.1 kΩ, V_{CM} = V_S / 2, and V_S = V_{PULLUP} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pHL}	Propagation delay time, high-to-low	Input overdrive = 100 mV		460		ns
t_{pLH}	Propagation delay time, low-to-high	Input overdrive = 100 mV		560		ns
t_R	Rise time	Input overdrive = 100 mV		365		ns
t_F	Fall time	Input overdrive = 100 mV		240		ns

7.7 Typical Characteristics

at T_A = 25°C, V_S = 5 V, R_{PULLUP} = 5.1 kΩ, and input overdrive = 100 mV (unless otherwise noted)

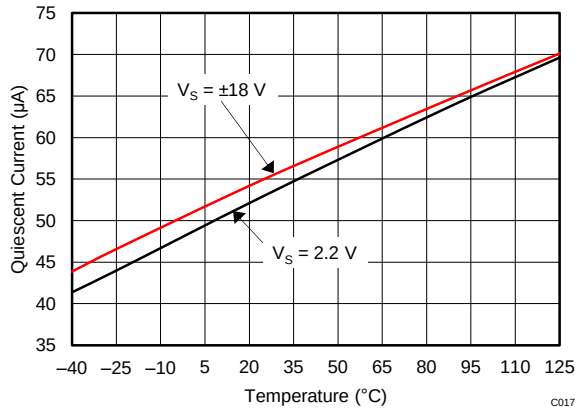


Figure 1. Quiescent Current vs Temperature

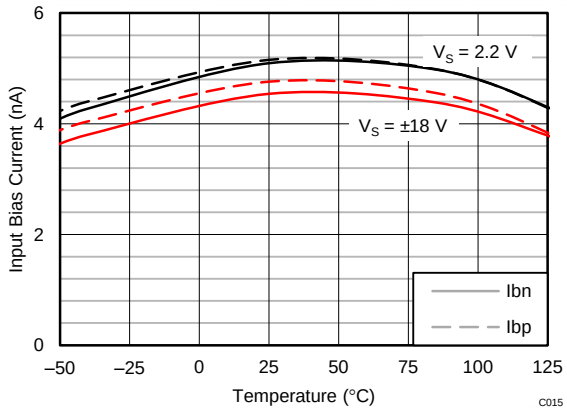


Figure 2. Input Bias Current vs Temperature

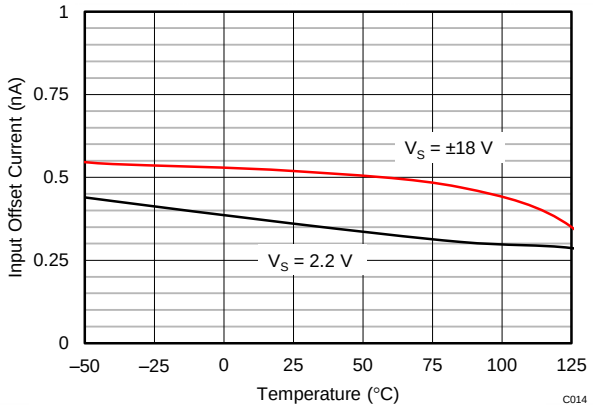


Figure 3. Input Offset Current vs Temperature

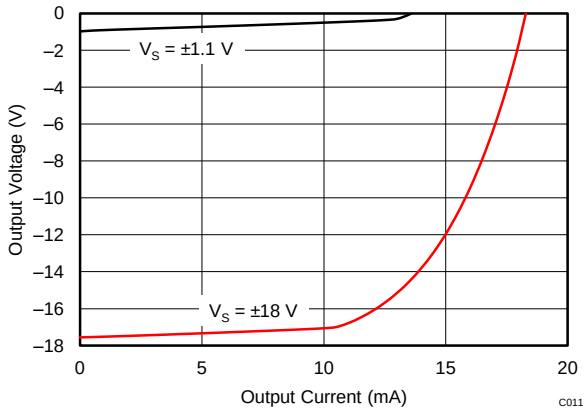
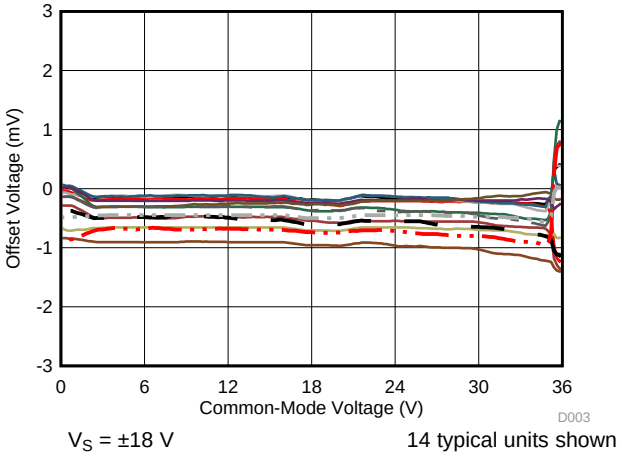
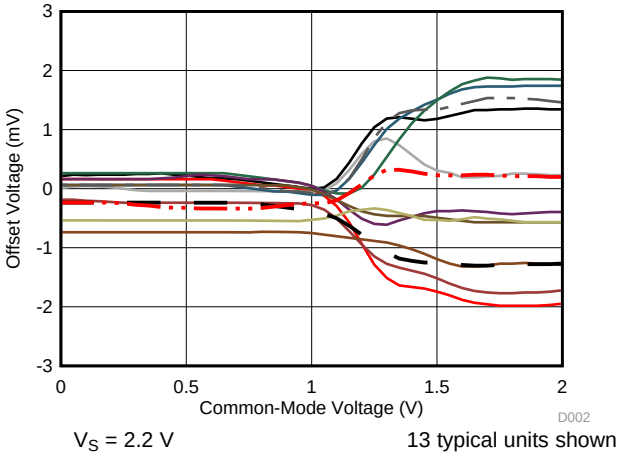


Figure 4. Output Voltage vs Output Current



V_S = ±18 V 14 typical units shown

Figure 5. Offset Voltage vs Common-Mode Voltage

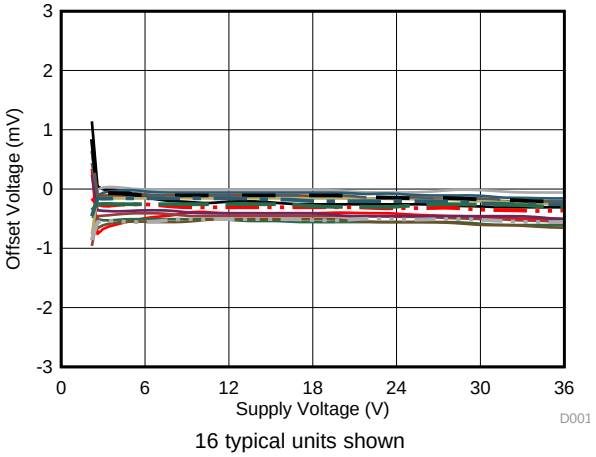


V_S = 2.2 V 13 typical units shown

Figure 6. Offset Voltage vs Common-Mode Voltage

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, R_{PULLUP} = 5.1 kΩ, and input overdrive = 100 mV (unless otherwise noted)



16 typical units shown

Figure 7. Offset Voltage vs Supply Voltage

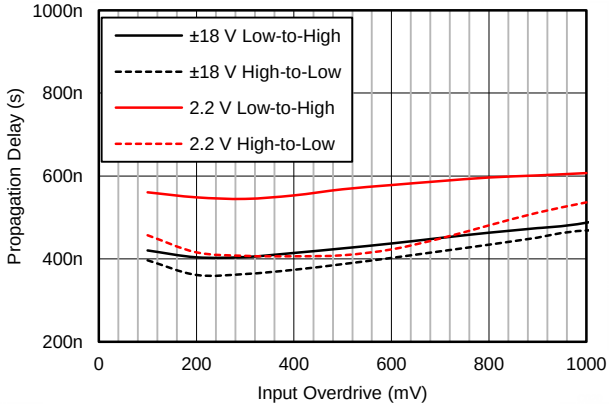


Figure 8. Propagation Delay vs Input Overdrive

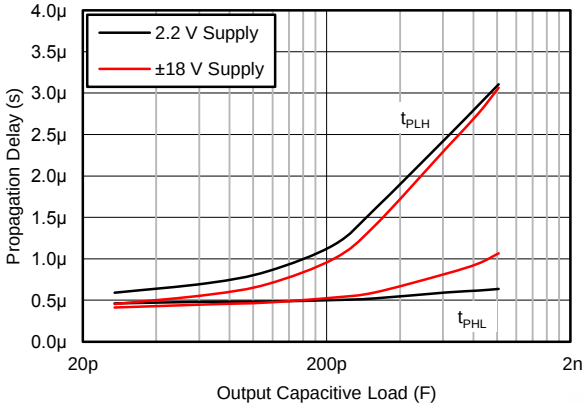
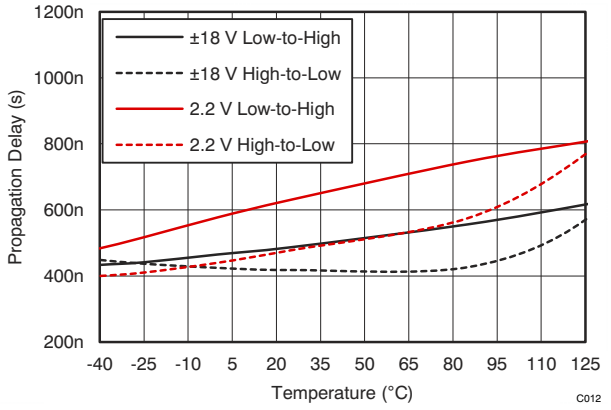
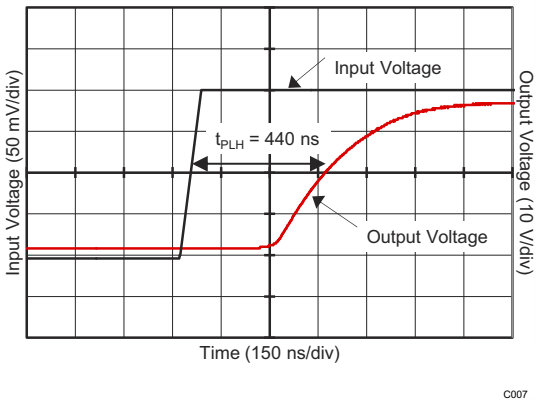


Figure 9. Propagation Delay vs Capacitive Load



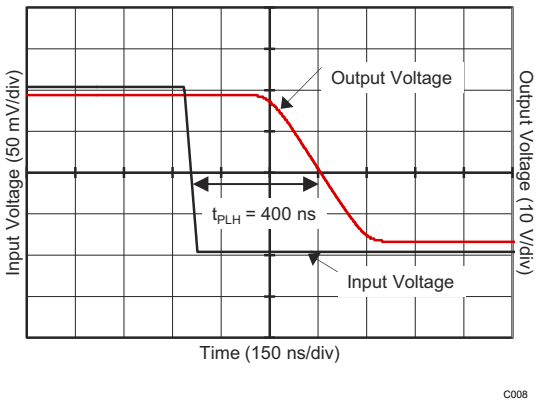
V_{OD} = 100 mV

Figure 10. Propagation Delay vs Temperature



V_S = 36 V Overdrive = 100 mV

Figure 11. Propagation Delay (T_{pLH})

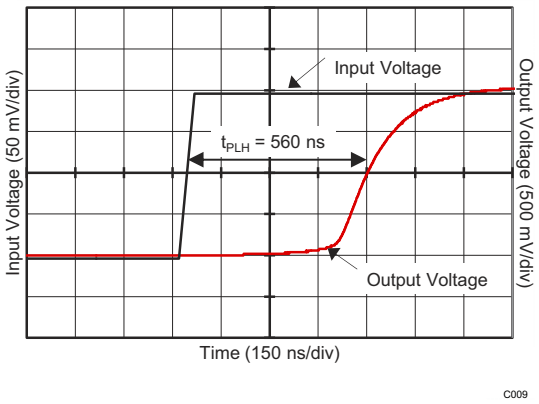


V_S = 36 V Overdrive = 100 mV

Figure 12. Propagation Delay (T_{pHL})

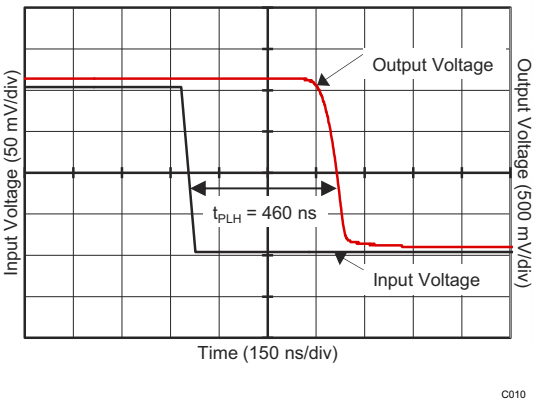
Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, R_{PULLUP} = 5.1 kΩ, and input overdrive = 100 mV (unless otherwise noted)



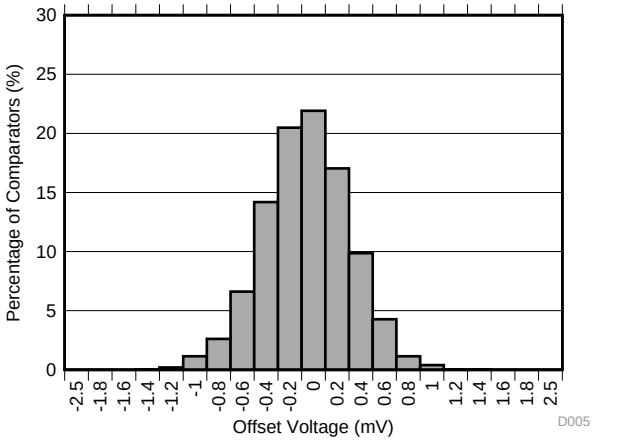
V_S = 2.2 V Overdrive = 100 mV

Figure 13. Propagation Delay (T_{pLH})



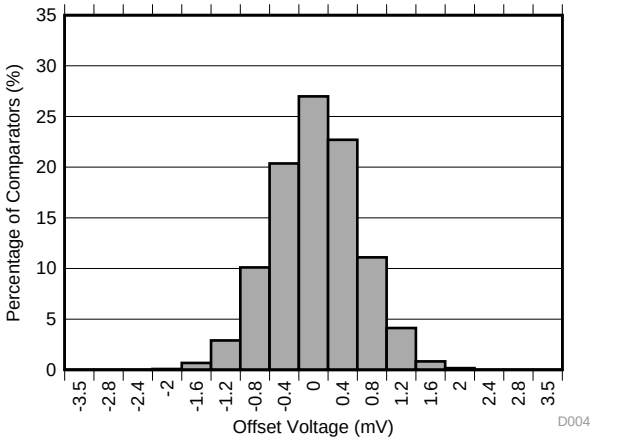
V_S = 2.2 V Overdrive = 100 mV

Figure 14. Propagation Delay (T_{pHL})



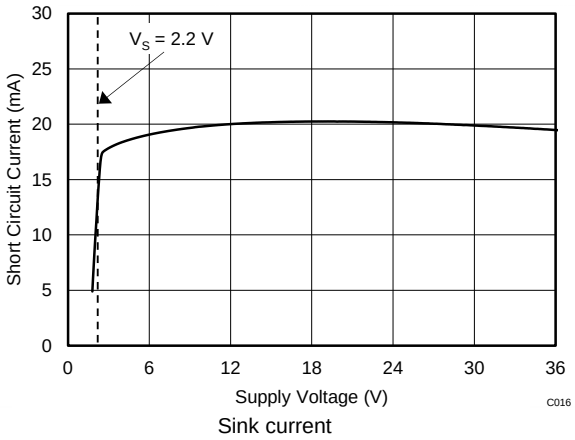
V_S = ±18 V Distribution taken from 2524 comparators

Figure 15. Offset Voltage Production Distribution



V_S = 2.2 V Distribution taken from 2524 comparators

Figure 16. Offset Voltage Production Distribution



Sink current

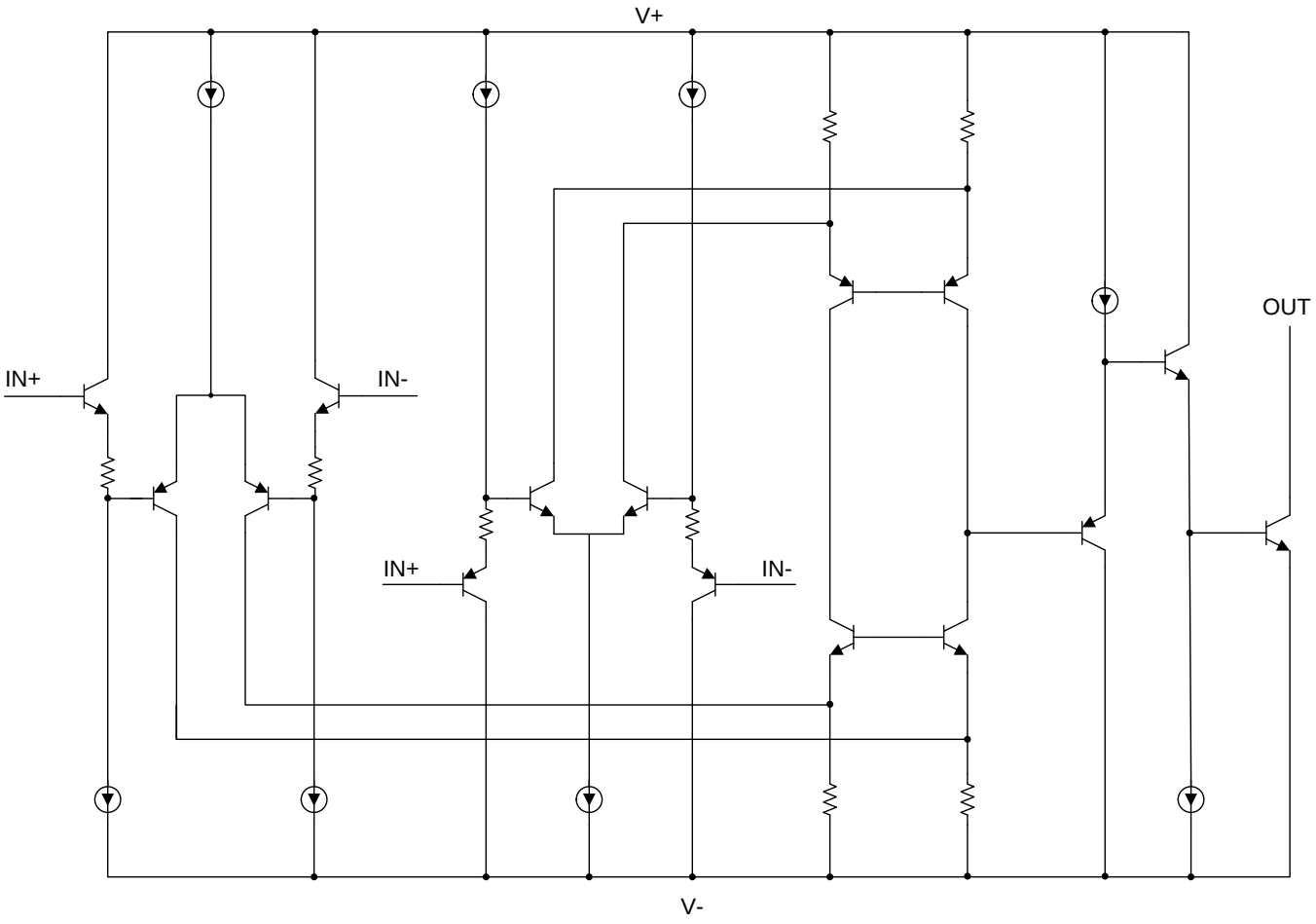
Figure 17. Short-Circuit Current vs Supply Voltage

8 Detailed Description

8.1 Overview

The TLV170x-Q1 comparator features rail-to-rail input and output on supply voltages as high as 36 V. The rail-to-rail input stage enables detection of signals close to the supply and ground. The open-collector configuration allows the device to be used in wired-OR configurations, such as a window comparator. A low supply current of 55 μA per channel with small, space-saving packages, makes these comparators versatile for use in a wide range of applications, from portable to industrial.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Comparator Inputs

The TLV170x-Q1 device is a rail-to-rail input comparator, with an input common-mode range that includes the supply rails. The TLV170x-Q1 device is designed to prevent phase inversion when the input pins exceed the supply voltage. Figure 18 shows the TLV170x-Q1 device response when input voltages exceed the supply, resulting in no phase inversion.

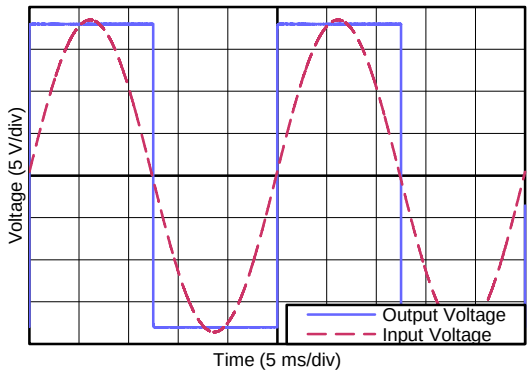


Figure 18. No Phase Inversion: Comparator Response to Input Voltage (Propagation Delay Included)

8.4 Device Functional Modes

8.4.1 Setting Reference Voltage

Using a stable reference is important when setting the transition point for the TLV170x-Q1 device. The REF3333, as shown in Figure 19, provides a 3.3-V reference voltage with low drift and only 3.9 μA of quiescent current.

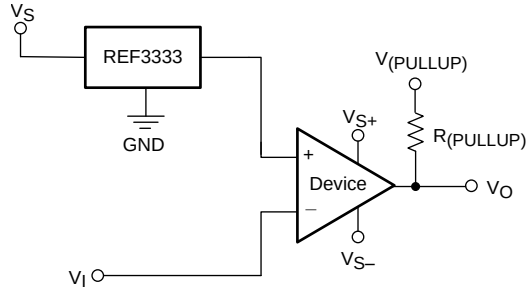


Figure 19. Reference Voltage for the TLV170x-Q1

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TLV170x-Q1 device can be used in a wide variety of applications, such as zero crossing detectors, window comparators, over and undervoltage detectors, and high-side voltage sense circuits.

9.2 Typical Application

Comparators are used to differentiate between two different signal levels. For example, a comparator differentiates between an overtemperature and normal-temperature condition. However, noise or signal variation at the comparison threshold causes multiple transitions. This application example sets upper and lower hysteresis thresholds to eliminate the multiple transitions caused by noise.

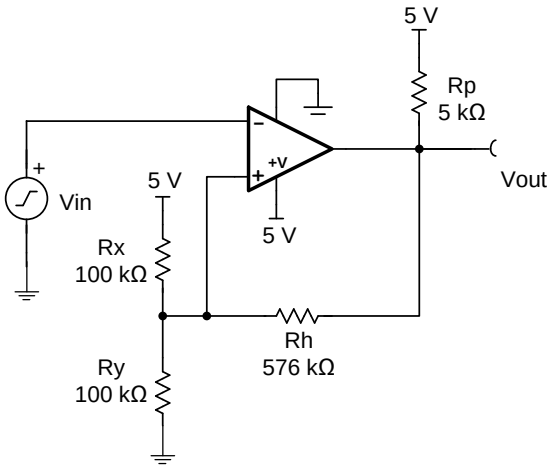


Figure 20. Comparator Schematic With Hysteresis

9.2.1 Design Requirements

The design requirements are as follows:

- Supply voltage: 5 V
- Input: 0 V to 5 V
- Lower threshold (VL) = 2.3 V ±0.1 V
- Upper threshold (VH) = 2.7 V ±0.1 V
- VH – VL = 2.4 V ±0.1 V
- Low-power consumption

Typical Application (continued)

9.2.2 Detailed Design Procedure

Make a small change to the comparator circuit to add hysteresis. Hysteresis uses two different threshold voltages to avoid the multiple transitions introduced in the previous circuit. The input signal must exceed the upper threshold (VH) to transition low, or below the lower threshold (VL) to transition high.

Figure 20 illustrates hysteresis on a comparator. Resistor Rh sets the hysteresis level. An open-collector output stage requires a pullup resistor (Rp). The pullup resistor creates a voltage divider at the comparator output that introduces an error when the output is at logic high. This error can be minimized if Rh > 100 Rp.

When the output is at a logic high (5 V), Rh is in parallel with Rx (ignoring Rp). This configuration drives more current into Ry, and raises the threshold voltage (VH) to 2.7 V. The input signal must drive above VH = 2.7 V to cause the output to transition to logic low (0 V).

When the output is at logic low (0 V), Rh is in parallel with Ry. This configuration reduces the current into Ry, and reduces the threshold voltage to 2.3 V. The input signal must drive below VL = 2.3 V to cause the output to transition to logic high (5 V).

For more details on this design and other alternative devices that can be used in place of the TLV1702, refer to Precision Design TIPD144, *Comparator with Hysteresis Reference Design*.

9.2.3 Application Curve

Figure 21 shows the upper and lower thresholds for hysteresis. The upper threshold is 2.76 V and the lower threshold is 2.34 V, both of which are close to the design target.

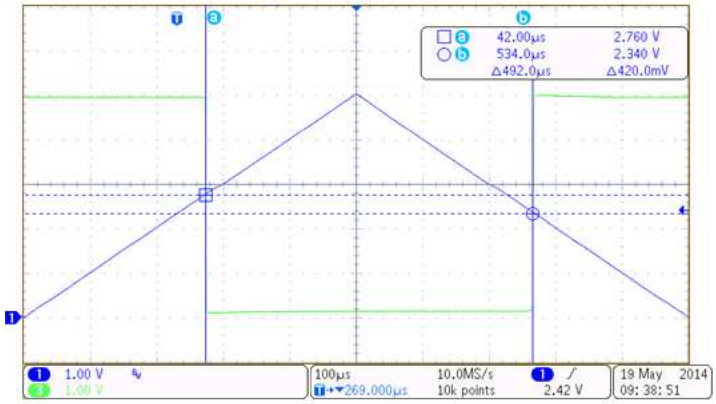


Figure 21. TLV1701 Upper and Lower Threshold With Hysteresis

10 Power Supply Recommendations

The TLV170x-Q1 device is specified for operation from 2.2 V to 36 V (±1.1 to ±18 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

CAUTION

Supply voltages larger than 40 V can permanently damage the device; see the *Absolute Maximum Ratings*.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement; see the *Layout Guidelines* section.

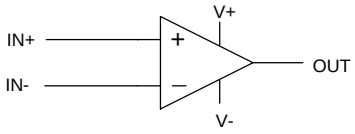
11 Layout

11.1 Layout Guidelines

Comparators are very sensitive to input noise. For best results, maintain the following layout guidelines:

- Use a printed-circuit board (PCB) with a good, unbroken low-inductance ground plane. Proper grounding (use of ground plane) helps maintain specified performance of the TLV170x-Q1 device.
- To minimize supply noise, place a decoupling capacitor (0.1-μF ceramic, surface-mount capacitor) as close as possible to V_S as shown in Figure 22.
- On the inputs and the output, keep lead lengths as short as possible to avoid unwanted parasitic feedback around the comparator. Keep inputs away from the output.
- Solder the device directly to the PCB rather than using a socket.
- For slow-moving input signals, take care to prevent parasitic feedback. A small capacitor (1000 pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes some degradation to propagation delay when the impedance is low. Run the topside ground plane between the output and inputs.
- Run the ground pin ground trace under the device up to the bypass capacitor, shielding the inputs from the outputs.

11.2 Layout Example



(Schematic Representation)

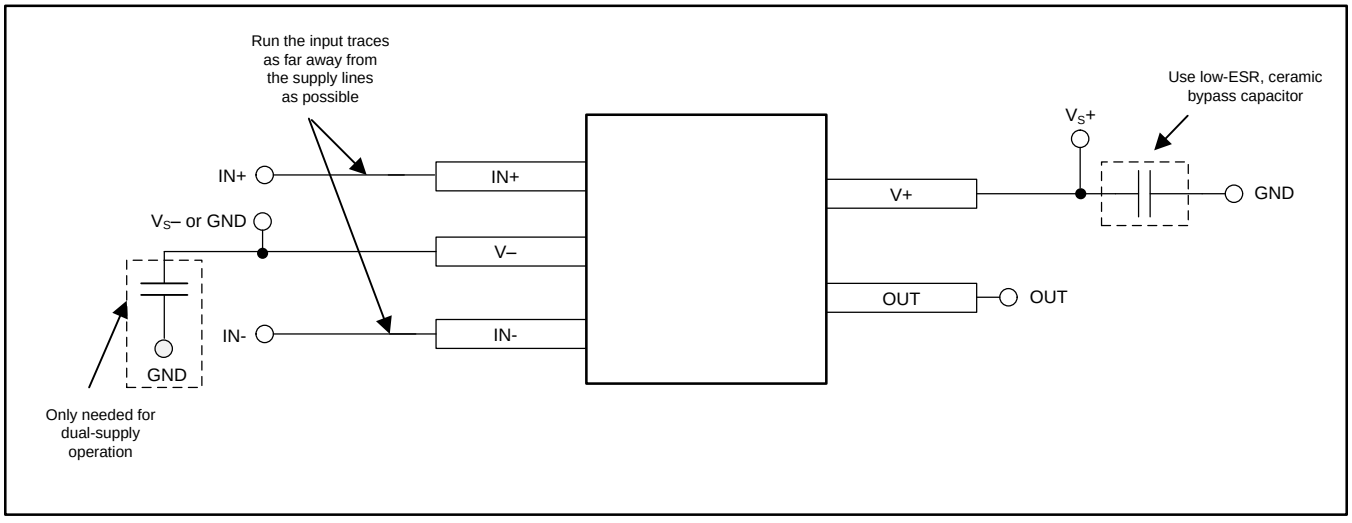


Figure 22. Comparator Board Layout

12 デバイスおよびドキュメントのサポート

12.1 ドキュメントのサポート

12.1.1 関連資料

関連資料については、以下を参照してください。

- 『Precision Design、ヒステリシス付きコンパレータのリファレンス・デザイン』、TIDU020
- 『REF33xx 3.9μA、SC70-3、SOT-23-3、UQFN-8、ドリフト30ppm/℃電圧リファレンス』、SBOS392

12.2 関連リンク

表 2 に、クイック・アクセス・リンクの一覧を示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 2. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
TLV1701-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TLV1702-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TLV1704-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

12.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E（Engineer-to-Engineer）コミュニティ。エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。***

設計サポート ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

12.5 商標

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV1701AQDCKRQ1	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	1FG
TLV1701AQDCKRQ1.B	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1FG
TLV1701QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1701
TLV1701QDBVRQ1.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1701
TLV1702AQDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1702Q
TLV1702AQDGKRQ1.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1702Q
TLV1704AQPWRQ1	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T1704Q1
TLV1704AQPWRQ1.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T1704Q1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV1701-Q1, TLV1702-Q1, TLV1704-Q1 :

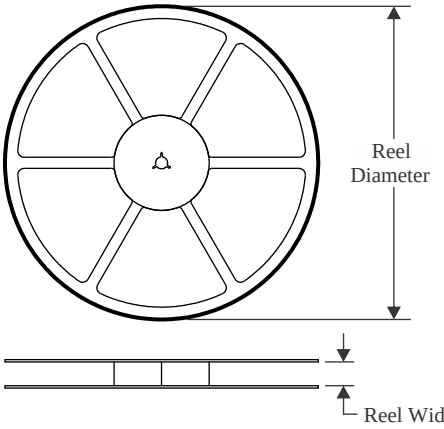
- Catalog : TLV1701, TLV1702, TLV1704

NOTE: Qualified Version Definitions:

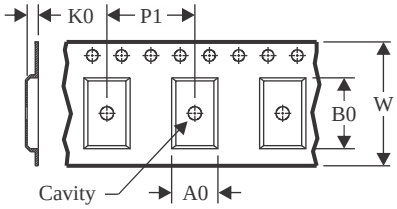
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

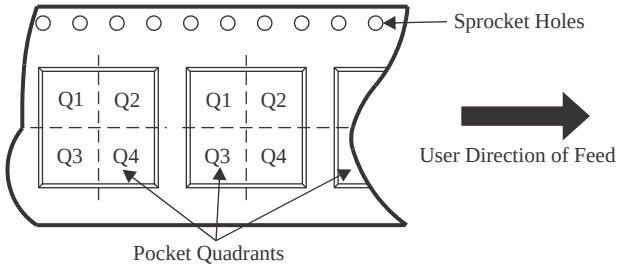


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

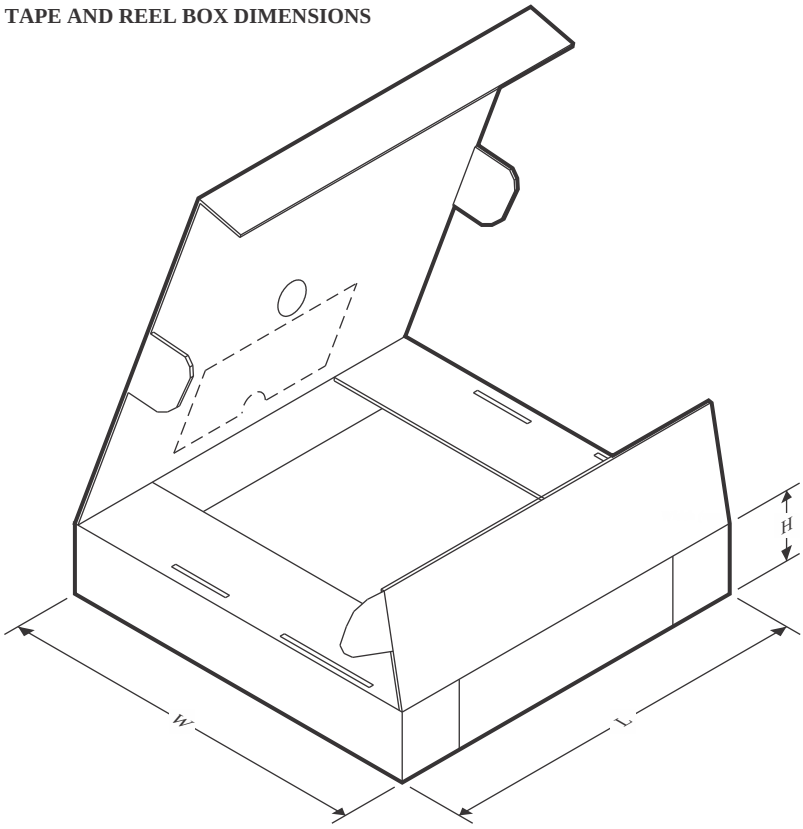
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV1701AQDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV1701QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV1702AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV1704AQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

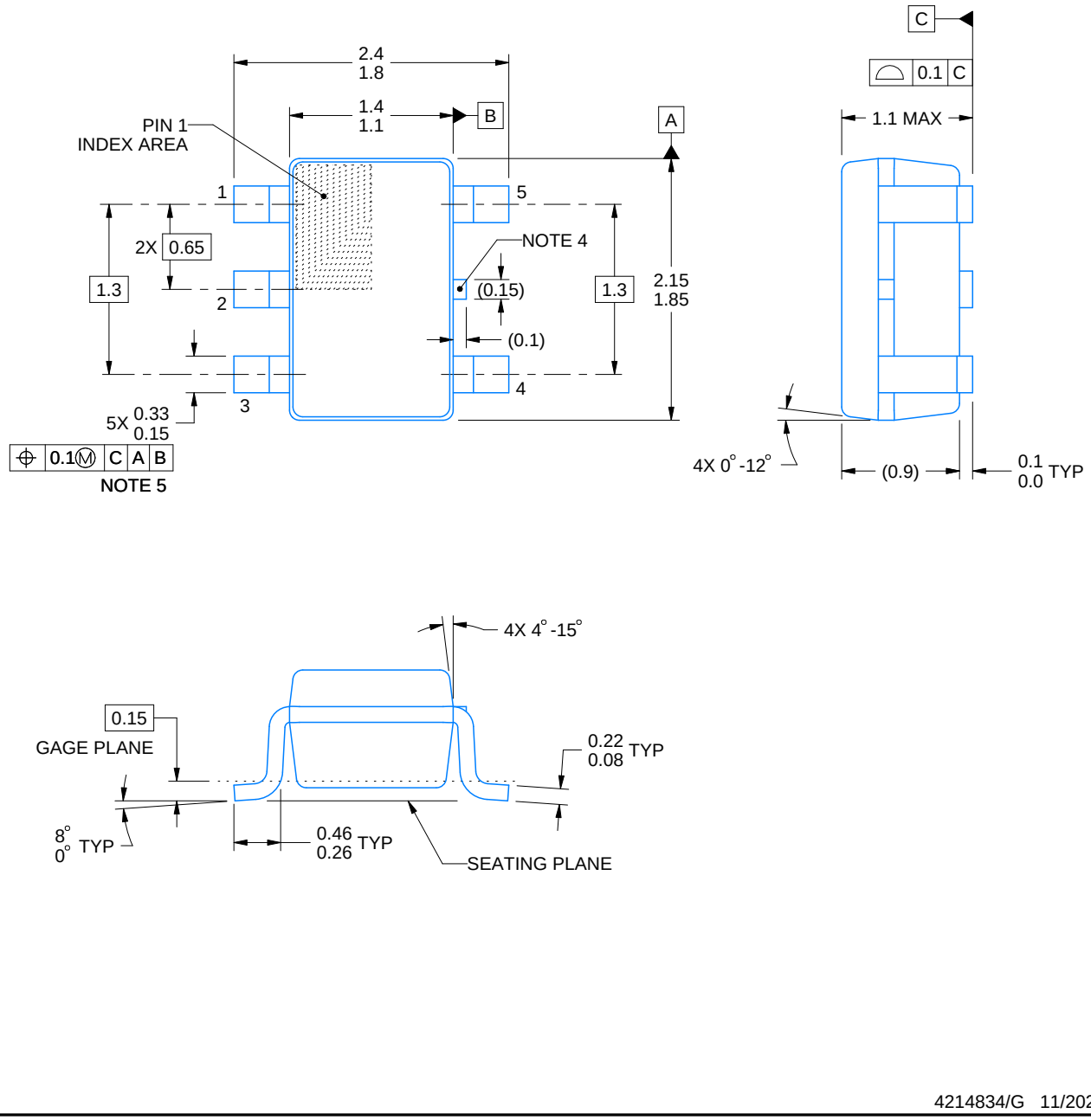
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV1701AQDCKRQ1	SC70	DCK	5	3000	190.0	190.0	30.0
TLV1701QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV1702AQDGKRQ1	VSSOP	DGK	8	2500	353.0	353.0	32.0
TLV1704AQPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

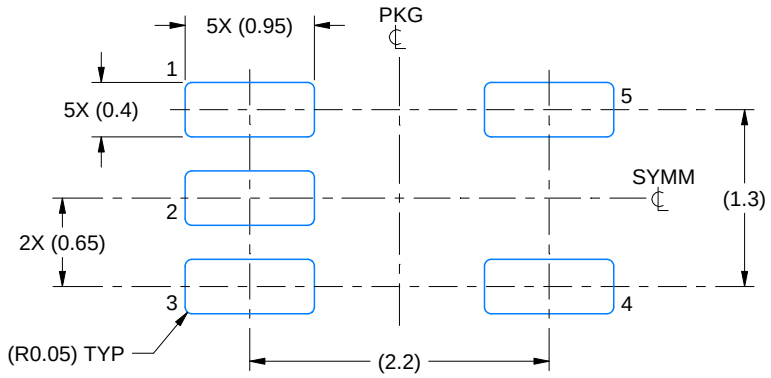
SMALL OUTLINE TRANSISTOR



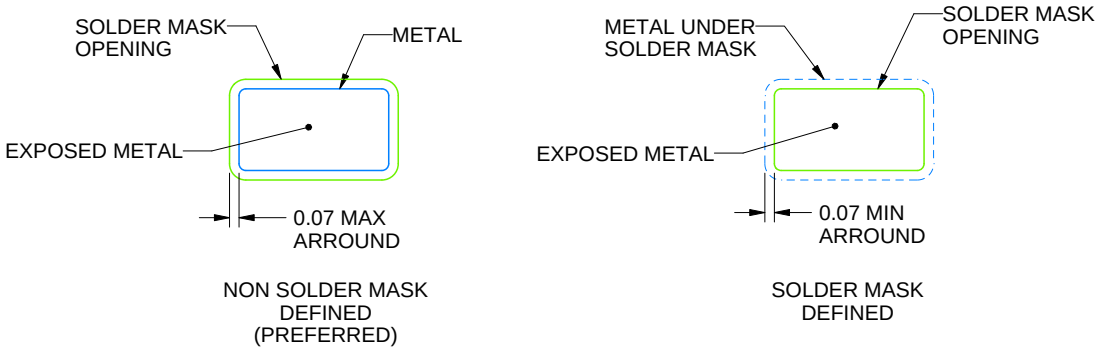
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

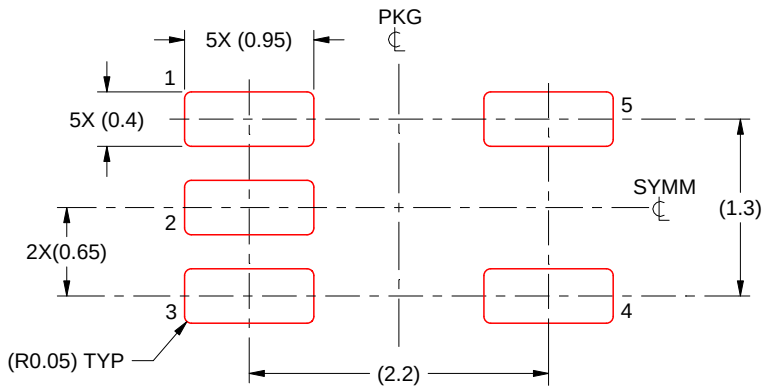


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

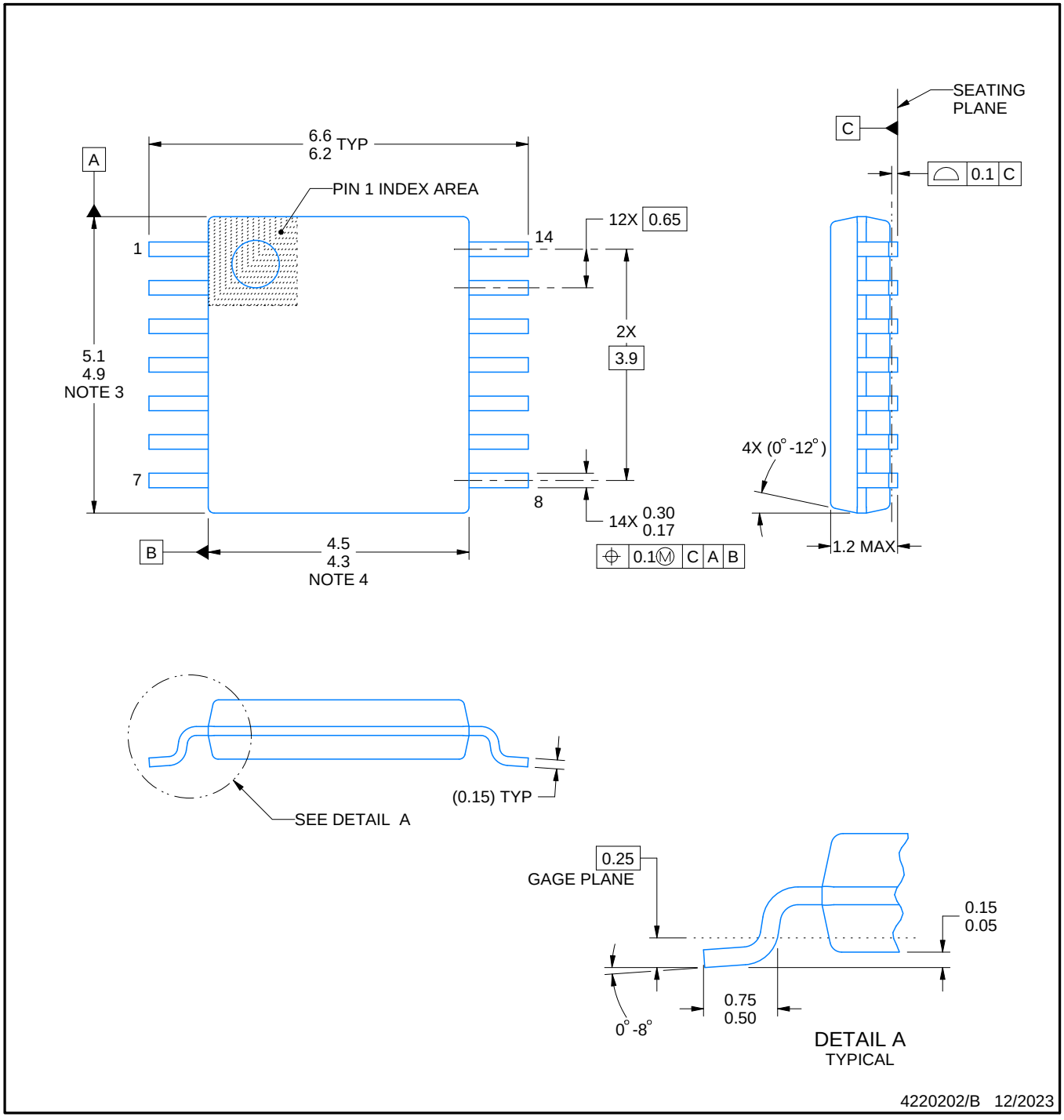
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

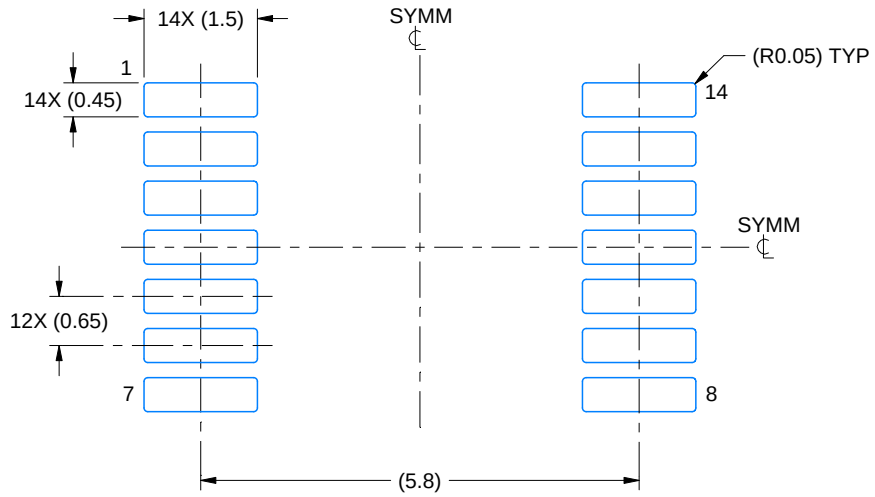
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

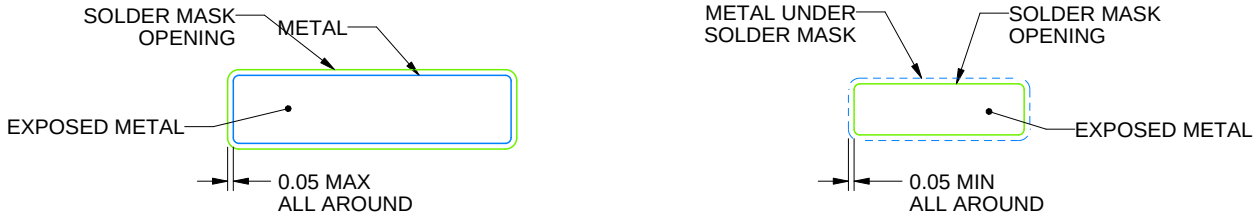


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

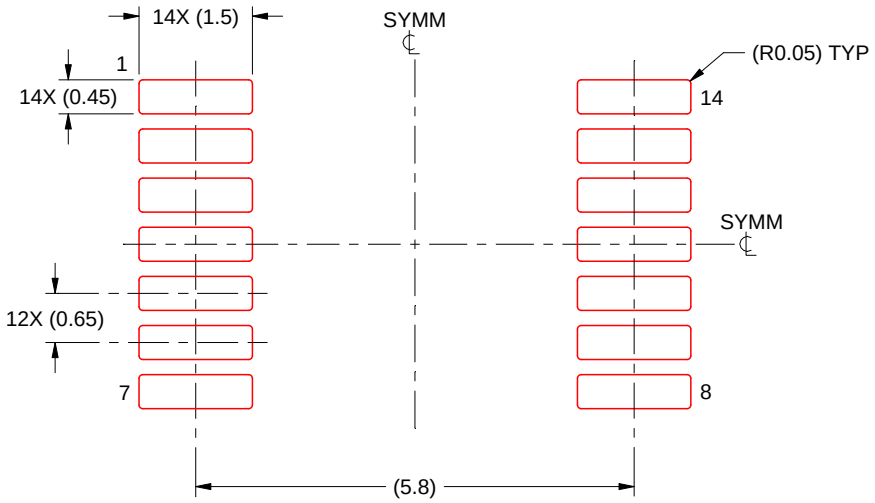


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

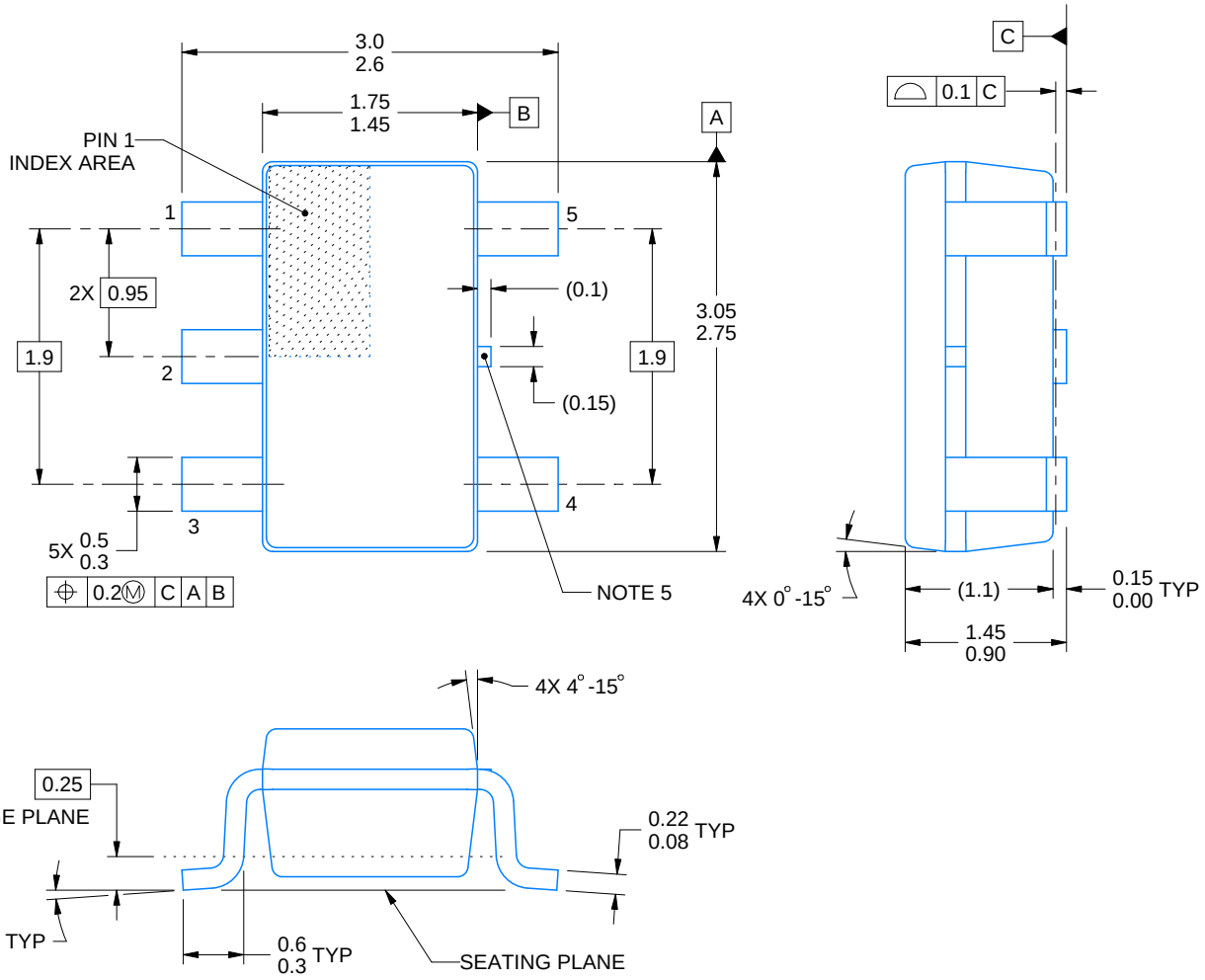
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

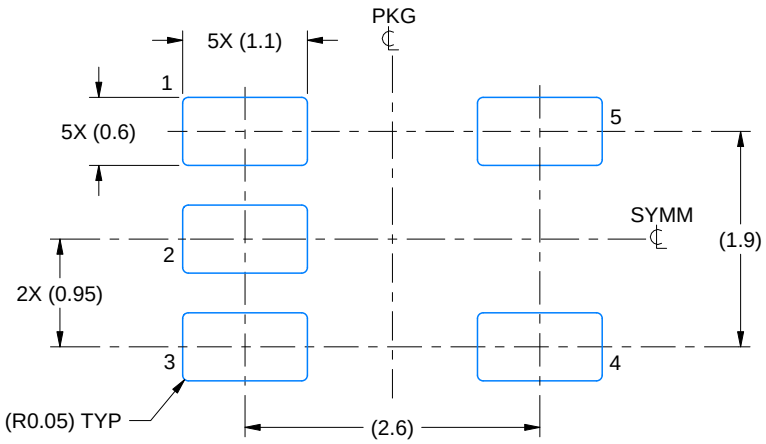
SMALL OUTLINE TRANSISTOR



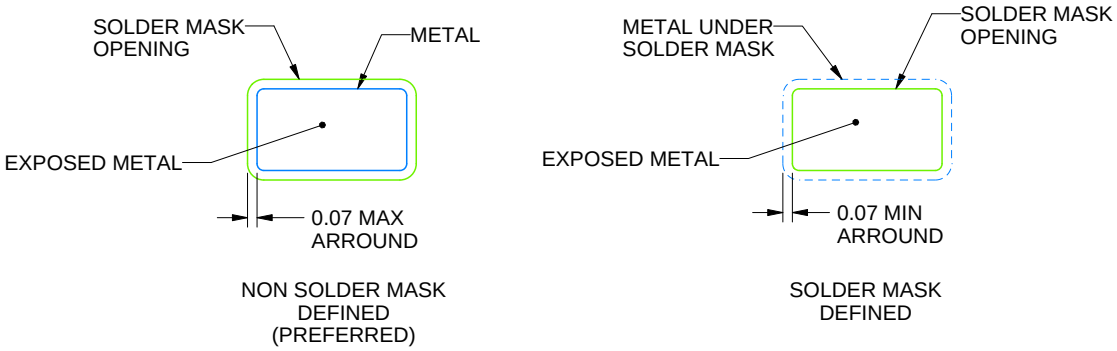
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

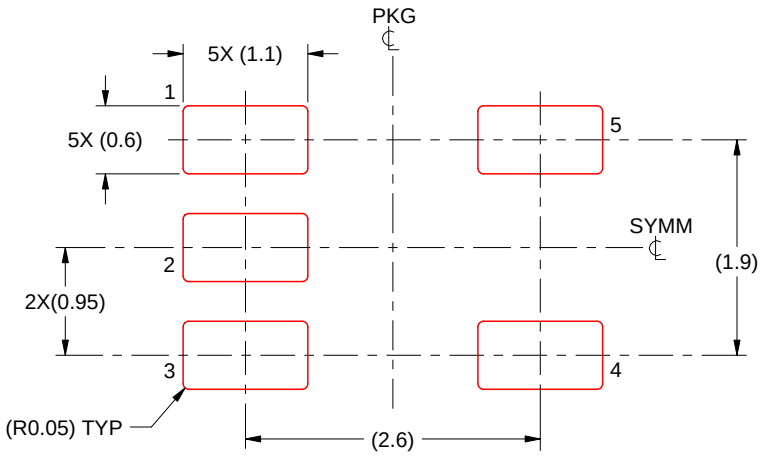


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

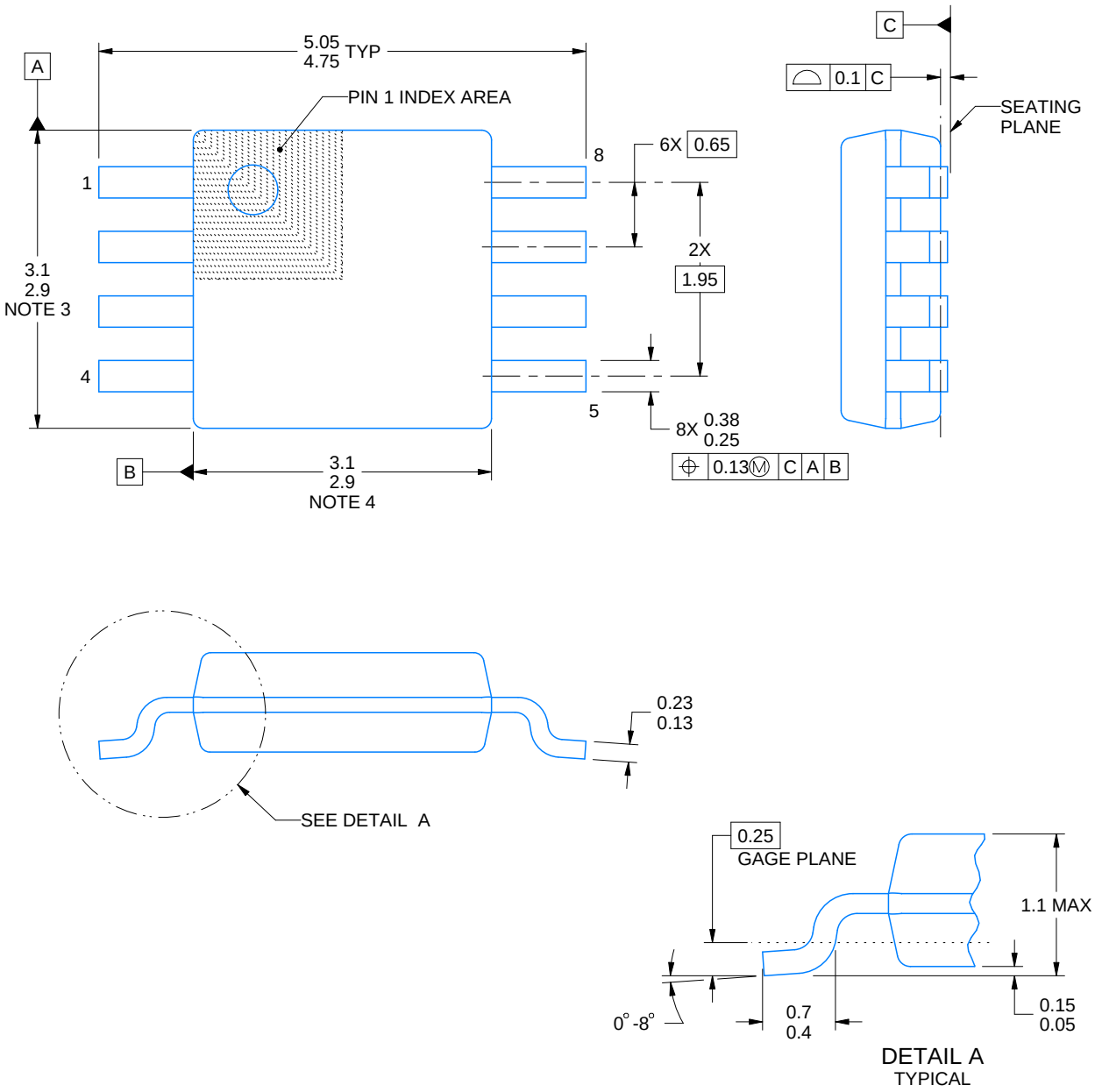
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

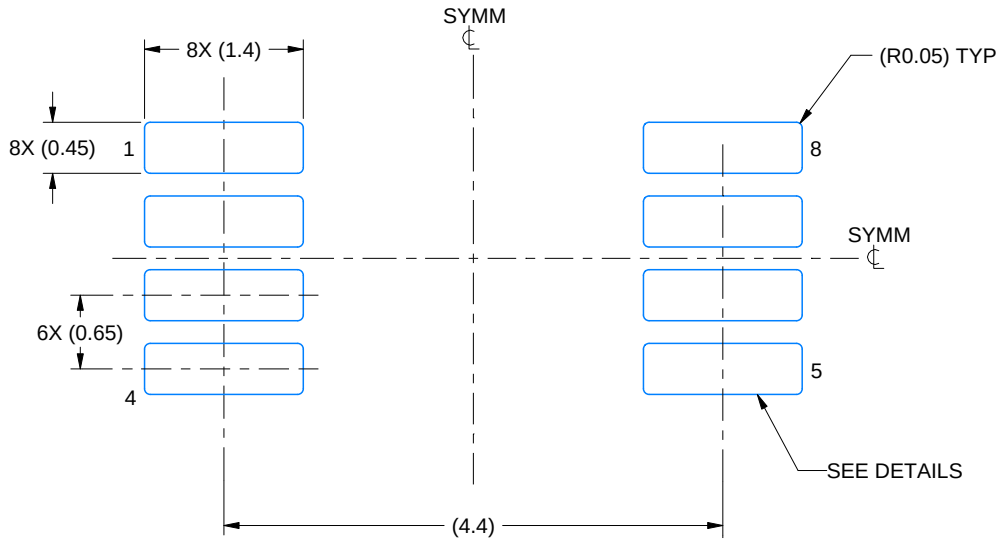
SMALL OUTLINE PACKAGE



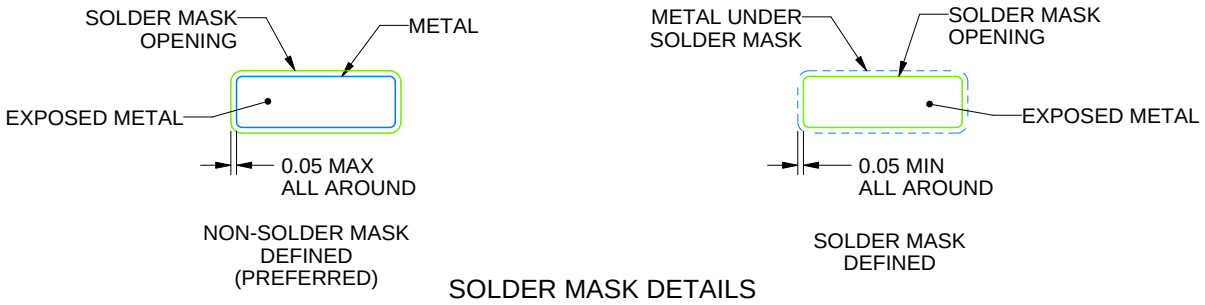
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

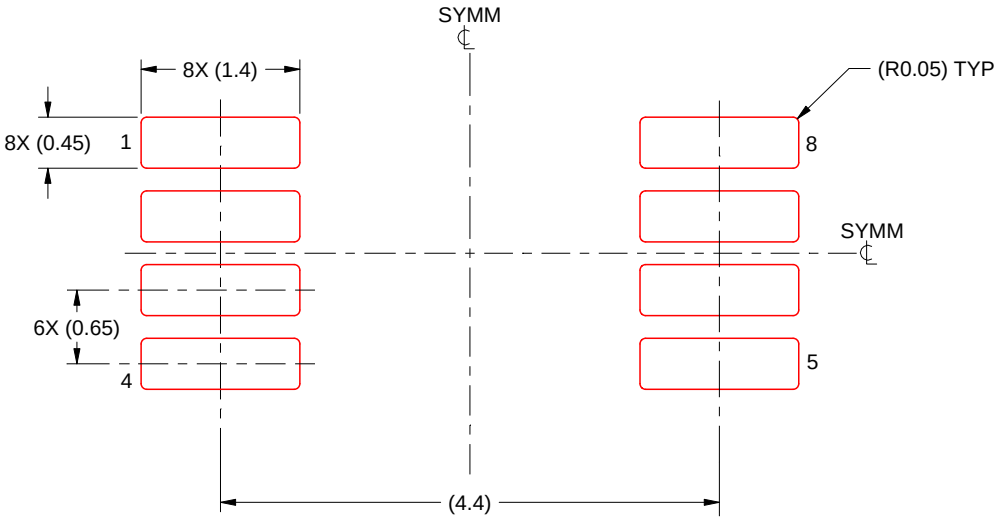


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月