TEXAS INSTRUMENTS

TLV376, TLV2376, TLV4376

JAJSCL1 – OCTOBER 2016

TLVx376 低オフセットおよびドリフト、低ノイズ、高精度オペアンプ、コスト制約の厳しいシステム用

1 特長

- 低ノイズ: 1kHz時に8nV/√Hz
- 0.1Hz～10Hzのノイズ: 1.6μV_{PP}
- 静止電流: 815μA (標準値)
- 低いオフセット電圧(標準値)
  - シングルおよびデュアル・バージョン: 40μV
  - クワッド・バージョン: 50μV
- ゲイン帯域幅積: 5.5MHz
- レール・ツー・レールの入出力
- 単一電源動作
- 電源電圧: 2.2V～5.5V
- 業界標準パッケージ:
  - SOT-23、SOIC、VSSOP、TSSOP

2 アプリケーション

- 太陽光インバータ
- 医療用計測機器
- ADCバッファ
- ハンドヘルド・テスト機器
- アクティブ・フィルタリング
- センサ・コンディショニング

3 概要

TLVx376ファミリは新世代の低ノイズ・オペアンプで、e-trim™を搭載し、非常に優れたDC精度とAC特性を実現しています。レール・ツー・レールの入力と出力、低オフセット(最大125μV)、低ノイズ(8nV/√Hz)、静止電流1.2mA (最大値)、5.5MHzの帯域幅と2V/μsの高速なスルー・レートから、このファミリのデバイスは各種の高精度な携帯アプリケーションに非常に魅力的な選択肢です。さらに、これらのデバイスは電源電圧範囲が広く、PSRRが非常に優れているため、バッテリから直接レギュレーションなしで動作するアプリケーションにも理想的です。

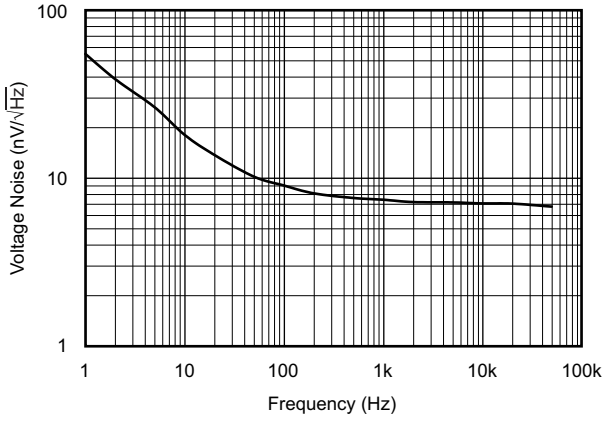
TLV376 (シングル・バージョン)はSOT-23-5およびSOIC-8パッケージで供給されます。TLV2376 (デュアル)はVSSOP-8およびSOIC-8パッケージで供給されます。TLV4376 (クワッド)は、TSSOP-14パッケージで供給されます。どのバージョンも、–40°C～+125°Cの動作が保証されています。

製品情報(1)

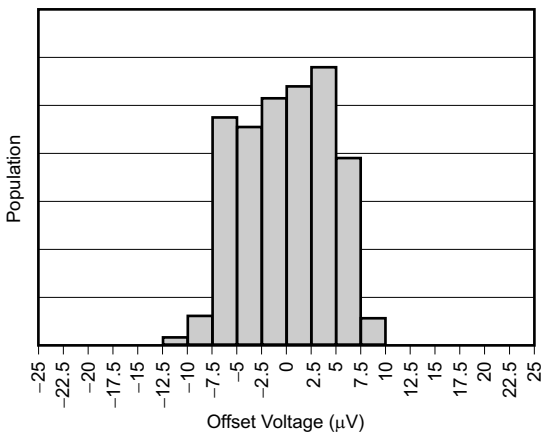
型番	パッケージ	本体サイズ(公称)
TLV376	SOIC (8)	4.90mm×3.91mm
	SOT-23 (5)	2.90mm×1.60mm
TLV2376	SOIC (8)	4.90mm×3.91mm
	VSSOP (8)	3.00mm×3.00mm
TLV4376	PW (14)	5.00mm×4.40mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。

INPUT VOLTAGE NOISE SPECTRAL DENSITY



OFFSET VOLTAGE PRODUCTION DISTRIBUTION



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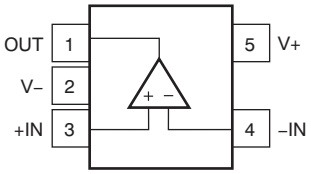
4 改訂履歴

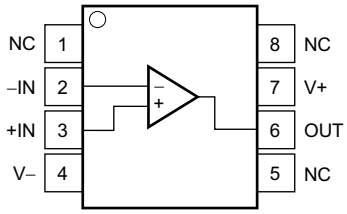
日付	改訂内容	注
2016年10月	*	初版

5 Pin Configuration and Functions

TLV376: DBV Package
5-Pin SOT23
Top View



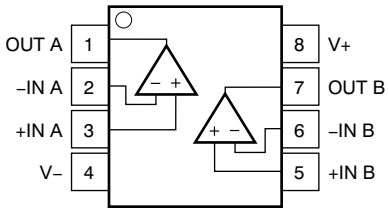
TLV376: D Package
8-Pin SOIC
Top View



Pin Functions: TLV376

PIN			I/O	DESCRIPTION
NAME	DBV	D		
–IN	4	2	I	Negative input signal
+IN	3	3	I	Positive input signal
NC	—	1, 5, 8	—	No connection
OUT	1	6	O	Output signal
V–	2	4	—	Negative supply voltage
V+	5	7	—	Positive supply voltage

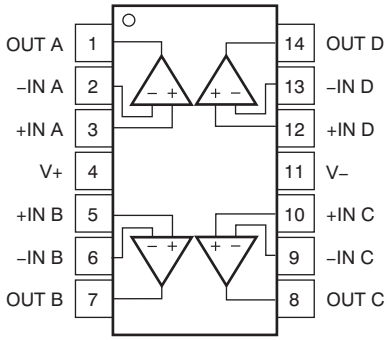
TLV2376: D and DGK Packages
8-Pin SOIC and 8-Pin VSSOP
Top View



Pin Functions: TLV2376

PIN		I/O	DESCRIPTION
NAME	D, DGK		
–IN A	2	I	Inverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN A	3	I	Noninverting input, channel A
+IN B	5	I	Noninverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V–	4	—	Negative supply voltage
V+	8	—	Positive supply voltage

TLV4376: PW Package
14-Pin TSSOP
Top View



Pin Functions: TLV4376

PIN		I/O	DESCRIPTION
NAME	PW		
–IN A	2	O	Inverting input, channel A
–IN B	6	O	Inverting input, channel B
–IN C	9	O	Inverting input, channel C
–IN D	13	O	Inverting input, channel D
+IN A	3	I	Noninverting input, channel A
+IN B	5	I	Noninverting input, channel B
+IN C	10	I	Noninverting input, channel C
+IN D	12	I	Noninverting input, channel D
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
OUT C	8	O	Output, channel C
OUT D	14	O	Output, channel D
V–	11	—	Negative supply voltage
V+	4	—	Positive supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply, V_S = (V+) – (V–)		7	V
	Signal input pin(2)	(V–) – 0.5	(V+) + 0.5	V
Current	Signal input pin(2)	–10	10	mA
	Output short-circuit(3)	Continuous		
Temperature	Specified, T_A	–40	125	°C
	Junction, T_J		150	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)	Single supply	2.2		5.5	V
	Dual supply	±1.1		±2.75	
T_A Specified temperature range		–40		125	°C

6.4 Thermal Information: TLV376

THERMAL METRIC(1)		TLV376		UNIT
		D (SOIC)	DBV (SOT-23)	
		8 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	100.1	273.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	42.4	126.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41.0	85.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.8	10.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	40.3	84.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Thermal Information: TLV2376

THERMAL METRIC(1)		TLV2376		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	111.1	171.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.7	63.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	51.7	92.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.5	9.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	51.2	91.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Thermal Information: TLV4376

THERMAL METRIC(1)		TLV4376	UNIT
		PW (TSSOP)	
		14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	107.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	51.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.7 Electrical Characteristics

at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	TLV376, TLV2376		40	100	µV
		TLV4376		50	125	
dV_{OS}/dT	Offset voltage vs temperature	T_A = –40°C to +125°C		1.0		µV/°C
PSRR	Power-supply rejection ratio	V_S = 2.2 V to 5.5 V, V_{CM} < (V+) – 1.3 V	84	110		dB
	Channel separation, dc	TLV2376, TLV4376		0.5		mV/V
INPUT BIAS CURRENT						
I_B	Input bias current			0.3		pA
		T_A = –40°C to +125°C		See *Typical Characteristics*		
I_{OS}	Input offset current			0.2		pA
NOISE						
	Input voltage noise	f = 0.1 Hz to 10 Hz		2.2		μV_{PP}
e_n	Input voltage noise density	f = 1 kHz		8.0		$nV/\sqrt{Hz}$
i_n	Input current noise	f = 1 kHz		2		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range		(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	(V–) < V_{CM} < (V+) – 1.3 V	72	88		dB
INPUT CAPACITANCE						
	Differential			6.5		pF
	Common-mode			13		pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	100 mV < V_O < (V+) – 100 mV, R_L = 2 kΩ	100	126		dB
FREQUENCY RESPONSE (C_L = 100 pF, V_S = 5.5 V)						
GBW	Gain-bandwidth product			5.5		MHz
SR	Slew rate	G = 1		2		V/µs
t_S	Settling time	To 0.1%, 2-V step , G = 1		1.6		µs
		To 0.01%, 2-V step , G = 1		2		
	Overload recovery time	V_{IN} × gain > V_S		0.33		µs
THD+N	Total harmonic distortion + noise	V_O = 1 V_{RMS}, G = 1, f = 1 kHz, R_L = 10 kΩ		0.0005%		
OUTPUT						
	Voltage output swing from rail	R_L = 10 kΩ		10	20	mV
I_{SC}	Short-circuit current	Sourcing		30		mA
		Sinking		–50		
C_{LOAD}	Capacitive load drive			See *Typical Characteristics*		
R_O	Open-loop output impedance			150		Ω
POWER SUPPLY						
V_S	Specified voltage range		2.2		5.5	V
	Operating voltage range			2 to 5.5		V
I_Q	Quiescent current per amplifier	I_O = 0 mA, V_S = 5.5 V, V_{CM} < (V+) – 1.3 V		815	1200	µA
TEMPERATURE						
	Specified range		–40		125	°C

6.8 Typical Characteristics

at T_A = 25°C, V_S = 5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

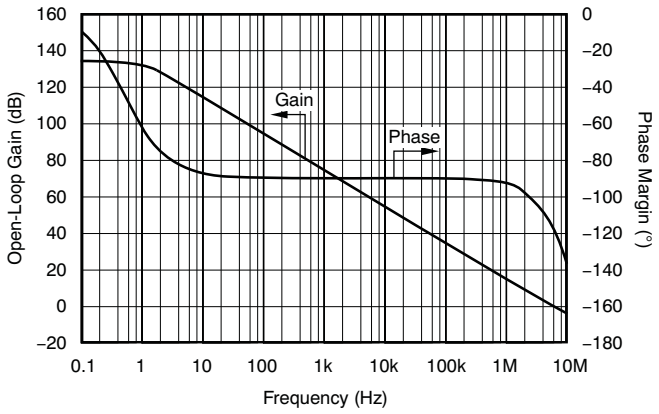


Figure 1. Open-Loop Gain and Phase vs Frequency

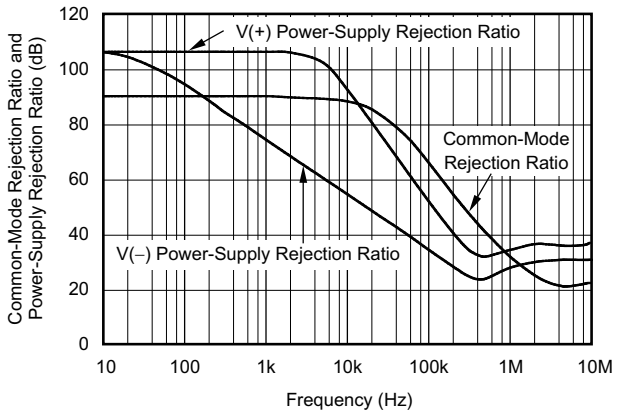


Figure 2. Power-Supply and Common-Mode Rejection Ratio vs Frequency

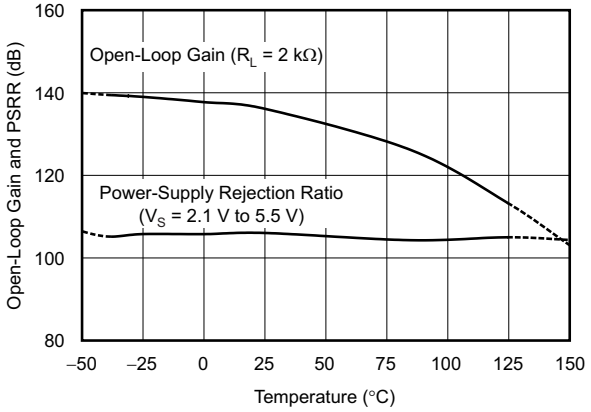


Figure 3. Open-Loop Gain and Power-Supply Rejection Ratio vs Temperature

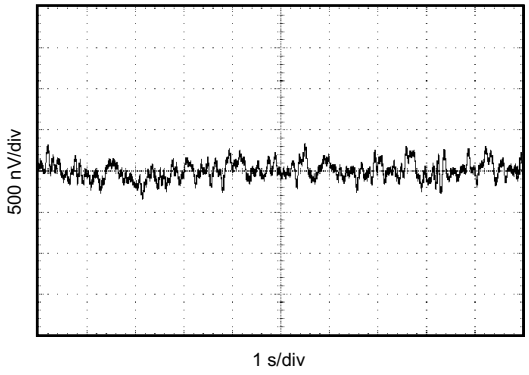


Figure 4. 0.1-Hz to 10-Hz Input Voltage Noise

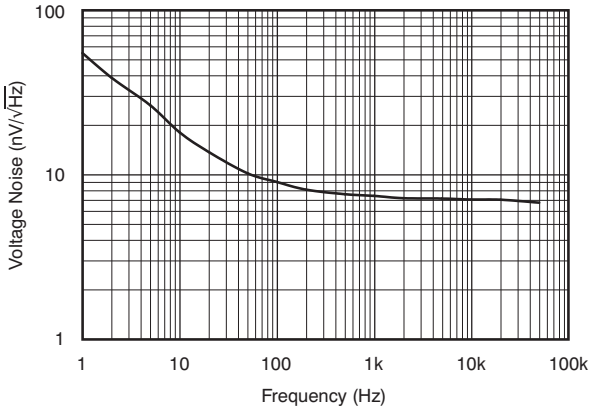
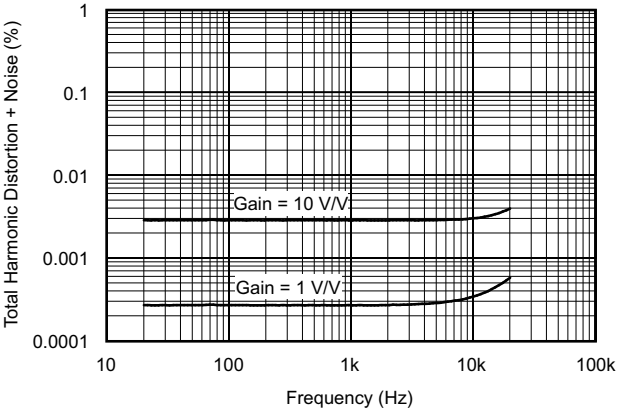


Figure 5. Input Voltage Noise Spectral Density



V_S = 5 V, V_{CM} = 2 V, V_{OUT} = 1 V_{RMS}

Figure 6. Total Harmonic Distortion + Noise vs Frequency

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

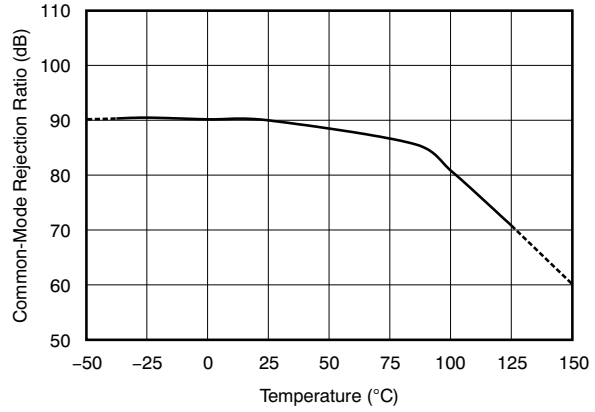


Figure 7. Common-Mode Rejection Ratio vs Temperature

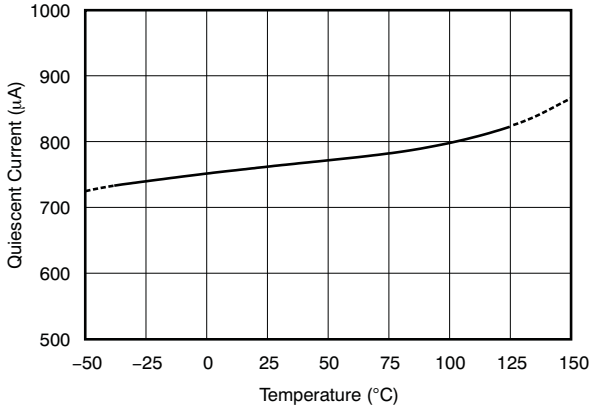


Figure 8. Quiescent Current vs Temperature

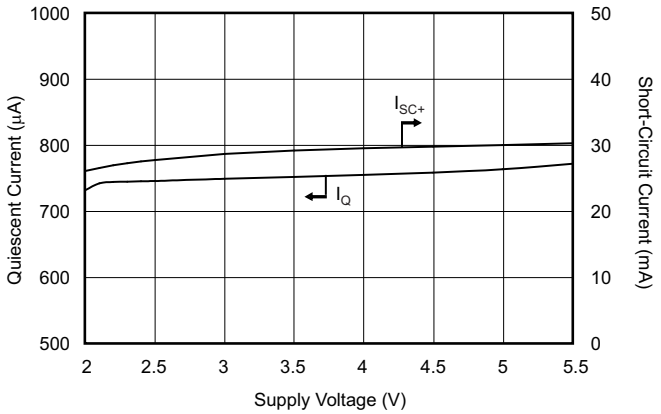


Figure 9. Quiescent and Short-Circuit Current vs Supply Voltage

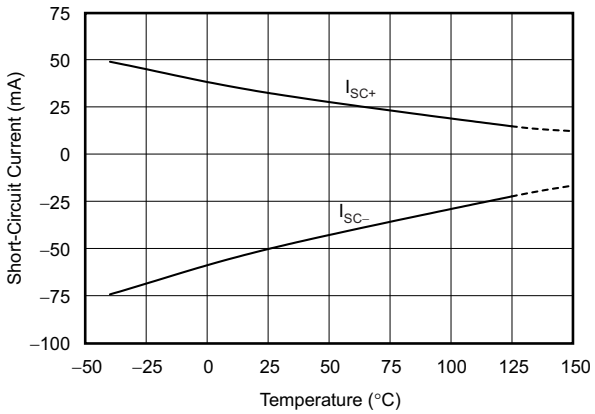


Figure 10. Short-Circuit Current vs Temperature

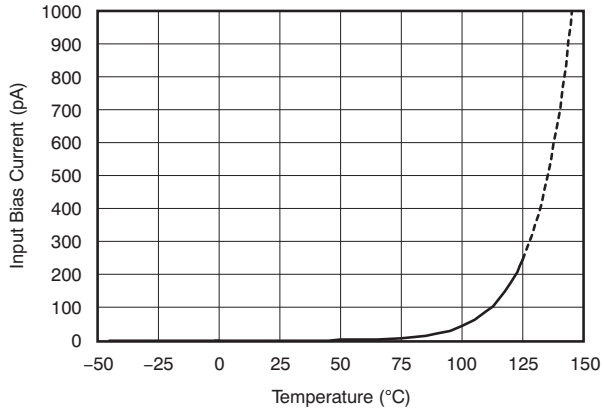


Figure 11. Input Bias Current vs Temperature

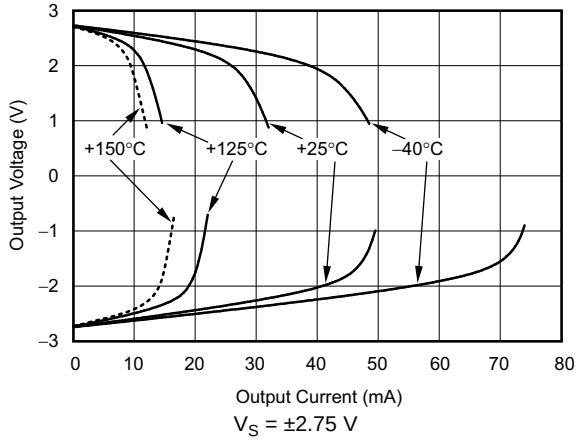


Figure 12. Output Voltage vs Output Current

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

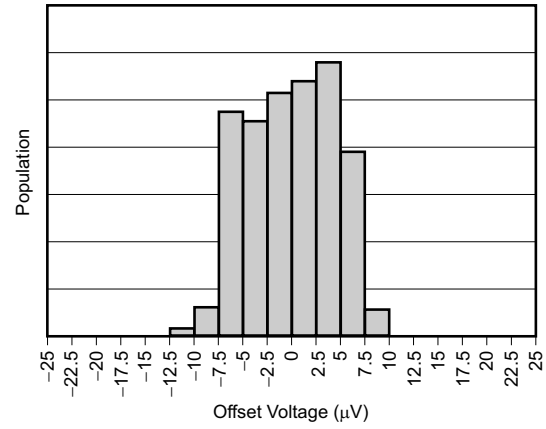


Figure 13. Offset Voltage Production Distribution Histogram

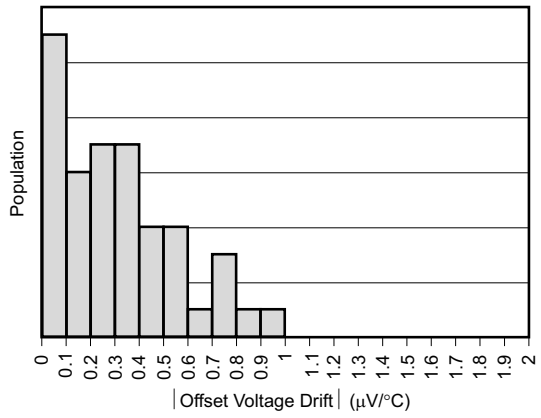


Figure 14. Offset Voltage Drift Production Distribution Histogram (–40°C to 125°C)

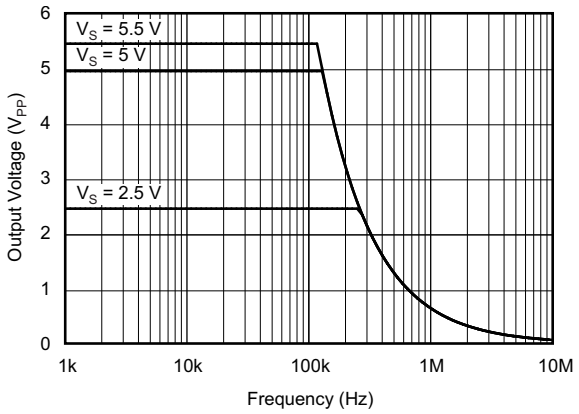


Figure 15. Maximum Output Voltage vs Frequency

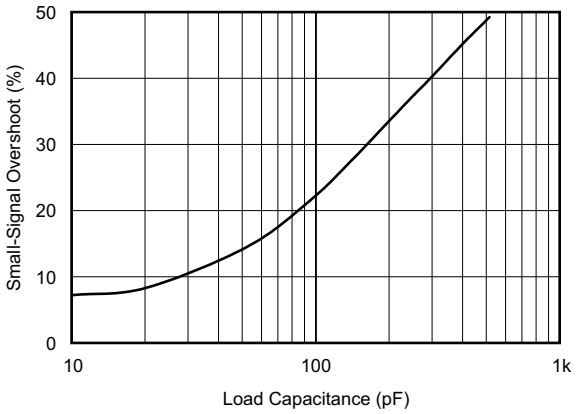
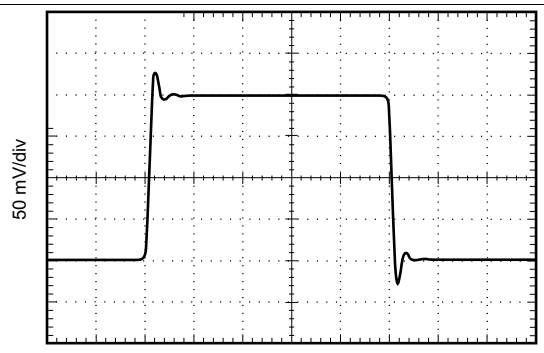
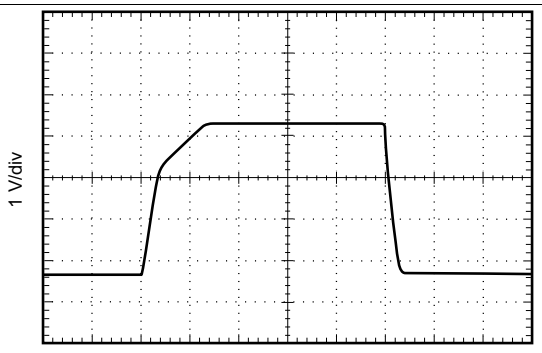


Figure 16. Small-Signal Overshoot vs Load Capacitance



G = +1 V/V, R_L = 10 kΩ, C_L = 50 pF

Figure 17. Small-Signal Pulse Response



G = +1 V/V, R_L = 2 kΩ, C_L = 50 pF

Figure 18. Large-Signal Pulse Response

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

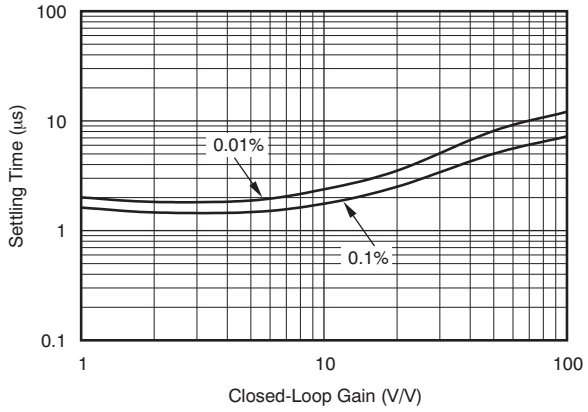


Figure 19. Settling Time vs Closed-Loop Gain

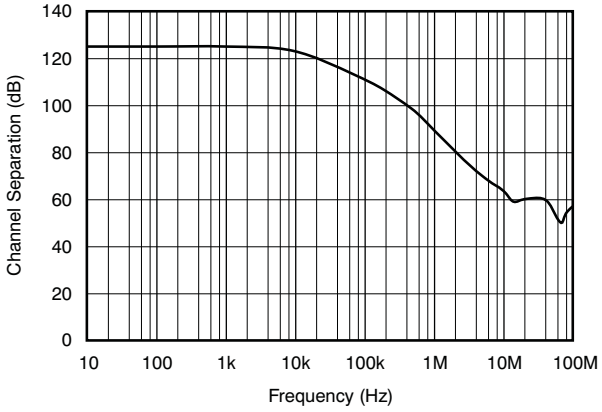


Figure 20. Channel Separation vs Frequency

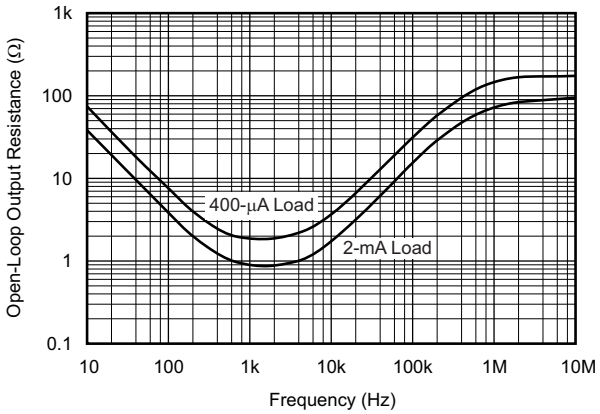


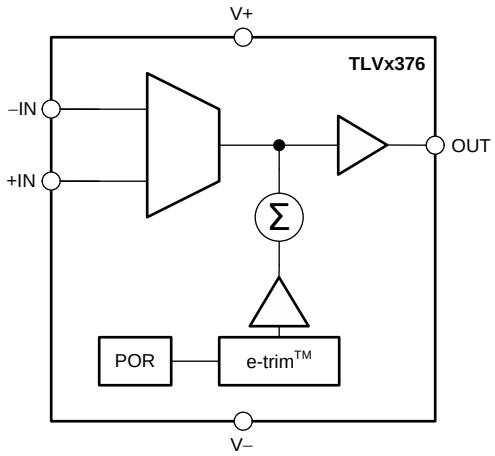
Figure 21. Open-Loop Output Resistance vs Frequency

7 Detailed Description

7.1 Overview

The TLVx376 family belongs to a new generation of low-noise operational amplifiers with e-trim™, giving customers outstanding dc precision and ac performance. Low noise, rail-to-rail input and output, and low offset, drawing a low quiescent current, make these devices ideal for a variety of precision and portable applications. In addition, this family of devices have a wide supply range with excellent PSRR, making the TLVx376 a suitable option for applications that are battery-powered without regulation.

7.2 Functional Block Diagram



7.3 Feature Description

The TLVx376 family of precision amplifiers offers excellent dc performance as well as excellent ac performance. Operating from a single power supply, the TLVx376 is capable of driving large capacitive loads, has a wide input common-mode voltage range, and is well-suited to drive the inputs of successive-approximation register (SAR) analog-to-digital converters (ADCs) as well as 24-bit and higher resolution converters. All devices feature internal ESD protection. The TLVx376 family is offered in a variety of industry-standard packages for applications that require space savings.

7.3.1 Operating Voltage

The TLVx376 family of amplifiers operate over a power-supply range of 2.2 V to 5.5 V (±1.1 V to ±2.75 V). Many of the specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

7.3.2 Capacitive Load and Stability

The TLVx376 series of amplifiers can be used in applications where driving a capacitive load is required. As with all op amps, there can be specific instances where the TLVx376 can become unstable, leading to oscillation. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier is stable in operation or not. An op amp in the unity-gain (+1 V/V) buffer configuration and driving a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the op amp output resistance, creates a pole within the feedback loop that degrades the phase margin. The phase margin reduces when the capacitive loading increases.

Feature Description (continued)

7.3.3 Input Offset Voltage and Input Offset Voltage Drift

The TLVx376 family of operational amplifiers is manufactured using TI's e-trim™ technology. Each amplifier is trimmed in production, thereby minimizing errors associated with input offset voltage and input offset voltage drift. The e-trim™ technology is a TI proprietary method of trimming internal device parameters during either wafer probing or final testing.

The TLVx376 in a unity-gain configuration can directly drive up to 250 pF of pure capacitive load. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads; see Figure 16. In unity-gain configurations, capacitive load drive can be improved by inserting a small (10 Ω to 20 Ω) resistor, R_S, in series with the output, as shown in Figure 22. This resistor significantly reduces ringing and maintains dc performance for purely capacitive loads. However, if there is a resistive load in parallel with the capacitive load, a voltage divider is created, introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_S / R_L, and is generally negligible at low output current levels.

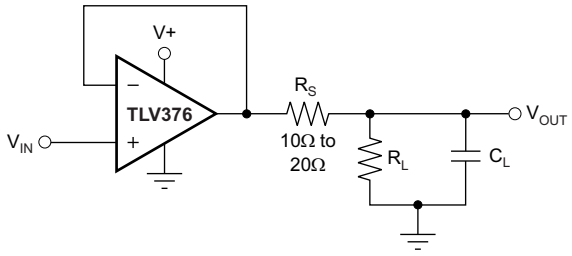


Figure 22. Improving Capacitive Load Drive

7.3.4 Common-Mode Voltage Range

The input common-mode voltage range of the TLVx376 series extends 100 mV beyond the supply rails. The offset voltage of the amplifier is very low, from approximately (V–) to (V+) – 1 V, as shown in Figure 23. The offset voltage increases when common-mode voltage exceeds (V+) –1 V. Common-mode rejection is specified from (V–) to (V+) – 1.3 V.

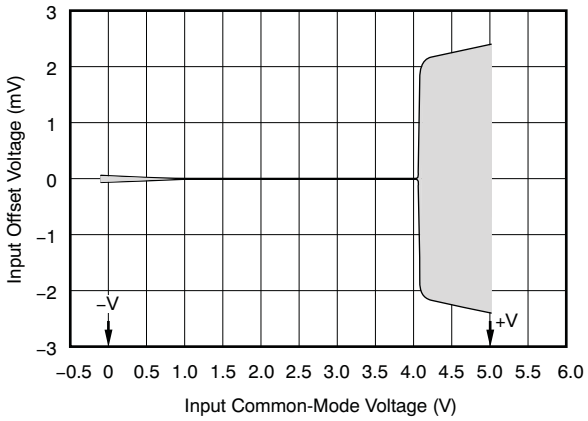


Figure 23. Offset and Common-Mode Voltage

Feature Description (continued)

Parameters that can vary across the common-mode voltage range are listed in Table 1.

Table 1. Parameters With Variation Across the Common-Mode Voltage Range

PARAMETER		(V–) - 0.1 V < V_{CM} < (V+) – 1.3 V	(V+) – 1.3 V < V_{CM} < (V+) + 0.1 V	UNIT
		TYP	TYP	
OFFSET VOLTAGE				
V_{OS}	Input offset voltage	40	2500	µV
dV_{OS}/dT	Offset voltage vs temperature	1	25	µV/°C
OPEN LOOP GAIN				
A_{OL}	Open-loop voltage gain	126	96	dB
INPUT VOLTAGE RANGE				
CMRR	Common-mode rejection ratio	88	43	dB
FREQUENCY RESPONSE				
GBW	Gain-bandwidth product	5.5	5.5	MHz
PM	Phase margin	72	72	Degrees
SR	Slew rate, G = 1	2	1.1	V/µs
NOISE				
e_n	Input voltage noise density, f = 1 kHz	8	135	nV/√Hz
i_n	Input current noise, f = 1 kHz	2	47	fA/√Hz

7.3.5 Input and ESD Protection

The TLVx376 family incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in the *Absolute Maximum Ratings* table. Figure 24 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input. In noise-sensitive applications, the value of this resistor must be as low as possible.

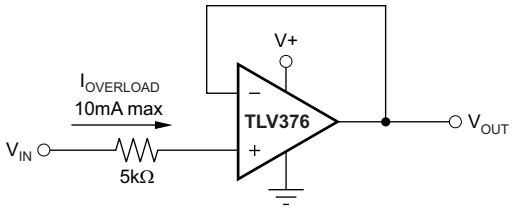


Figure 24. Input Current Protection

7.4 Device Functional Modes

The TLVx376 family has a single functional mode and is operational when the power-supply voltage is greater than 2.2 V (±1.1 V). The maximum power-supply voltage for the TLVx376 family is 5.5 V (±2.75 V).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV376 family of operational amplifiers is built using e-trim™, a proprietary technique in which offset voltage is adjusted during the final steps of manufacturing. This technique compensates for performance shifts that can occur during the molding process. Through e-trim™, the TLV376 family delivers excellent offset voltage (40 μV, typical). Additionally, the amplifier boasts a fast slew rate, low drift, low noise, and excellent PSRR and A_{OL}. These 5.5-MHz CMOS op amps only consume 815-μA (typical) quiescent current.

8.1.1 Operating Characteristics

The TLVx376 family of amplifiers has parameters that are fully specified from 2.2 V to 5.5 V (±1.1 V to ±2.75 V). Many of the specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

8.1.2 Basic Amplifier Configurations

The TLVx376 family is unity-gain stable. The TLVx376 does not exhibit output phase inversion when the input is overdriven. A typical single-supply connection is shown in Figure 25. The TLV376 is configured as a basic inverting amplifier with a gain of –10 V/V. This single-supply connection has an output centered on the common-mode voltage, V_{CM}. For the circuit shown, this voltage is 2.5 V, but can be any value within the common-mode input voltage range.

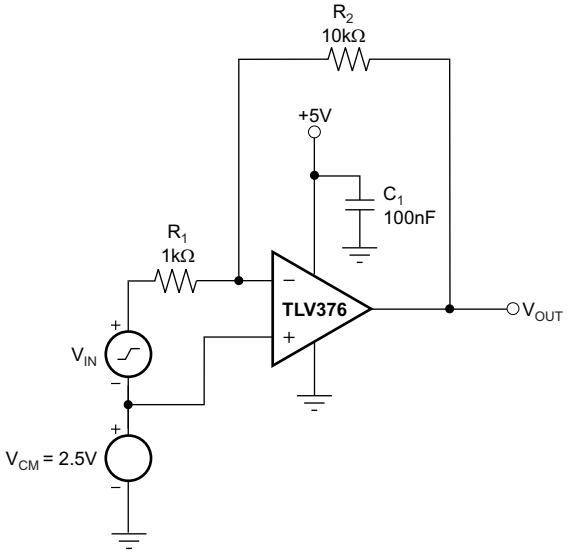


Figure 25. Basic Single-Supply Connection

Application Information (continued)

8.1.3 Active Filtering

The TLVx376 family is well-suited for filter applications requiring a wide-bandwidth, fast slew rate, low-noise, single-supply operational amplifier. Figure 26 shows a 50-kHz, 2nd-order, low-pass filter. The components have been selected to provide a maximally-flat Butterworth response. Beyond the cutoff frequency, roll-off is –40 dB per decade. The Butterworth response is ideal for applications requiring predictable gain characteristics (such as the antialiasing filter used ahead of an ADC).

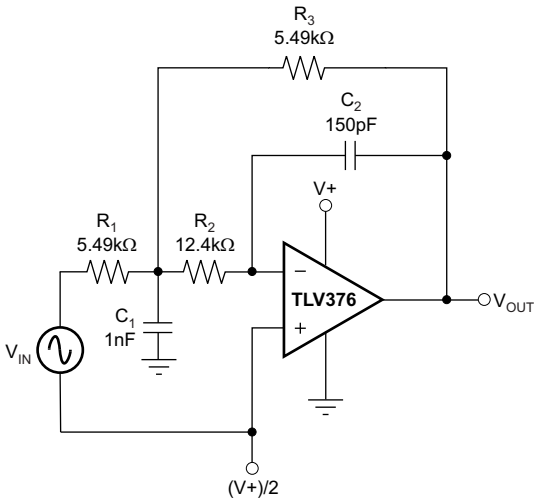
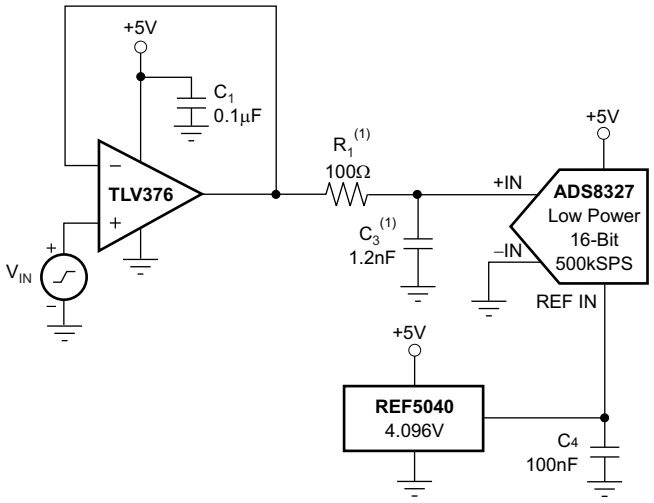


Figure 26. Second-Order, Butterworth, 50-kHz, Low-Pass Filter

8.1.4 Driving an Analog-to-Digital Converter

The low-noise and wide-gain bandwidth of the TLVx376 family make these devices ideal for driving ADCs. Figure 27 shows the TLV376 driving an ADS8327, a 16-bit, 250-kSPS converter. The amplifier is connected as a unity-gain, noninverting buffer.



NOTE: Suggested value; may require adjustment based on specific application.

Figure 27. Driving an ADS8327

Application Information (continued)

8.1.5 Phantom-Powered Microphone

The circuit shown in Figure 28 depicts how a remote microphone amplifier can be powered by a phantom source on the output side of the signal cable. The cable serves double duty, carrying both the differential output signal from and dc power to the microphone amplifier stage.

A TLV2376 serves as a single-ended input to a differential output amplifier with a 6-dB gain. Common-mode bias for the two op amps is provided by the dc voltage developed across the electret microphone element. A 48-V phantom supply is reduced to 5.1 V by the series 6.8-kΩ resistors on the output side of the cable, and the 4.7 kΩ and zener diode on the input side of the cable. AC coupling blocks the different dc voltage levels from each other on each end of the cable.

An INA163 instrumentation amplifier provides differential inputs and receives the balanced audio signals from the cable. The INA163 gain can be set from 0 dB to 80 dB by selecting the R_G value. The INA163 circuit is typical of the input circuitry used in mixing consoles.

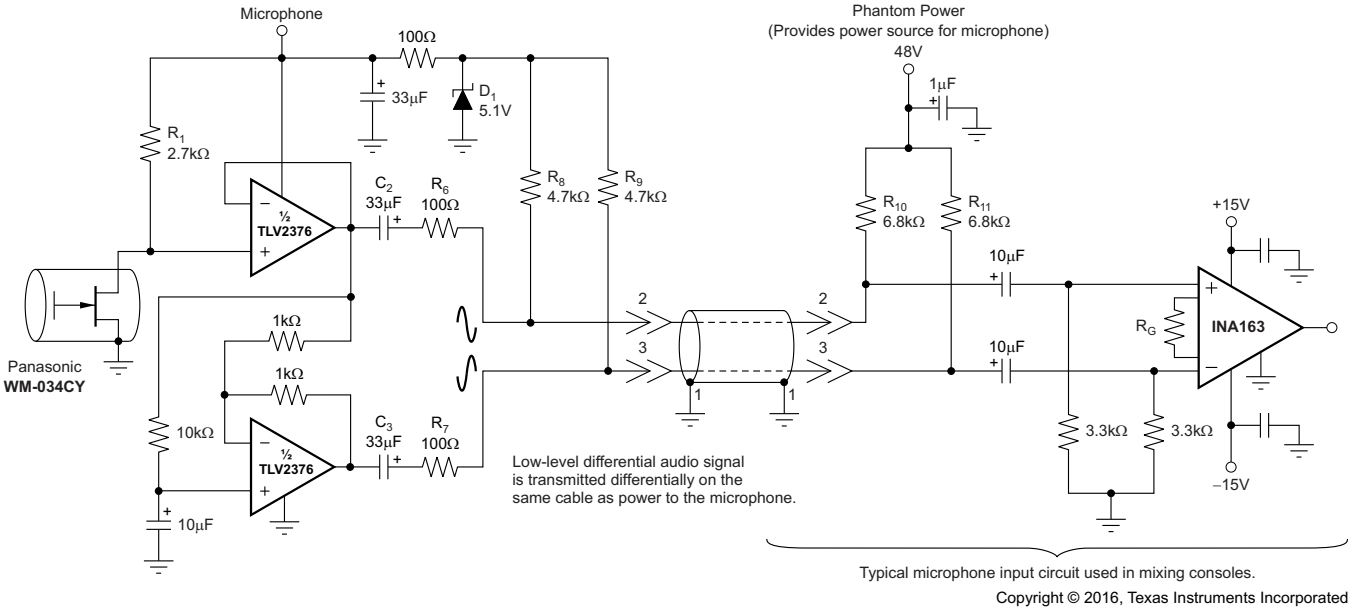


Figure 28. Phantom-Powered Electret Microphone

8.2 Typical Application

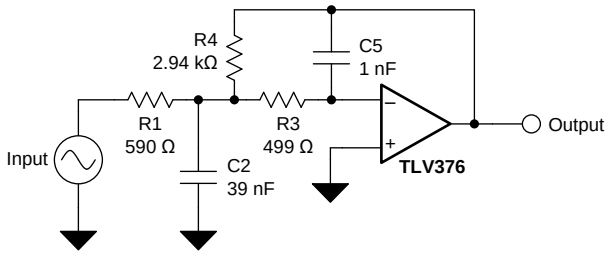


Figure 29. Second-Order, Low-Pass Filter

8.2.1 Design Requirements

Low-pass filters are commonly employed in signal-processing applications to reduce noise and prevent aliasing. The TLV376 is ideally suited to construct high-speed, high-precision active filters. Figure 29 shows a second-order, low-pass filter commonly encountered in signal-processing applications.

Use the following parameters for this design example:

- Gain = 5 V/V (inverting gain)
- Low-pass cutoff frequency = 25 kHz
- Second-order Chebyshev filter response with 3-dB gain peaking in the passband

8.2.2 Detailed Design Procedure

The infinite-gain multiple-feedback circuit for a low-pass network function is shown in the *Application Curve* section. Use Equation 1 to calculate the voltage transfer function.

$$\frac{\text{Output}}{\text{Input}}(s) = \frac{-1/R_1R_3C_2C_5}{s^2 + (s/C_2)(1/R_1 + 1/R_3 + 1/R_4) + 1/R_3R_4C_2C_5} \quad (1)$$

This circuit in Figure 29 produces a signal inversion. For this circuit, the gain at dc and the low-pass cutoff frequency are calculated by Equation 2:

$$\text{Gain} = \frac{R_4}{R_1}$$

$$f_C = \frac{1}{2\pi}\sqrt{(1/R_3R_4C_2C_5)} \quad (2)$$

Software tools are readily available to simplify filter design. The WEBENCH® filter designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH® filter designer allows optimized filter designs to be created by using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the WEBENCH® design center, the WEBENCH® filter designer allows complete multistage active filter solutions to be designed, optimized, and simulated within minutes.

Typical Application (continued)

8.2.3 Application Curve

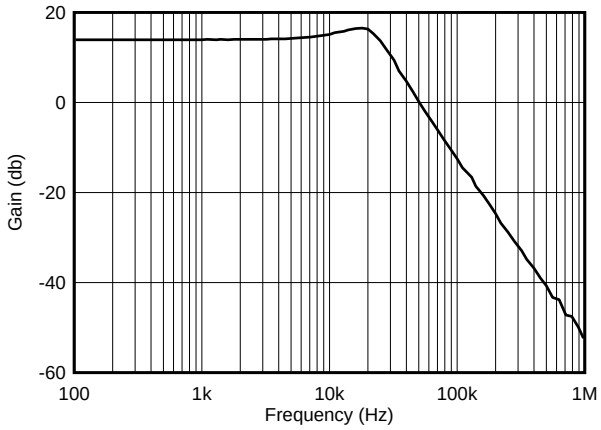


Figure 30. Measured Frequency Response of the Second-Order, Low-Pass Filter

9 Power Supply Recommendations

The TLVx376 family of devices are specified for operation from 2.2 V to 5.5 V (±1.1 V to ±2.75 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-equivalent series resistance (ESR), 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information, see the *Circuit Board Layout Techniques* application report.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in Figure 32, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.

Layout Guidelines (continued)

- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example

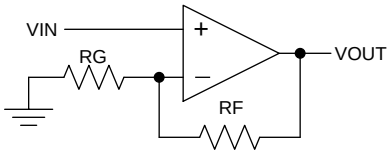


Figure 31. Schematic Representation of Figure 32

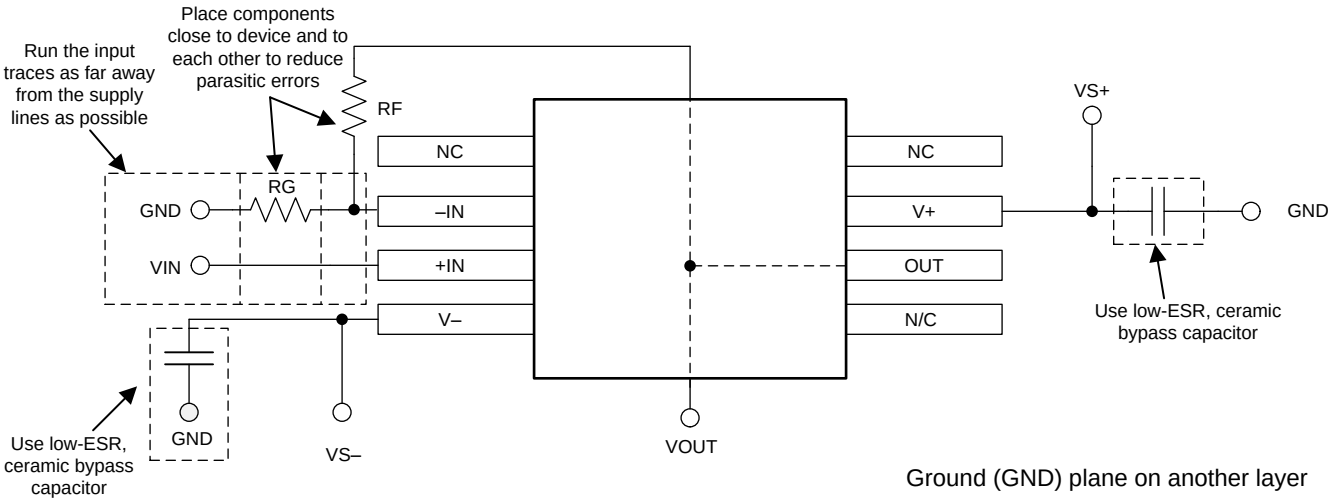


Figure 32. Layout Example

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 開発サポート

11.1.1.1 TINA-TI™(無料のダウンロード・ソフトウェア)

TINA-TI™は、SPICEエンジンをベースにした単純かつ強力な、使いやすい回路シミュレーション・プログラムです。TINA-TI™はTINA-TI™ソフトウェアの無料バージョンで、完全な機能を持ち、パッシブとアクティブ両方のモデルに加えて、マクロ・モデルのライブラリがプリロードされています。TINA-TI™には従来型のDC、過渡、および周波数ドメインのSPICEによる分析と、追加の設計機能が搭載されています。

TINA-TI™はAnalog eLab Design Centerから無料でダウンロードでき、ユーザーが結果をさまざまな方法でフォーマットできる、広範な後処理機能を備えています。仮想計測器により、入力波形を選択し、回路ノード、電圧、および波形をプローブして、動的なクイック・スタート・ツールを作成できます。

注

これらのファイルを使用するには、TINAソフトウェア（DesignSoft™製）またはTINA-TI™ソフトウェアがインストールされている必要があります。TINA-TI™フォルダから、無料のTINA-TI™ソフトウェアをダウンロードしてください。

11.1.1.2 TI Precision Designs

TI Precision Designsは、TIの高精度アナログ・アプリケーションの専門家により作成されたアナログ・ソリューションで、多くの有用な回路に関して、動作理論、コンポーネント選択、シミュレーション、完全なPCB回路図とレイアウト、部品表、性能測定結果を提供します。TI Precision Designsは、www.ti.com/ww/en/analog/precision-designs/からオンラインで入手できます。

11.1.1.3 WEBENCH® Filter Designer

WEBENCH® Filter Designerは単純で強力な、使いやすいアクティブ・フィルタ設計プログラムです。WEBENCH® Filter Designerを使用すると、TIのベンダ・パートナーからのTI製オペアンプやパッシブ・コンポーネントを使用して、最適なフィルタ設計を作成できます。

WEBENCH® Filter Designerは、WEBENCH® Design CenterからWebベースのツールとして利用でき、包括的な複数段アクティブ・フィルタ・ソリューションをわずか数分で設計、最適化、シミュレーションできます。

11.2 ドキュメントのサポート

11.2.1 関連資料

関連資料については、以下を参照してください：

- *『基板のレイアウト技法』*アプリケーション・レポート(SLOA089)
- *『オペアンプのゲイン安定性、第3部: ACゲイン誤差の解析』*アプリケーション・レポート(SLYT383)
- *『オペアンプのゲイン安定性、第2部: DCゲイン誤差の解析』*アプリケーション・レポート(SLYT374)
- *『完全差動アクティブ・フィルタにおける無限ゲイン、MFBフィルタ・トポロジの使用』*アプリケーション・レポート(SLYT343)
- *『オペアンプの性能解析』*アプリケーション・レポート(SBOA054)
- *『オペアンプの単一電源動作』*アプリケーション・レポート(SBOA059)
- *『アンプのチューニング』*アプリケーション・レポート(SBOA067)
- *『鉛フリー仕上げ部品の保管寿命評価』*アプリケーション・レポート(SZZA046)
- *『ADS832x 低消費電力、16ビット、500kHz、シングル/デュアル、ユニポーラ入力A/Dコンバータ、シリアル・インターフェイス付き』*(SLAS415)
- *『REF50xx 低ノイズ、超低ドリフト係数、高精度基準電圧』*(SBOS410)
- *『INA163 低ノイズ、低歪計装用アンプ』*(SBOS177)
- *『ADS7822 12ビット、200kHz、microPowerサンプリングA/Dコンバータ』*(SBAS062)

11.3 関連リンク

表 2 に、クイック・アクセス・リンクの一覧を示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 2. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
TLV376	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TLV2376	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TLV4376	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

11.4 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.5 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.6 商標

e-trim, TINA-TI, E2E are trademarks of Texas Instruments.
DesignSoft is a trademark of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

11.7 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV2376IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	13F6
TLV2376IDGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13F6
TLV2376IDGKRG4	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13F6
TLV2376IDGKRG4.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13F6
TLV2376IDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	13F6
TLV2376IDGKT.B	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13F6
TLV2376IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV 2376
TLV2376IDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV 2376
TLV376IDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	12J
TLV376IDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	12J
TLV376IDBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	12J
TLV376IDBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	12J
TLV376IDBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	12J
TLV376IDBVT.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	12J
TLV376IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV 15M
TLV376IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV 15M
TLV376IDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV 15M
TLV4376IPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV4376
TLV4376IPWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV4376
TLV4376IPWRG4	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV4376
TLV4376IPWRG4.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV4376

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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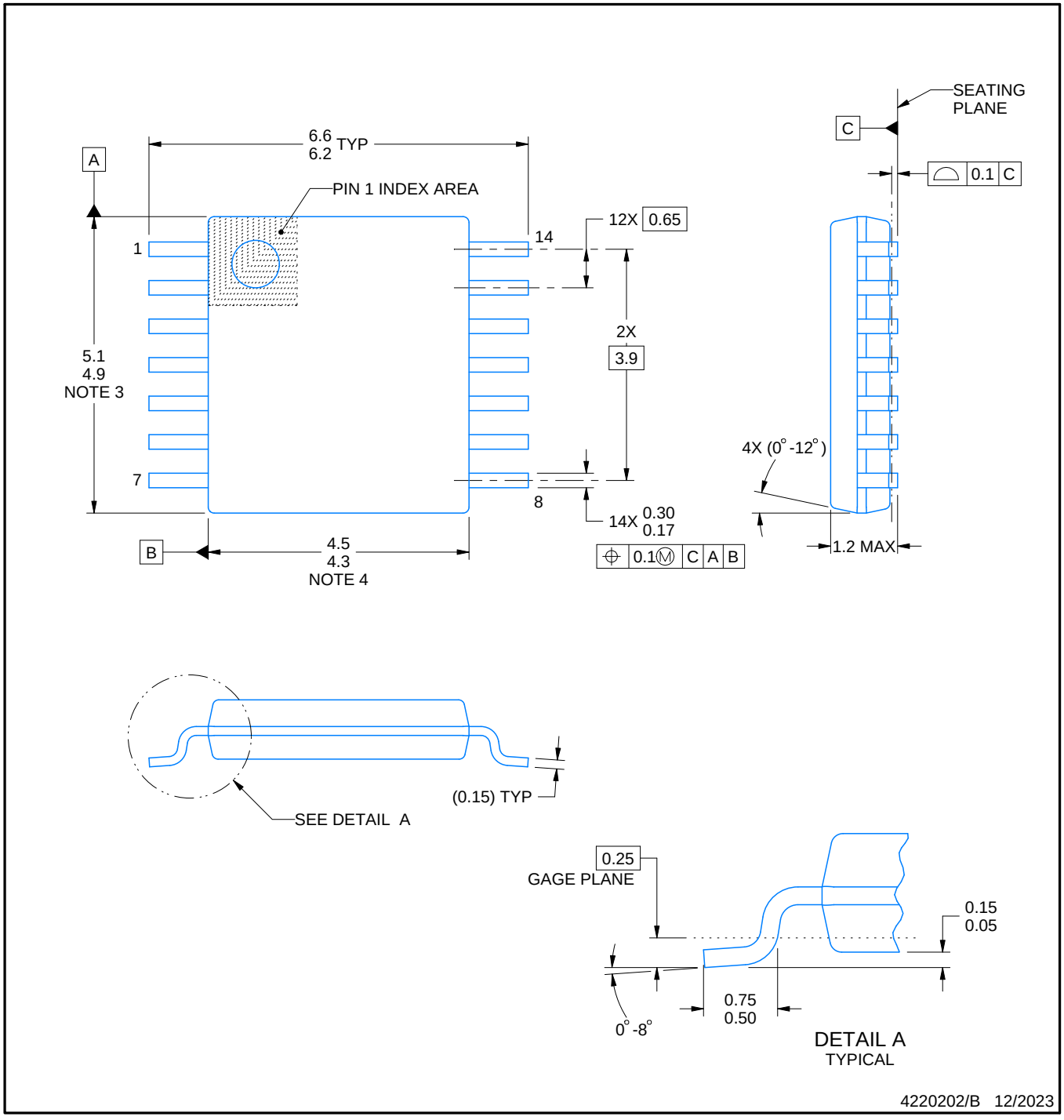
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE OUTLINE

PW0014A

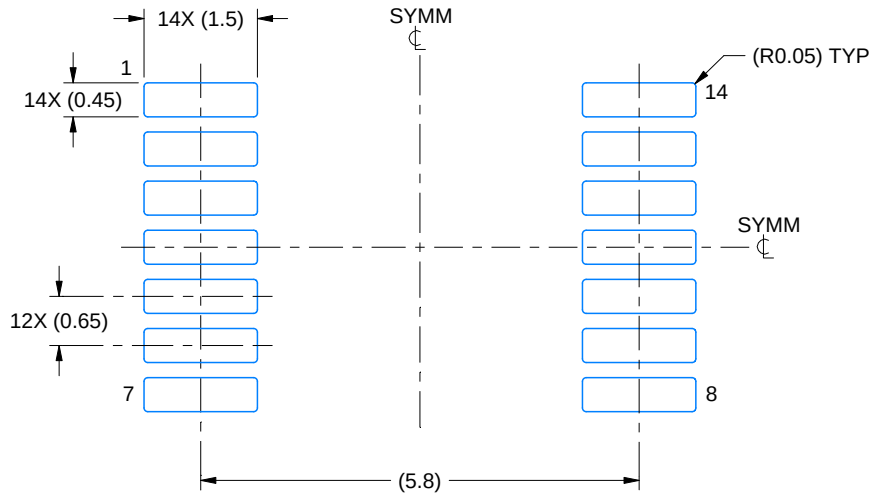
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

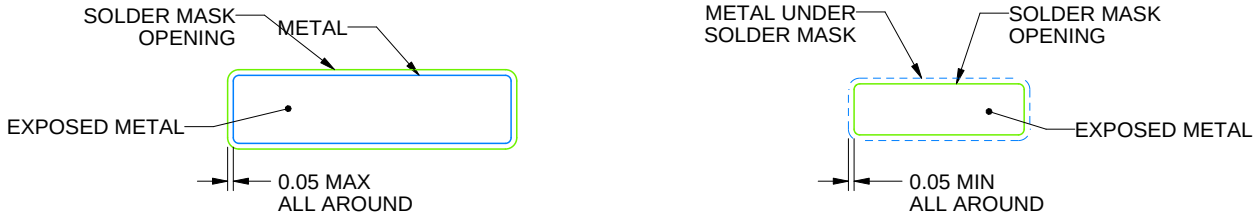


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

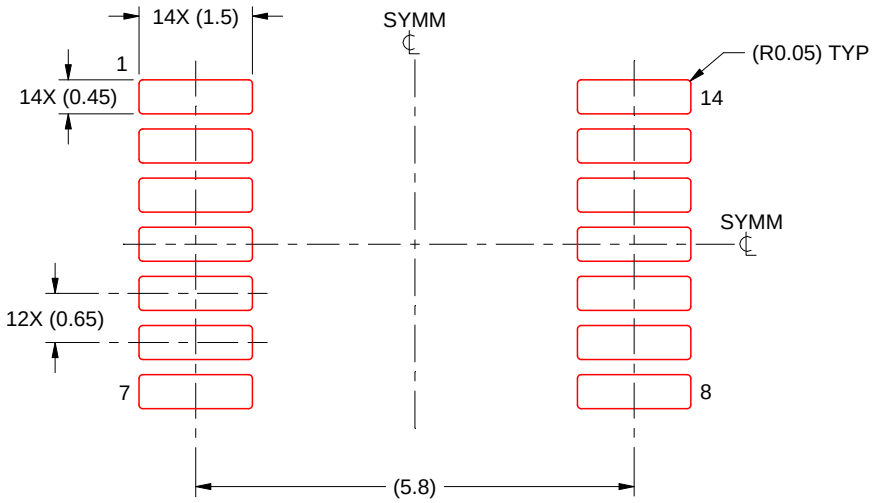


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

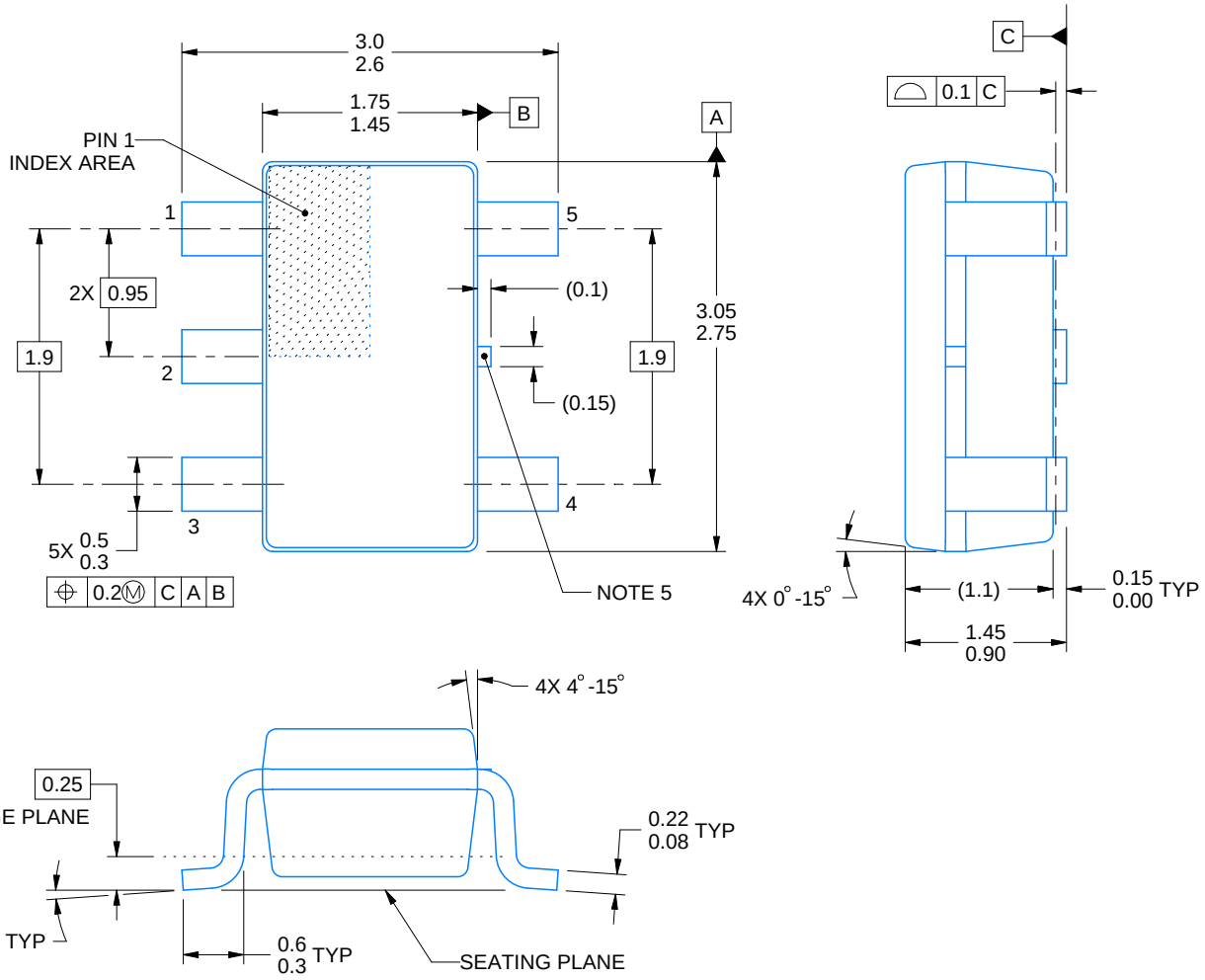
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

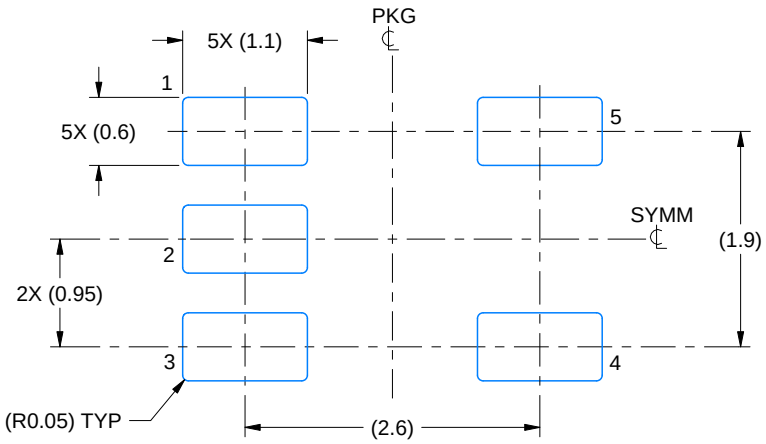
SMALL OUTLINE TRANSISTOR



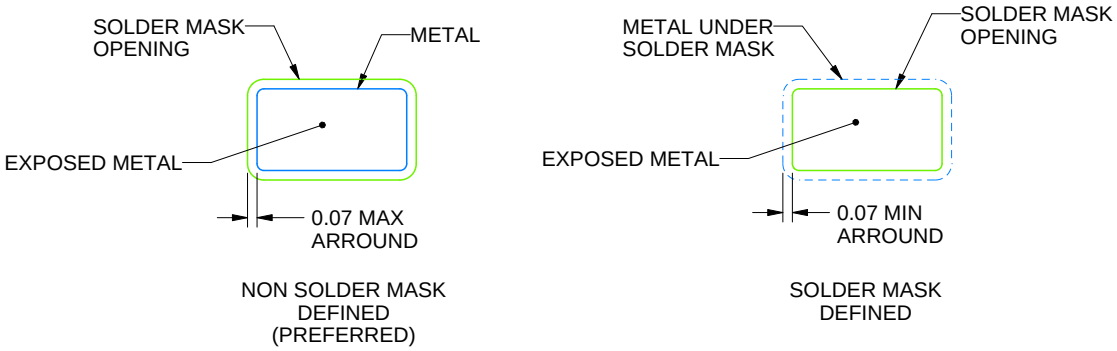
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

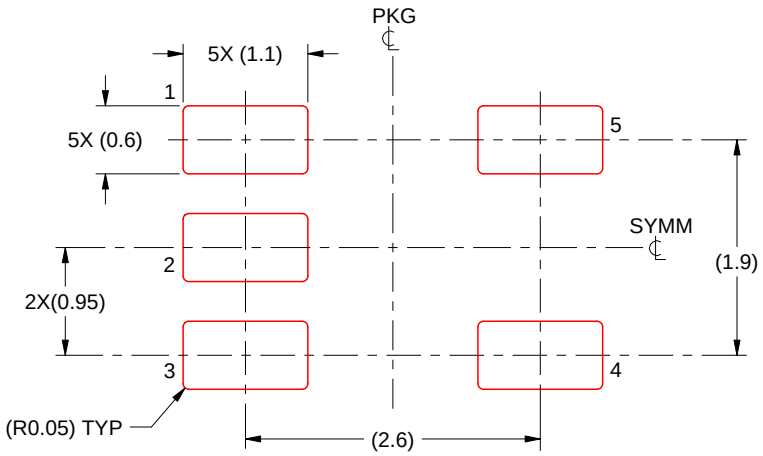


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

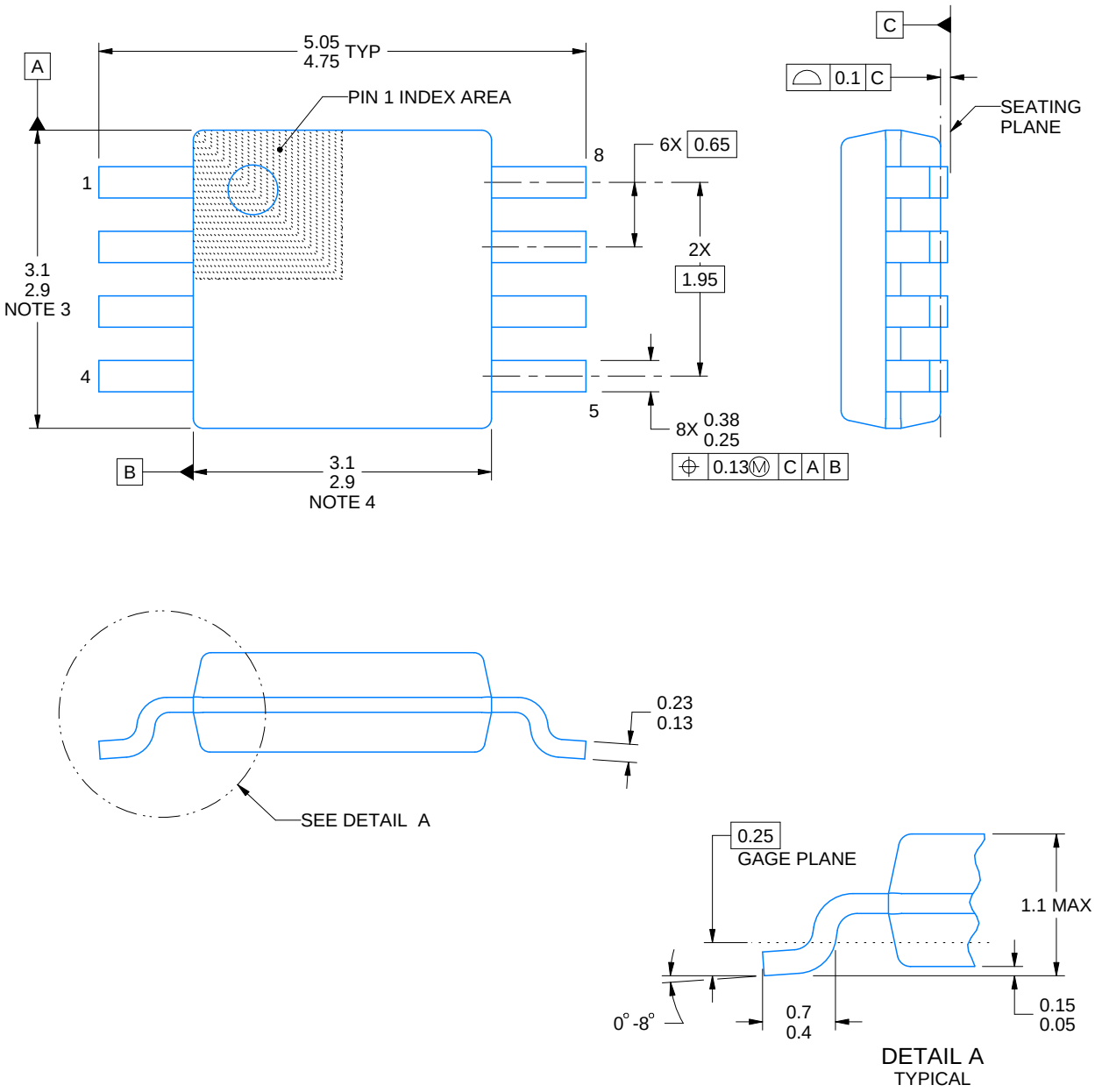
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

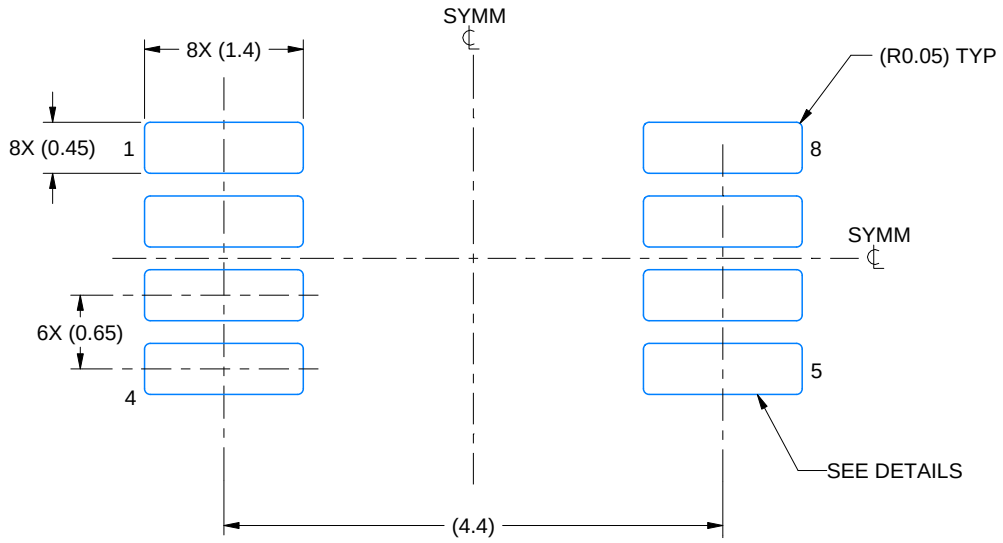
SMALL OUTLINE PACKAGE



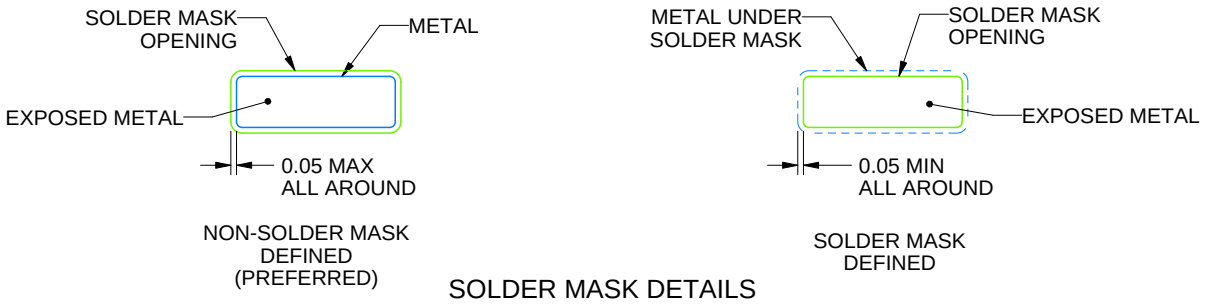
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

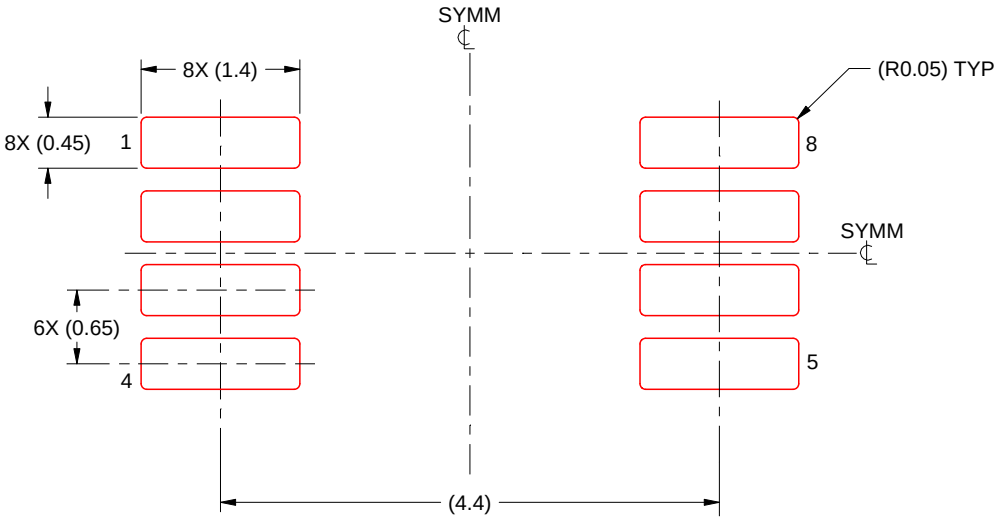


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

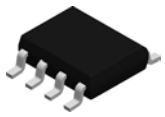


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

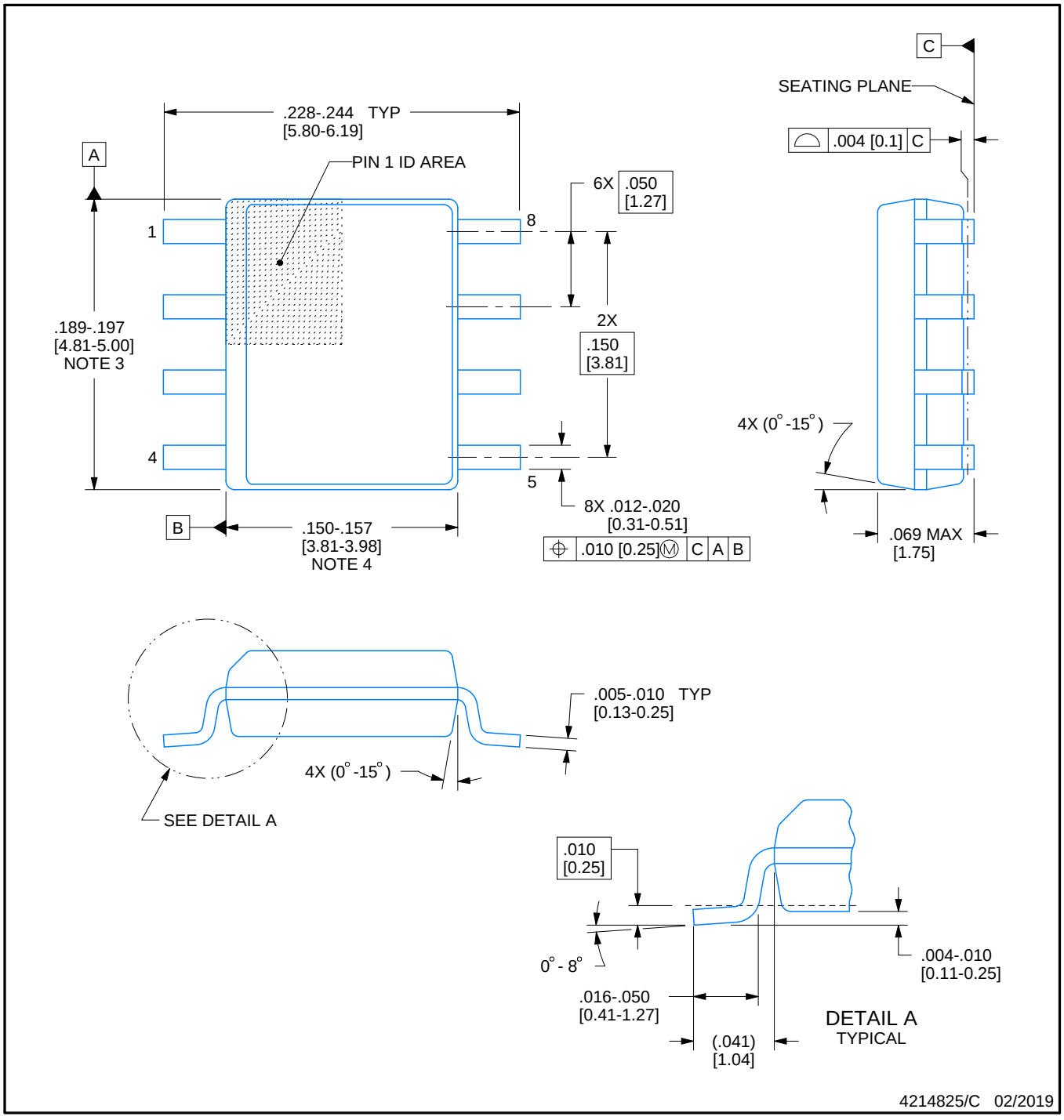


PACKAGE OUTLINE

D0008A

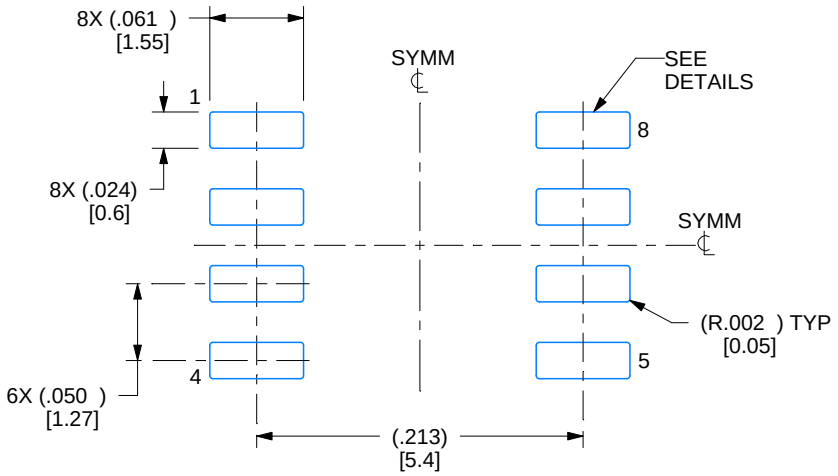
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

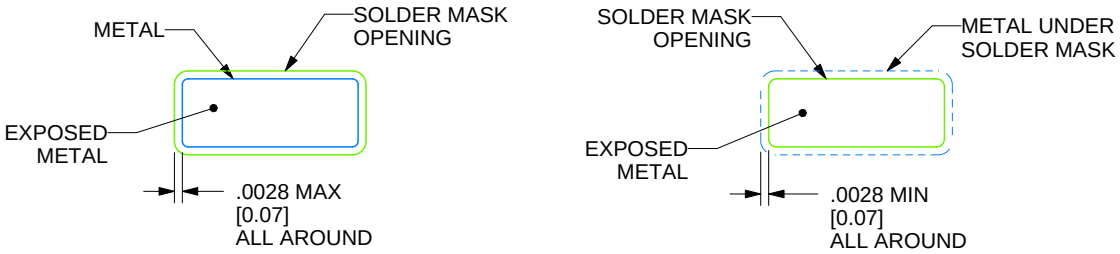


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

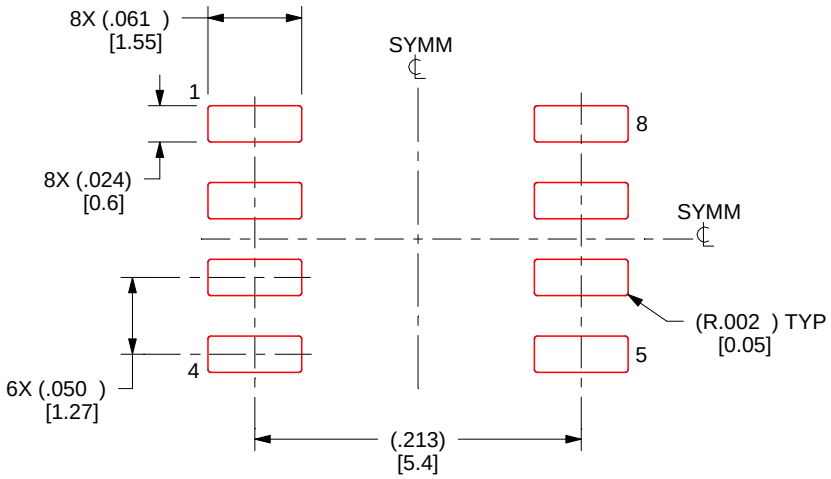
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月