

TLV246xx-Q1 低消費電力、レール・ツー・レール入力/出力、 シャットダウン機能搭載のオペアンプ

1 特長

- 車載アプリケーションに認定済み
- 下記内容でAEC-Q100認定済み
 - デバイス温度グレード1: 動作時周囲温度範囲 $-40^{\circ}\text{C} \sim +125^{\circ}\text{C}$
 - デバイスHBM ESD分類レベル2
 - デバイスCDM ESD分類レベルC6
- MIL-STD-883, Method 3015に従い2000Vを超えるESD保護、機械モデルC = 200pF, R = 0では200V超
- レール・ツー・レール出力
- ゲイン帯域幅積: 6.4MHz
- 出力駆動能力: $\pm 80\text{mA}$
- 消費電流: 500 μA /チャンネル
- 入力ノイズ電圧: 11nV/ $\sqrt{\text{Hz}}$
- スルー・レート: 1.6V/ μs
- マイクロパワー・シャットダウン・モード (TLV2460-Q1およびTLV2463-Q1): 0.3 μA /チャンネル
- ユニバーサル・オペアンプ評価モジュール
- シングル、デュアル、クワッド・バージョンで供給

2 アプリケーション

- クラスタ
- テレマティクス
- HEV/EVおよびパワートレイン
- DC/DCインバータ
- パワー・ステアリング
- 照明モジュール
- バッテリー管理システム

3 概要

TLV246x-Q1ファミリの低消費電力、レール・ツー・レール入力/出力オペアンプ・デバイスは、HEV/EVおよびパワートレインのバッテリー管理システム、車体の照明および屋根用モジュール・システム、その他の照明アプリケーション用に設計されています。入力同相範囲が電源電圧を超えているため、低電圧のシステムでも最大のダイナミック・レンジが得られます。アンプの出力はレール・ツー・レールで高い出力駆動能力を持ち、旧来のレール・ツー・レール入力/出力オペアンプの制限の1つが解決されます。レール・ツー・レールのダイナミック・レンジと高い出力駆動能力から、TLV246x-Q1はアナログ/デジタル・コンバータのバッファ用に適しています。

オペアンプは6.4MHzの帯域幅と1.6V/ μs のスルー・レートをもち、わずか500 μA の電流しか消費しないため、低消費電力で優れたAC性能が得られます。オプションのシャットダウン端子を持つデバイスも用意されており、アンプを超低消費電流モード(チャンネルごとに $I_{\text{DD}} = 0.3\mu\text{A}$)に移行できます。シャットダウン中、オペアンプの出力はハイ・インピーダンス状態になります。入力ノイズ電圧11nV/ $\sqrt{\text{Hz}}$ 、入力オフセット電圧100 μV でDCアプリケーションを設計できます。

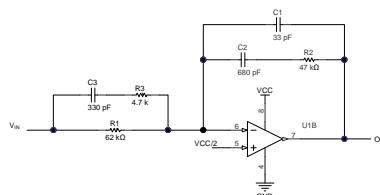
製品情報⁽¹⁾

型番	パッケージ	本体サイズ(公称)
TLV246x-Q1、 TLV246xA-Q1	TSSOP (8)	4.40mmx3.00mm
	SOIC (8)	3.91mmx4.90mm
TLV2462-Q1、 TLV2462A-Q1	TSSOP (8)	4.40mmx3.00mm
	VSSOP (8)	3.00mmx3.00mm
TLV246x-Q1、 TLV246xA-Q1	TSSOP (14)	4.40mmx5.00mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

(2) 利用可能なすべてのデバイス・オプションについては、[メカニカル、パッケージ、および注文情報](#)を参照してください。

代表的なアプリケーション



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision F (December 2015) から Revision G に変更	Page
• 最新のデータシートおよび翻訳標準に合わせてデータシートのテキストを更新	1
• 「特長」セクションの「入力オフセット電圧: 100 μ V」箇条書き項目を削除	1
• 「特長」セクションの「ユニバーサル・オペアンプEVM」箇条書き項目を削除	1
• ドキュメントからTLV2464デバイスを削除	1
• Deleted <i>Device Comparison</i> table	3
• Reformatted <i>Thermal Information</i> tables and table notes	5
• Changed I_{IO} and I_{IB} unit from pA to nA in <i>Electrical Characteristics: $V_{DD} = 3\text{ V}$</i> table	7
• Changed I_{IO} and I_{IB} unit from pA to nA in <i>Electrical Characteristics: $V_{DD} = 5\text{ V}$</i> table	8
• 「関連資料」セクションのドキュメント参照のフォーマットを変更	31

Revision E (October 2012) から Revision F に変更	Page
• AEC-Q100の箇条書き項目を追加	1
• 「ESD定格」の表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加	1
• Deleted D package from TLV2460-Q1, TLV2461-Q1, TLV2463-Q1, and TLV2464A-Q1 and added TLV246xA-Q1 device number to pin drawings	3
• Deleted table note 3 reference to JESD 51-5 from <i>Absolute Maximum Ratings</i> table	5

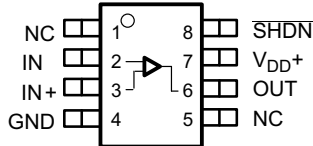
Revision D (September 2010) から Revision E に変更

Page

• ドキュメント全体を通してデバイス名をTLV246xxからTLV246xx-Q1に変更	1
• Changed I _{DD} unit from μ A to mA.	7
• Changed I _{DD} unit from μ A to mA	8

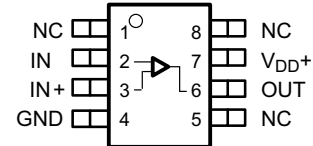
5 Pin Configuration and Functions

TLV2460-Q1, TLV2460A-Q1 PW Package
 8-Pin TSSOP
 Top View



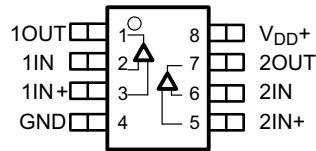
NC- no internal connection

TLV2461-Q1, TLV2461A-Q1 PW Package
 8-Pin TSSOP
 Top View



NC- no internal connection

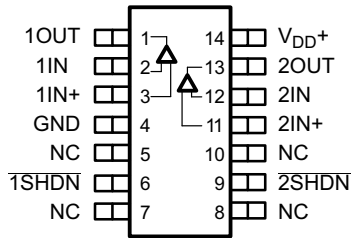
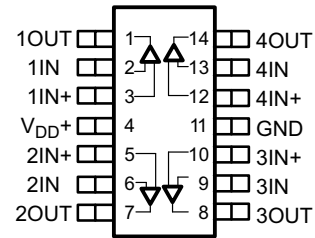
TLV2462-Q1, TLV2462A-Q1 D, DGK, or PW Package
 8-Pin SOIC, TSSOP, or VSSOP
 Top View



NC – No internal connection

Pin Functions

NAME	PIN			I/O	DESCRIPTION
	TLV2460-Q1, TLV2460A-Q1	TLV2461-Q1, TLV2461A-Q1	TLV2462-Q1, TLV2462A-Q1		
1IN	—	—	2	I	Inverting input, channel 1
1IN+	—	—	3	I	Noninverting input, channel 1
1OUT	—	—	1	O	Output, channel 1
2IN	—	—	6	I	Inverting input, channel 2
2IN+	—	—	5	I	Noninverting input, channel 2
2OUT	—	—	7	O	Output, channel 2
IN	2	2	—	I	Inverting input
IN+	3	3	—	I	Noninverting input
GND	4	4	4	—	Negative (lowest) supply
NC	1, 5	1, 5, 8	—	—	No internal connection
OUT	6	6	—	O	Output
SHDN	8	—	—	I	Shutdown
V _{DD+}	7	7	8	—	Positive (highest) supply

**TLV2463-Q1, TLV2463A-Q1 PW Package
14-Pin TSSOP
Top View**

**TLV2463-Q1, TLV2463A-Q1 PW Package
14-Pin TSSOP
Top View**


NC – No internal connection

Pin Functions

NAME	PIN		I/O	DESCRIPTION
	TLV2463-Q1, TLV2463A-Q1	TLV2464A-Q1		
1IN	2	2	I	Inverting input, channel 1
1IN+	3	3	I	Noninverting input, channel 1
1OUT	1	1	O	Output, channel 1
1SHDN	6	—	I	Shutdown for channel 1
2IN	12	6	I	Inverting input, channel 2
2IN+	11	5	I	Noninverting input, channel 2
2OUT	13	7	O	Output, channel 2
2SHDN	9	—	I	Shutdown for channel 2
3IN	—	9	I	Inverting input, channel 3
3IN+	—	10	I	Noninverting input, channel 3
3OUT	—	8	O	Output, channel 3
4IN	—	13	I	Inverting input, channel 4
4IN+	—	12	I	Noninverting input, channel 4
4OUT	—	14	O	Output, channel 4
IN	—	—	I	Inverting input
IN+	—	—	I	Noninverting input
GND	4	11	—	Negative (lowest) supply
NC	5, 7, 8, 10	—	—	No internal connection
OUT	—	—	O	Output
SHDN	—	—	I	Shutdown
V _{DD+}	14	4	—	Positive (highest) supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

	MIN	MAX	UNIT
Supply voltage ⁽²⁾ , V_{DD}		6	V
Differential input voltage, V_{ID}	-0.2	$V_{DD} + 0.2$	V
Input current (any input), I_I	-200	200	mA
Output current, I_O	-175	175	mA
Total input current (into V_{DD+}), I_I		175	mA
Total output current (out of GND), I_O		175	mA
Operating free-air temperature, T_A	-40	125	°C
Maximum junction temperature, T_J		150	°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds		260	°C
Storage temperature, T_{stg}	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to GND.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000	V
	Charged-device model (CDM), per AEC Q100-011	±1000	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{DD} Supply voltage	Single-supply	2.7	6	V
	Split-supply	±1.35	±3	
V_{ICR} Common-mode input voltage range ⁽¹⁾		-0.2	$V_{DD} + 0.2$	V
T_A Operating free-air temperature		-40	125	°C
Shutdown on and off voltage level ⁽¹⁾	V_{IH}	2		V
	V_{IL}		0.7	

- (1) Relative to voltage on the GND terminal of the device

6.4 Thermal Information: TLV2460x-Q1

THERMAL METRIC ⁽¹⁾		TLV2460x-Q1	UNIT
		PW (TSSOP)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	185.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	69	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	114.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	112.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Thermal Information: TLV2461x-Q1

THERMAL METRIC ⁽¹⁾		TLV2461x-Q1	
		PW (TSSOP)	
		8 PINS	
			UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	185.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	69	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	114.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	9.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	112.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.6 Thermal Information: TLV2462-Q1

THERMAL METRIC ⁽¹⁾		TLV2462-Q1			UNIT
		D (SOIC)	DGK (VSSOP)	PW (TSSOP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	120.1	179.3	183.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	68.3	71.1	67	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60.4	100.4	112.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	20.6	10.7	9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	59.9	98.8	110.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.7 Thermal Information: TLV2462A-Q1

THERMAL METRIC ⁽¹⁾		TLV2462A-Q1		UNIT
		D (SOIC)	PW (TSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	120.1	185.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	68.3	69	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60.4	114.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	20.6	9.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	59.9	112.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.8 Thermal Information: TLV2463x-Q1

THERMAL METRIC ⁽¹⁾		TLV2463x-Q1	
		PW (TSSOP)	
		8 PINS	
			UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	185.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	69	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	114.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	9.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	112.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.9 Electrical Characteristics: $V_{DD} = 3\text{ V}$

at specified free-air temperature, $V_{DD} = 3\text{ V}$, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{DD} = 3\text{ V}$ $V_{IC} = 1.5\text{ V}$ $V_O = 1.5\text{ V}$ $R_S = 50\ \Omega$	TLV246x-Q1	$T_A = 25^\circ\text{C}$	100	2000	μV
				Full range ⁽¹⁾		2200	
			TLV246xA-Q1	$T_A = 25^\circ\text{C}$	150	1500	
				Full range ⁽¹⁾		1700	
α_{VIO}	Temperature coefficient of input offset voltage	$V_{DD} = 3\text{ V}$ $V_{IC} = 1.5\text{ V}$ $V_O = 1.5\text{ V}$ $R_S = 50\ \Omega$			2		$\mu\text{V}/^\circ\text{C}$
I_{IO}	Input offset current	$V_{DD} = 3\text{ V}$ $V_{IC} = 1.5\text{ V}$ $V_O = 1.5\text{ V}$ $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$		2.8	7	nA
			Full range ⁽¹⁾			75	
I_{IB}	Input bias current	$V_{IC} = 1.5\text{ V}$ $V_O = 1.5\text{ V}$ $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$		4.4	14	nA
			Full range ⁽¹⁾			75	
V_{OH}	High-level output voltage	$I_O = -2.5\text{ mA}$	$T_A = 25^\circ\text{C}$			2.9	V
			Full range ⁽¹⁾		2.8		
			$T_A = 25^\circ\text{C}$			2.7	
V_{OL}	Low-level output voltage	$V_{IC} = 1.5\text{ V}$ $I_{OL} = 2.5\text{ mA}$	$T_A = 25^\circ\text{C}$			0.1	V
			Full range ⁽¹⁾			0.2	
			$V_{IC} = 1.5\text{ V}$ $I_{OL} = 10\text{ mA}$	$T_A = 25^\circ\text{C}$			
I_{OS}	Short circuit output current	Sourcing	$T_A = 25^\circ\text{C}$			50	mA
			Full range ⁽¹⁾		20		
			$T_A = 25^\circ\text{C}$			40	
I_O	Output current	Measured 1 V from rail	$T_A = 25^\circ\text{C}$			± 40	mA
			Full range ⁽¹⁾				
A_{VD}	Large-signal differential voltage amplification	$R_L = 10\text{ k}\Omega$	$T_A = 25^\circ\text{C}$		90	105	dB
			Full range ⁽¹⁾		89		
$r_{i(d)}$	Differential input resistance		$T_A = 25^\circ\text{C}$			10^9	Ω
$c_{i(o)}$	Common-mode input capacitance	$f = 10\text{ kHz}$	$T_A = 25^\circ\text{C}$			7	pF
z_o	Closed-loop output impedance	$f = 100\text{ kHz}$ $A_V = 10$	$T_A = 25^\circ\text{C}$			33	Ω
CMRR	Common-mode rejection ratio	$V_{ICR} = 0\text{ V to } 3\text{ V}$ $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$		66	80	dB
			Full range ⁽¹⁾		60		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD} = 2.7\text{ V to } 6\text{ V}$ $V_{IC} = V_{DD} / 2$; no load	$T_A = 25^\circ\text{C}$		80	85	dB
			Full range ⁽¹⁾		75		
			$T_A = 25^\circ\text{C}$		85	95	
I_{DD}	Supply current (per channel)	$V_O = 1.5\text{ V}$; no load	$T_A = 25^\circ\text{C}$		0.5	0.575	mA
			Full range ⁽¹⁾			0.9	
$I_{DD(SHDN)}$	Supply current in shutdown (TLV2460-Q1, TLV2463-Q1)	$\overline{\text{SHDN}} < 0.7\text{ V}$, per channel in shutdown	$T_A = 25^\circ\text{C}$		0.3		μA
			Full range ⁽¹⁾			2.5	

(1) Full range is -40°C to $+125^\circ\text{C}$.

6.10 Electrical Characteristics: $V_{DD} = 5\text{ V}$

 at specified free-air temperature, $V_{DD} = 5\text{ V}$, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{DD} = 5\text{ V}$ $V_{IC} = 2.5\text{ V}$ $V_O = 2.5\text{ V}$ $R_S = 50\ \Omega$	TLV246x-Q1	$T_A = 25^\circ\text{C}$	150	2000	μV
				Full range ⁽¹⁾		2200	
		TLV246xA-Q1	$T_A = 25^\circ\text{C}$	150	1500		
			Full range ⁽¹⁾		1700		
α_{VIO}	Temperature coefficient of input offset voltage	$V_{DD} = 5\text{ V}$ $V_{IC} = 2.5\text{ V}$ $V_O = 2.5\text{ V}$ $R_S = 50\ \Omega$			2		$\mu\text{V}/^\circ\text{C}$
I_{IO}	Input offset current	$V_{DD} = 5\text{ V}$ $V_{IC} = 2.5\text{ V}$ $V_O = 2.5\text{ V}$ $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$	0.3	7	nA	
			Full range ⁽¹⁾		60		
I_{IB}	Input bias current	$V_{DD} = 5\text{ V}$ $V_{IC} = 2.5\text{ V}$ $V_O = 2.5\text{ V}$ $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$	1.3	14	nA	
			Full range ⁽¹⁾		60		
V_{OH}	High-level output voltage	$I_O = -2.5\text{ mA}$	TLV246x-Q1, TLV246xA-Q1	$T_A = 25^\circ\text{C}$	4.9		V
				Full range ⁽¹⁾	4.8		
		$I_O = -10\text{ mA}$	TLV2462QDGKRQ1	$T_A = 25^\circ\text{C}$	4.8		
				Full range ⁽¹⁾	4.7		
V_{OL}	Low-level output voltage	$V_{IC} = 2.5\text{ V}$ $I_{OL} = 2.5\text{ mA}$	TLV246x-Q1, TLV246xA-Q1	$T_A = 25^\circ\text{C}$	0.1		V
				Full range ⁽¹⁾		0.2	
		$V_{IC} = 2.5\text{ V}$ $I_{OL} = 10\text{ mA}$	TLV246x-Q1, TLV246xA-Q1	$T_A = 25^\circ\text{C}$	0.2		
				Full range ⁽¹⁾		0.3	
I_{OS}	Short circuit output current	Sourcing	TLV246x-Q1, TLV246xA-Q1	$T_A = 25^\circ\text{C}$	145		mA
				Full range ⁽¹⁾	60		
		Sinking	TLV246x-Q1, TLV246xA-Q1	$T_A = 25^\circ\text{C}$	100		
				Full range ⁽¹⁾	60		
I_O	Output current	Measured 1 V from rail	TLV246x-Q1, TLV246xA-Q1	$T_A = 25^\circ\text{C}$	± 80		mA
A_{VD}	Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}$ $R_L = 10\text{ k}\Omega$ $V_O = 1\text{ V to }4\text{ V}$	TLV246x-Q1, TLV246xA-Q1	$T_A = 25^\circ\text{C}$	92	109	dB
				Full range ⁽¹⁾	90		
$r_{i(d)}$	Differential input resistance		TLV246x-Q1, TLV246xA-Q1	$T_A = 25^\circ\text{C}$	10^9		Ω
$C_{i(o)}$	Common-mode input capacitance	$f = 10\text{ kHz}$	TLV246x-Q1, TLV246xA-Q1	$T_A = 25^\circ\text{C}$	7		pF
Z_o	Closed-loop output impedance	$f = 100\text{ kHz}, A_V = 10$	TLV246x-Q1, TLV246xA-Q1	$T_A = 25^\circ\text{C}$	29		Ω
CMRR	Common-mode rejection ratio	$V_{ICR} = 0\text{ V to }5\text{ V}$ $R_S = 50\ \Omega$	TLV246x-Q1, TLV246xA-Q1	$T_A = 25^\circ\text{C}$	71	85	dB
				Full range ⁽¹⁾	60		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD} = 2.7\text{ V to }6\text{ V}$ $V_{IC} = V_{DD} / 2$; no load	TLV246x-Q1, TLV246xA-Q1	$T_A = 25^\circ\text{C}$	80	85	dB
				Full range ⁽¹⁾	75		
		$V_{DD} = 3\text{ V to }5\text{ V}$ $V_{IC} = V_{DD} / 2$; no load	TLV246x-Q1, TLV246xA-Q1	$T_A = 25^\circ\text{C}$	85	95	
				Full range ⁽¹⁾	80		
I_{DD}	Supply current (per channel)	$V_O = 2.5\text{ V}$; no load	TLV246x-Q1, TLV246xA-Q1	$T_A = 25^\circ\text{C}$	0.55	0.65	mA
				Full range ⁽¹⁾		1	

 (1) Full range is -40°C to $+125^\circ\text{C}$.

Electrical Characteristics: $V_{DD} = 5\text{ V}$ (continued)

at specified free-air temperature, $V_{DD} = 5\text{ V}$, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{DD(SHD)}$ N)	Supply current in shutdown (TLV2460-Q1, TLV2463-Q1)	$\overline{SHDN} < 0.7\text{ V}$, Per channel in shutdown	$T_A = 25^\circ\text{C}$		1		μA
			Full range ⁽¹⁾			3	

6.11 Operating Characteristics: $V_{DD} = 3\text{ V}$

 $V_{DD} = 3\text{ V}$, at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_{O(PP)} = 2\text{ V}$ $C_L = 160\text{ pF}$ $R_L = 10\text{ k}\Omega$	$T_A = 25^\circ\text{C}$	1	1.6		$\text{V}/\mu\text{s}$
			Full range ⁽¹⁾	0.8			
V_n	Equivalent input noise voltage	$f = 100\text{ Hz}$ $f = 1\text{ kHz}$	$T_A = 25^\circ\text{C}$		16		$\text{nV}/\sqrt{\text{Hz}}$
					11		
I_n	Equivalent input noise current	$f = 1\text{ kHz}$	$T_A = 25^\circ\text{C}$		0.13		$\text{pA}/\sqrt{\text{Hz}}$
THD + N	Total harmonic distortion plus noise	$V_{O(PP)} = 2\text{ V}$ $R_L = 10\text{ k}\Omega$, $f = 1\text{ kHz}$	$A_V = 1$	$T_A = 25^\circ\text{C}$	0.006%		
			$A_V = 10$		0.02%		
			$A_V = 100$		0.08%		
$t_{(on)}$	Amplifier turn-on time	$A_V = 1$ $R_L = 10\text{ k}\Omega$	Both channels	$T_A = 25^\circ\text{C}$	7.6		μs
			Channel 1 only, Channel 2 on		7.65		
$t_{(off)}$	Amplifier turn-off time	$A_V = 1$ $R_L = 10\text{ k}\Omega$	Both channels	$T_A = 25^\circ\text{C}$	333		ns
			Channel 1 only, Channel 2 on		328		
			Channel 2 only, Channel 1 on		329		
Gain-bandwidth product		$f = 10\text{ kHz}$ $C_L = 160\text{ pF}$ $R_L = 10\text{ k}\Omega$	$T_A = 25^\circ\text{C}$		5.2		MHz
t_s	Settling time	$V_{(STEP)PP} = 2\text{ V}$ $A_V = -1$ $C_L = 10\text{ pF}$ $R_L = 10\text{ k}\Omega$	0.1%	$T_A = 25^\circ\text{C}$	1.47		μs
			0.01%		1.78		
		$V_{(STEP)PP} = 2\text{ V}$ $A_V = -1$ $C_L = 56\text{ pF}$ $R_L = 10\text{ k}\Omega$	0.1%		1.77		
			0.01%		1.98		
ϕ_m	Phase margin at unity gain	$R_L = 10\text{ k}\Omega$ $C_L = 160\text{ pF}$	$T_A = 25^\circ\text{C}$		44		$^\circ$
Gain margin		$R_L = 10\text{ k}\Omega$ $C_L = 160\text{ pF}$	$T_A = 25^\circ\text{C}$		7		dB

 (1) Full range is -40°C to $+125^\circ\text{C}$.

6.12 Operating Characteristics: $V_{DD} = 5\text{ V}$

$V_{DD} = 5\text{ V}$, at specified free-air temperature, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_{O(PP)} = 2\text{ V}$ $C_L = 160\text{ pF}$ $R_L = 10\text{ k}\Omega$	$T_A = 25^\circ\text{C}$	1	1.6		V/ μs
			Full range ⁽¹⁾	0.8			
V_n	Equivalent input noise voltage	$f = 100\text{ Hz}$ $f = 1\text{ kHz}$	$T_A = 25^\circ\text{C}$		14		nV/ $\sqrt{\text{Hz}}$
					11		
I_n	Equivalent input noise current	$f = 100\text{ Hz}$	$T_A = 25^\circ\text{C}$		0.13		pA/ $\sqrt{\text{Hz}}$
THD + N	Total harmonic distortion plus noise	$V_{O(PP)} = 4\text{ V}$ $R_L = 10\text{ k}\Omega$ $f = 10\text{ kHz}$	$T_A = 25^\circ\text{C}$	$A_V = 1$	0.004%		
				$A_V = 10$	0.01%		
				$A_V = 100$	0.04%		
$t_{(on)}$	Amplifier turn-on time	$A_V = 1\ R_L = 10\text{ k}\Omega$	$T_A = 25^\circ\text{C}$	Both channels	7.6		μs
				Channel 1 only, Channel 2 on	7.65		
				Channel 2 only, Channel 1 on	7.25		
$t_{(off)}$	Amplifier turn-off time	$A_V = 1\ R_L = 10\text{ k}\Omega$	$T_A = 25^\circ\text{C}$	Both channels	333		ns
				Channel 1 only, Channel 2 on	328		
				Channel 2 only, Channel 1 on	329		
	Gain-bandwidth product	$f = 10\text{ kHz}$ $C_L = 160\text{ pF}$ $R_L = 10\text{ k}\Omega$	$T_A = 25^\circ\text{C}$		6.4		MHz
t_s	Settling time	$V_{(STEP)PP} = 2\text{ V}$ $A_V = -1$ $C_L = 10\text{ pF}$ $R_L = 10\text{ k}\Omega$	$T_A = 25^\circ\text{C}$	0.1%	1.53		μs
				0.01%	1.83		
		$V_{(STEP)PP} = 2\text{ V}$ $A_V = -1$ $C_L = 56\text{ pF}$ $R_L = 10\text{ k}\Omega$		0.1%	3.13		
				0.01%	3.33		
ϕ_m	Phase margin at unity gain	$R_L = 10\text{ k}\Omega$ $C_L = 160\text{ pF}$	$T_A = 25^\circ\text{C}$		45		$^\circ$
	Gain margin	$R_L = 10\text{ k}\Omega$ $C_L = 160\text{ pF}$	$T_A = 25^\circ\text{C}$		7		dB

(1) Full range is -40°C to $+125^\circ\text{C}$.

6.13 Typical Characteristics

CONDITION STATEMENT TBD

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I_{IO}	Input offset current vs free-air temperature	3, 4
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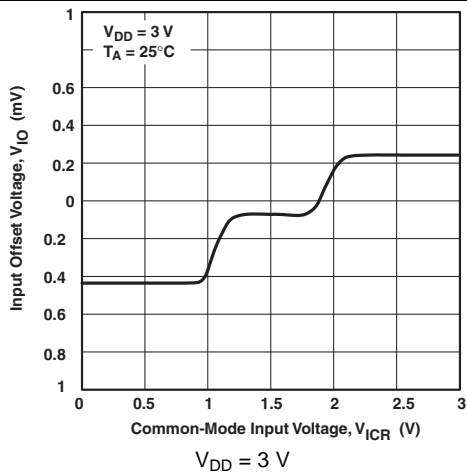


Fig. 1. Input Offset Voltage vs Common-Mode Input Voltage

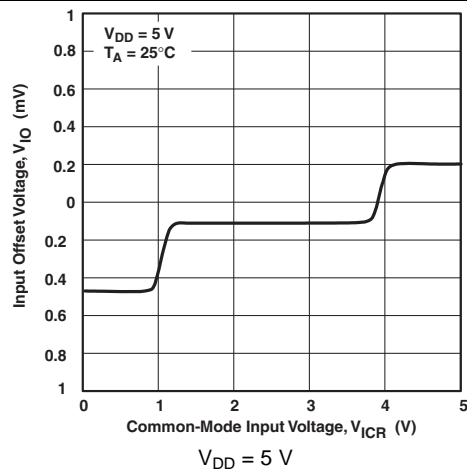


Fig. 2. Input Offset Voltage vs Common-Mode Input Voltage

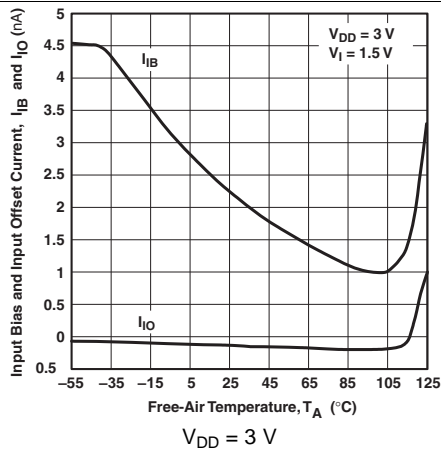


Fig. 3. Input Bias and Input Offset Current vs Free-Air Temperature

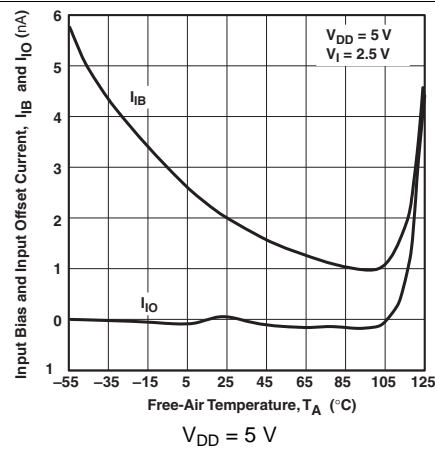


Fig. 4. Input Bias and Input Offset Current vs Free-Air Temperature

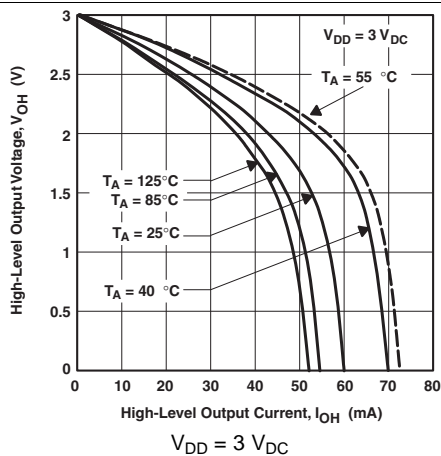


Fig. 5. High-Level Output Voltage vs High-Level Output Current

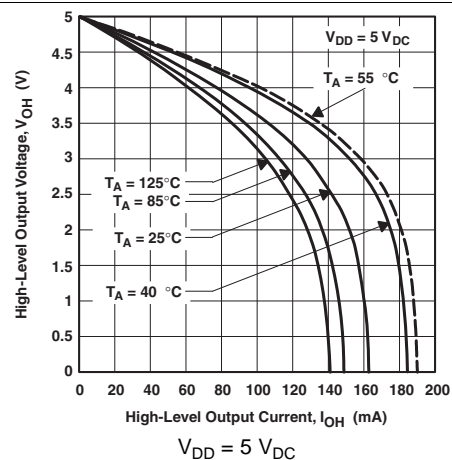
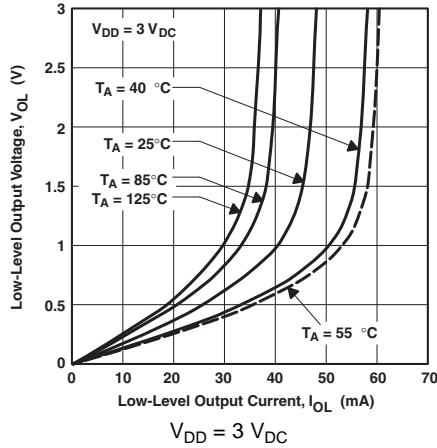
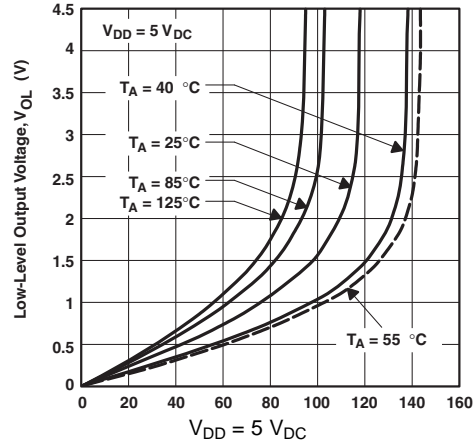


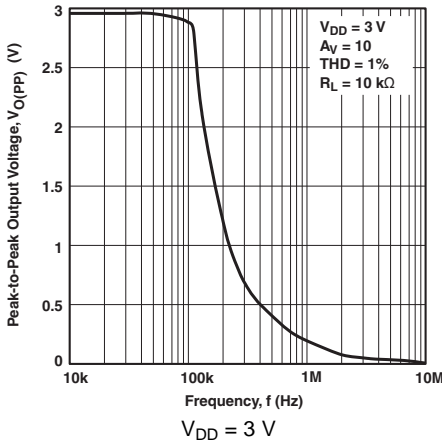
Fig. 6. High-Level Output Voltage vs High-Level Output Current



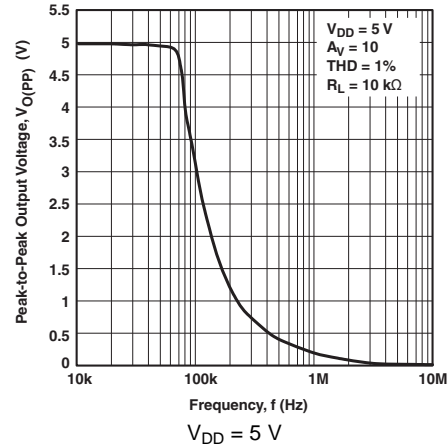
7. Low-Level Output Voltage vs Low-Level Output Current



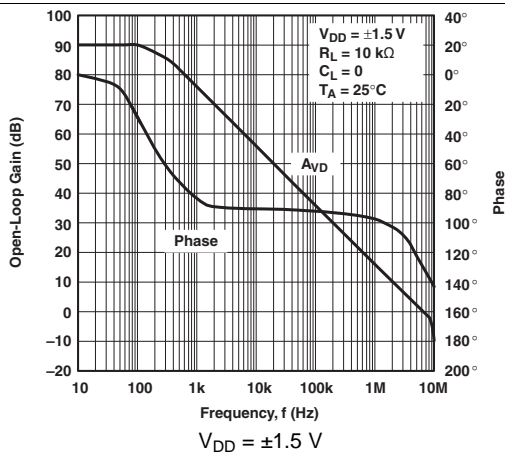
8. Low-level Output Voltage vs Low-Level Output Current



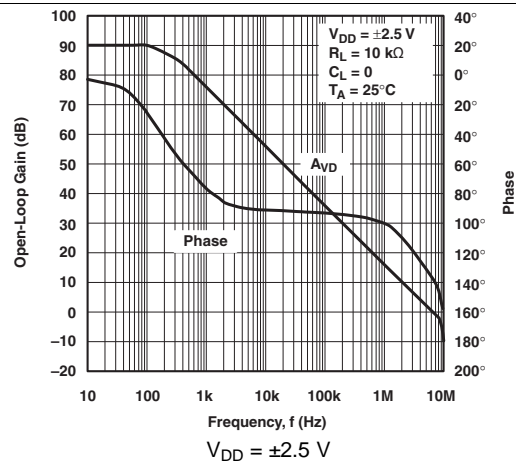
9. Peak-to-Peak Output Voltage vs Frequency



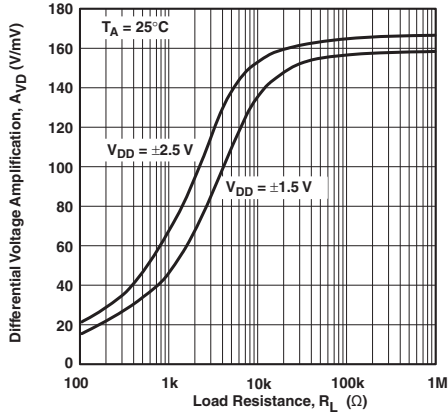
10. Peak-to-Peak Output Voltage vs Frequency



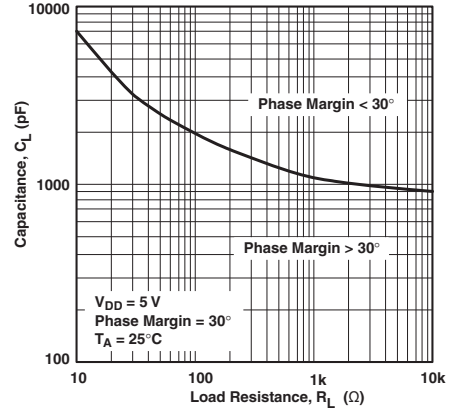
11. Open-Loop Gain and Phase vs Frequency



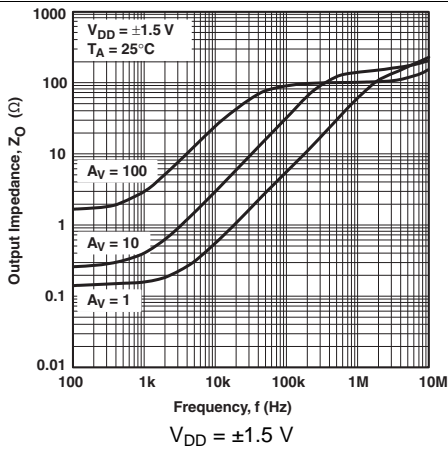
12. Open-Loop Gain and Phase vs Frequency



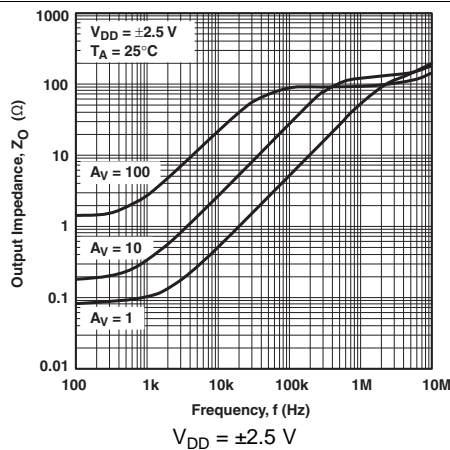
13. Differential Voltage Amplification vs Load Resistance



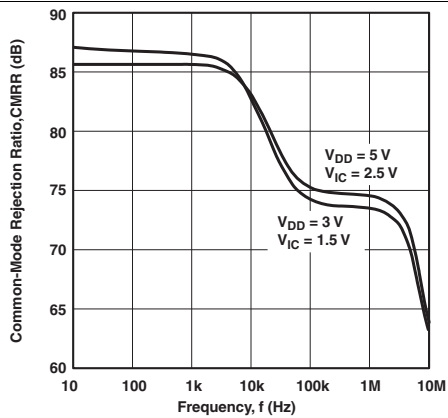
14. Capacitive Load vs Load Resistance



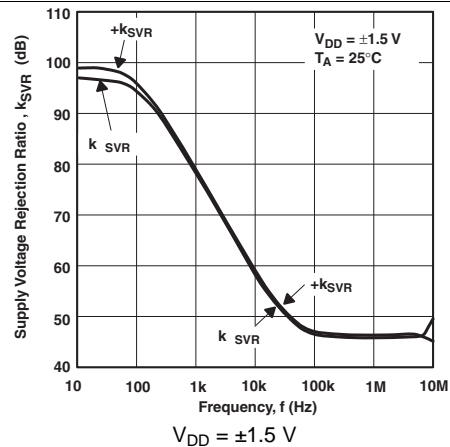
15. Output Impedance vs Frequency



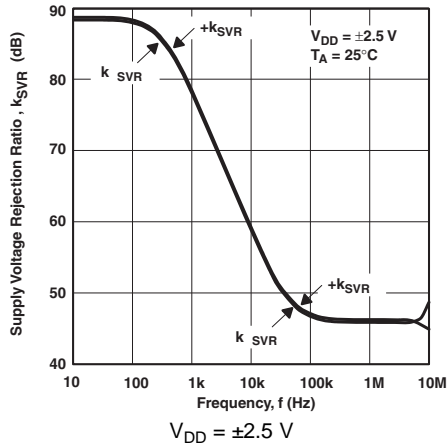
16. Output Impedance vs Frequency



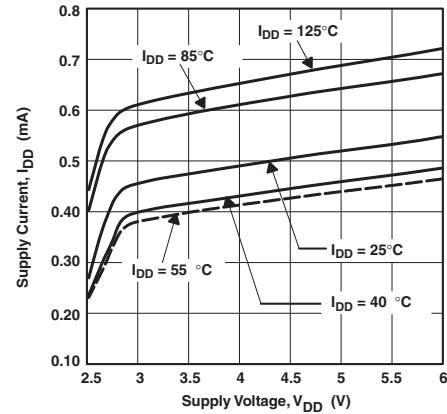
17. Common-Mode Rejection Ratio vs Frequency



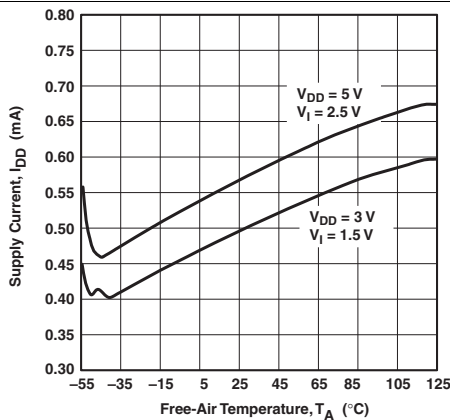
18. Supply-Voltage Rejection Ratio vs Frequency



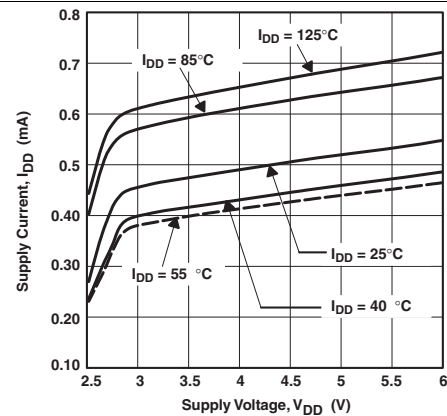
19. Supply-Voltage Rejection Ratio vs Frequency



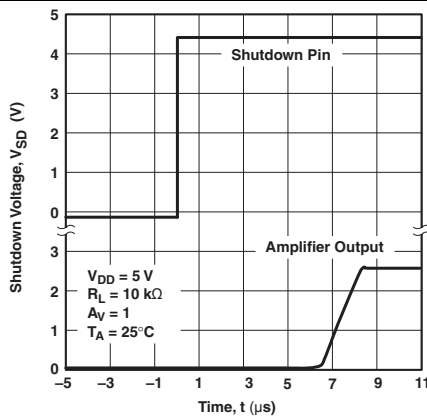
20. Supply Current vs Supply Voltage



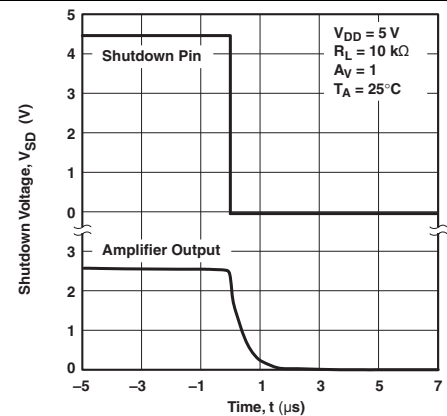
21. Supply Current vs Free-Air Temperature



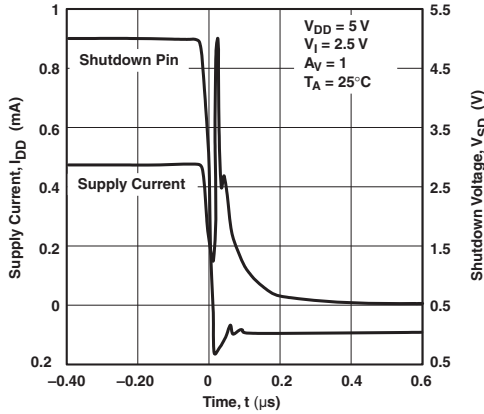
22. Amplifier With a Shutdown Pulse Turnon Characteristics



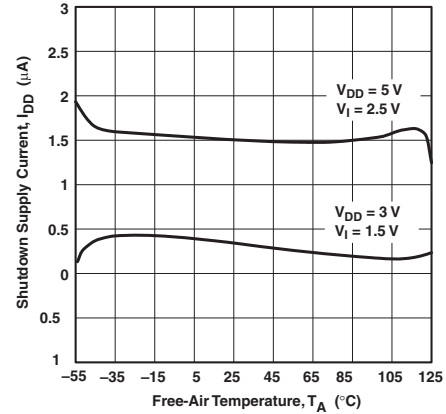
23. Amplifier With a Shutdown Pulse Turnoff Characteristics



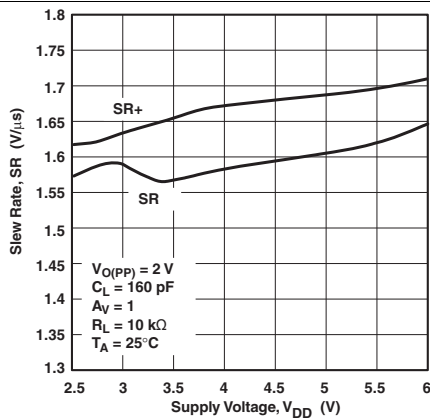
24. Supply Current With a Shutdown Pulse Turnon Characteristics



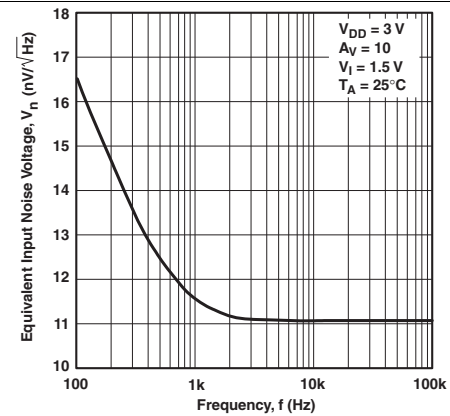
25. Turnoff Supply Current With a Shutdown Pulse



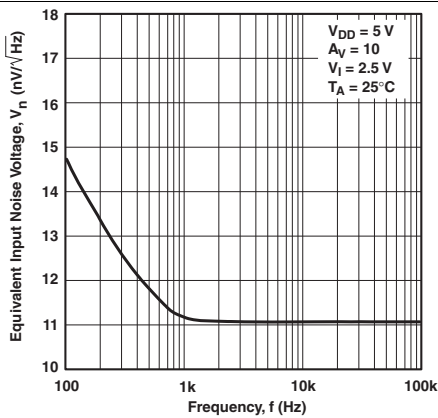
26. Shutdown Supply Current vs Free-Air Temperature



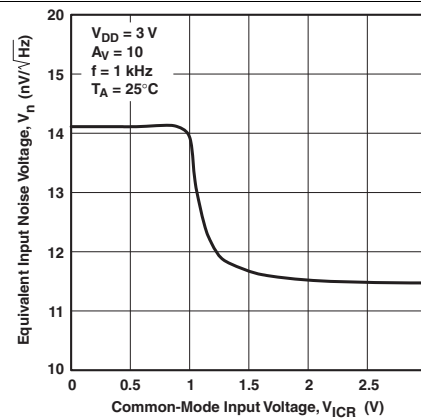
27. Slew Rate vs Supply Voltage



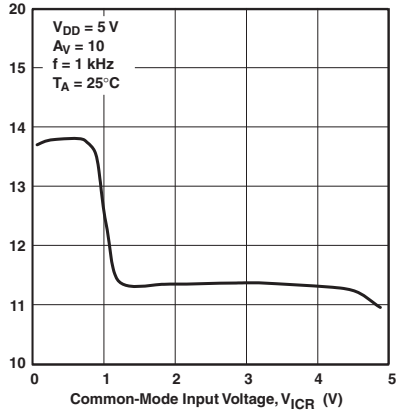
28. Equivalent Input Noise Voltage vs Frequency



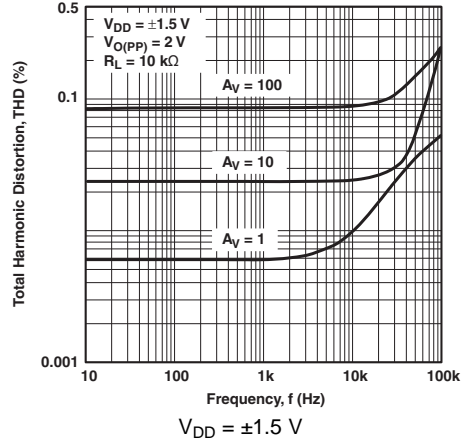
29. Equivalent Input Noise Voltage vs Frequency



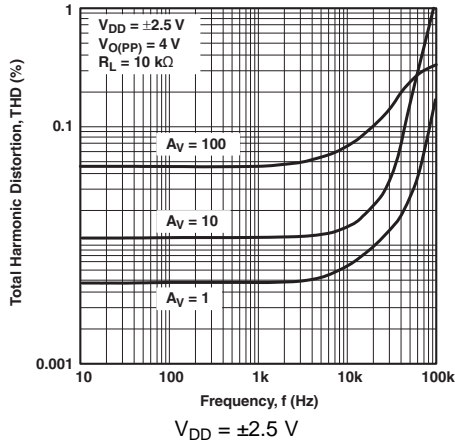
30. Equivalent Input Noise Voltage vs Common-Mode Input Voltage



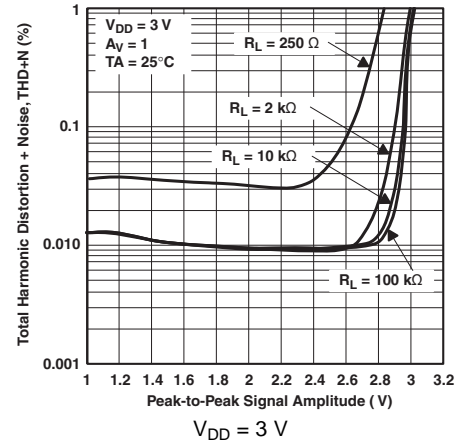
31. Equivalent Input Noise Voltage vs Common-Mode Input Voltage



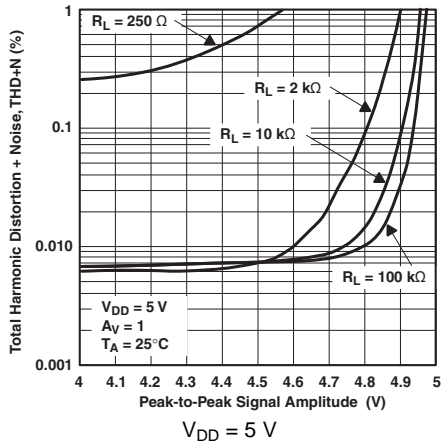
32. Total Harmonic Distortion vs Frequency



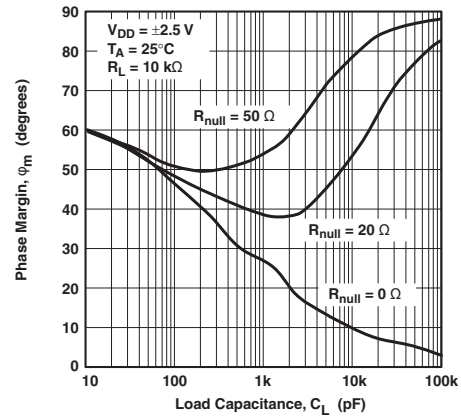
33. Total Harmonic Distortion vs Frequency



34. Total Harmonic Distortion Plus Noise vs Peak-to-Peak Signal Amplitude



35. Total Harmonic Distortion Plus Noise vs Peak-to-Peak Signal Amplitude



36. Phase Margin vs Load Capacitance

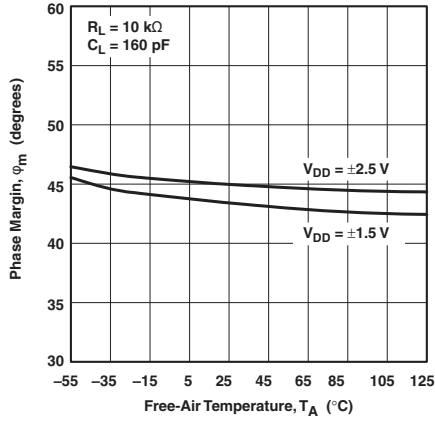


图 37. Phase Margin vs Free-Air Temperature

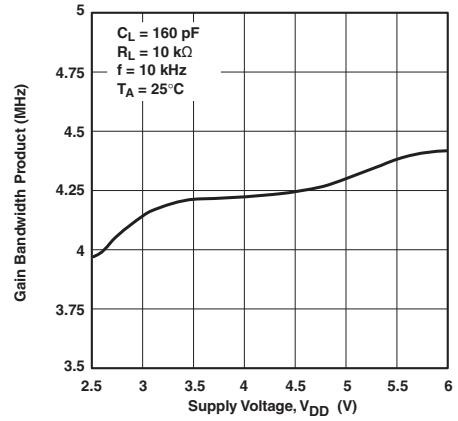


图 38. Gain Bandwidth Product vs Supply Voltage

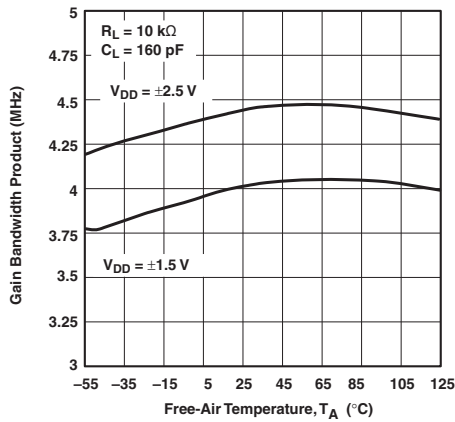


图 39. Gain Bandwidth Product vs Free-Air Temperature

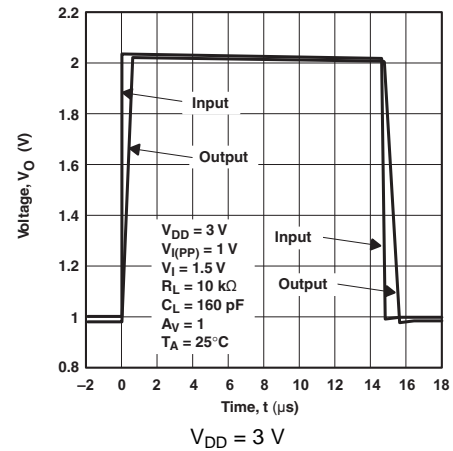


图 40. Large Signal Follower

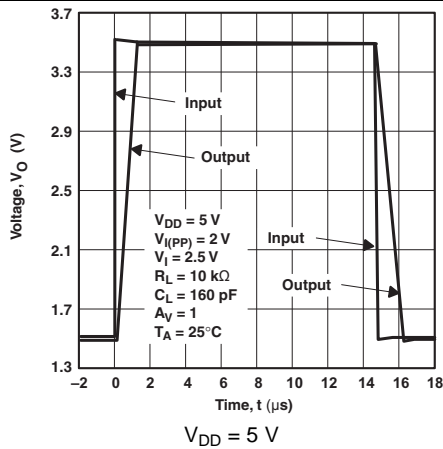


图 41. Large Signal Follower

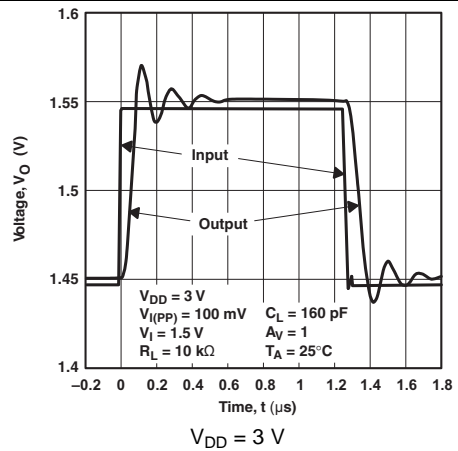
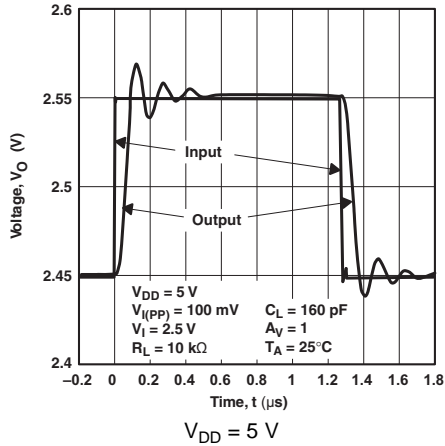
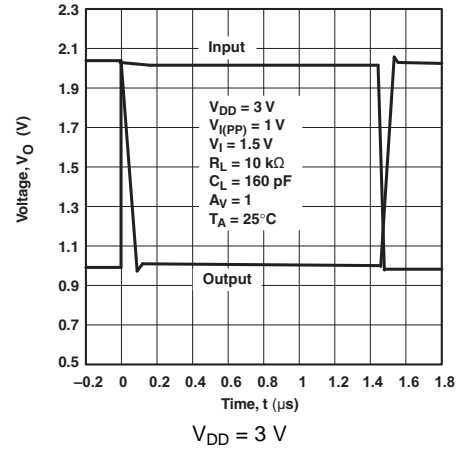


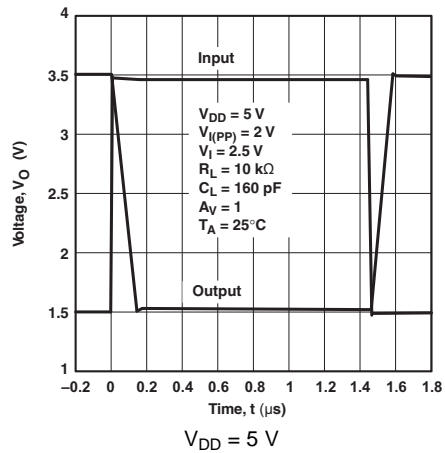
图 42. Small Signal Follower



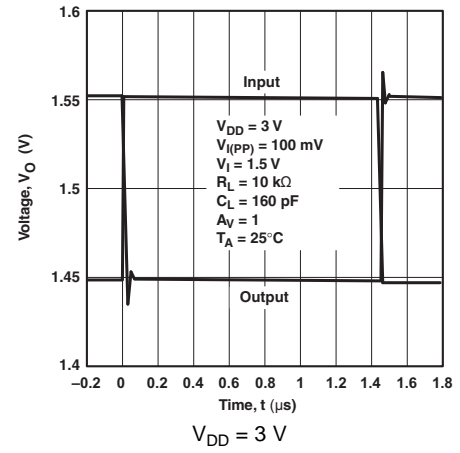
⊠ 43. Small Signal Follower



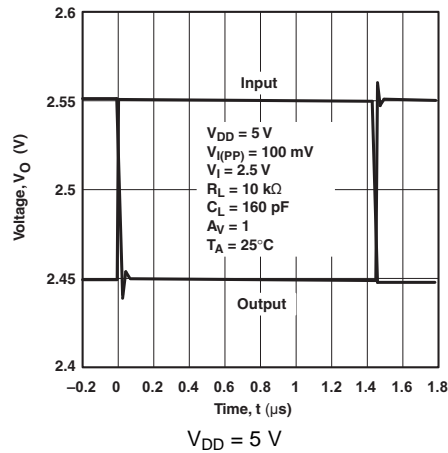
⊠ 44. Inverting Large Signal



⊠ 45. Inverting Large Signal



⊠ 46. Inverting Small Signal



⊠ 47. Inverting Small Signal

7 Parameter Measurement Information

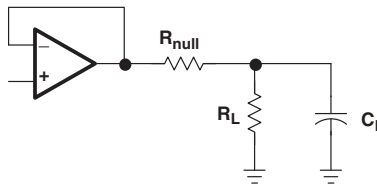


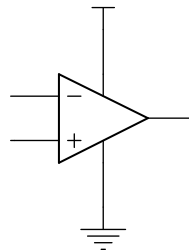
FIG 48. Capacitive Load Drive

8 Detailed Description

8.1 Overview

The TLV246x-Q1 family of devices are low-power rail-to-rail input and output operational amplifiers. The input common-mode voltage range extends beyond the supply rails for maximum dynamic range in a low-voltage system. The amplifier output has rail-to-rail performance with high drive capability, solving one of the limitations of older rail-to-rail input and output operational amplifiers.

8.2 Functional Block Diagram



8.3 Feature Description

The TLV246x-Q1 family features 6.4-MHz bandwidth and voltage noise of 11 nV/ $\sqrt{\text{Hz}}$ with performance rated from 2.7 V to 6 V across an automotive temperature range (-40°C to $+125^{\circ}\text{C}$). This family is designed for a wide range of automotive applications.

8.3.1 Driving a Capacitive Load

When the amplifier configuration is in this manner, capacitive loading directly on the output decreases the phase margin of the device leading to high-frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, TI recommends placing a resistor in series (R_{NULL}) with the output of the amplifier; see FIG 49. A minimum value of 20 Ω works well for most applications.

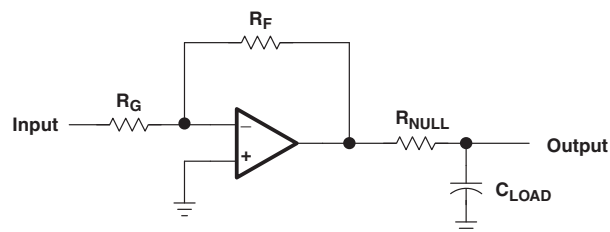
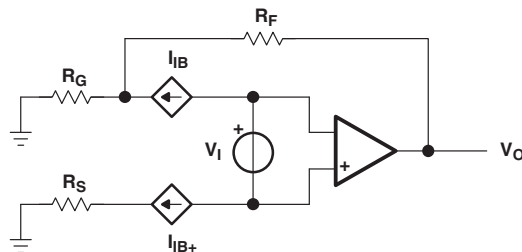


FIG 49. Driving a Capacitive Load

Feature Description (continued)

8.3.2 Offset Voltage

The output offset voltage (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input-bias currents (I_{IB}) times the corresponding gains. Use the schematic and formula in [Figure 50](#) to calculate the output offset voltage.

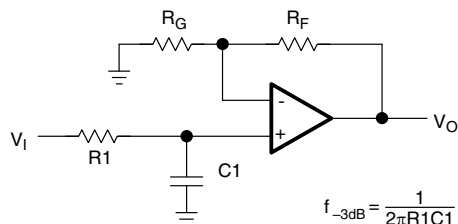


$$V_{OO} = V_{IO} \left(1 + \frac{R_F}{R_G}\right) \pm I_{IB-} R_S \left(1 + \frac{R_F}{R_G}\right) \pm I_{IB+} R_F$$

Figure 50. Output Offset Voltage Model

8.3.3 General Configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. To limit bandwidth, place an RC filter at the noninverting terminal of the amplifier (see [Figure 51](#)).

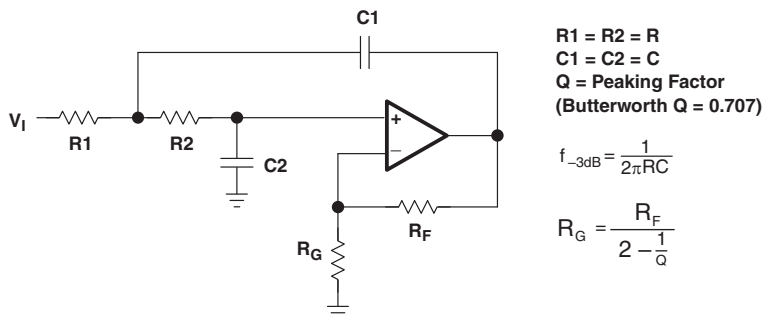


$$f_{-3dB} = \frac{1}{2\pi R_1 C_1}$$

$$\frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_G}\right) \left(\frac{1}{1 + sR_1 C_1}\right)$$

Figure 51. Single-Pole Low-Pass Filter

If even more attenuation is required, a multiple pole filter is required. Use a Sallen-Key filter for this task; see [Figure 52](#). For best results, the amplifier must have a bandwidth that is eight to ten times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.



$R_1 = R_2 = R$
 $C_1 = C_2 = C$
 $Q = \text{Peaking Factor}$
(Butterworth $Q = 0.707$)

$$f_{-3dB} = \frac{1}{2\pi RC}$$

$$R_G = \frac{R_F}{2 - \frac{1}{Q}}$$

Figure 52. 2-Pole Low-Pass Sallen-Key Filter

Feature Description (continued)

8.3.4 General Power Dissipation Considerations

For a given θ_{JA} value, the maximum power dissipation is shown in [Figure 53](#) and is calculated by [Equation 1](#):

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

- P_D = Maximum power dissipation of TLV246x-Q1 (watts)
- T_{MAX} = Absolute maximum junction temperature (150°C)
- T_A = Ambient free-air temperature (°C)
- $\theta_{JA} = \theta_{JC} + \theta_{CA}$
- θ_{JC} = Thermal coefficient from junction to case
- θ_{CA} = Thermal coefficient from case to ambient air (°C/W)

(1)

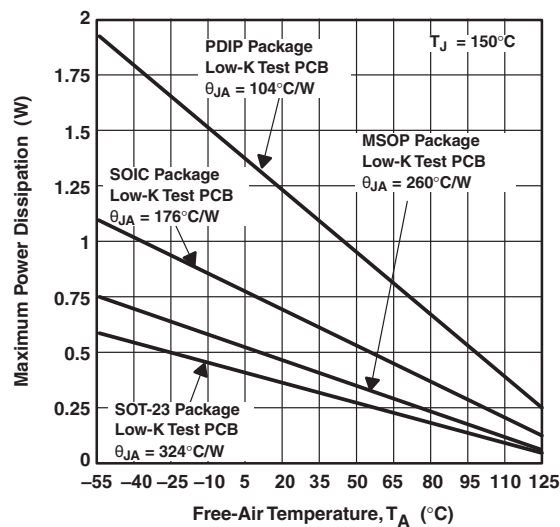


Figure 53. Maximum Power Dissipation vs Free-Air Temperature

8.4 Device Functional Modes

The TLV2461-Q1, TLV2462-Q1, and TLV2464A-Q1 devices power on when the supply is connected. These devices can operate with a single supply or dual supplies, depending on the application. The devices are in their full performance once the supply is above the recommended value. The TLV2460-Q1 and TLV2463-Q1 devices feature a shutdown mode, which reduces the quiescent current to 0.3 μA in shutdown mode.

8.4.1 Shutdown Function

Two members of the TLV246x-Q1 family (TLV2460-Q1 and TLV2463-Q1) feature a shutdown terminal that conserves battery life in portable applications. When the shutdown terminal is tied low, the supply current is reduced to 0.3 μA per channel, the amplifier is disabled and the outputs are placed in a high-impedance mode. To enable the amplifier, leave the shutdown terminal floating or pull the shutdown terminal high. When the shutdown terminal is left floating, take care to ensure that parasitic leakage current at the shutdown terminal does not inadvertently place the operational amplifier into shutdown. The shutdown terminal threshold is always referenced to $V_{\text{DD}} / 2$. As a result, when operating the device with split-supply voltages (for example, $\pm 2.5\text{ V}$), the shutdown terminal must be pulled to $V_{\text{DD-}}$ (not GND) to disable the operational amplifier.

The output of the amplifier with a shutdown pulse is shown in [Figure 22](#), [Figure 23](#), [Figure 24](#), and [Figure 25](#). The amplifier is powered with a single 5-V supply and configured as a noninverting configuration with a gain of 5. The amplifier turnon and turnoff times are measured from the 50% point of the shutdown pulse to the 50% point of the output waveform. The times for the single, dual, and quad are listed in the data tables.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Most DC-to-DC converters use output-filter ceramic capacitors with very low equivalent series resistance (ESR).

This causes a double pole at the resonance frequency $\frac{1}{2\pi\sqrt{LC}}$.

To achieve an adequate bandwidth and phase margin for the DC-to-DC converter, the device requires

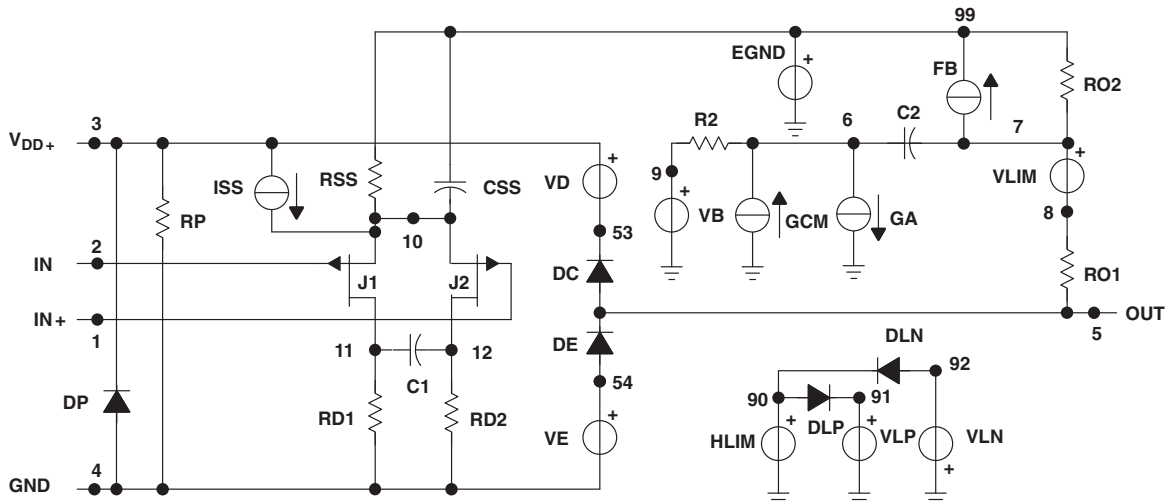
compensation around the $\frac{1}{2\pi\sqrt{LC}}$ resonance frequency. To achieve this, configure the error amplifier as type-3 compensation. The TLV2426x-Q1 series features a wide bandwidth UGBD of 6 MHz with rail-to-rail output for increased dynamic range. These features are designed for DC-to-DC loop compensation with any LC filter.

9.1.1 Macromodel Information

Macromodel information provided was derived using Microsim Parts™ Release 8, the model generation software used with Microsim PSpice™. The Boyle macromodel ⁽¹⁾ and subcircuit in [Figure 54](#) are generated using the TLV246x-Q1 typical electrical and operating characteristics at $T_A = 25^\circ\text{C}$. Using this information, output simulations of the following key parameters are generated to a tolerance of 20% (in most cases):

(1) G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit



```
.SUBCKT TLV246X 1 2 3 4 5
C1 11 12 2.46034E-12
C2 6 7 10.0000E-12
CSS 10 99 443.21E-15
DC 5 53 DY
DE 54 5 DY
DLP 90 91 DX
DLN 92 90 DX
DP 4 3 DX
EGND 99 0 POLY (2) (3,0) (4,0) 0 .5 .5
FB 7 99 POLY (5) VB VC VE VLP
+ VLN 0 21.600E6 - 1E3 1E3 22E6 - 22E6
GA 6 0 11 12 345.26E- 6
GCM 0 6 10 99 15.4226E- 9
ISS 10 4 DC 18.850E- 6
HLIM 90 0 VLIM 1K
J1 11 2 10 JX1
J2 12 1 10 JX2
R2 6 9 100.00E3
```

```
RD1 3 11 2.8964E3
RD2 3 12 2.8964E3
RO1 8 5 5.6000
RO2 7 99 6.2000
RP 3 4 8.9127
RSS 10 99 10.610E6
VB 9 0 DC 0
VC 3 53 DC .7836
VE 54 4 DC .7436
VLIM 7 8 DC 0
VLP 91 0 DC 117
VLN 0 92 DC 117
.MODEL DX D (IS=800.00E-18)
.MODEL DY D (IS=800.00E-18 Rs = 1m Cjo=10p)
.MODEL JX1 NJF (IS=1.0000E-12 BETA=6.3239E-3
+ VTO=-1)
.MODEL JX2 NJF (IS=1.0000E-12 BETA=6.3239E-3
+ VTO=-1)
.ENDS
```

```
.subckt TLV_246Y 1 2 3 4 5 6
c1 11 12 2.4603E-12
c2 72 7 10.000E-12
css 10 99 443.21E-15
dc 70 53 dy
de 54 70 dy
dip 90 91 dx
din 92 90 dx
dp 4 3 dx
egnd 99 0 poly(2) (3,0) (4,0) 0 .5 .5
fb 7 99 poly(5) vb vc ve vlp vln 0
21.600E6 - 1E3 1E3 22E6 - 22E6
ga 72 0 11 12 345.26E- 6
gcm 0 72 10 99 15.422E- 9
iss 74 4 dc 18.850E- 6
hlim 90 0 vlim 1K
j1 11 2 10 jx1
j2 12 1 10 jx2
r2 72 9 100.00E3
rd1 3 11 2.8964E3
rd2 3 12 2.8964E3
ro1 8 70 5.6000
ro2 7 99 6.2000
```

```
rp 3 71 8.9127
rss 10 99 10.610E6
rs1 6 4 1G
rs2 6 4 1G
rs3 6 4 1G
rs4 6 4 1G
s1 71 4 6 4 s1x
s2 70 5 6 4 s1x
s3 10 74 6 4 s1x
s4 74 4 6 4 s2x
vb 9 0 dc 0
vc 3 53 dc .7836
ve 54 4 dc .7436
vlim 7 8 dc 0
vlp 91 0 dc 117
vln 0 92 dc 117
.model dx D(Is=800.00E-18)
.model dy D(Is=800.00E-18 Rs=1m Cjo=10p)
.model jx1 NJF(Is=1.0000E-12 Beta=6.3239E-3 Vto=-1)
.model jx2 NJF(Is=1.0000E-12 Beta=6.3239E-3 Vto=-1)
.model s1x VSWITCH(Roff=1E8 Ron=1.0 Voff=2.5 Von=0.0)
.model s2x VSWITCH(Roff=1E8 Ron=1.0 Voff=0 Von=2.5)
.ends
```

54. Boyle Macromodel and Sub-Circuit

9.2 Typical Application

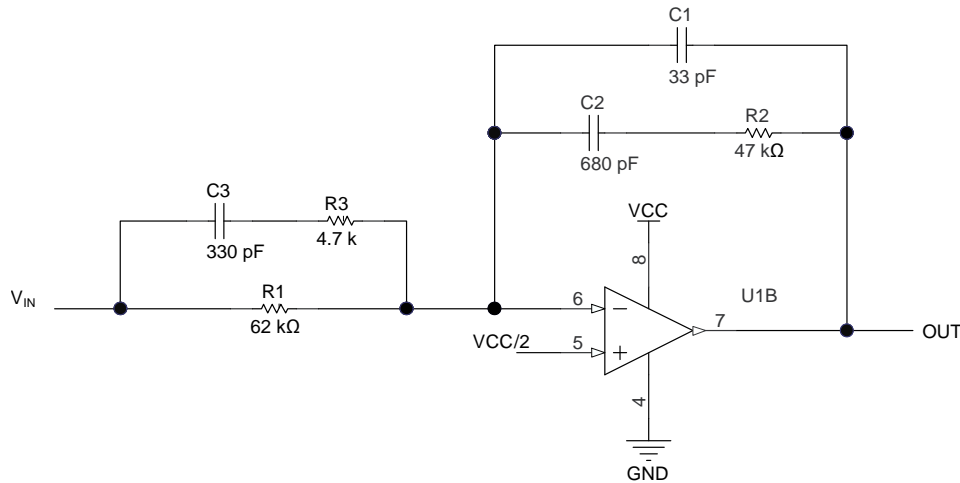


图 55. Typical Operational Amplifier Application

9.2.1 Design Requirements

See 表 2 for design requirements.

表 2. Recommended Design Parameters

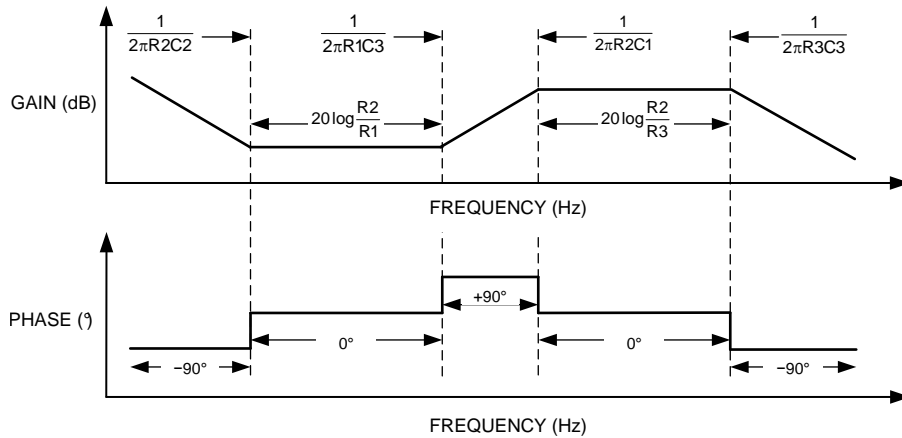
PARAMETER	VALUE
Supply voltage	5 V
Reference voltage	2.5 V
Input voltage	2.5 V DC and maximum ripple 40 mV peak-to-peak
Capacitors	Better than X5R
Resistors	Better than 2% tolerance

9.2.2 Detailed Design Procedure

The following section shows the detailed design procedure. See 式 2 for the type-3 compensation gain.

$$\text{Type 3 Compensation Gain} = \frac{(1 + R2C2s)(1 + (R1 + R3)C3s)}{R1(C1 + C2)s(1 + R2 \frac{C1C2}{C1 + C2}s)(1 + R3Cs)} \quad (2)$$

Type-3 compensation poles and zeros are shown in the preferred asymptotic graph; see 图 56. Relocate the compensation poles and zeroes by changing the values of the resistors and capacitors according to the compensation requirement. The operational amplifier cannot achieve the preferred case because of the open-loop gain and phase limitation of the amplifier.



56. Preferred Asymptotic Graph

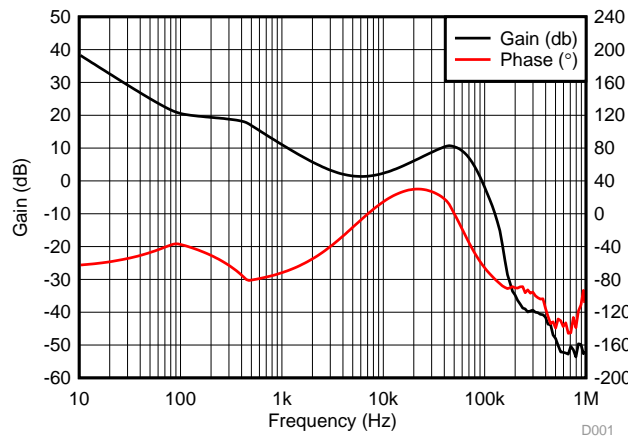
The poles and zeros are calculated assuming $C2 \gg C1$ and $R1 \gg R3$. This assumption is correct because the $C1$ and $R3$ components set the high frequencies.

This TLV226x-Q1 device type-3 compensation circuit design boosts the gain and phase for the DC-to-DC converter around 30-KHz resonance frequencies. This corresponds to 1 μ H and 22 μ F for the output filter.

The operational amplifier is configured as type-2 compensation by omitting the $C3$ capacitor. Type-2 compensates the DC-to-DC converter with an output capacitor with a series resistor ESR; see 式 3.

$$\text{Type 2 Compensation Gain} = \frac{(1 + R2C2s)}{R1(C1 + C2) s (1 + R2 \frac{C1C2}{C1+C2} s)} \quad (3)$$

9.2.3 Application Curve



Frequency: 10 Hz to 1 MHz Gain boost = 12 dB around 30 KHz Phase boost = 30° around 30 KHz

57. Gain and Phase Plot

10 Power Supply Recommendations

The TLV246X-Q1 family of devices operation specification is from 2.7 V to 6 V for a single power supply and ± 1.35 V to ± 3 V for dual power supplies.

TI recommends placing a 0.1- μ F bypass capacitor close to the power supply pins to reduce errors coupling in from noisy or high-impedance power supplies.

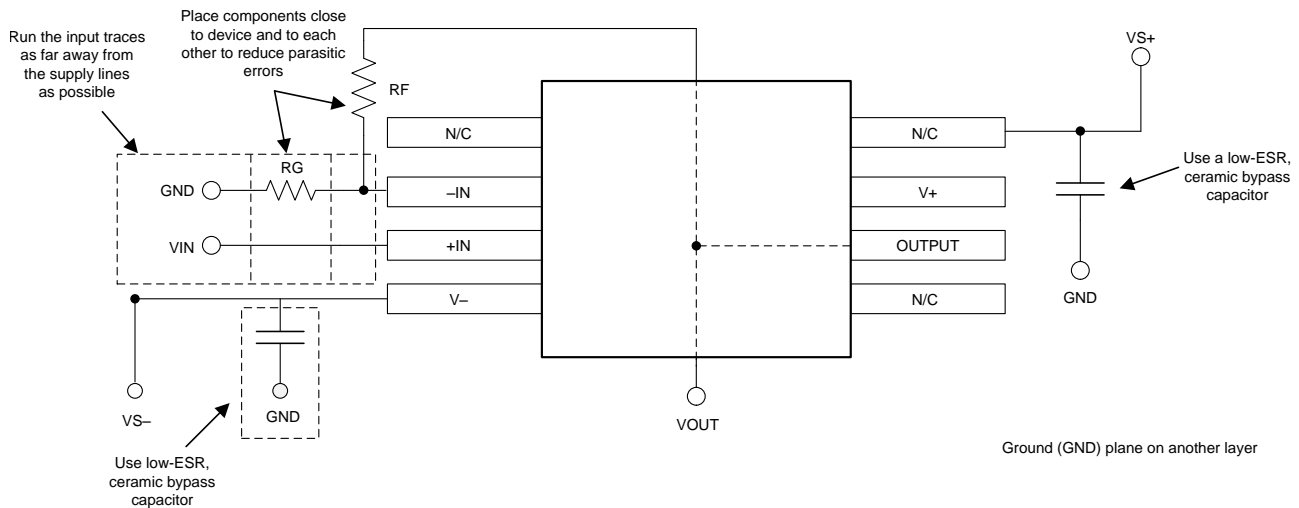
11 Layout

11.1 Layout Guidelines

To achieve the levels of high performance of the TLV246x-Q1, follow proper printed-circuit board design techniques. A general set of guidelines is shown in the following list.

- TI recommends using a ground plane on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane is removed to minimize the stray capacitance.
- Use a 6.8- μ F tantalum capacitor in parallel with a 0.1- μ F ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1- μ F ceramic capacitor must always be used on the supply terminal of every amplifier. In addition, the 0.1- μ F capacitor must be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer must strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- TI does not recommend using sockets. The additional lead inductance in the socket pins often leads to stability problems. For best implementation, solder surface-mount packages directly to the printed circuit board.
- Optimum high performance is achieved when stray series inductance is minimized. The circuit layout must be made as compact as possible, which minimizes the length of all trace runs. Take care to pay attention to the inverting input of the amplifier; keep the length as short as possible. This minimizes stray capacitance at the input of the amplifier.
- TI recommends using surface mount passive components for high performance amplifier circuits. Stray series inductance is reduced because of the low lead inductance of surface mount components.. The small size of surface-mount components leads to a compact layout, which minimizes stray inductance and capacitance. TI recommends that lead lengths be kept as short as possible if leaded components are used.

11.2 Layout Example



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58. Operational Amplifier Board Layout for Noninverting Configuration

12 デバイスおよびドキュメントのサポート

12.1 ドキュメントのサポート

12.1.1 関連資料

関連資料については、以下を参照してください。

- テキサス・インスツルメンツ、『オーディオ回路コレクション、第1部』
- G. R. Boyle, B. M. Cohn, D. O. Pederson, J. E. Solomon 共著、『集積回路オペアンプのマクロモデル化』、*IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974)

12.2 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 3. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
TLV2460-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TLV2461-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TLV2462-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TLV2463-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TLV2460A-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TLV2461A-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TLV2462A-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TLV2463A-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TLV2464A-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

12.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ オンライン・コミュニティ TI の E2E (Engineer-to-Engineer) コミュニティ。 エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.com では、他のエンジニアに質問し、知識を共有し、アイデアを検討して、問題解決に役立てることができます。

設計サポート TI の設計サポート 役に立つ E2E フォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

12.4 商標

E2E is a trademark of Texas Instruments.
 All other trademarks are the property of their respective owners.

12.5 静電気放電に関する注意事項



これらのデバイスは、限定的な ESD (静電破壊) 保護機能を内蔵しています。保存時または取り扱い時は、MOS ゲートに対する静電破壊を防止するために、リード線同士をショートさせておくか、デバイスを導電フォームに入れる必要があります。

12.6 Glossary

[SLYZ022](#) — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2460AQPWRG4Q1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2460AQ	Samples
TLV2461AQPWRG4Q1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2461AQ	Samples
TLV2462AQDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2462AQ	Samples
TLV2462AQPWRG4Q1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2462AQ	Samples
TLV2462AQPWRQ1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2462AQ	Samples
TLV2462QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	QVM	Samples
TLV2462QDRG4Q1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2462Q1	Samples
TLV2462QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2462Q1	Samples
TLV2462QPWRG4Q1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2462Q1	Samples
TLV2463AQPWRG4Q1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2463AQ1	Samples
TLV2464AQPWRG4Q1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2464AQ	Samples
TLV2464AQPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2464AQ	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TLV2460A-Q1, TLV2461A-Q1, TLV2462-Q1, TLV2462A-Q1, TLV2463A-Q1, TLV2464A-Q1 :

- Catalog : [TLV2460A](#), [TLV2461A](#), [TLV2462](#), [TLV2462A](#), [TLV2463A](#), [TLV2464A](#)
- Enhanced Product : [TLV2462A-EP](#), [TLV2464A-EP](#)
- Military : [TLV2462M](#), [TLV2462AM](#), [TLV2463AM](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2460AQPWRG4Q1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV2461AQPWRG4Q1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV2462AQPWRG4Q1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV2462AQPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV2462QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2462QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2462QPWRG4Q1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV2463AQPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2464AQPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2464AQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2460AQPWRG4Q1	TSSOP	PW	8	2000	367.0	367.0	35.0
TLV2461AQPWRG4Q1	TSSOP	PW	8	2000	367.0	367.0	35.0
TLV2462AQPWRG4Q1	TSSOP	PW	8	2000	367.0	367.0	35.0
TLV2462AQPWRQ1	TSSOP	PW	8	2000	356.0	356.0	35.0
TLV2462QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
TLV2462QDGKRQ1	VSSOP	DGK	8	2500	346.0	346.0	29.0
TLV2462QPWRG4Q1	TSSOP	PW	8	2000	367.0	367.0	35.0
TLV2463AQPWRG4Q1	TSSOP	PW	14	2000	367.0	367.0	35.0
TLV2464AQPWRG4Q1	TSSOP	PW	14	2000	367.0	367.0	35.0
TLV2464AQPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW0008A



PACKAGE OUTLINE
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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