

## TLV716/P Capacitor-Free, Dual, 150-mA, Low-Dropout Voltage Regulator in 1.2-mm x 1.2-mm SON Package

### 1 Features

- No Input or Output Capacitors Required
- Inrush Current Control
- Low Crosstalk
- Accuracy: 1.5% (–40°C to 125°C)
- Input Voltage Range: 1.4 V to 5.5 V
- Multiple Fixed-Output Voltage Combinations Possible from 1 V to 3.3 V
- Foldback Current Limit Protection
- Package: 1.2-mm x 1.2-mm SON-6 (DPQ)

### 2 Applications

- Wireless Handsets, Smart Phones, Tablets
- Set-Top Boxes (STBs), Cameras, Modems
- Portable Battery-Powered Products

### 3 Description

The TLV716 is a family of dual-channel, capacitor-free, 150-mA, low-dropout (LDO) voltage regulators with multiple fixed-output options available from 1 V to 3.3 V. These devices provide an initial 1% accuracy and 1.5% accuracy overtemperature.

The TLV716 family is designed to be stable with or without an input or output capacitor. Eliminating the output capacitor allows for a very small solution size. The TLV716P series provides an active pulldown circuit to quickly discharge the output voltage if the application requires an output capacitor.

The device provides inrush current control during device power up and enabling. Inrush control provides constant-current charging of the output load during start-up, thereby reducing the risk of an undesired overcurrent fault from the input supply or battery.

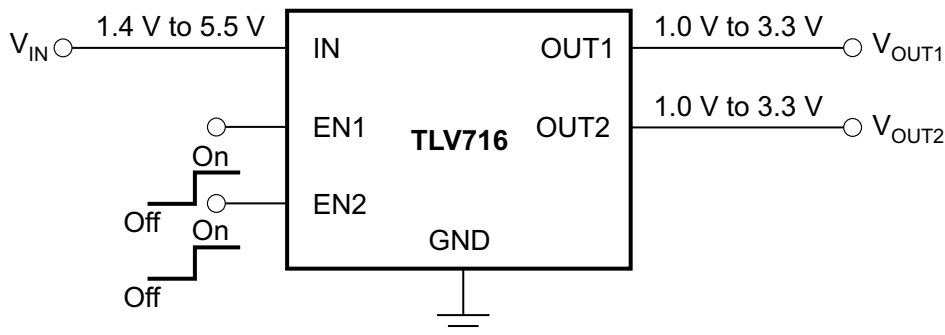
The TLV716 family is available in a 1.2-mm x 1.2-mm SON-6 package and is ideal for space-constrained applications.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV716	X2SON (6)	1.20 mm x 1.20 mm
TLV716P		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Typical Application Circuit



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## 4 Revision History

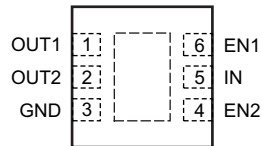
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision A (September 2013) to Revision B</b>	<b>Page</b>
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	1
• Deleted (LDO) from title.....	1
• Changed Accuracy bullet from 1% to 1.5% and added temperature range (–40°C to 125°C) .....	1

<b>Changes from Original (June 2013) to Revision A</b>	<b>Page</b>
• Changed document status from Product Preview to Production Data; pre-RTM changes made throughout.....	1
• Changed junction temperature range in second paragraph of <i>Overview</i> section .....	10

## 5 Pin Configuration and Functions

DPQ Package  
6-Pin X2SON  
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT1	1	O	Regulated output voltage pin. See the <a href="#">Input and Output Capacitor Requirements</a> section for more details.
OUT2	2	O	Regulated output voltage pin. See the <a href="#">Input and Output Capacitor Requirements</a> section for more details.
GND	3	—	Ground pin.
EN2	4	I	Enable pin for regulator 2. Driving EN2 over 0.9 V turns on regulator 2. Driving EN2 below 0.4 V places regulator 2 into shutdown mode.
IN	5	I	Input voltage pin. See the <a href="#">Input and Output Capacitor Requirements</a> section for more details.
EN1	6	I	Enable pin for regulator 1. Driving EN1 over 0.9 V turns on regulator 1. Driving EN1 below 0.4 V places regulator 1 into shutdown mode.
PAD	—	—	Connecting the thermal pad to the ground plane improves the thermal performance.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

at  $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$ , unless otherwise noted. <sup>(1)</sup>

		MIN	MAX	UNIT
Voltage <sup>(2)</sup>	IN	-0.3	6	V
	EN1, EN2	-0.3	$V_{IN} + 0.3$	V
	OUT1, OUT2	-0.3	$3.6$ or $V_{IN} + 0.3$	V
Current, OUT1, OUT2		-30	Internally limited	mA
Output short circuit duration		Indefinite		s
$T_J$	Operating junction temperature	-55	150	$^\circ\text{C}$
$T_{stg}$	Storage temperature	-55	150	$^\circ\text{C}$

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground.

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	$\pm 2000$	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	$\pm 500$	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
$V_{IN}$	Input voltage	1.4		5.5	V
$V_{EN}$	Enable range: $V_{EN1}$ , $V_{EN2}$	0		$V_{IN}$	V
$I_{OUT}$	Output current: $I_{OUT1}$ , $I_{OUT2}$	0		150	mA
$C_{IN}$	Input capacitor	0	1		$\mu\text{F}$
$C_{OUT}$	Output capacitor: $C_{OUT1}$ , $C_{OUT2}$	0	0.1	100	$\mu\text{F}$
$T_J$	Operating junction temperature range	-40		125	$^\circ\text{C}$

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TLV716, TLV716P	UNIT
		DPQ (X2SON)	
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	149.3	$^\circ\text{C}/\text{W}$
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	93	$^\circ\text{C}/\text{W}$
$R_{\theta JB}$	Junction-to-board thermal resistance	110.1	$^\circ\text{C}/\text{W}$
$\Psi_{JT}$	Junction-to-top characterization parameter	3.4	$^\circ\text{C}/\text{W}$
$\Psi_{JB}$	Junction-to-board characterization parameter	114.9	$^\circ\text{C}/\text{W}$
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	91	$^\circ\text{C}/\text{W}$

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

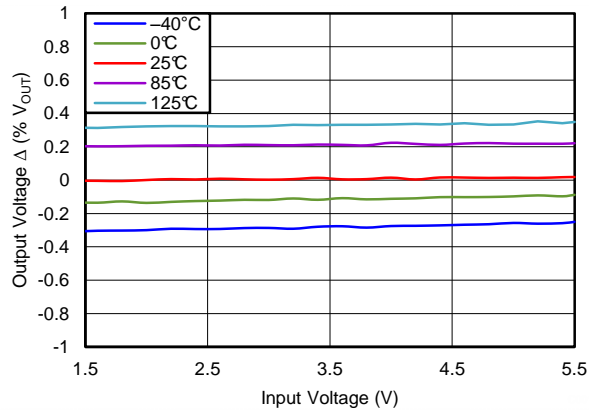
over operating temperature range of  $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $V_{IN} = V_{OUT(TYP)} + 0.5\text{ V}$  or  $2\text{ V}$  (whichever is greater),  $I_{OUT} = 1\text{ mA}$ ,  $V_{EN1} = V_{EN2} = 0.9\text{ V}$ , and  $C_{IN} = C_{OUT1} = C_{OUT2} = 1\text{ }\mu\text{F}$ , unless otherwise noted. Typical values are at  $T_J = 25^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT		
$V_{IN}$	Input voltage range	1.4		5.5	V		
$V_{OUT}$	Output voltage accuracy	$T_J = 25^{\circ}\text{C}$ , $V_{OUT} > 1.2\text{ V}$	-1%	0.33%	1%		
		$T_J = 25^{\circ}\text{C}$ , $V_{OUT} \leq 1.2\text{ V}$	-20		20	mV	
		$T_J = -40^{\circ}\text{C}$ to $85^{\circ}\text{C}$ , $V_{OUT} > 1.2\text{ V}$	-1.5%		1.5%		
		$T_J = -40^{\circ}\text{C}$ to $85^{\circ}\text{C}$ , $V_{OUT} \leq 1.2\text{ V}$	-50		50	mV	
$I_{OUT}$	Output current	Each channel			150	mA	
$\Delta V_{OUT} / \Delta V_{IN}$	Line regulation	$V_{OUT} + 0.5\text{ V} < V_{IN} \leq 5.5\text{ V}$			0.02	0.2	%/V
$\Delta V_{OUT} / \Delta I_{OUT}$	Load regulation	$1\text{ mA} < I_{OUT} < 150\text{ mA}$			0.07	0.2	mV/mA
$\Delta V_{OUT} / \Delta I_{OUT}$	Cross load regulation	$1\text{ mA} < I_{OUT} < 150\text{ mA}$			0.005	0.066	mV/mA
$V_{DO}$	Dropout voltage	$I_{OUT} = 150\text{ mA}$ , $1\text{ V} \leq V_{OUT} < 1.2\text{ V}$		0.78	1	V	
		$I_{OUT} = 150\text{ mA}$ , $1.2\text{ V} \leq V_{OUT} < 1.8\text{ V}$		0.6	0.9	V	
		$I_{OUT} = 150\text{ mA}$ , $1.8\text{ V} \leq V_{OUT} < 2.1\text{ V}$		0.35	0.575	V	
		$I_{OUT} = 150\text{ mA}$ , $2.1\text{ V} \leq V_{OUT} < 2.5\text{ V}$		0.29	0.48	V	
		$I_{OUT} = 150\text{ mA}$ , $2.5\text{ V} \leq V_{OUT} < 3\text{ V}$		0.23	0.45	V	
		$I_{OUT} = 150\text{ mA}$ , $3\text{ V} \leq V_{OUT} < 3.3\text{ V}$		0.21	0.42	V	
$V_{HI}$	Enable high voltage	0.9		$V_{IN}$	V		
$V_{LO}$	Enable low voltage	0		0.4	V		
$R_{PD}$	Output pulldown resistance	TLV716P only			120	$\Omega$	
$I_{CL}$	Output current limit	$V_{IN} = V_{OUT(TYP)} + 0.5\text{ V}$ or $2.1\text{ V}$ (whichever is greater)			160	500	mA
$I_{SC}$	Output short current limit	$V_{OUT} = 0\text{ V}$			40		mA
$I_{GND}$	Ground pin current	Per channel, $I_{OUT} = 0\text{ mA}$ , $V_{IN} = 5.5\text{ V}$			50	75	$\mu\text{A}$
$I_{SHUTDOWN}$	Shutdown current	Per channel, $V_{IN} = 5.5\text{ V}$ , $T_J = 25^{\circ}\text{C}$			0.1	1	$\mu\text{A}$
PSRR	Power-supply rejection ratio	$f = 100\text{ Hz}$ , $V_{OUT} = 2.8\text{ V}$ , $I_{OUT} = 30\text{ mA}$			80		dB
		$f = 10\text{ kHz}$ , $V_{OUT} = 2.8\text{ V}$ , $I_{OUT} = 30\text{ mA}$			46		dB
$V_N$	Output noise voltage	BW = 10 Hz to 100 kHz, $V_{OUT} = 1.8\text{ V}$ , $V_{IN} = 2.3\text{ V}$ , $I_{OUT} = 10\text{ mA}$			70		$\mu\text{V}_{RMS}$
$t_{STR}$	Start-up time <sup>(1)</sup>	$V_{OUT} = 1\text{ V}$ , $I_{OUT} = 150\text{ mA}$			170		$\mu\text{s}$
		$V_{OUT} = 3.3\text{ V}$ , $I_{OUT} = 150\text{ mA}$			900		$\mu\text{s}$
$T_{SD}$	Thermal shutdown temperature	Shutdown, temperature increasing			158		$^{\circ}\text{C}$
		Reset, temperature decreasing			140		$^{\circ}\text{C}$
$T_J$	Operating Junction Temperature				-40	125	$^{\circ}\text{C}$

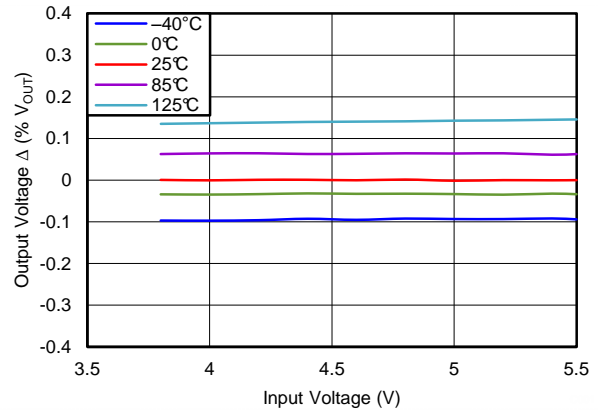
(1) Start-up time = time from EN assertion to  $0.98 \times V_{OUT(NOM)}$ .

### 6.6 Typical Characteristics

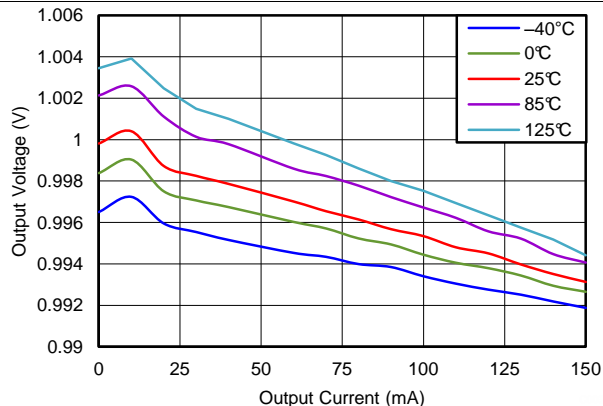
Over operating temperature range of  $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $V_{IN} = V_{OUT(TYP)} + 0.5\text{ V}$  or  $2\text{ V}$  (whichever is greater),  $V_{EN1} = V_{EN2} = V_{IN}$ ,  $I_{OUT1} = I_{OUT2} = 10\text{ mA}$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{OUT1} = 1\text{ }\mu\text{F}$ , and  $C_{OUT2} = 1\text{ }\mu\text{F}$ , unless otherwise noted. Output current plots show typical performance with a single output current sweep. Typical values are at  $T_J = 25^{\circ}\text{C}$ .



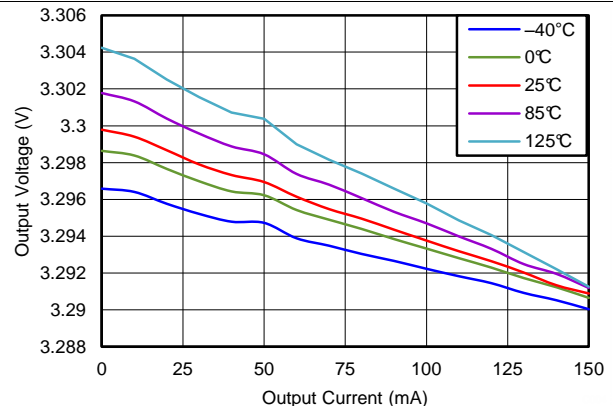
**Figure 1. Line Regulation**  
%V<sub>OUT</sub> Deviation vs V<sub>IN</sub> (V<sub>OUT</sub> = 1 V)



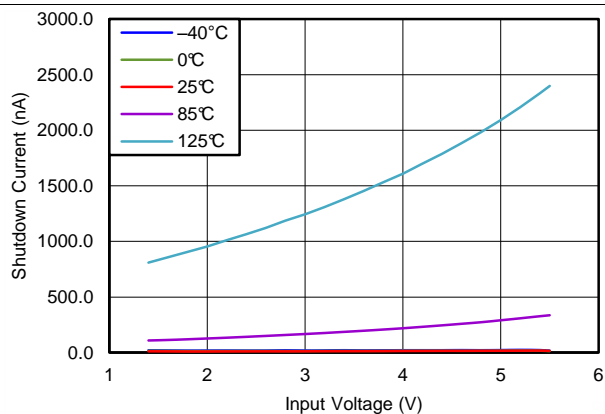
**Figure 2. Line Regulation**  
%V<sub>OUT</sub> Deviation vs V<sub>IN</sub> (V<sub>OUT</sub> = 3.3 V)



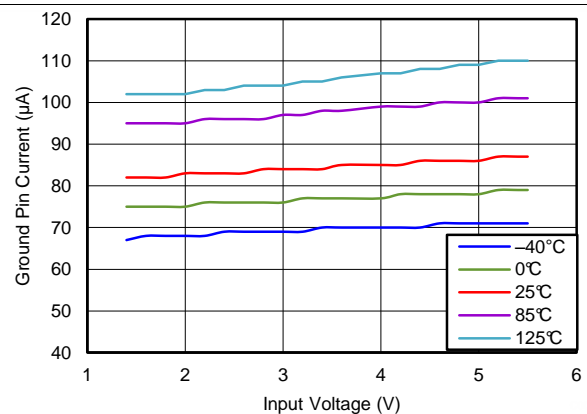
**Figure 3. Load Regulation**  
V<sub>OUT</sub> vs I<sub>OUT</sub> (V<sub>OUT</sub> = 1 V)



**Figure 4. Load Regulation**  
V<sub>OUT</sub> vs I<sub>OUT</sub> (V<sub>OUT</sub> = 3.3 V)



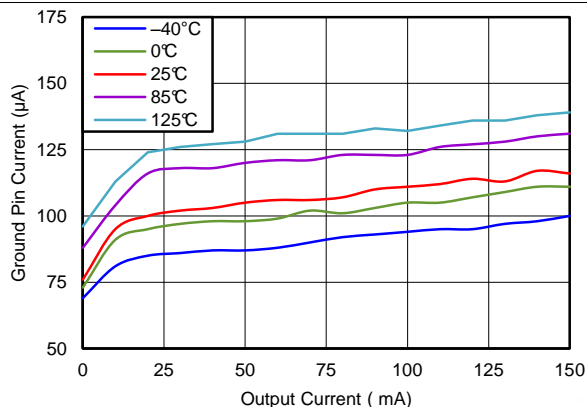
**Figure 5. Shutdown Current vs V<sub>IN</sub>**



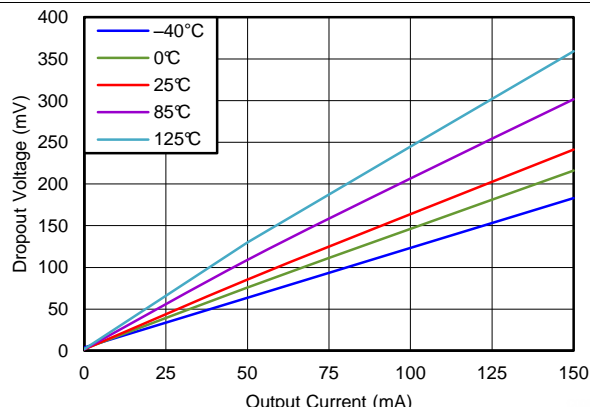
**Figure 6. Ground Pin Current vs V<sub>IN</sub>**

**Typical Characteristics (continued)**

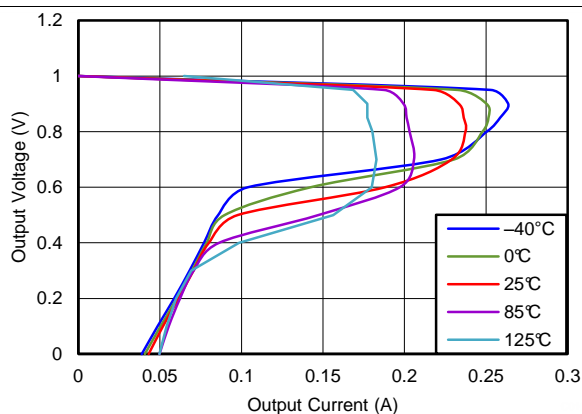
Over operating temperature range of  $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $V_{IN} = V_{OUT(TYP)} + 0.5\text{ V}$  or  $2\text{ V}$  (whichever is greater),  $V_{EN1} = V_{EN2} = V_{IN}$ ,  $I_{OUT1} = I_{OUT2} = 10\text{ mA}$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{OUT1} = 1\text{ }\mu\text{F}$ , and  $C_{OUT2} = 1\text{ }\mu\text{F}$ , unless otherwise noted. Output current plots show typical performance with a single output current sweep. Typical values are at  $T_J = 25^{\circ}\text{C}$ .



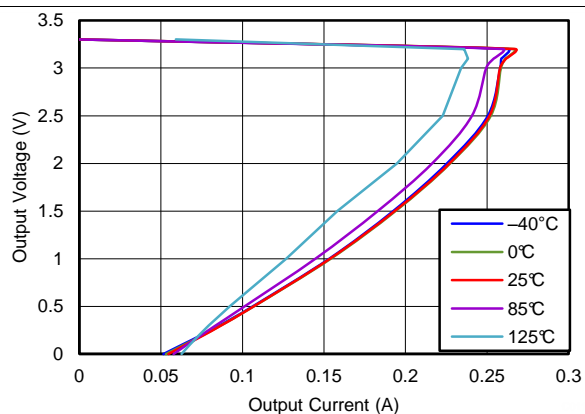
**Figure 7. Ground Pin Current vs  $I_{OUT}$**



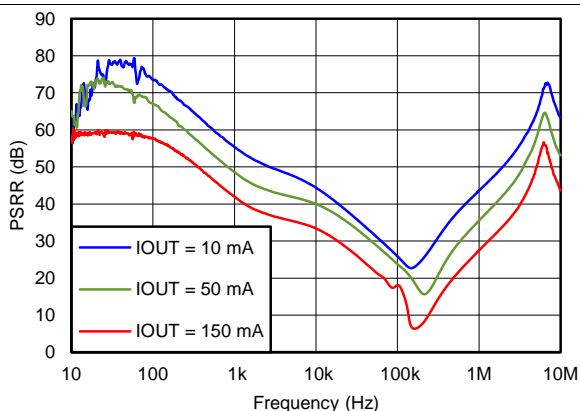
**Figure 8. Dropout Voltage vs  $I_{OUT}$   
( $V_{OUT} = 3.3\text{ V}$ )**



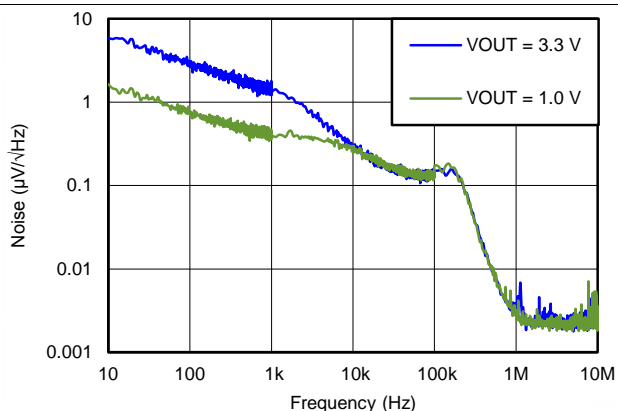
**Figure 9. Output Voltage vs Output Current ( $V_{OUT} = 1\text{ V}$ )  
(Foldback Current Limit)**



**Figure 10. Output Voltage vs Output Current ( $V_{OUT} = 3.3\text{ V}$ )  
(Foldback Current Limit)**



**Figure 11. Power-Supply Rejection Ratio vs Frequency  
( $V_{OUT} = 3.3\text{ V}$ )**



**Figure 12. Output Spectral Noise Density**

### Typical Characteristics (continued)

Over operating temperature range of  $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $V_{IN} = V_{OUT(TYP)} + 0.5\text{ V}$  or  $2\text{ V}$  (whichever is greater),  $V_{EN1} = V_{EN2} = V_{IN}$ ,  $I_{OUT1} = I_{OUT2} = 10\text{ mA}$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{OUT1} = 1\text{ }\mu\text{F}$ , and  $C_{OUT2} = 1\text{ }\mu\text{F}$ , unless otherwise noted. Output current plots show typical performance with a single output current sweep. Typical values are at  $T_J = 25^{\circ}\text{C}$ .

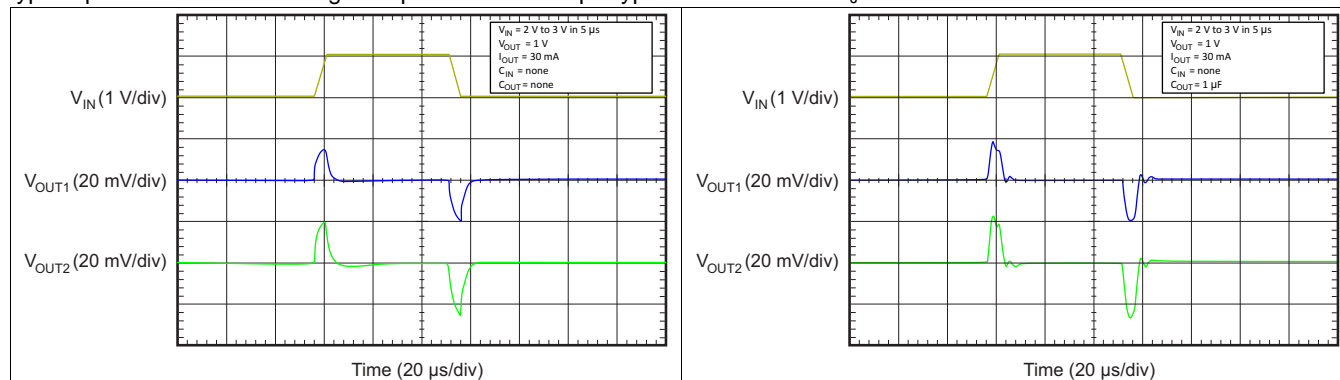


Figure 13. Line Transient

Figure 14. Line Transient

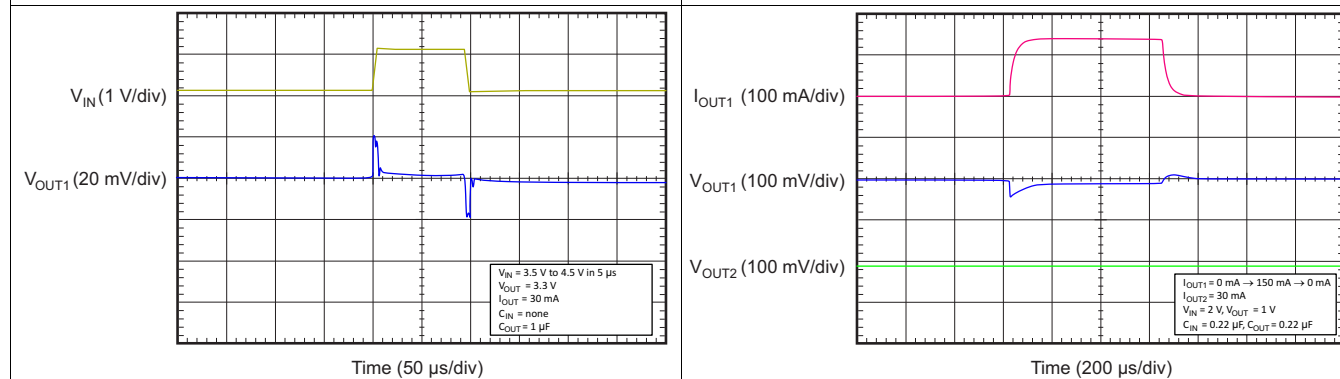


Figure 15. Line Transient

Figure 16. Load Transient

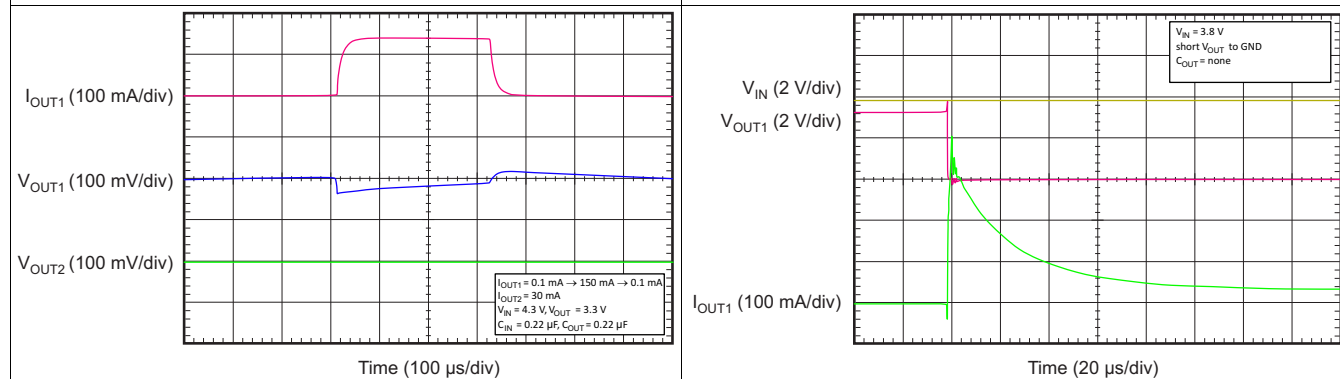


Figure 17. Load Transient

Figure 18. Foldback Current Limit



Typical Characteristics (continued)

Over operating temperature range of  $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $V_{IN} = V_{OUT(TYP)} + 0.5\text{ V}$  or  $2\text{ V}$  (whichever is greater),  $V_{EN1} = V_{EN2} = V_{IN}$ ,  $I_{OUT1} = I_{OUT2} = 10\text{ mA}$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{OUT1} = 1\text{ }\mu\text{F}$ , and  $C_{OUT2} = 1\text{ }\mu\text{F}$ , unless otherwise noted. Output current plots show typical performance with a single output current sweep. Typical values are at  $T_J = 25^{\circ}\text{C}$ .

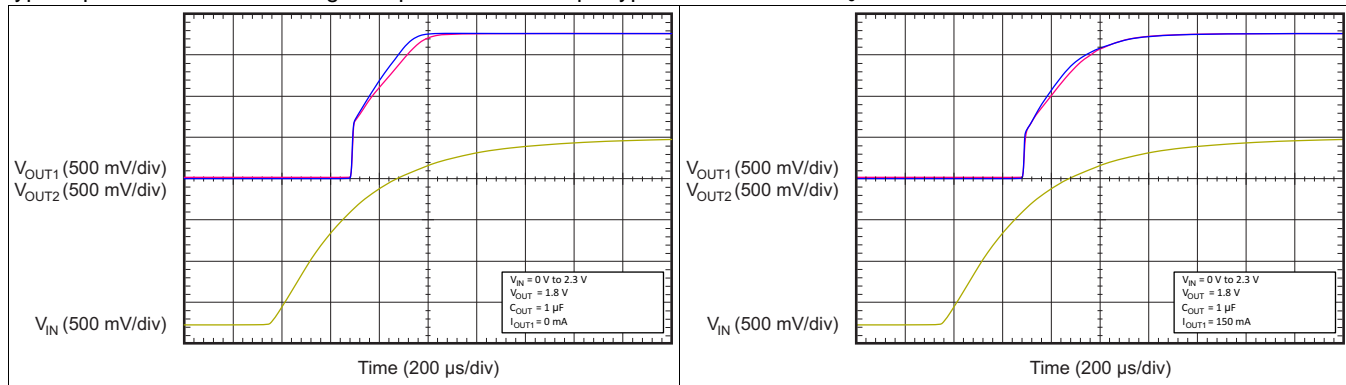


Figure 19. Start-Up

Figure 20. Start-Up

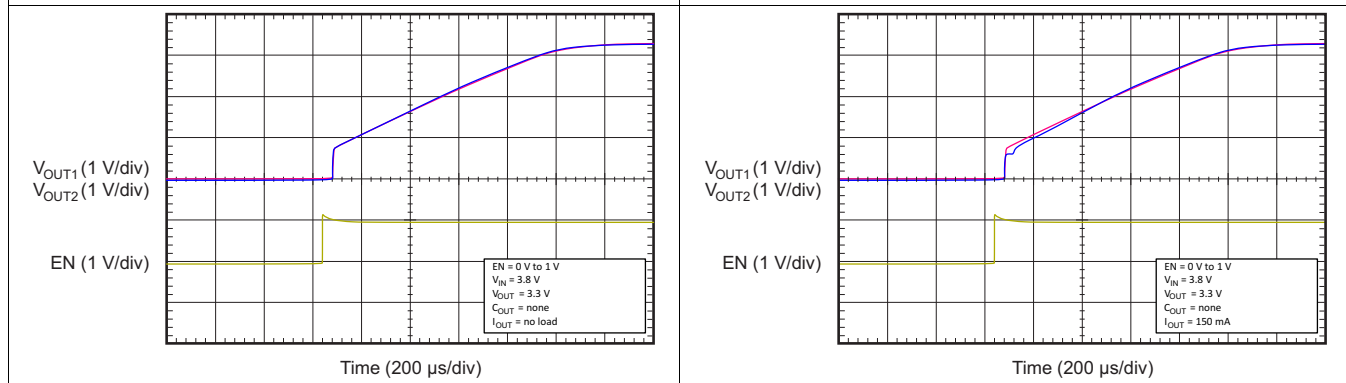


Figure 21. Start-Up With EN

Figure 22. Start-Up With EN

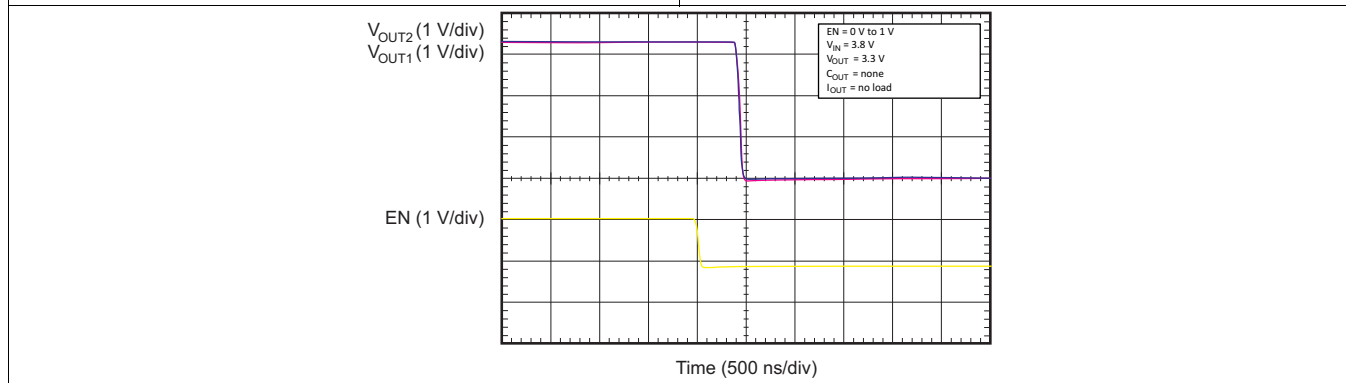


Figure 23. Shutdown With EN

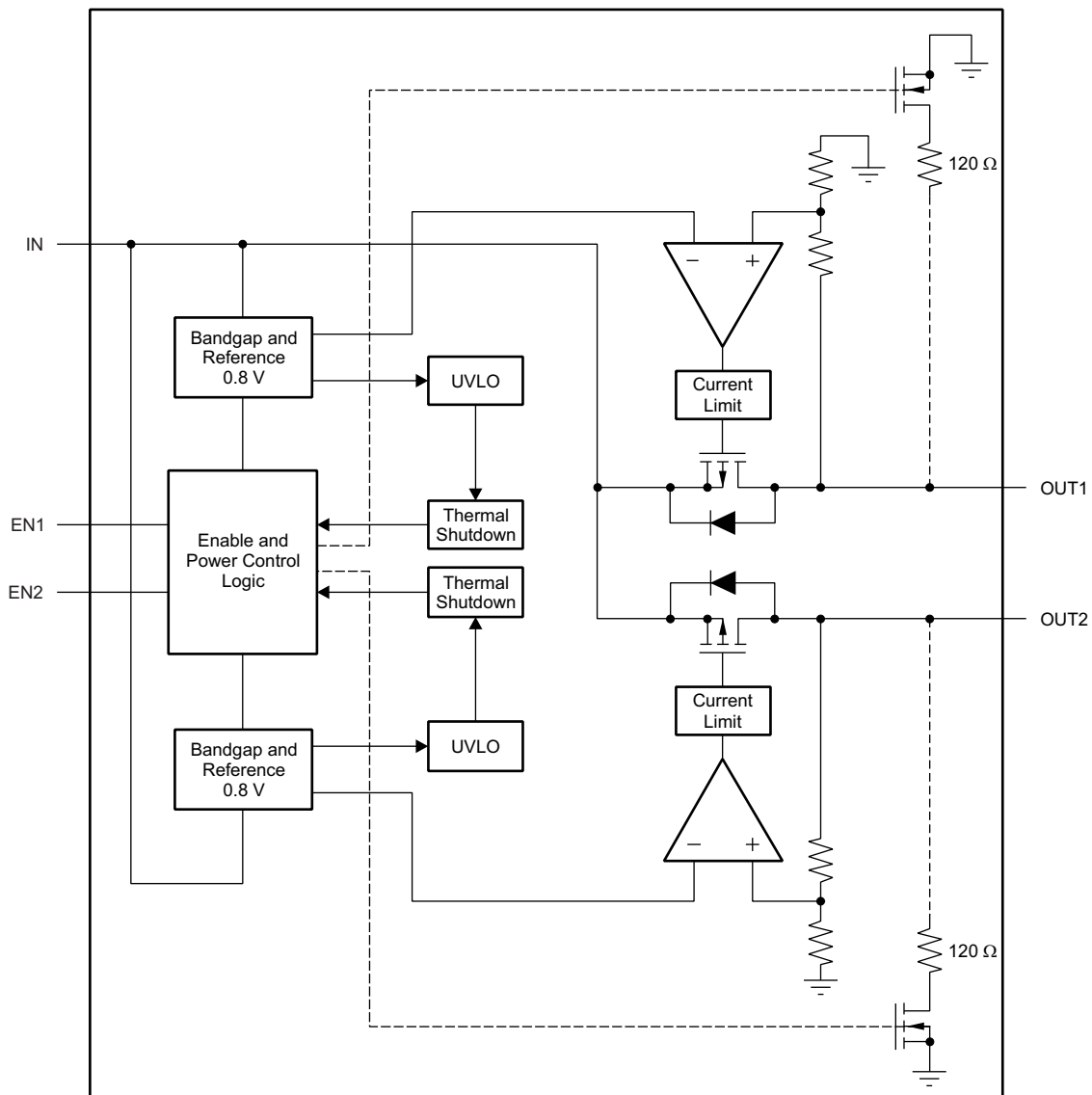
## 7 Detailed Description

### 7.1 Overview

The TLV716 and TLV716P devices belong to a new family of next-generation of dual-value, low-dropout (LDO) regulators. These devices consume low quiescent current and deliver excellent line and load transient performance. These characteristics, combined with low noise, very good PSRR with little ( $V_{IN} - V_{OUT}$ ) headroom, make this family of devices ideal for RF portable applications.

This family of regulators offers current limit and thermal protection. Device operating junction temperature is  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

### 7.2 Functional Block Diagram



NOTE: Dashed lines are for the TLV716P only.

## 7.3 Feature Description

### 7.3.1 Internal Current Limit

The TLV716 and TLV716P have an internal foldback current limit that helps protect the regulator during fault conditions. The current supplied by the device gradually reduces while the output voltage decreases. When the output is connected to ground, the LDO supplies a typical current of 40 mA. When in current limit, the output voltage is not regulated and  $V_{OUT} = I_{OUT} \times R_{LOAD}$ ; see [Figure 10](#) and [Figure 11](#). The PMOS pass transistor dissipates  $[(V_{IN} - V_{OUT}) \times I_{LIMIT}]$  until thermal shutdown is triggered and the device turns off. When the device cools down, the internal thermal shutdown circuit turns on the device. If the fault condition continues, the device cycles between current limit and thermal shutdown. See the [Thermal Considerations](#) section for more details.

The TLV716 PMOS pass element has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of the rated output current is recommended. A small schottky diode connected with the anode to OUT and the cathode to IN can accomplish this limiting.

### 7.3.2 Shutdown

The enable pin (EN) is active high. The device is enabled when the EN pin goes above 0.9 V. This relatively low value of voltage required to turn the LDO regulator on can be used to enable the device with the general-purpose input/output (GPIO) of recent processors whose GPIO voltage is lower than traditional microcontrollers.

The device is turned off when the EN pin is held at less than 0.4 V. When shutdown capability is not required, the EN pin can be connected to the IN pin. The TLV716P will pull down the output with a 120-Ω resistor when the EN pin falls below 0.4 V.

### 7.3.3 Undervoltage Lockout (UVLO)

The TLV716 and TLV716P use an undervoltage lockout circuit (1.3 V, typical) to keep the output shut off until the internal circuitry is operating properly.

## 7.4 Device Functional Modes

### 7.4.1 Capacitor-Free Operation

The TLV716 and TLV716P are stable without the use of input or output capacitors. This functionality results in a reduction of component count, cost, and solution size. In addition, without the need of external capacitors, the ultra-small, 1.2-mm × 1.2-mm DPQ package optimizes the solution size for board space-constrained applications. To optimize device AC performance, an input and output capacitor is recommended, as described in the [Input and Output Capacitor Requirements](#) section.

## 8 Application and Implementation

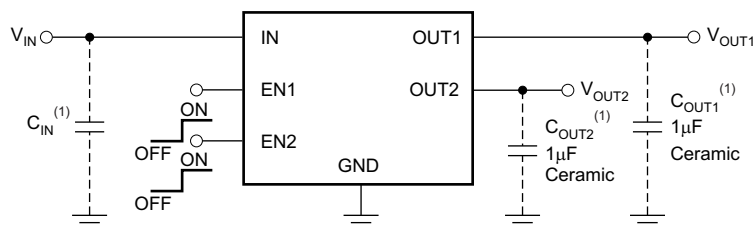
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The TLV716 and TLV716P belong to a family of dual-channel, capacitor-free, 150-mA, low-dropout voltage (LDO) regulators. These devices can be used with or without external capacitors and are available in a 1.2-mm x 1.2-mm package, making these devices a very small solution size for dual-channel, low-dropout (LDO) regulators. This family of LDO regulators offers current limit and thermal protection, and is specified from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ . [Figure 24](#) shows an application circuit for this family of devices.

### 8.2 Typical Application



(1) Optional.

**Figure 24. Typical Application Circuit**

#### 8.2.1 Design Requirements

[Table 1](#) lists the design requirements.

**Table 1. Design Parameters**

PARAMETER	DESIGN REQUIREMENT
Input voltage	4.2 V to 3 V (Lithium Ion battery)
Output 1 voltage	2.8 V $\pm$ 1.5%
Output 1 DC current	50 mA
Output 2 voltage	1.8 V $\pm$ 1.5%
Output2 DC current	10 mA
Maximum ambient temperature	65°C

#### 8.2.2 Detailed Design Procedure

An input capacitor is not required for this design because of the low impedance connection directly to the battery. No output capacitor allows for the minimal possible inrush current during start-up, ensuring the 180-mA maximum input current limit is not exceeded. Verify that the maximum junction temperature is not exceeded by calculating the total power dissipation and the junction temperature rise. For this example the total worst case power dissipation is  $(4.2\text{ V} - 2.8\text{ V}) \times 0.05\text{ A} + (4.2\text{ V} - 1.8\text{ V}) \times 0.01 = 0.094\text{ W}$ . The rise in junction temperature is calculated by multiplying the power dissipation by thermal resistance  $R_{\theta\text{JA}}$ . For this example, assuming the board size is similar to the JEDEC High K standard, the rise in junction temperature is  $0.094\text{ W} \times 149.3\text{ }^{\circ}\text{C/W} = 14^{\circ}\text{C}$ . The junction temperature is calculated by adding the rise in junction temperature to the maximum ambient temperature; in this example the maximum junction temperature can be calculated to be  $65^{\circ}\text{C} + 14^{\circ}\text{C} = 79^{\circ}\text{C}$ . It is mandatory to keep the junction temperature below the maximum operating junction temperature. For additional thermal information see the [Thermal Considerations](#) and [Power Dissipation](#) sections.

### 8.2.2.1 Input and Output Capacitor Requirements

The TLV716 and TLV716P uses an advanced internal control loop to obtain stable operation both with or without the use of input or output capacitors. If an output capacitor is used the device can support values as high as 100- $\mu$ F. The dynamic performance of the device is improved with the use of an output capacitor. An output capacitance of 0.1  $\mu$ F or larger generally provides good dynamic response. X5R- and X7R-type ceramic capacitors are recommended because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature.

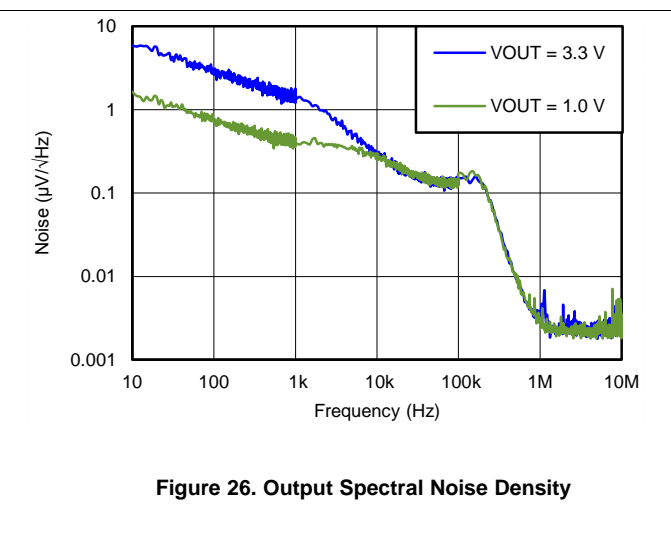
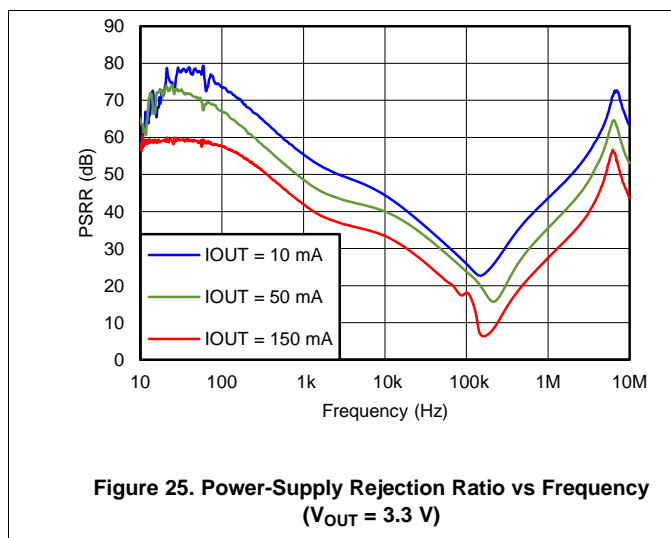
Although an input capacitor is not required for stability, good analog design practice is to connect a 0.1- $\mu$ F to 1- $\mu$ F capacitor from IN to GND. This capacitor counteracts input source impedance and improves supply transient response, input ripple, and PSRR. A higher value capacitor may be necessary if large, fast, rise-time load transients are anticipated or if the device is located several inches from the input power source.

### 8.2.2.2 Dropout Voltage

The TLV716 and TLV716P use a PMOS pass transistor to achieve low dropout. When  $(V_{IN} - V_{OUT})$  is less than the dropout voltage ( $V_{DO}$ ), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the  $R_{DS(ON)}$  of the PMOS pass element.  $V_{DO}$  scales approximately with the output current because the PMOS device behaves like a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded as  $(V_{IN} - V_{OUT})$  approaches dropout.

### 8.2.3 Application Curves



## 9 Power Supply Recommendations

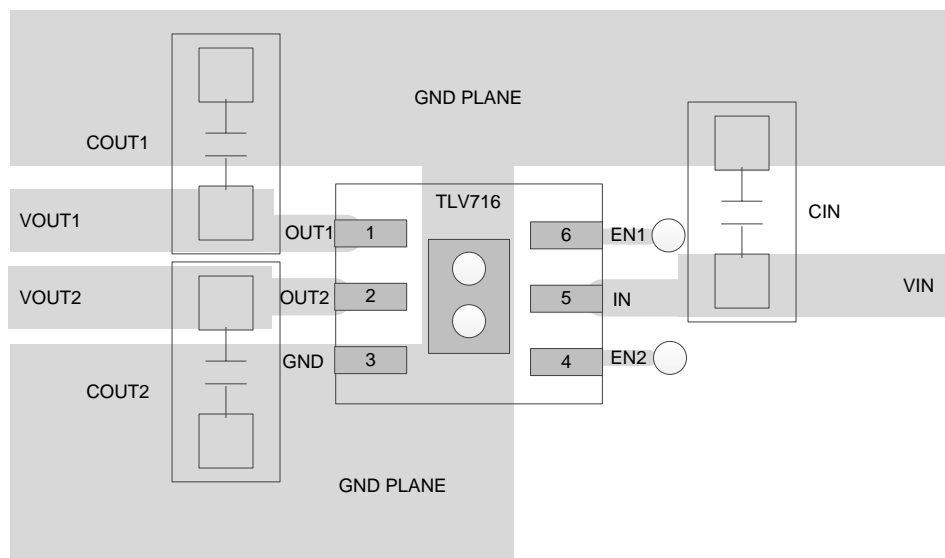
These devices are designed to operate from an input voltage supply range from 1.4 V to 5.5 V. The input voltage range must provide adequate headroom for the device to have a regulated output. This input supply must be well-regulated and stable. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

## 10 Layout

### 10.1 Layout Guidelines

If used, place the input and output capacitors as close to the device pins as possible. To maximize AC performance refer to [Figure 27](#).

### 10.2 Layout Example



**Figure 27. Layout Recommendation**

### 10.3 Thermal Considerations

Thermal protection disables the output when the junction temperature rises to approximately 158°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to 125°C maximum. To estimate the margin of safety in a complete design, increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. The ambient temperature at which thermal shutdown occurs on the device is 33°C higher (158°C - 125°C) than the maximum recommended operating conditions.

The internal protection circuitry of the TLV716 and TLV716P is designed to protect against overload conditions. This circuitry is not intended to replace proper PCB layout and heatsinking. Continuously running the device into thermal shutdown degrades reliability.

### 10.4 Power Dissipation

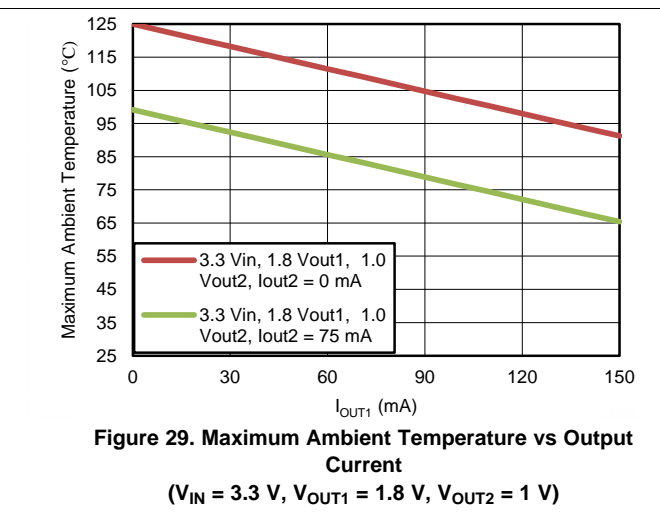
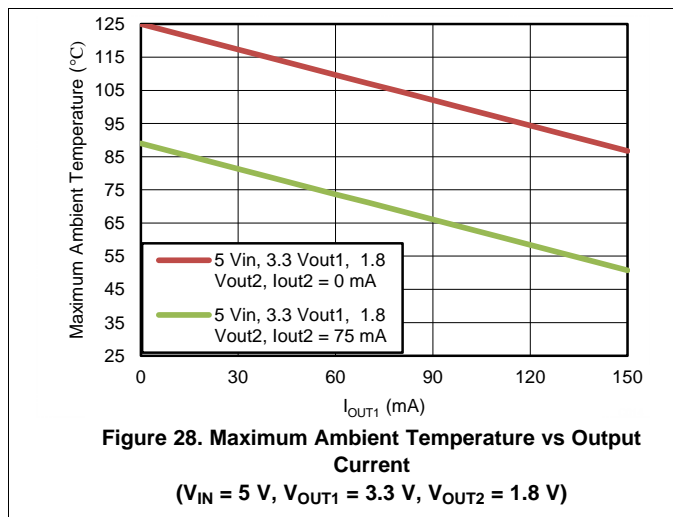
The ability to remove heat from a die is different for each package type, presenting different considerations in the printed-circuit-board (PCB) layout. The copper PCB area around the device that is free of other components moves the heat from the device to ambient air. Performance data for JEDEC high-K boards are given in the [Thermal Information](#) table. Using heavier copper increases effectiveness in removing heat from the device.

Power dissipation ( $P_D$ ) is equal to the product of the output current and the voltage drop across both output pass elements, as shown in [Equation 1](#):

$$P_D = (V_{IN} - V_{OUT1}) \times I_{OUT1} + (V_{IN} - V_{OUT2}) \times I_{OUT2} \quad (1)$$

### Power Dissipation (continued)

The maximum ambient temperature that the device can operate within the maximum  $T_J$  operating temperature of 125°C depends on the thermal impedance and the total power dissipated within the device. Figure 28 and Figure 29 show maximum ambient temperature versus output current for two different LDO configurations. Figure 28 shows the maximum ambient temperature with  $V_{IN} = 3.3\text{ V}$ ,  $V_{OUT1} = 1.8\text{ V}$ , and  $V_{OUT2} = 1\text{ V}$  versus  $I_{OUT1}$ . Figure 29 shows the maximum ambient temperature with  $V_{IN} = 5\text{ V}$ ,  $V_{OUT1} = 3.3\text{ V}$ , and  $V_{OUT2} = 1.8\text{ V}$  versus  $I_{OUT1}$ .



## 11 Device and Documentation Support

### 11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 2. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TLV716	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TLV716P	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.3 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.5 Glossary

**SLYZ022** — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TLV716120275PDPQR</a>	Active	Production	X2SON (DPQ)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	EI
TLV716120275PDPQR.B	Active	Production	X2SON (DPQ)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	EI
<a href="#">TLV716120275PDPQT</a>	Active	Production	X2SON (DPQ)   6	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	EI
TLV716120275PDPQT.B	Active	Production	X2SON (DPQ)   6	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	EI
<a href="#">TLV7162818PDPQR</a>	Active	Production	X2SON (DPQ)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CW
TLV7162818PDPQR.B	Active	Production	X2SON (DPQ)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CW
<a href="#">TLV7162818PDPQT</a>	Active	Production	X2SON (DPQ)   6	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CW
TLV7162818PDPQT.B	Active	Production	X2SON (DPQ)   6	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CW
<a href="#">TLV7162828PDPQR</a>	Active	Production	X2SON (DPQ)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CX
TLV7162828PDPQR.B	Active	Production	X2SON (DPQ)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CX
<a href="#">TLV7162828PDPQT</a>	Active	Production	X2SON (DPQ)   6	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CX
TLV7162828PDPQT.B	Active	Production	X2SON (DPQ)   6	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CX
<a href="#">TLV7163030PDPQR</a>	Active	Production	X2SON (DPQ)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CY
TLV7163030PDPQR.B	Active	Production	X2SON (DPQ)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CY
<a href="#">TLV7163030PDPQT</a>	Active	Production	X2SON (DPQ)   6	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CY
TLV7163030PDPQT.B	Active	Production	X2SON (DPQ)   6	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CY
<a href="#">TLV7163318PDPQR</a>	Active	Production	X2SON (DPQ)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CZ
TLV7163318PDPQR.B	Active	Production	X2SON (DPQ)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CZ
<a href="#">TLV7163318PDPQT</a>	Active	Production	X2SON (DPQ)   6	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CZ
TLV7163318PDPQT.B	Active	Production	X2SON (DPQ)   6	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CZ
V716120275PDPQRG4	Active	Production	X2SON (DPQ)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	EI
V716120275PDPQRG4.B	Active	Production	X2SON (DPQ)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	EI

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV7162818PDPQR	X2SON	DPQ	6	3000	180.0	9.5	1.33	1.33	0.47	4.0	8.0	Q2
TLV7162818PDPQT	X2SON	DPQ	6	250	180.0	9.5	1.33	1.33	0.47	4.0	8.0	Q2
TLV7162828PDPQR	X2SON	DPQ	6	3000	180.0	9.5	1.33	1.33	0.47	4.0	8.0	Q2
TLV7162828PDPQT	X2SON	DPQ	6	250	180.0	9.5	1.33	1.33	0.47	4.0	8.0	Q2
TLV7163030PDPQR	X2SON	DPQ	6	3000	180.0	9.5	1.33	1.33	0.47	4.0	8.0	Q2
TLV7163030PDPQT	X2SON	DPQ	6	250	180.0	9.5	1.33	1.33	0.47	4.0	8.0	Q2
TLV7163318PDPQR	X2SON	DPQ	6	3000	180.0	9.5	1.33	1.33	0.47	4.0	8.0	Q2
TLV7163318PDPQT	X2SON	DPQ	6	250	180.0	9.5	1.33	1.33	0.47	4.0	8.0	Q2

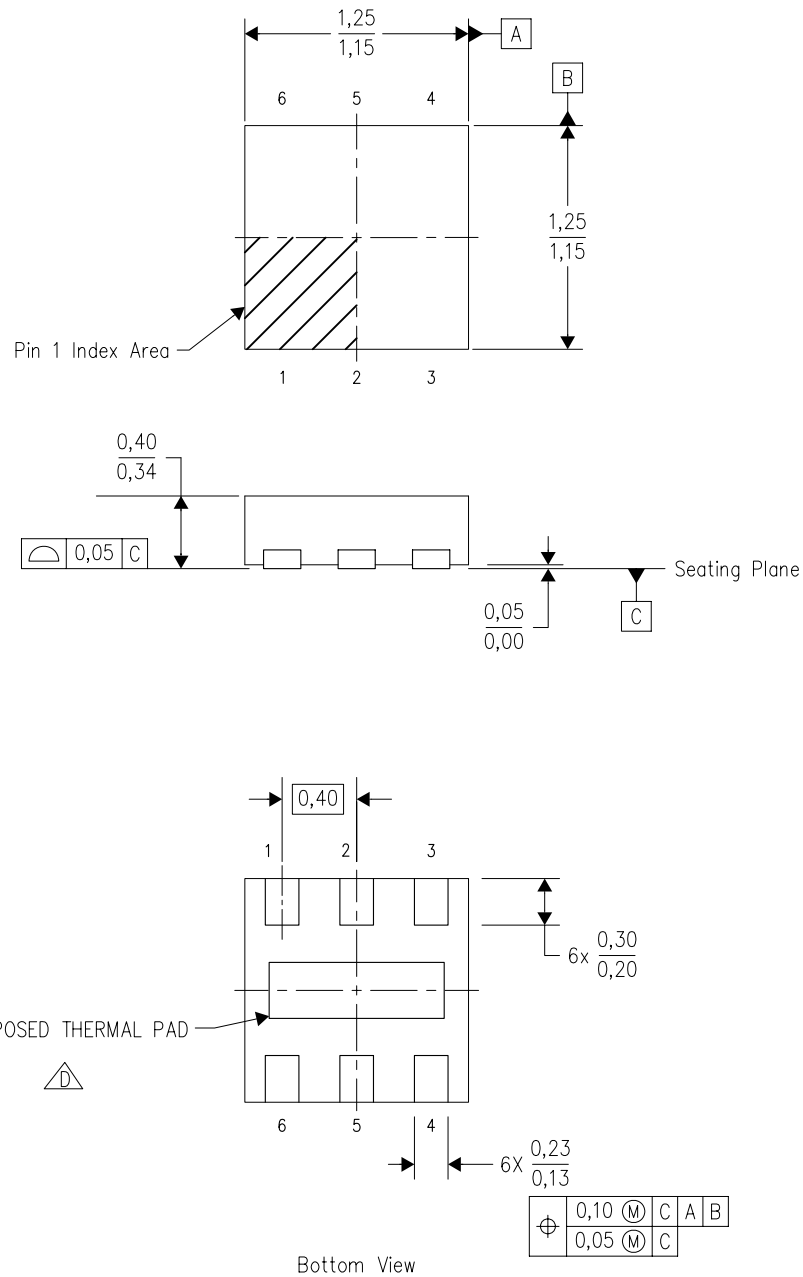
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal


Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV7162818PDPQR	X2SON	DPQ	6	3000	184.0	184.0	19.0
TLV7162818PDPQT	X2SON	DPQ	6	250	184.0	184.0	19.0
TLV7162828PDPQR	X2SON	DPQ	6	3000	184.0	184.0	19.0
TLV7162828PDPQT	X2SON	DPQ	6	250	184.0	184.0	19.0
TLV7163030PDPQR	X2SON	DPQ	6	3000	184.0	184.0	19.0
TLV7163030PDPQT	X2SON	DPQ	6	250	184.0	184.0	19.0
TLV7163318PDPQR	X2SON	DPQ	6	3000	184.0	184.0	19.0
TLV7163318PDPQT	X2SON	DPQ	6	250	184.0	184.0	19.0

DPQ (S-PX2SON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



4211511/A 12/10

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. SON (Small Outline No-Lead) package configuration.
  -  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

# THERMAL PAD MECHANICAL DATA

DPQ (S-PX2SON-N6)

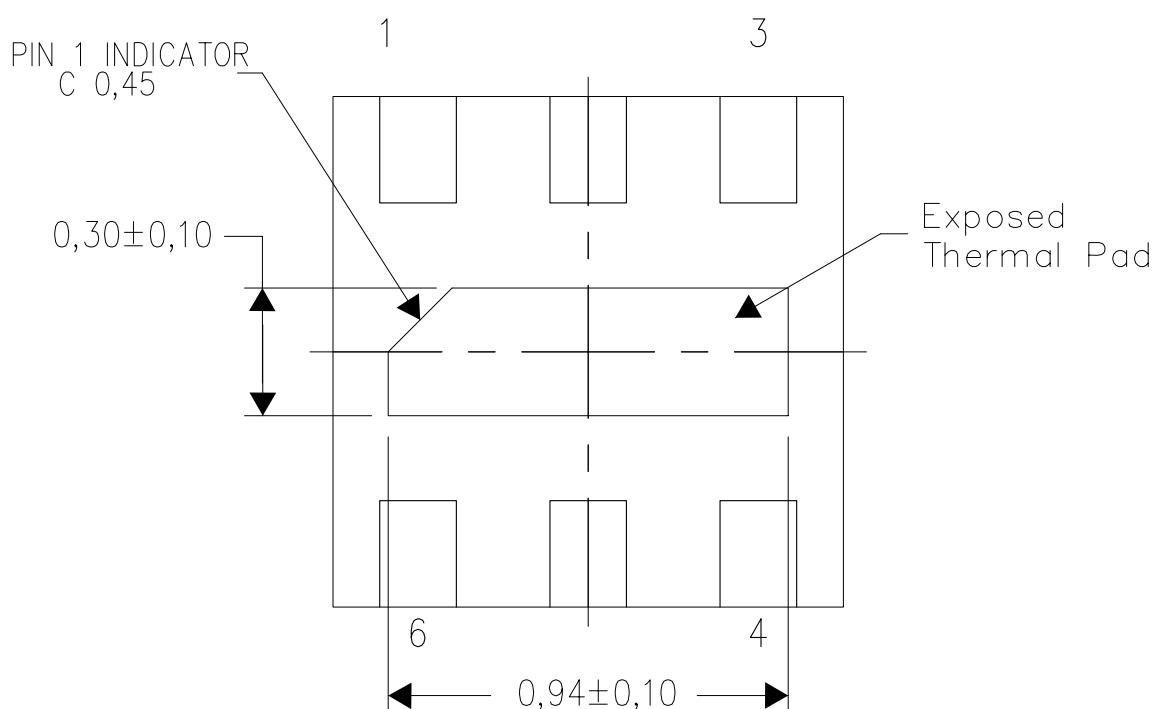
PLASTIC SMALL OUTLINE NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.

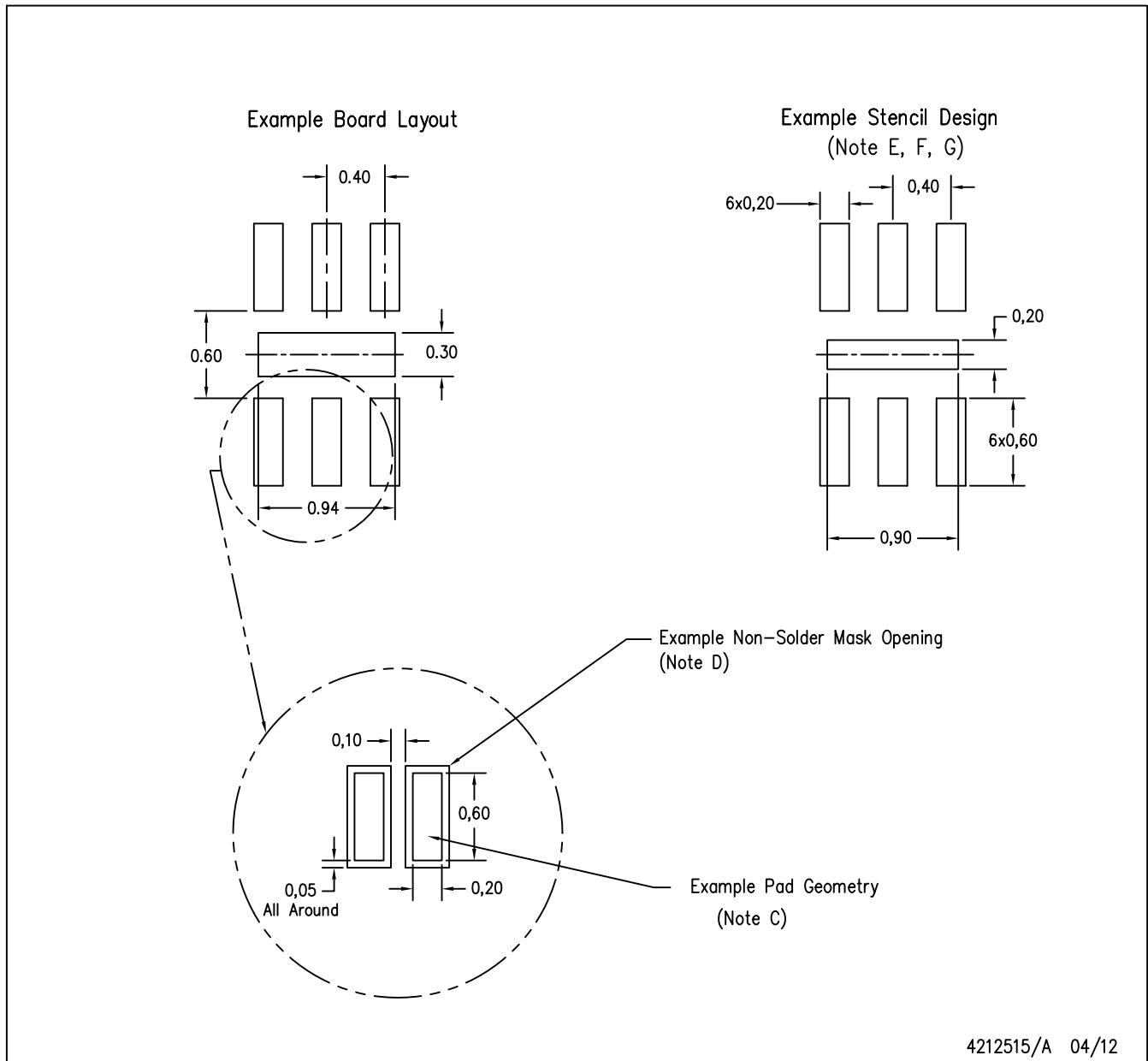


Bottom View

Exposed Thermal Pad Dimensions

4211579/B 02/12

NOTES: All linear dimensions are in millimeters



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
  - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
  - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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