**TEXAS INSTRUMENTS**
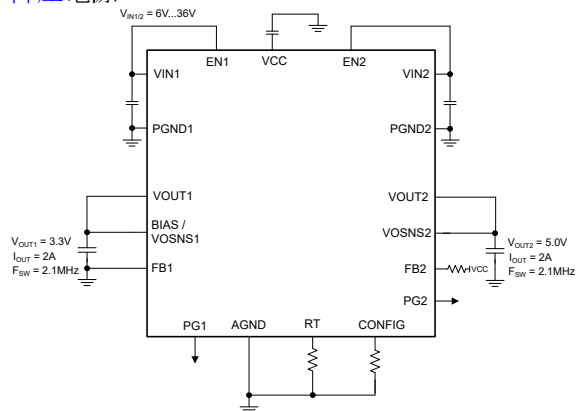
# TLVM1440x 高密度、36V、0.8V～9V 出力、デュアル 2/3A またはシングル 4/6A 出力のパワー モジュール

## 1 特長

- 多用途のデュアル出力電圧または単一出力同期整流降圧モジュール
  - MOSFET、インダクタ、コントローラを内蔵
  - 広い入力電圧範囲：3V～36V
  - 出力電圧を 0.8V～9V の範囲で調整可能
  - 6.5mm × 7.0mm × 2mm のオーバーモールド パッケージ
  - 接合部温度範囲：-40℃～125℃
- 全負荷範囲にわたって極めて高い効率を実現
  - 93.5% のピーク効率
  - 外部バイアス オプションによる効率向上
  - 露出パッドによる熱インピーダンスの低減 EVM $\theta_{JA}$ = 20°C/W。
  - シャットダウン時静止電流：0.6μA (標準値)
- 非常に小さい 伝導および放射 EMI
  - デュアル入力パスと内蔵コンデンサを備えた低ノイズ パッケージにより、スイッチのリンギングが減少
  - CISPR 11 および 32 Class B の放射規格に準拠
- 堅牢な設計用の本質的な保護機能
  - 高精度のイネーブル入力とオープン ドレインの PGOOD インジケータによるシーケンシング、制御、$V_{IN}$ UVLO
  - 過電流およびサーマル シャットダウン保護機能
- WEBENCH® Power Designer により、TLVM1440x を使用するカスタム設計を作成

## 2 アプリケーション

- 試験および測定、航空宇宙および防衛
- ファクトリ オートメーション / 制御
- 降圧電源

## 3 概要

TLVM1440x は、パワー MOSFET、シールド付きインダクタ、受動部品を拡張 HotRod™ QFN パッケージに実装した、高集積 36V 入力対応 DC/DC 設計です。このデバイスは、デュアル出力または大電流の単一出力をサポートし、インターリーブされたスタック可能な電流モード制御アーキテクチャを使用しているので、ループ補償が簡単であり、過渡応答が高速で、優れた負荷およびライン レギュレーションが可能です。このモジュールは、VIN および VOUT ピンをパッケージの角に配置し、入力および出力コンデンサの配置を最適化しています。モジュールの下面には大きなサーマル パッドがあるため、単純なレイアウトが可能で、製造時の扱いも容易です。

出力電圧範囲が 1V～9V の TLVM1440x は、小さな PCB フットプリントで低 EMI の設計を迅速かつ容易に実装できるよう設計されています。このトータル設計を使用すると、外付け部品はわずか 6 個で済み、設計プロセスでの磁気部品の選択も不要です。

TLVM1440x モジュールはスペースに制約のあるアプリケーション向けに小型でシンプルな設計となっていますが、可変入力電圧 UVLO 用のヒステリシス付き高精度イネーブルなど、堅牢な性能を実現するための多くの機能を備えているほか、VCC、ブートストラップ、入力コンデンサを内蔵し、信頼性および密度を高めています。このモジュールは、重負荷時には固定スイッチング周波数 (FPWM) を使用しますが、軽負荷時には効率向上のため可変周波数 (PFM) に自動的に遷移します。シーケンシング、フォルト保護、出力電圧監視用の PGOOD インジケータも内蔵しています。

### 製品情報

| 部品番号 [3] | パッケージ [1] | パッケージ サイズ [2] |
|---|---|---|
| TLVM14404 TLVM14406 | RCH (QFN-FCMOD、28) | 6.50mm × 7.0mm |

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。
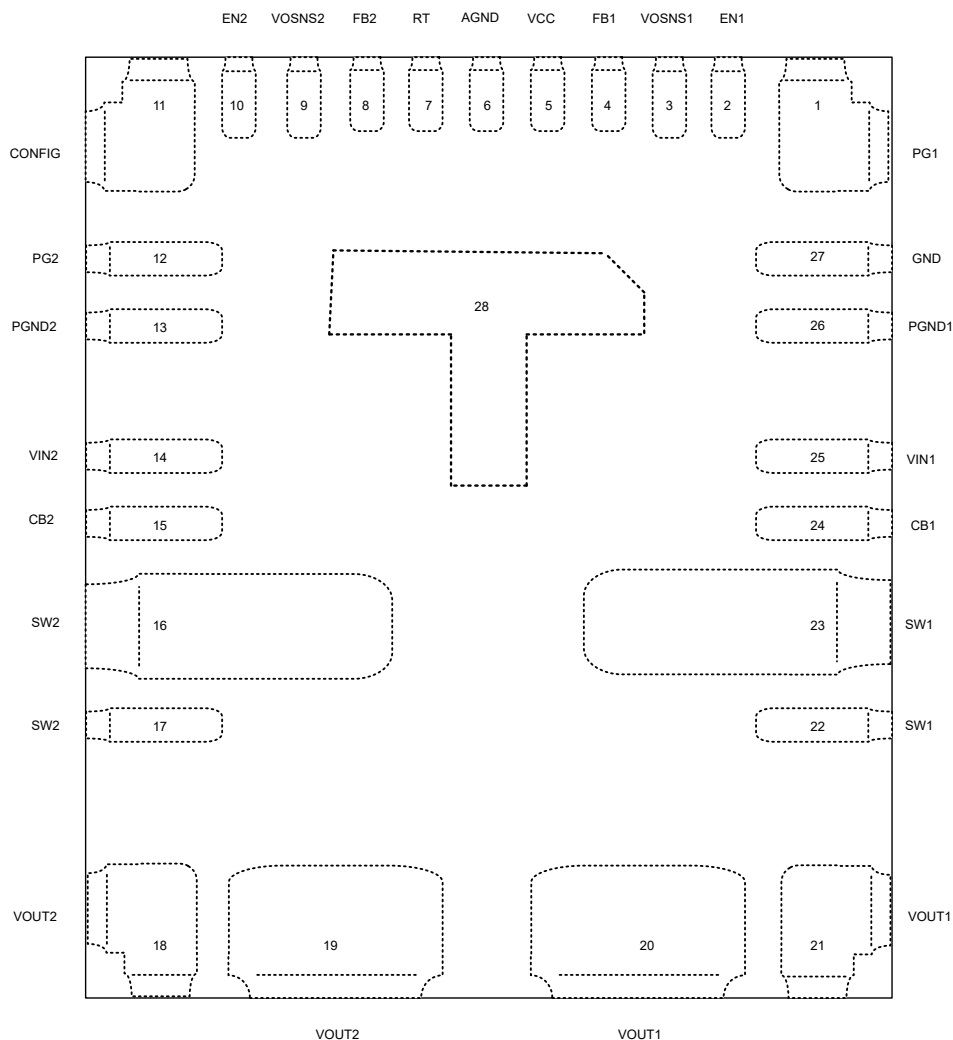(3) 「製品比較」表を参照してください。



**代表的な回路図**

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Product Folder Links: *TLVM14404 TLVM14406*

English Data Sheet: SLVSHP0

## 4 Device Comparison Table

| DEVICE | ORDERABLE PART NUMBER | RATED OUTPUT CURRENT | PACKAGE | JUNCTION TEMPERATURE RANGE |
|---|---|---|---|---|
| TLVM14404 | TLVM14404RCHR | Dual 2A / 2A or Single 4A | RCH (28) | –40°C to 125°C |
| TLVM14406 | TLVM14406RCHR | Dual 3A / 3A or Single 6A | RCH (28) | –40°C to 125°C |

Product Folder Links: *TLVM14404 TLVM14406*

English Data Sheet: SLVSHP0

## 5 Pin Configuration and Functions

RCH package, 28-pin QFN-FCMOD with Wettable Flanks



図 **5-1. Dual Output (Top View)**

EN2  COMP  SS  RT  AGND  VCC  FB1  VOSNS1  EN1

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |

CONFIG — 11 ... PG1 — 1

NC — 12

GND — 27

PGND2 — 13

28

PGND1 — 26

VIN2 — 14

VIN1 — 25

CB2 — 15

CB1 — 24

SW2 — 16

SW1 — 23

SW2 — 17

SW1 — 22

VOUT2 — 18

19    20

VOUT1 — 21

VOUT2       VOUT1

**図 5-2. Single Output Primary (Top View)**

資料に関するフィードバック(ご意見やお問い合わせ) を送信

Product Folder Links: *TLVM14404 TLVM14406*

English Data Sheet: SLVSHP0

表 5-1. Pin Functions

| PIN | | | TYPE[1] | DESCRIPTION |
|---|---|---|---|---|
| NO. | NAME | | | |
| | DUAL OUTPUT | SINGLE OUTPUT | | |
| 14 | VIN2 | VIN2 | I | Input supply to the regulator. Connect a high quality bypass capacitors from this pin to PGND. Low impedance connection must be provided to VIN1. |
| 15 | BOOT2 | BOOT2 | I/O | Channel 2 high-side driver upper supply rail. Connected to an internal 100nF capacitor between SW2 and BOOT2. An internal diode charges the capacitor while SW2 is low. Mechanical connection, use as NC in design. |
| 16, 17 | SW2 | SW2 | P | Channel 2 Switching node that is internally connected to the source of the high-side NMOS buck switch and the drain of the low-side NMOS synchronous rectifier. Mechanical connection, use as NC in design. |
| 22, 23 | SW1 | SW1 | P | Channel 1 Switching node that is internally connected to the source of the high-side NMOS buck switch and the drain of the low-side NMOS synchronous rectifier. Mechanical connection, use as NC in design. |
| 24 | BOOT1 | BOOT1 | I/O | Channel 1 High-side driver upper supply rail. Connected to an internal 100nF between SW1 and BOOT1. An internal diode charges the capacitor while SW1 is low. Mechanical connection, use as NC in design. |
| 25 | VIN1 | VIN1 | I | Input supply to the regulator. Connect a high quality bypass capacitors from this pin to PGND. Low impedance connection must be provided to VIN2. |
| 27 | GND | GND | G | Analog ground connection. Ground return for the internal logic. |
| 1 | PG1 | PG1 | O | Dual function pin. An open drain output that transitions low if VOSNS1 is outside a specified regulation window in dual output and single output primary configuration. |
| 2 | EN1 | EN1 | I | An active high input TLVM1440x ($V_{OH}$ > 1.375V) enables Output 1 in dual output operation. When in single output operation, an active high input enables all phases in the system. When disabled, the TLVM1440x is in shutdown mode. EN1 must never be floating. |
| 3 | BIAS & VOSNS1 | BIAS & VOSNS1 | I | Output voltage sense and input to internal voltage regulator. Connect to non-switching side of the inductor. Connect an optional high quality 0.1µF capacitor from this pin to AGND for best performance. |
| 4 | FB1 | FB1 | I | Feedback input to channel 1 of the TLVM1440x in dual output operation and feedback input to all channels in single output operation. Connect FB1 to VCC through a 10kΩ resistor for a 5V output or connect FB1 to AGND for a 3.3V output. A resistive divider from the non-switching side of the inductor to FB1 sets the output voltage level between 0.8V and 20V. The regulation threshold at FB1 is 0.8V. For lower output voltages use at least a 10kΩ for the top of the resistor divider. |
| 5 | VCC | VCC | O | Internal regulator output. Used as supply to internal control circuits. Do not connect to any external loads. Connect a high quality 1µF capacitor from this pin to AGND. |
| 6 | AGND | AGND | G | Analog ground connection. Ground return for the internal voltage reference and analog circuits. |
| 7 | RT | RT | I | Frequency programming pin. A resistor from RT to AGND sets the oscillator frequency between 100kHz and 2.2MHz. |
| 8 | FB2 | SS | I | Dual function pin. When in dual output operation, the pin functions as FB2, feedback input to channel 2 of the TLVM1440x. Connect FB2 to VCC through a 10kΩ resistor for a 5V output or connect FB2 to AGND for a 3.3V output. A resistive divider from the non-switching side of the inductor to FB2 sets the output voltage level between 0.8V and 20V. For lower output voltages use at least a 10kΩ for the top of the resistor divider. When in single output mode, the pin functions as SS. An external capacitor must be placed from SS to AGND for external soft start of the output. Connect the SS pins of primary and secondaries for fault communication between devices. |
| 9 | VOSNS2 | COMP | I | Dual function pin. In dual output operation, the pin functions as VOSNS2 for the fixed 3.3V and 5V and adjustable output conditions. In single output operation, the pin is the output of the internal error amplifier. |
| 10 | EN2 | EN2 | I | An active high input ($V_{OH}$ > 1.375V) enables Output 2 in dual output operation. When in single output mode, EN2 of all TLVM1440x must be connected together. An active high input enables all secondary phases in the system. When disabled, only one channel in the primary TLVM1440x is active while all remaining phases are in shutdown mode. EN2 must never be floating. |

### 表 5-1. Pin Functions (続き)

| PIN | | | TYPE[1] | DESCRIPTION |
|---|---|---|---|---|
| **NO.** | **NAME** | | | |
| | **DUAL OUTPUT** | **SINGLE OUTPUT** | | |
| 11 | CONFIG | CONFIG | I | Single or Dual output selection. Connect specific resistor values to the pin (refer to 表 7-1) to select number of phases, primary and secondary and dither options. |
| 12 | PG2 | NC | O | Dual function pin. In dual output operation, this pin behaves as PG2, an open drain output that transitions low if VOSNS2 is outside a specified regulation window. In single output mode, leave the pin floating. |
| 18, 19 | VOUT2 | VOUT | O | Output of module. Connect a high quality bypass capacitors from this pin to PGND. |
| 20, 21 | VOUT1 | VOUT | O | Output of module. Connect a high quality bypass capacitors from this pin to PGND. |
| 13. 26 | PGND | PGND | G | Power ground to internal low side MOSFET. Connect to system ground. Low impedance connection must be provided to PGND1, PGND3 and PGND4. Connect a high quality bypass capacitors from this pin to VIN2. |
| 28 | PGND | PGND | G | Power ground and heat sink connection. Solder directly to system ground plane. Low impedance connection must be provided to other PGND pins. |

(1)     I = input, O = output, P = power, G = ground

Product Folder Links: *TLVM14404 TLVM14406*

English Data Sheet: SLVSHP0

# 6 Specifications

## 6.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted) [1]

|  |  | MIN | MAX | UNIT |
|---|---|---|---|---|
| Pin voltage | VIN1, VIN2 (transient) | −0.3 | 42 | V |
| Pin voltage | SW1, SW2 (less than 10ns transient) | −6 | 42 | V |
| Pin voltage | SW1, SW2 (transient) | −0.3 | 42 | V |
| Pin voltage | BOOT1 - SW1, BOOT2 - SW2 | −0.3 | 5.5 | V |
| Pin voltage | EN1, EN2 | −0.3 | 42 | V |
| Pin voltage | PG1, PG2 | −0.3 | 20 | V |
| Pin voltage | FB1, FB2/SS, CONFIG | −0.3 | 5.5 | V |
| Pin voltage | BIAS/VOSNS1, COMP/VOSNS2 | −0.3 | 22 | V |
| Pin voltage | RT, VCC | −0.3 | 5.5 | V |
| Pin voltage | PGND1/2/3/4 voltage differential | −1 | 2 | V |
| Sink current | PG1, PG2 |  | 10 | mA |
| $T_J$ | Operating junction temperature | −40 | 150 | °C |
| $T_{stg}$ | Storage temperature | −55 | 150 | °C |

(1)     Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

## 6.2 ESD Ratings

|  |  |  | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 [1] | ±2000 | V |
|  |  | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 [2] | ±750 | |

(1)     JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2)     JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

|  |  |  | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{VOSNS1/2}$ | Output voltage range |  | 0.8 |  | 9 | V |
| $V_{IN1/2}$ | Input supply voltage range | VIN1, VIN2 | 3 |  | 36 | V |
|  | Pin voltage | SW1, SW2 | 0 |  | 36 | V |
|  | Pin voltage | BOOT1, BOOT2 | 0 |  | VIN + 3.3 | V |
|  | Pin voltage | BOOT1 – SW1, BOOT2 – SW2 | 0 |  | 3.3 | V |
|  | Pin voltage | VCC | 0 |  | 3.3 | V |
| $F_{SW}$ | Frequency | Switching frequency range | 300 |  | 2200 | kHz |
| $I_{OUT1/2}$ | Output current range |  | 0 |  | 3 | A |
| $T_A$ | Ambient temperature | Operating ambient temperature | −40 |  | 105 | °C |
| $T_J$ | Operating junction temperature |  | −40 |  | 125 | °C |

Product Folder Links: *TLVM14404 TLVM14406*

English Data Sheet: SLVSHP0

## 6.4 Thermal Information

| THERMAL METRIC[1] | | TLVM1440X | UNIT |
|---|---|---|---|
| | | RCH (QFN-FCMOD) | |
| | | 28 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance (TLVM14406 EVM) | 20 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 5.5 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

## 6.5 Electrical Characteristics

$T_J$ = –40°C to 125°C. Typical values are at $T_J$ = 25°C and $V_{IN}$ = 13.5V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY** | | | | | | |
| $I_{Q(VIN-ST5p0)}$ | VIN quiescent current, single output mode | Non-switching, $V_{EN}$ = 2V, $V_{BIAS}$ = $V_{VOSNS1}$ = 5V + 10%, $T_J$ = 125℃ | | 25 | 45 | µA |
| $I_{Q(VIN-ST3p3)}$ | VIN quiescent current, single output mode | Non-switching, $V_{EN}$ = 2V, $V_{BIAS}$ = $V_{VOSNS1}$ = 3.3V + 10%, $T_J$ = 125℃ | | 15 | 35 | µA |
| $I_{Q(VIN-DT3p3)}$ | VIN quiescent current, dual output mode, BIAS = 3.3V | Non-switching, $V_{EN}$ = 2V, $V_{BIAS}$ = $V_{VOSNS1}$ = 3.3 V + 10%, $V_{VOSNS2}$ = 5 V + 10%, $T_J$ = 125℃ | | 9 | 18 | µA |
| $I_{SD(VIN)}$ | VIN shutdown supply current | $V_{EN}$ = 0 V | | 1 | 8 | µA |
| **UVLO** | | | | | | |
| $VIN_{UVLO(R)}$ | VIN UVLO rising threshold | $V_{IN}$ rising | | 3.5 | 3.80 | V |
| $VIN_{UVLO(F)}$ | VIN UVLO falling threshold | $V_{IN}$ falling | | 2.55 | 3 | V |
| $VIN_{UVLO(H)}$ | VIN UVLO hysteresis | | 0.735 | 0.95 | 1.25 | V |
| **ENABLE** | | | | | | |
| $V_{EN(R)}$ | EN1/2 voltage rising threshold | EN1/2 rising, enable switching | 1.125 | 1.25 | 1.375 | V |
| $V_{EN(F)}$ | EN1/2 voltage falling threshold | EN1/2 falling, disable switching | 0.8 | 0.9 | 1.0 | V |
| $V_{EN(H)}$ | EN1/2 voltage hysteresis | | 0.25 | 0.325 | 0.55 | V |
| $V_{EN(W)}$ | EN1/2 voltage wake-up threshold | | 0.4 | | | V |
| $I_{EN}$ | EN1/2 pin sourcing current post EN rising threshold | $V_{EN1/2}$ = $V_{IN}$ = 13.5V | | 0.6 | 400 | nA |
| **INTERNAL LDO** | | | | | | |
| $V_{VCC}$ | Internal LDO output voltage | $V_{BIAS}$ ≥ 3.4V, $I_{VCC}$ ≤ 100mA | 2.7 | 3.1 | 3.7 | V |
| $I_{VCC}$ | Internal LDO short-circuit current limit | $V_{IN}$ = 13.5V | 100 | 377 | 880 | mA |
| $V_{VCC(UVLO-R)}$ | VCC UVLO rising threshold for start-up | | 3.3 | 3.5 | 3.75 | V |
| $V_{VCC(UVLO-F)}$ | VCC UVLO falling threshold for shutdown | | 2.3 | 2.5 | 2.7 | V |
| **REFERENCE VOLTAGE** | | | | | | |
| $V_{FB1/2}$ | Dual output feedback voltages in adjustable output configuration | | 788 | 800 | 812 | mV |
| $V_{FB1\_so}$ | Single Output mode FB voltage in adjustable output configuration | | 788 | 800 | 812 | mV |
| $I_{FB1/2(LKG)}$ | FB input leakage current in dual output configuration | $V_{FB1/2}$ = 0.8V | | 10 | 250 | nA |
| $I_{FB1\_so(LKG)}$ | FB input leakage current in single output configuration | $V_{FB}$ = 0.8V | | 2 | 250 | nA |
| $FB_{Sel-5v0}$ | Voltage threshold for fixed 5V setting | | VCC-0.5 | | | V |
| $FB_{Sel-3v0}$ | Resistor for fixed 3.3V setting | | | | 300 | Ω |
| $FB_{Sel-ext}$ | Minimum Thevenin Equivalent resistance of external FB divider option to select adjustable output voltage. | | 4 | | | kΩ |
| **ERROR AMPLIFIER** | | | | | | |
| $g_{m-S1}$ | EA transconductance - single output mode | $V_{FB1}$ = $V_{COMP}$ | 625 | 888 | 1300 | µS |
| **SWITCHING FREQUENCY** | | | | | | |

## 6.5 Electrical Characteristics (続き)

$T_J$ = –40°C to 125°C. Typical values are at $T_J$ = 25°C and $V_{IN}$ = 13.5V (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{SW1(FCCM)}$ | Switching frequency, FCCM operation | $R_{RT}$ = 7.15kΩ to AGND | 1.9 | 2.1 | 2.3 | MHz |
| $f_{SW2(FCCM)}$ | Switching frequency, FCCM operation | $R_{RT}$ = 39.2 kΩ to AGND | 360 | 400 | 450 | kHz |
| $f_{ADJ(FCCM)}$ | Adjustable switching frequency range | $R_{RT}$ resistor from 6.81kΩ to 158kΩ to AGND | 0.1 | | 2.2 | MHz |
| **STARTUP** | | | | | | |
| $t_{SS(R)}$ | Internal fixed soft-start time - dual output mode | From $V_{VOSNS1/2}$ = 0% (first SW pulse) to $V_{VOSNS1/2}$ = 90% | 2.7 | 4.5 | 7 | ms |
| $I_{SS(R)}$ | Soft-start charge current - single output mode | $V_{SS}$ = 0V | 15 | 20 | 25 | μA |
| $R_{SS(F)}$ | Soft-start discharge resistance - single output mode | | | 10 | 27 | Ω |
| $t_{EN}$ | EN1 (Single output mode) or EN1/EN2 (whichever first in dual output mode) HIGH to start of switching delay | | | 687 | 900 | μs |
| **POWER STAGE** | | | | | | |
| $R_{DSON(HS)}$ | High-side MOSFET on-resistance | $V_{BOOT-SW}$ = 3.3V, $I_{OUT}$ = 1A | | 37 | | mΩ |
| $R_{DSON(LS)}$ | Low-side MOSFET on-resistance | $V_{VCC}$ = 3.3 V, $I_{OUT}$ = 1A | | 23.9 | | mΩ |
| $t_{ON(min)}$ | Minimum ON pulse width | $V_{IN}$ = 20V, $I_{OUT}$ = 2A | | 40 | 62 | ns |
| $t_{ON(max)}$ | Maximum ON pulse width (dual output, single output primary) | $R_{RT}$ = 7.15kΩ | 5 | 8 | 12 | μs |
| $t_{ON(max)}$ | Maximum ON pulse width (Single output secondary) | $R_{RT}$ = 7.15kΩ | | 16 | 25 | μs |
| $t_{OFF(min)}$ | Minimum OFF pulse width | $V_{IN}$ = 4V | | 70 | 110 | ns |
| **OVERCURRENT PROTECTION** | | | | | | |
| $I_{HS(OC1)}$ | High-side peak current limit TLVM14404 | Peak current limit on HS FET when Duty Cycle approaches 0% | | 4.76 | | A |
| $I_{HS(OC2)}$ | High-side peak current limit TLVM14406 | Peak current limit on HS FET when Duty Cycle approaches 0% | | 5.5 | | A |
| $I_{LS(OC1)}$ | Low-side valley current limit TLVM14404 | Valley current limit on LS FET | | 3.2 | | A |
| $I_{LS(OC2)}$ | Low-side valley current limit TLVM14406 | Valley current limit on LS FET | | 3.7 | | A |
| $IL_{PEAK1(min-0)}$ | Minimum peak inductor current at minimum duty cycle TLVM14404 | $V_{VCC}$ = 3.3V, $t_{pulse}$ ≤ 100ns | | 0.71 | | A |
| $IL_{PEAK1(min-100)}$ | Minimum peak inductor current at maximum duty cycle TLVM14406 | $V_{VCC}$ = 3.3V, $t_{pulse}$ ≥ 1μs | | 0.19 | | A |
| $IL_{PEAK2(min-0)}$ | Minimum peak inductor current at minimum duty cycle TLVM14404 | $V_{VCC}$ = 3.3V, $t_{pulse}$ ≤ 100ns | | 0.81 | | A |
| $IL_{PEAK2(min-100)}$ | Minimum peak inductor current at maximum duty cycle TLVM14406 | $V_{VCC}$ = 3.3V, $t_{pulse}$ ≥ 1μs | | 0.22 | | A |
| $V_{Hiccup-FB}$ | Hiccup threshold on FB pin - dual output mode, adjustable output option | HS FET On-time > 165ns | 0.25 | 0.3 | 0.35 | V |
| $t_{Hiccup-1}$ | Wait time before entering Hiccup - single and dual output mode | | 126 | 128 | 130 | Curent Limit cycles |
| $t_{Hiccup-2}$ | Hiccup time before re-start | | 50 | 88 | | ms |
| **POWER GOOD** | | | | | | |
| $V_{PGTH-1}$ | Power-Good threshold (PG1/2) | PGOOD low, $V_{VOSNS1/2}$ rising | 93% | 95% | 97% | |
| $V_{PGTH-2}$ | Power-Good threshold (PG1/2) | PGOOD high, $V_{VOSNS1/2}$ falling | 92% | 94% | 96% | |
| $V_{PGTH-3}$ | Power-Good threshold (PG1/2) | PGOOD high, $V_{VOSNS1/2}$ rising | 105% | 107% | 110% | |
| $V_{PGTH-4}$ | Power-Good threshold (PG1/2) | PGOOD low, $V_{VOSNS1/2}$ falling | 104% | 106% | 109% | |
| $t_{PGOOD(R)}$ | PG1/2 delay from $V_{VOSNS1/2}$ valid to PGOOD high during start-up | $V_{VOSNS1/2}$ = 3.3V | 1.5 | 2.1 | 3 | ms |
| $t_{PGOOD(F)}$ | PG1/2 delay from $V_{VOSNS1/2}$ invalid to PGOOD low | $V_{VOSNS1/2}$ = 3.3V | 25 | 40 | 70 | μs |
| $I_{PG(LKG)}$ | PG1/2 pin leakage current when open drain output is high | $V_{PG}$ = 3.3V | | | 0.075 | μA |

## 6.5 Electrical Characteristics (続き)

$T_J$ = –40°C to 125°C. Typical values are at $T_J$ = 25°C and $V_{IN}$ = 13.5V (unless otherwise noted)

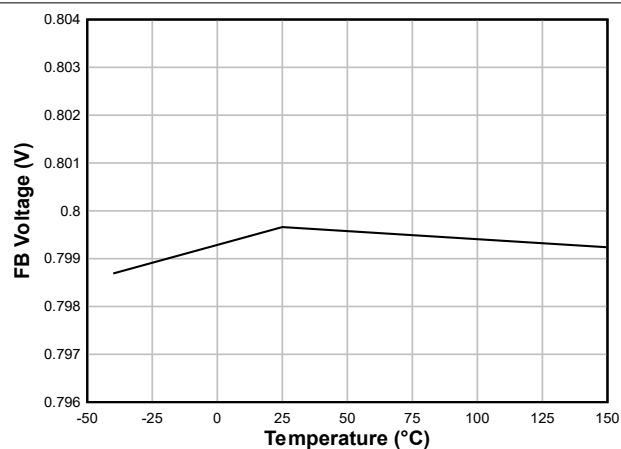| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{PG-D(LOW)}$ | PG pin output low-level voltage for both channels | $I_{PG}$ = 1mA, $V_{EN}$ = 0V. | | | 400 | mV |
| $R_{PG-1}$ | Pulldown MOSFET resistance | $I_{PG}$ = 1mA, $V_{EN}$ = 3.3V. | | 30 | 90 | Ω |
| $V_{IN(PG\_VALID)}$ | Minimum VIN for valid PG output | Pull up resistance on PG - $R_{PG}$ = 10kΩ, Voltage Pull up on PG - $V_{PULLUP\_PG}$ = 3V, $V_{PG-D\ (LOW)}$ = 0.4V | 0.45 | | 1.2 | V |
| THERMAL SHUTDOWN | | | | | | |
| $T_{J(SD)}$ | Thermal shutdown threshold [1] | Temperature rising | 160 | 170 | 180 | °C |
| $T_{J(HYS)}$ | Thermal shutdown hysteresis [1] | | | 10 | | °C |

(1)    Specified by design.

## 6.6 System Characteristics

The following specifications apply only to the typical applications circuit, with nominal component values. Specifications in the typical (TYP) column apply to $T_J$ = 25°C only. Specifications in the minimum (MIN) and maximum (MAX) columns apply to the case of typical components over the temperature range of $T_J$ = –40°C to 125°C. These specifications are not specified by production testing.
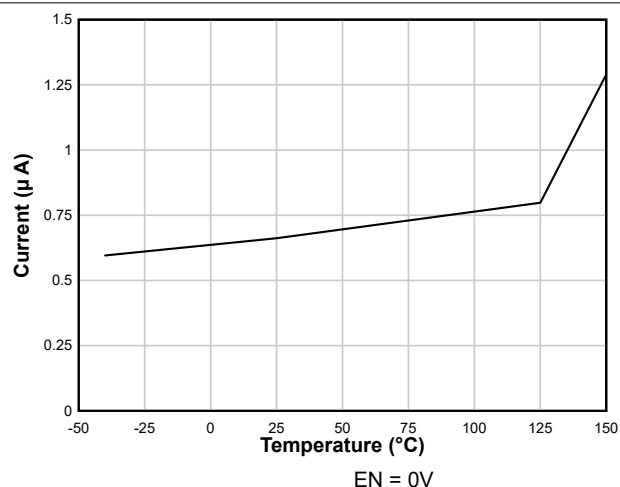
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| OUTPUT VOLTAGE | | | | | | |
| | Load and Line Regulation on VOUT1(3.3V) - single and dual output mode | $V_{BIAS/VOSNS1}$ = 3.3V, $V_{VOSNS2}$ = 5V (dual output mode), $V_{IN}$ = 3.8V to 36V, $I_{OUT}$ = 0A to full load, PFM Mode | | 60 | | mV |
| | Load and Line Regulation on VOUT1(5V) - single and dual output mode | $V_{BIAS/VOSNS1}$ = 5V, $V_{VOSNS2}$ = 3.3V (dual output mode), $V_{IN}$ = 6V to 36V, $I_{OUT}$ = 0A to full load, PFM Mode | | 70 | | mV |
| $D_{MAX(ffb)}$ | Maximum switch duty cycle | $V_{IN}$ = 3.3V, $V_{VOSNS1}$ = 3.3V, $I_{OUT}$ = 2A, frequency foldback | | 99% | | |
| $D_{MAX}$ | Maximum switch duty cycle | $V_{IN}$ = 6 V, $V_{VOSNS1}$ = 5 V, $I_{OUT}$ = 2 A, $f_{sw}$ = 1 MHz | | 88% | | |
| EFFICIENCY | | | | | | |
| | Efficiency on VOUT1(5V) - dual output mode | $V_{BIAS/VOSNS1}$ = 5V, $V_{VOSNS2}$ = 3.3V, $V_{IN}$ = 12V, $I_{OUT}$ = 3A, $f_{sw}$ = 1MHz | | 91.5% | | |
| | Efficiency on VOUT2(3.3V) - dual output mode | $V_{BIAS/VOSNS1}$ = 5V, $V_{VOSNS2}$ = 3.3V, $V_{IN}$ = 12V, $I_{OUT}$ = 3A, $f_{sw}$ = 1MHz | | 88% | | |
| | Efficiency - single output mode | $V_{BIAS/VOSNS1}$ = 5V, $V_{IN}$ = 12V, $I_{OUT}$ = 6A, $f_{sw}$ = 2.1MHz | | 91% | | |

## 6.7 Typical Characteristics

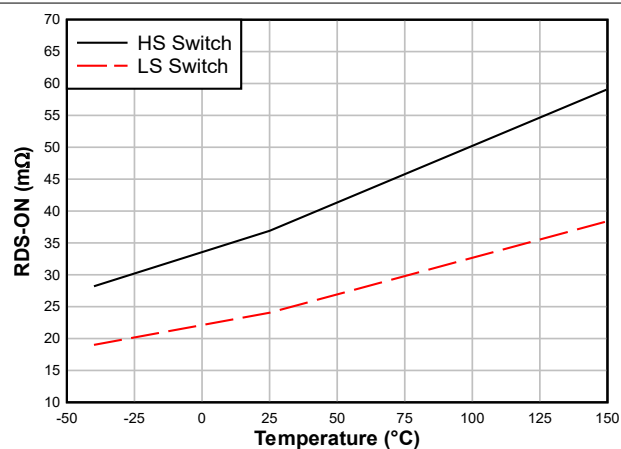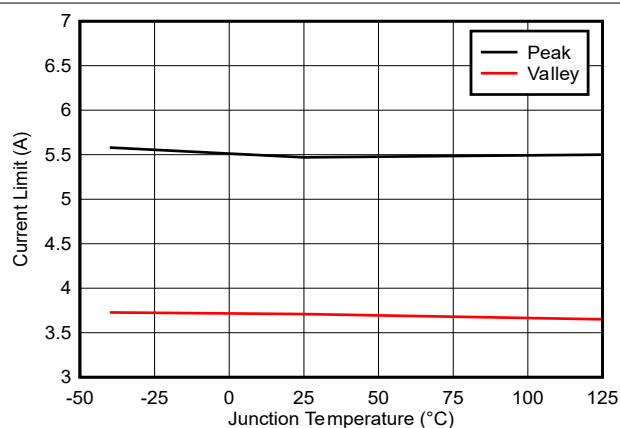Unless otherwise specified, $V_{IN}$ = 13.5V.



図 6-1. Feedback Voltage



EN = 0V

図 6-2. Shutdown Supply Current



図 6-3. High-side and Low-side Switches $R_{DS\_ON}$



図 6-4. High-side and Low-side Current Limits
TLVM14406

Product Folder Links: *TLVM14404 TLVM14406*

English Data Sheet: SLVSHP0

# 7 Detailed Description

## 7.1 Overview

The TLVM1440x is an easy-to-use, synchronous buck DC/DC power module designed for a wide variety of applications where reliability, small design size, and low EMI signature are of paramount importance. With integrated power MOSFETs, a buck inductor, and PWM controller, the TLVM1440x operates over an input voltage range of 3V to 36V with transients as high as 42V. The module delivers up to 3A per phase DC load current with high conversion efficiency and ultra-low input quiescent current in a very small footprint. Control loop compensation is not required for dual out configuration, reducing design time and external component count for multiple output voltages.

Due to a programmable switching frequency from 300kHz to 2.2MHz using the RT pin, the TLVM1440x has a very wide range adjustable output voltage, even with a fixed inductor.

Several EMI reduction features are included in the module.

- Integrated high-frequency capacitor layouts minimize parasitic inductance, switch-voltage ringing, and radiated field coupling
- Integrated power MOSFETs with enhanced gate drive control enable low-noise PWM switching
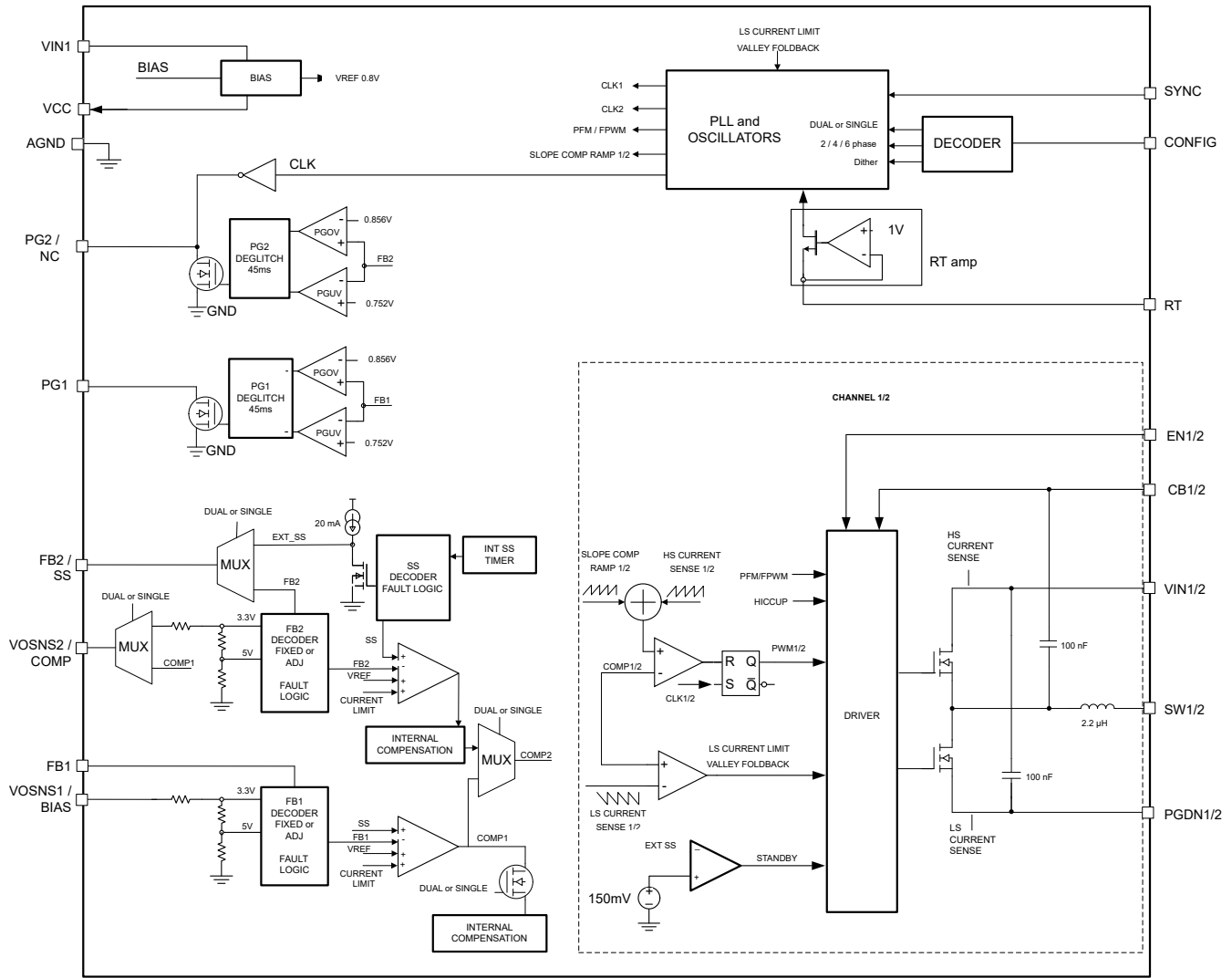
Together, these features significantly reduce EMI filtering requirements, while helping to meet CISPR 11 and CISPR 32 Class B EMI limits for conducted and radiated emissions.

The TLVM1440x module also includes inherent protection features for robust system requirements:

- An open-drain PGOOD indicator for power-rail sequencing and fault reporting
- Precision enable input with hysteresis, providing
  - Programmable line undervoltage lockout (UVLO)
  - Remote ON and OFF capability
- Internally fixed output-voltage soft start with monotonic start-up into prebiased loads in two output mode
- Externally adjustable soft start with monotonic start-up into prebiased loads in single output mode
- Hiccup-mode overcurrent protection with cycle-by-cycle peak and valley current limits
- Thermal shutdown with automatic recovery

Leveraging a pin arrangement designed for simple layout that requires only a few external components, the TLVM1440x is specified to maximum junction temperatures of 125°C. See typical thermal performance to estimate suitability in a given ambient environment.
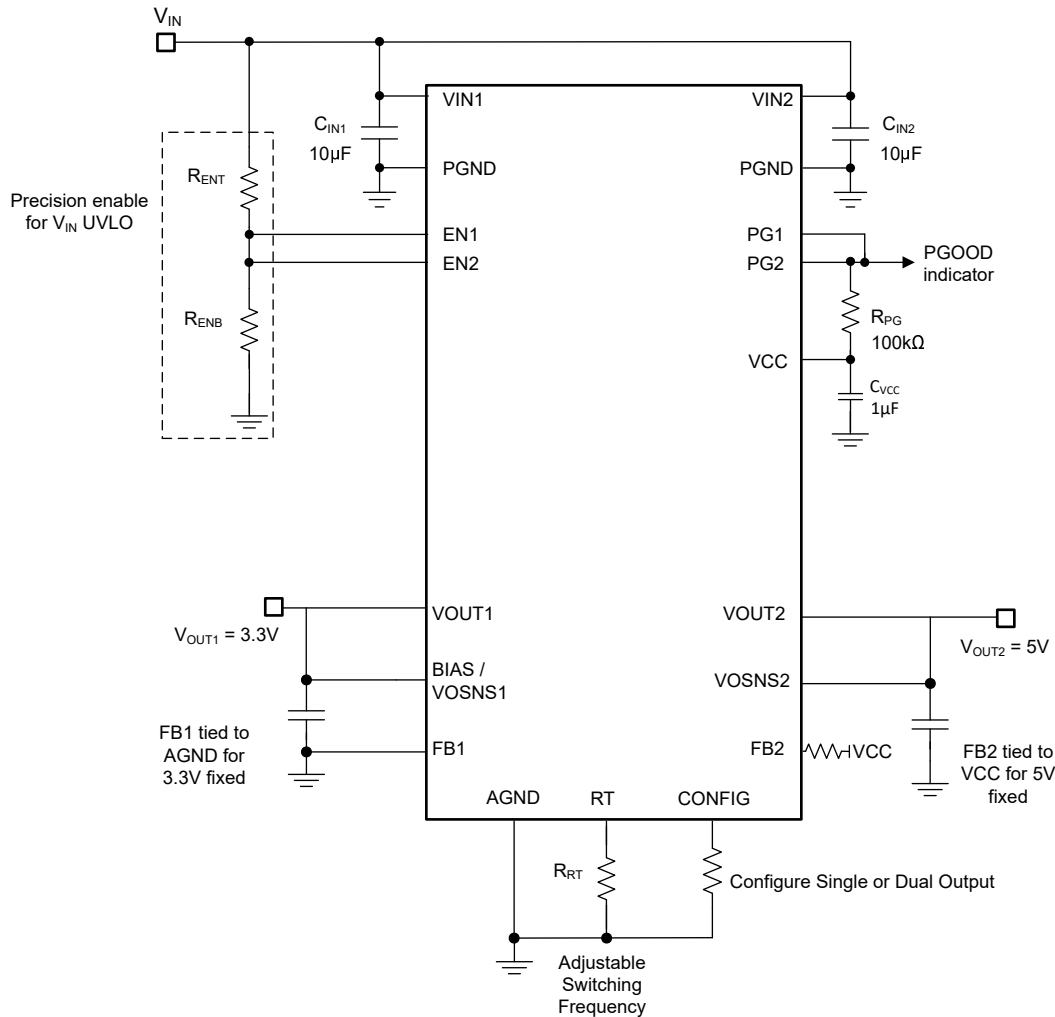
## 7.2 Functional Block Diagram

## 7.3 Feature Description

### 7.3.1 Input Voltage Range (VIN1, VIN2)

With a steady-state input voltage range from 3V to 36V, the TLVM1440x module is intended for step-down conversions from typical 12V, 24V, and 28V input supply rails. The schematic circuit in 図 7-1 shows all the necessary components to implement a TLVM1440x-based buck regulator using a single input supply.



**図 7-1. TLVM1440x Schematic Diagram With Input Voltage Operating Range of 3V to 36V**

The minimum input voltage required for start-up is 3.7V. Take extra care to make sure that the voltage at the VIN pins of the module (VIN1 and VIN2) does not exceed the absolute maximum voltage rating of 42V during line or load transient events. Voltage ringing at the VIN pins that exceeds the absolute maximum ratings can damage the IC.
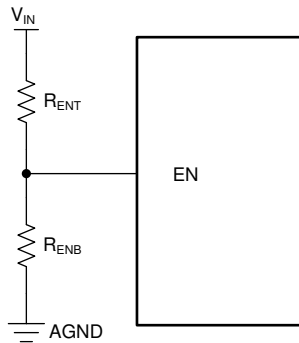
### 7.3.2 Enable EN Pin and Use as $V_{IN}$ UVLO

Apply a voltage less than 0.25V to the EN1 pin to put the TLVM1440x into shutdown mode. In shutdown mode, the quiescent current drops to 0.5µA (typical). Above this voltage but below the lower EN threshold, VCC is active but switching on SW1 and SW2 remains inactive. After EN1 is above $V_{EN}$, the SW1 becomes active. EN2 controls switching on the second output SW2. In dual output configuration EN2 can be used to independently turn off the second output voltage, but does not control when the device enters shutdown mode. In single output configuration EN1 must not be used to disable the secondary device for phase shedding and must be tied to

EN2. The very high efficiency of the device in PFM operation eliminates the need to phase shed in most designs as phase of the secondaries is controlled even under PFM operation.

The EN terminals can not be left floating. The simplest method to enable the operation is to connect the EN pins to VIN. This action allows the self-start-up of the device when VIN drives the internal VCC above the UVLO level. However, many applications benefit from employing an enable divider string, which establishes a precision input undervoltage lockout (UVLO). The precision UVLO can be used for the following:

- Sequencing
- Preventing the device from retriggering when used with long input cables
- Reducing the occurrence of deep discharge of a battery power source

Note that EN thresholds are accurate. The rising enable threshold has a 10% tolerance. Hysteresis is enough to prevent retriggering upon shutdown of the load (approximately 38%). The external logic output of another IC can also be used to drive the EN terminals, allowing system power sequencing.



**図 7-2. VIN UVLO Using the EN Pin**

Resistor values can be calculated using the following equations.

$$R_{ENB} = R_{ENT} \times \left( \frac{V_{EN(R)}}{V_{IN(on)} - V_{EN(R)}} \right) \tag{1}$$

$$V_{OFF} = V_{IN(on)} \times \left( 1 - V_{EN(H)} \right) \tag{2}$$

where

- $V_{ON}$ = $V_{IN}$ turn-on voltage
- $V_{OFF}$ = $V_{IN}$ turn-off voltage

Product Folder Links: *TLVM14404 TLVM14406*

English Data Sheet: SLVSHP0

### 7.3.3 CONFIG Device Configuration Pin

The CONFIG terminal is used to set up the device for either dual output or single output operation.

**表 7-1. R$_{CONFIG}$ Resistor Selection**

| R $_{CONFIG}$ (kΩ) | Mode |
|---|---|
| 0 | Dual output |
| 9.53 | Single output |
| 121 | Dual output |

When configured for single output operation, the VOSNS2 pin becomes the output of the error amplifier (COMP) and a resistor and capacitor are needed at this pin to compensate the control loop. R$_C$ = 11kΩ, C$_C$ = 2.2nF can be used in initial evaluation for many designs. Increasing the resistance results in higher loop gain and tends to require proportionately larger output capacitors. Decreasing the capacitance increases the loop response of the device, resulting in faster transients but can lower phase margin at the cross-over frequency and can require adjustments to the output capacitance. 表 7-2 provides several settings for different output configurations.

**表 7-2. Typical Bill of Materials**

| MODE | V$_{OUT1}$ | V$_{OUT2}$ | FREQUENCY | C$_{OUT}$ EACH PHASE | C$_{IN}$ + C$_{HF}$ | R$_C$ | C$_C$ |
|---|---|---|---|---|---|---|---|
| DUAL | 3.3V | 5V | 500kHz | 47 + 22µF | 2 × 10µF + 2 × 100nF | INTERNAL | INTERNAL |
| DUAL | 3.3V | 5V | 2100kHz | 2 × 22µF | 1 × 10µF + 2 × 100nF | INTERNAL | INTERNAL |
| SINGLE | 3.3V | 3.3V | 500kHz | 47 + 22µF | 2 × 10µF + 2 × 100nF | 11kΩ | 2.2nF |
| SINGLE | 5V | 5V | 2100kHz | 2 × 22µF | 1 × 10µF + 2 × 100nF | 11kΩ | 2.2nF |

Product Folder Links: *TLVM14404 TLVM14406*
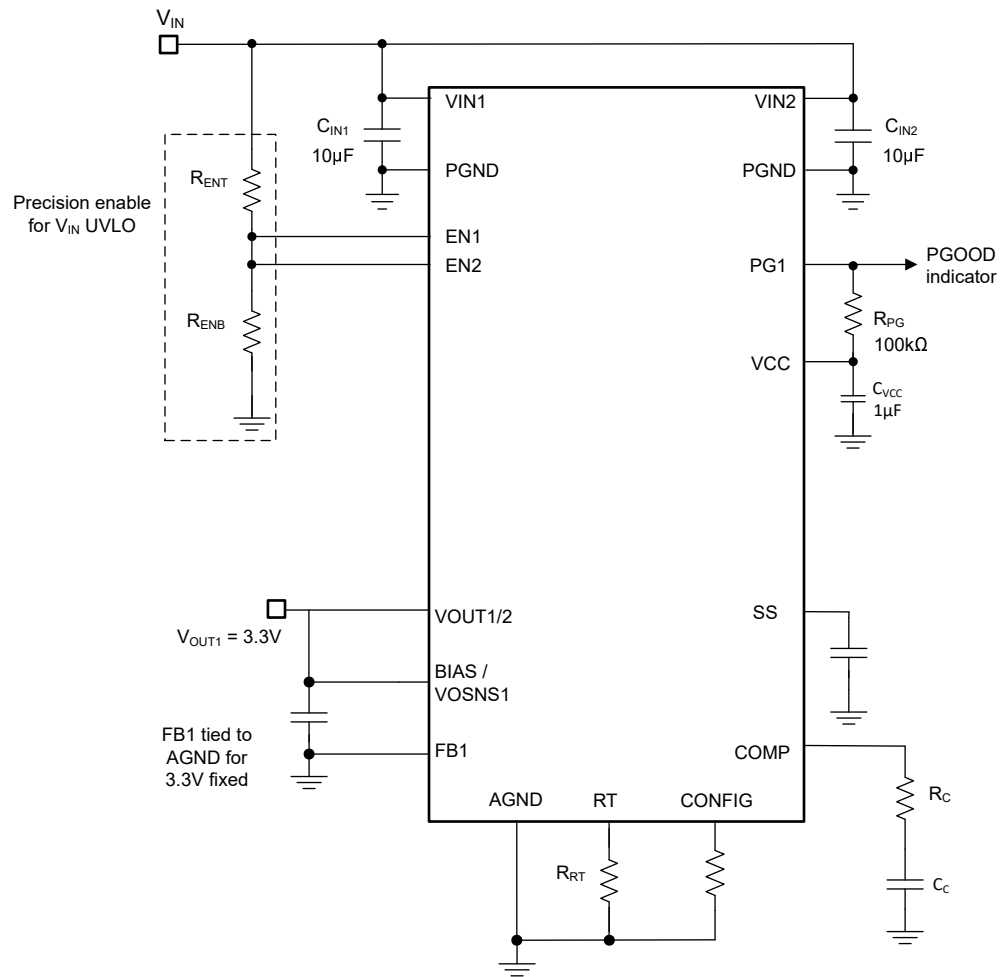
English Data Sheet: SLVSHP0

**図 7-3. High-efficiency, Single Output 2-Phase Step-Down Converter**

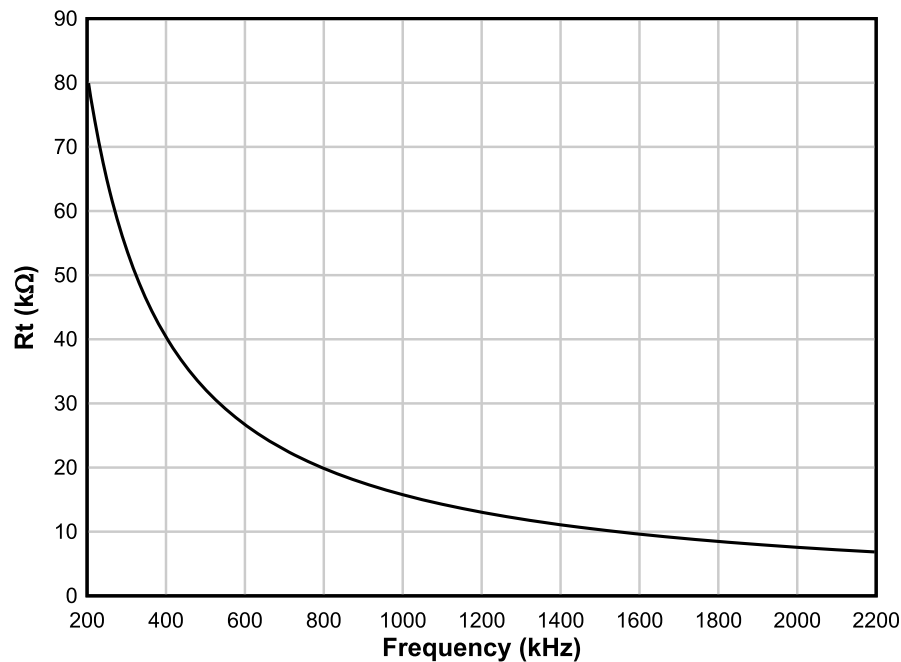### 7.3.4 Adjustable Switching Frequency

The frequency is set using a resistor on the RT pin. A resistor to AGND is used to set the adjustable operating frequency. See below for resistor values. A resistor value that falls outside of the recommended range can cause the device to stop switching.

$$R_T[k\Omega] = \left( \frac{16.4}{F_{SW}[\text{MHz}]} - 0.633 \right) \tag{3}$$

For example, for $f_{SW}$ = 400kHz, $R_T$ = (16.4 / 0.4) – 0.633 = 40.37, so a 40.2kΩ resistor is selected as the closest choice.

**表 7-3. Typical $R_T$ values**

| $R_T$ (kΩ) | Frequency (kHz) |
|---|---|
| 6.81 | 2206 |
| 7.15 | 2106 |
| 15.4 | 1005 |
| 31.6 | 497.4 |
| 39.2 | 402 |
| 158 | 101 |



**図 7-4. Setting Clock Frequency**

### 7.3.5 Adjustable Output Voltage (FB)

The TLVM1440x has an adjustable output voltage range from 0.8V up to a maximum of 9V or slightly less than $V_{IN}$, whichever is lower. Setting the output voltage requires two feedback resistors, designated as $R_{FBT}$ and $R_{FBB}$ in schematics. The reference voltage at the feedback (FB) pin is set at 0.8V with a feedback system accuracy over the full junction temperature range of ±1%. The junction temperature range for the device is −40°C to 125°C.

Calculate the value for $R_{FBB}$ using 式 4 below based on a recommended value for $R_{FBT}$ of 100kΩ.

$$R_{FBB}(k\Omega) = \frac{R_{FBT}(k\Omega)}{\frac{V_{OUT}}{0.8} - 1} \tag{4}$$

表 7-4 lists the standard resistor values for several output voltages and the recommended switching frequency range to maintain reasonable peak-to-peak inductor ripple current. This table also includes the minimum required output capacitance for each output voltage setting to maintain stability. The capacitances as listed represent *effective* values for ceramic capacitors derated for DC bias voltage and temperature. Furthermore, place a feedforward capacitor, $C_{FF}$, in parallel with $R_{FBT}$ to increase the phase margin when the output capacitance is close to the minimum recommended value.

**表 7-4. Standard $R_{FBT}$ Values, Recommended $F_{SW}$ Range and Minimum $C_{OUT}$**

| $V_{OUT}$ (V) | $R_{FBT}$ (kΩ) [1] | $R_{FBB}$ (kΩ) [1] | SUGGESTED $F_{SW}$ RANGE (kHz) | $C_{OUT(min)}$ (µF), Per Phase (EFFECTIVE) | BOM[2] | $C_{FF}$ (pF) |
|---|---|---|---|---|---|---|
| 0.8 | 10 | Open | 300 to 700 | 470 | 1 × 47µF (6.3V), 1 × 470µF (2.5V) | — |
| 1.8 | 12.4 | 10 | 300 to 1000 | 125 | 3 × 47µF (6.3V), 1 × 22µF (6.3V) | 330 |
| 3.3 | 31.2 | 10 | 500 to 1300 | 64 | 4 × 22µF (10V) | Internal |
| 5 | 52.3 | 10 | 700 to 2100 | 64 | 4 × 22µF (10V) | Internal |
| 9 | 105 | 10 | 1200 to 2100 | 40 | 3 × 22µF (16V) | 4.7 |

(1)  $R_{FBT}$ = 100kΩ.
(2)  Refer to 表 7-6 for the output capacitor list.

Note that higher feedback resistances consume less DC current. However, an upper $R_{FBT}$ resistor value higher than 1MΩ renders the feedback path more susceptible to noise. Higher feedback resistances generally require more careful layout of the feedback path. Make sure to locate the feedback resistors close to the FB and AGND pins, keeping the feedback trace as short as possible (and away from noisy areas of the PCB). See *Layout Example* guidelines for more detail.

### 7.3.6 Input Capacitors

Input capacitors are necessary to limit the input ripple voltage to the module due to switching-frequency AC currents. TI recommends using ceramic capacitors to provide low impedance and high RMS current rating over a wide temperature range. 式 5 gives the input capacitor RMS current. The highest input capacitor RMS current occurs at D = 0.5, at which point the RMS current rating of the capacitors must be greater than half the output current.

$$I_{CIN,rms} = \sqrt{D \times \left( I_{OUT}^2 \times (1 - D) + \frac{\Delta i_L^2}{12} \right)} \tag{5}$$

where

- D = $V_{OUT}$ / $V_{IN}$ is the module duty cycle.

Ideally, the DC and AC components of input current to the buck stage are provided by the input voltage source and the input capacitors, respectively. Neglecting inductor ripple current, the input capacitors source current of amplitude ($I_{OUT}$ − $I_{IN}$) during the D interval and sink $I_{IN}$ during the 1 − D interval. Thus, the input capacitors conduct a square-wave current of peak-to-peak amplitude equal to the output current. The resultant capacitive component of AC ripple voltage is a triangular waveform. Together with the ESR-related ripple component, 式 6 gives the peak-to-peak ripple voltage amplitude:

$$\Delta V_{IN} = \left( \frac{I_{OUT} \times D \times (1 - D)}{F_{SW} \times C_{IN}} + I_{OUT} \times R_{ESR} \right) \tag{6}$$

式 7 gives the input capacitance required for a particular load current:

$$C_{IN} \geq \left( \frac{I_{OUT} \times D \times (1 - D)}{F_{SW} \times (\Delta V_{IN} - I_{OUT} \times R_{ESR})} \right) \qquad (7)$$

where

- $\Delta V_{IN}$ is the input voltage ripple specification.

The TLVM1440x requires a minimum of two 10µF ceramic input capacitors, preferably with X7R or X7S dielectric and in 1206 or 1210 footprint. Additional capacitance can be required for applications to meet conducted EMI specifications, such as CISPR 11 or CISPR 32.

表 7-5 includes a preferred list of capacitors by vendor. To minimize the parasitic inductance in the switching loops, position the ceramic input capacitors in a symmetrical layout close to the VIN1 and VIN2 pins and connect the capacitor return terminals to the PGND pins using a copper ground plane under the module.

**表 7-5. Recommended Ceramic Input Capacitors**

| VENDOR[1] | DIELECTRIC | PART NUMBER | CASE SIZE | CAPACITANCE (µF)[2] | RATED VOLTAGE (V) |
|---|---|---|---|---|---|
| TDK | X7R | C3216X7R1H106K160AC | 1206 | 10 | 50 |
| Murata | X7S | GCM32EC71H106KA03K | 1210 | 10 | 50 |
| AVX | X7R | 12105C106MAT2A | 1210 | 10 | 50 |
| Murata | X7R | GRM32ER71H106KA12L | 1210 | 10 | 50 |

(1) Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table. See *Third-Part Products Disclaimer*.

(2) Nameplate capacitance values (the effective values are lower based on the applied DC voltage and temperature).

As discussed in *Power Supply Recommendations* , an electrolytic bulk capacitance (68µF to 100µF) provides low-frequency filtering and parallel damping to mitigate the effects of input parasitic inductance resonating with the low-ESR, high-Q ceramic input capacitors.

### 7.3.7 Output Capacitors

表 7-4 lists the TLVM1440x minimum amount of required output capacitance. The effects of DC bias and temperature variation must be considered when using ceramic capacitance. For ceramic capacitors in particular, the package size, voltage rating, and dielectric material contribute to differences between the standard rated value and the actual effective value of the capacitance.

When including additional capacitance above $C_{OUT(min)}$, the capacitance can be ceramic type, low-ESR polymer type, or a combination of the two. See 表 7-6 for a preferred list of output capacitors by vendor.

**表 7-6. Recommended Ceramic Output Capacitors**

| VENDOR[1] | DIELECTRIC | PART NUMBER | CASE SIZE | CAPACITANCE (µF)[2] | VOLTAGE (V) |
|---|---|---|---|---|---|
| Murata | X7R | GRM31CZ71C226ME15L | 1206 | 22 | 16 |
| TDK | X7R | C3225X7R1C226M250AC | 1210 | 22 | 16 |
| Murata | X7R | GRM32ER71C226KEA8K | 1210 | 22 | 16 |
| TDK | X6S | C3216X6S1E226M160AC | 1206 | 22 | 25 |
| AVX | X7R | 12103C226KAT4A | 1210 | 22 | 25 |
| Murata | X7R | GRM32ER71E226ME15L | 1210 | 22 | 25 |
| AVX | X7R | 1210ZC476MAT2A | 1210 | 47 | 10 |
| Murata | X7R | GRM32ER71A476ME15L | 1210 | 47 | 10 |
| Murata | X6S | GRM32EC81C476ME15L | 1210 | 47 | 16 |
| TDK | X6S | C3216X6S0G107M160AC | 1206 | 100 | 4 |
| Murata | X6T | GRM31CD80J107MEA8L | 1206 | 100 | 6.3 |
| Murata | X7S | GRM32EC70J107ME15L | 1210 | 100 | 6.3 |

(1) Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in the table. See *Third-Part Products Disclaimer* .

(2) Nameplate capacitance values (the effective values are lower based on the applied DC voltage and temperature).

### 7.3.8 Power-Good Output Voltage Monitoring

While the PG1/PG2 of the TLVM1440x resembles a standard power-good function, the functionality is designed to replace a discrete reset IC, reducing BOM cost. There are three major differences between the PG function and the normal power-good function seen in most regulators:

- A delay has been added for release of reset. See 表 7-7.
- PG output signals a fault (pulls the output to ground) while the part is disabled.
- PG continues to operate with input voltage as low as 1.2V. Below this input voltage, PG output can be high impedance.

For dual output configuration (R $_{CONFIG}$ = 0 or 121kΩ), The PG1 is an open-drain and must be tied through a resistor to an external voltage, and pulls low if the monitors on FB1 or VOSNS1 trip. The PG2 flag is configured in the same manner as PG1 and monitors the second output at either FB2 or VOSNS2.

For single-output operation (R $_{CONFIG}$ = 9.53kΩ), PG2 is no long active and the PG2/NC terminal of the primary device can be left floating.
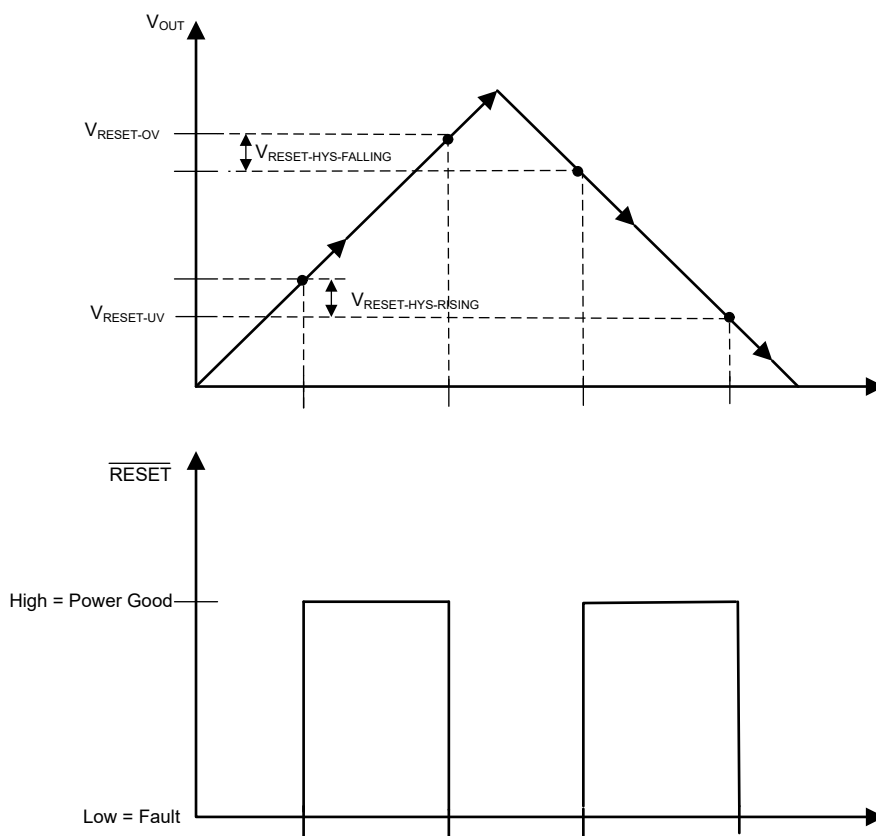


**図 7-5. PG Static Voltage Thresholds**

Product Folder Links: *TLVM14404 TLVM14406*

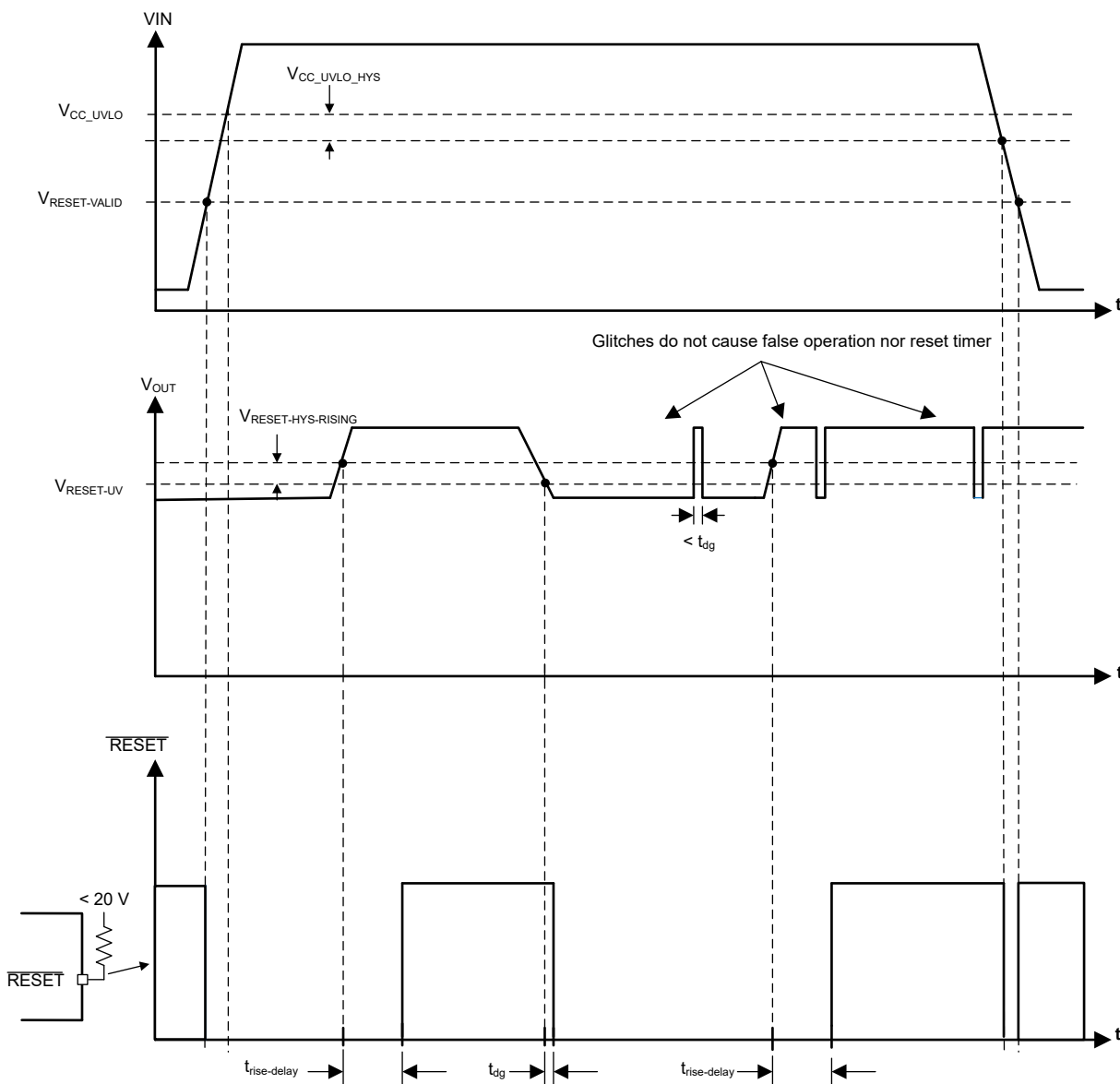English Data Sheet: SLVSHP0
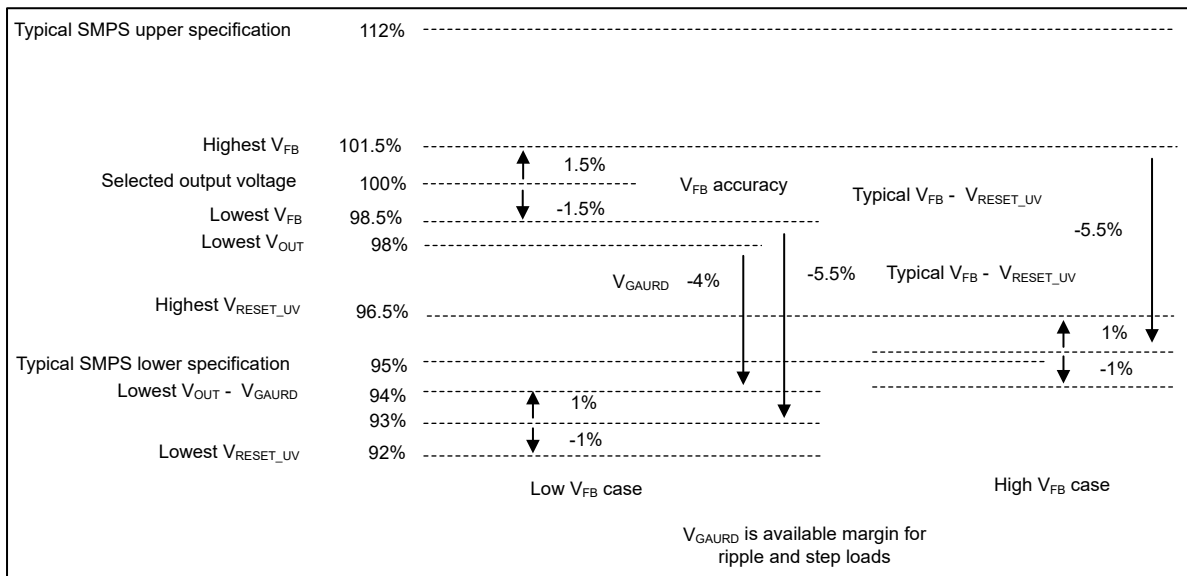
**図 7-6. PG Timing Diagram (Excludes OV Events)**

**表 7-7. Conditions that Cause PG to Signal a Fault (Pull Low)**

| FAULT CONDITION INITIATED | FAULT CONDITION ENDS (AFTER WHICH $t_{RESET\_ACT}$ MUST PASS BEFORE RESET OUTPUT IS RELEASED) |
|---|---|
| FB below $V_{RESET\_UV}$ for longer than $t_{RESET\_FILTER}$ | FB above $V_{RESET\_UV}$ + $V_{RESET\_HYST}$ for longer than $t_{RESET\_FILTER}$ |
| FB above $V_{RESET\_OV}$ for longer than $t_{RESET\_FILTER}$ | FB below $V_{RESET\_OV}$ − $V_{RESET\_HYST}$ for longer than $t_{RESET\_FILTER}$ |
| Junction temperature exceeds $T_{SD\_R}$ | Junction temperature falls below $T_{SD\_F}$ [1] |
| EN low | $t_{EN}$ passes after EN becomes high[1] |
| VIN falls low enough so that VCC falls below $V_{CC\_UVLO}$ - $V_{CC\_UVLO\_HYST}$. This value is called $V_{IN\_OPERATE}$. | Voltage on VIN is high enough so that VCC pin exceed $V_{CC\_UVLO}$ [1] |

(1) As an additional operational check, PG remains low during soft start. Soft start is defined as until the lesser of either full output voltage reached or $t_{SS2}$ has passed since initiation. This definition is true even if all other conditions in this table are met and $t_{RESET\_ACT}$ has passed. Lockout during soft start does not require $t_{RESET\_ACT}$ to pass before PG is released.

The threshold voltage for the PG function is specified to take advantage of the availability of the internal feedback threshold to the PG circuit. This allows a maximum threshold of 96.5% of selected output voltage to be specified at the same time as 96% of actual operating point. The net result is a more accurate reset function while expanding the system allowance for transient response. See the output voltage error stack-up comparison in 図 7-7.
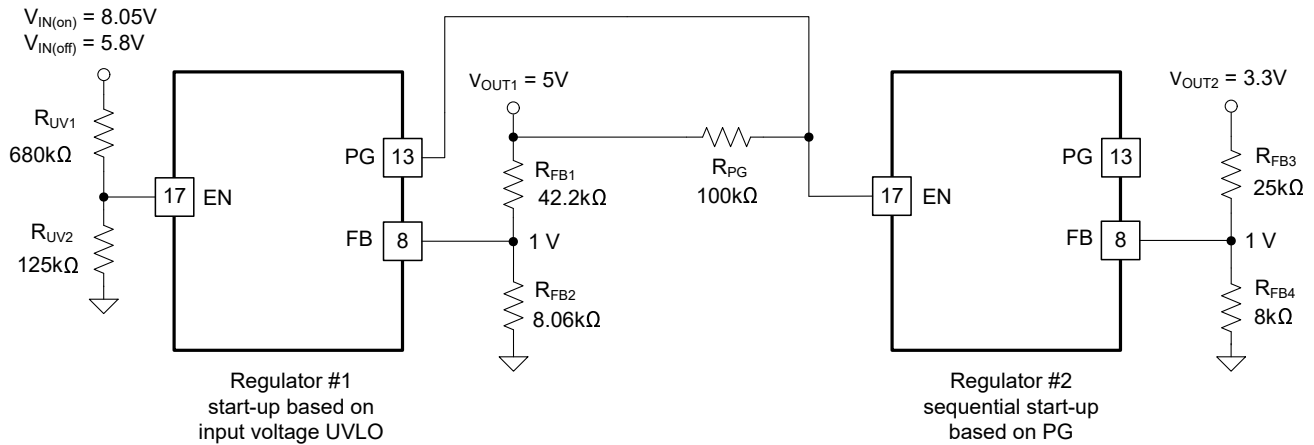
In addition to signaling a fault upon overvoltage detection (FB above $V_{RESET\_OV}$), the switch node is shut down and a small, approximately 1mA pulldown is applied to the SW node.



**図 7-7. Reset Threshold Voltage Stack-up**

Product Folder Links: *TLVM14404 TLVM14406*

English Data Sheet: SLVSHP0

The PG signal can be used for start-up sequencing of downstream regulators, as shown in the following figure, or for fault protection and output monitoring.



図 7-8. TLVM1440x Sequencing Implementation Using PG and EN|

### 7.3.9 Bias Supply Regulator (VCC, VOSNS)

VCC is the output of the internal LDO sub-regulator used to supply the control circuits of the TLVM1440x. The nominal VCC voltage is 3.3V. The VOSNS pin is the input to the internal LDO. Connect this input to $V_{OUT}$ to provide the lowest possible input supply current. If the VOSNS voltage is less than 3.1V, VIN1 and VIN2 directly power the internal LDO.

To prevent unsafe operation, VCC has UVLO protection that prevents switching if the internal voltage is too low. See $V_{CC\_UVLO}$ and $V_{CC\_UVLO\_HYS}$ in the *Electrical Characteristics* .

VCC must not be used to power external circuitry. Do not load VCC or short VCC to ground. VOSNS is an optional input to the internal LDO. Connect an optional high quality 0.1µF to 1µF capacitor from VOSNS to AGND for improved noise immunity.

The LDO provides the VCC voltage from one of two inputs: $V_{IN}$ or VOSNS. When VOSNS is tied to ground or below 3.1V, the LDO derives power from $V_{IN}$. The LDO input becomes VOSNS when VOSNS is tied to a voltage above 3.1V. The VOSNS voltage must not exceed both $V_{IN}$ and 12V.

式 8 specifies the LDO power loss reduction as:

$$P_{LDO-LOSS} = I_{LDO} \times (V_{VOSNS} - V_{VCC}) \qquad (8)$$

The VOSNS input provides an option to supply the LDO with a lower voltage than $V_{IN}$, thus minimizing the LDO input voltage relative to VCC and reducing power loss. For example, if the LDO current is 10mA at 1MHz with $V_{IN}$ = 24V and $V_{OUT}$ = 5V, the LDO power loss with VOSNS tied to ground is 10mA × (24V – 3.3V) = 207mW, while the loss with VOSNS tied to $V_{OUT}$ is equal to 10mA × (5V – 3.3V) = 17mW – a reduction of 190mW.

### 7.3.10 Overcurrent Protection (OCP)

The TLVM1440x is protected from overcurrent conditions using cycle-by-cycle current limiting of the peak inductor current. The current is compared every switching cycle to the current limit threshold. During an overcurrent condition, the output voltage decreases.

The TLVM1440x employs hiccup overcurrent protection if there is an extreme overload. In hiccup mode, the TLVM1440x module is shut down and kept off for 40ms (typical) before a restart is attempted. If an overcurrent or short-circuit fault condition still exists, hiccup repeats until the fault condition is removed. Hiccup mode reduces power dissipation under severe overcurrent conditions, thus preventing overheating and potential

damage to the device. After the fault is removed, the module automatically recovers and returns to normal operation.

### 7.3.11 Thermal Shutdown

Thermal shutdown is an integrated self-protection used to limit junction temperature and prevent damage related to overheating. Thermal shutdown turns off the device when the junction temperature exceeds 168°C (typical) to prevent further power dissipation and temperature rise. Junction temperature decreases after shutdown, and the TLVM1440x attempts to restart when the junction temperature falls to 159°C (typical).

## 7.4 Device Functional Modes

### 7.4.1 Shutdown Mode

The EN pin provides ON and OFF control for the TLVM1440x. When $V_{EN}$ is below approximately 0.4V, the device is in shutdown mode. Both the internal LDO and the switching regulator are off. The quiescent current in shutdown mode drops to 0.6µA (typical). The TLVM1440x also employs internal undervoltage protection. If the input voltage is below the UV threshold, the regulator remains off.

### 7.4.2 Standby Mode

The internal LDO for the VCC bias supply has a lower enable threshold than the regulator. When $V_{EN}$ is above 1.1V (maximum) and below the precision enable threshold of 1.263V (typical), the internal LDO is on and regulating. The precision enable circuitry is turned on after the internal $V_{CC}$ is above the UVLO threshold. The switching action and voltage regulation are not enabled until $V_{EN}$ rises above the precision enable threshold.

### 7.4.3 Active Mode

The TLVM1440x is in active mode when $V_{VCC}$ and $V_{EN}$ are above the relevant thresholds and no fault conditions are present. The simplest method to enable operation is to connect EN to $V_{IN}$, which allows self start-up when the applied input voltage exceeds the minimum start-up voltage.

Product Folder Links: *TLVM14404 TLVM14406*

English Data Sheet: SLVSHP0

# 8 Applications and Implementation

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注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

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## 8.1 Application Information

The TLVM1440x synchronous buck module requires only a few external components to convert from a wide range of supply voltages to an output voltage at an output current up to 3A per for dual output configuration and 6A for single output configuration.

## 8.2 Typical Applications

### 8.2.1 Design 1 – High-efficiency, Dual Output 5V at 3A, 3.3V at 3A, Synchronous Buck Regulator

図 8-1 shows the schematic diagram of a dual output 5V at 3A and 3.3V at 3A buck regulator with a switching frequency of 1MHz. In this example, the target efficiencies is 91.5% at full load, based on a nominal input voltage of 12V that ranges from 6.3V to 36V. A resistor of 15.4kΩ, $R_{RT}$, sets the free-running switching frequency at 1MHz.
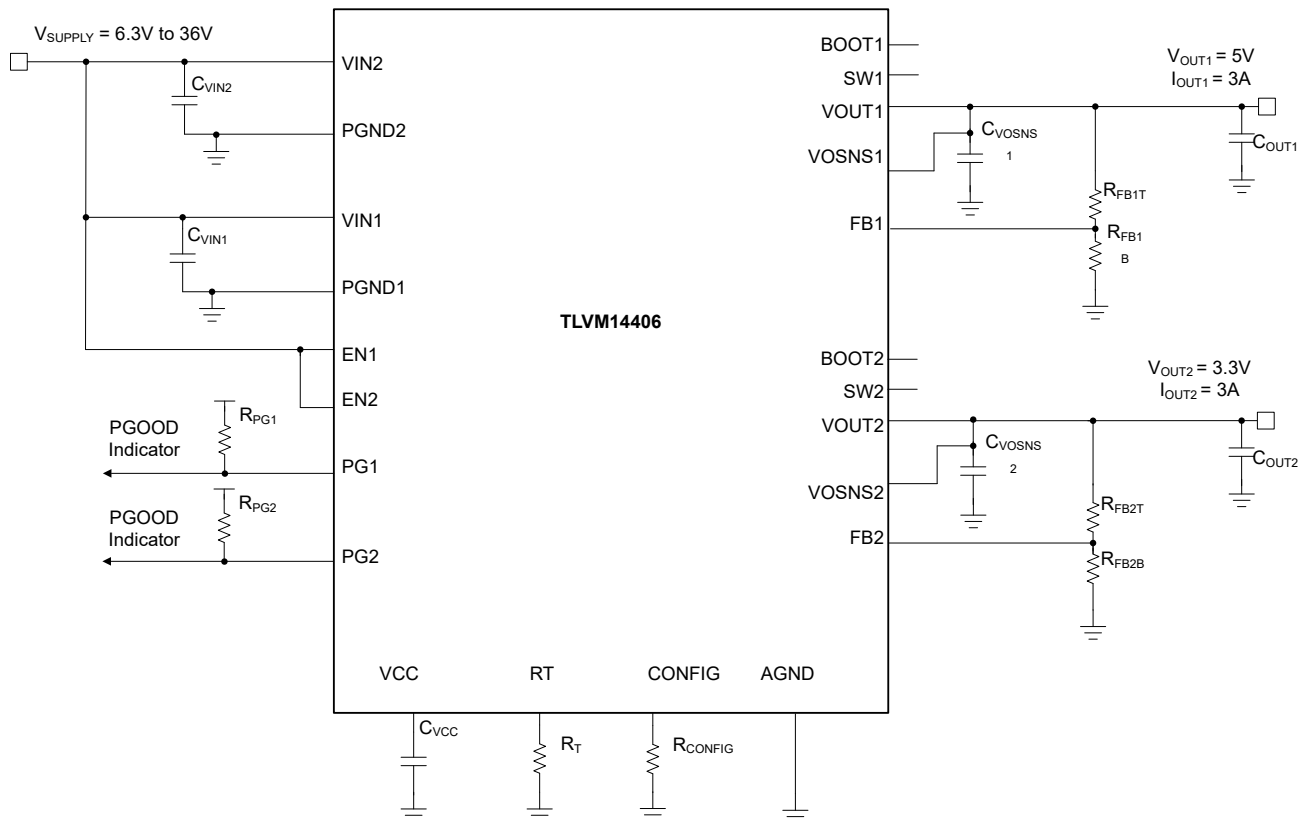


**図 8-1. Circuit Schematic**

#### 8.2.1.1 Design Requirements

表 8-1 shows the intended input, output, and performance parameters for this application example.

---

表 8-1. Design Parameters

| DESIGN PARAMETER | VALUE |
|---|---|
| Input voltage range | 6.3V to 36V |
| Input voltage UVLO turn on, off | 6V, 4.3V |
| Output voltage 1 | 5V |
| Output voltage 2 | 3.3V |
| Full-load current 1 | 3A |
| Full-load current 2 | 3A |
| Switching frequency | 1MHz |
| Output voltage regulation | ±1% |

表 8-2 provides the selected buck module power-stage components with availability from multiple vendors. This design uses an all-ceramic output capacitor implementation.

表 8-2. List of Materials for Application Circuit 1

| REF DES | QTY | SPECIFICATION | MANUFACTURER[1] | PART NUMBER |
|---|---|---|---|---|
| $C_{IN1}$, $C_{IN2}$ | 4 | 10µF, 50V, X5R, 0805, ceramic | Murata | GRM21BR61H106ME43L |
| $C_{INBULK}$ | 1 | 100µF, 50V electrolytic | Panasonic | EEE-FK1H101P |
| $C_{OUT1}$, $C_{OUT2}$ | 4 | 22µF, 25V, X7R, 1210, ceramic | Murata | GRM32ER71E226KE15L |
| | 2 | 1µF, 25V, X7R, 0603, ceramic | Murata | GCM188R71E105KA64D |
| $U_1$ | 1 | TLVM1440x 36V, 6A synchronous buck module | Texas Instruments | TLVM1440xRDLR |

(1)     See *Third-Party Product Disclaimer*.

Product Folder Links: *TLVM14404 TLVM14406*

English Data Sheet: SLVSHP0

### 8.2.1.2 Detailed Design Procedure

#### 8.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TLVM1440x module with WEBENCH® Power Designer.

1.  Start by entering the input voltage ($V_{IN}$), output voltage ($V_{OUT}$), and output current ($I_{OUT}$) requirements.
2.  Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3.  Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

*   Run electrical simulations to see important waveforms and circuit performance.
*   Run thermal simulations to understand board thermal performance.
*   Export customized schematic and layout into popular CAD formats.
*   Print PDF reports for the design, and share the design with colleagues.

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

#### 8.2.1.2.2 Output Voltage Setpoint

The feedback resistor divider equation can be used to calculate the output voltage setpoint for both outputs. Recommended values for $R_{FB1T}$ and $R_{FB2T}$ is 100kΩ for improved noise immunity compared to 1MΩ and reduced current consumption compared to lower resistance values. Calculate $R_{FB1B}$ and $R_{FB2B}$ using the following equation:

$$R_{FBB} = \frac{R_{FBT} \times V_{REF}}{V_{OUT} - V_{REF}}$$

(9)

Choose the closest standard value of 19kΩ for $R_{FB1B}$ which correlates to a $V_{OUT1}$ of 5V. Additionally, choose the closest standard value of 32kΩ for $R_{FB2B}$ which correlates to a $V_{OUT2}$ of 3.3V.

#### 8.2.1.2.3 Switching Frequency Selection

Connect a 15.4kΩ resistor from RT to AGND to set a switching frequency of 1MHz for each output.

#### 8.2.1.2.4 Input Capacitor Selection

The TLVM1440x requires a minimum input capacitance of 4 × 10µF ceramic, preferably with X7R dielectric. The voltage rating of input capacitors must be greater than the maximum input voltage. For this design, select four 10µF, X7R, 50V, 0805 case size, ceramic capacitors connected from VIN1 and VIN2 to PGND as close as possible to the module. See 図 8-24 for recommended layout placement.

#### 8.2.1.2.5 Output Capacitor Selection

From 表 7-4, the TLVM1440x requires a minimum of 24µF of effective output capacitance for proper operation at an output voltage of 5V at 1MHz and requires a minimum of 37µF of effective output capacitance for proper operation at an output voltage of 3.3V at 1MHz. Use high-quality ceramic type capacitors with sufficient voltage and temperature rating. If needed, connect additional output capacitance to reduce ripple voltage or for applications with specific load transient requirements.

For this design example, use two 22µF, 25V rated, X7R, 1210, ceramic capacitors connected close to the module from the VOUT1 to PGND and two 22µF, 25V rated, X7R, 1210, ceramic capacitors from the VOUT2 pins to PGND. Use the derating curves from the capacitor data sheet to gauge the effective capacitance by temperature and DC bias.

#### 8.2.1.2.6 Other Considerations

To increase phase margin when using an output capacitance close to the minimum in 表 7-4, a feedforward capacitor, designated as $C_{FF}$ can be placed across the upper feedback resistor. Place the zero created by $C_{FF}$ and $R_{FBT}$ higher than one fifth the switching to boost the phase without significantly increasing the crossover

frequency. Because this $C_{FF}$ capacitor can conduct noise from the output of the circuit directly to the FB node of the IC, a 4.99kΩ resistor, $R_{FF}$, must be placed in series with $C_{FF}$. If the ESR zero of the output capacitor is below 200kHz, do not use CFF.

Additionally, for a dual output voltage output of 5V for VOUT1 and 3.3V for VOUT2, a fixed-frequency configuration can be used. Connect FB to VCC through a 10kΩ resistor for a 5V output or connect FB to AGND for a 3.3V output. With the use of internal fixed feedback resistors, higher efficiency can be observed.

### 8.2.1.3 Application Curves

**Efficiency and Load Regulation Performance**

Unless otherwise indicated, VIN = 12V, VOUT1 = 5V, VOUT2 = 3.3V, IOUT1 = 3A, IOUT2 = 3A and $f_{SW}$ = 1MHz.



PFM Mode, FSW = 1MHz

**図 8-2. Efficiency, VOUT = 5V**



PFM Mode, FSW = 1MHz

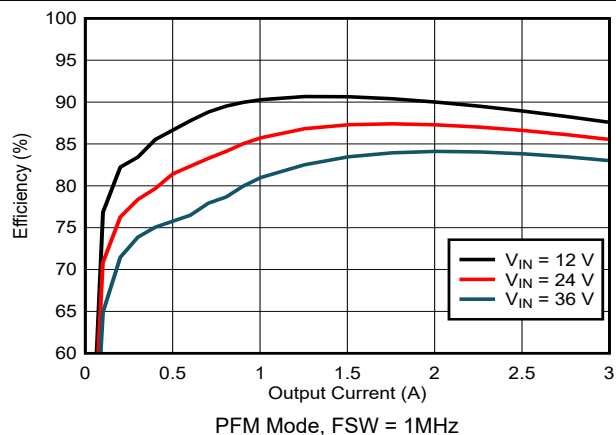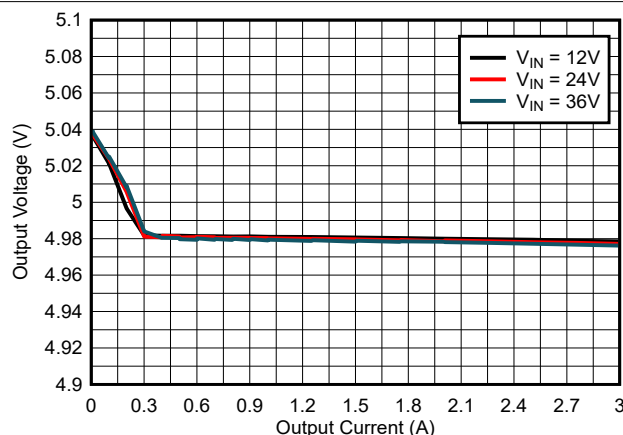**図 8-3. Efficiency, VOUT = 3.3V**



**図 8-4. Load Regulation, VOUT = 5V, PFM Mode**



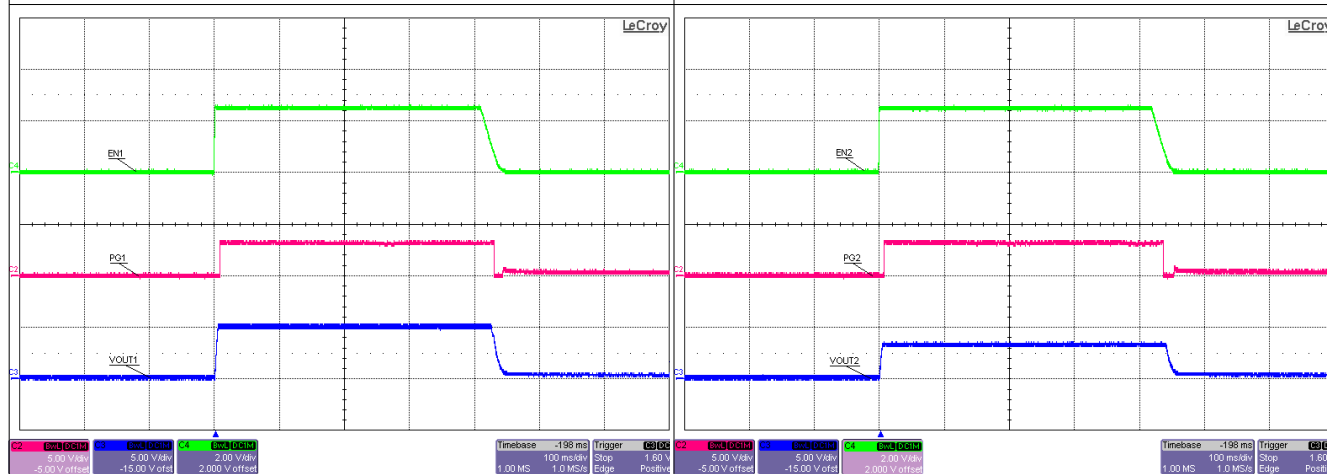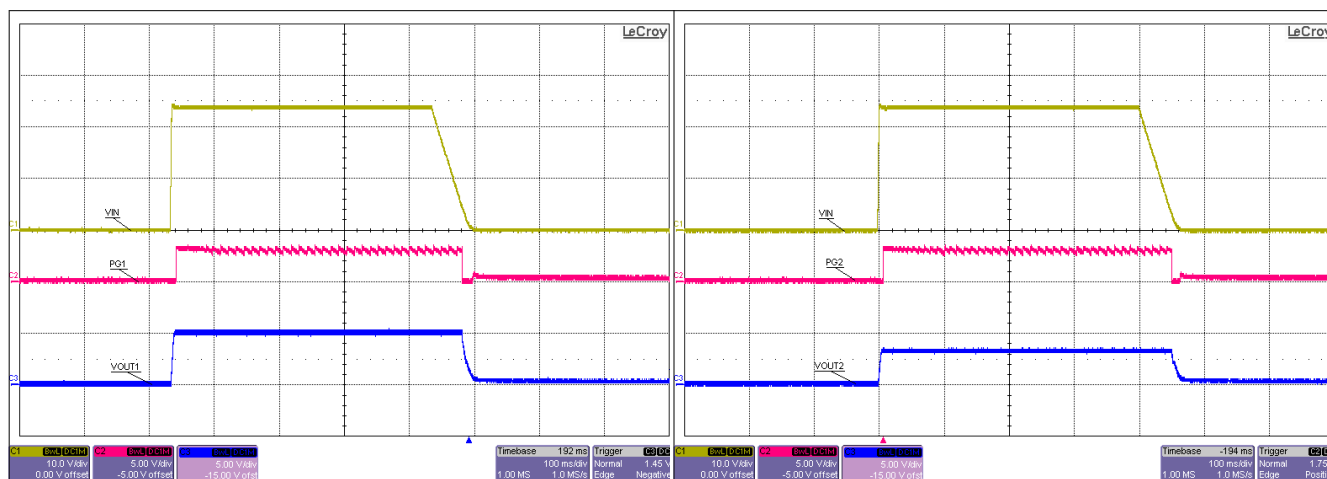**図 8-5. Load Regulation, VOUT = 3.3V, PFM Mode**

Product Folder Links: *TLVM14404 TLVM14406*

English Data Sheet: SLVSHP0

## Waveforms and Plots



図 8-6. Start-up and Shutdown, VOUT1 = 5V



図 8-7. Start-up and Shutdown, VOUT2 = 3.3V



VIN = 24V

図 8-8. Enable ON and OFF, VOUT1 = 5V



VIN = 24V

図 8-9. Enable ON and OFF, VOUT2 = 3.3V



VOUT1 = 5V, IOUT1 = 3A to 6A at 1A/μs

図 8-10. Load Transient Rising (CH1)



VOUT1 = 5V, IOUT1 = 6A to 3A at 1A/μs

図 8-11. Load Transient Falling (CH1)

Product Folder Links: *TLVM14404 TLVM14406*
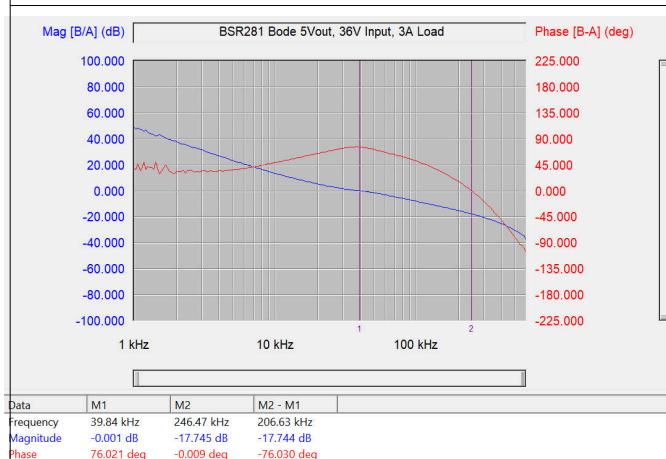
English Data Sheet: *SLVSHP0*
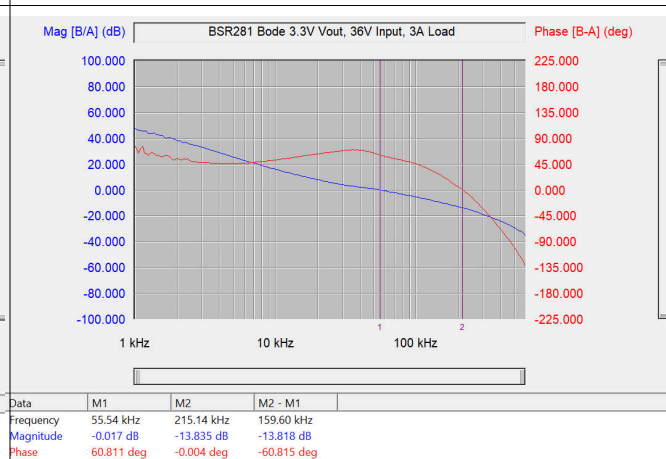
VOUT2 = 3.3V, IOUT2 = 1.5A to 3A at 1A/µs

**図 8-12. Load Transient Rising (CH2)**



VOUT2 = 3.3V, IOUT2 = 3A to 1.5A at 1A/µs
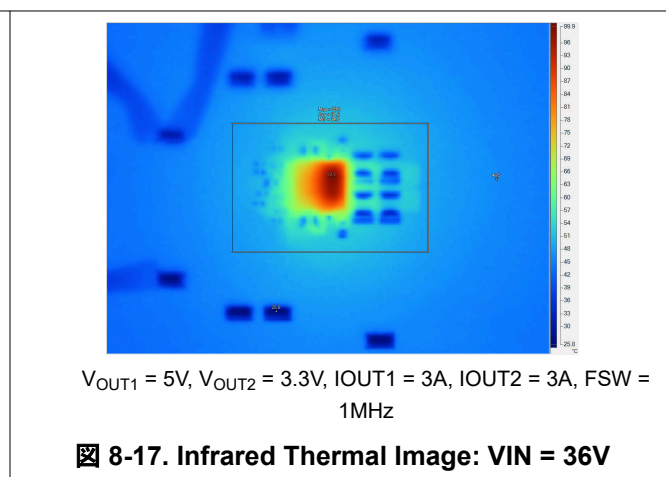
**図 8-13. Load Transient Falling (CH2)**



**図 8-14. Bode Plot (CH1)**
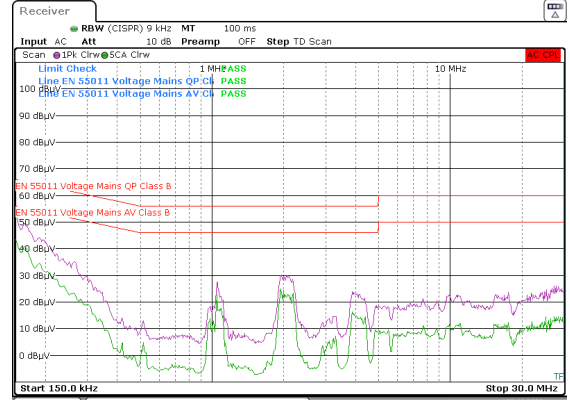


**図 8-15. Bode Plot (CH2)**

## Thermal Performance



$V_{OUT1}$ = 5V, $V_{OUT2}$ = 3.3V, IOUT1 = 3A, IOUT2 = 3A, FSW = 1MHz

**図 8-16. Infrared Thermal Image: VIN = 12V**



$V_{OUT1}$ = 5V, $V_{OUT2}$ = 3.3V, IOUT1 = 3A, IOUT2 = 3A, FSW = 1MHz

**図 8-17. Infrared Thermal Image: VIN = 36V**

## EMI Performance



$V_{OUT1}$ = 5V, $V_{OUT2}$ = 3.3V, $I_{OUT1}$ = 3A, $I_{OUT2}$ = 3A, $F_{SW}$ = 1MHz

**図 8-18. CISPR 11/32 Class B Conducted Emissions: $V_{IN}$ = 12V**
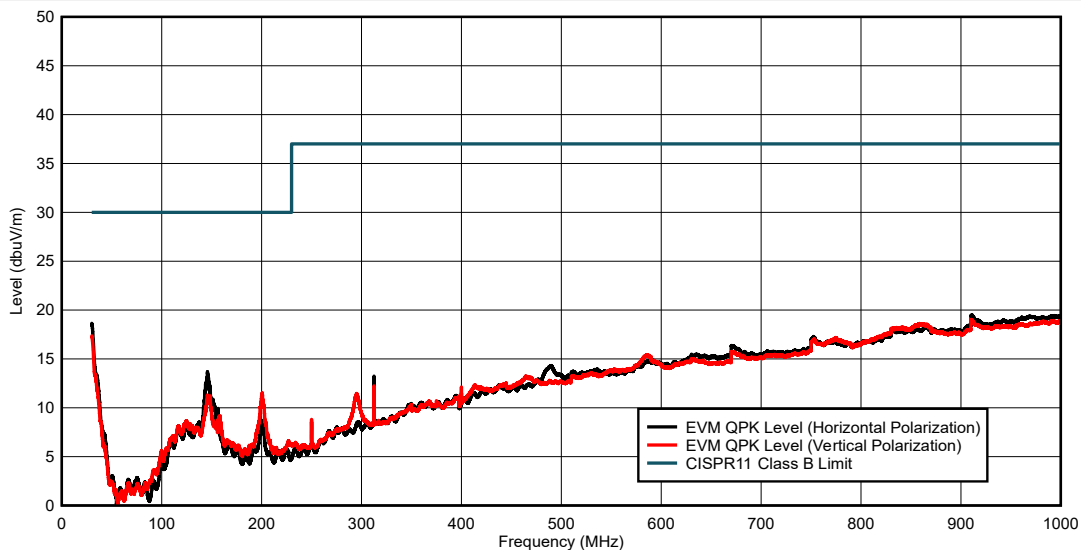


$V_{OUT}$ = 5V, $V_{OUT2}$ = 3.3V, $I_{OUT1}$ = 3A, $I_{OUT2}$ = 3A, $F_{SW}$ = 1MHz

**図 8-19. CISPR 11/32 Class B Conducted Emissions: $V_{IN}$ = 24V**



$V_{OUT}$ = 5V, $V_{OUT2}$ = 3.3V, $I_{OUT1}$ = 3A, $I_{OUT2}$ = 3A, $F_{SW}$ = 1MHz

**図 8-20. CISPR 11/32 Class B Radiated Emissions: $V_{IN}$ = 24V**

Product Folder Links: *TLVM14404 TLVM14406*

English Data Sheet: SLVSHP0

### 8.2.2 Design 2 – High-efficiency, 6A, Synchronous Buck Regulator for Industrial Applications

The following figure shows the schematic diagram of a 5V, 6A buck regulator with a switching frequency of 2.1MHz. In this example, the target efficiencies is 90%, based on a nominal input voltage of 12V that ranges from 7V to 36V. A resistor of 6.9kΩ, $R_{RT}$, sets the free-running switching frequency at 2.1MHz.
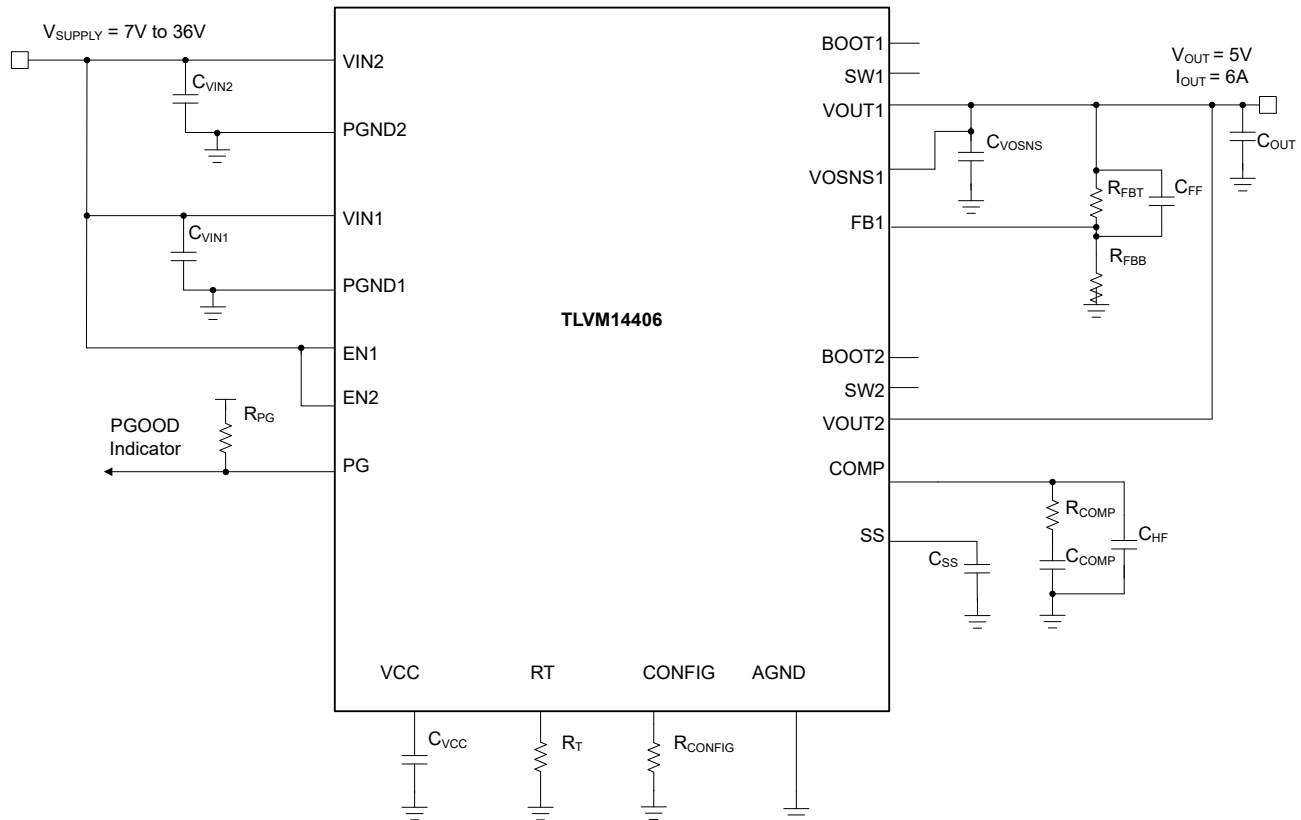


**図 8-21. Circuit Schematic**

#### 8.2.2.1 Design Requirements

The following table shows the intended input, output, and performance parameters for this application example. Note that if the input voltage decreases below approximately 7V, the regulator operates in dropout with the output voltage below the 5V setpoint.

**表 8-3. Design Parameters**

| DESIGN PARAMETER | VALUE |
|---|---|
| Input voltage range | 7V to 36V |
| Input voltage UVLO turn on, off | 6V, 4.3V |
| Output voltage | 5V |
| Maximum output current | 6A |
| Switching frequency | 2.1MHz |
| Output voltage regulation | ±1% |
| Module shutdown current | < 1μA |

表 8-4 provides the selected buck module power-stage components with availability from multiple vendors. This design uses an all-ceramic output capacitor implementation.

Product Folder Links: *TLVM14404 TLVM14406*

English Data Sheet: SLVSHP0

#### 表 8-4. List of Materials for Application Circuit 2

| REFERENCE DESIGNATOR | QTY | SPECIFICATION | MANUFACTURER[1] | PART NUMBER |
|---|---|---|---|---|
| $C_{IN1}$, $C_{IN2}$ | 4 | 2.2µF, 50V, X7R, 0805, ceramic | TDK | C2012X7R1H225K125AC |
| $C_{INBULK}$ | 1 | 100µF, 50V electrolytic | Panasonic | EEE-FK1H101P |
| $C_{OUT1}$, $C_{OUT2}$ | 5 | 10µF, 25V, X7R, 1210, ceramic | TDK | C3225X7R1E106K250AC |
| | 1 | 22µF, 25V, X7R, 1210, ceramic | TDK | CNA6P1X7R1E226M250AE |
| $U_1$ | 1 | TLVM1440x 36V, 6A synchronous buck module | Texas Instruments | TLVM1440xRDLR |

(1)   See *Third-Party Product Disclaimer*.

More generally, the TLVM1440x module is designed to operate with a wide range of external components and system parameters. However, the integrated loop compensation is optimized for a certain range of output capacitance.

#### 8.2.2.2 Detailed Design Procedure

##### 8.2.2.2.1 Output Voltage Setpoint

The output voltage of a TLVM1440x module is externally adjustable using a resistor divider. A recommended value for $R_{FBT}$ of 100kΩ for improved noise immunity compared to 1MΩ and reduced current consumption compared to lower resistance values. Calculate $R_{FBB}$ using the following equation:

$$R_{FBB} = \frac{R_{FBT} \times V_{REF}}{V_{OUT} - V_{REF}} \tag{10}$$

Choose the closest standard value of 19kΩ for $R_{FBB}$ which correlates to a $V_{OUT}$ of 5V.

##### 8.2.2.2.2 Switching Frequency Selection

Connect a 6.9kΩ resistor from RT to AGND to set a switching frequency of 2.1MHz per phase, which is designed for an output of 5V as the device establishes an inductor peak-to-peak ripple current in the range of 20% to 40% of the 6A rated output current at a nominal input voltage of 12V.

##### 8.2.2.2.3 Input Capacitor Selection

The TLVM1440x requires a minimum input capacitance of 4 × 10µF ceramic, preferably with X7R dielectric. The voltage rating of input capacitors must be greater than the maximum input voltage. For this design, select four 10µF, X7R, 50V, 0805 case size, ceramic capacitors connected from VIN1 and VIN2 to PGND as close as possible to the module. See 図 8-24 for recommended layout placement.

##### 8.2.2.2.4 Output Capacitor Selection

From the quick-start calculator, the TLVM1440x requires a minimum of 15µF of effective output capacitance for proper operation at an output voltage of 5V at 2.1MHz. Use high-quality ceramic type capacitors with sufficient voltage and temperature rating. If needed, connect additional output capacitance to reduce ripple voltage or for applications with specific load transient requirements.

For this design example, use five 10µF, 25V, X7R, 1210 and one 4µF, 16V, X5R, 1210 ceramic capacitors connected close to the module from the VOUT1 and VOUT2 pins to PGND. Use the derating curves from the capacitor data sheet to gauge the effective capacitance by temperature and DC bias.
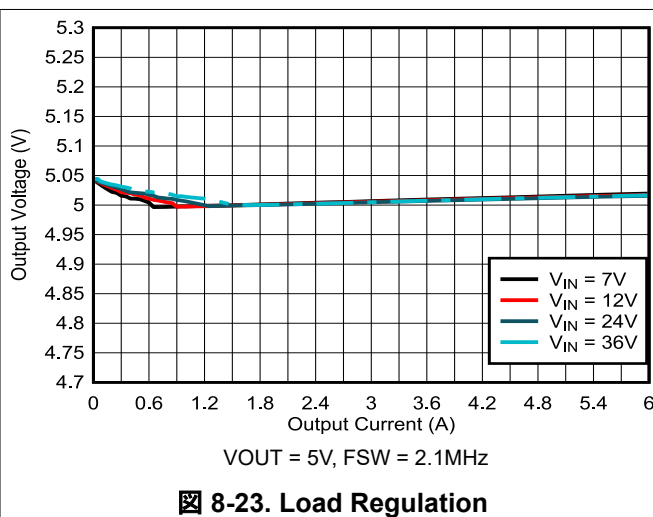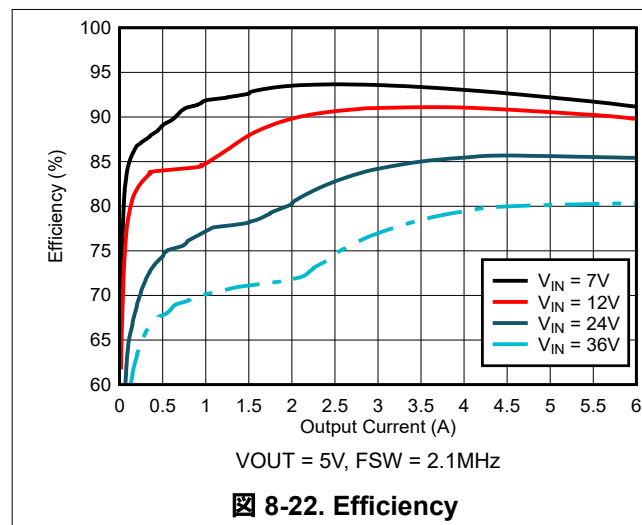
##### 8.2.2.2.5 Other Connections

To increase phase margin when using an output capacitance close to the minimum in 表 7-4, a feedforward capacitor, designated as $C_{FF}$ can be placed across the upper feedback resistor. Place the zero created by $C_{FF}$ and $R_{FBT}$ higher than one fifth the switching to boost the phase without significantly increasing the crossover frequency. Because this $C_{FF}$ capacitor can conduct noise from the output of the circuit directly to the FB node of the IC, a 4.99kΩ resistor, $R_{FF}$, must be placed in series with $C_{FF}$. If the ESR zero of the output capacitor is below 200kHz, do not use CFF.

Additionally, for an output voltage output of 5V or 3.3V, a fixed-frequency configuration can be used. Connect FB to VCC through a 10kΩ resistor for a 5V output or connect FB to AGND for a 3.3V output. With the use of internal fixed feedback resistors, higher efficiency can be observed.

### 8.2.2.3 Application Curves

### Efficiency Performance



VOUT = 5V, FSW = 2.1MHz

**図 8-22. Efficiency**



VOUT = 5V, FSW = 2.1MHz

**図 8-23. Load Regulation**

## 8.3 Power Supply Recommendations

The TLVM1440x buck module is designed to operate over a wide input voltage range of 3V to 36V. The characteristics of the input supply must be compatible with the *Absolute Maximum Ratings* and *Recommended Operating Conditions* in this data sheet. In addition, the input supply must be capable of delivering the required input current to the loaded regulator circuit. Estimate the average input current with 式 11.

$$I_{IN} = \left( \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \right) \tag{11}$$

where

- η is the efficiency.

If the module is connected to an input supply through long wires or PCB traces with a large impedance, take special care to achieve stable performance. The parasitic inductance and resistance of the input cables can have an adverse affect on module operation. More specifically, the parasitic inductance in combination with the low-ESR ceramic input capacitors form an under-damped resonant circuit, possibly resulting in instability or voltage transients each time the input supply is cycled ON and OFF. The parasitic resistance causes the input voltage to dip during a load transient. If the module is operating close to the minimum input voltage, this dip can cause false UVLO triggering and a system reset.

The best method to solve such issues is to reduce the distance from the input supply to the module and use an electrolytic input capacitor in parallel with the ceramics. The moderate ESR of the electrolytic capacitor helps damp the input resonant circuit and reduce any overshoot or undershoot at the input. A capacitance in the range of 47µF to 100µF is typically sufficient to provide input parallel damping and helps hold the input voltage steady during large load transients. A typical ESR of 0.1Ω to 0.4Ω provides enough damping for most input circuit configurations.

## 8.4 Layout

Proper PCB design and layout is important in high-current, fast-switching module circuits (with high internal voltage and current slew rates) to achieve reliable device operation and design robustness this primarily affects the performance of EMI and thermal dissipation of the device on the board.

### 8.4.1 Layout Guidelines

The following list summarizes the essential guidelines for PCB layout and component placement to optimize DC/DC module performance, including thermals and EMI signature. 図 8-24 shows a recommended PCB layout for the TLVM1440x with optimized placement and routing of the power-stage and small-signal components.

- *Place input capacitors as close as possible to the VIN pins.* Note the dual and symmetrical arrangement of the input capacitors based on the VIN1 and VIN2 pins located on each side of the module package. The high-frequency currents are split in two and effectively flow in opposing directions such that the related magnetic fields contributions cancel each other, leading to improved EMI performance.
  - Use low-ESR 1206 or 1210 ceramic capacitors with X7R or X7S dielectric. The module has integrated dual 0402 input capacitors for high-frequency bypass.
  - Ground return paths for the input capacitors must consist of localized top-side planes that connect to the PGND pads under the module.
  - Use a wide polygon plane on a lower PCB layer to connect these pins together and to the input supply, even though the VIN pins are connected internally
- *Place output capacitors as close as possible to the VOUT pins.* A similar dual and symmetrical arrangement of the output capacitors enables magnetic field cancellation and EMI mitigation.
  - Make sure ground return paths for the output capacitors consist of localized top-side planes that connect to the PGND pads under the module.
  - Use a wide polygon plane on a lower PCB layer to connect these pins together and to the load, thus reducing conduction loss and thermal stress, even though the VOUT pins are connected internally

- *Keep the FB trace as short as possible by placing the feedback resistors close to the FB pin.* Reduce noise sensitivity of the output voltage feedback path by placing the resistor divider close to the FB pin, rather than close to the load. FB is the input to the voltage-loop error amplifier and represents a high-impedance node sensitive to noise. Route a trace from the upper feedback resistor to the required point of output voltage regulation.
- *Use a solid ground plane on the PCB layer directly below the top layer with the module.* This plane acts as a noise shield by minimizing the magnetic fields associated with the currents in the switching loops. Connect AGND pins 6 and 11 directly to PGND pin 19 under the module.
- *Provide enough PCB area for proper heat sinking.* Use sufficient copper area to achieve a low thermal impedance commensurate with the maximum load current and ambient temperature conditions. Provide adequate heat sinking for the TLVM1440x to keep the junction temperature below 150°C. For operation at full rated load, the top-side ground plane is an important heat-dissipating area. Use an array of heat-sinking vias to connect the exposed pads (PGND) of the package to the PCB ground plane. If the PCB has multiple copper layers, connect these thermal vias to inner-layer ground planes. Make the top and bottom PCB layers preferably with two-ounce copper thickness (and no less than one ounce).
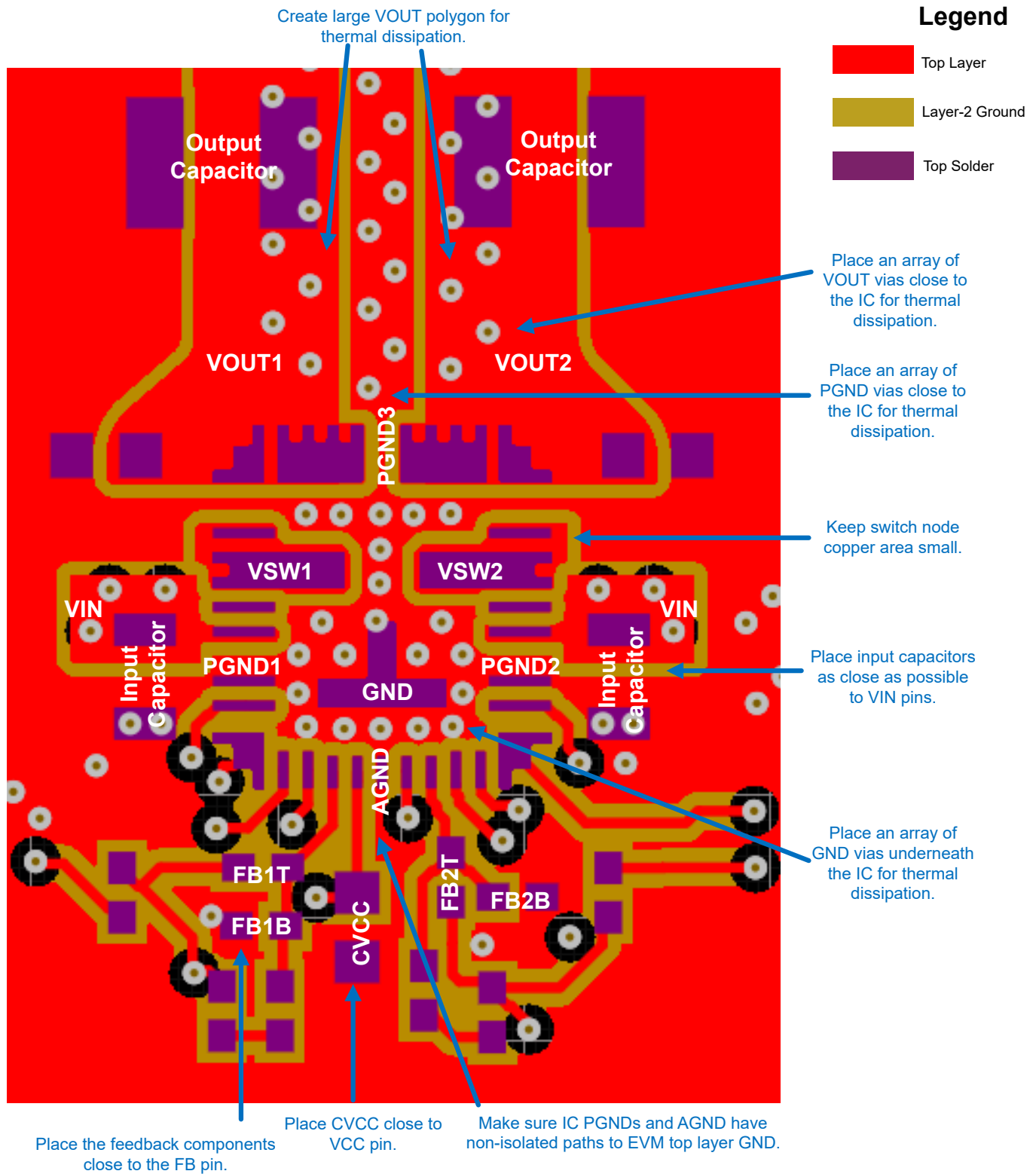
**8.4.1.1 Thermal Design and Layout**

For a DC/DC module to be useful over a particular temperature range, the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The TLVM1440x module is available in a small 6.5mm × 7.55mm 28-pin QFN package to cover a range of application requirements. The *Thermal Information* table summarizes the thermal metrics of this package with related detail provided by the *Semiconductor and IC Package Thermal Metrics* application note.

The 28-pin QFN package offers a means of removing heat through the exposed thermal pads at the base of the package. This design allows a significant improvement in heat sinking. Designing the PCB with thermal lands, thermal vias, and one or more grounded planes is imperative to complete the heat removal subsystem. The exposed pads of the TLVM1440x are soldered to the ground-connected copper lands on the PCB directly underneath the device package, reducing the thermal resistance to a very low value.

Preferably, use a four-layer board with 2oz copper thickness for all layers to provide low impedance, proper shielding and lower thermal resistance. Numerous vias with a 0.3mm diameter connected from the thermal lands to the internal and solder-side ground planes are vital to promote heat transfer. In a multilayer PCB stack-up, a solid ground plane is typically placed on the PCB layer below the power-stage components. Not only does this design provide a plane for the power-stage currents to flow, but the design also represents a thermally conductive path away from the heat-generating device.

### 8.4.2 Layout Example



**図 8-24. Typical Top Layer Design**

Product Folder Links: *TLVM14404 TLVM14406*

English Data Sheet: SLVSHP0

# 9 Device and Documentation Support

## 9.1 Device Support

### 9.1.1 サード・パーティ製品に関する免責事項

サード・パーティ製品またはサービスに関するテキサス・インスツルメンツの出版物は、単独またはテキサス・インスツルメンツの製品、サービスと一緒に提供される場合に関係なく、サード・パーティ製品またはサービスの適合性に関する是認、サード・パーティ製品またはサービスの是認の表明を意味するものではありません。

### 9.1.2 Development Support

With an input operating voltage from 3V to 36V and rated output current up to 6A, the TLVM1440x family of synchronous buck power modules provides flexibility, scalability and optimized design size for a range of applications. These modules enable DC/DC designs with high density, low EMI, and increased flexibility. Available EMI mitigation features include integrated input bypass capacitors.

**表 9-1. Synchronous Buck DC/DC Power Module Family**

| DC/DC MODULE | RATED $I_{OUT}$ | PACKAGE | DIMENSIONS | FEATURES | EMI MITIGATION |
|---|---|---|---|---|---|
| TLVM14404 | 4A | B3QFN (28) | 6.5mm × 7.0mm × 4mm | RT adjustable $F_{SW}$, PGOOD | integrated input and BOOT capacitors |
| TLVM14406 | 6A | | | | |

For development support see the following:

- For TI's reference design library, visit the *TI Reference Design library* .
- For TI's WEBENCH Design Environment, visit the *WEBENCH® Design Center* .
- To design a low-EMI power supply, review TI's comprehensive *EMI Training Series* .
- To design an inverting buck-boost (IBB) regulator, visit *DC/DC inverting buck-boost modules* .
- TI Reference Designs:
  - *Multiple Output Power Solution For Kintex 7 Application*
  - *Arria V Power Reference Design*
  - *Altera Cyclone V SoC Power Supply Reference Design*
  - *Space-optimized DC/DC Inverting Power Module Reference Design With Minimal BOM Count*
  - *3- To 11.5-$V_{IN}$, −5-$V_{OUT}$, 1.5-A Inverting Power Module Reference Design For Small, Low-noise Systems*
- Technical Articles:
  - *Powering Medical Imaging Applications With DC/DC Buck Converters*
  - *How To Create A Programmable Output Inverting Buck-boost Regulator*

#### 9.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TLVM1440x module with WEBENCH® Power Designer.

1. Start by entering the input voltage ($V_{IN}$), output voltage ($V_{OUT}$), and output current ($I_{OUT}$) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance.
- Run thermal simulations to understand board thermal performance.
- Export customized schematic and layout into popular CAD formats.
- Print PDF reports for the design, and share the design with colleagues.

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

## 9.2 Documentation Support

### 9.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Quick Reference Guide to TI Buck Switching DC/DC Application Notes* compilation of application notes
- Texas Instruments, *Innovative DC/DC Power Modules* selection guide
- Texas Instruments, *Enabling Small, Cool and Quiet Power Modules with Enhanced HotRod™ QFN Package Technology* white paper
- Texas Instruments, *Benefits and Trade-offs of Various Power-Module Package Options* white paper
- Texas Instruments, *Simplify Low EMI Design with Power Modules* white paper
- Texas Instruments, *Power Modules for Lab Instrumentation* white paper
- Texas Instruments, *An Engineer's Guide To EMI In DC/DC Regulators* e-book
- Texas Instruments, *Soldering Considerations for Power Modules* application note
- Texas Instruments, *Practical Thermal Design With DC/DC Power Modules* application note
- Texas Instruments, *Using New Thermal Metrics* application note
- Texas Instruments, *AN-2020 Thermal Design By Insight, Not Hindsight* application note
- Texas Instruments, *Using the TPSM53602/3/4 for Negative Output Inverting Buck-Boost Applications* application note

## 9.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

## 9.4 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

## 9.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

## 10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| DATE | REVISION | NOTES |
|------|----------|-------|
| July 2024 | * | Initial Release |

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: *TLVM14404 TLVM14406*

English Data Sheet: SLVSHP0

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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TLVM14404RCHR | Active | Production | QFN-FCMOD (RCH) \| 28 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 14404 |
| TLVM14404RCHR.A | Active | Production | QFN-FCMOD (RCH) \| 28 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 14404 |
| TLVM14406RCHR | Active | Production | QFN-FCMOD (RCH) \| 28 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 14406 |
| TLVM14406RCHR.A | Active | Production | QFN-FCMOD (RCH) \| 28 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 14406 |

**(1)** **Status:** For more details on status, see our product life cycle.

**(2)** **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

**(3)** **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

**(4)** **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**(5)** **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6)** **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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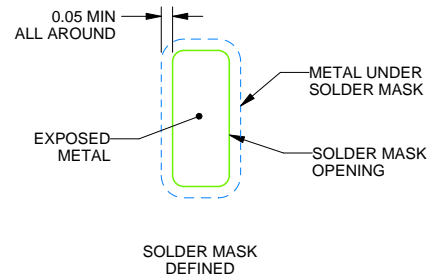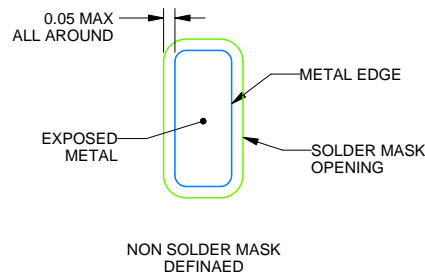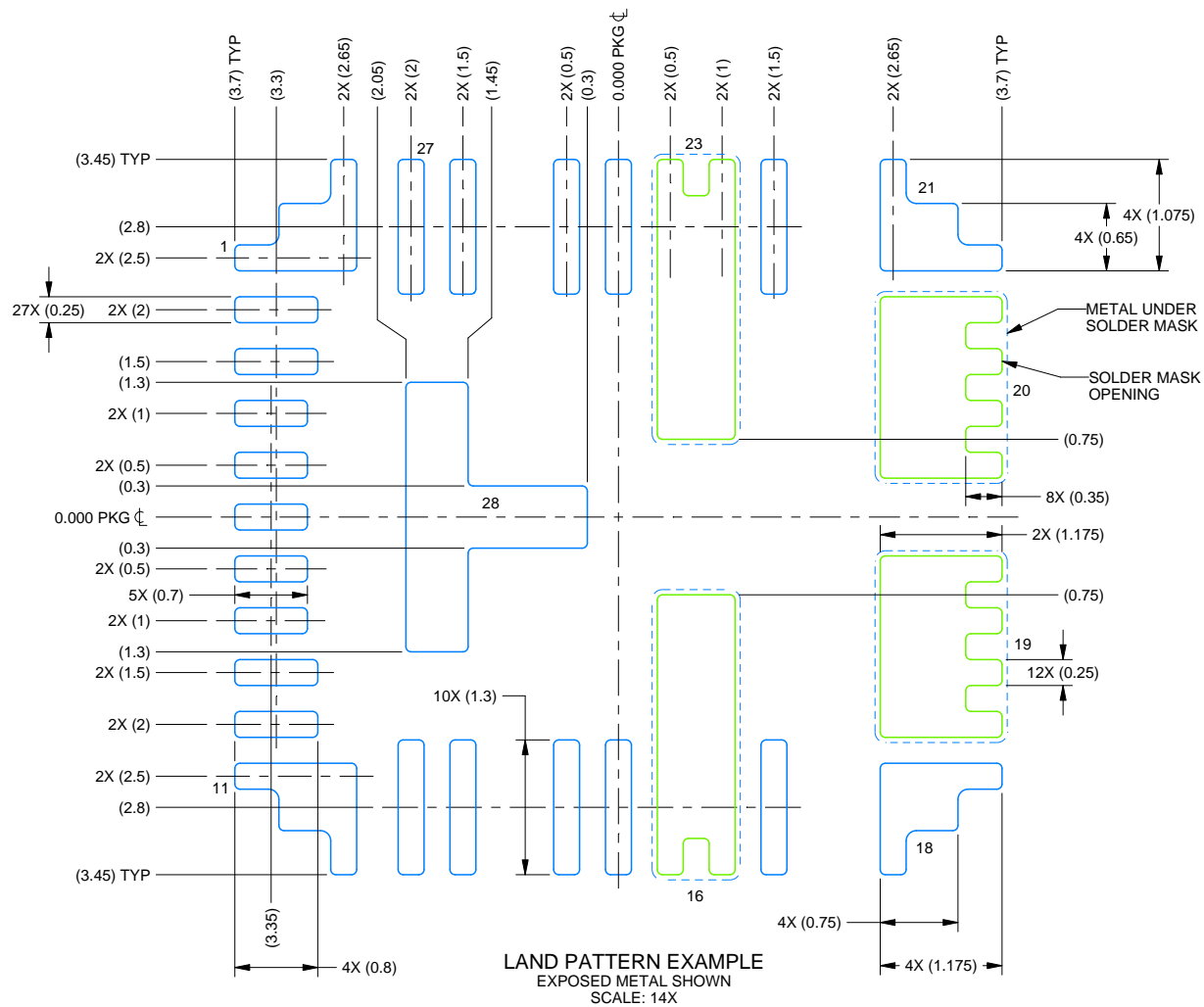
4229068/B   02/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

## RCH0028B

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 14X

METAL UNDER SOLDER MASK

SOLDER MASK OPENING

0.05 MAX
ALL AROUND

METAL EDGE

EXPOSED
METAL

SOLDER MASK
OPENING

NON SOLDER MASK
DEFINAED

0.05 MIN
ALL AROUND

METAL UNDER
SOLDER MASK

EXPOSED
METAL

SOLDER MASK
OPENING

SOLDER MASK
DEFINED

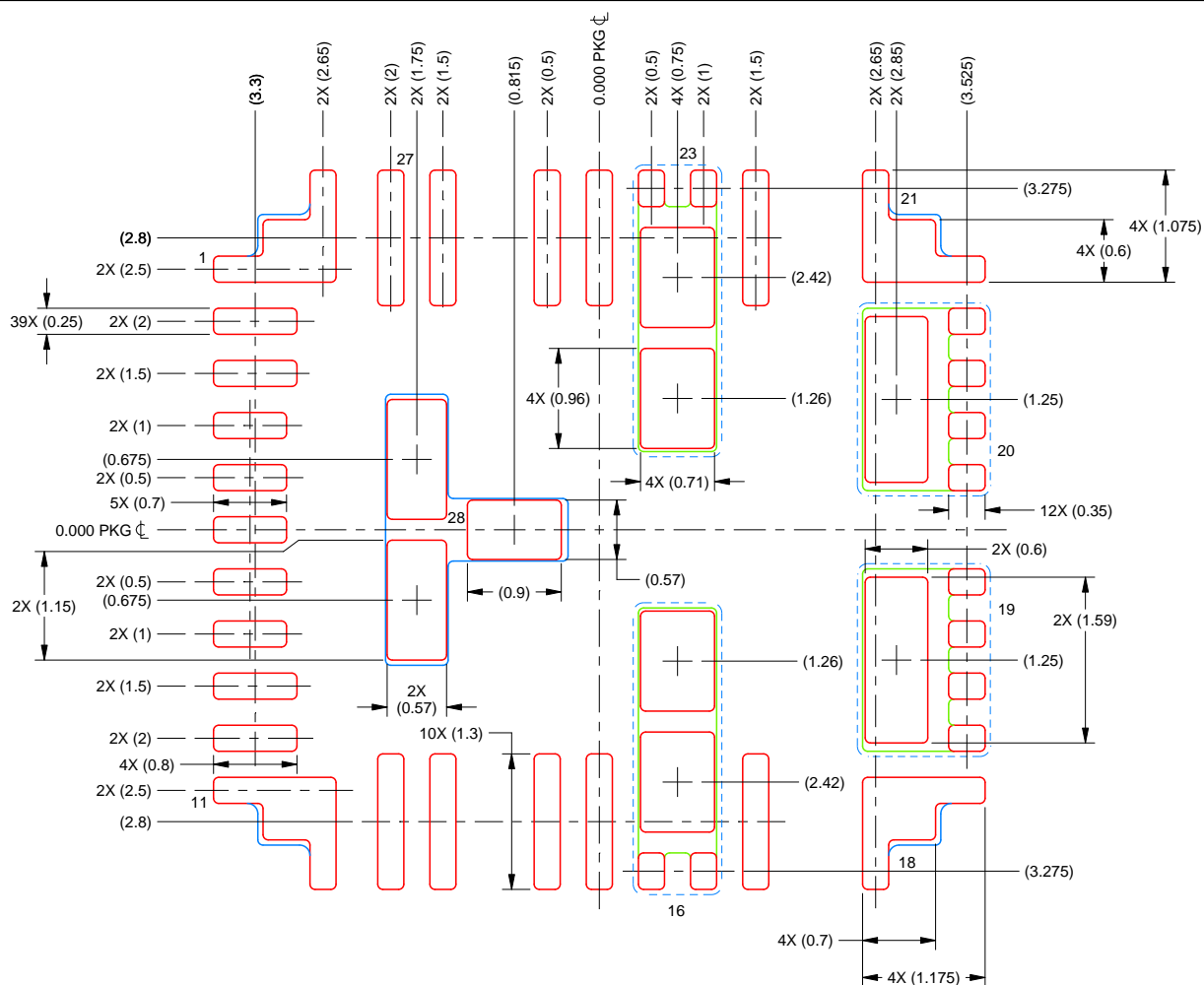SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature
   number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown
   on this view. It is recommended that vias under paste be filled, plugged or tented.

SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 14X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 1, 11, 18 & 21: 94%
PADS 16 & 23: 80%
PADS 19 & 20: 73%
PAD 28: 81%

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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