

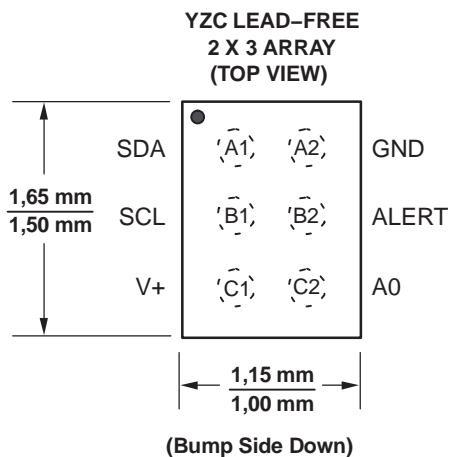
Digital Temperature Sensor with Two-Wire Interface

FEATURES

- TWO ADDRESSES
- DIGITAL OUTPUT: Two-Wire Serial Interface
- RESOLUTION: 9- to 12-Bits, User-Selectable
- ACCURACY:
 $\pm 2.0^{\circ}\text{C}$ (max) from -25°C to $+85^{\circ}\text{C}$
 $\pm 3.0^{\circ}\text{C}$ (max) from -40°C to $+125^{\circ}\text{C}$
- LOW QUIESCENT CURRENT:
 $50\mu\text{A}$, $0.1\mu\text{A}$ Standby
- NO POWER-UP SEQUENCE REQUIRED, I²C PULLUPS CAN BE ENABLED PRIOR TO V⁺

APPLICATIONS

- NOTEBOOK COMPUTERS
- COMPUTER PERIPHERAL THERMAL PROTECTION
- CELL PHONES
- BATTERY MANAGEMENT
- THERMOSTAT CONTROLS
- ENVIRONMENTAL MONITORING AND HVAC



Note: Pin A1 is marked with a '0' for Pb-free (Y2Z)

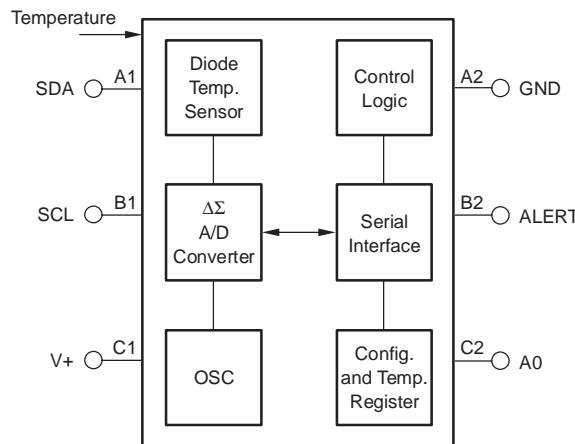
DESCRIPTION

The TMP106 is a two-wire, serial output temperature sensor available in a WCSP package. Requiring no external components, the TMP106 is capable of reading temperatures with a resolution of 0.0625°C .

The TMP106 features a Two-Wire interface that is SMBus-compatible, with the TMP106 allowing up to two devices on one bus. The TMP106 also features an SMBus Alert function.

The TMP106 is ideal for extended temperature measurement in a variety of communication, computer, consumer, environmental, industrial, and instrumentation applications.

The TMP106 is specified for operation over a temperature range of -40°C to $+125^{\circ}\text{C}$.



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ABSOLUTE MAXIMUM RATINGS(1)

| | |
|---|-----------------|
| Power Supply, V+ | 7.0V |
| Input Voltage(2) | -0.5V to 7.0V |
| Input Current | 10mA |
| Operating Temperature Range | -55°C to +127°C |
| Storage Temperature Range | -60°C to +130°C |
| Junction Temperature (T _J max) | +150°C |
| ESD Rating(3): | |
| Human Body Model (HBM) | 2000V |
| Charged-Device Model (CDM) | 500V |
| Machine Model (MM) | 200V |

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

(2) Input voltage rating applies to all TMP106 input voltages.

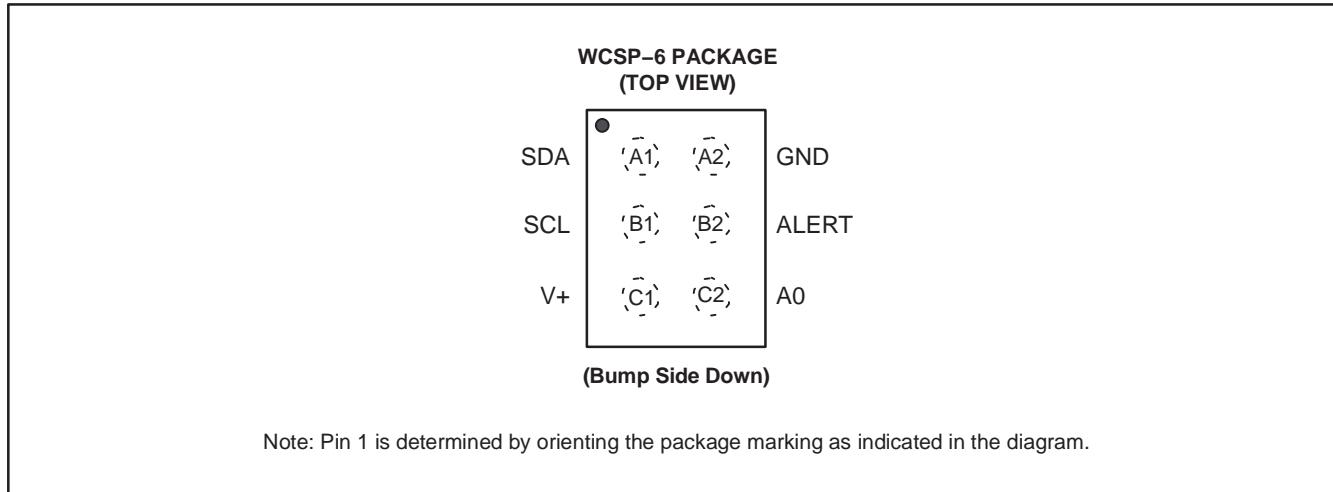
(3) ESD testing has been tested to TI specifications JEDEC J-Std 020.

ORDERING INFORMATION(1)

| PACKAGE | PART NUMBER | SYMBOL |
|--------------------------------|-------------|--------|
| Wafer chip-scale package (YZC) | TMP106YZC | F7 |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

PIN ASSIGNMENTS



ELECTRICAL CHARACTERISTICS

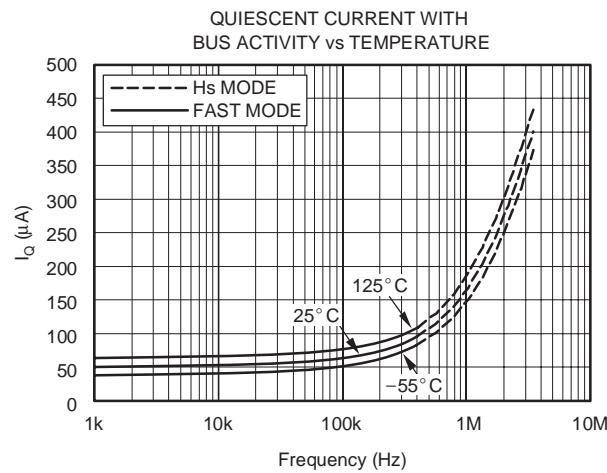
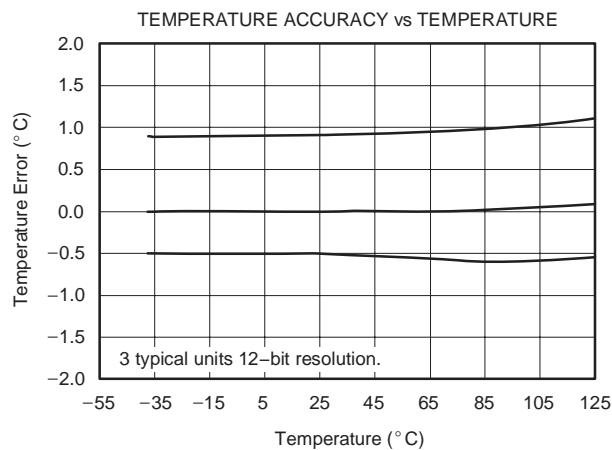
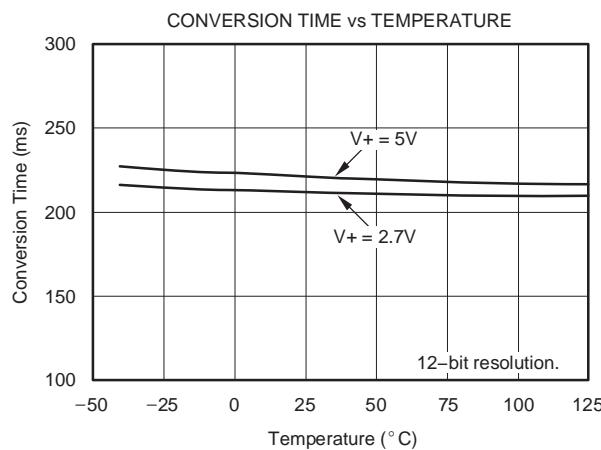
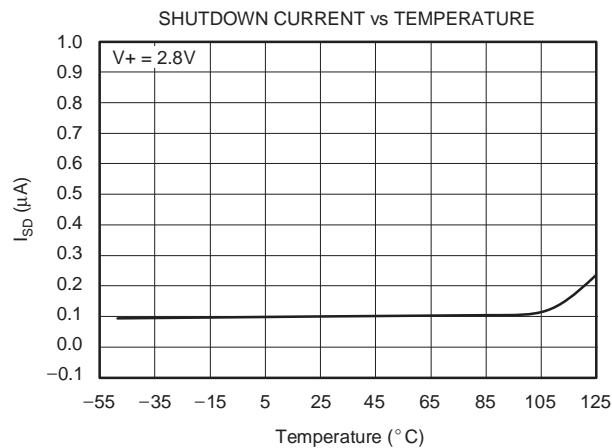
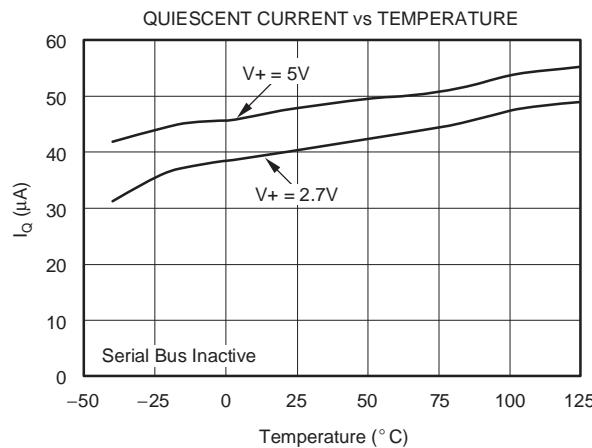
 At $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, and $V_+ = 2.7\text{V}$ to 5.5V , unless otherwise noted.

| PARAMETER | CONDITION | TMP106 | | | UNITS |
|---------------------------------|--|--------|-----------|-----------|---------------------------|
| | | MIN | TYP | MAX | |
| TEMPERATURE INPUT | | | | | |
| Range | | -40 | | +125 | $^\circ\text{C}$ |
| Accuracy (Temperature Error) | -25°C to +85°C | | ± 0.5 | ± 2.0 | $^\circ\text{C}$ |
| vs Supply | -40°C to +125°C | | ± 1.0 | ± 3.0 | $^\circ\text{C}$ |
| Resolution ⁽¹⁾ | Selectable | | 0.2 | ± 0.5 | $^\circ\text{C}/\text{V}$ |
| | | | 0.0625 | | $^\circ\text{C}$ |
| DIGITAL INPUT/OUTPUT | | | | | |
| Input Capacitance | | | 3 | | pF |
| Input Logic Levels: | | | | | |
| V_{IH} | | 2.1 | | 6.0 | V |
| V_{IL} | | -0.5 | | 0.8 | V |
| Leakage Input Current, I_{IN} | $0\text{V} \leq V_{IN} \leq 6\text{V}$ | | | 1 | μA |
| Input Voltage Hysteresis | SCL and SDA Pins | | 250 | | mV |
| Output Logic Levels: | | | | | |
| V_{OL} SDA | $I_{OL} = 3\text{mA}$ | 0 | 0.15 | 0.4 | V |
| V_{OL} ALERT | $I_{OL} = 4\text{mA}$ | 0 | 0.15 | 0.4 | V |
| Resolution | Selectable | | 9 to 12 | | Bits |
| Conversion Time | 9-Bit | | 27.5 | 37.5 | ms |
| | 10-Bit | | 55 | 75 | ms |
| | 11-Bit | | 110 | 150 | ms |
| | 12-Bit | | 220 | 300 | ms |
| Timeout Time | | 25 | 54 | 74 | ms |
| POWER SUPPLY | | | | | |
| Operating Range | | 2.7 | | 5.5 | V |
| Quiescent Current | I_Q | | 50 | 85 | μA |
| | Serial Bus Inactive | | 100 | | μA |
| | Serial Bus Active, SCL Freq = 400kHz | | 410 | | μA |
| | Serial Bus Active, SCL Freq = 3.4MHz | | 0.1 | 3 | μA |
| Shutdown Current | I_{SD} | | 60 | | μA |
| | Serial Bus Inactive | | 380 | | μA |
| | Serial Bus Active, SCL Freq = 400kHz | | | | |
| | Serial Bus Active, SCL Freq = 3.4MHz | | | | |
| TEMPERATURE RANGE | | | | | |
| Specified Range | | -40 | | +125 | $^\circ\text{C}$ |
| Operating Range | | -55 | | +127 | $^\circ\text{C}$ |
| Thermal Resistance | θ_{JA} | | 240 | | $^\circ\text{C}/\text{W}$ |

(1) Specified for 12-bit resolution.

TYPICAL CHARACTERISTICS

At $T_A = +25^\circ\text{C}$ and $V+ = 5.0\text{V}$, unless otherwise noted.



APPLICATIONS INFORMATION

The TMP106 is a digital temperature sensor that is optimal for thermal management and thermal protection applications. The TMP106 is Two-Wire and SMBus interface-compatible, and is specified over a temperature range of -40°C to $+125^{\circ}\text{C}$.

The TMP106 requires no external components for operation except for pull-up resistors on SCL, SDA, and ALERT, although a $0.1\mu\text{F}$ bypass capacitor is recommended, as shown in Figure 1.

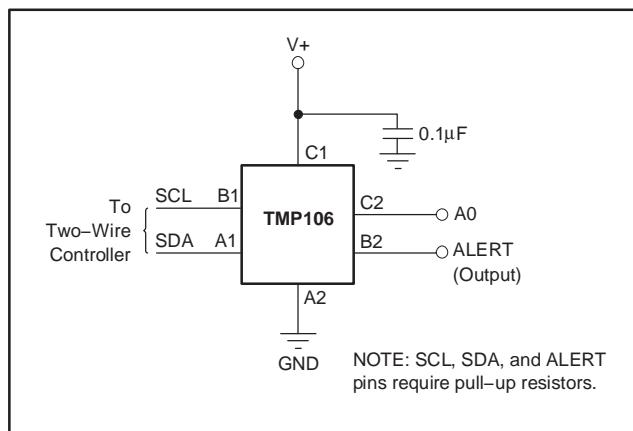


Figure 1. Typical Connections of the TMP106

The sensing device of the TMP106 is the chip itself. Thermal paths run through the package leads. The lower thermal resistance of metal causes the leads to provide the primary thermal path.

To maintain accuracy in applications requiring air or surface temperature measurement, care should be taken to isolate the package and leads from ambient air temperature.

POINTER REGISTER

Figure 2 shows the internal register structure of the TMP106. The 8-bit Pointer Register of the device is used to address a given data register. The Pointer Register uses the two LSBs to identify which of the data registers should respond to a read or write command. Table 1 identifies the bits of the Pointer Register byte. Table 2 describes the pointer address of the registers available in the TMP106. Power-up reset value of P1/P0 is 00.

| P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
|----|----|----|----|----|----|---------------|----|
| 0 | 0 | 0 | 0 | 0 | 0 | Register Bits | |

Table 1. Pointer Register Byte

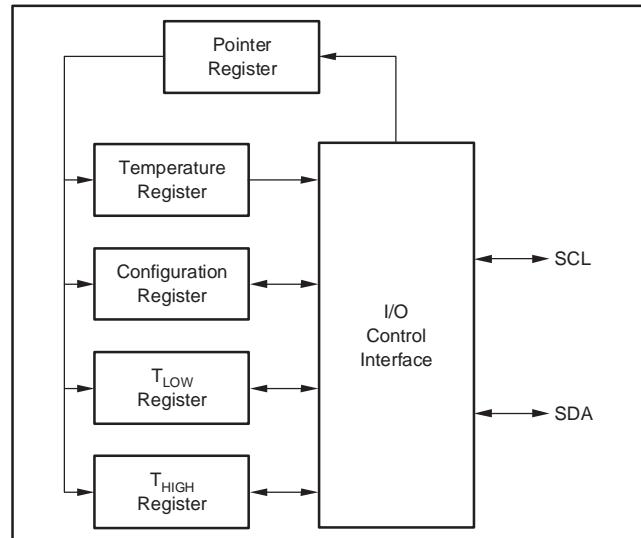


Figure 2. Internal Register Structure of the TMP106

| P1 | P0 | REGISTER |
|----|----|---|
| 0 | 0 | Temperature Register (Read Only) |
| 0 | 1 | Configuration Register (Read/Write) |
| 1 | 0 | T _{LOW} Register (Read/Write) |
| 1 | 1 | T _{HIGH} Register (Read/Write) |

Table 2. Pointer Addresses of the TMP106

TEMPERATURE REGISTER

The Temperature Register of the TMP106 is a 12-bit, read-only register that stores the output of the most recent conversion. Two bytes must be read to obtain data, and are described in Table 3 and Table 4. Note that byte 1 is the most significant byte; byte 2 is the least significant byte. The first 12 bits are used to indicate temperature, with all remaining bits equal to zero. The least significant byte does not have to be read if that information is not needed. Data format for temperature is summarized in Table 5. Following power-up or reset, the Temperature Register will read 0°C until the first conversion is complete.

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|-----|----|----|----|----|----|----|
| T11 | T10 | T9 | T8 | T7 | T6 | T5 | T4 |

Table 3. Byte 1 of Temperature Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| T3 | T2 | T1 | T0 | 0 | 0 | 0 | 0 |

Table 4. Byte 2 of Temperature Register

| TEMPERATURE (°C) | DIGITAL OUTPUT (BINARY) | HEX |
|---------------------|----------------------------|-----|
| 128 | 0111 1111 1111 | 7FF |
| 127.9375 | 0111 1111 1111 | 7FF |
| 100 | 0110 0100 0000 | 640 |
| 80 | 0101 0000 0000 | 500 |
| 75 | 0100 1011 0000 | 4B0 |
| 50 | 0011 0010 0000 | 320 |
| 25 | 0001 1001 0000 | 190 |
| 0.25 | 0000 0000 0100 | 004 |
| 0 | 0000 0000 0000 | 000 |
| -0.25 | 1111 1111 1100 | FFC |
| -25 | 1110 0111 0000 | E70 |
| -55 | 1100 1001 0000 | C90 |

Table 5. Temperature Data Format

The user can obtain 9, 10, 11, or 12 bits of resolution by addressing the Configuration Register and setting the resolution bits accordingly. For 9-, 10-, or 11-bit resolution, the most significant bits in the Temperature Register are used with the unused LSBs set to zero.

CONFIGURATION REGISTER

The Configuration Register is an 8-bit read/write register used to store bits that control the operational modes of the temperature sensor. Read/write operations are performed MSB first. The format of the Configuration Register for the TMP106 is shown in Table 6, followed by a breakdown of the register bits. The power-up/reset value of the Configuration Register is all bits equal to 0.

| BYTE | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----|----|----|----|----|-----|----|----|
| 1 | OS | R1 | R0 | F1 | F0 | POL | TM | SD |

Table 6. Configuration Register Format

SHUTDOWN MODE (SD)

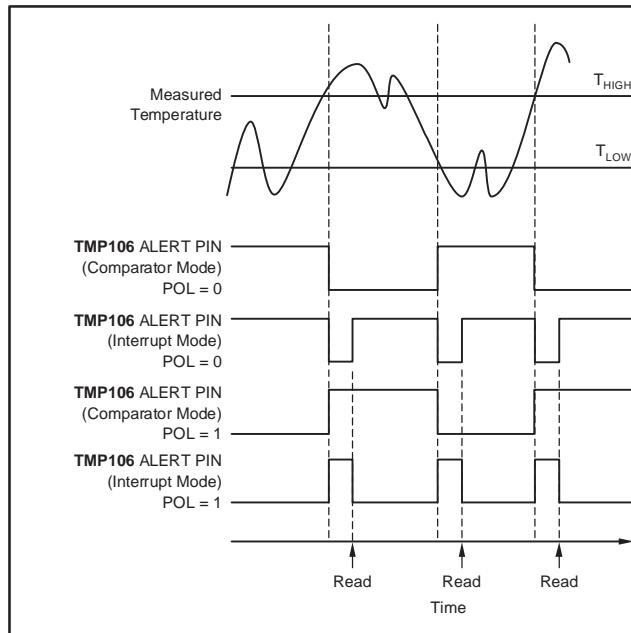
The Shutdown Mode of the TMP106 allows the user to save maximum power by shutting down all device circuitry other than the serial interface, which reduces current consumption to typically less than 0.1 μ A. Shutdown Mode is enabled when the SD bit is 1; the device will shut down once the current conversion is completed. When SD is equal to 0, the device will maintain a continuous conversion state.

THERMOSTAT MODE (TM)

The Thermostat Mode bit of the TMP106 indicates to the device whether to operate in Comparator Mode (TM = 0) or Interrupt Mode (TM = 1). For more information on comparator and interrupt modes, see the *High and Low Limit Registers* section.

POLARITY (POL)

The Polarity Bit of the TMP106 allows the user to adjust the polarity of the ALERT pin output. If POL = 0, the ALERT pin will be active LOW, as shown in Figure 3. For POL = 1, the ALERT pin will be active HIGH, and the state of the ALERT pin is inverted.

**Figure 3. Output Transfer Function Diagrams**

FAULT QUEUE (F1/F0)

A fault condition is defined as when the measured temperature exceeds the user-defined limits set in the T_{HIGH} and T_{LOW} Registers. Additionally, the number of fault conditions required to generate an alert may be programmed using the fault queue. The fault queue is provided to prevent a false alert as a result of environmental noise. The fault queue requires consecutive fault measurements in order to trigger the alert function. Table 7 defines the number of measured faults that may be programmed to trigger an alert condition in the device. For T_{HIGH} and T_{LOW} register format and byte order, see the *High and Low Limit Registers* section.

| F1 | F0 | CONSECUTIVE FAULTS |
|----|----|--------------------|
| 0 | 0 | 1 |
| 0 | 1 | 2 |
| 1 | 0 | 4 |
| 1 | 1 | 6 |

Table 7. Fault Settings of the TMP106

CONVERTER RESOLUTION (R1/R0)

The Converter Resolution bits control the resolution of the internal analog-to-digital (A/D) converter. This control allows the user to maximize efficiency by programming for higher resolution or faster conversion time. Table 8 identifies the resolution bits and the relationship between resolution and conversion time.

| R1 | R0 | RESOLUTION | CONVERSION TIME (typical) |
|----|----|--------------------|------------------------------|
| 0 | 0 | 9 Bits (0.5°C) | 27.5ms |
| 0 | 1 | 10 Bits (0.25°C) | 55ms |
| 1 | 0 | 11 Bits (0.125°C) | 110ms |
| 1 | 1 | 12 Bits (0.0625°C) | 220ms |

Table 8. Resolution of the TMP106

ONE-SHOT (OS)

The TMP106 features a One-Shot Temperature Measurement Mode. When the device is in Shutdown Mode, writing a '1' to the OS bit starts a single temperature conversion. The device will return to the shutdown state at the completion of the single conversion. This option is useful to reduce power consumption in the TMP106 when continuous temperature monitoring is not required. When the Configuration Register is read, the OS always reads zero.

HIGH AND LOW LIMIT REGISTERS

In Comparator Mode (TM = 0), the ALERT pin of the TMP106 becomes active when the temperature equals or exceeds the value in T_{HIGH} and generates a consecutive number of faults according to fault bits F1 and F0. The ALERT pin remains active until the temperature falls below the indicated T_{LOW} value for the same number of faults.

In Interrupt Mode (TM = 1), the ALERT pin becomes active when the temperature equals or exceeds T_{HIGH} for a consecutive number of fault conditions. The ALERT pin remains active until a read operation of any register occurs, or until the device successfully responds to the SMBus Alert Response address. The ALERT pin clears if the device is placed in Shutdown Mode. Once the ALERT pin is cleared, it will only become active again by the temperature falling below T_{LOW} . When the temperature falls below T_{LOW} , the ALERT pin becomes active and remains active until cleared by a read operation of any register or a successful response to the SMBus Alert

Response address. When the ALERT pin clears, the above cycle will repeat, with the ALERT pin becoming active when the temperature equals or exceeds T_{HIGH} . The ALERT pin can also be cleared by resetting the device with the General Call Reset command. This reset also clears the state of the internal registers in the device, returning the device to Comparator Mode (TM = 0).

Both operational modes are represented in Figure 3. Table 9 and Table 10 describe the format for the T_{HIGH} and T_{LOW} Registers. Note that the most significant byte is sent first, followed by the least significant byte. Power-up reset values for T_{HIGH} and T_{LOW} are:

$$T_{HIGH} = 80^{\circ}\text{C} \text{ and } T_{LOW} = 75^{\circ}\text{C}$$

The format of the data for T_{HIGH} and T_{LOW} is the same as for the Temperature Register.

| BYTE | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----|-----|----|----|----|----|----|----|
| 1 | H11 | H10 | H9 | H8 | H7 | H6 | H5 | H4 |
| BYTE | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 2 | H3 | H2 | H1 | H0 | 0 | 0 | 0 | 0 |

Table 9. Bytes 1 and 2 of T_{HIGH} Register

| BYTE | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----|-----|----|----|----|----|----|----|
| 1 | L11 | L10 | L9 | L8 | L7 | L6 | L5 | L4 |
| BYTE | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 2 | L3 | L2 | L1 | L0 | 0 | 0 | 0 | 0 |

Table 10. Bytes 1 and 2 of T_{LOW} Register

All 12 bits for the Temperature, T_{HIGH} , and T_{LOW} Registers are used in the comparisons for the ALERT function for all converter resolutions. The three LSBs in T_{HIGH} and T_{LOW} can affect the ALERT output even if the converter is configured for 9-bit resolution.

SERIAL INTERFACE

The TMP106 operates only as a slave device on the Two-Wire bus and SMBus. Connections to the bus are made via the open-drain I/O lines SDA and SCL. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The TMP106 supports the transmission protocol for fast (1kHz to 400kHz) and high-speed (1kHz to 3.4MHz) modes. All data bytes are transmitted MSB first.

SERIAL BUS ADDRESS

To communicate with the TMP106, the master must first address slave devices via a slave address byte. The slave address byte consists of seven address bits, and a direction bit indicating the intent of executing a read or write operation.

The TMP106 features one address pin allowing up to two devices to be connected per bus. Pin logic levels are described in Table 11. The address pin of the TMP106 is read after reset, at start of communication, or in response to a Two-Wire address acquire request. Following the reading of the pin state, the address is latched to minimize power dissipation associated with detection.

| A0 | SLAVE ADDRESS |
|----|---------------|
| 0 | 1001000 |
| 1 | 1001001 |

Table 11. Address Pin and Slave Addresses for the TMP106

BUS OVERVIEW

The device that initiates the transfer is called a *master*, and the devices controlled by the master are *slaves*. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device, a START condition is initiated, indicated by pulling the data-line (SDA) from a HIGH to LOW logic level while SCL is HIGH. All slaves on the bus shift in the slave address byte, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an Acknowledge and pulling SDA LOW.

Data transfer is then initiated and sent over eight clock pulses followed by an Acknowledge Bit. During data transfer SDA must remain stable while SCL is HIGH, as any change in SDA while SCL is HIGH will be interpreted as a control signal.

Once all data has been transferred, the master generates a STOP condition, indicated by pulling SDA from LOW to HIGH while SCL is HIGH.

WRITING/READING TO THE TMP106

Accessing a particular register on the TMP106 is accomplished by writing the appropriate value to the Pointer Register. The value for the Pointer Register is the first byte transferred after the slave address byte with the R/W bit LOW. Every write operation to the TMP106 requires a value for the Pointer Register. (Refer to Figure 5.)

When reading from the TMP106, the last value stored in the Pointer Register by a write operation is used to determine which register is read by a read operation. To change the register pointer for a read operation, a new value must be written to the Pointer Register. This is accomplished by issuing a slave address byte with the R/W bit LOW, followed by the Pointer Register byte. No additional data are required. The master can then generate a START condition and send the slave address byte with the R/W bit HIGH to initiate the read command. See Figure 6 for details of this sequence. If repeated reads from the same register are desired, it is not necessary to continually send the Pointer Register byte, as the TMP106 remembers the Pointer Register value until it is changed by the next write operation.

Note that register bytes are sent most-significant byte first, followed by the least-significant byte.

SLAVE MODE OPERATIONS

The TMP106 can operate as a slave receiver or slave transmitter.

Slave Receiver Mode:

The first byte transmitted by the master is the slave address, with the R/W bit LOW. The TMP106 then acknowledges reception of a valid address. The next byte transmitted by the master is the Pointer Register. The TMP106 then acknowledges reception of the Pointer Register byte. The next byte or bytes are written to the register addressed by the Pointer Register. The TMP106 acknowledges reception of each data byte. The master may terminate data transfer by generating a START or STOP condition.

Slave Transmitter Mode:

The first byte is transmitted by the master and is the slave address, with the R/W bit HIGH. The slave acknowledges reception of a valid slave address. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the Pointer Register. The master acknowledges reception of the data byte. The next byte transmitted by the slave is the least significant byte. The master acknowledges reception of the data byte. The master may terminate data transfer by generating a Not-Acknowledge on reception of any data byte, or generating a START or STOP condition.

SMBus ALERT FUNCTION

The TMP106 supports the SMBus Alert function. When the TMP106 is operating in Interrupt Mode (TM = 1), the ALERT pin of the TMP106 may be connected as an SMBus Alert signal. When a master senses that an ALERT condition is present on the ALERT line, the master sends an SMBus Alert command (00011001) on the bus. If the ALERT pin of the TMP106 is active, the devices will acknowledge the SMBus Alert command and respond by returning its slave address on the SDA line. The eighth bit (LSB) of the slave address byte will indicate if the temperature exceeding T_{HIGH} or falling below T_{LOW} caused the ALERT condition. This bit will be HIGH if the temperature is greater than or equal to T_{HIGH} . This bit will be LOW if the temperature is less than T_{LOW} . Refer to Figure 7 for details of this sequence.

If multiple devices on the bus respond to the SMBus Alert command, arbitration during the slave address portion of the SMBus Alert command will determine which device will clear its ALERT status. If the TMP106 wins the arbitration, its ALERT pin will become inactive at the completion of the SMBus Alert command. If the TMP106 loses the arbitration, its ALERT pin will remain active.

GENERAL CALL

The TMP106 responds to a Two-Wire General Call address (00000000) if the eighth bit is 0. The device will acknowledge the General Call address and respond to commands in the second byte. If the second byte is 00000100, the TMP106 will latch the status of the address pin, but will not reset. If the second byte is 00000110, the TMP106 will latch the status of the address pin and reset the internal registers to their power-up values.

HIGH-SPEED MODE

In order for the Two-Wire bus to operate at frequencies above 400kHz, the master device must issue an Hs-mode master code (00001XXX) as the first byte after a START condition to switch the bus to high-speed operation. The TMP106 will not acknowledge this byte, but will switch its input filters on SDA and SCL and its output filters on SDA to operate in Hs-mode, allowing transfers at up to 3.4MHz. After the Hs-mode master code has been issued, the master will transmit a Two-Wire slave address to initiate a data transfer operation. The bus will continue to operate in Hs-mode until a STOP condition occurs on the bus. Upon receiving the STOP condition, the TMP106 will switch the input and output filters back to fast-mode operation.

TIMEOUT FUNCTION

The TMP106 will reset the serial interface if either SCL or SDA are held LOW for 54ms (typ) between a START and STOP condition. The TMP106 will release the bus if it is pulled LOW and will wait for a START condition. To avoid activating the timeout function, it is necessary to maintain a communication speed of at least 1kHz for SCL operating frequency.

TIMING DIAGRAMS

The TMP106 is Two-Wire- and SMBus-compatible. Figure 4 to Figure 7 describe the various operations on the TMP106. Bus definitions are given below. Parameters for Figure 4 are defined in Table 12.

Bus Idle: Both SDA and SCL lines remain HIGH.

Start Data Transfer: A change in the state of the SDA line, from HIGH to LOW, while the SCL line is HIGH, defines a START condition. Each data transfer is initiated with a START condition.

Stop Data Transfer: A change in the state of the SDA line from LOW to HIGH while the SCL line is HIGH defines a STOP condition. Each data transfer is terminated with a repeated START or STOP condition.

Data Transfer: The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the master device. The receiver acknowledges the transfer of data.

Acknowledge: Each receiving device, when addressed, is obliged to generate an Acknowledge bit. A device that acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the Acknowledge clock pulse. Setup and hold times must be taken into account. On a master receive, the termination of the data transfer can be signaled by the master generating a Not-Acknowledge on the last byte that has been transmitted by the slave.

| PARAMETER | FAST MODE | | HIGH-SPEED MODE | | UNITS |
|---|-----------|-----|-----------------|-----|-------|
| | MIN | MAX | MIN | MAX | |
| SCL Operating Frequency $f_{(SCL)}$ | 0.001 | 0.4 | 0.001 | 3.4 | MHz |
| Bus Free Time Between STOP and START Condition $t_{(BUF)}$ | 600 | | 160 | | ns |
| Hold time after repeated START condition. After this period, the first clock is generated. $t_{(HDSTA)}$ | 100 | | 100 | | ns |
| Repeated START Condition Setup Time $t_{(SUSTA)}$ | 100 | | 100 | | ns |
| STOP Condition Setup Time $t_{(SUSTO)}$ | 100 | | 100 | | ns |
| Data Hold Time $t_{(HDDAT)}$ | 0 | | 0 | | ns |
| Data Setup Time $t_{(SUDAT)}$ | 100 | | 10 | | ns |
| SCL Clock LOW Period $t_{(LOW)}$ | 1300 | | 160 | | ns |
| SCL Clock HIGH Period $t_{(HIGH)}$ | 600 | | 60 | | ns |
| Clock/Data Fall Time t_F | | 300 | | 160 | ns |
| Clock/Data Rise Time t_R for $SCLK \leq 100\text{kHz}$ | | 300 | 1000 | 160 | ns |

Table 12. Timing Diagram Definitions for the TMP106

TWO-WIRE TIMING DIAGRAMS

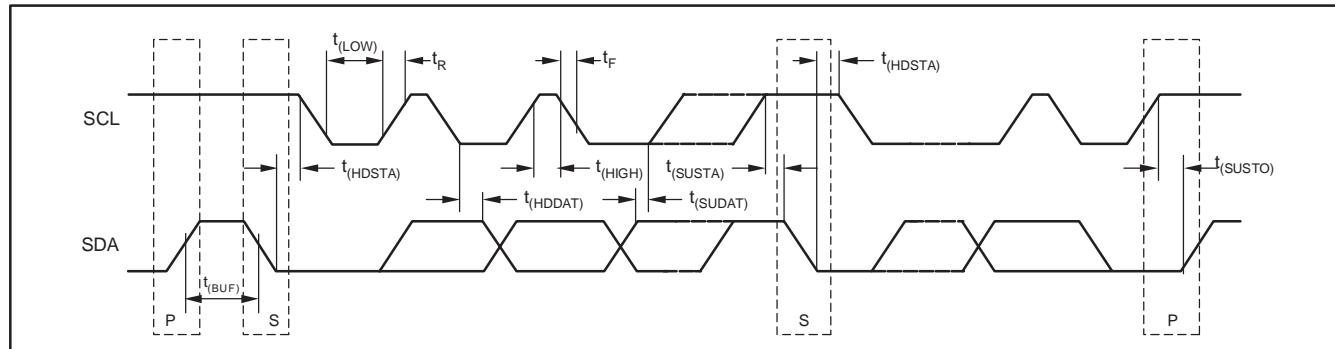


Figure 4. Two-Wire Timing Diagram

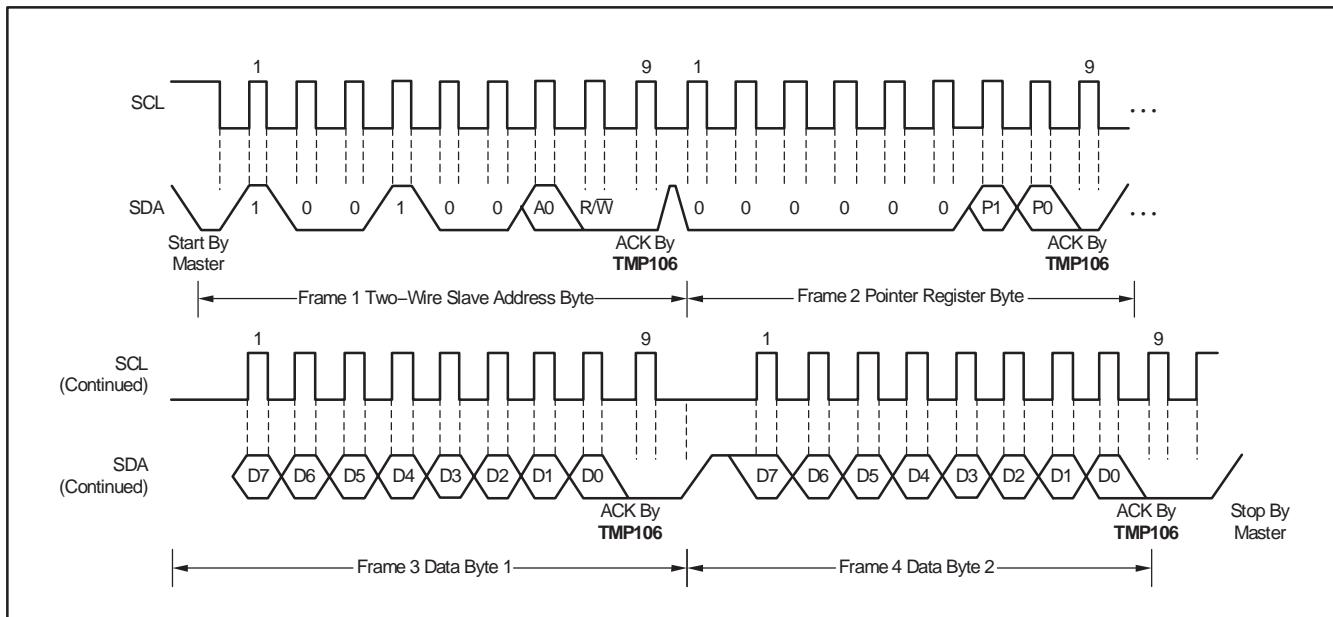


Figure 5. Two-Wire Timing Diagram for TMP106 Write Word Format

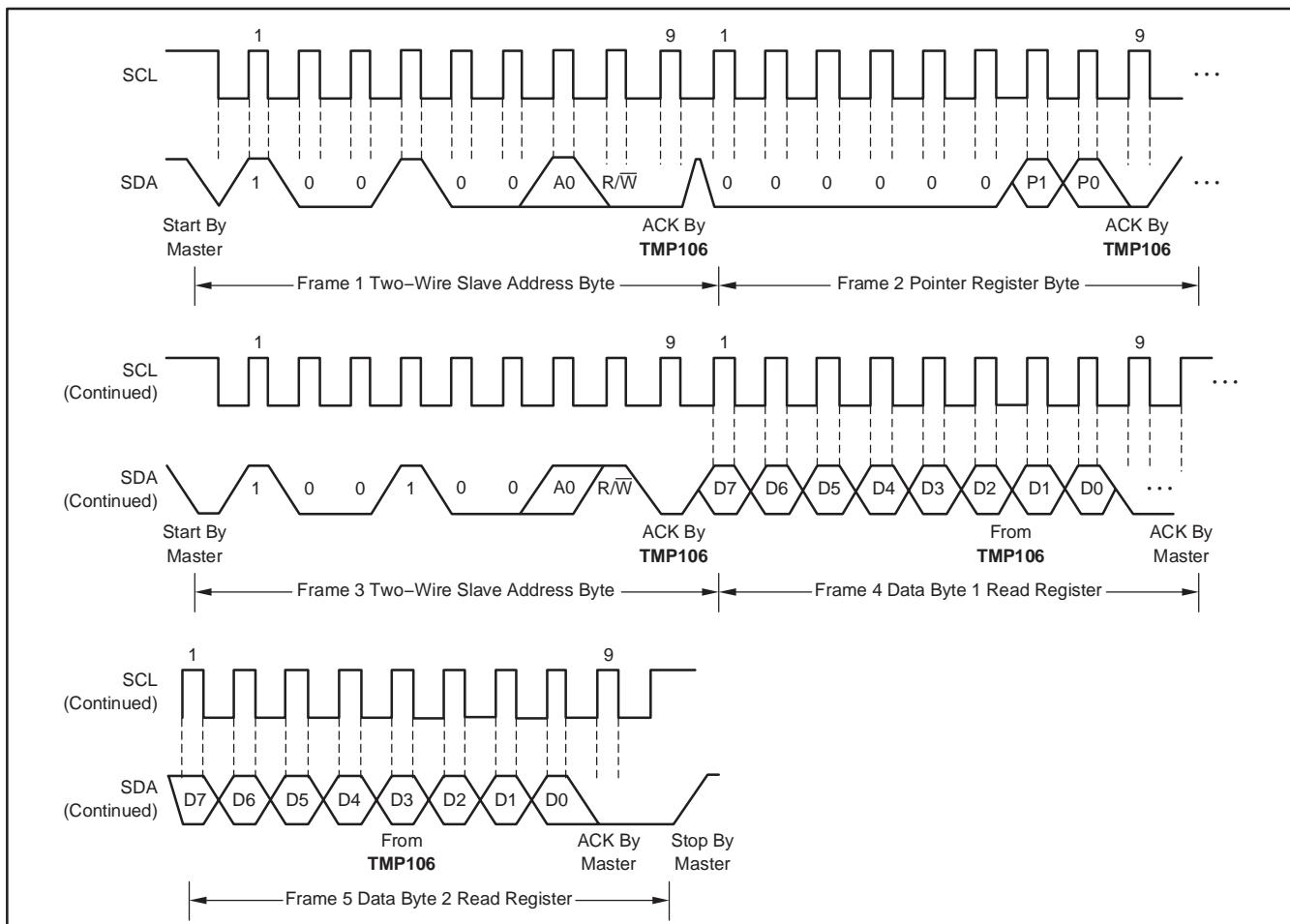


Figure 6. Two-Wire Timing Diagram for Read Word Format

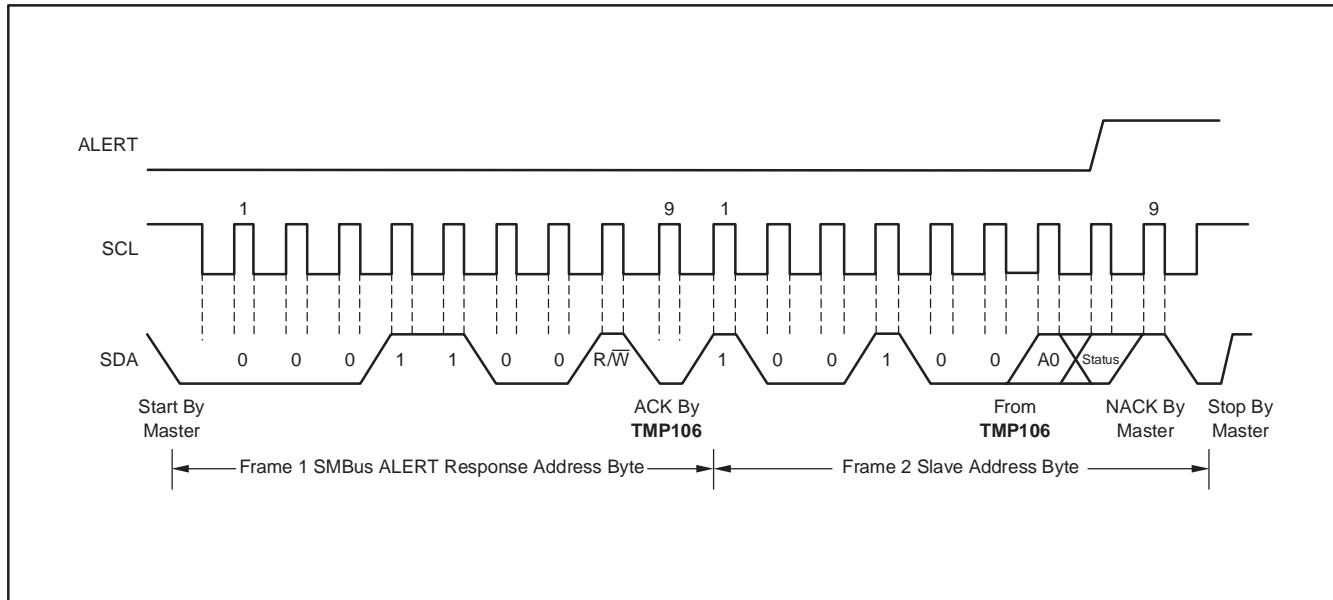
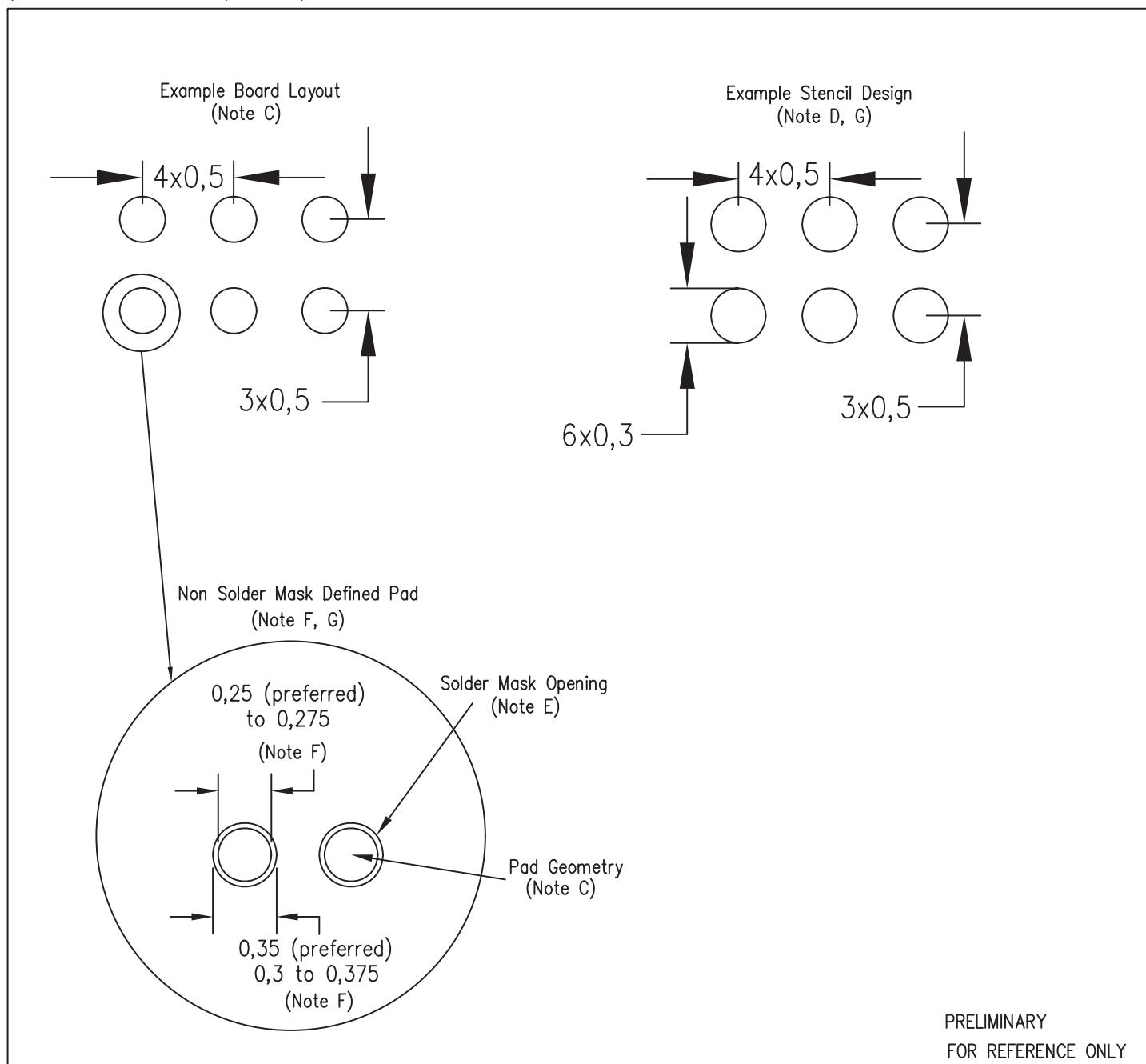


Figure 7. Timing Diagram for SMBus ALERT

YZC (S-XBGA-N6)
(Pb-Free Solder Spheres)



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
- F. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Wafer Chip Scale Packages, Texas Instruments Literature No. SBVA017 and also the Product Data Sheet for specific thermal information via requirements, and recommended routing guidelines. These documents are available at www.ti.com <<http://www.ti.com>>.
- G. Placement force during assembly must be kept below 30g per solder sphere.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| TMP106YZCR | Active | Production | DSBGA (YZC) 6 | 3000 LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | F7 |
| TMP106YZCR.B | Active | Production | DSBGA (YZC) 6 | 3000 LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | F7 |
| TMP106YZCT | Obsolete | Production | DSBGA (YZC) 6 | - | - | Call TI | Call TI | -40 to 125 | F7 |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

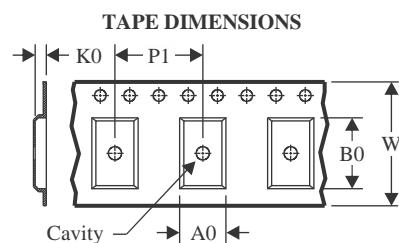
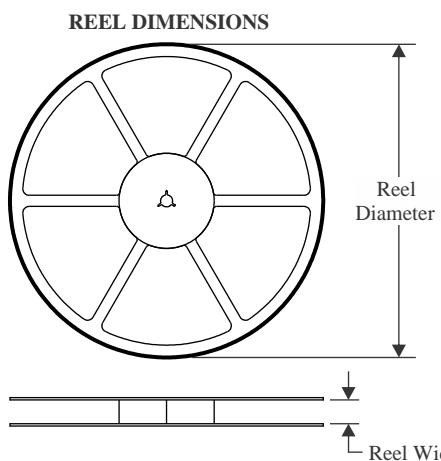
⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

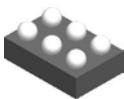

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TMP106YZCR | DSBGA | YZC | 6 | 3000 | 178.0 | 8.4 | 1.24 | 1.7 | 0.76 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TMP106YZCR | DSBGA | YZC | 6 | 3000 | 220.0 | 220.0 | 35.0 |

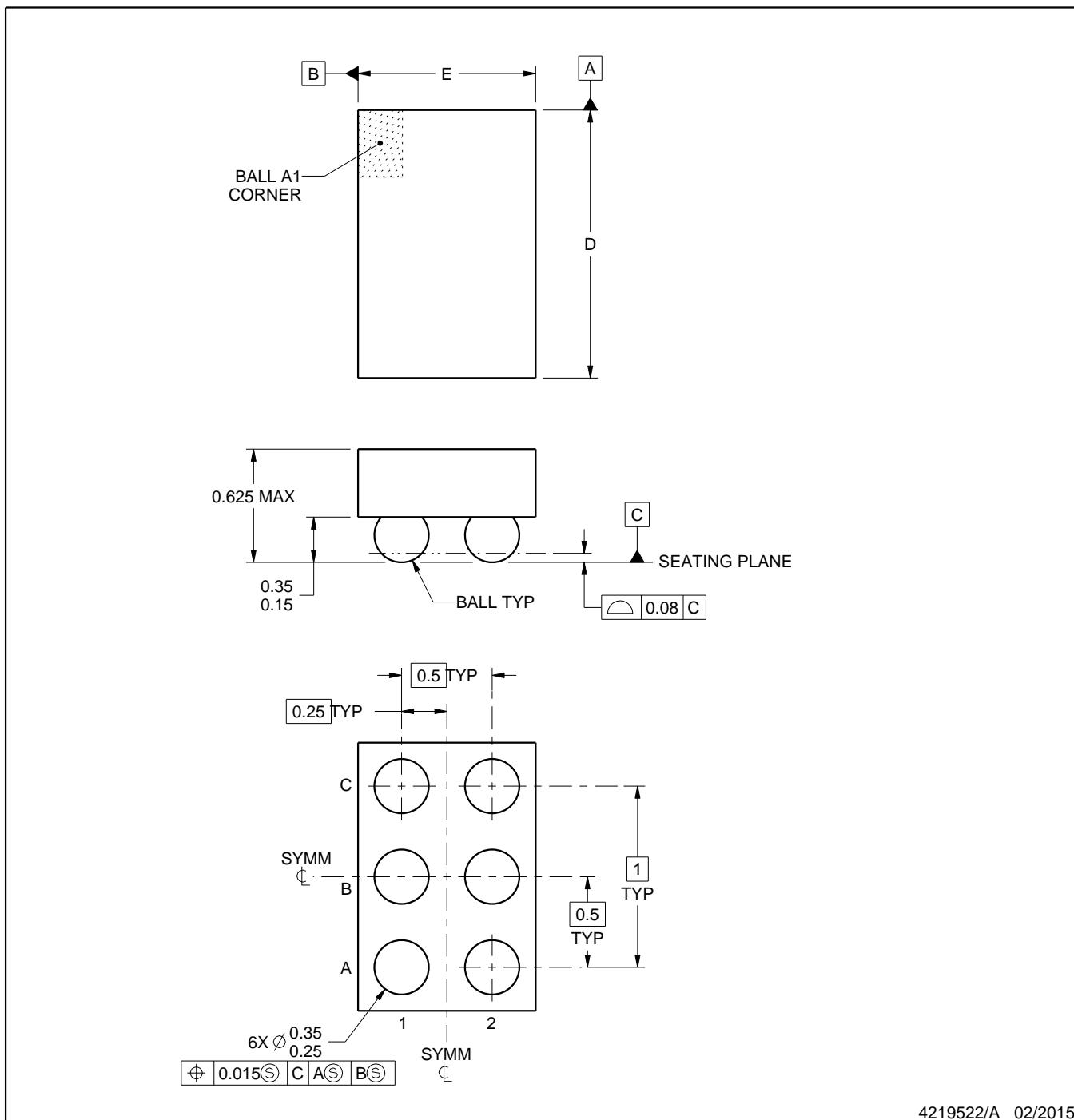


PACKAGE OUTLINE

YZC0006

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



4219522/A 02/2015

NOTES:

NanoFree is a trademark of Texas Instruments.

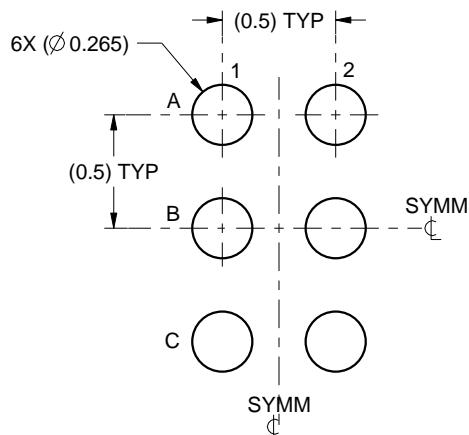
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.

EXAMPLE BOARD LAYOUT

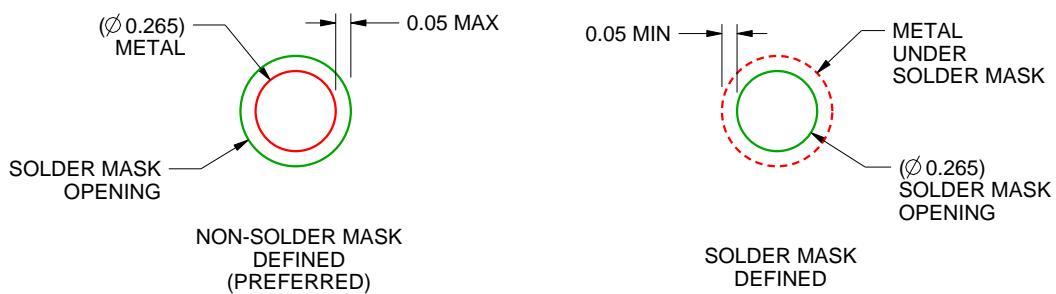
YZC0006

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

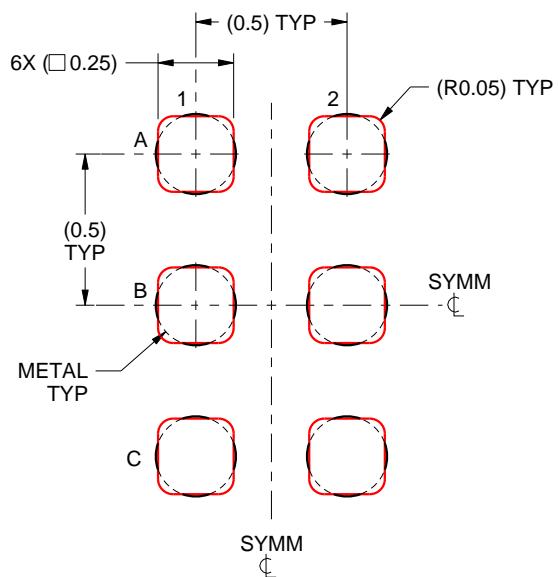
4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YZC0006

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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