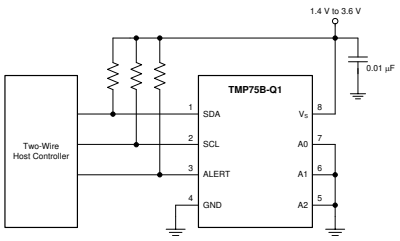
TMP75B-Q1 1.8V デジタル温度センサ、2 線式インターフェイスおよびアラート付き

1 特長

- 車載アプリケーション認定済み
- 以下の結果で AEC-Q100 認定済み:
  - 温度グレード 1:-40℃～125℃
  - HBM ESD 分類レベル 2
  - CDM ESD 分類レベル C4B
- 3 つの温度でテスト済みのオプション:
  TMP75BTQDGKRQ1
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 2 線式シリアル インターフェイス付きのデジタル出力
- ピンによりプログラム可能な 8 つまでのバス アドレス
- 過熱アラートをプログラム可能
- シャットダウン モードによる消費電力削減
- ワンショット変換モード
- 動作温度範囲:-40℃～125℃
- 動作電源電圧範囲:1.4V～3.6V
- 静止電流:
  - 45µA アクティブ (標準値)
  - 0.3µA シャットダウン (標準値)
- 精度:
  - -20℃～85℃で ±0.5℃ (標準値)
  - -40℃～125℃で ±1℃ (標準値)
- 分解能:12 ビット (0.0625℃)
- パッケージ:SOIC-8、VSSOP-8

2 アプリケーション

- 自動運転モジュール
- メディア ハブ / ディスプレイ
- ヘッド / デジタル コックピット ユニット
- スマート テレマティクス / ゲートウェイ
- ADAS ドメイン コントローラ / センサ フュージョン
- ボディ コントロール モジュール
- オンボード チャージャ
- バッテリ システム



概略回路図

3 概要

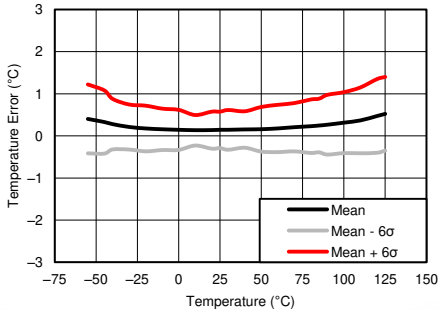
TMP75B-Q1 は、12 ビットのアナログ / デジタル コンバータ (ADC) を統合したデジタル温度センサで、1.8V の電源で動作可能であり、業界標準規格の LM75 および TMP75 とピンおよびレジスタ互換です。このデバイスは SOIC-8 および VSSOP-8 パッケージで供給され、外付け部品なしで温度を感知できます。TMP75B-Q1 は、–40°C～125°C の動作温度範囲で温度を 0.0625°C の分解能で読み取ることができます。TMP75BTQDGKRQ1 は、高い堅牢性を実現するために、生産時に 3 つの温度 (–40°C、25°C、125°C) でテストされています。

TMP75B-Q1 には SMBus および 2 線式インターフェイスとの互換性があり、8 つまでのデバイスを同じバスに接続でき、SMBus の過熱アラート機能を使用できます。プログラム可能な温度制限と ALERT ピンにより、このセンサはスタンドアロンのサーモスタット、または電源スロットルやシステム シャットダウン用の過熱アラームとして動作できます。工場で較正済みの温度精度と、ノイズ耐性のあるデジタル インターフェイスにより、TMP75B-Q1 は他のセンサーや電子部品の温度補償に適切なソリューションです。TMP75B-Q1 は、さまざまな車載アプリケーションの熱管理と保護を目的として設計されており、PCB に実装されるサーミスタに代わる高性能の代替品です。

パッケージ情報

型番	パッケージ (1)	パッケージ サイズ(2)
TMP75BQDRQ1	D (SOIC、8)	4.9mm × 6mm
TMP75BQDGKRQ1	DGK (VSSOP、8)	3mm × 4.9mm
TMP75BTQDGKRQ1		

(1) 供給されているすべてのパッケージについては、セクション 12 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



温度精度(誤差)と周囲温度との関係

Table of Contents

4 Device Comparison

表 4-1. Device Comparison

Device	Package	Production Test Condition
TMP75BQDRQ1	D (SOIC, 8 pin)	Room Temp (25°C)
TMP75BQDGKRQ1	DGK (VSSOP, 8 pin)	
TMP75BTQDGKRQ1	DGK (VSSOP, 8 pin)	Tri-temp (–40°C, 25°C, and 125°C)

5 Pin Configuration and Functions

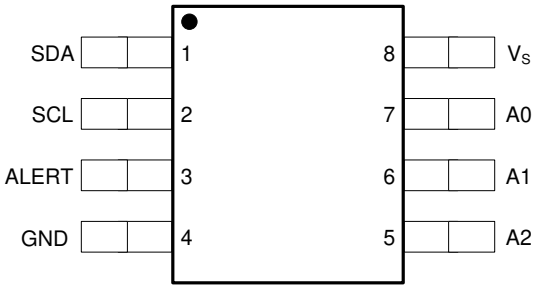


図 5-1. D and DGK Packages 8-Pin SOIC and 8-Pin VSSOP (Top View)

表 5-1. Pin Functions

PIN		Type(1)	DESCRIPTION
NAME	NO.		
A0	7	I	Address select. Connect to GND or V_S.
A1	6	I	Address select. Connect to GND or V_S.
A2	5	I	Address select. Connect to GND or V_S.
ALERT	3	O	Overtemperature alert. Open-drain output; requires a pullup resistor.
GND	4	G	Ground
SCL	2	I	Serial clock
SDA	1	I/O	Serial data. Open-drain output; requires a pullup resistor.
V_S	8	I	Supply voltage, 1.4V to 3.6V

(1) I = input, O = output, I/O = input or output, and G = ground

6 Specifications

6.1 Absolute Maximum Ratings

Over free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage			4	V
$V_{I/O}$	I/O voltage	SDA, SCL, ALERT, A2, A1	–0.3	4	V
		A0	–0.3	(V_S) + 0.3	V
I_{SINK}	Sink current	SDA, ALERT		10	mA
T_J	Operating junction temperature		–55	150	°C
T_{stg}	Storage temperature range		–60	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

				MIN	MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		–2000	2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 4, 5, and 8)	–1000	1000	V
			Other pins	–1000	1000	V

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage	1.4	1.8	3.6	V
Operating free-air temperature, T_A	-40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TMP75BQDRQ1	TMP75BQDGKRQ1	TMP75BTQDGKRQ1	UNIT
		D (SOIC)	DGK (VSSOP)	DGK (VSSOP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	125.4	188.1	188.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	71.5	79.1	79.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	65.8	109.6	109.6	
ψ_{JT}	Junction-to-top characterization parameter	21.1	15.3	15.3	
ψ_{JB}	Junction-to-board characterization parameter	65.3	108	108	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics application note*.

6.5 Electrical Characteristics

At T_A = –40°C to 125°C and V_S = 1.4 V to 3.6 V, unless otherwise noted. Typical values at T_A = 25°C and V_S = 1.8 V

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
TEMPERATURE SENSOR							
	Temperature Range			-40		125	°C
	Temperature resolution				0.0625		°C
	Temperature accuracy (error)	TMP75BQDGKRQ1 TMP75BQDRQ1	–20°C to 85°C		±0.5	±2	°C
			–40°C to 125°C		±1	±3	°C
		TMP75BTQDGKRQ1	–40°C to 125°C		±0.5	±2	°C
DIGITAL INPUT/OUTPUT							
V_{IH}	High-level input voltage			0.7(V_S)		V_S	V
V_{IL}	Low-level input voltage			–0.3		0.3(V_S)	V
I_{IN}	Input current	0 V< V_{IN} < (V_S) + 0.3 V				1	µA
V_{OL}	Low-level output voltage	V_S ≥ 2 V, I_{OUT} = 3 mA		0		0.4	V
V_{OL}		V_S < 2 V, I_{OUT} = 3 mA		0		0.2(V_S)	V
	ADC resolution				12		Bits
	Conversion time	One-shot mode		20	27	35	ms
	Conversion modes	CR1 = 0, CR0 = 0 (default)			37		Conv/s
		CR1 = 0, CR0 = 1			18		Conv/s
		CR1 = 1, CR0 = 0			9		Conv/s
		CR1 = 1, CR0 = 1			4		Conv/s
	Timeout time			38	54	70	ms
POWER SUPPLY							
	Operating supply range			1.4		3.6	V
I_Q	Quiescent current	Serial bus inactive, CR1 = 0, CR0 = 0 (default)			45	89	µA
		Serial bus inactive, CR1 = 0, CR0 = 1			22	48	µA
		Serial bus inactive, CR1 = 1, CR0 = 0			12	30	µA
		Serial bus inactive, CR1 = 1, CR0 = 1			6.5	21	µA
I_{SD}	Shutdown current	Serial bus inactive			0.3	8	µA
		Serial bus active, SCL frequency = 400 kHz			10		µA
		Serial bus active, SCL frequency = 3.4 MHz			80		µA

6.6 Timing Requirements

			STANDARD		FAST-MODE		UNIT
			Min	Max	Min	Max	
f_{SCL}	SCL operating frequency	$V_S \geq 1.8$ V	0.001	0.4	0.001	3	MHz
		$V_S < 1.8$ V	0.001	0.4	0.001	2.5	MHz
$t_{(BUF)}$	Bus-free time between STOP and START conditions	$V_S \geq 1.8$ V	1300		160		ns
		$V_S < 1.8$ V	1300		260		ns
$t_{(HDSTA)}$	Hold time after repeated START condition. After this period, the first clock is generated.		600		160		ns
$t_{(SUSTA)}$	Repeated START condition setup time		600		160		ns
$t_{(SUSTO)}$	STOP condition setup time		600		160		ns
$t_{(HDDAT)}$	Data hold time	$V_S \geq 1.8$ V	0	900	0	100	ns
		$V_S < 1.8$ V	0	900	0	140	ns
$t_{(SUDAT)}$	Data setup time	$V_S \geq 1.8$ V	100		10		ns
		$V_S < 1.8$ V	100		20		ns
$t_{(LOW)}$	SCL clock low period	$V_S \geq 1.8$ V	1300		190		ns
		$V_S < 1.8$ V	1300		240		ns
$t_{(HIGH)}$	SCL clock high period		600		60		ns
$t_{R(SDA)}$, $t_{F(SDA)}$	Data rise and fall time			300		80	ns
$t_{R(SCL)}$, $t_{F(SCL)}$	Clock rise and fall time			300		40	ns
t_R	Clock and data rise time for SCLK ≤ 100 kHz			1000			ns

6.7 Typical Characteristics

At T_A = 25°C and V_S = 1.8V (unless otherwise noted).

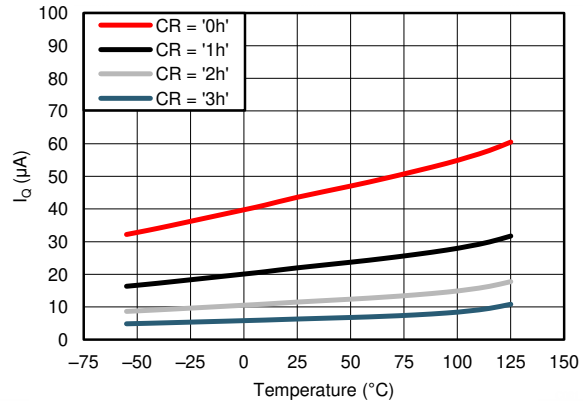


図 6-1. Quiescent Current vs Temperature

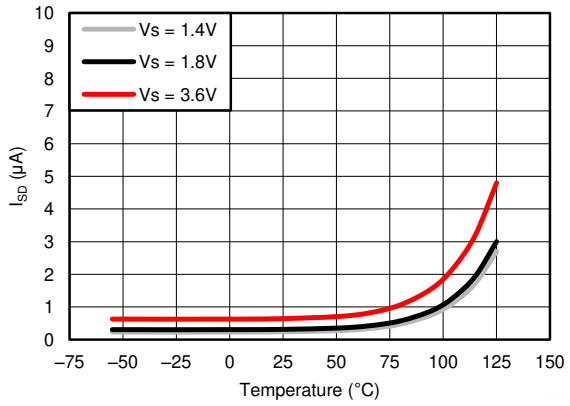


図 6-2. Shutdown Current vs Temperature

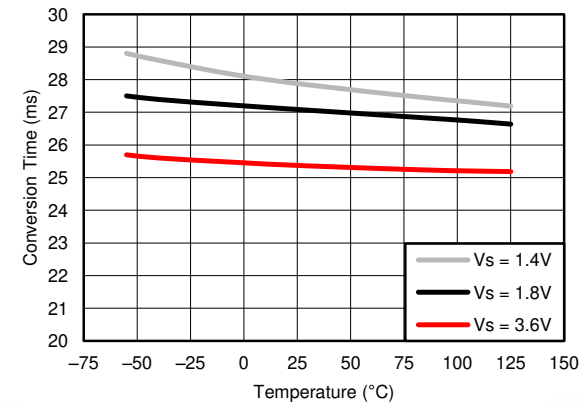


図 6-3. Conversion Time vs Temperature

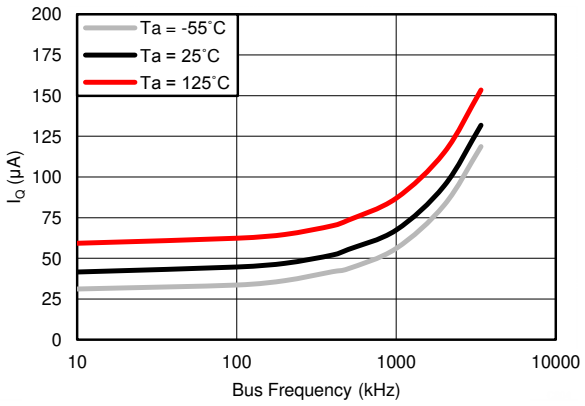


図 6-4. Quiescent Current vs Bus Frequency

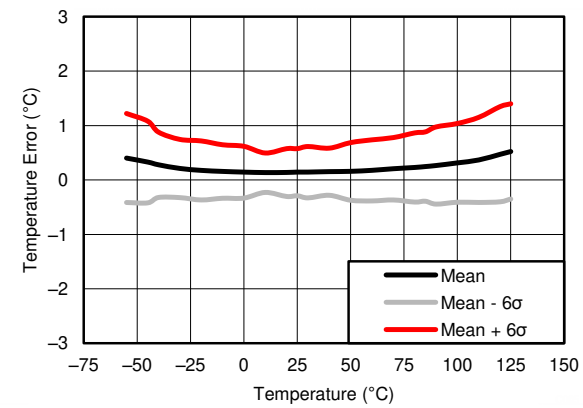


図 6-5. Temperature Error vs Temperature

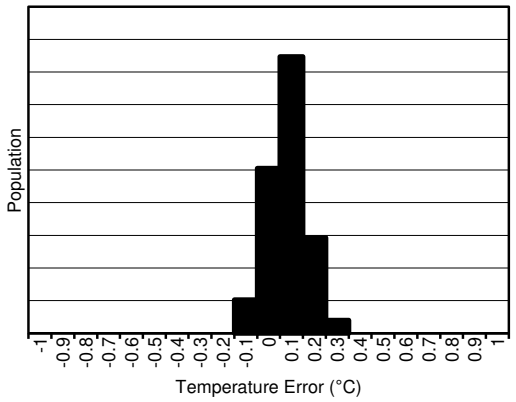


図 6-6. Temperature Error at 25°C

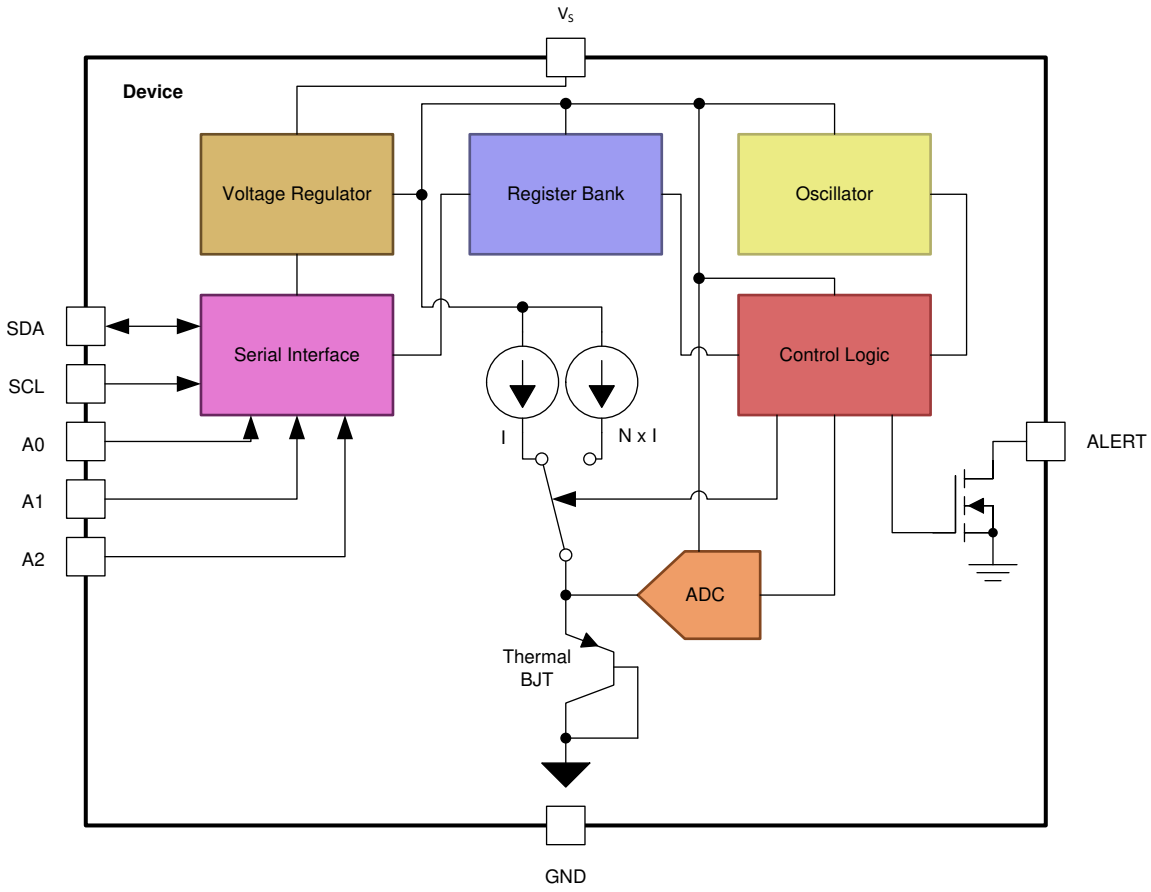
7 Detailed Description

7.1 Overview

The TMP75B-Q1 is a digital temperature sensor optimal for thermal management and thermal protection applications. The TMP75B-Q1 is two-wire and SMBus interface compatible, and is specified over a temperature range of –40°C to 125°C. The TMP75B**T**QDGKRQ1 is tri-temperature (–40°C, 25°C, and 125°C) tested in production for improved robustness.

The temperature sensing device for the TMP75B-Q1 is the chip. A bipolar junction transistor (BJT) inside the chip is used in a band-gap configuration to produce a voltage proportional to the chip temperature. The voltage is digitized and converted to a 12-bit temperature result in degrees Celsius, with a resolution of 0.0625°C. The package leads provide the primary thermal path because of the lower thermal resistance of the metal. Thus, the temperature result is equivalent to the local temperature of the printed circuit board (PCB) where the sensor is mounted.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Digital Temperature Output

The 12-bit digital output from each temperature measurement conversion is stored in the read-only temperature register. Two bytes must be read to obtain the data; see 図 8-2. Note that byte 1 is the most significant byte, followed by byte 2, the least significant byte. The temperature result is left-justified with the 12 most significant bits used to indicate the temperature. There is no need to read the second byte if resolution below 1°C is not required. 表 7-1 summarizes the temperature data format. One LSB equals 0.0625°C. Negative numbers are represented in binary 2's complement format.

表 7-1. Temperature Data Format

TEMPERATURE (°C) (1)	DIGITAL OUTPUT	
	BINARY	HEX
128	0111 1111 1111	7FF
127.9375	0111 1111 1111	7FF
100	0110 0100 0000	640
80	0101 0000 0000	500
75	0100 1011 0000	4B0
50	0011 0010 0000	320
25	0001 1001 0000	190
0.25	0000 0000 0100	004
0	0000 0000 0000	000
–0.25	1111 1111 1100	FFC
–25	1110 0111 0000	E70
–55	1100 1001 0000	C90

(1) The temperature sensor resolution is 0.0625°C/LSB.

表 7-1 does not supply a full list of all temperatures. Use the following rules to obtain the digital data format for a given temperature, and so forth.

To convert positive temperatures to a digital data format:

Divide the temperature by the resolution. Then, convert the result to binary code with a 12-bit, left-justified format, and MSB = 0 to denote a positive sign.

Example: (50°C) / (0.0625°C / LSB) = 800 = 320h = 0011 0010 0000

To convert a positive digital data format to temperature:

Convert the 12-bit, left-justified binary temperature result, with the MSB = 0 to denote a positive sign, to a decimal number. Then, multiply the decimal number by the resolution to obtain the positive temperature.

Example: 0011 0010 0000 = 320h = 800 × (0.0625°C / LSB) = 50°C

To convert negative temperatures to a digital data format:

Divide the absolute value of the temperature by the resolution, and convert the result to binary code with a 12-bit, left-justified format. Then, generate the 2's complement of the result by complementing the binary number and adding one. Denote a negative number with MSB = 1.

Example: (|–25°C|) / (0.0625°C / LSB) = 400 = 190h = 0001 1001 0000

Two's complement format: 1110 0110 1111 + 1 = 1110 0111 0000

To convert a negative digital data format to temperature:

Generate the 2's compliment of the 12-bit, left-justified binary number of the temperature result (with MSB = 1, denoting negative temperature result) by complementing the binary number and adding one. This represents the binary number of the absolute value of the temperature. Convert to decimal number and multiply by the resolution to get the absolute temperature, then multiply by –1 for the negative sign.

Example: 1110 0111 0000 has twos compliment of 0001 1001 0000 = 0001 1000 1111 + 1

Convert to temperature: 0001 1001 0000 = 190h = 400; 400 × (0.0625°C / LSB) = 25°C = (|–25°C|); (|–25°C|) × (–1) = –25°C

7.3.2 Temperature Limits and Alert

The temperature limits are stored in the T_{LOW} and T_{HIGH} registers (表 8-4 and 表 8-5) in the same format as the temperature result, and the values are compared to the temperature result on every conversion. The outcome of the comparison drives the behavior of the ALERT pin, which can operate as a comparator output or an interrupt, and is set by the TM bit in the configuration register (表 8-3).

In comparator mode (TM = 0, default), the ALERT pin becomes active when the temperature is equal to or exceeds the value in T_{HIGH} (fault conditions) for a consecutive number of conversions as set by the FQ bits of the configuration register. ALERT clears when the temperature falls below T_{LOW} for the same consecutive number of conversions. The difference between the two limits acts as a hysteresis on the comparator output, and a fault counter prevents false alerts as a result of environmental noise.

In interrupt mode (TM = 1), the ALERT pin becomes active when the temperature equals or exceeds the value in T_{HIGH} for a consecutive number of fault conditions. The ALERT pin remains active until a read operation of any register occurs, or the device successfully responds to the SMBus alert response address. The ALERT pin is also cleared if the device is placed in shutdown mode (see the *Shutdown Mode* section for shutdown mode description). After the ALERT pin is cleared, this pin becomes active again only when the temperature falls below T_{LOW} for a consecutive number of fault conditions, and remains active until cleared by a read operation of any register, or a successful response to the SMBus alert response address. After the ALERT pin is cleared, the cycle repeats with the ALERT pin becoming active when the temperature equals or exceeds T_{HIGH}, and so on. The ALERT pin can also be cleared by resetting the device with the general-call reset command. This action also clears the state of the internal registers in the device and the fault counter memory, returning the device to comparator mode (TM = 0).

The active state of the ALERT pin is set by the POL bit in the configuration register. When POL = 0 (default), the ALERT pin is active low. When POL = 1, the ALERT pin is active high. The operation of the ALERT pin in various modes is shown in 図 7-1.

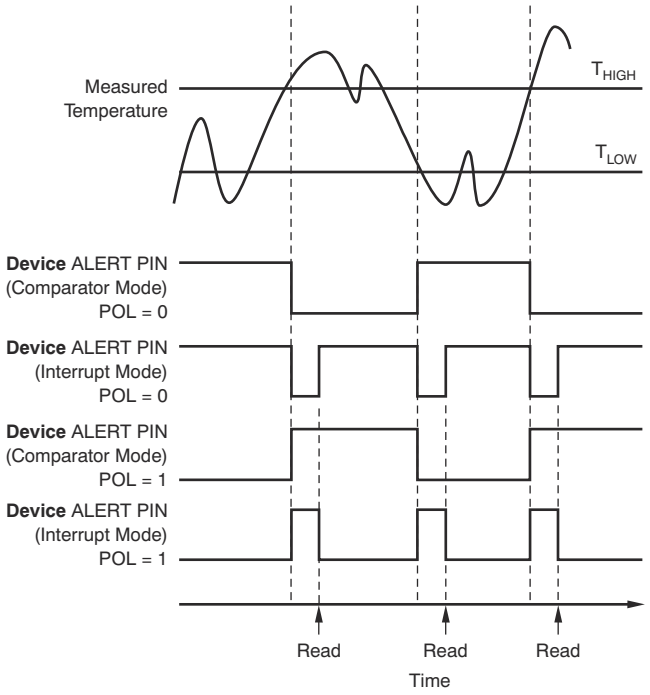


図 7-1. ALERT Pin Modes of Operation

7.3.3 Serial Interface

The TMP75B-Q1 operates as a target device only on the two-wire bus and SMBus. Connections to the bus are made using the open-drain I/O lines, SDA and SCL. The SDA and SCL pins feature integrated spike-suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The TMP75B-Q1 supports the transmission protocol for both fast (1kHz to 400kHz) and high-speed (1kHz to 3MHz) modes. All data bytes are transmitted MSB first.

7.3.3.1 Bus Overview

The device that initiates the transfer is called a *controller*, and the devices controlled by the controller are *targets*. The bus must be controlled by a controller device that generates the serial clock (SCL), controls the bus access, and generates the start and stop conditions.

To address a specific device, initiate a start condition by pulling the data line (SDA) from a high to a low logic level while SCL is high. All targets on the bus shift in the target address byte; the last bit indicates whether a read or write operation follows. During the ninth clock pulse, the target being addressed responds to the controller by generating an acknowledge bit and pulling SDA low.

Data transfer is then initiated and sent over eight clock pulses followed by an acknowledge bit. During data transfer, SDA must remain stable while SCL is high because any change in SDA while SCL is high is interpreted as a start or stop signal.

After all data have been transferred, the controller generates a stop condition indicated by pulling SDA from low to high, while SCL is high.

7.3.3.2 Serial Bus Address

To communicate with the TMP75B-Q1, the controller must first communicate with target devices using a target address byte. The target address byte consists of seven address bits, and a direction bit indicating the intent of executing either a read or write operation. The TMP75B-Q1 features three address pins that allow up to eight devices to be addressed on a single bus. The TMP75B-Q1 latches the status of the address pins at the start of a communication. 表 7-2 describes the pin logic levels and the corresponding address values.

表 7-2. Address Pin Connections and Target Addresses

DEVICE TWO-WIRE ADDRESS	A2	A1	A0
1001000	GND	GND	GND
1001001	GND	GND	V_S
1001010	GND	V_S	GND
1001011	GND	V_S	V_S
1001100	V_S	GND	GND
1001101	V_S	GND	V_S
1001110	V_S	V_S	GND
1001111	V_S	V_S	V_S

7.3.3.3 Writing and Reading Operation

Accessing a particular register on the TMP75B-Q1 is accomplished by writing the appropriate value to the pointer register. The value for the pointer register is the first byte transferred after the target address byte with the R/W bit low. Every write operation to the TMP75B-Q1 requires a value for the pointer register (see 図 7-3).

When reading from the TMP75B-Q1, the last value stored in the pointer register by a write operation is used to determine which register is read by a read operation. To change the register pointer for a read operation, a new value must be written to the pointer register. This action is accomplished by issuing a target address byte with the R/W bit low, followed by the pointer register byte. No additional data are required. The controller can then generate a start condition and send the target address byte with the R/W bit high to initiate the read command. See 図 7-4 for details of this sequence. If repeated reads from the same register are desired, there is no need to continually send the pointer register bytes because the TMP75B-Q1 stores the pointer register value until the value is changed by the next write operation.

Note that register bytes are sent with the most significant byte first, followed by the least significant byte.

7.3.3.4 Target-Mode Operations

The TMP75B-Q1 can operate as a target receiver or target transmitter.

7.3.3.4.1 Target Receiver Mode:

The first byte transmitted by the controller is the target address, with the R/W bit low. The TMP75B-Q1 then acknowledges reception of a valid address. The next byte transmitted by the controller is the pointer register. The TMP75B-Q1 then acknowledges reception of the pointer register byte. The next byte or bytes are written to the register addressed by the pointer register. The TMP75B-Q1 acknowledges reception of each data byte. The controller can terminate data transfer by generating a start or stop condition.

7.3.3.4.2 Target Transmitter Mode:

The first byte transmitted by the controller is the target address, with the R/W bit high. The target acknowledges reception of a valid target address. The next byte is transmitted by the target and is the most significant byte of the register indicated by the pointer register. The controller acknowledges reception of the data byte. The next byte transmitted by the target is the least significant byte. The controller acknowledges reception of the data byte. The controller can terminate data transfer by generating a not-acknowledge bit on reception of any data byte, or by generating a start or stop condition.

7.3.3.5 SMBus Alert Function

The TMP75B-Q1 supports the SMBus alert function. When the TMP75B-Q1 operates in interrupt mode (TM = 1), the ALERT pin can be connected as an SMBus alert signal. When a controller senses that an alert condition is present on the ALERT line, the controller sends an SMBus alert command (00011001) to the bus. If the ALERT pin is active, the device acknowledges the SMBus alert command and responds by returning the target address on the SDA line. The eighth bit (LSB) of the target address byte indicates whether the alert condition is caused by the temperature exceeding T_{HIGH} or falling below T_{LOW}. The LSB is high if the temperature is greater than T_{HIGH}, or low if the temperature is less than T_{LOW}. See 図 7-5 for details of this sequence.

If multiple devices on the bus respond to the SMBus alert command, arbitration during the target address portion of the SMBus alert command determines which device clears the alert status first. If the TMP75B-Q1 wins the arbitration, the ALERT pin becomes inactive at the completion of the SMBus alert command. If the TMP75B-Q1 loses the arbitration, the ALERT pin remains active.

7.3.3.6 General Call

The TMP75B-Q1 responds to a two-wire general call address (0000000) if the eighth bit is 0. The device acknowledges the general call address and responds to commands in the second byte. If the second byte is 00000100, the TMP75B-Q1 latches the status of the address pin, but does not reset. If the second byte is 00000110, the TMP75B-Q1 internal registers are reset to power-up values.

7.3.3.7 High-Speed (Hs) Mode

For the two-wire bus to operate at frequencies above 400kHz, the controller device must issue an SMBus Hs-mode controller code (00001xxx) as the first byte after a start condition to switch the bus to high-speed operation. The TMP75B-Q1 does not acknowledge this byte, but does switch the input filters on SDA and SCL and the output filters on SDA to operate in Hs-mode, allowing transfers at up to 3MHz. After the Hs-mode controller code has been issued, the controller transmits a two-wire target address to initiate a data-transfer operation. The bus continues to operate in Hs-mode until a stop condition occurs on the bus. Upon receiving the stop condition, the TMP75B-Q1 switches the input and output filters back to fast-mode operation.

7.3.3.8 Timeout Function

The TMP75B-Q1 resets the serial interface if SCL or SDA are held low for 54ms (typical) between a start and stop condition. If the TMP75B-Q1 is pulled low, the device releases the bus and then waits for a start condition. To avoid activating the timeout function, maintaining a communication speed of at least 1kHz is necessary for the SCL operating frequency.

7.3.3.9 Two-Wire Timing

The TMP75B-Q1 is two-wire and SMBus compatible. 図 7-2 to 図 7-5 describe the various operations on the TMP75B-Q1. Parameters for 図 7-2 are defined in セクション 6.6. Bus definitions are:

Bus Idle	Both SDA and SCL lines remain high.
Start Data Transfer	A change in the state of the SDA line, from high to low, while the SCL line is high defines a start condition. Each data transfer is initiated with a start condition.
Stop Data Transfer	A change in the state of the SDA line from low to high while the SCL line is high defines a stop condition. Each data transfer is terminated with a repeated start or stop condition.
Data Transfer	The number of data bytes transferred between a start and a stop condition is not limited, and is determined by the controller device. The receiver acknowledges the transfer of data. Using the TMP75B-Q1 for single-byte updates is also possible. To update only the MS byte, terminate communication by issuing a start or stop condition on the bus.
Acknowledge	Each receiving device, when addressed, must generate an acknowledge bit. A device that acknowledges must pull down the SDA line during the acknowledge clock pulse so that the SDA line is stable low during the high period of the acknowledge clock pulse. Setup and hold times must be taken into account. When a controller receives data, the termination of the data transfer can be signaled by the controller generating a *not-acknowledge* (1) on the last byte transmitted by the target.

7.3.3.10 Two-Wire Timing Diagrams

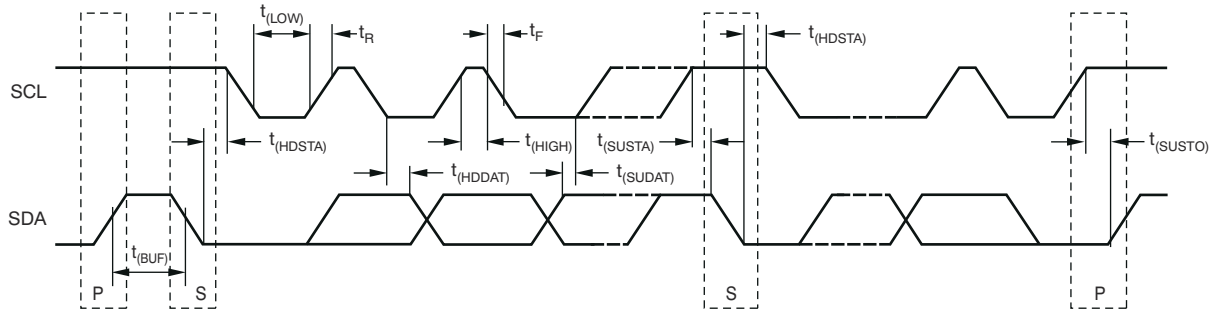
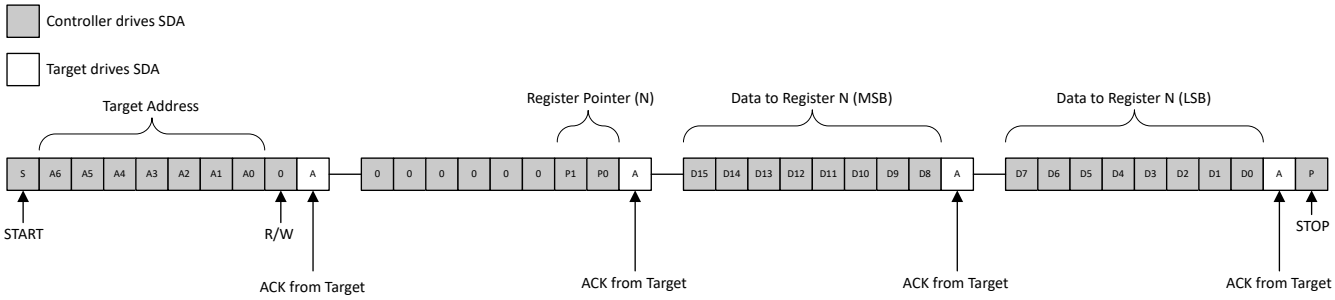


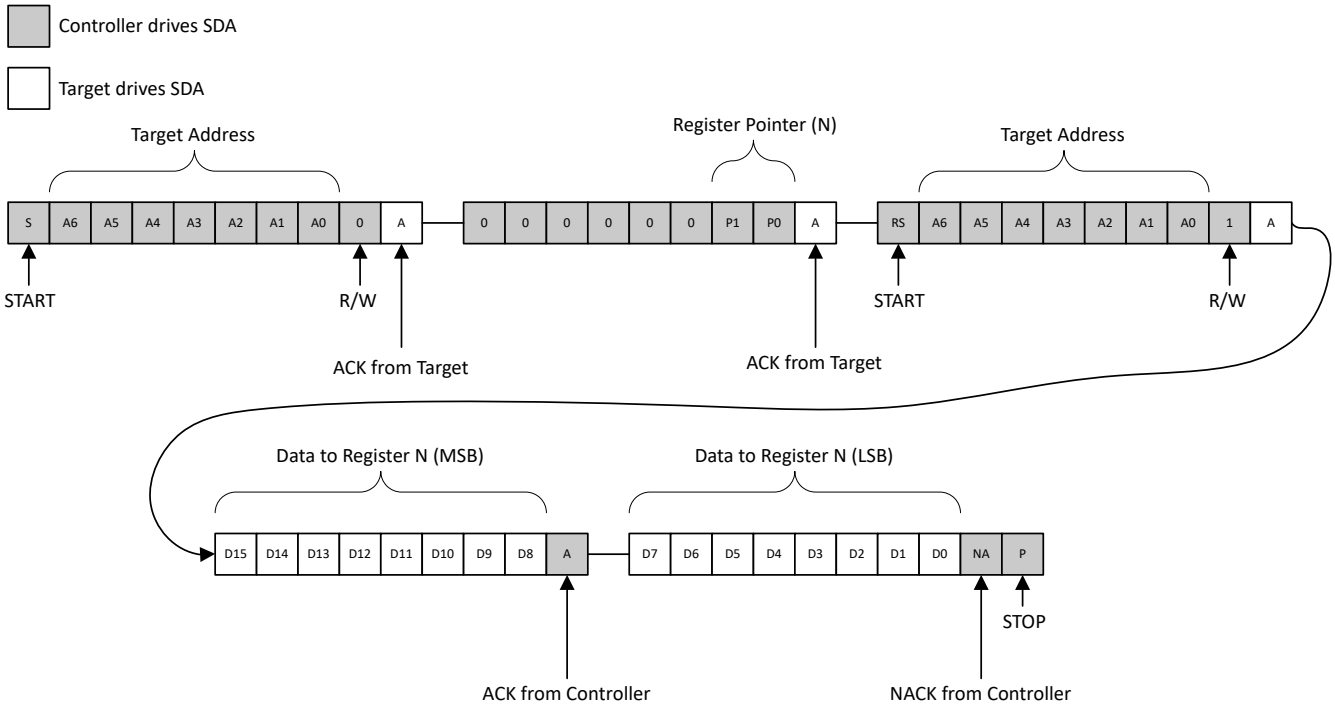
図 7-2. Two-Wire Timing Diagram



注

The value of A7 through A0 are determined by the connections of the corresponding pins. See also 表 7-2.

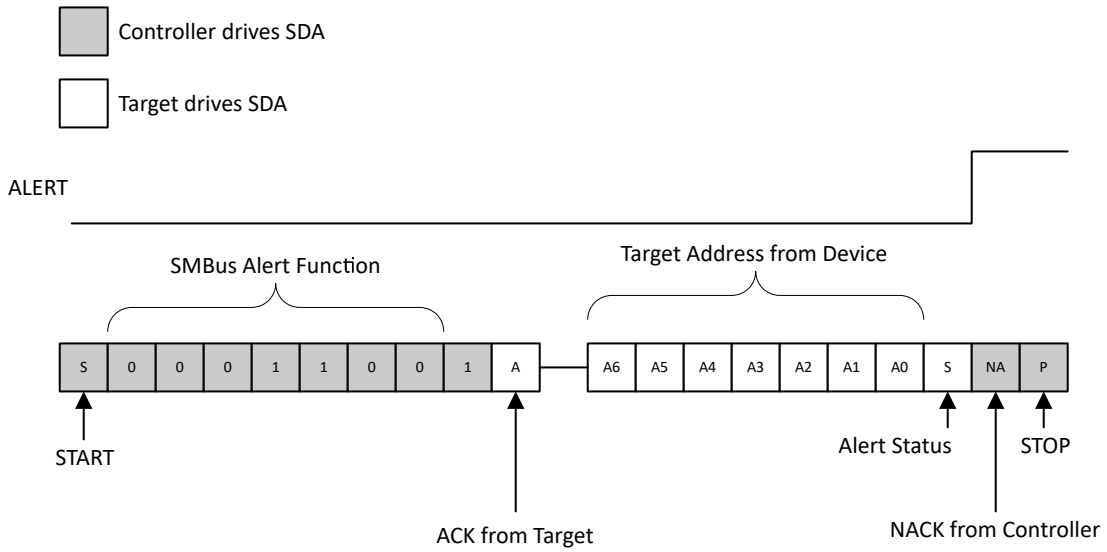
図 7-3. Two-Wire Timing Diagram for Write Word Format



注

The value of A7 through A0 are determined by the connections of the corresponding pins. See also 表 7-2.

図 7-4. Two-Wire Timing Diagram for Read Word Format



注

The value of A7 through A0 are determined by the connections of the corresponding pins. See also 表 7-2.

図 7-5. Timing Diagram for SMBus Alert

7.4 Device Functional Modes

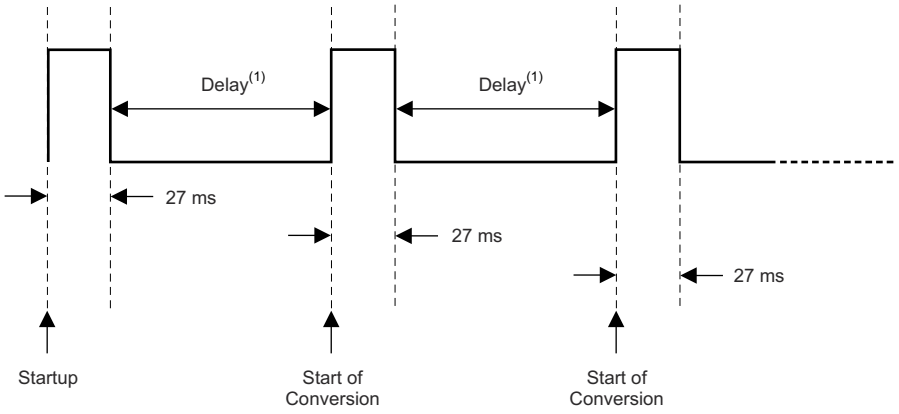
7.4.1 Continuous-Conversion Mode

The default mode of the TMP75B-Q1 is continuous conversion, where the ADC performs continuous temperature conversions and stores each result to the temperature register, overwriting the result from the previous conversion. Conversion rate bits CR1 and CR0 in the configuration register configure the TMP75B-Q1 for typical conversion rates of 37Hz, 18Hz, 9Hz, or 4Hz. The TMP75B-Q1 has a typical conversion time of 27ms. To achieve different conversion rates, the TMP75B-Q1 makes a conversion, and then powers down and waits for the appropriate delay set by CR1 and CR0. The default rate is 37Hz (no delay between conversions). 表 7-3 shows the settings for CR1 and CR0.

表 7-3. Conversion Rate Settings

CR1	CR0	CONVERSION RATE (TYP)	I_Q (TYP)
0	0	37Hz (continuous conversion, default)	45µA
0	1	18Hz	22µA
1	0	9Hz	12µA
1	1	4Hz	6.5µA

After power-up or a general-call reset, the TMP75B-Q1 immediately starts a conversion, as shown in 図 7-6. The first result is available after 27ms (typical). The active quiescent current during conversion is 45µA (typical at 25°C). The quiescent current during delay is 1µA (typical at 25°C).



A. Delay is set by the CR bits in the configuration register.

図 7-6. Conversion Start

7.4.2 Shutdown Mode

Shutdown mode saves maximum power by shutting down all device circuitry other than the serial interface, and reduces current consumption to typically less than 0.3µA. Shutdown mode is enabled when the SD bit in the configuration register is set to 1; the device shuts down after the current conversion is completed. When SD is equal to 0, the device operates in continuous-conversion mode. When shutdown mode is enabled, the ALERT pin and fault counter clear in both comparator and interrupt modes; however, this clearing occurs with the rising edge of the shutdown signal. After shutdown is enabled, reprogramming shutdown does not clear the ALERT pin and the fault counter until a rising edge is generated on the shutdown signal.

7.4.3 One-Shot Mode

The TMP75B-Q1 features a *one-shot* temperature measurement mode. When the device is in shutdown mode, writing a 1 to the OS bit starts a single temperature conversion. The device returns to the shutdown state at the completion of the single conversion. This mode reduces power consumption in the TMP75B-Q1 when continuous temperature monitoring is not required. When the configuration register is read, the OS bit always reads zero.

7.5 Programming

図 7-7 shows the internal register structure of the TMP75B-Q1. Use the 8-bit pointer register to address a given data register. The pointer register uses the two LSBs to identify which of the data registers respond to a read or write command. 図 8-1 identifies the bits of the pointer register byte.

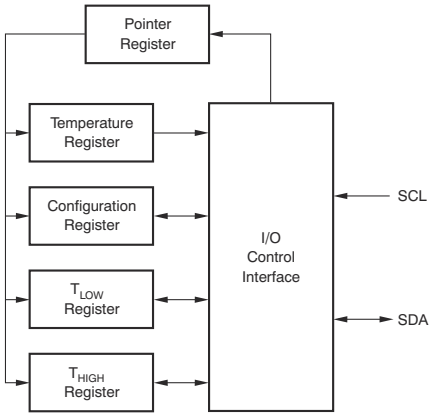


図 7-7. Internal Register Structure

8 Register Map

表 8-1 describes the registers available in the TMP75B-Q1 with the corresponding pointer addresses, followed by the description of the bits in each register.

表 8-1. Register Map and Pointer Addresses

P1	P0	REGISTER
0	0	Temperature register (read only, default)
0	1	Configuration register (read/write)
1	0	T_{LOW} register (read/write)
1	1	T_{HIGH} register (read/write)

図 8-1. Pointer Register (pointer = N/A) [reset = 00h]

7	6	5	4	3	2	1	0
Reserved						P1	P0
W-0h						W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

図 8-2. Temperature Register (pointer = 0h) [reset = 0000h]

15	14	13	12	11	10	9	8
T11	T10	T9	T8	T7	T6	T5	T4
R-0h							
7	6	5	4	3	2	1	0
T3	T2	T1	T0	**Reserved**			
R-0h				R-0h			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-2. Temperature Register Description

Name	Description
T11 to T4	The 8 MSBs of the temperature result (resolution of 1°C)
T3 to T0	The 4 LSBs of the temperature result (resolution of 0.0625°C)

図 8-3. Configuration Register (pointer = 1h) [reset = 00FFh]

15	14	13	12	11	10	9	8
OS	CR		FQ		POL	TM	SD
R/W-0h	R/W-0h		R/W-0h		R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
Reserved							
R-FFh							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-3. Configuration Register Description

Name	Description
OS	One-shot mode In shutdown (SD = 1), write 1 to start a conversion. OS always reads back 0.

表 8-3. Configuration Register Description (続き)

Name	Description
CR	Conversion rate control CR = 0h: 37Hz conversion rate (typ) (default) CR = 1h: 18Hz conversion rate (typ) CR = 2h: 9Hz conversion rate (typ) CR = 3h: 4Hz conversion rate (typ)
FQ	Fault queue to trigger the ALERT pin FQ = 0h: 1 fault (default) FQ = 1h: 2 faults FQ = 2h: 4 faults FQ = 3h: 6 faults
POL	ALERT polarity control POL = 0: ALERT is active low (default) POL = 1: ALERT is active high
TM	ALERT thermostat mode control TM = 0: ALERT is in comparator mode (default) TM = 1: ALERT is in interrupt mode
SD	Shutdown control bit SD = 0: Device is in continuous conversion mode (default) SD = 1: Device is in shutdown mode

図 8-4. T_{LOW}: Temperature Low Limit Register (pointer = 2h) [reset = 4B00h] (1)

15	14	13	12	11	10	9	8
L11	L10	L9	L8	L7	L6	L5	L4
R/W-4Bh							
7	6	5	4	3	2	1	0
L3	L2	L1	L0	**Reserved**			
R/W-0h				R-0h			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

(1) 4B00h = 75°C.

表 8-4. T_{LOW} Register Description

Name	Description
L11 to L4	The 8 MSBs of the temperature low limit (resolution of 1°C)
L3 to L0	The 4 LSBs of the temperature low limit (resolution of 0.0625°C)

図 8-5. T_{HIGH}: Temperature High Limit Register (pointer = 3h) [reset = 5000h] (1)

15	14	13	12	11	10	9	8
H11	H10	H9	H8	H7	H6	H5	H4
R/W-50h							
7	6	5	4	3	2	1	0
H3	H2	H1	H0	**Reserved**			
R/W-0h				R-0h			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

(1) 5000h = 80°C.

表 8-5. T_{HIGH} Register Description

Name	Description
H11 to H4	The 8 MSBs of the temperature high limit (resolution of 1°C)
H3 to H0	The 4 LSBs of the temperature high limit (resolution of 0.0625°C)

9 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The TMP75B-Q1 is used to measure the PCB temperature where the device is mounted. The programmable address options allow up to eight locations on the board to be monitored on a single serial bus. Connecting the ALERT pins together and programming the temperature limit registers to desired values allows for a temperature watchdog operation of all devices, interrupting the host controller only if the temperature exceeds the limits.

9.2 Typical Application

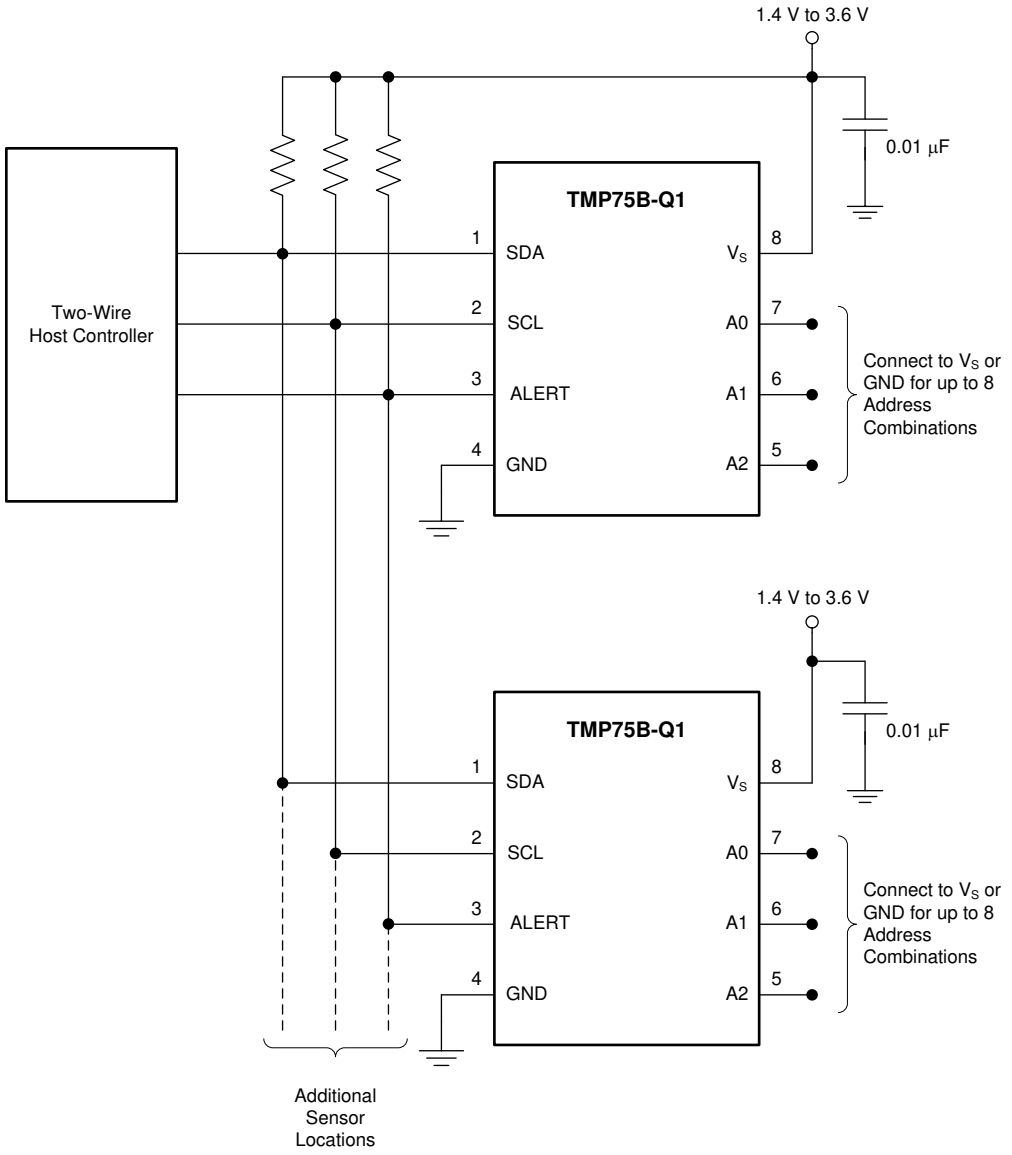


図 9-1. Temperature Monitoring of Multiple Locations on a PCB

9.2.1 Design Requirements

The TMP75B-Q1 only requires pullup resistors on SDA and ALERT, although a pullup resistor is typically present on the SCL as well. A 0.01µF bypass capacitor on the supply is recommended, as shown in 図 9-1. The SCL, SDA, and ALERT lines can be pulled up to a supply that is equal to or higher than V_S through the pullup resistors. To configure one of eight different addresses on the bus, connect A0, A1, and A2 to either V_S or GND.

9.2.2 Detailed Design Procedure

The TMP75B-Q1 must be placed in close proximity to the heat source to be monitored, with a proper layout for good thermal coupling. This placement verifies that temperature changes are captured within the shortest possible time interval.

9.2.3 Application Curve

図 9-2 shows the step response of the TMP75B-Q1 to a submersion in an oil bath of 100°C from room temperature (27°C). The time-constant, or the time for the output to reach 63% of the input step, is 1.5 seconds.

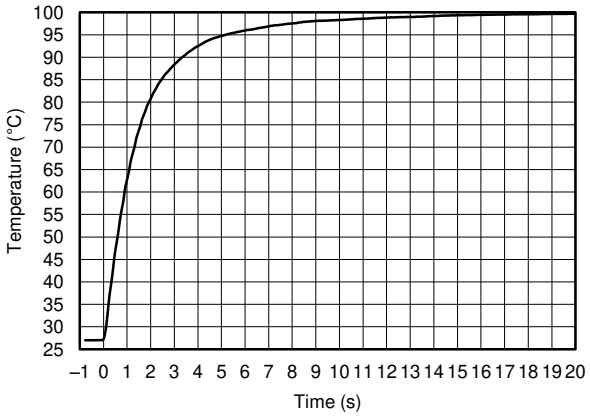


図 9-2. Temperature Step Response

9.3 Power-Supply Recommendations

The TMP75B-Q1 operates with power supply in the range of 1.4V to 3.6V. The device is optimized for operation at 1.8V supply but can measure temperature accurately in the full supply range.

A power-supply bypass capacitor is recommended; place this capacitor as close as possible to the supply and ground pins of the device. A typical value for this supply bypass capacitor is 0.01µF. Applications with noisy or high-impedance power supplies can require additional decoupling capacitors to reject power-supply noise.

9.4 Layout

9.4.1 Layout Guidelines

Place the temperature sensor as close as possible and run copper planes on the ground or other layers to provide good thermal coupling to the heat source for fast settling and accurate measurement of the temperature of the hot spot.

Place the power-supply bypass capacitor as close as possible to the supply and ground pins.

Pull up the open-drain output pins (SDA and ALERT) to a supply voltage rail (V_S or higher but up to 3.6V) through 10kΩ pullup resistors. Smaller values of the resistors can be used to compensate for long bus traces that can cause an increase in capacitance and slow rise time for the open-drain outputs; the values must not be less than 1kΩ to avoid self-heating effects due to increased current through the part in the low states of the outputs.

9.4.2 Layout Example

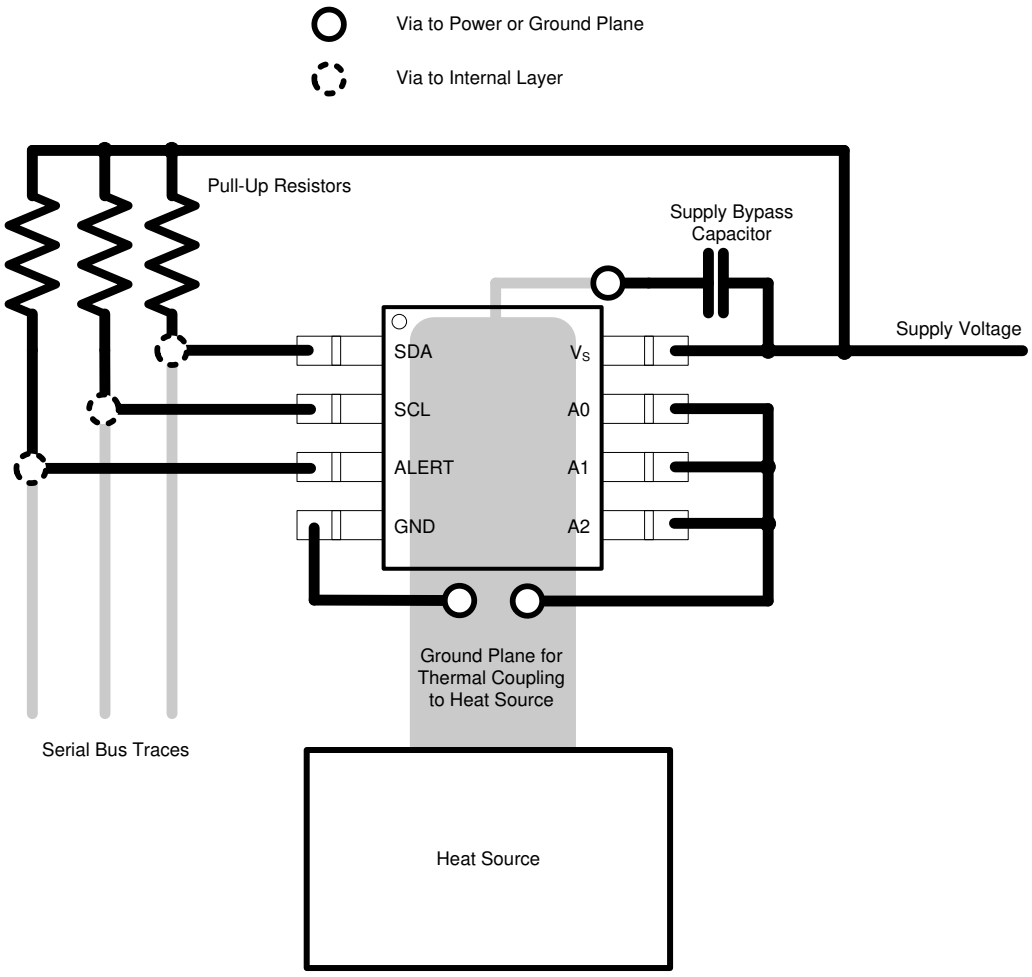


図 9-3. Layout Example

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

Texas Instruments, TMP75xEVM User's Guide, EVM user's guide

10.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

10.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

10.4 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

10.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

Changes from Revision A (June 2022) to Revision B (October 2024)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新	1
• Added the TMP75BTQDGKR device information in the specifications section and throughout the document.	5

Changes from Revision * (October 2014) to Revision A (June 2022)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新	1
• I^2C に言及している場合、すべての旧式の用語をコントローラおよびターゲットに変更	1
• 「特長」セクションに機能安全の情報を追加	1

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、テキサス・インスツルメンツの販売条件、または ti.com やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMP75BQDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	T75BQ
TMP75BQDGKRQ1.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	T75BQ
TMP75BQDQ1	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	T75BQ
TMP75BQDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T75BQ
TMP75BQDRQ1.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T75BQ
TMP75BTQDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	75BTQ
TMP75BTQDGKRQ1.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	75BTQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TMP75B-Q1 :

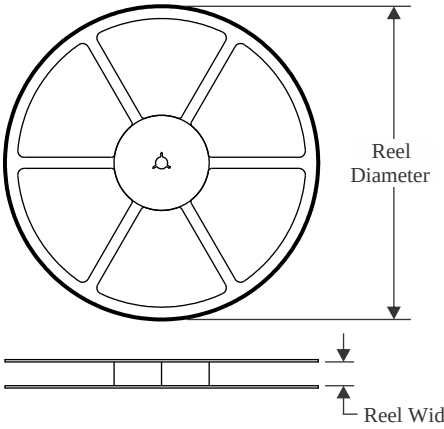
- Catalog : TMP75B

NOTE: Qualified Version Definitions:

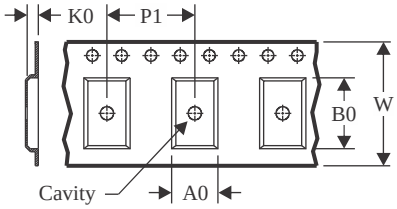
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

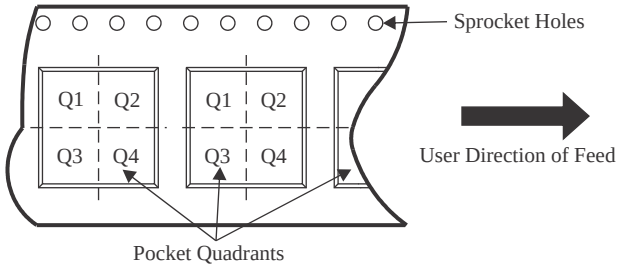


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

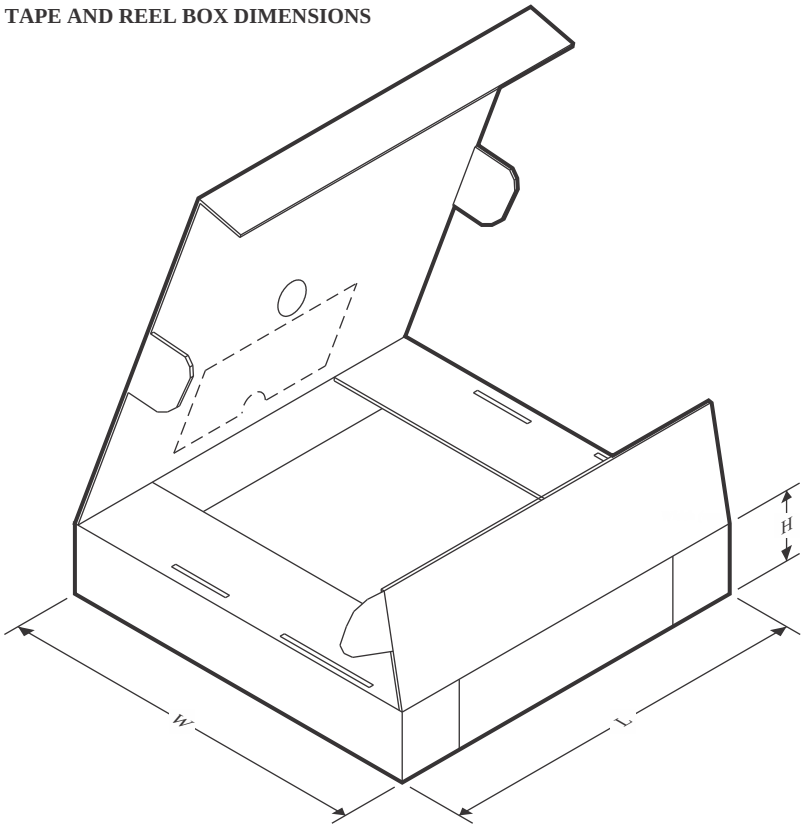
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP75BQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP75BQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP75BQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TMP75BTQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

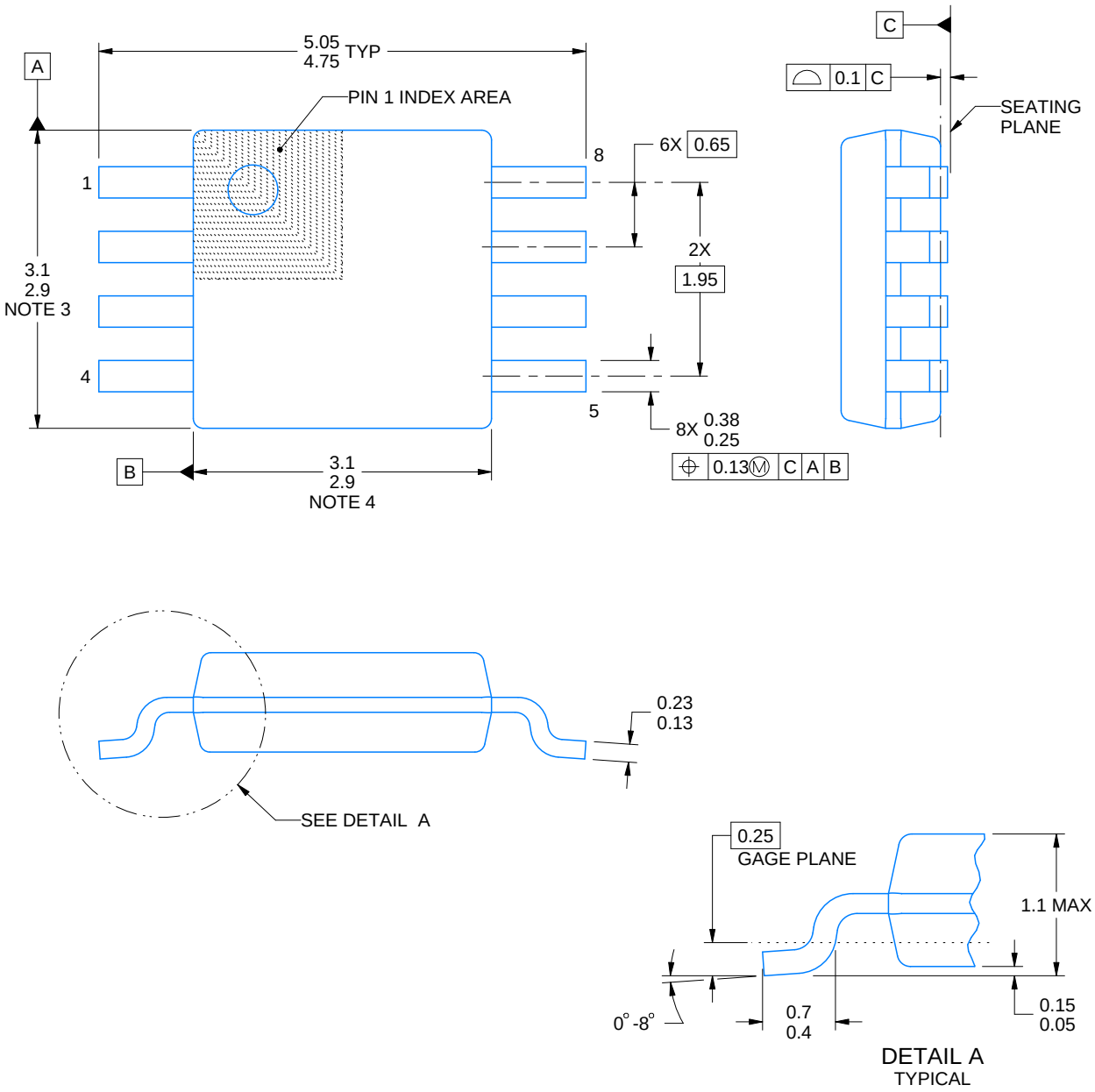
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP75BQDGKRQ1	VSSOP	DGK	8	2500	353.0	353.0	32.0
TMP75BQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
TMP75BQDRQ1	SOIC	D	8	2500	353.0	353.0	32.0
TMP75BTQDGKRQ1	VSSOP	DGK	8	2500	353.0	353.0	32.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

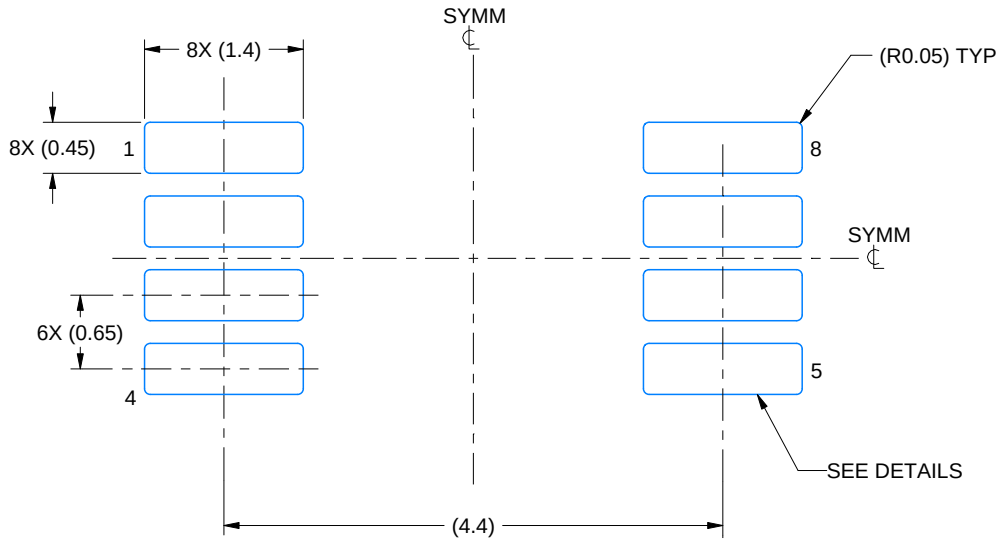
SMALL OUTLINE PACKAGE



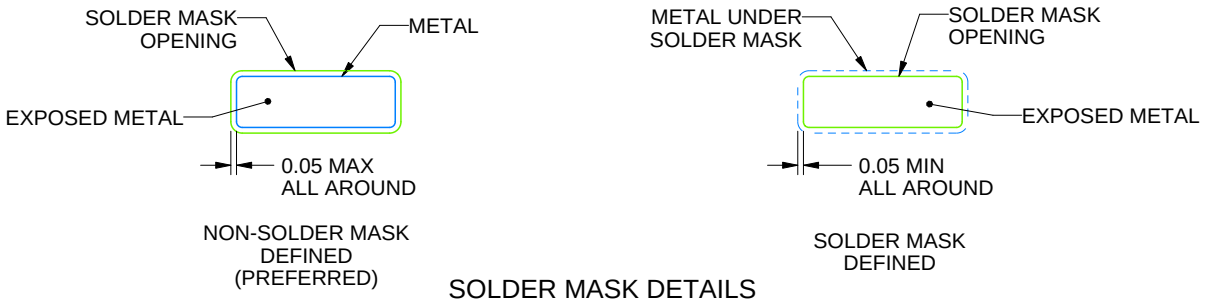
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

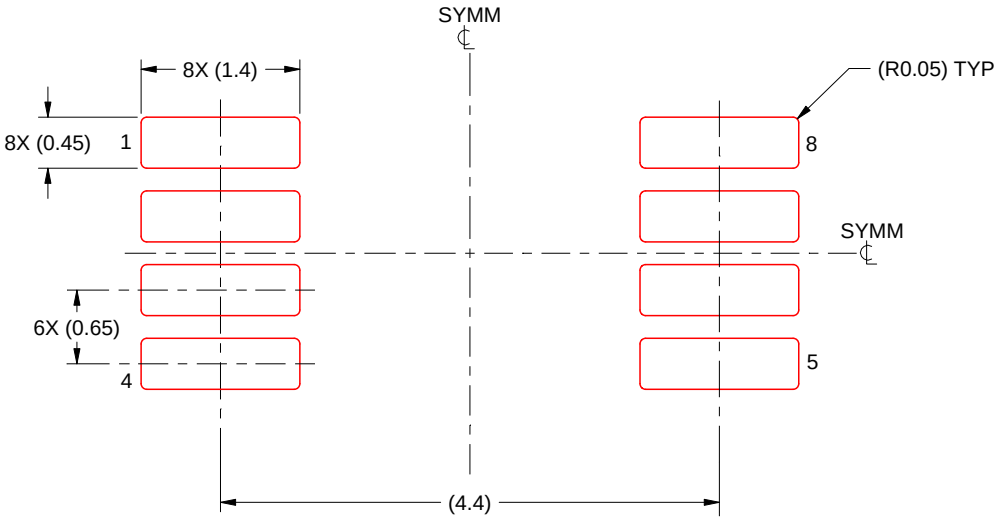


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

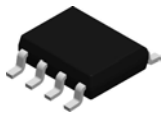


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

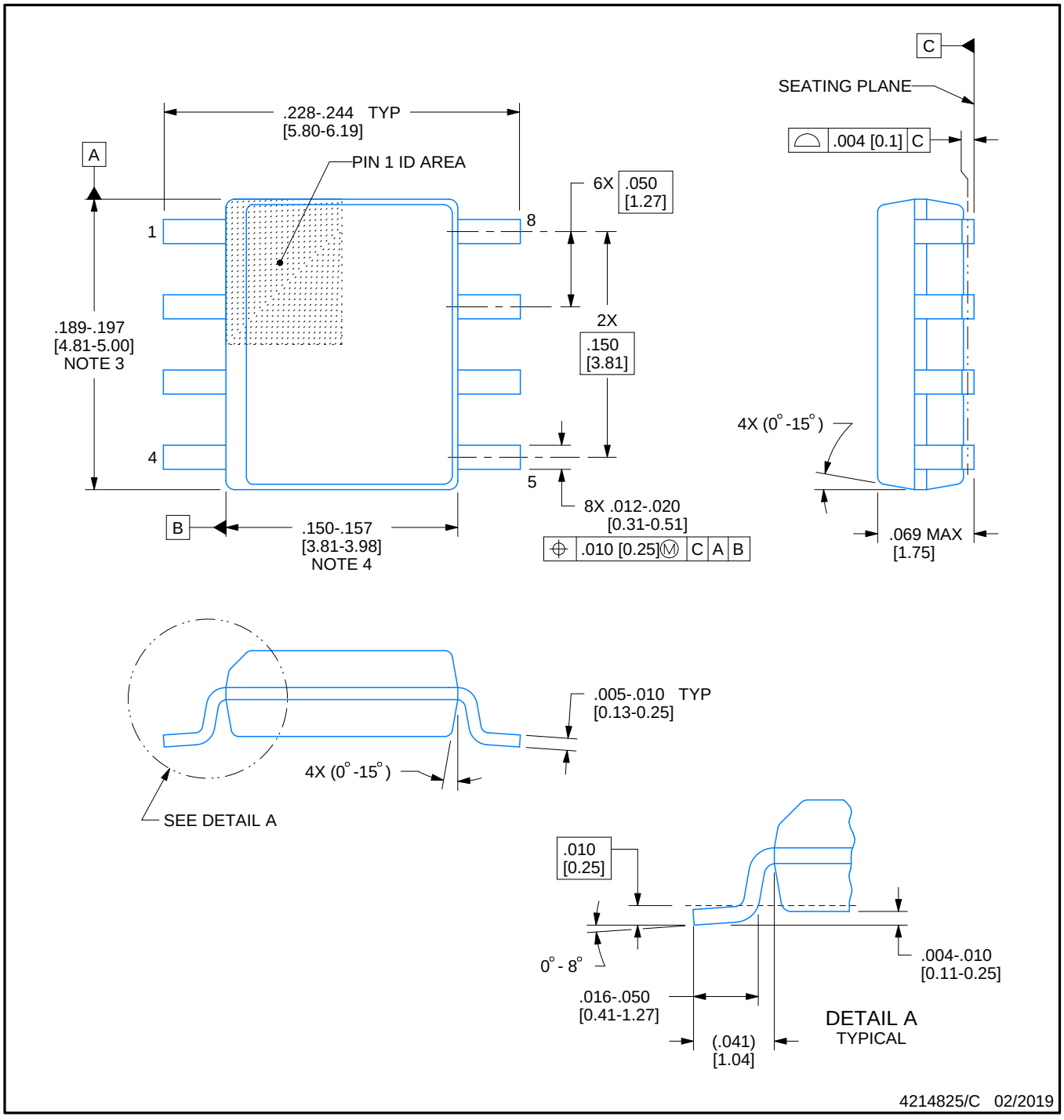


PACKAGE OUTLINE

D0008A

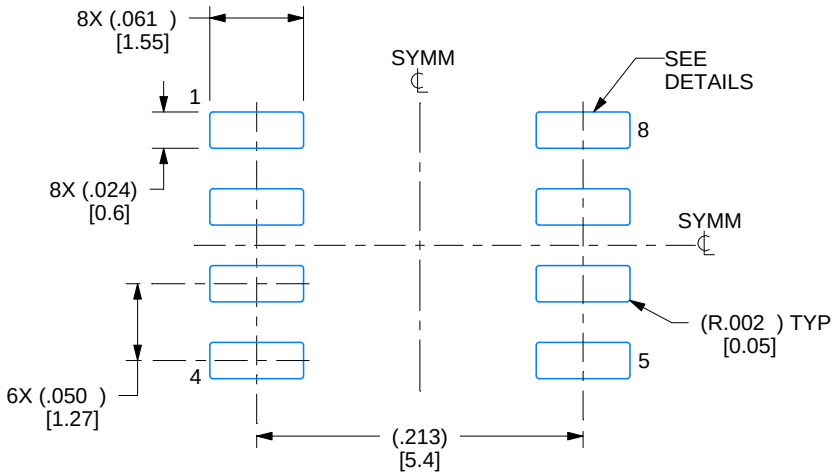
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

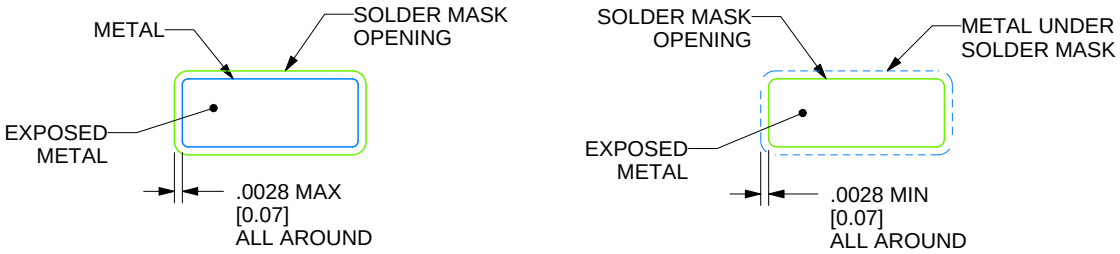


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

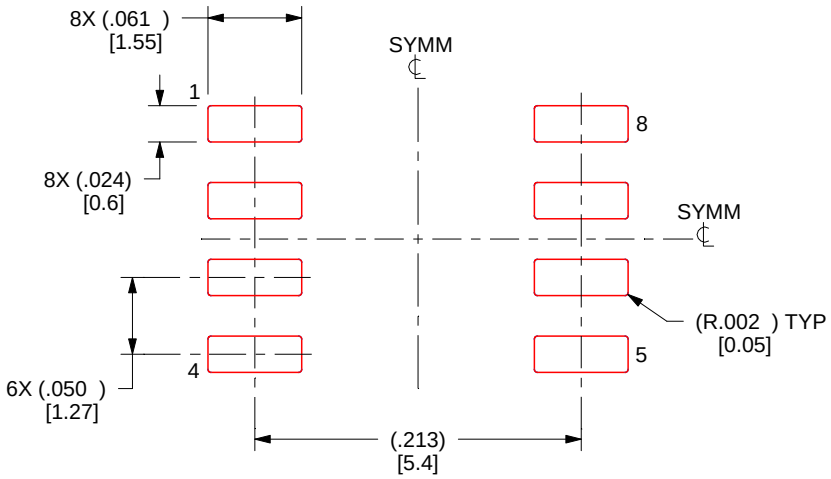
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、 TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

最終更新日：2025 年 10 月