TMUX1219 5V、双方向、2:1 の汎用スイッチ

1 特長

- レール・ツー・レールの動作
- 双方向の信号パス
- 1.8V ロジック互換
- フェイルセーフ・ロジック
- 低いオン抵抗: 3Ω
- 広い電源電圧範囲: 1.08V～5.5V
- -40°C～+125°C の動作温度範囲
- 低い消費電流: 4nA
- 遷移時間: 14ns
- Break-Before-Make のスイッチング動作
- ESD 保護 (HBM): 2000V

2 アプリケーション

- アナログおよびデジタル・スイッチング
- I2C および SPI バスの多重化
- リモート無線ユニット
- バーコード・スキャナ
- モータ・ドライブ
- ビルディング・オートメーション
- アナログ入力モジュール
- パワー・デリバリ
- ビデオ監視
- POS システム
- 家電製品
- コンシューマ・オーディオ

3 概要

TMUX1219 は、汎用の CMOS (相補型金属酸化膜半導体) 単極双投 (SPDT) スイッチです。TMUX1219 は、SEL ピンの状態に基づいて、2 つのソース入力間のスイッチングを行います。1.08V～5.5V の広い動作電源電圧範囲により、個人用電子機器からビルディング・オートメーションまで、幅広い用途に使用可能です。このデバイスは、ソース (Sx) およびドレイン (D) ピンで、GND から V_{DD} までの範囲の双方向アナログおよびデジタル信号をサポートします。消費電流が 4μA と低いため、携帯型アプリケーションで使用できます。

すべてのロジック入力には1.8Vロジック互換のスレッショルドがあり、有効な電源電圧範囲で動作していれば、TTLとCMOSの両方のロジックと互換性が保証されます。フェイルセーフ・ロジック 回路により、電源ピンよりも前に制御ピンに電圧が印加されるため、デバイスへの損傷の可能性が避けられます。

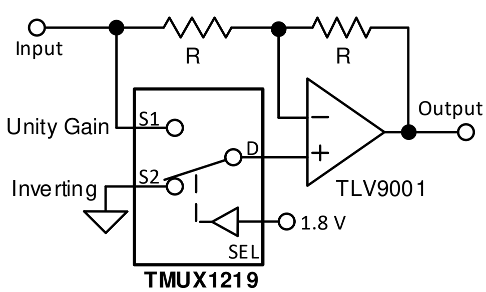
製品情報(1)

型番	パッケージ	本体サイズ(公称)
TMUX1219	SC70 (6)	2.00mm×1.25mm
	SOT-23 (6)(2)	2.90mm×1.60mm

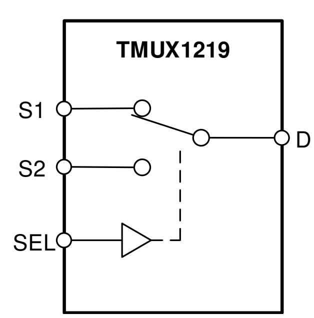
(1) 提供されているすべてのパッケージについては、データシートの末尾にあるパッケージ・オプションについての付録を参照してください。

(2) 製品プレビュー

アプリケーションの例



ブロック図



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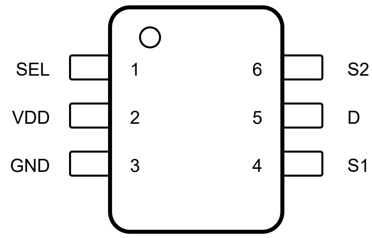
4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

日付	リビジョン	注
2019 年 5 月	*	初版

5 Pin Configuration and Functions

DCK Package
6-Pin SC70
Top View



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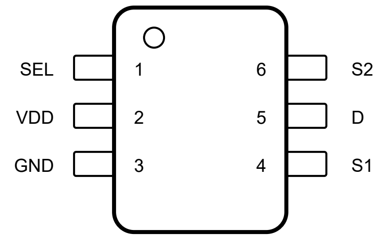
DBV Package
6-Pin SOT-23
Top View



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Product Preview

Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
SEL	1	I	Select pin: controls state of the switch according to 表 1. (Logic Low = S1 to D, Logic High = S2 to D)
VDD	2	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{DD} and GND.
GND	3	P	Ground (0 V) reference
S1	4	I/O	Source pin 1. Can be an input or output.
D	5	I/O	Drain pin. Can be an input or output.
S2	6	I/O	Source pin 2. Can be an input or output.

(1) I = input, O = output, I/O = input and output, P = power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
V_{DD}	Supply voltage	–0.5	6	V
V_{SEL}	Logic control input pin voltage (SEL)	–0.5	6	V
I_{SEL}	Logic control input pin current (SEL)	–30	30	mA
V_S or V_D	Source or drain voltage (Sx, D)	–0.5	V_{DD}+0.5	V
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx, D)	–30	30	mA
T_{stg}	Storage temperature	–65	150	°C
T_J	Junction temperature		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002, all pins(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	1.08		5.5	V
V_S or V_D	Signal path input/output voltage (source or drain pin) (Sx, D)	0		V_{DD}	V
V_{SEL}	Logic control input pin voltage (SEL)	0		5.5	V
T_A	Ambient temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TMUX1219 SC70 (DCK) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	243.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	206.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	128.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	107.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	128.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics (V_{DD} = 5 V ±10 %)

at T_A = 25°C, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to On-Resistance	25°C		3		Ω
			–40°C to +85°C			5	Ω
			–40°C to +125°C			6	Ω
ΔR_{ON}	On-resistance matching between channels	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to On-Resistance	25°C		0.15		Ω
			–40°C to +85°C			0.4	Ω
			–40°C to +125°C			1	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to On-Resistance	25°C		1.5		Ω
			–40°C to +85°C		2		Ω
			–40°C to +125°C		3		Ω
$I_{S(OFF)}$	Source off leakage current[(1)]	V_{DD} = 5 V Switch Off V_D = 4.5 V / 1.5 V V_S = 1.5 V / 4.5 V Refer to Off-Leakage Current	25°C		±5		nA
			–40°C to +85°C	–25		25	nA
			–40°C to +125°C	–40		40	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = 5 V Switch On V_D = V_S = 4.5 V / 1.5 V Refer to On-Leakage Current	25°C		±15		nA
			–40°C to +85°C	–50		50	nA
			–40°C to +125°C	–80		80	nA
LOGIC INPUTS (SEL)							
V_{IH}	Input logic high		–40°C to +125°C	1.49		5.5	V
V_{IL}	Input logic low		–40°C to +125°C	0		0.87	V
I_{IH} I_{IL}	Input leakage current		25°C		±0.005		µA
I_{IH} I_{IL}	Input leakage current		–40°C to +125°C			±0.05	µA
C_{IN}	Logic input capacitance		25°C		1		pF
C_{IN}	Logic input capacitance		–40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Logic inputs = 0 V or 5.5 V	25°C		0.003		µA
			–40°C to +125°C			1.5	µA

(1) When V_S is 4.5 V, V_D is 1.5 V or when V_S is 1.5 V, V_D is 4.5 V.

Electrical Characteristics (V_{DD} = 5 V ±10 %) (continued)

at T_A = 25°C, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Switching time between channels	V_S = 3 V R_L = 200 Ω, C_L = 15 pF Refer to Transition Time	25°C		12		ns
			–40°C to +85°C			18	ns
			–40°C to +125°C			19	ns
t_{OPEN} (BBM)	Break before make time	V_S = 3 V R_L = 200 Ω, C_L = 15 pF Refer to Break-Before-Make	25°C		8		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
Q_C	Charge Injection	V_D = 1 V R_S = 0 Ω, C_L = 1 nF Refer to Charge Injection	25°C		–10		pC
O_{ISO}	Off Isolation	R_L = 50 Ω, C_L = 5 pF f = 1 MHz Refer to Off Isolation	25°C		–65		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz Refer to Off Isolation	25°C		–45		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5 pF f = 1 MHz Refer to Crosstalk	25°C		–65		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz Refer to Crosstalk	25°C		–45		dB
BW	Bandwidth	R_L = 50 Ω, C_L = 5 pF Refer to Bandwidth	25°C		250		MHz
C_{SOFF}	Source off capacitance	f = 1 MHz	25°C		7		pF
C_{SON} C_{DON}	On capacitance	f = 1 MHz	25°C		23		pF

6.6 Electrical Characteristics (V_{DD} = 3.3 V ±10 %)

at T_A = 25°C, V_{DD} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to On-Resistance	25°C		5		Ω
			–40°C to +85°C			10	Ω
			–40°C to +125°C			12	Ω
ΔR_{ON}	On-resistance matching between channels	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to On-Resistance	25°C		0.15		Ω
			–40°C to +85°C			1	Ω
			–40°C to +125°C			1	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to On-Resistance	25°C		3.5		Ω
			–40°C to +85°C		4		Ω
			–40°C to +125°C		5		Ω
$I_{S(OFF)}$	Source off leakage current[1]	V_{DD} = 3.3 V Switch Off V_D = 3 V / 1 V V_S = 1 V / 3 V Refer to Off-Leakage Current	25°C		±5		nA
			–40°C to +85°C	–25		25	nA
			–40°C to +125°C	–40		40	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = 3.3 V Switch On V_D = V_S = 3 V / 1 V Refer to On-Leakage Current	25°C		±15		nA
			–40°C to +85°C	–50		50	nA
			–40°C to +125°C	–80		80	nA
LOGIC INPUTS (SEL)							
V_{IH}	Input logic high		–40°C to +125°C	1.35		5.5	V
V_{IL}	Input logic low		–40°C to +125°C	0		0.8	V
I_{IH} I_{IL}	Input leakage current		25°C		±0.005		µA
I_{IH} I_{IL}	Input leakage current		-40°C to 125°C			±0.05	µA
C_{IN}	Logic input capacitance		25°C		1		pF
C_{IN}	Logic input capacitance		–40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Logic inputs = 0 V or 5.5 V	25°C		0.003		µA
			–40°C to +125°C			0.8	µA

(1) When V_S is 3 V, V_D is 1 V or when V_S is 1 V, V_D is 3 V.

Electrical Characteristics (V_{DD} = 3.3 V ±10 %) (continued)

at T_A = 25°C, V_{DD} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Switching time between channels	V_S = 2 V R_L = 200 Ω, C_L = 15 pF Refer to Transition Time	25°C		14		ns
			–40°C to +85°C			20	ns
			–40°C to +125°C			21	ns
t_{OPEN} (BBM)	Break before make time	V_S = 2 V R_L = 200 Ω, C_L = 15 pF Refer to Break-Before-Make	25°C		9		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
Q_C	Charge Injection	V_D = 1 V R_S = 0 Ω, C_L = 1 nF Refer to Charge Injection	25°C		–6		pC
O_{ISO}	Off Isolation	R_L = 50 Ω, C_L = 5 pF f = 1 MHz Refer to Off Isolation	25°C		–65		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz Refer to Off Isolation	25°C		–45		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5 pF f = 1 MHz Refer to Crosstalk	25°C		–65		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz Refer to Crosstalk	25°C		–45		dB
BW	Bandwidth	R_L = 50 Ω, C_L = 5 pF Refer to Bandwidth	25°C		250		MHz
C_{SOFF}	Source off capacitance	f = 1 MHz	25°C		7		pF
C_{SON} C_{DON}	On capacitance	f = 1 MHz	25°C		23		pF

6.7 Electrical Characteristics (V_{DD} = 1.8 V ±10 %)

at T_A = 25°C, V_{DD} = 1.8 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to On-Resistance	25°C		40		Ω
			–40°C to +85°C			80	Ω
			–40°C to +125°C			80	Ω
ΔR_{ON}	On-resistance matching between channels	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to On-Resistance	25°C		0.4		Ω
			–40°C to +85°C			1.5	Ω
			–40°C to +125°C			1.5	Ω
$I_{S(OFF)}$	Source off leakage current[(1)]	V_{DD} = 1.98 V Switch Off V_D = 1.62 V / 1 V V_S = 1 V / 1.62 V Refer to Off-Leakage Current	25°C		±5		nA
			–40°C to +85°C	–25		25	nA
			–40°C to +125°C	–40		40	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = 1.98 V Switch On V_D = V_S = 1.62 V / 1 V Refer to On-Leakage Current	25°C		±15		nA
			–40°C to +85°C	–50		50	nA
			–40°C to +125°C	–80		80	nA
LOGIC INPUTS (SEL)							
V_{IH}	Input logic high		–40°C to +125°C	1.07		5.5	V
V_{IL}	Input logic low		–40°C to +125°C	0		0.68	V
I_{IH} I_{IL}	Input leakage current		25°C		±0.005		µA
I_{IH} I_{IL}	Input leakage current		–40°C to +125°C			±0.05	µA
C_{IN}	Logic input capacitance		25°C		1		pF
C_{IN}	Logic input capacitance		–40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Logic inputs = 0 V or 5.5 V	25°C		0.001		µA
			–40°C to +125°C			0.6	µA

(1) When V_S is 1.62 V, V_D is 1 V or when V_S is 1 V, V_D is 1.62 V.

Electrical Characteristics (V_{DD} = 1.8 V ±10 %) (continued)

at T_A = 25°C, V_{DD} = 1.8 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Transition time between channels	V_S = 1 V R_L = 200 Ω, C_L = 15 pF Refer to Transition Time	25°C		28		ns
			–40°C to +85°C			44	ns
			–40°C to +125°C			44	ns
t_{OPEN} (BBM)	Break before make time	V_S = 1 V R_L = 200 Ω, C_L = 15 pF Refer to Break-Before-Make	25°C		16		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
Q_C	Charge Injection	V_D = 1 V R_S = 0 Ω, C_L = 1 nF Refer to Charge Injection	25°C		–3		pC
O_{ISO}	Off Isolation	R_L = 50 Ω, C_L = 5 pF f = 1 MHz Refer to Off Isolation	25°C		–65		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz Refer to Off Isolation	25°C		–45		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5 pF f = 1 MHz Refer to Crosstalk	25°C		–65		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz Refer to Crosstalk	25°C		–45		dB
BW	Bandwidth	R_L = 50 Ω, C_L = 5 pF	25°C		250		MHz
C_{SOFF}	Source off capacitance	f = 1 MHz	25°C		7		pF
C_{SON} C_{DON}	On capacitance	f = 1 MHz	25°C		23		pF

6.8 Electrical Characteristics (V_{DD} = 1.2 V ±10 %)

at T_A = 25°C, V_{DD} = 1.2 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to On-Resistance	25°C		70		Ω
			–40°C to +85°C			105	Ω
			–40°C to +125°C			105	Ω
ΔR_{ON}	On-resistance matching between channels	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to On-Resistance	25°C		0.4		Ω
			–40°C to +85°C			1.5	Ω
			–40°C to +125°C			1.5	Ω
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 1.32 V Switch Off V_D = 1 V / 0.8 V V_S = 0.8 V / 1 V Refer to Off-Leakage Current	25°C		±5		nA
			–40°C to +85°C	–25		25	nA
			–40°C to +125°C	–40		40	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = 1.32 V Switch On V_D = V_S = 1 V / 0.8 V Refer to On-Leakage Current	25°C		±15		nA
			–40°C to +85°C	–50		50	nA
			–40°C to +125°C	–80		80	nA
LOGIC INPUTS (SEL)							
V_{IH}	Input logic high		–40°C to +125°C	0.96		5.5	V
V_{IL}	Input logic low		–40°C to +125°C	0		0.36	V
I_{IH} I_{IL}	Input leakage current		25°C		±0.005		µA
I_{IH} I_{IL}	Input leakage current		–40°C to +125°C			±0.05	µA
C_{IN}	Logic input capacitance		25°C		1		pF
C_{IN}	Logic input capacitance		–40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Logic inputs = 0 V or 5.5 V	25°C		0.003		µA
			–40°C to +125°C			0.5	µA

(1) When V_S is 1 V, V_D is 0.8 V or when V_S is 0.8 V, V_D is 1 V.

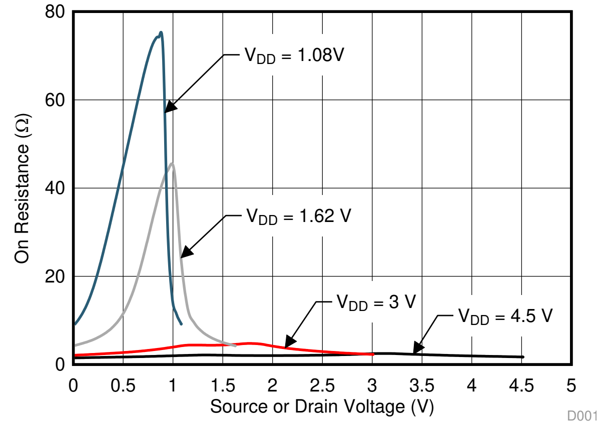
Electrical Characteristics (V_{DD} = 1.2 V ±10 %) (continued)

at T_A = 25°C, V_{DD} = 1.2 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Transition time between channels	V_S = 1 V R_L = 200 Ω, C_L = 15 pF Refer to Transition Time	25°C		55		ns
			–40°C to +85°C			190	ns
			–40°C to +125°C			190	ns
t_{OPEN} (BBM)	Break before make time	V_S = 1 V R_L = 200 Ω, C_L = 15 pF Refer to Break-Before-Make	25°C		28		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
Q_C	Charge Injection	V_D = 1 V R_S = 0 Ω, C_L = 1 nF Refer to Charge Injection	25°C		–2		pC
O_{ISO}	Off Isolation	R_L = 50 Ω, C_L = 5 pF f = 1 MHz Refer to Off Isolation	25°C		–65		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz Refer to Off Isolation	25°C		–45		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5 pF f = 1 MHz Refer to Crosstalk	25°C		–65		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz Refer to Crosstalk	25°C		–45		dB
BW	Bandwidth	R_L = 50 Ω, C_L = 5 pF	25°C		250		MHz
C_{SOFF}	Source off capacitance	f = 1 MHz	25°C		7		pF
C_{SON} C_{DON}	On capacitance	f = 1 MHz	25°C		23		pF

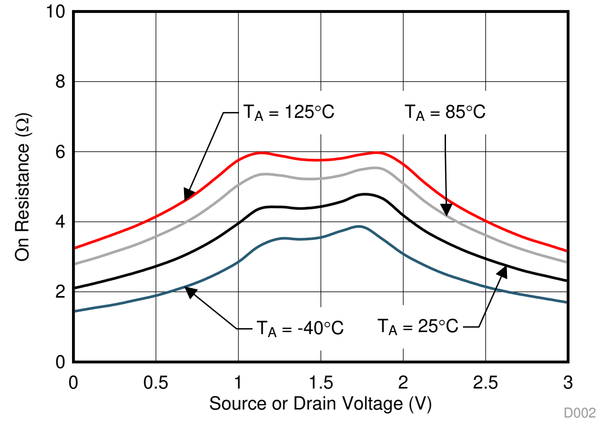
6.9 Typical Characteristics

at T_A = 25°C, V_{DD} = 5 V (unless otherwise noted)



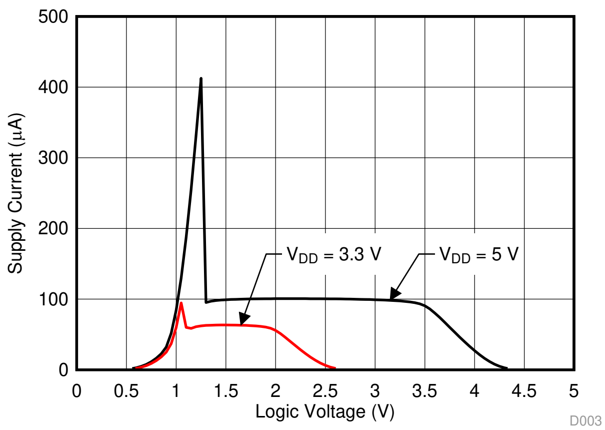
T_A = 25°C

図 1. On-Resistance vs Source or Drain Voltage



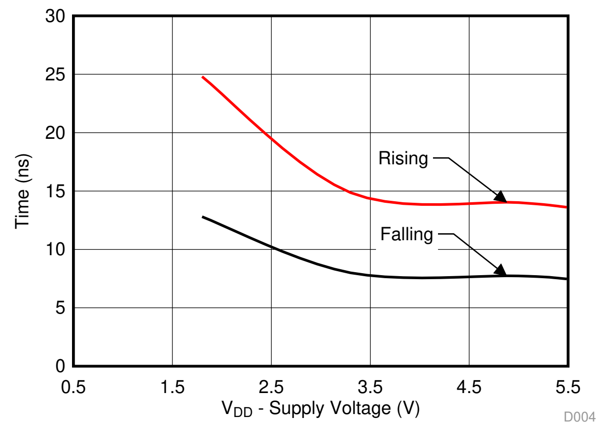
V_{DD} = 3 V

図 2. On-Resistance vs Source or Drain Voltage



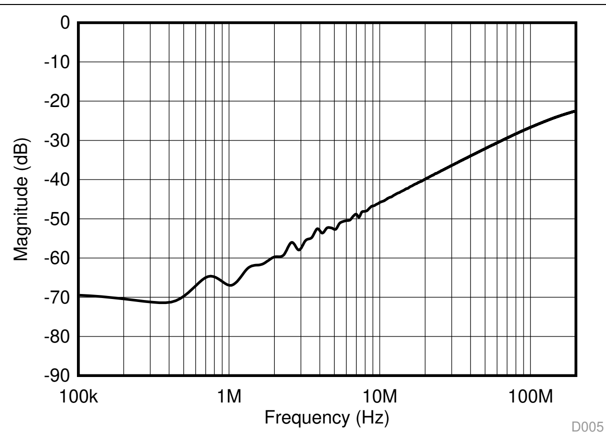
T_A = 25°C

図 3. Supply Current vs Logic Voltage



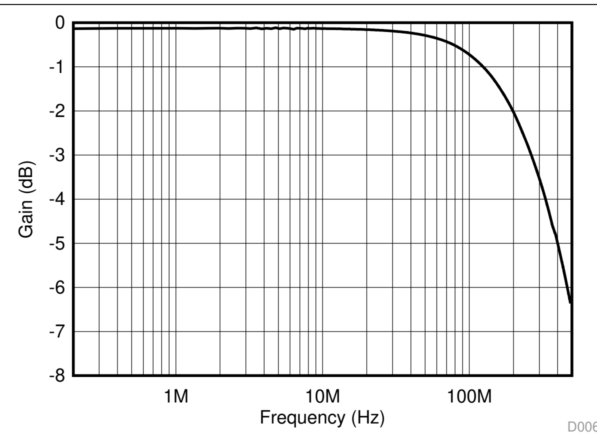
T_A = 25°C

図 4. $T_{transition}$ vs Supply Voltage



T_A = 25°C

図 5. Crosstalk and Off-Isolation vs Frequency



T_A = 25°C

図 6. Frequency Response

7 Parameter Measurement Information

7.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (D) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. The measurement setup used to measure R_{ON} is shown in 図 7. Voltage (V) and current (I_{SD}) are measured using this setup, and R_{ON} is computed with R_{ON} = V / I_{SD}:

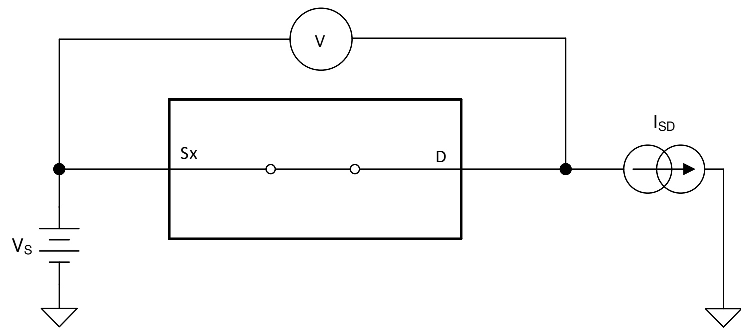


図 7. On-Resistance Measurement Setup

7.2 Off-Leakage Current

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

The setup used to measure off-leakage current is shown in 図 8.

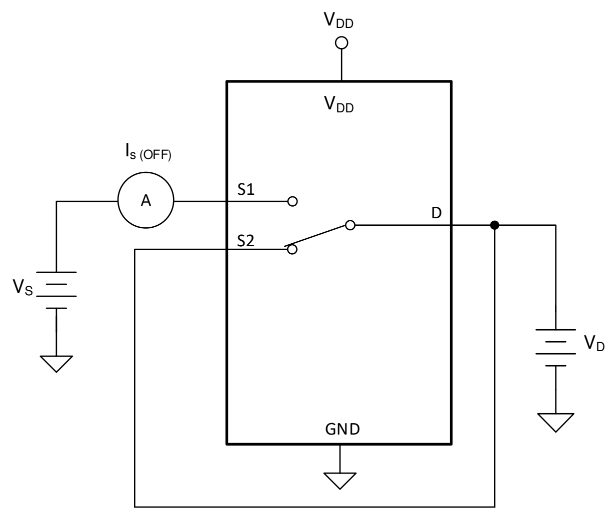


図 8. Off-Leakage Measurement Setup

7.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$.

Either the source pin or drain pin is left floating during the measurement. 図 9 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

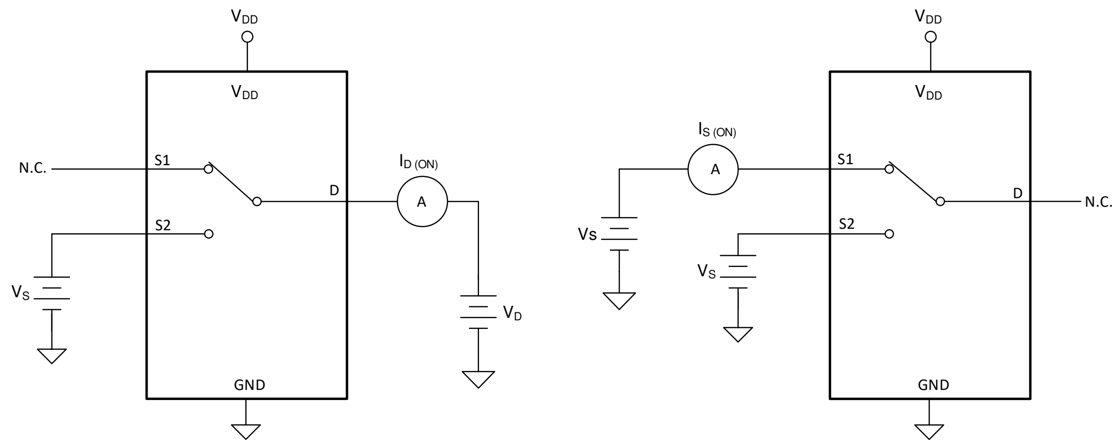


図 9. On-Leakage Measurement Setup

7.4 Transition Time

Transition time is defined as the time taken by the output of the device to rise or fall 10% after the logic control signal has risen or fallen past the logic threshold. The 10% transition measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. 図 10 shows the setup used to measure transition time, denoted by the symbol $t_{TRANSITION}$.

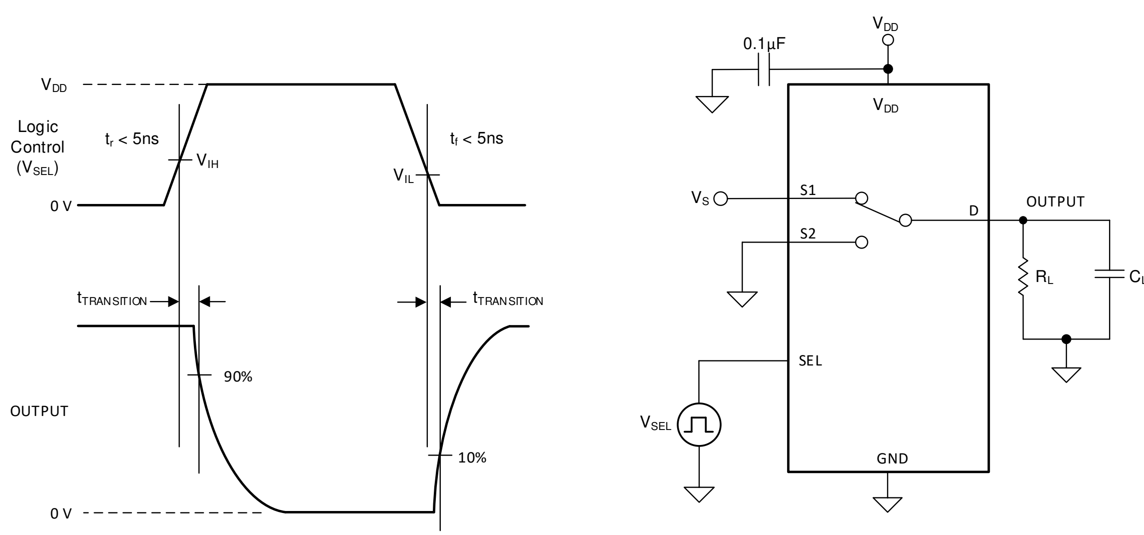


図 10. Transition-Time Measurement Setup

7.5 Break-Before-Make

Break-before-make delay is a safety feature that prevents two inputs from connecting when the device is switching. The output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. 図 11 shows the setup used to measure break-before-make delay, denoted by the symbol $t_{OPEN(BBM)}$.

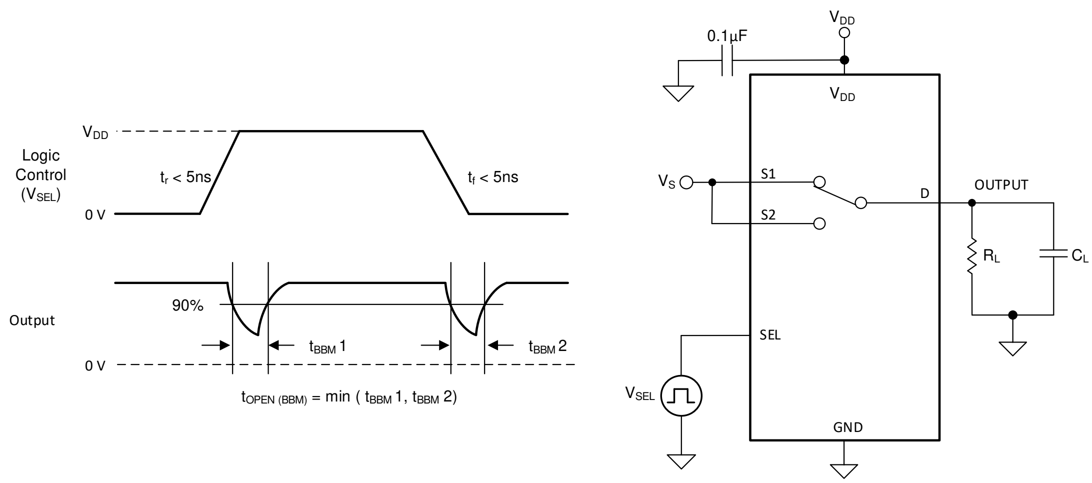


図 11. Break-Before-Make Delay Measurement Setup

7.6 Charge Injection

The TMUX1219 has a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_C. 図 12 shows the setup used to measure charge injection from Drain (D) to Source (Sx).

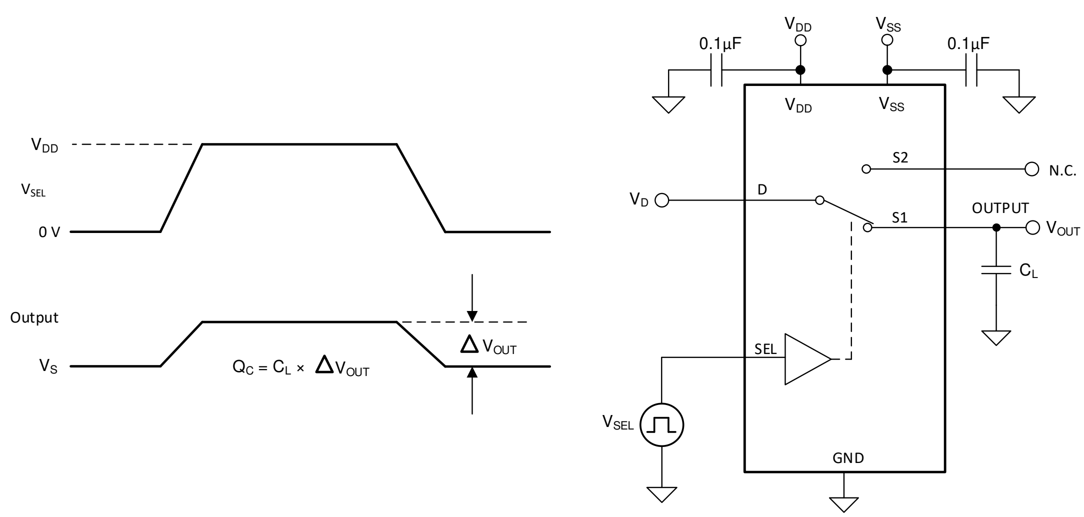


図 12. Charge-Injection Measurement Setup

7.7 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (D) of the device when a signal is applied to the source pin (Sx) of an off-channel. 図 13 shows the setup used to measure, and the equation used to calculate off isolation.

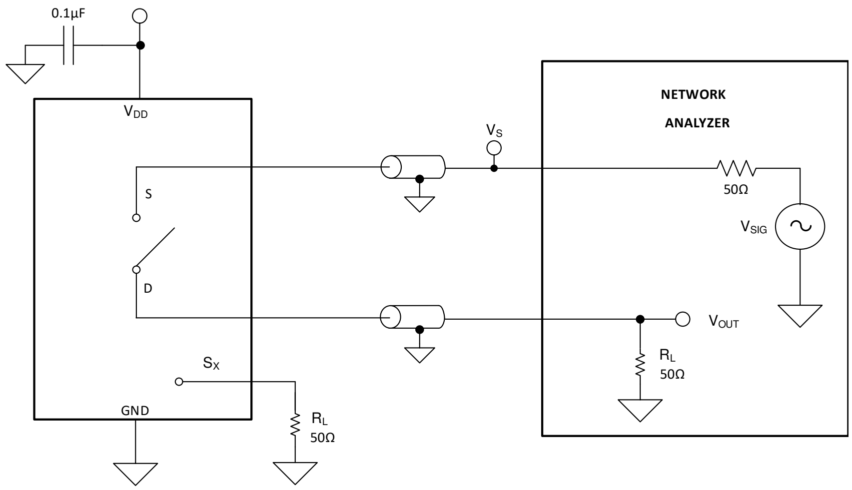


図 13. Off Isolation Measurement Setup

$$\text{Off Isolation} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \quad (1)$$

7.8 Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (D) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. 図 14 shows the setup used to measure, and the equation used to calculate crosstalk.

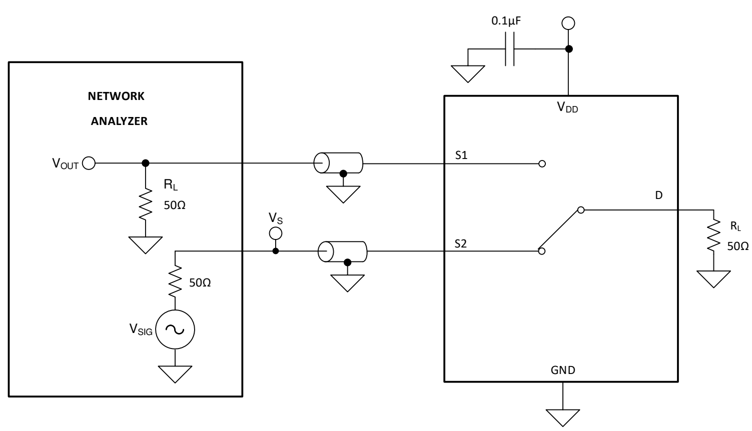


図 14. Crosstalk Measurement Setup

$$\text{Channel-to-Channel Crosstalk} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \quad (2)$$

7.9 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (D) of the device. 図 15 shows the setup used to measure bandwidth.

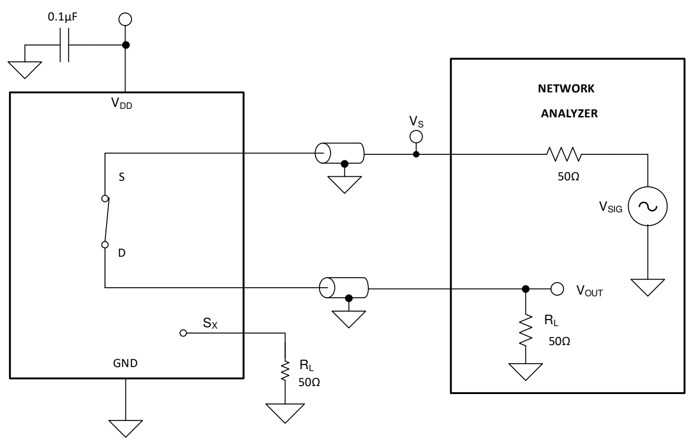


図 15. Bandwidth Measurement Setup

8 Detailed Description

8.1 Functional Block Diagram

The TMUX1219 is an 2:1 (SPDT), 1-channel switch where the input is controlled with a single select (SEL) control pin.

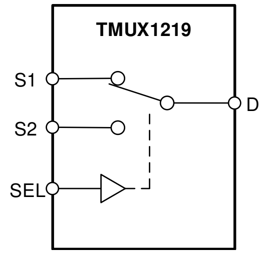


図 16. TMUX1219 Functional Block Diagram

8.2 Feature Description

8.2.1 Bidirectional Operation

The TMUX1219 conducts equally well from source (Sx) to drain (D) or from drain (D) to source (Sx). The device has very similar characteristics in both directions and supports both analog and digital signals.

8.2.2 Rail to Rail Operation

The valid signal path input/output voltage for TMUX1219 ranges from GND to V_{DD}.

8.2.3 1.8 V Logic Compatible Inputs

The TMUX1219 has 1.8-V logic compatible control for the logic control input (SEL). The logic input threshold scales with supply but still provides 1.8-V logic control when operating at 5.5 V supply voltage. 1.8-V logic level inputs allow the TMUX1219 to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. For more information on 1.8 V logic implementations refer to *Simplifying Design with 1.8 V logic Muxes and Switches*

8.2.4 Fail-Safe Logic

The TMUX1219 supports Fail-Safe Logic on the control input pin (SEL) allowing for operation up to 5.5 V, regardless of the state of the supply pin. This feature allows voltages on the control pin to be applied before the supply pin, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins. For example, the Fail-Safe Logic feature allows the select pin of the TMUX1219 to be ramped to 5.5 V while V_{DD} = 0 V. Additionally, the feature enables operation of the TMUX1219 with V_{DD} = 1.2 V while allowing the select pin to interface with a logic level of another device up to 5.5 V.

8.3 Device Functional Modes

The select (SEL) pin of the TMUX1219 controls which source channel is connected to the drain of the device. When a signal path is not selected, that source pin is in high impedance mode (HI-Z). The control pin can be as high as 5.5 V.

8.4 Truth Tables

表 1. TMUX1219 Truth Table

CONTROL LOGIC (SEL)	Selected Source (Sx) Connected To Drain (D) Pin
0	S1
1	S2

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TMUX12xx family offers good system performance across a wide operating supply (1.08V to 5.5V). These devices include 1.8V logic compatible control input pins that enable operation in systems with 1.8V I/O rails. Additionally, the control input pin supports Fail-Safe Logic which allows for operation up to 5.5V, regardless of the state of the supply pin. This protection stops the logic pins from back-powering the supply rail. These features of the TMUX12xx, a family of general purpose multiplexers and switches, reduce system complexity, board size, and overall system cost.

9.2 Typical Application

9.2.1 Switchable Operational Amplifier Gain Setting

One example application of the TMUX1219 is to change an Op Amp from unity gain setting to an inverting amplifier configuration. Utilizing a switch allows a system to have a configurable gain and allows the same architecture to be utilized across the board for various inputs to the system. 図 17 shows the TMUX1219 configured for gain setting application.

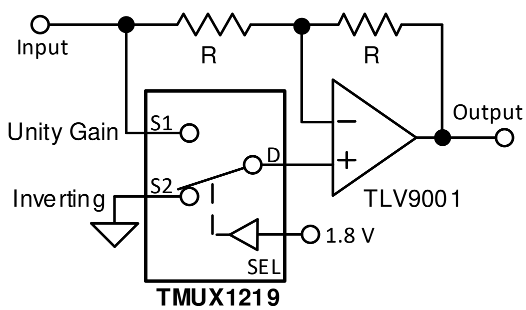


図 17. Switchable Op Amp Gain Setting

9.2.1.1 Design Requirements

This design example uses the parameters listed in 表 2.

表 2. Design Parameters

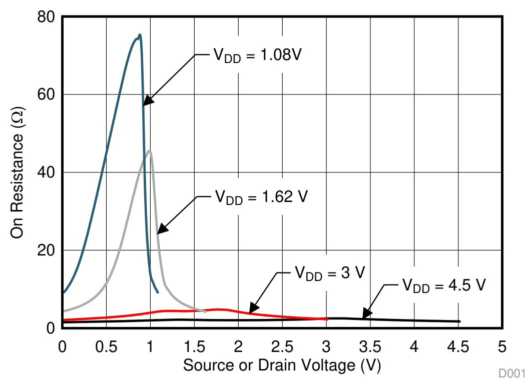
PARAMETERS	VALUES
Input Signal	0 V to 2.75 V
Mux Supply (V_{DD})	2.75 V
Op Amp Supply (V_+/ V_-)	±2.75 V
Mux I/O signal range	0 V to V_{DD} (Rail to Rail)
Control logic thresholds	1.8 V compatible (up to 5.5V)

9.2.1.2 Detailed Design Procedure

The application shown in 図 17 demonstrates how to use a single control input and toggle between gain settings of -1 and +1. If switching between inverting and unity gain is not required, the TMUX1219 can be utilized in the feedback path to select different feedback resistors and provide scalable gain settings for configurable signal conditioning.

The TMUX1219 can be operated without any external components except for the supply decoupling capacitors. The select pin is recommended to have a weak pull-down or pull-up resistor to ensure the input is in a known state. All inputs to the switch must fall within the recommend operating conditions of the TMUX1219 including signal range and continuous current. For this design with a supply of 2.75 V the signal range can be 0 V to 2.75 V and the max continuous current can be 30 mA.

9.2.1.3 Application Curve



T_A = 25°C

図 18. On-Resistance vs Source or Drain Voltage

9.2.2 Input Control for Power Amplifier

Another application of the TMUX1219 is for input control of a power amplifier. Utilizing a switch allows a system to control when the DAC is connected to the power amplifier, and can stop biasing the power amplifier by switching the gate to GND. 図 19 shows the TMUX1219 configured for control of the power amplifier.

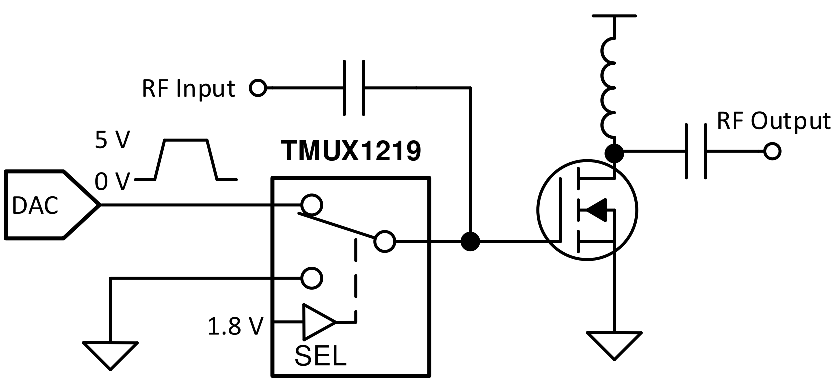


図 19. Input Control of Power Amplifier

9.2.2.1 Design Requirements

This design example uses the parameters listed in 表 2.

表 3. Design Parameters

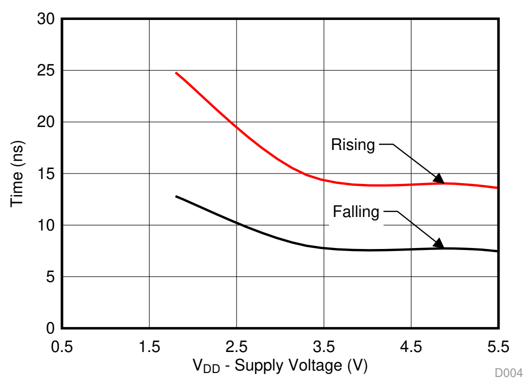
PARAMETERS	VALUES
Supply (V_{DD})	5 V
Mux I/O signal range	0 V to V_{DD} (Rail to Rail)
Control logic thresholds	1.8 V compatible (up to 5.5V)

9.2.2.2 Detailed Design Procedure

The application shown in 図 19 demonstrates how to toggle between the DAC output and GND for control of a power amplifier using a single control input. The DAC output is utilized to bias the gate of the power amplifier and can be disconnected from the circuit using the select pin of the switch. The TMUX1219 can support 1.8-V logic signals on the control input, allowing the device to interface with low logic controls of an FPGA or MCU. The TMUX1219 can be operated without any external components except for the supply decoupling capacitors. The select pin is recommended to have a weak pull-down or pull-up resistor to ensure the input is in a known state. All inputs to the switch must fall within the recommend operating conditions of the TMUX1219 including signal range and continuous current. For this design with a supply of 5 V the signal range can be 0 V to 5 V and the max continuous current can be 30 mA.

9.2.2.3 Application Curve

A key parameter for this application is the transition time of the device. Faster transition time allows the system to toggle between input sources at a faster rate and allows the output to settle to the final value. The TMUX1219 has a transition time that varies with supply voltage and is shown in 図 20



T_A = 25°C

図 20. $T_{transition}$ vs Supply Voltage

10 Power Supply Recommendations

The TMUX1219 operates across a wide supply range of 1.08 V to 5.5 V. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the V_{DD} supply to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 µF to 10 µF from V_{DD} to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes.

11 Layout

11.1 Layout Guidelines

11.1.1 Layout Information

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. 図 21 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

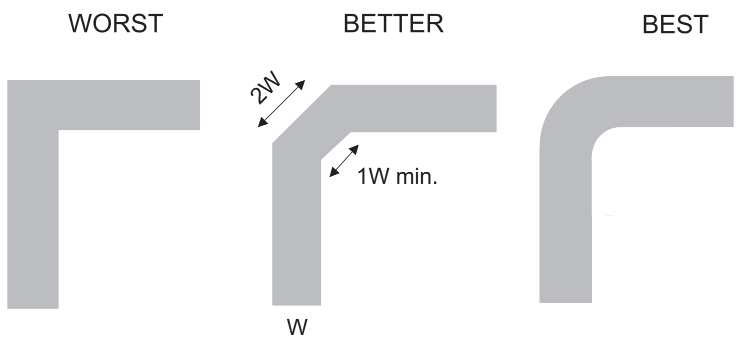


図 21. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

図 22 illustrates an example of a PCB layout with the TMUX1219. Some key considerations are:

- Decouple the V_{DD} pin with a 0.1-µF capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the V_{DD} supply.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

11.2 Layout Example

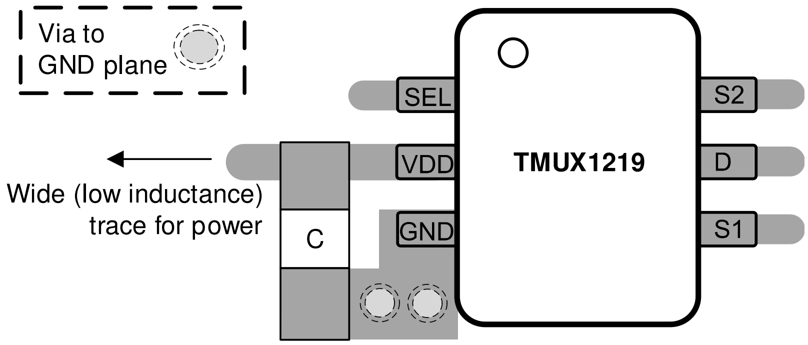


図 22. TMUX1219 Layout Example

12 デバイスおよびドキュメントのサポート

12.1 ドキュメントのサポート

12.1.1 関連資料

テキサス・インスツルメンツ、*『低CONマルチプレクサにおける安定性の問題の改善』*

テキサス・インスツルメンツ、*『1.8Vロジックのマルチプレクサおよびスイッチにおける設計の単純化』*

テキサス・インスツルメンツ、*『電源オフ保護を備えた信号スイッチで電源シーケンスを不要に』*

テキサス・インスツルメンツ、*『高電圧アナログ・マルチプレクサのシステムレベル保護』*

12.2 ドキュメントの更新通知を受け取る方法

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12.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 商標

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12.5 静電気放電に関する注意事項

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静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMUX1219DBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	26IT
TMUX1219DBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	26IT
TMUX1219DBVRG4	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	26IT
TMUX1219DBVRG4.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	26IT
TMUX1219DCKR	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1F5
TMUX1219DCKR.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1F5
TMUX1219DCKRG4	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1F5
TMUX1219DCKRG4.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1F5

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TMUX1219 :

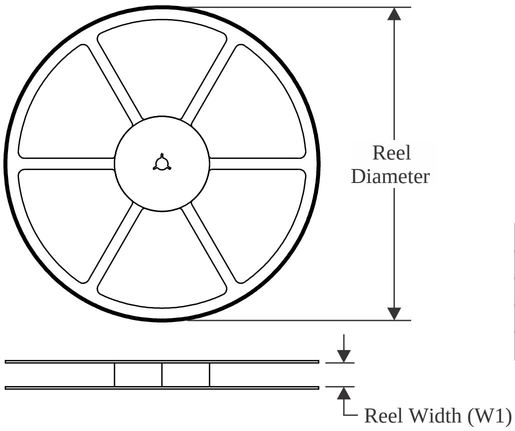
- Automotive : TMUX1219-Q1

NOTE: Qualified Version Definitions:

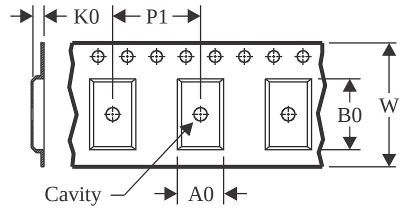
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

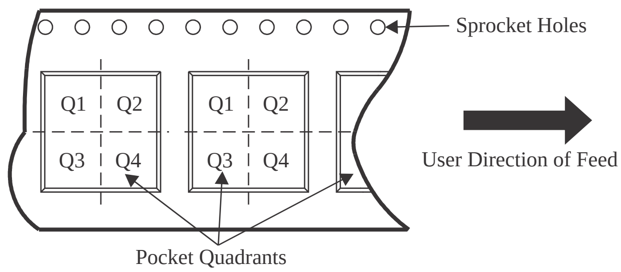


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

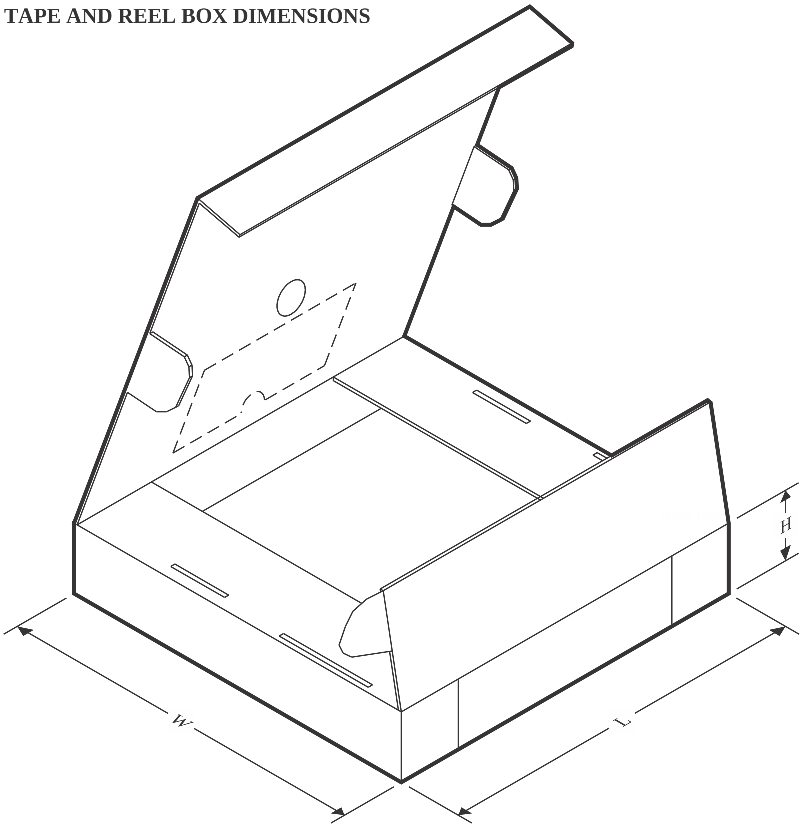
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

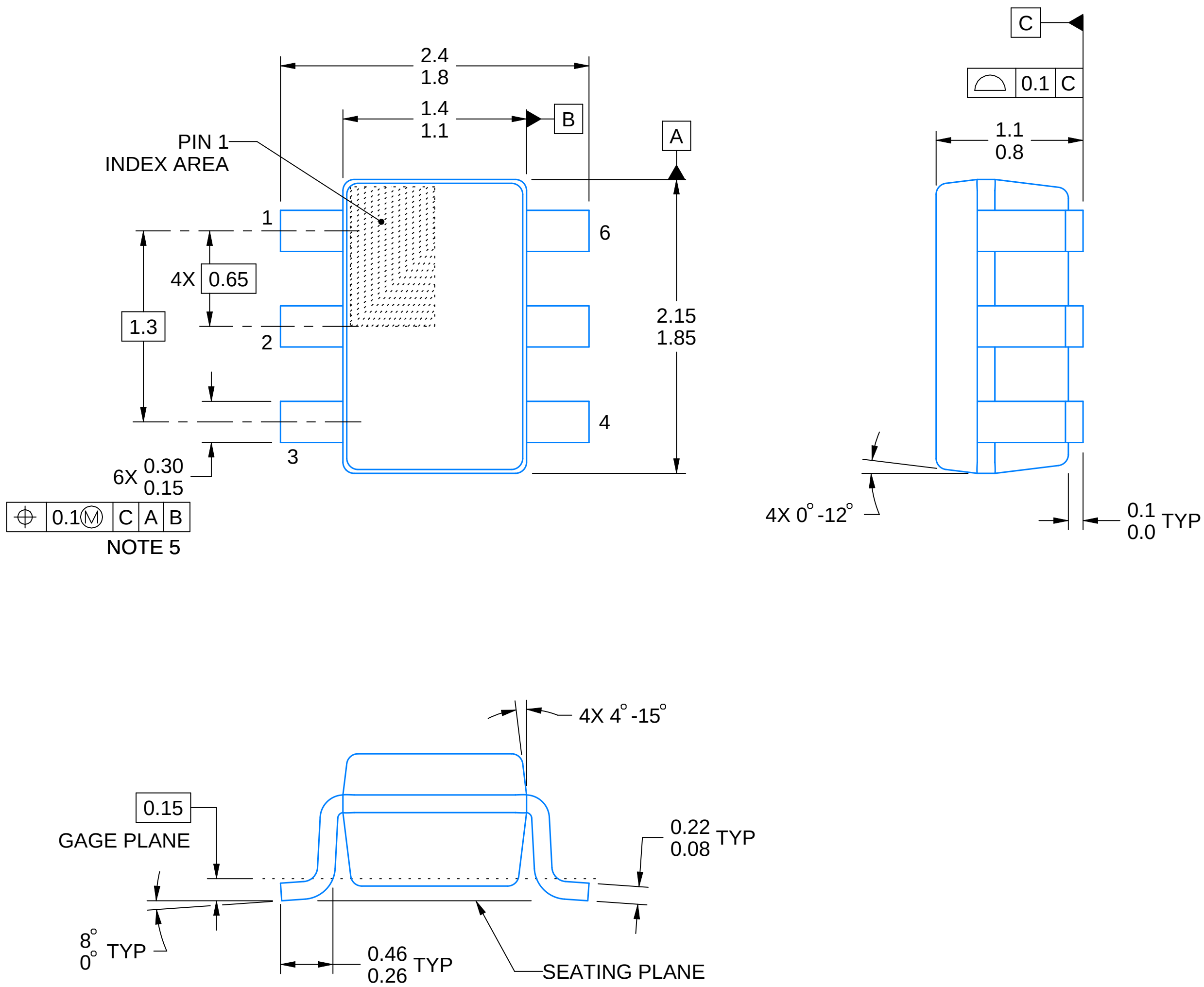
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX1219DBVR	SOT-23	DBV	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TMUX1219DBVRG4	SOT-23	DBV	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TMUX1219DCKR	SC70	DCK	6	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
TMUX1219DCKRG4	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX1219DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TMUX1219DBVRG4	SOT-23	DBV	6	3000	180.0	180.0	18.0
TMUX1219DCKR	SC70	DCK	6	3000	210.0	185.0	35.0
TMUX1219DCKRG4	SC70	DCK	6	3000	180.0	180.0	18.0



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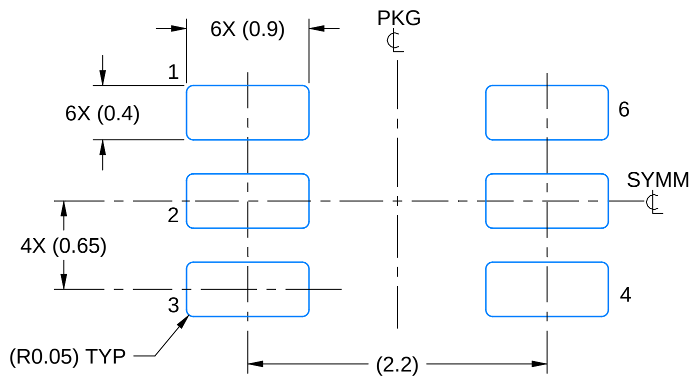
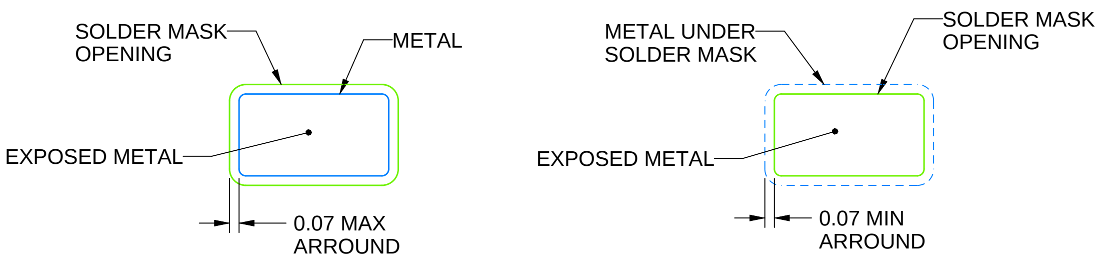
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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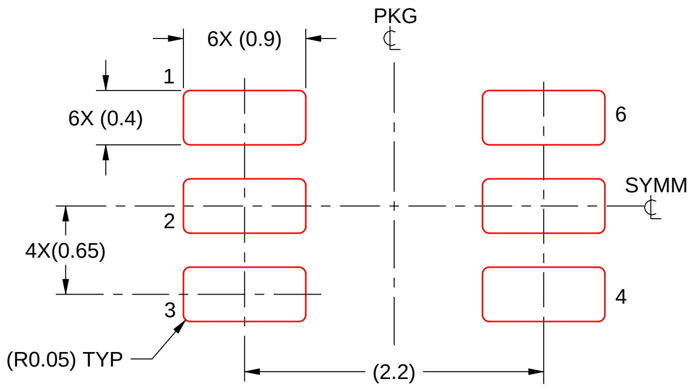
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

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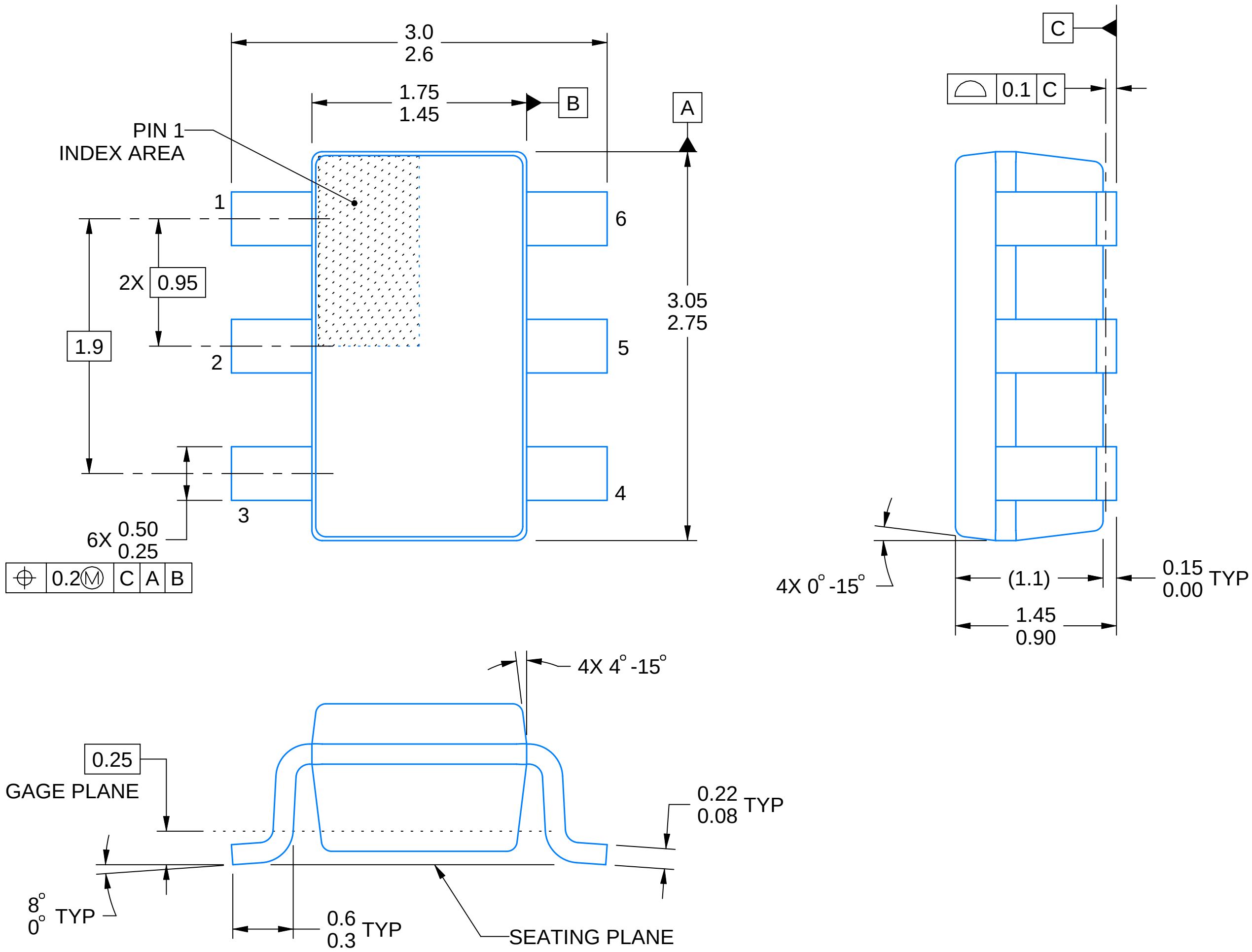
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



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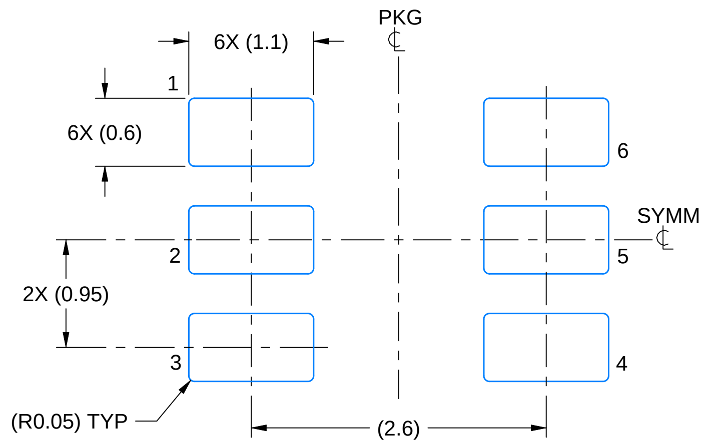
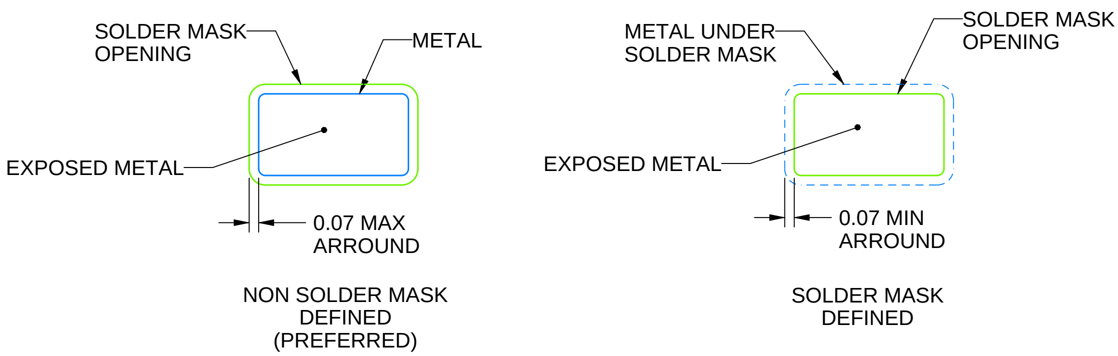
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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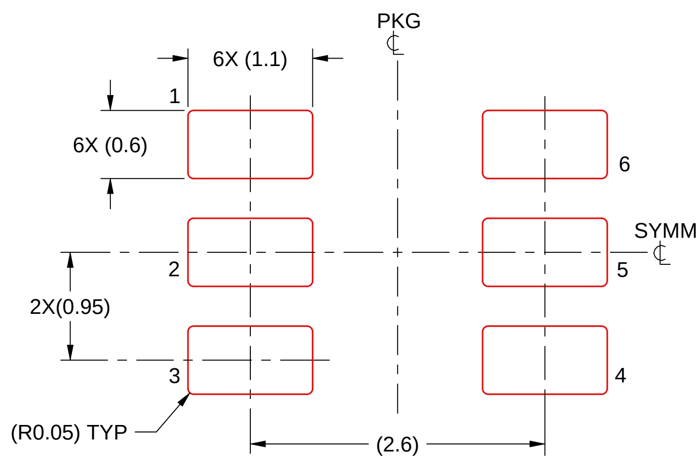
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月