TPD4S480 USB Type-C® 48V EPR ポート プロテクタ：VBUS への短絡過電圧および IEC ESD 保護

1 特長

- 4 チャネルの V_{BUS} への短絡過電圧保護 (CC1、CC2、SBU1、SBU2)：63V_{DC} 許容
- 4 チャネルの IEC 61000-4-2 ESD 保護 (CC1、CC2、SBU1、SBU2)
- CC1 および CC2 過電圧保護 FET：V_{CONN} 電力用
- CC ピンの ±65V サージ保護
- SBU ピンの +65V/-35V サージ保護
- EPR レベル V_{BUS} を分割するためのイネーブルを搭載した内蔵 VBUS 分周回路
- 外部 EPR ブロッキング FET 制御用の FET ドライバを内蔵
- CC デッド バッテリ抵抗の内蔵により、モバイル デバイスでのデッド バッテリ状況に対応
- 3mm × 3mm QFN パッケージ

2 アプリケーション

- デスクトップ PC / マザーボード
- 標準的ノート PC
- Chromebook と WOA (Windows on Arm)
- ドッキング ステーション
- ポート / ケーブル アダプタとドングル
- スマートフォン

3 概要

TPD4S480 は、シングル チップの USB Type-C ポート保護デバイスで、48V の V_{BUS} への短絡過電圧および IEC ESD 保護を行います。

USB Type-C コネクタのリリース以降、USB Type-C 用でありながら、USB Type-C の仕様を満たしていない多くの製品やアクセサリがリリースされました。このような例の 1 つに USB Type-C パワー デリバリ アダプタがありますが、これは V_{BUS} ライン上にしか高電圧を印加しません。USB Type-C に関する別の懸念として、小さなコネクタのピンが互いに近接して配置されているため、コネクタの機械的なねじれや水平方向のずれによってピン間が短絡することがあります。これによって、48V V_{BUS} が CC および SBU ピンと短絡するおそれがあります。また、Type-C コネクタのピンが互いに近接して配置されていることから、破片や湿気により 48V V_{BUS} ピンが CC および SBU ピンと短絡する危険も高まっています。

これらの理想的でない機器や機械的事象が存在するため、CC および SBU ピンは 5V 以下の電圧でのみ動作するにもかかわらず、48V 許容にする必要があります。TPD4S480 は CC および SBU ピンの過電圧保護を行うため、通常の動作に影響を与えずに CC および SBU ピンを 48V 許容にできます。このデバイスは、SBU および CC ラインと直列に高電圧 FET を配置します。OVP スレッショルドを超える電圧がこれらのラインに検出された場合、高電圧スイッチが開き、システムの他の部分を、コネクタに存在している高電圧の状況から絶縁します。

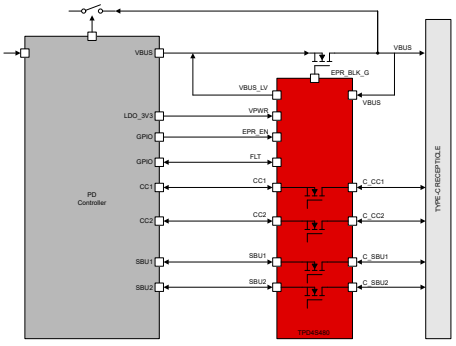
内蔵の VBUS 分圧回路と FET ドライバにより、EPR 動作に適した定格を持たない PD コントローラでも EPR 電圧範囲で安全に動作することができます。GPIO でイネーブルにしたとき、または V_{BUS} が 24V を超えたとき自動的に、TPD4S480 はオプションの外部ブロッキング FET をディセーブルし、分圧器をイネーブルします。この動作により、20V 定格の PD コントローラが保護されるため、既存の V_{BUS} センス回路を使用できます。

最後に、ほとんどのシステムでは外部ピンについて IEC 61000-4-2 システム レベルの ESD 保護が必要です。TPD4S480 には、CC1、CC2、SBU1、SBU2 ピンの IEC 61000-4-2 ESD 保護が内蔵されているため、コネクタの外部に高電圧 TVS ダイオードを配置する必要がありません。

パッケージ情報 (1)

部品番号	パッケージ	本体サイズ (公称)
TPD4S480	RUK (WQFN、20)	3mm × 3mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



CC および SBU の過電圧保護

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4 Pin Configuration and Functions

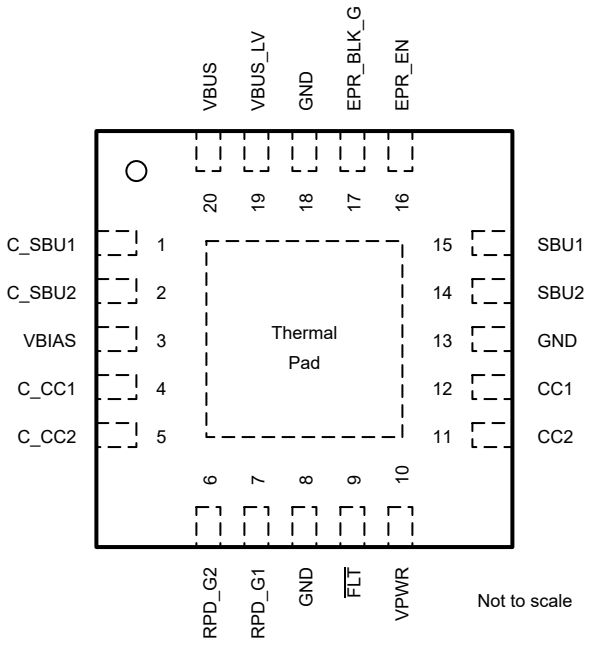


図 4-1. RUK Package 20-Pin QFN

表 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
12	CC1	I/O	System side of the CC1 OVP FET. Connect to either CC pin of the CC/PD controller.
11	CC2	I/O	System side of the CC2 OVP FET. Connect to either CC pin of the CC/PD controller.
4	C_CC1	I/O	Connector side of the CC1 OVP FET. Connect to either CC pin of the USB Type-C connector.
5	C_CC2	I/O	Connector side of the CC2 OVP FET. Connect to either CC pin of the USB Type-C connector.
1	C_SBU1	I/O	Connector side of the SBU1 OVP FET. Connect to either SBU pin of the USB Type-C connector. Alternatively, connect to either USB2.0 pin of the USB Type-C connector to protect the USB2.0 pins instead of the SBU pins.
2	C_SBU2	I/O	Connector side of the SBU2 OVP FET. Connect to either SBU pin of the USB Type-C connector. Alternatively, connect to either USB2.0 pin of the USB Type-C connector to protect the USB2.0 pins instead of the SBU pins.
15	SBU1	I/O	System side of the SBU1 OVP FET. Connect to either SBU pin of the SBU MUX. Alternatively, connect to either USB2.0 pin of the USB2.0 Phy when protecting the USB2.0 pins instead of protecting the SBU pins.
14	SBU2	I/O	System side of the SBU2 OVP FET. Connect to either SBU pin of the SBU MUX. Alternatively, connect to either USB2.0 pin of the USB2.0 Phy when protecting the USB2.0 pins instead of protecting the SBU pins.
7	RPD_G1	I/O	Short to C_CC1 if dead battery resistors are needed. If dead battery resistors are not needed, short pin to GND.
6	RPD_G2	I/O	Short to C_CC2 if dead battery resistors are needed. If dead battery resistors are not needed, short pin to GND.
9	$\overline{\text{FLT}}$	O	Open drain for fault reporting.

表 4-1. Pin Functions (続き)

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
8, 13, 18	GND	GND	Ground
3	VBIAS	P	Pin for ESD support capacitor. Place a 0.1-µF capacitor on this pin to ground.
10	VPWR	P	2.7V to 4.5V power supply.
20	VBUS	I	Input for EPR VBUS divider. Tie to USB-C receptacle VBUS pins.
19	VBUS_LV	O	Output of EPR VBUS divider. When EPR_EN is asserted, VBUS_LV is divided down voltage from VBUS. When EPR_EN is de-asserted VBUS_LV is equal to VBUS.
16	EPR_EN	I	EPR mode enable input. When asserted EPR_BLK_G is disabled and VBUS_LV is divided VBUS.
17	EPR_BLK_G	O	Gate driver output to optional VBUS blocking FET. FET is enabled when in SPR mode and disabled in EPR mode.
-	Thermal Pad	GND	Internally connected to GND. Used as a heatsink. Connect to the PCB GND plane

(1) I = input, O = output, I/O = input and output, GND = ground, P = power

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_I	Input voltage	EPR_EN	-0.3	6.0	V
V_I	Input voltage	VPWR	-0.3	5	V
		RPD_G1, RPD_G2, VBUS	-0.3	63	V
V_I	Input voltage	VBUS (VPWR = 0V)	-0.3	24	V
V_I	Input voltage	VBUS (VPWR > 2.7V)	-0.3	63	V
V_O	Output voltage	$\overline{FLT}$	-0.3	6	V
		VBIAS	-0.3	63	V
V_O	Output voltage	VBUS_LV	-0.3	24	V
V_O	Output voltage	EPR_BLK_G	-0.3	30	V
V_{IO}	I/O voltage	CC1, CC2, SBU1, SBU2	-0.3	6	V
		C_CC1, C_CC2, C_SBU1, C_SBU2	-0.3	63	V
t_{rise}	Input voltage rise time (V_I > 36V)	CC1, CC2, SBU1, SBU2	400		ns
T_J	Operating junction temperature		-40	125	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings—IEC Specification

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2, C_CC1, C_CC2	Contact discharge	±8000	V
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2, C_CC1, C_CC2	Air-gap discharge	±15000	V
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2, C_SBU1, C_SBU2	Contact discharge	±8000	V
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2, C_SBU1, C_SBU2	Air-gap discharge	±15000	V
$V_{(Surge)}$	Lightning and Surge	IEC 61000-4-5, C_CC1, C_CC2		±65	V
		IEC 61000-4-5, C_SBU1, C_SBU2		+65/-35	V

5.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_I	Input voltage	VPWR	2.7	3.3	4.5	V
		RPD_G1, RPD_G2	0		5.5	V
		EPR_EN	0		VPWR	V
		VBUS	0		51	V
V_O	Output voltage	$\overline{FLT}$ Pull-up resistor power rail	2.7		5.5	V
V_{IO}	I/O voltage	CC1, CC2, C_CC1, C_CC2	0		5.5	V
		SBU1, SBU2, C_SBU1, C_SBU2	0		4.3	V
I_{VCONN}	V_{CONN} Current	Current flowing into CC1/2 and flowing out of C_CC1/2, $T_J \le 105$ °C			600	mA
I_{VCONN}	V_{CONN} Current	Current flowing into CC1/2 and flowing out of C_CC1/2, $T_J \le 85$ °C			1.25	A
T_J	Operating Junction Temperature		-40		125	°C

			MIN	NOM	MAX	UNIT
External Components[1]	External Components[1]	$\overline{FLT}$ Pull-up resistance	1.7		300	kΩ
		VBIAS capacitance [2]	0.04	0.1	0.14	µF
		VPWR Capacitance	0.3	1		µF
		VBUS_LV Capacitance		0.1		µF

(1) For recommended values for capacitors and resistors, the typical values assume a component placed on the board near the pin. Minimum and maximum values listed are inclusive of manufacturing tolerances, voltage derating, board capacitance, and temperature variation. The effective value presented should be within the minimum and maximums listed in the table.
(2) The VBIAS pin requires a minimum 63-VDC rated capacitor. A 100-VDC rated capacitor is recommended to reduce capacitance derating.
See the VBIAS Capacitor Selection section for more information on selecting the VBIAS capacitor.

5.4 Thermal Information

THERMAL METRIC[1]		TPD4S480 QFN 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	44.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	41.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	17.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over operating junction temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CC OVP Switches						
R_{ON}	On Resistance of CC OVP FETs	CCx = 5.5V, $T_J \le 85$ ℃		272	420	mΩ
C_{ON_CC}	Equivalent on Capacitance	Capacitance from CCx or C_CCx to GND when device is powered. Measure at V_{C_CCx}/V_{CCx} = 0V to 1.2V, f = 400kHz.	40	74	120	pF
RD_DB	Dead Battery Pull-Down Resistors (only present when device is unpowered)	V_{C_CCx} = 2.6V	4.1	5.1	6.1	kΩ
VTH_DB	Threshold voltage of the pull-down FET in series with RD during dead battery	I_{C_CCx} = 80µA	0.5	0.9	1.2	V
V_{OVPCC}	OVP Threshold on CC Pins	Place 5.5V on C_CCx. Step up C_CCx until $\overline{FLT}$ pin is asserted. Put 100mA load through the CC FET and see the FET shuts off.	5.6	5.9	6.2	V
V_{OVPCC_HYS}	Hysteresis on CC OVP	Place 6.5 V on C_CCx. Step down the voltage on C_CCx until the FLT pin is deasserted. Measure difference between rising and falling OVP threshold for C_CCx.		50		mV
BW_{ON}	On Bandwidth Single Ended (-3dB)	Measure the -3 dB bandwidth from C_CCx to CCx. Single ended measurement, 50-Ω system. Vcm = 0.1V to 1.2 V.		125		MHz
V_{STBUS_CC}	Short-to-VBUS tolerance on the CC pins	Hot-Plug C_CCx with a 1 meter USB Type C Cable, place a 30-Ω load on CCx			51	V
$V_{STBUS\_CC\_CLAMP}$	Short-to-VBUS System-Side Clamping Voltage on the CC pins (CCx)	Hot-Plug C_CCx with a 1 meter USB Type C Cable. Hot-Plug voltage C_CCx = 51 V. VPWR = 3.3 V. Place a 30-Ω load on CCx.		7		V
SBU OVP Switches						
R_{ON}	On Resistance of SBU OVP FETs	SBUx = 3.6 V. –40°C ≤ TJ ≤ +85°C		4	6.8	Ω

5.5 Electrical Characteristics (続き)

over operating junction temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ON_SBU}	Equivalent on Capacitance	Capacitance from SBUx or C_SBUx to GND when device is powered. Measure at V_{C_SBUx}/V_{SBUx} = 0.3V to 4.0V.		6		pF
V_{OVPSBU}	OVP Threshold on SBU Pins	Place 3.6V on C_SBUx. Step up C_SBUx until $\overline{FLT}$ pin is asserted.	4.0	4.2	4.41	V
V_{OVPSBU_HYS}	Hysteresis on SBU OVP	Place 5 V on C_CCx. Step down the voltage on C_CCx until the FLT pin is deasserted. Measure difference between rising and falling OVP threshold for C_SBUx.		50		mV
BW_{ON}	On Bandwidth Single Ended (-3dB)	Measure the -3 dB bandwidth from C_SBUx to SBUx. Single ended measurement, 50Ω system. Vcm = 0.1V to 3.6V.	600	760		MHz
X_{TALK}	Crosstalk	Measure crosstalk at f = 1 MHz from SBU1 to C_SBU2 or SBU2 to C_SBU1. Vcm1 = 3.6 V, Vcm2 = 0.3 V. Terminate open sides to 50Ω.		-70		dB
V_{STBUS_SBU}	Short-to-VBUS tolerance on the SBU pins	Hot-Plug C_SBUx with a 1 meter USB Type C Cable. Put a 100-nF capacitor in series with a 40-Ω resistor to GND on SBUx.			51	V
$V_{STBUS\_SBU\_CLAMP}$	Short-to-VBUS System-Side Clamping Voltage on the SBU pins (SBUx)	Hot-Plug C_SBUx with a 1 meter USB Type C Cable. Hot-Plug voltage C_SBUx = 51V. VPWR = 3.3 V. Put a 150-nF capacitor in series with a 40-Ω resistor to GND on SBUx.		7		V
EPR Adapter						
VBUS_DIV_SPR	VBUS_LV to VBUS divider ratio, SPR Mode	VBUS_LV/VBUS, EPR_EN = 0, VBUS = 4.5 - 21V, I_VBUS_LV = 0-20mA		1		V/V
VBUS_DIV_EPR	VBUS_LV to VBUS divider ratio, EPR Mode	VBUS_LV/VBUS, EPR_EN = 1, VBUS = 26.6-50.4, I_VBUS_LV = 0-20mA		0.42		V/V
I_{VBUSLV}	Current from VBUS_LV				20	mA
V_{FWD_VBUSLV}	VBUS to VBUS_LV forward voltage drop	I_VBUS_LV=20mA, VBUS=4.5V, EPR_EN=0		456	700	mV
V_{FWD_VBUSLV}	VBUS to VBUS_LV forward voltage drop	I_VBUS_LV=20mA, VBUS=26V, EPR_EN=1		823	940	mV
$V_{EPR\_THRESH\_R}$	Rising VBUS EPR enable threshold		22.7		24	V
$V_{EPR\_THRESH\_F}$	Falling VBUS EPR enable threshold		22.4		23.4	V
$V_{EPR\_BLK\_G}$	Gate Drive voltage for EPR_BLK_G	0 ≤ VBUS ≤ 22 V	5		12	V
$I_{EPR\_BLK\_G}$	Gate Driver Sourcing Current	$0 \le V_{EPR\_BLKG}\text{-}V_{VBUS} \le 5$ V, $0 \le V_{VBUS} \le 22$ V, measure $I_{EPR\_BLK\_G}$		4		µA
$V_{EPR\_EN\_V+}$	EPR_EN rising threshold				0.7*VPWR	V
$V_{EPR\_EN\_V-}$	EPR_EN falling threshold		0.3*VPWR			V
Power Supply and Leakage Currents						
V_{PWR_UVLO}	V_{PWR} Under Voltage Lockout	Place 1 V on VPWR and raise voltage until SBU or CC FETs turn-on.	2.1	2.3	2.6	V
$V_{PWR\_UVLO\_HYS}$	V_{PWR} UVLO Hysteresis	Place 3 V on VPWR and lower voltage until SBU or CC FETs turnoff; measure difference between rising and falling UVLO to calculate hysteresis.	70	100	130	mV
I_{VPWR}	V_{PWR} supply current	VPWR = 3.3 V (typical), VPWR = 4.5 V (maximum). –40°C ≤ T_J ≤ +85°C.		112	160	µA
$I_{C\_CC\_LEAK}$	Leakage current for C_CCx pins when device is powered	VPWR = 3.3 V, V_{C_CCx} = 3.6 V, CCx pins are floating, measure leakage current into C_CCx pins.			5	µA

5.5 Electrical Characteristics (続き)

over operating junction temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{C\_SBU\_LEAK}$	Leakage current for C_SBUx pins when device is powered	VPWR = 3.3 V, VC_SBUx = 3.6 V, SBUx pins are floating, measure leakage current into C_SBUx pins. Result should be same if SBUx side is biased and C_SBUx is left floating.-40°C ≤ T_J ≤ +85°C			3.2	µA
$I_{C\_CC\_LEAK\_OVP}$	Leakage current for C_CCx pins when device is in OVP	VPWR = 0 V or 3.3 V, V_{C_CCx} = 51 V, CCx pins are set to 0 V, measure leakage current into C_CCx pins.			1200	µA
$I_{C\_SBU\_LEAK\_OVP}$	Leakage current for C_SBUx pins when device is in OVP	VPWR = 0 V or 3.3 V, V_{C_SBUx} = 51 V, SBUx pins are set to 0 V, measure leakage current into C_SBUx pins.			720	µA
$I_{CC\_LEAK\_OVP}$	Leakage current for CC pins when device is in OVP	VPWR = 0 V or 3.3 V, V_{C_CCx} = 51 V, CCx pins are set to 0 V, measure leakage current out of CCx pins.			30	µA
$I_{SBU\_LEAK\_OVP}$	Leakage current for SBU pins when device is in OVP	VPWR = 0 V, V_{C_SBUx} = 51 V, SBUx pins are set to 0 V, measure leakage current into SBUx pins.	-1		1	µA
/FLT Pin						
V_{OL}	Low-level output voltage	IOL = 3mA. Measure voltage at $\overline{FLT}$ pin.			0.4	V
Over Temperature Protection						
T_{SD_RISING}	The rising over-temperature protection shutdown threshold		150	175		°C
$T_{SD\_FALLING}$	The falling over-temperature protection shutdown threshold		130	140		°C
T_{SD_HYST}	The over-temperature protection shutdown threshold hysteresis			35		°C

5.6 Timing Requirements

		MIN	NOM	MAX	UNIT
Power-On and Off Timings					
t_{ON_FET}	Time from Crossing Rising VPWR UVLO until CC and SBU OVP FETs are on.		1.3	3.5	ms
$t_{ON\_FET\_DB}$	Time from Crossing Rising VPWR UVLO until CC and SBU OVP FETs are on and the dead battery resistors are off.		5.7	9.5	ms
dV_{PWR_OFF}/dt	Minimum slew rate for CC and FETs turn off during a power off.	-0.5			V/µs
Over Voltage Protection					
$t_{OVP\_RESPONSE\_CC}$	OVP response time on the CCx pins. Time from OVP asserted until OVP FETs turn off.		70		ns
$t_{OVP\_RESPONSE\_SBU}$	OVP response time on the SBUx pins. Time from OVP asserted until OVP FETs turn off.		80		ns
$t_{OVP\_RECOVERY\_CC}$	OVP recovery time on the CCx pins. Once an OVP has occurred, the minimum time duration until the CC FETs turn back on. OVP must be removed for CC FETs to turn back on.		0.9	2.3	ms
$t_{OVP\_RECOVERY\_CC\_DB}$	OVP recovery time on the CCx pins. Once an OVP has occurred, the minimum time duration until the CC FETs turn back on and the dead battery resistors turn off. OVP must be removed for CC FETs to turn back on.		5		ms
$t_{OVP\_RECOVERY\_SBU}$	OVP recovery time on the SBUx pins. Once an OVP has occurred, the minimum time duration until the SBU FETs turn back on. OVP must be removed for SBU FETs to turn back on.		0.62		ms
$t_{OVP\_FLT\_ASSERTION}$	Time from OVP Asserted to /FLT assertion. $\overline{FLT}$ assertion is 10% of the maximum value. Set C_CCx or C_SBUx above the maximum OVP threshold. Start the time where it passes the typical OVP threshold value.		20		µs
$t_{OVP\_FLT\_DEASSERTION}$	Time from CC FET turn on after an OVP to $\overline{FLT}$ deassertion.		5		ms

5.7 Typical Characteristics

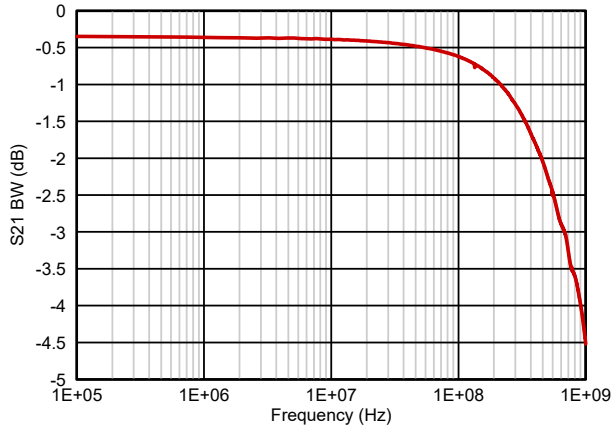


図 5-1. SBU Bandwidth

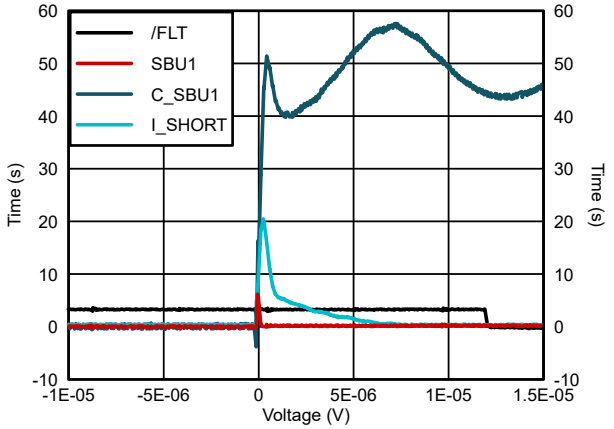


図 5-2. SBU Short-to-V_{BUS} 48V

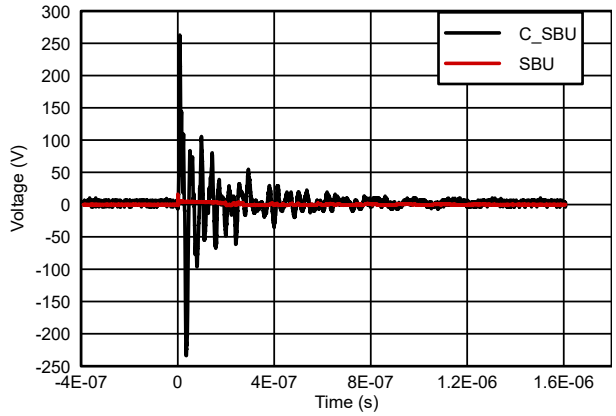


図 5-3. SBU IEC 61000-4-2 4kV Response Waveform

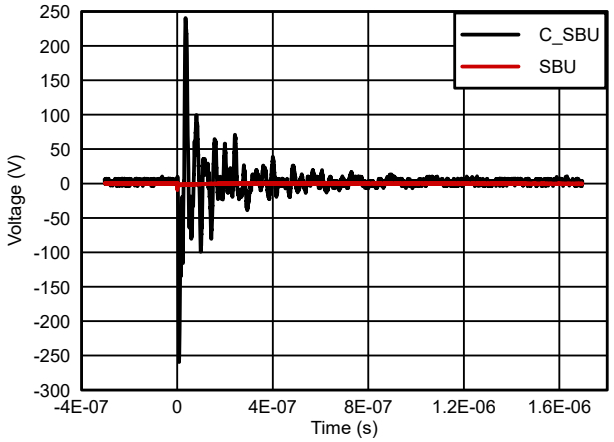


図 5-4. SBU IEC 61000-4-2 –4kV Response Waveform

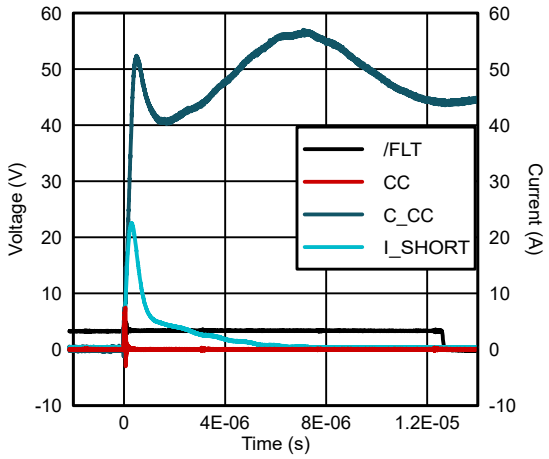


図 5-5. CC Short-to-V_{BUS} 48V

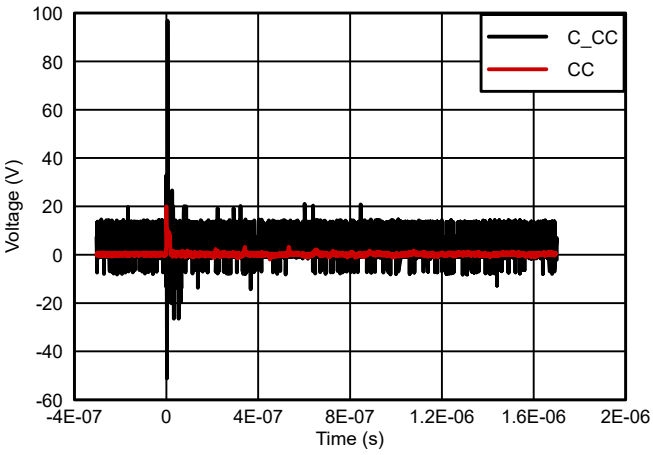


図 5-6. CC IEC 61000-4-2 8kV Response Waveform

5.7 Typical Characteristics (continued)

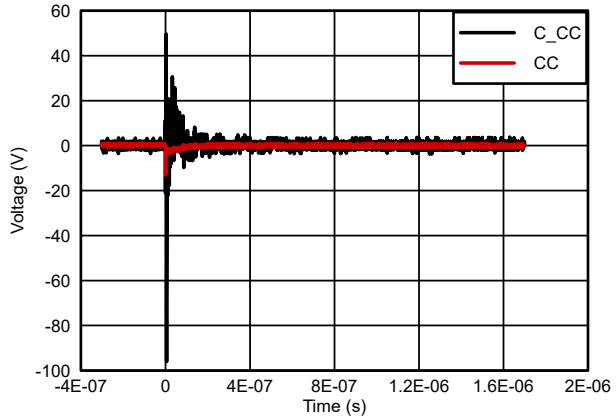


図 5-7. CC IEC 61000-4-2 –8kV Response Waveform

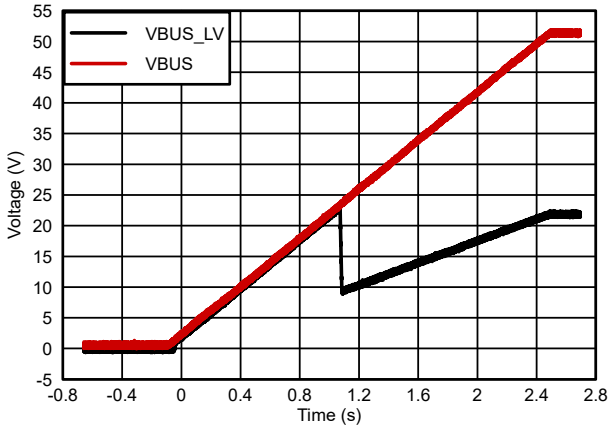


図 5-8. VBUS Sweep with EPR_EN low

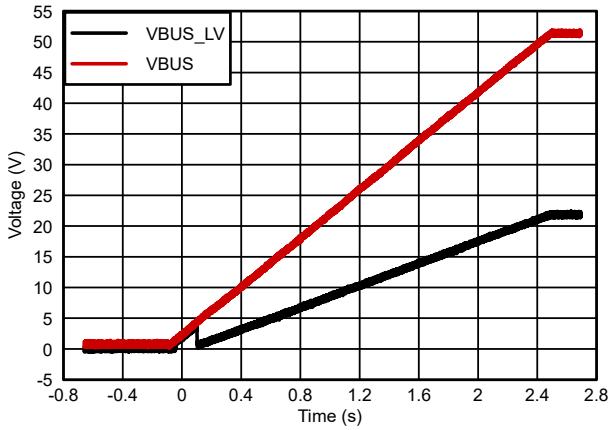


図 5-9. VBUS Sweep with EPR_EN high

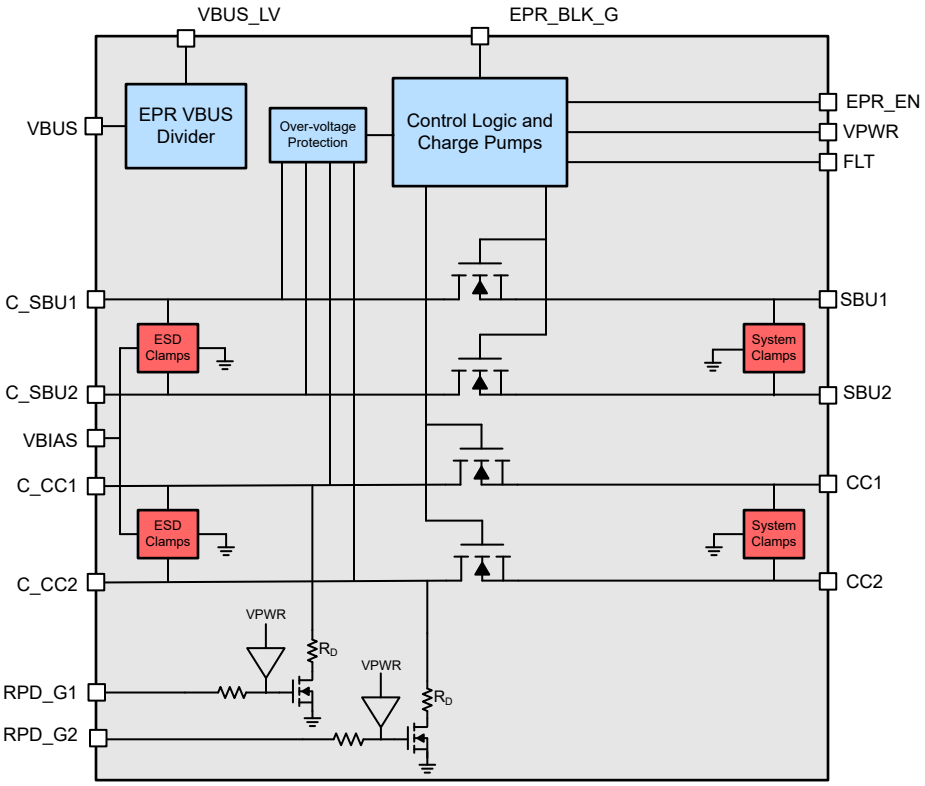
6 Detailed Description

6.1 Overview

The TPD4S480 is a single chip USB Type-C port protector that provides 48V Short-to-V_{BUS} overvoltage and ESD protection. Due to the small pin pitch of the USB Type-C connector and non-compliant USB Type-C cables and accessories, the V_{BUS} pins can get shorted to the CC and SBU pins inside the USB Type-C connector. Because of this short-to-V_{BUS} event, the CC and SBU pins need to be 48V tolerant, to support protection on the full USB PD-EPR voltage range. The TPD4S480 integrates four channels of 48V Short-to-V_{BUS} overvoltage protection for the CC1, CC2, SBU1, and SBU2 pins of the USB Type-C connector.

Additionally, IEC 61000-4-2 system level ESD protection is required to protect a USB Type-C port from ESD strikes generated by end product users. The TPD4S480 integrates four channels of IEC61000-4-2 ESD protection for the CC1, CC2, SBU1, and SBU2 pins of the USB Type-C connector. This means ESD protection is provided for all of the low-speed pins on the USB Type-C connector in a single chip by the TPD4S480. Additionally, high-voltage ESD protection that is 55V DC tolerant is required for the CC and SBU lines to simultaneously support ESD and Short-to-V_{BUS} protection. The TPD4S480 integrates a high-voltage ESD diode designed to work in conjunction with the overvoltage protection FETs inside the device.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 4-Channels of Short-to-V_{BUS} Overvoltage Protection (CC1, CC2, SBU1, SBU2 Pins or CC1, CC2, DP, DM Pins): 63-V_{DC} Tolerant

The TPD4S480 provides 4-channels of Short-to-V_{BUS} Overvoltage Protection for the CC1, CC2, SBU1, and SBU2 pins (or the CC1, CC2, DP, and DM pins) of the USB Type-C connector. The TPD4S480 is able to handle 63V_{DC} on its C_CC1, C_CC2, C_SBU1, and C_SBU2 pins. This level of protection is necessary because according to the USB PD specification, with V_{BUS} set for 48-V operation, the V_{BUS} voltage is allowed to legally swing up to 50.4V and 50.9V on voltage transitions from a different USB PD V_{BUS} voltage. The TPD4S480 builds

in tolerance up to 63V_{BUS} to provide margin above this 50.9V specification to be able to support inductive ringing that may occur during a short event.

When a short-to-V_{BUS} event occurs, ringing happens due to the RLC elements in the hot-plug event. With very low resistance in this RLC circuit, ringing up to twice the settling voltage can appear on the connector. Ringing of more than twice the DC level can be generated if any capacitor on the line derates in capacitance value during the short-to-V_{BUS} event. This behavior means that more than 90V could be seen on a USB Type-C pin during a Short-to-V_{BUS} event. The TPD4S480 has built in circuit protection to handle this ringing. The diode clamps used for IEC ESD protection also clamp the ringing voltage during the short-to-V_{BUS} event to limit the peak ringing to approximately 53V. Additionally, the overvoltage protection FETs integrated inside the TPD4S480 are 63V tolerant, therefore being capable of supporting the high-voltage ringing waveform that is experienced during the short-to-V_{BUS} event. The well designed combination of voltage clamps and 63V tolerant OVP FETs insures the TPD4S480 can handle Short-to-V_{BUS} hot-plug events with hot-plug voltages as high as 51V_{DC}.

The TPD4S480 has an extremely fast turnoff time of 70ns typical. Furthermore, additional voltage clamps are placed after the OVP FET on the system side (CC1, CC2, SBU1, SBU2) pins of the TPD4S480, to further limit the voltage and current that are exposed to the USB Type-C CC/PD controller during the 70ns interval while the OVP FET is turning off. The combination of connector side voltage clamps, OVP FETs with extremely fast turnoff time, and system side voltage clamps all work together to insure the level of stress seen on a CC1, CC2, SBU1, or SBU2 pin during a short-to-V_{BUS} event is less than or equal to an HBM event.

The SBU OVP FETs are designed with to be able to optionally protect the DP, DM (USB2.0) pins in lieu of the SBU pins. Some systems designers also prefer to protect the DP, DM pins from Short-to-V_{BUS} events due to the potential for moisture/water in the connector to short the V_{BUS} pins to DP, DM pins. This can be especially applicable in cases where the end equipment with a USB Type-C connector is trying to be made water-proof. If desiring to protect the DP, DM pins on the USB Type-C connector from a Short-to-V_{BUS} event, connect the C_SBUx pins to the DP, DM pins on the USB Type-C connector, and the SBUx pins to the USB2.0 pins of the system device being protected from the Short-to-V_{BUS} event.

6.3.2 CC1, CC2 Overvoltage Protection FETs 600-mA Capable for Passing VCONN Power

The CC pins on the USB Type-C connector serve many functions; one of the functions is to be a provider of power to active cables. Active cables are required when desiring to pass greater than 3 A of current on the V_{BUS} line or when the USB Type-C port uses the super-speed lines (TX1+, TX2–, RX1+, RX1–, TX2+, TX2–, RX2+, RX2–). When CC is configured to provide power, it is called VCONN. VCONN is a DC voltage source in the range of 3V to 5.5V. If supporting VCONN, a VCONN provider must be able to provide 1.5 W of power to a cable; this translates into a current range of 273mA to 500mA (depending on the VCONN voltage level).

When a USB Type-C port is configured for VCONN and using the TPD4S480, this VCONN current flows through the OVP FETs of the TPD4S480. Therefore, the TPD4S480 has been designed to handle these currents and have an RON low enough to provide a specification compliant VCONN voltage to the active cable.

6.3.3 CC Dead Battery Resistors Integrated for Handling the Dead Battery Use Case in Mobile Devices

An important feature of USB Type-C and USB PD is the ability for this connector to serve as the sole power source to mobile devices. With support up to 240W, the USB Type-C connector supporting USB PD can be used to power a whole new range of mobile devices not previously possible with legacy USB connectors.

When the USB Type-C connector is the sole power supply for a battery powered device, the device must be able to charge from the USB Type-C connector even when its battery is dead. In order for a USB Type-C power adapter to supply power on V_{BUS}, RD pulldown resistors must be exposed on the CC pins. These RD resistors are typically included inside a USB Type-C CC/PD controller. However, when the TPD4S480 is used to protect the USB Type-C port, the OVP FETs inside the device isolate these RD resistors in the CC/PD controller when the mobile device has no power. When the TPD4S480 has no power, the OVP FETs are turned off to provide overvoltage protection in a dead battery condition. Therefore, the TPD4S480 integrates high-voltage, dead battery RD pull-down resistors to allow dead battery charging simultaneously with high-voltage OVP protection.

If dead battery support is required, short the RPD_G1 pin to the C_CC1 pin, and short the RPD_G2 pin to the C_CC2 pin. This short connects the dead battery resistors to the connector CC pins. When the TPD4S480 is unpowered, and the RP pull-up resistor is connected from a power adapter, this RP pull-up resistor activates the RD resistor inside the TPD4S480, and enables V_{BUS} to be applied from the power adapter even in a dead battery condition. Once power is restored back to the system and back to the TPD4S480 on its VPWR pin, the TPD4S480 turns ON its OVP FETs in 3.5ms and then turns OFF its dead battery RD. The TPD4S480 first turns ON its CC OVP FETs fully, and then removes its dead battery RDs to make sure the PD controller RD is fully exposed before removing the RD of the TPD4S480.

If desiring to power the CC/PD controller during dead battery mode and if the CC/PD Controller is configured as a DRP, it is critical that the TPD4S480 be powered before or at the same time that the CC/PD controller is powered. It is also critical that when unpowered, the CC/PD controller also expose its dead battery resistors. When the TPD4S480 gets powered, it exposes the CC pins of the CC/PD controller within 3.5ms, and then removes its own RD dead battery resistors. Once the TPD4S480 turns on, the RD pull-down resistors of the CC/PD controller must be present immediately, in order to maintain a connection. If the power adapter does not see RD present, it can disconnect V_{BUS}. This event removes power from the device with its battery still not sufficiently charged, which consequently removes power from the CC/PD controller and the TPD4S480. Then the RD resistors of the TPD4S480 are exposed again, and connects the V_{BUS} of the power adapter to start the cycle over.

If the CC/PD Controller is configured for DRP and has started to DRP toggle before the TPD4S480 turns on, this DRP toggle is unable to maintain a connection with a power adapter. If the CC/PD controller is configured for DRP, the dead battery resistors of the PD controller need to be exposed as well, and that the resistors remain exposed until the TPD4S480 turns on. This behavior is typically accomplished by powering the TPD4S480 at the same time as the CC/PD controller when powering the CC/PD controller in dead battery operation.

If dead battery charging is not required in your application, connect the RPD_G1 and RPD_G2 pins to ground.

6.3.4 EPR Adapter

The TPD4S480 integrates additional circuitry that may be used to adapt a PD controller with pin tolerances below EPR levels for use in EPR applications. The EPR adapter consists of two components, the VBUS divider and the EPR blocking FET gate driver. The EPR adapter features are enabled by asserting the EPR_EN pin or when the VBUS pin exceeds EPR_THRESH_R.

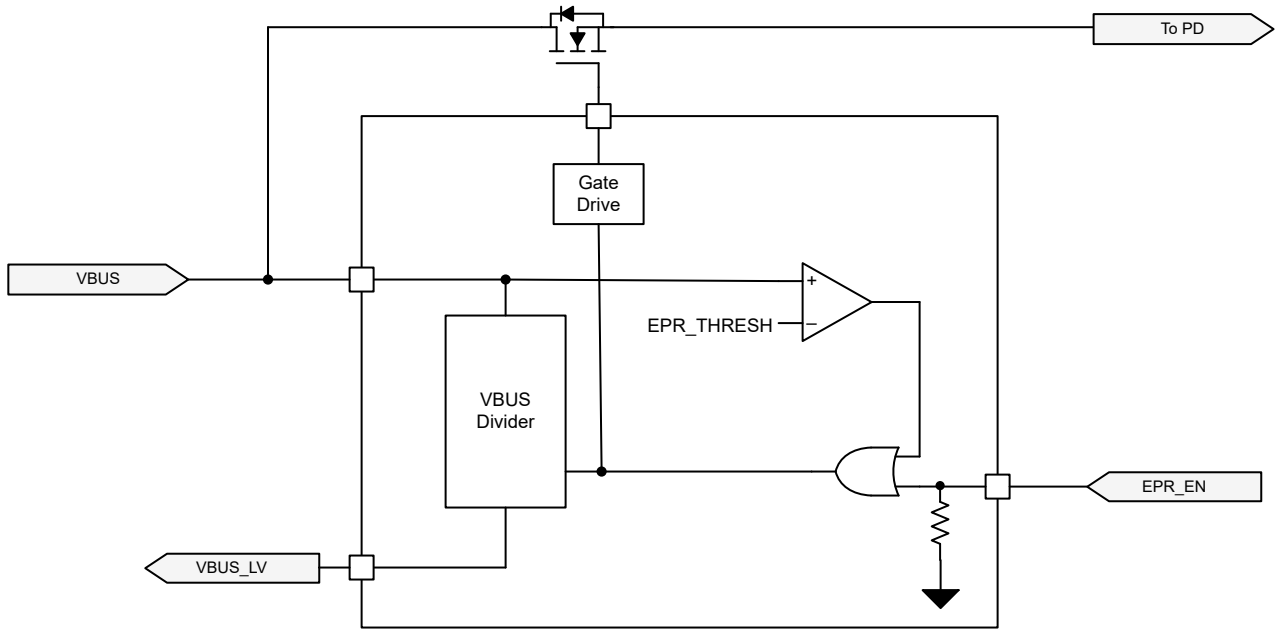


図 6-1. EPR Adapter

6.3.4.1 VBUS Divider

The VBUS divider provides a divided down output of VBUS so that an attached PD controller can safely sense EPR voltages. 表 6-1 summarizes the operating states of the VBUS divider.

表 6-1. VBUS Divider States

EPR_EN	VBUS	VBUS_LV Ratio (VBUS_LV / VBUS)	Description
0	< EPR_THRES_R	1	SPR Operation
1	X	0.42	EPR Operation
X	> EPR_THRESH_R	0.42	

6.3.4.2 EPR Blocking FET Gate Driver

An NFET gate driver is integrated for controlling an external blocking FET. When in EPR mode the gate driver is disabled, isolating any non-EPR tolerant circuitry from VBUS. When in SPR mode the gate driver is enabled connecting low voltage components to VBUS.

表 6-2. VBUS Divider States

EPR_EN	VBUS	Gate Driver State	Description
0	< EPR_THRES_R	Enabled	SPR Operation
1	X	Disabled	EPR Operation
X	> EPR_THRESH_R	Disabled	

6.4 Device Functional Modes

表 6-3 describes all of the functional modes for the TPD4S480. The "X" in the below table are "don't care" conditions, meaning any value can be present within the absolute maximum ratings of the data sheet and maintain that functional mode.

表 6-3. Device Mode Table

Device Mode Table		Inputs					Outputs				
MODE		VPWR	C_CCx	C_SBUx	RPD_Gx	T_J	$\overline{FLT}$	CC FETs	SBU FETs	VBUS_LV	EPR_BLK_G
Normal Operating Conditions	Unpowered, no dead battery support	<UVLO	X	X	Grounded	X	High-Z	OFF	OFF	VBUS	Disabled
	Unpowered, dead battery support	<UVLO	X	X	Shorted to C_CCx	X	High-Z	OFF	OFF	VBUS	Disabled
	Powered on, SPR mode	>UVLO	<OVP	<OVP	X, forced OFF	<TSD	High-Z	ON	ON	VBUS	Enabled
	Powered on, EPR mode	>UVLO	<OVP	<OVP	X, forced OFF	<TSD	High-Z	ON	ON	Divided VBUS	Disabled
Fault Conditions	Thermal shutdown	>UVLO	X	X	X, forced OFF	>TSD	Low (Fault Asserted)	OFF	OFF	Maintains EPR state	Maintains EPR state
	CC over voltage condition	>UVLO	>OVP	X	X, forced OFF	<TSD	Low (Fault Asserted)	OFF	OFF	Maintains EPR state	Maintains EPR state
	SBU over voltage condition	>UVLO	X	>OVP	X, forced OFF	<TSD	Low (Fault Asserted)	OFF	OFF	Maintains EPR state	Maintains EPR state
	IEC ESD generated over voltage condition(1)	>UVLO	X	X	R_D ON if RPD_Gx is shorted to C_CCx	<TSD	Low (Fault Asserted)	OFF	OFF	Maintains current EPR state	Maintains current EPR state

(1) This row describes the state of the device while still in OVP after the IEC ESD strike which put the device into OVP is over, and the voltages on the C_CCx and C_SBUx pins have returned to their normal voltage levels.

7 Application and Implementation

注

以下のアプリケーション情報は、テキサス・インスツルメンツの製品仕様に含まれるものではなく、テキサス・インスツルメンツはその正確性も完全性も保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。また、お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Application Information

The TPD4S480 provides 4-channels of Short-to-V_{BUS} overvoltage protection for the CC1, CC2, SBU1, and SBU2 pins of the USB Type-C connector Care must be taken to insure that the TPD4S480 provides adequate system protection as well as insuring that proper system operation is maintained. The following application example explains how to properly design the TPD4S480 into a USB Type-C system.

7.2 Typical Application

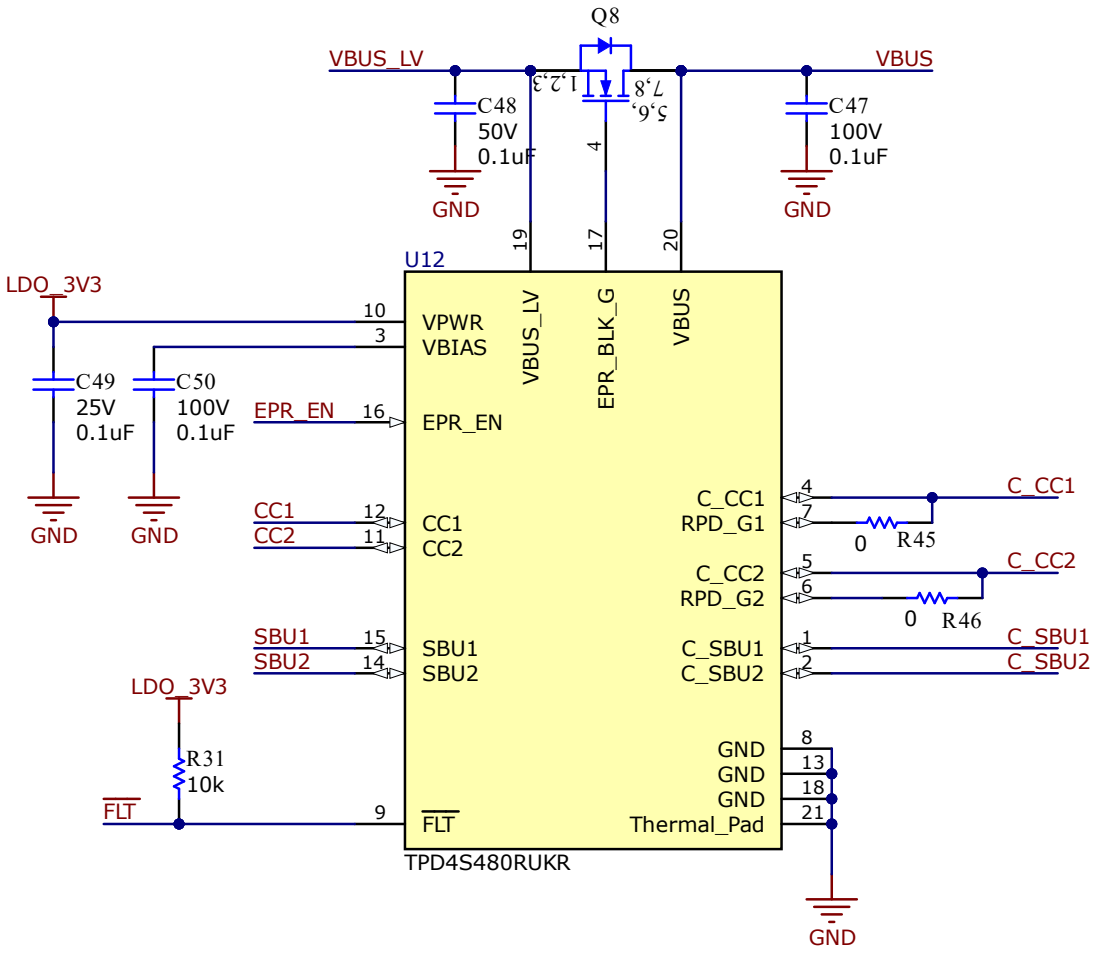


図 7-1. TPD4S480 Reference Schematic

7.2.1 Design Requirements

In this application example we study the protection requirements for a USB Type-C DRP Port, fully equipped with USB-PD, and 240W charging. The TPS26750 is used to easily enable a DRP port. Both the CC and SBU pins are susceptible to shorting to the V_{BUS} pin. With 240W charging, V_{BUS} operates at 48V, requiring the CC and SBU pins to tolerate $48V_{DC}$. With these protection requirements present for the USB Type-C connector, the TPD4S480 is used.

表 7-1 lists the TPD4S480 design parameters.

表 7-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{BUS} nominal operating voltage	48V
Short-to-V_{BUS} tolerance for the CC and SBU pins	63V
VBIAS nominal capacitance	0.1µF
Dead battery charging	240W
Maximum ambient temperature requirement	85°C

The recommended MOSFET settings for Q8, as shown in 表 7-2, are as follows:

表 7-2. MOSFET Selection

VDS (V)	VGS (V)	Type	RDS (on)
> = 30V	> = 15V	N-channel	< = 10mOhms (3A max Q8 current) < = 20mOhms (1.5A max Q8 current)

7.2.1.1 EPR Design Requirements

The TPD4S480 works in conjunction with the PD controller to provide the following functionality in USB-PD EPR:

- Short to VBUS protection for direct shorts to CC1 and CC2 pins of the Type-C connector.
- Short to VBUS protection for the liquid detection circuitry that is connected to the SBU1 and SBU2 pins of the Type-C connector, if the liquid detection feature is implemented.
- Voltage level translation from up the EPR maximum voltage down to the operation range of the VBUS pins of the PD controller.
- Gate drive for a high voltage NMOS transistor to allow the internal 5V power path to be used to source 5V in systems that only require a 5V output.

7.2.2 Detailed Design Procedure

7.2.2.1 VBIAS Capacitor Selection

As noted in the *セクション 5.3* table, a minimum of 63V_{BUS} rated capacitor is required for the VBIAS pin, and a 100V_{BUS} capacitor is recommended. The VBIAS capacitor is in parallel with the central diode clamp integrated inside the TPD4S480. A forward biased hiding diode connects the VBIAS pin to the C_CCx and C_SBUx pins. Therefore, when a Short-to-V_{BUS} event occurs at 48V, 48V_{BUS} minus a forward biased diode drop is exposed to the VBIAS pin. Additionally, during the short-to-V_{BUS} event, ringing can occur almost double the settling voltage of 48V, allowing a potential 96V to be exposed to the C_CCx and C_SBUx pins. However, the internal diode clamps limit the voltage exposed to the C_CCx and C_SBUx pins to around 63V. Therefore, at least 63V capacitor is required to insure the VBIAS capacitor does not get destroyed during Short-to-V_{BUS} events.

A 100V, X7R capacitor is recommended to further improve the derating performance of the capacitors. When the voltage across a real capacitor is increased, the capacitance value derates. The more the capacitor derates, the larger the ringing in the short-to-V_{BUS} RLC circuit. The 100V X7R capacitors have great derating performance, allowing for the best short-to-V_{BUS} performance of the TPD4S480.

7.2.2.2 Dead Battery Operation

For this application, we want to support 240W dead battery operation; when the device is out of battery, we still want to charge the laptop at 48V and 5A. This means that the USB PD Controller must receive power in dead battery mode. The TPS26750 has a built in LDO to supply the TPS26750 power from V_{BUS} in a dead battery condition.

The OVP FETs of the TPD4S480 remain OFF when unpowered to provide protection in dead battery or unpowered situations. However, when the OVP FETs are OFF, this isolates the TPS26750s dead battery resistors from the USB Type-C ports CC pins. A USB Type-C power adapter must see the RD pull-down dead battery resistors on the CC pins to provide power on V_{BUS}. Since the dead battery resistors of the TPS26750 are isolated from the USB Type-C connector CC pins, the built-in, dead battery resistors of the TPD4S480 must be connected. Short the RPD_G1 pin to the C_CC1 pin, and short the RPD_G2 pin to the C_CC2 pin.

Once the power adapter sees the dead battery resistors of the TPD4S480, 5V is applied on the V_{BUS} pin. This provides power to the TPS26750, turning the PD controller on, and allowing the battery to begin to charge. However, this application requires 240W charging in dead battery mode, so V_{BUS} at 48V and 5A is required. USB PD negotiation is required to accomplish this, so the TPS26750 needs to be able to communicate on the CC pins. The TPD4S480 needs to be turned on in dead battery mode as well so the PD controller can be exposed to the CC lines. To turn on the device, the TPD4S480 is powered by the internal LDO of the TPS26750, the LDO_3V3 pin. When the TPS26750 receives power on V_{BUS}, the TPD4S480 is turned on simultaneously.

The dead battery resistors of the PD controller also need to be present so the PD controller properly boots up in dead battery operation with the correct voltages on the CC pins.

Once this process has occurred, the TPS26750 can start negotiating with the power adapter through USB PD for higher power levels, allowing 240W operation in dead battery mode.

For more information on the TPD4S480 dead battery operation, see the *CC Dead Battery Resistors Integrated for Handling the Dead Battery Use Case in Mobile Devices* section of the data sheet.

7.2.2.3 CC Line Capacitance

USB PD has a specification for the total amount of capacitance that is required for proper USB PD BMC operation on the CC lines.

表 7-3. USB PD cReceiver Specification

NAME	DESCRIPTION	MIN	MAX	UNIT	COMMENT
cReceiver	CC receiver capacitance	200	600	pF	The DFP or UFP system shall have capacitance within this range when not transmitting on the line

The capacitance on the CC lines must stay in between 200pF and 600pF when USB PD is being used. Therefore, the combination of capacitances added to the system by the TPS26750, the TPD4S480, and any external capacitor must fall within these limits.

7.2.2.4 Additional ESD Protection on CC and SBU Lines

If additional IEC ESD protection is desired to be placed on either the CC or SBU lines, it is important that high-voltage ESD protection diodes be used. The maximum DC voltage that can be seen in USB PD is 50.4V, with 50.9V allowed during voltage transitions. Therefore, an ESD protection diode must have a reverse stand off voltage higher than 50.9V to prevent the diode from breakdown during a short-to-V_{BUS} event.

Due to the fact that the Short-to-V_{BUS} event applies a DC voltage to the CC and SBU pins, a deep-snap-back diode cannot be used unless its minimum trigger voltage is above 96V. During a Short-to-V_{BUS} event, RLC ringing of up to twice the settling voltage can be exposed to CC and SBU, allowing for up to 48V to be exposed. Furthermore, if any capacitor derates on the CC or SBU line, greater ringing can occur. Since this ringing is hard to bound, it is recommended to not use deep-snap-back diodes. If the deep-snap-back diode triggers during the short-to-V_{BUS} hot-plug event, it begins to operate in its conduction region. With a 48V V_{BUS} source present on the CC or SBU line, this allows the diode to conduct indefinitely.

7.2.2.5 $\overline{\text{FLT}}$ Pin Operation

Once a Short-to-V_{BUS} occurs on the C_CCx or C_SBUx pins, the $\overline{\text{FLT}}$ pin is asserted in 20µs (typical) so the PD controller can be notified quickly. If V_{BUS} is being shorted to CC or SBU, it is recommended to respond to the event by forcing a detach in the USB PD controller to remove V_{BUS} from the port. Although the USB Type-C port using the TPD4S480 is not damaged, as the TPD4S480 provides protection from these events, the other device connected through the USB Type-C Cable or any active circuitry in the cable can be damaged. Although shutting the V_{BUS} off through a detach does not ensure it stops the other device or cable from being damaged, it can mitigate any high current paths from causing further damage after the initial damage takes place. Additionally, even if the active cable or other device does have proper protection, the short-to-V_{BUS} event may corrupt a configuration in an active cable or in the other PD controller, so it is best to detach and reconfigure the port.

7.2.2.6 How to Connect Unused Pins

If either the RPD_Gx pins are unused in a design, they must be connected to GND.

7.2.3 EPR Application Curves

図 7-2 shows the VBUS and VBUS_LV pins during a 5V to 48V voltage transition.

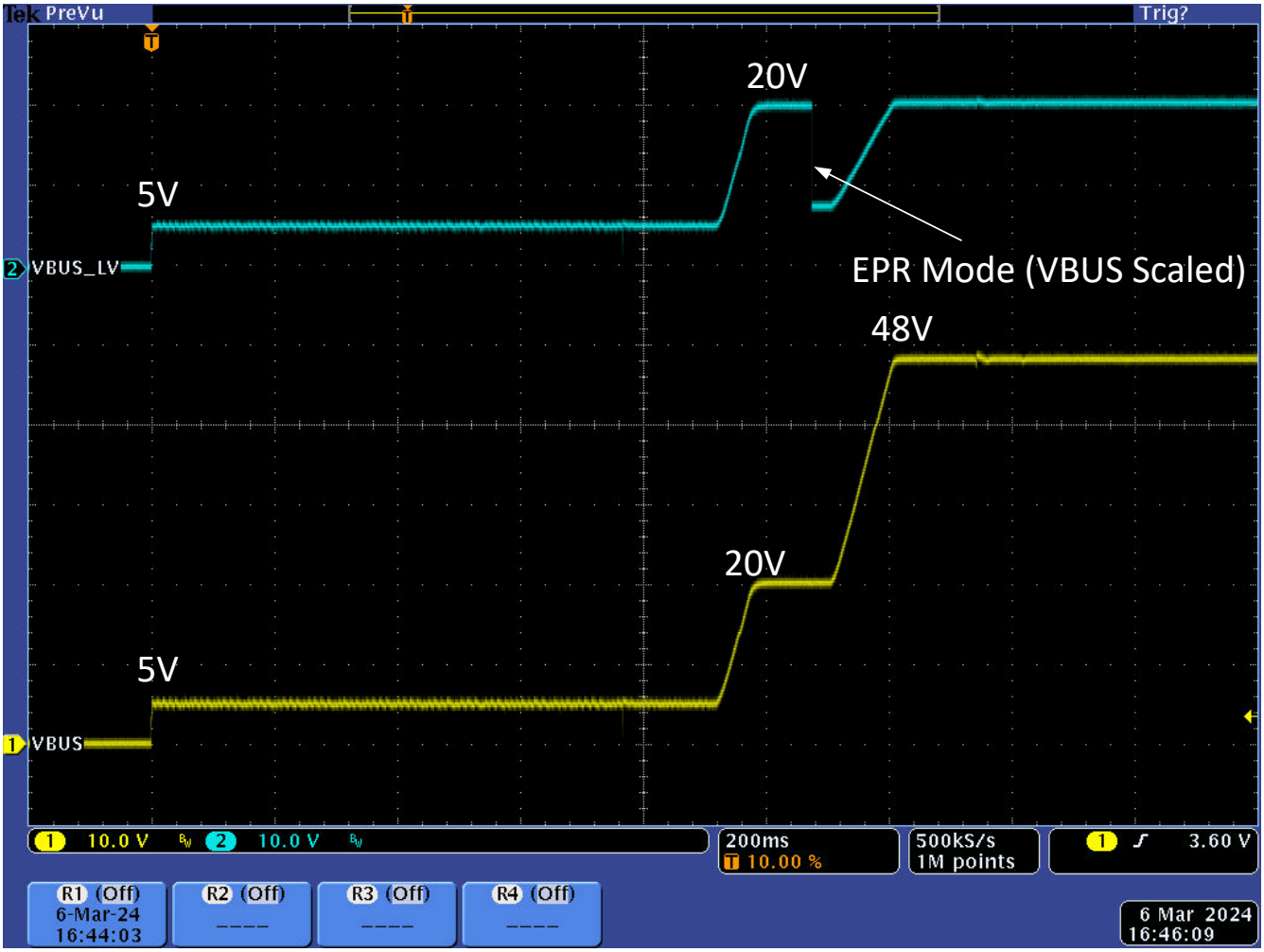


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図 7-2. 48V EPR Contract Negotiation VBUS and VBUS LV

7.3 Power Supply Recommendations

The V_{PWR} pin provides power to all the circuitry in the TPD4S480. It is recommended a 1-µF decoupling capacitor is placed as close as possible to the VPWR pin. If USB PD is desired to be operated in dead battery conditions, it is critical that the TPD4S480 share the same power supply as the PD controller in dead battery boot-up (such as sharing the same dead battery LDO). See the *CC Dead Battery Resistors Integrated for Handling the Dead Battery Use Case in Mobile Devices* section for more details.

7.4 Layout

7.4.1 Layout Guidelines

Proper routing and placement is important to maintain the signal integrity the USB2.0, SBU, CC line signals. The following guidelines apply to the TPD4S480 device:

- Place the bypass capacitors as close as possible to the V_{PWR} pin, and ESD protection capacitor as close as possible to the V_{BIAS} pin. Capacitors must be attached to a solid ground. This minimizes voltage disturbances during transient events such as short-to-V_{BUS} and ESD strikes.
- The USB2.0 and SBU lines must be routed as straight as possible and any sharp bends must be minimized.

Standard ESD recommendations apply to the C_CC1, C_CC2, C_SBU1, and C_SBU2 as well:

- The optimum placement for the device is as close to the connector as possible:

  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TPD4S480 device and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

7.4.2 Layout Example

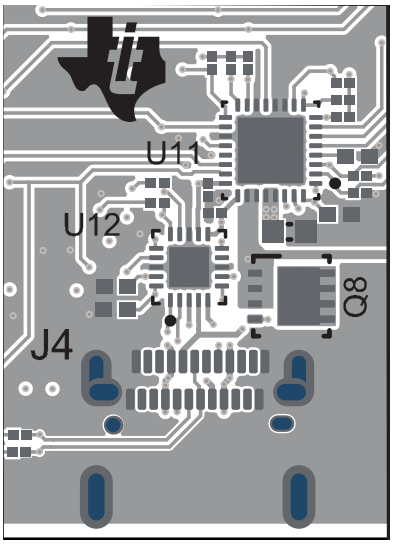

図 7-3. TPS26750 PCB Layout - Top Composite

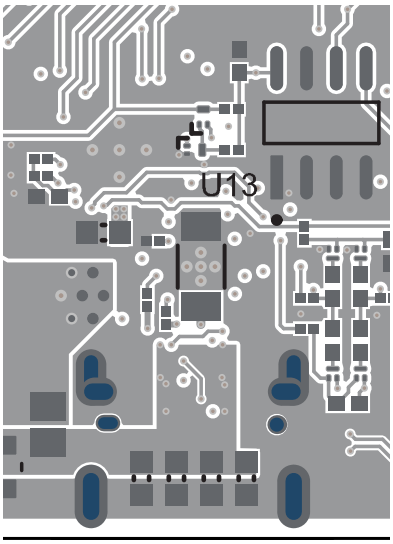

図 7-4. TPS26750 PCB Layout - Bottom Composite

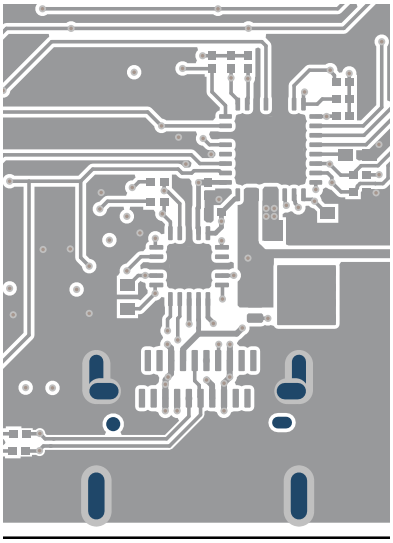

図 7-5. TPS26750 PCB Layout - Top Layer 1

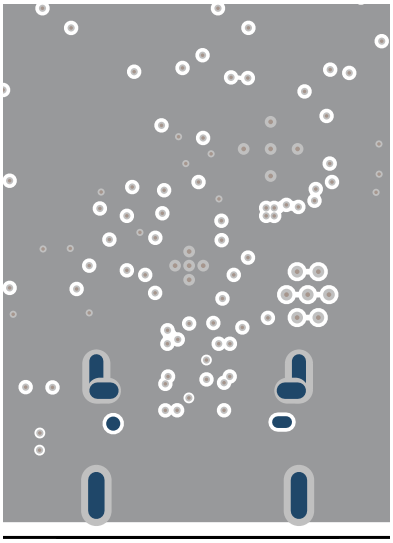

図 7-6. TPS26750 PCB Layout - GND Layer 2

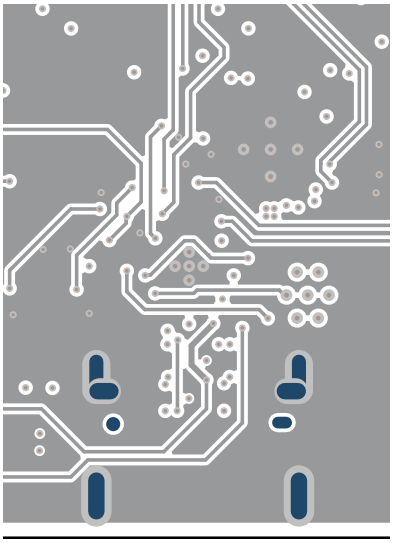

図 7-7. TPS26750 PCB Layout - Signal Layer 3

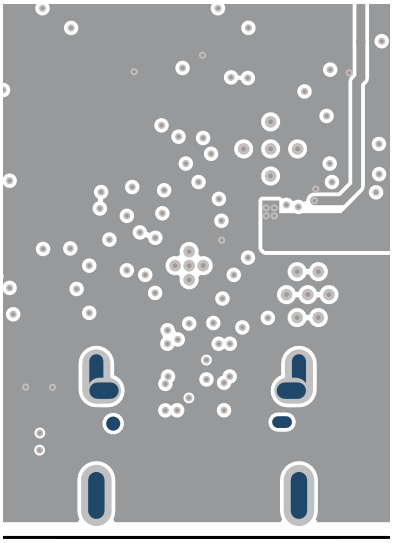

図 7-8. TPS26750 PCB Layout - Signal Layer 4

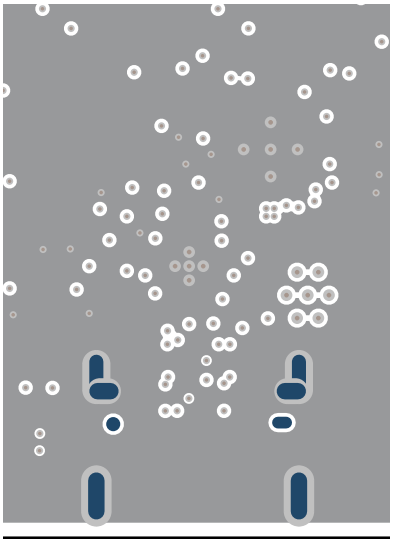

図 7-9. TPS26750 PCB Layout - GND Layer 5

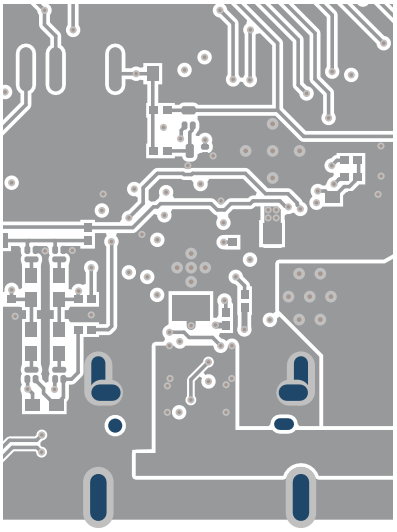

図 7-10. TPS26750 PCB Layout - Bottom Layer 6

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation see the following:

TPS26750 USB Type-C® and USB PD Controller With Integrated Power Switches Optimized for Power Applications

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.3 サポート・リソース

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8.4 Trademarks

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8.5 静電気放電に関する注意事項

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8.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
November 2024	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

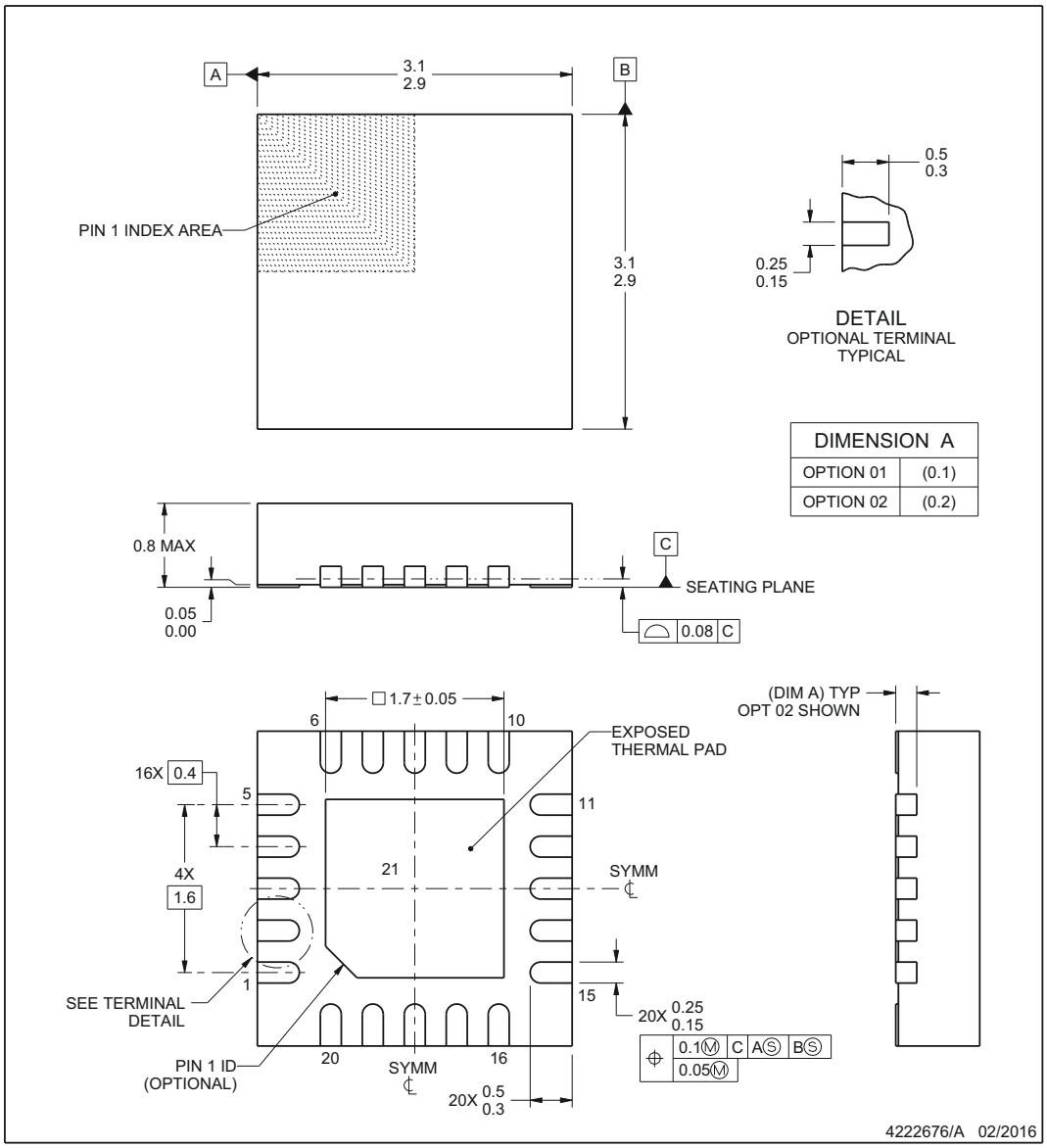
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

RUK0020B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



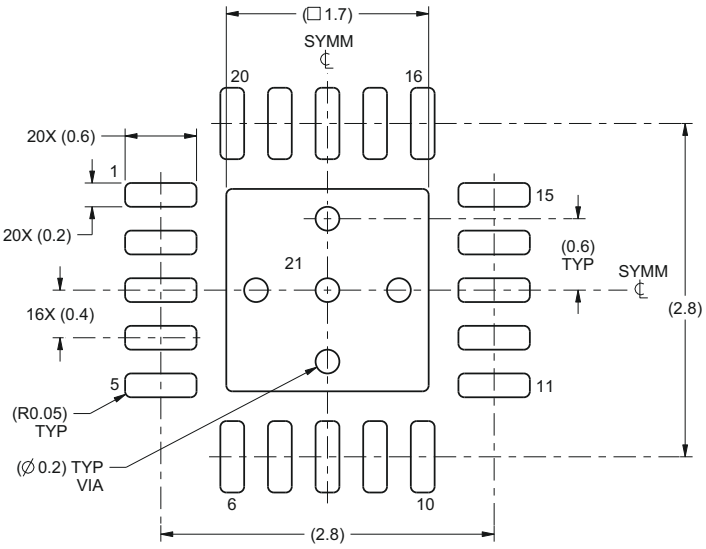
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

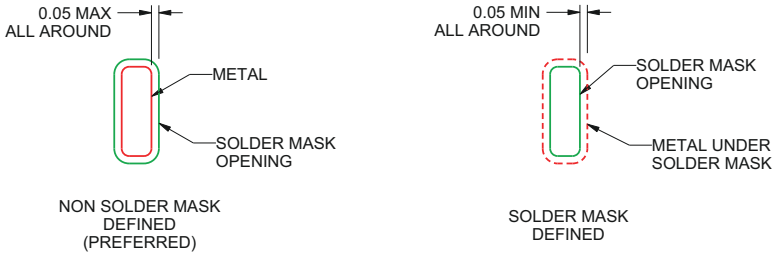
EXAMPLE BOARD LAYOUT

RUK0020B — **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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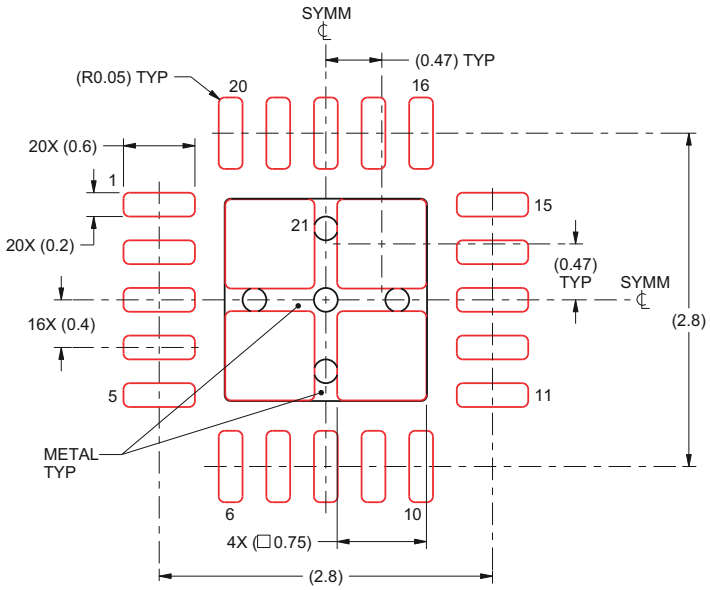
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RUK0020B — **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 21:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4222676/A 02/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPD4S480RUKR	Active	Production	WQFN (RUK) | 20	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4S480
TPD4S480RUKR.A	Active	Production	WQFN (RUK) | 20	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4S480

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TPD4S480 :

- Automotive : TPD4S480-Q1

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

GENERIC PACKAGE VIEW

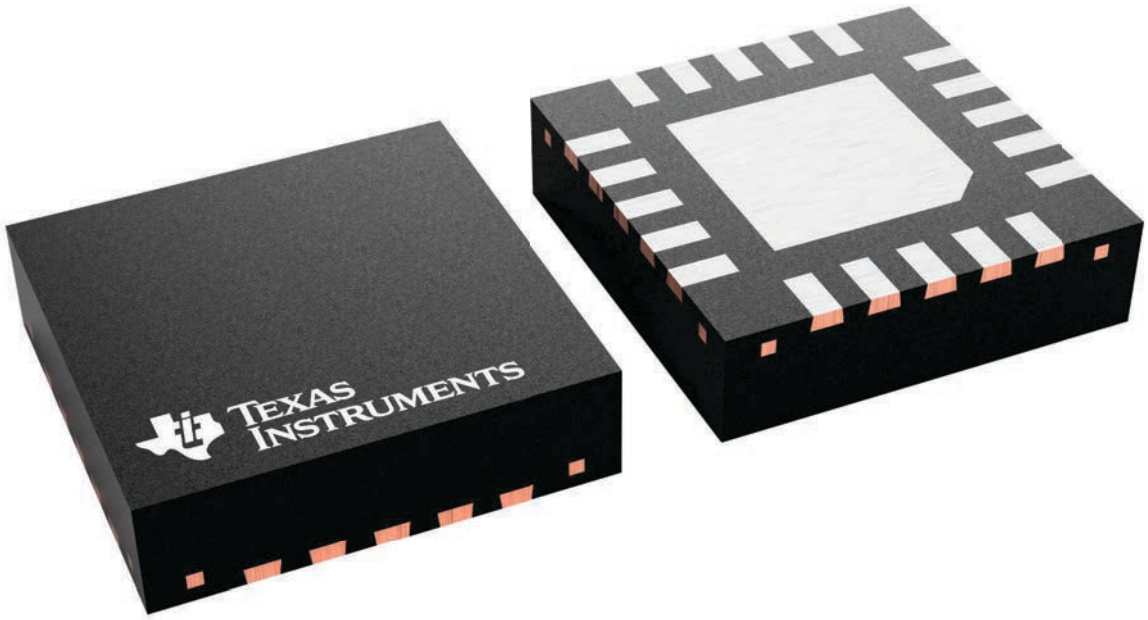
RUK 20

WQFN - 0.8 mm max height

3 x 3, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



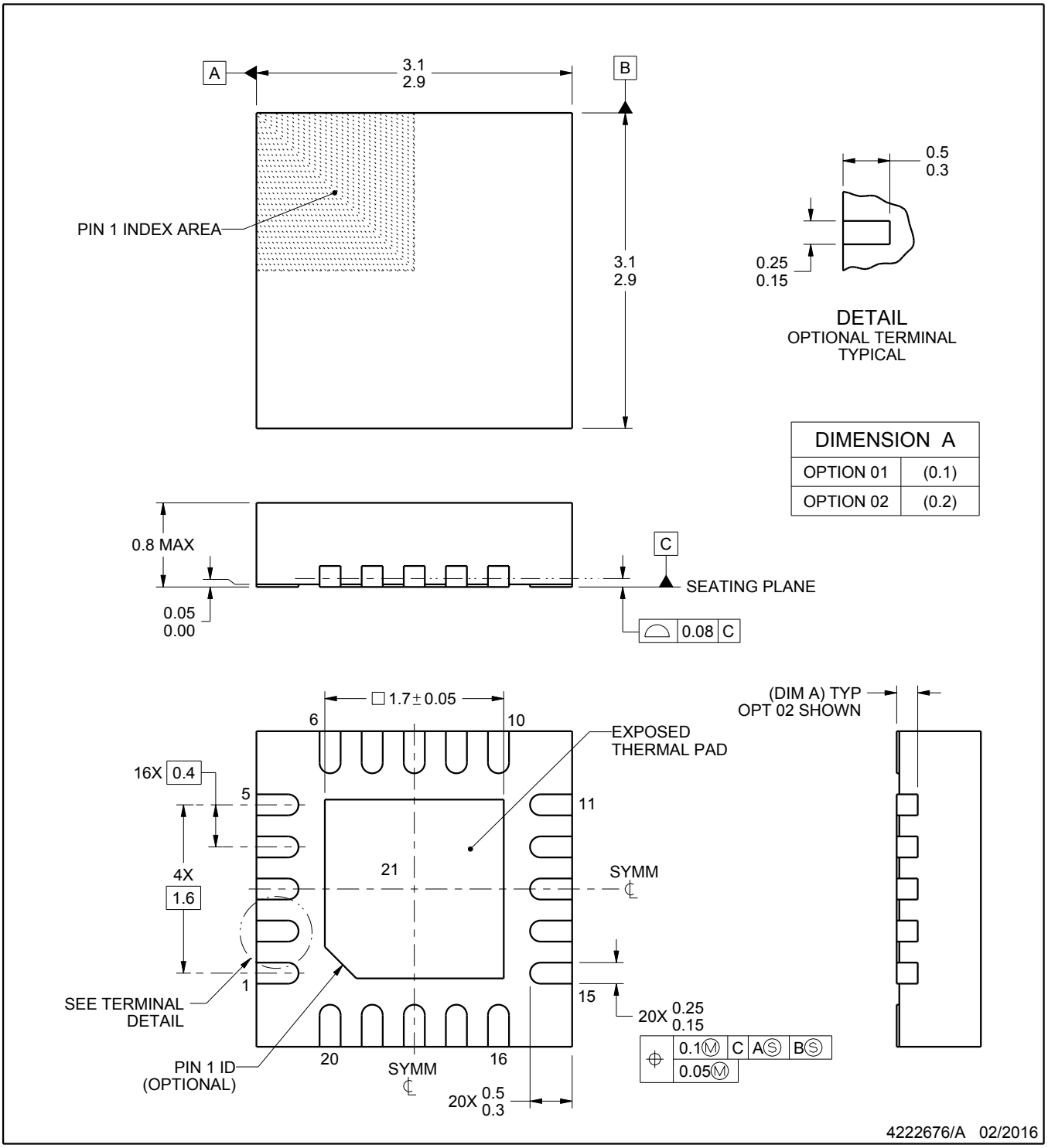
4229651/A

PACKAGE OUTLINE

RUK0020B

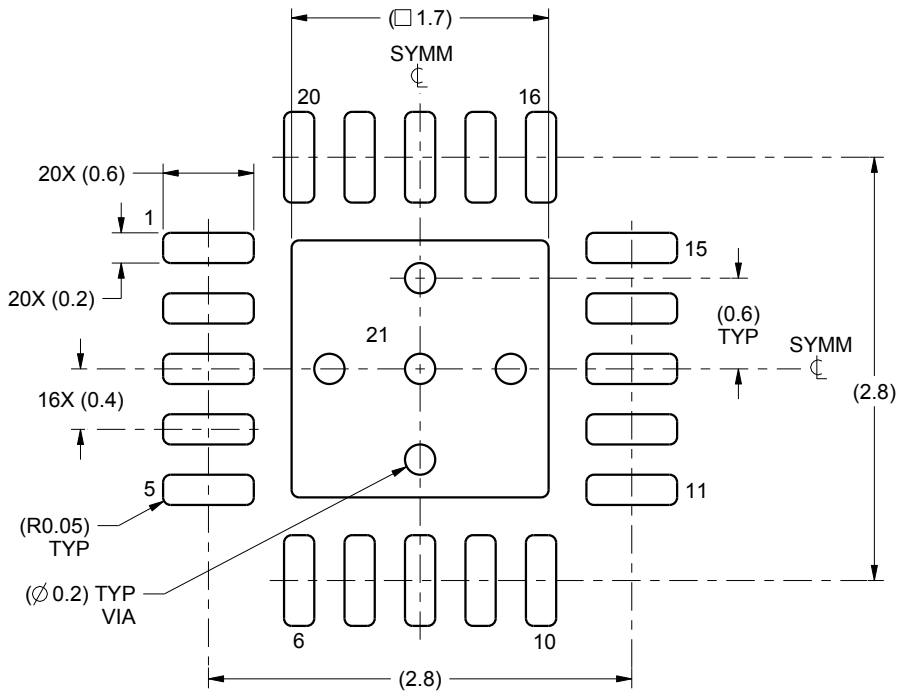
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

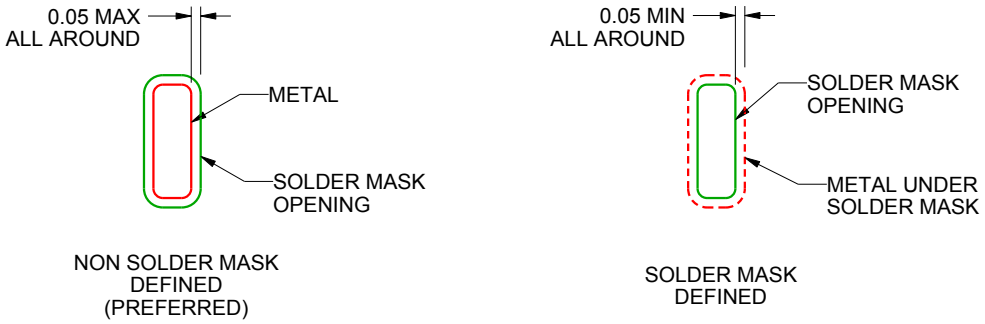


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4222676/A 02/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
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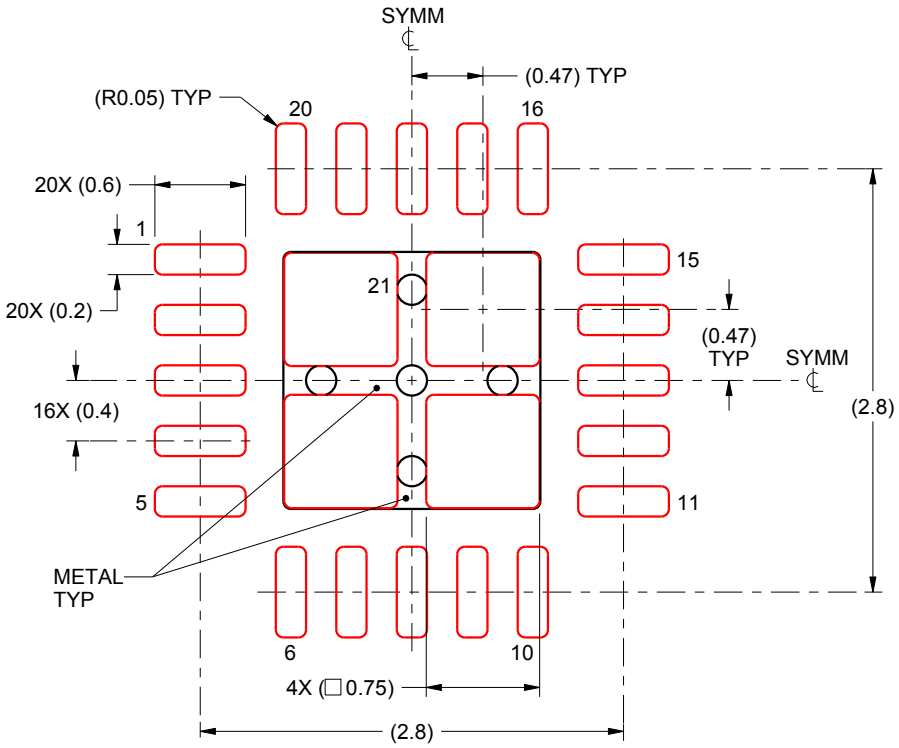

SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 21:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4222676/A 02/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月