

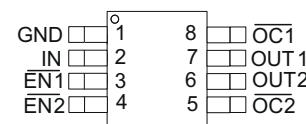
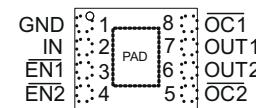
## TPS206xA 2 チャネル、電流制限、パワー ディストリビューションスイッチ

## 1 特長

- 70mΩ ハイサイド MOSFET
- 1A の連続電流
- 過熱および短絡保護
- 正確な電流制限 (最小 1.2A、最大 2A)
- 動作範囲: 2.7V ~ 5.5V
- 0.6ms の立ち上がり時間 (代表値)
- 低電圧誤動作防止
- デグリッチ フォルトルエポート ( $\overline{OCx}$ )
- 電源投入時の  $\overline{OCx}$  グリッチなし
- スタンバイ時電源電流: 最大 1μA
- 双方方向スイッチ
- 周囲温度範囲: -40°C ~ 85°C
- ソフト・スタート内蔵
- UL 認定済み - ファイル番号 E169910 (单一と一括制御の両方のチャネル構成)

## 2 アプリケーション

- 大きな容量性負荷
- 短絡保護

TPS2062A/TPS2066A  
D PACKAGE  
(TOP VIEW)TPS2062A/TPS2066A  
DRB PACKAGE  
(TOP VIEW)

Enable inputs are active low for all TPS2062A  
and active high for all TPS2066A

## 3 概要

TPS206xA 配電スイッチは、大きな容量性負荷と短絡が発生しやすいアプリケーションを対象としています。TPS206xA ファミリは TPS206x ファミリとピン互換で、過電流許容範囲がより狭くなっています。このファミリのデバイスは、複数のパワー スイッチを 1 つのパッケージに搭載する必要があるパワー ディストリビューション システム向けに、2 つの 70mΩ N チャネル MOSFET パワー スイッチを内蔵しています。各スイッチは、ロジック イネーブル入力によって制御されます。ゲートドライブは、スイッチング中の電流サージを最小限に抑えるためにパワー スイッチの立ち上がり時間と立ち下がり時間を制御するように設計された、内部チャージ ポンプによって提供されています。チャージ ポンプには外付け部品が不要で、最低 2.7V の電源で動作できます。

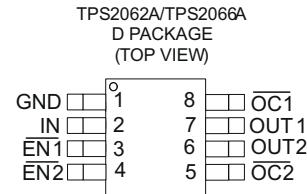
各デバイスは、出力負荷が電流制限スレッショルドを超えたとき、あるいは短絡が存在するときに、定電流モードに切り替わることにより、出力電流を安全なレベルに制限します。個々のチャネルは、対応する  $\overline{OCx}$  出力 (アクティブ Low) をアサートすることで過電流状態の存在を示します。過熱保護回路は、過電流または短絡イベント中にデバイスをディセーブルにし、永続的な損傷を防止します。デバイスの温度が十分に低下すると、デバイスは自動的にサーマル シャットダウンから回復します。デバイスには低電圧誤動作防止機能があり、入力電圧が 2.0V を超えるまでデバイスをディセーブルにします。TPS206xA は、電流制限がチャネルあたり標準 1.6A になるように設計されています。

GENERAL SWITCH CATALOG						
<b>33 mΩ, single</b>	<b>80 mΩ, single</b>	<b>80 mΩ, dual</b>	<b>80 mΩ, dual</b>	<b>80 mΩ, triple</b>	<b>80 mΩ, quad</b>	<b>80 mΩ, quad</b>
TPS201xA 0.2A - 2A TPS202x 0.2A - 2A TPS203x 0.2A - 2A	TPS2014 600 mA TPS2015 1 A TPS2041B 500 mA TPS2051B 500 mA TPS2045A 250 mA TPS2049 100 mA TPS2055A 250 mA TPS2061 1 A TPS2065 1 A TPS2068 1.5 A TPS2069 1.5 A	TPS2042B 500 mA TPS2052B 500 mA TPS2046B 250 mA TPS2056 250 mA TPS2062 1 A TPS2066 1 A TPS2060 1.5 A TPS2064 1.5 A	TPS2080 500 mA TPS2081 500 mA TPS2082 500 mA TPS2090 250 mA TPS2066 1 A TPS2060 1.5 A TPS2064 1.5 A	TPS2043B 500 mA TPS2053B 500 mA TPS2047B 250 mA TPS2057A 250 mA TPS2091 250 mA TPS2092 250 mA	TPS2044B 500 mA TPS2054B 500 mA TPS2063 1 A TPS2067 1 A	TPS2085 500 mA TPS2086 500 mA TPS2087 500 mA TPS2095 250 mA TPS2096 250 mA TPS2097 250 mA

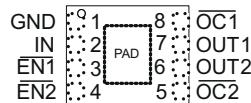
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## 4 Pin Configuration and Functions



TPS2062A/TPS2066A  
DRB PACKAGE  
(TOP VIEW)



Enable inputs are active low for all TPS2062A  
and active high for all TPS2066A

表 4-1. Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	TPS2062A	TPS2066A		
EN1	3	—	I	Enable input, logic low turns on power switch IN-OUT1
EN2	4	—	I	Enable input, logic low turns on power switch IN-OUT2
EN1	—	3	I	Enable input, logic high turns on power switch IN-OUT1
EN2	—	4	I	Enable input, logic high turns on power switch IN-OUT2
GND	1	1		Ground
IN	2	2	I	Input voltage
OC1	8	8	O	Channel 1 over-current indicator; the output is open-drain, active low type
OC2	5	5	O	Channel 2 over-current indicator; the output is open-drain, active low type
OUT1	7	7	O	Power-switch output, IN-OUT1
OUT2	6	6	O	Power-switch output, IN-OUT2
PowerPAD™ (1)	PAD	PAD		Connect PowerPAD to GND for proper operation (DRB package only)

(1) The PowerPad must be connected externally to GND pin to meet qualifying conditions for CB Certificate (DRB package only)

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating temperature range unless otherwise noted<sup>(1) (2)</sup>

			VALUE	UNIT
$V_I$	Input voltage range	IN	–0.3 to 6	V
$V_O$	Output voltage range	OUTx	–0.3 to 6	V
$V_I$	Input voltage range	$\overline{EN_x}$ , $EN_x$	–0.3 to 6	V
	Voltage range	OCx	–0.3 to 6	V
$I_O$	Continuous output current	OUTx	Internally limited	
$T_J$	Operating junction temperature range		–40 to 125	°C
$T_{stg}$	Storage temperature range		–65 to 150	°C
ESD	Electrostatic discharge protection	Human body model MIL-STD-883C	2	kV
		Charge device model (CDM)	500	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to GND.

### 5.2 Recommended Operating Conditions

		MIN	MAX	UNIT
$V_I$	Input voltage, IN	2.7	5.5	V
	Input voltage, $\overline{EN_x}$ , $EN_x$	0	5.5	V
$I_O$	Continuous output current, OUTx	0	1	A
$T_J$	Operating virtual junction temperature	–40	125	°C

### 5.3 Thermal Information

THERMAL METRIC <sup>(1)</sup>	D (SOIC)	DRB (SON)	UNIT
	8 PINS	8 PINS	
$R_{\theta JA}$	119.3	47.5	°C/W <sup>(2)</sup>
$R_{\theta JC(\text{top})}$	67.6	53	
$R_{\theta JB}$	59.6	14.2	
$\Psi_{JT}$	20.3	1.2	
$\Psi_{JB}$	59.1	14.2	
$R_{\theta JC(\text{bot})}$	N/A	7.3	

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

### 5.4 Electrical Characteristics

over recommended operating junction temperature range,  $V_I = 5.5$  V,  $I_O = 1$  A,  $V_{ENx} = 0$  V (TPS2062A) or  $V_{ENx} = 5.5$  V (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>(1)</sup>		MIN	TYP	MAX	UNIT
<b>POWER SWITCH</b>						
$r_{DS(\text{on})}$	Static drain-source on-state resistance $2.7 \text{ V} \leq V_I \leq 5.5 \text{ V}$ , $I_O = 1 \text{ A}$		$T_J = 25^\circ\text{C}$ $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	70	100	$\text{m}\Omega$
					135	

## 5.4 Electrical Characteristics (続き)

over recommended operating junction temperature range,  $V_I = 5.5\text{ V}$ ,  $I_O = 1\text{ A}$ ,  $V_{ENx} = 0\text{ V}$  (TPS2062A) or  $V_{ENx} = 5.5\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>(1)</sup>		MIN	TYP	MAX	UNIT	
$t_r$	Rise time, output	$V_I = 5.5\text{ V}$	$C_L = 1\text{ }\mu\text{F}$ , $R_L = 5\text{ }\Omega$ , $T_J = 25^\circ\text{C}$	0.6	1.5	1.5	ms	
		$V_I = 2.7\text{ V}$		0.4	1	1		
$t_f$	Fall time, output	$V_I = 5.5\text{ V}$	$C_L = 100\text{ }\mu\text{F}$ , $R_L = 5\text{ }\Omega$	0.05	0.5	0.5	ms	
		$V_I = 2.7\text{ V}$		0.05	0.5	0.5		
<b>ENABLE INPUT EN OR EN</b>								
$V_{IH}$	High-level input voltage	$2.7\text{ V} \leq V_I \leq 5.5\text{ V}$		2			V	
$V_{IL}$	Low-level input voltage					0.8		
$I_I$	Input current			-0.5	0.5	0.5	$\mu\text{A}$	
$t_{on}$	Turnon time	$C_L = 100\text{ }\mu\text{F}$ , $R_L = 5\text{ }\Omega$				3	ms	
$t_{off}$	Turnoff time					3		
<b>CURRENT LIMIT</b>								
$I_{os}$	Short-circuit output current per channel	$V_I = 5\text{ V}$ , OUTx connected to GND, device enabled into short-circuit	$T_J = 25^\circ\text{C}$	1.2	1.6	2.0	A	
			$-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	1.1	1.6	2.1		
$I_{oc}$ <sup>(2)</sup>	Overcurrent trip threshold	$V_{IN} = 5\text{ V}$	TPS2062ADRB, TPS2066AD, TPS2066ADRB	$I_{os}$	2.1	2.45	A	
$I_{os\_G}$	Ganged short-circuit output current	$V_I = 5\text{ V}$ , OUT1 & OUT2 connected to GND, device enabled into short-circuit	$T_J = 25^\circ\text{C}$	2.4	3.2	4.0	A	
			$-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	2.2	3.2	4.2		
$I_{oc\_G}$ <sup>(2)</sup>	Ganged overcurrent trip threshold	$V_I = 5\text{ V}$ , OUT1 & OUT2 tied together	TPS2062ADRB, TPS2066AD, TPS2066ADRB	$I_{os\_G}$	4.2	4.9		
<b>SUPPLY CURRENT (All devices excluding TPS2062AD)</b>								
$I_{IL}$	Supply current, device disabled	No load on OUT	$T_J = 25^\circ\text{C}$	0.5	1		$\mu\text{A}$	
			$-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	0.5	5	5		
$I_{IH}$	Supply current, device enabled	No load on OUT	$T_J = 25^\circ\text{C}$	50	60		$\mu\text{A}$	
			$-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	50	75	75		
$I_{lkg}$	Leakage current, device disabled	OUT connected to ground	$-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	1		1	$\mu\text{A}$	
Reverse leakage current	$V_O = 5.5\text{ V}$ , $V_I = 0\text{ V}$		$T_J = 25^\circ\text{C}$	0.2		0.2	$\mu\text{A}$	
<b>SUPPLY CURRENT (TPS2062AD)</b>								
$I_{IL}$	Supply current, device disabled	No load on OUT	$T_J = 25^\circ\text{C}$	0.5	1		$\mu\text{A}$	
			$-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	0.5	5	5		
$I_{IH}$	Supply current, device enabled	No load on OUT	$T_J = 25^\circ\text{C}$	95	120		$\mu\text{A}$	
			$-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	95	120	120		
$I_{lkg}$	Leakage current, device disabled	OUT connected to ground	$-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	1		1	$\mu\text{A}$	
Reverse leakage current	$V_O = 5.5\text{ V}$ , $V_I = 0\text{ V}$		$T_J = 25^\circ\text{C}$	0.2		0.2	$\mu\text{A}$	
<b>UNDERVOLTAGE LOCKOUT (All devices excluding TPS2062AD)</b>								
Low-level input voltage, IN	$V_I$ rising			2	2.5	V		
Hysteresis, IN	$V_I$ falling			75		mV		
<b>UNDERVOLTAGE LOCKOUT (TPS2062AD)</b>								
Low-level input voltage, IN	$V_I$ rising			2	2.6	V		
Hysteresis, IN	$V_I$ falling			75		mV		
<b>OVERCURRENT FLAG</b>								
$V_{OL}$	Output low voltage, OC	$I_{OCx} = 5\text{ mA}$			0.4	V		
Off-state current		$V_{OCx} = 5.0\text{ V}$ or $3.3\text{ V}$			1	$\mu\text{A}$		
OC deglitch		OCx assertion or de-assertion		4	8	15	ms	
<b>THERMAL SHUTDOWN<sup>(3)</sup></b>								
Thermal shutdown threshold				135			$^\circ\text{C}$	
Recovery from thermal shutdown				125			$^\circ\text{C}$	

## 5.4 Electrical Characteristics (続き)

over recommended operating junction temperature range,  $V_I = 5.5$  V,  $I_O = 1$  A,  $V_{ENx} = 0$  V (TPS2062A) or  $V_{ENx} = 5.5$  V (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>(1)</sup>	MIN	TYP	MAX	UNIT
Hysteresis			10		°C

(1) Pulsed load testing used to maintain junction temperature close to ambient

(2) TPS2062AD does not have an overcurrent trip threshold. The current limit is defined by  $I_{OS}$ . See [セクション 7.3](#) for more details.

(3) The thermal shutdown only reacts under overcurrent conditions.

## 5.5 Typical Characteristics

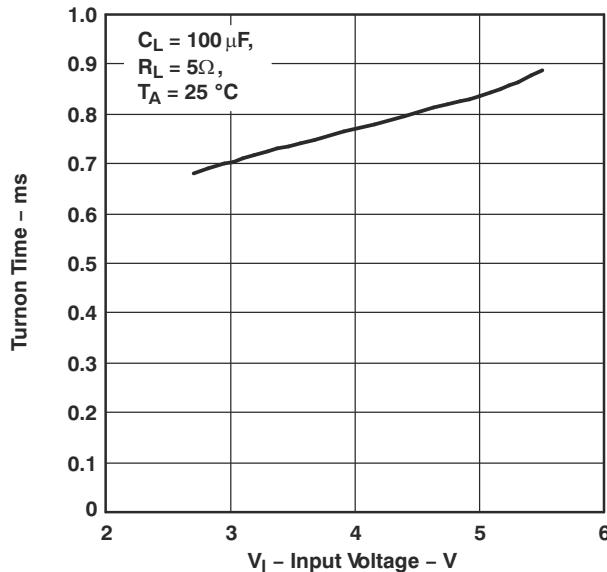


図 5-1. Turnon Time vs Input Voltage

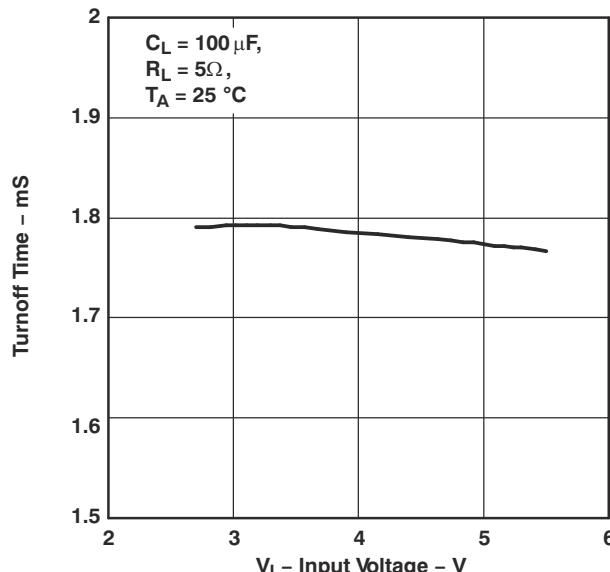


図 5-2. Turnoff Time vs Input Voltage

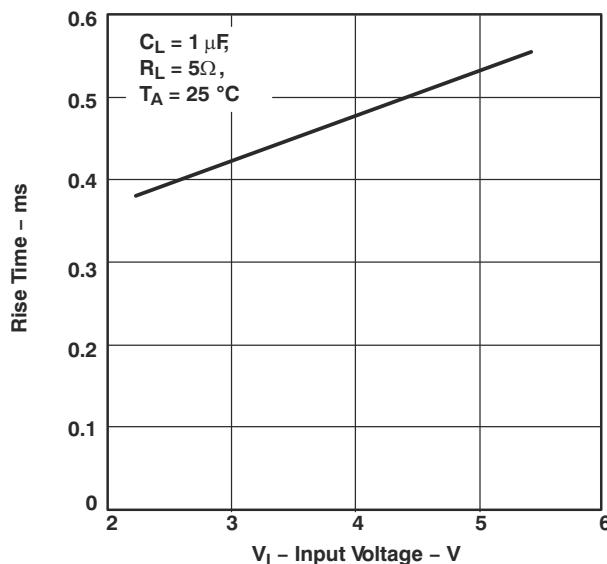


図 5-3. Rise Time vs Input Voltage

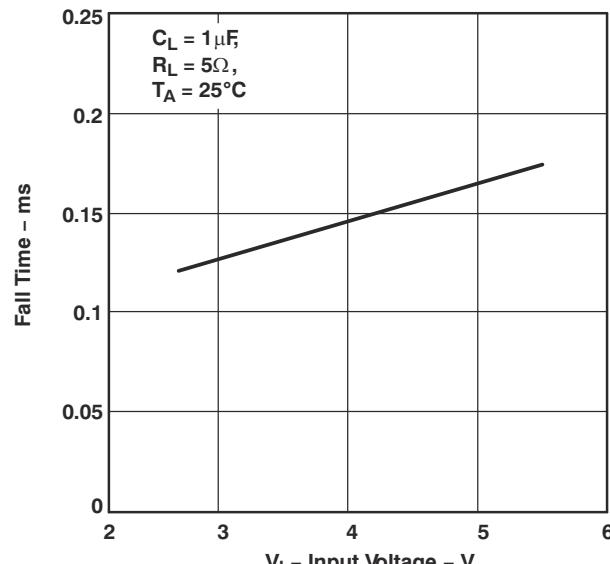


図 5-4. Fall Time vs Input Voltage

## 5.5 Typical Characteristics (continued)

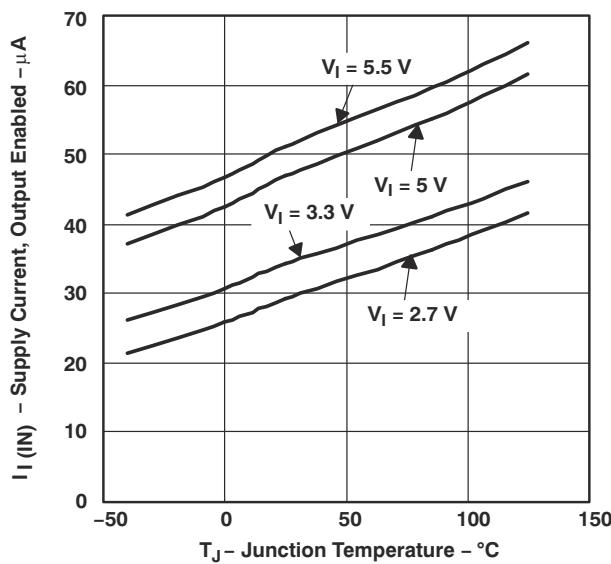


FIG 5-5. TPS2062A, TPS2066A Supply Current, Output Enabled vs Junction Temperature

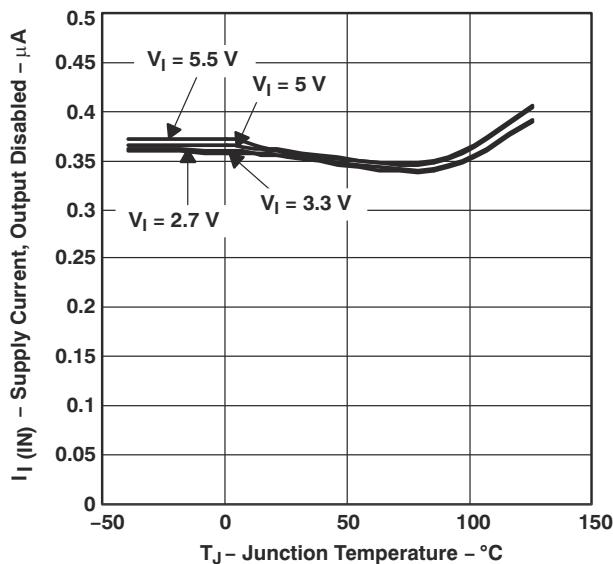


FIG 5-6. TPS2062A, TPS2066A Supply Current, Output Disabled vs Junction Temperature

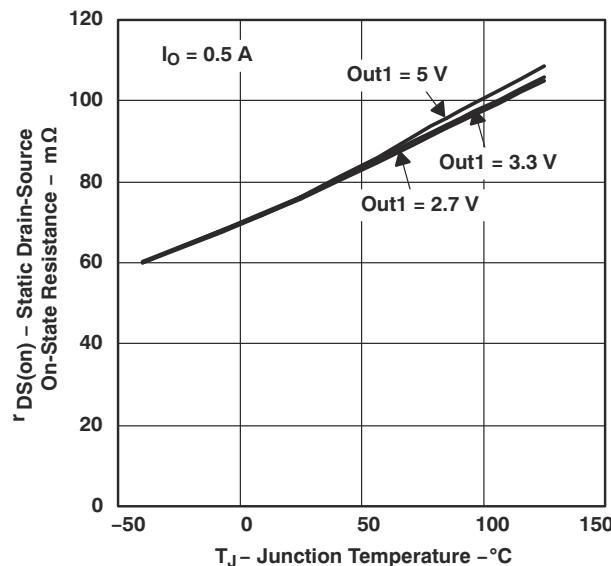


FIG 5-7. Static Drain-Source On-State Resistance vs Junction Temperature

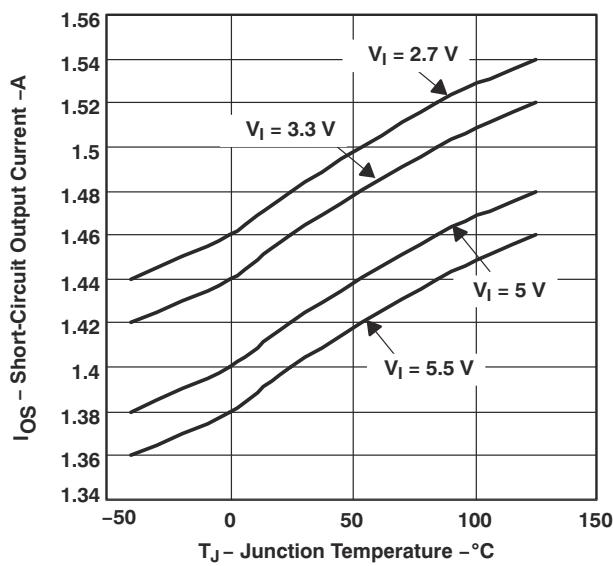


FIG 5-8. Short-Circuit Output Current vs Junction Temperature

## 5.5 Typical Characteristics (continued)

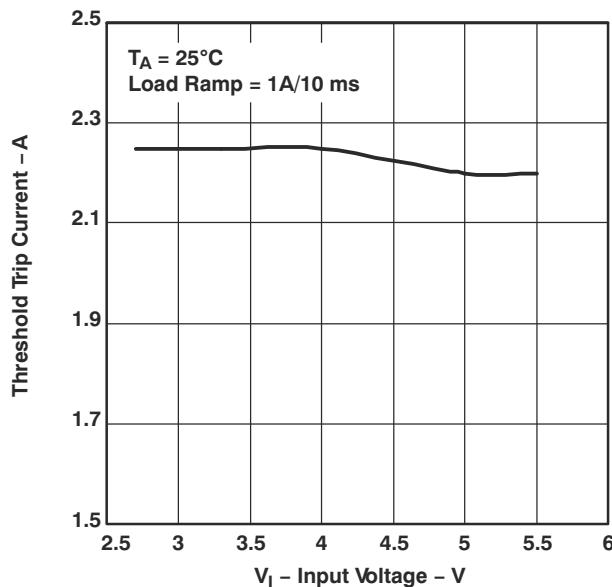


图 5-9. Threshold Trip Current vs Input Voltage

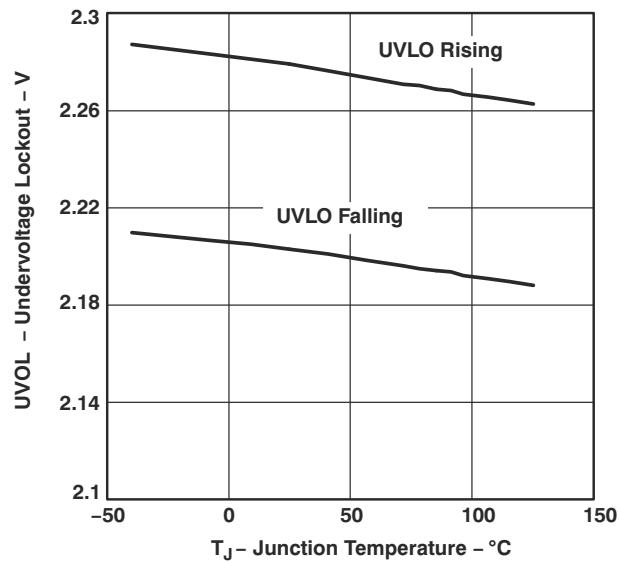


图 5-10. Undervoltage Lockout vs Junction Temperature

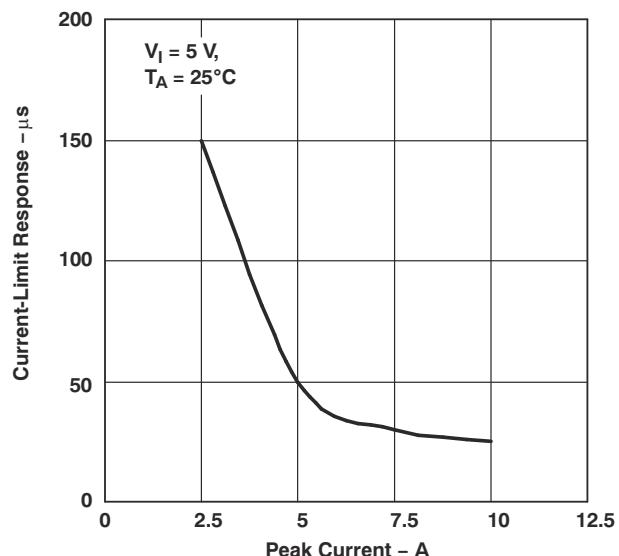


图 5-11. Current-Limit Response vs Peak Current

## 6 Parameter Measurement Information

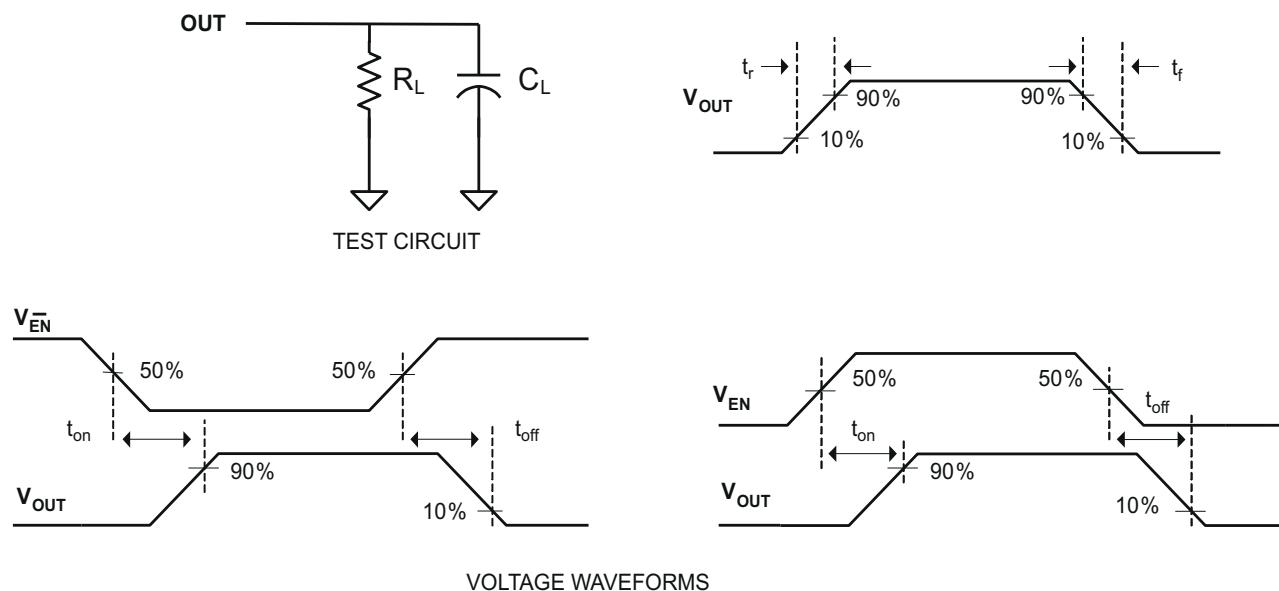


図 6-1. Test Circuit and Voltage Waveforms

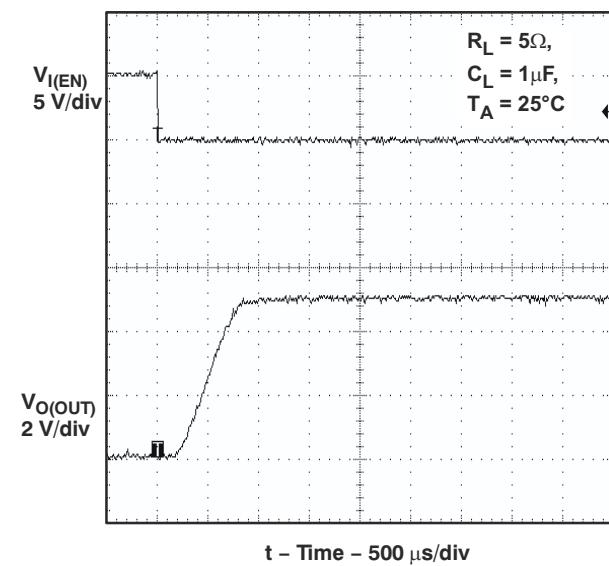


図 6-2. Turnon Delay and Rise Time With 1- $\mu$ F Load

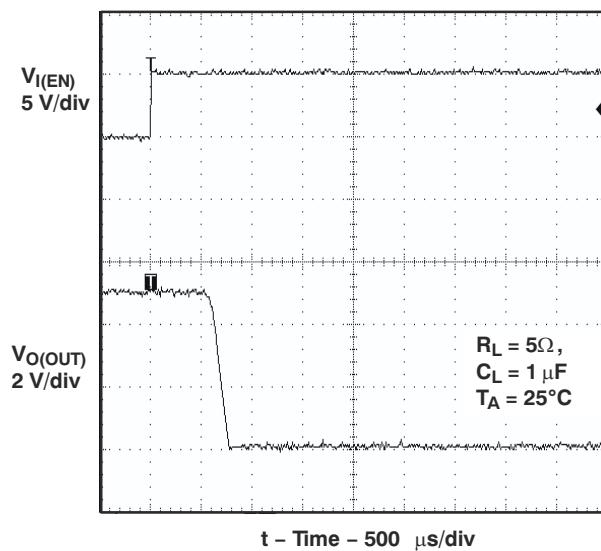


図 6-3. Turnoff Delay and Fall Time With 1- $\mu$ F Load

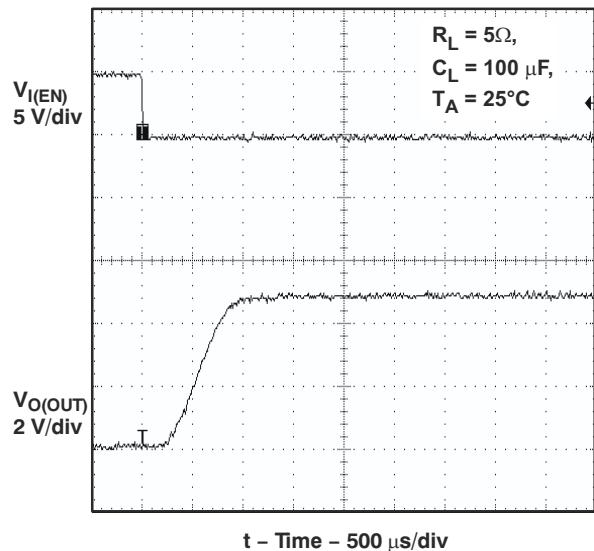


図 6-4. Turnon Delay and Rise Time With 100- $\mu$ F Load

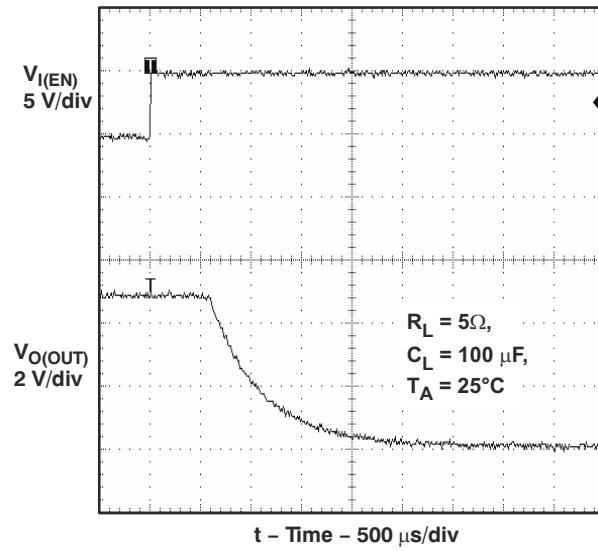


図 6-5. Turnoff Delay and Fall Time With 100- $\mu$ F Load

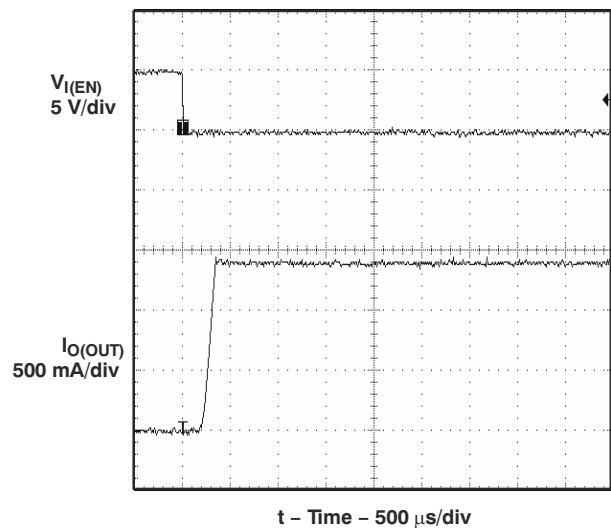


図 6-6. Short-Circuit Current, Device Enabled Into Short

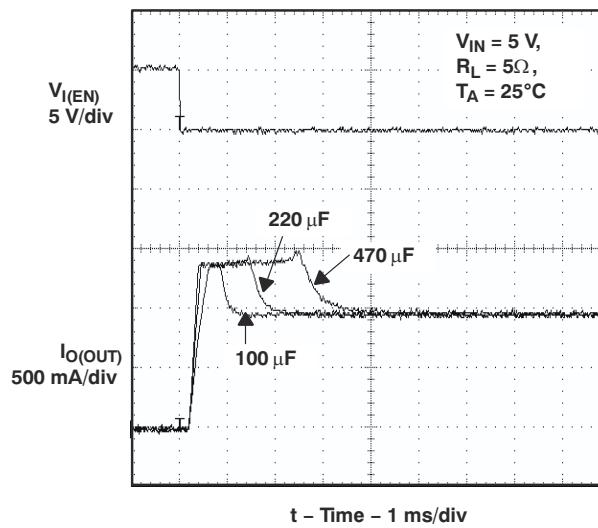


図 6-7. Inrush Current With Different Load Capacitance

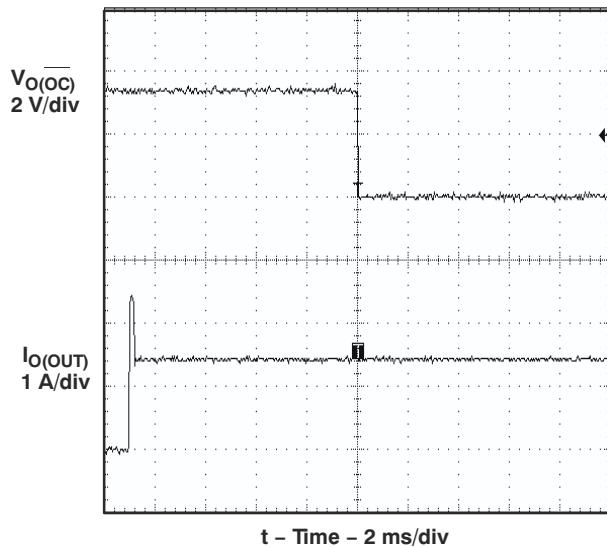


図 6-8. 2-Ω Load Connected to Enabled Device

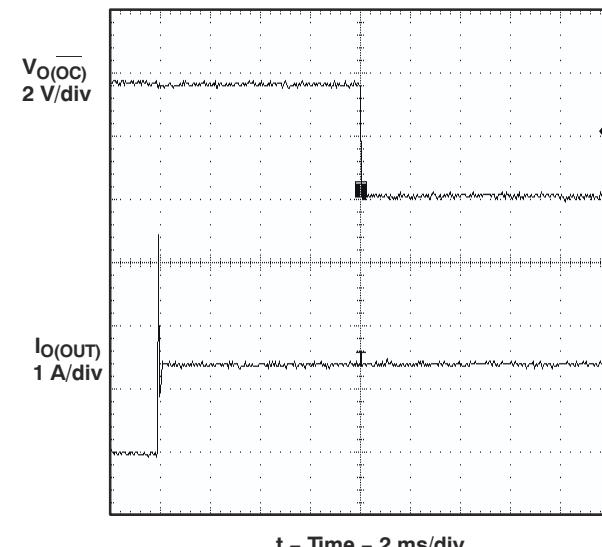


図 6-9. 1-Ω Load Connected to Enabled Device

## 7 Detailed Description

表 7-1. Package Information

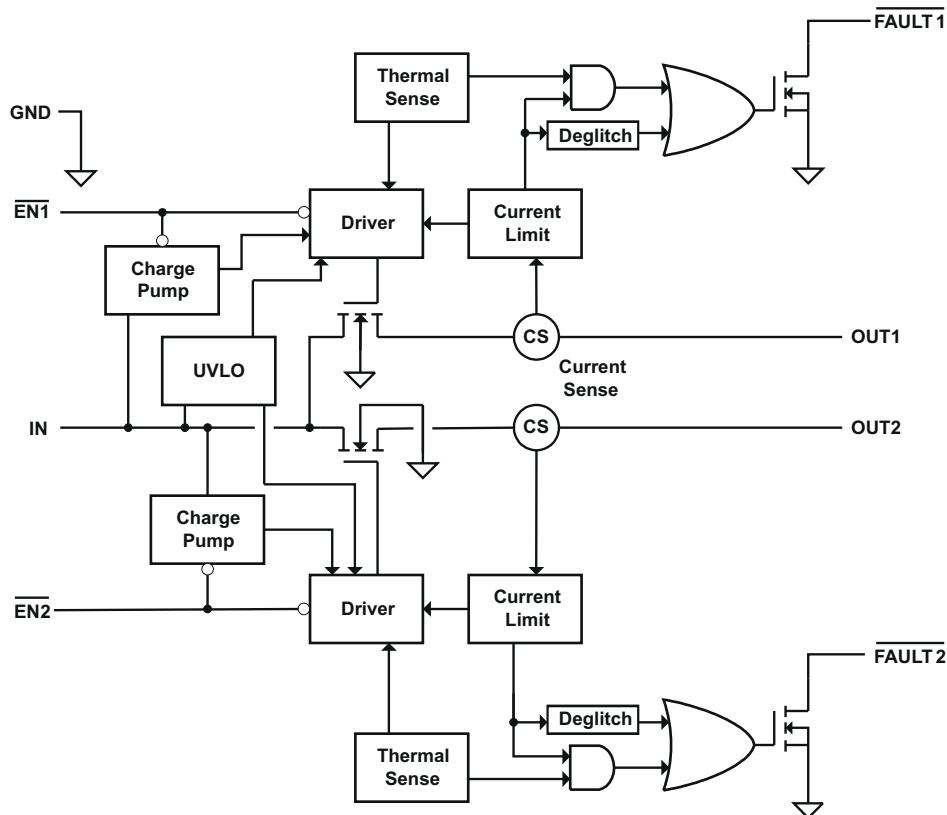
T <sub>A</sub>	ENABLE	RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT	TYPICAL SHORT-CIRCUIT LIMIT	PACKAGE <sup>(1)</sup>			
				D-8 (SOIC)		DRB-8 (SON)	
				PART #	STATUS	PART #	STATUS
-40°C to 85°C	Active low	1 A	1.6 A	TPS2062AD	AVAILABLE	TPS2062ADRB	AVAILABLE
	Active high			TPS2066AD	AVAILABLE	TPS2066ADRB	AVAILABLE

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

### 7.1 Overview

The devices are current-limited, power distribution switches using N-channel MOSFETs for applications where short-circuits or heavy capacitive loads are encountered. These devices have a minimum fixed current-limit threshold above 1.1A allowing for continuous operation up to 1A per channel. Overtemperature protection is an additional device shutdown feature. Each device incorporates an internal charge pump and gate drive circuitry necessary to drive the N-channel MOSFETs. The charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7V and requires little supply current. The driver controls the gate voltage of the power switch. The driver incorporates circuitry that controls the rise and fall times of the output voltage to provide "soft-start" and to limit large current and voltage surges.

### 7.2 Functional Block Diagram



- A. Current sense
- B. Active low (EN<sub>x</sub>) for TPS2062A. Active high (EN<sub>x</sub>) for TPS2066A.

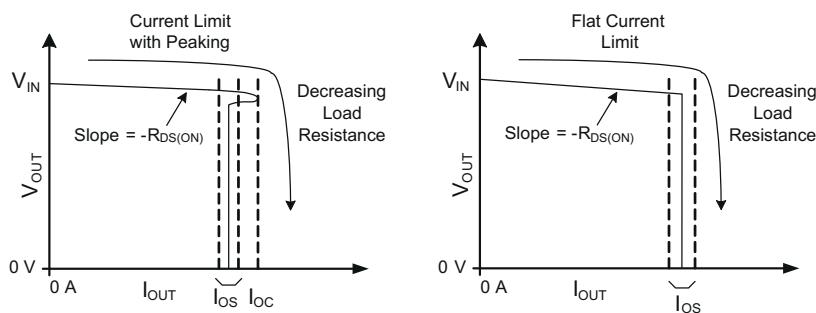
## 7.3 Overcurrent

A sense FET is employed to check for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

There are two kinds of current limit profiles for the TPS206xA devices.

The TPS2062ADRB, TPS2066ADRB, and TPS2066AD have an output I vs V characteristic similar to the plot labeled **Current Limit with Peaking** in [图 7-1](#). This type of limiting can be characterized by two parameters, the overcurrent trip threshold ( $I_{OC}$ ), and the short-circuit output current threshold ( $I_{OS}$ ).

The TPS2062AD has an output I vs V characteristic similar to the plot labeled **Flat Current Limit** in [图 7-1](#). This type of limiting can be characterized by one parameters, the short circuit current ( $I_{OS}$ ).



**图 7-1. Current Limit Profiles**

### 7.3.1 Overcurrent Conditions (TPS2062ADRB, TPS2066ADRB, and TPS2066AD)

Three possible overload conditions can occur for the TPS2062ADRB, TPS2066ADRB, and TPS2066AD. In the first condition, the output has been shorted before the device is enabled or before  $V_{I(IN)}$  has been applied (see [图 6-6](#) through [图 6-9](#)). The TPS2062ADRB, TPS2066ADRB, and TPS2066AD senses the short and immediately switches into a constant-current output.

In the second condition, a short or an overload occurs while the device is enabled. At the instant the overload occurs, high currents may flow for a short period of time before the current-limit circuit can react. After the current-limit circuit has tripped (reached the overcurrent trip threshold ( $I_{OC}$ )), the device switches into constant-current mode and current is limited at the short-circuit output current threshold ( $I_{OS}$ ).

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the overcurrent trip threshold ( $I_{OC}$ ) is reached or until the thermal limit of the device is exceeded. The TPS2062ADRB, TPS2066ADRB, and TPS2066AD are capable of delivering current up to the current-limit threshold without damaging the device. Once the overcurrent trip threshold ( $I_{OC}$ ) has been reached, the device switches into its constant-current mode current is limited at the short-circuit output current threshold ( $I_{OS}$ ).

### 7.3.2 Overcurrent Conditions (TPS2062AD)

Three possible overload conditions can occur for the TPS2062AD. In the first condition, the output has been shorted before the device is enabled or before  $V_{I(IN)}$  has been applied. The TPS2062AD senses the short and immediately switches into a constant-current output.

In the second condition, a short or an overload occurs while the device is enabled. At the instant the overload occurs, high currents may flow for a short period of time before the current-limit circuit can react. After the short-circuit output current threshold ( $I_{OS}$ ) is reached, the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. After the short-circuit output current threshold ( $I_{OS}$ ) is reached, the device switches into constant-current mode.

## 7.4 $\overline{OCx}$ Response

Each  $\overline{OCx}$  open-drain output is asserted (active low) during an overcurrent or overtemperature condition on that channel. The output remains asserted until the fault condition is removed. The TPS206xA eliminates false  $\overline{OCx}$  reporting by using internal delay circuitry after entering or leaving an overcurrent condition. This "deglitch" time is approximately 8-ms and ensures that  $\overline{OCx}$  is not accidentally asserted due to normal operation such as starting into a heavy capacitive load. Overtemperature conditions are not deglitched and assert and de-assert the  $\overline{OCx}$  signal immediately.

## 7.5 Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turn-on threshold. Built-in hysteresis prevents unwanted on/off cycling due to input voltage drop from large current surges.

## 7.6 Enable ( $\overline{ENx}$ or $ENx$ )

The logic enable controls the power switch, bias for the charge pump, driver, and other circuits to reduce the supply current. The supply current is reduced to less than 5  $\mu$ A when a logic high is present on  $\overline{ENx}$ , or when a logic low is present on  $ENx$ . A logic low input on  $\overline{ENx}$  or a logic high input on  $ENx$  enables the driver, control circuits, and power switch for that channel.

## 7.7 Thermal Sense

The TPS206xA monitors the operating temperature of both power distribution switches with individual thermal sensors. The junction temperature of each channel rises during an overcurrent or short-circuit condition. When the die temperature of a particular channel rises above a minimum of 135°C in an overcurrent condition, the internal thermal sense circuitry disables the individual channel in overtemperature to prevent damage. Hysteresis is built into the thermal sensor and re-enables the power switch individually after it has cooled approximately 10°C. The power switch cycles on and off until the fault is removed. This topology allows one channel to continue normal operation even if the other channel is in an overtemperature condition. The open-drain overcurrent flag (  $\overline{OCx}$  ) is asserted (active low) corresponding to the channel that is in an overtemperature or overcurrent condition.

## 8 Application Information

### 8.1 Power-Supply Considerations

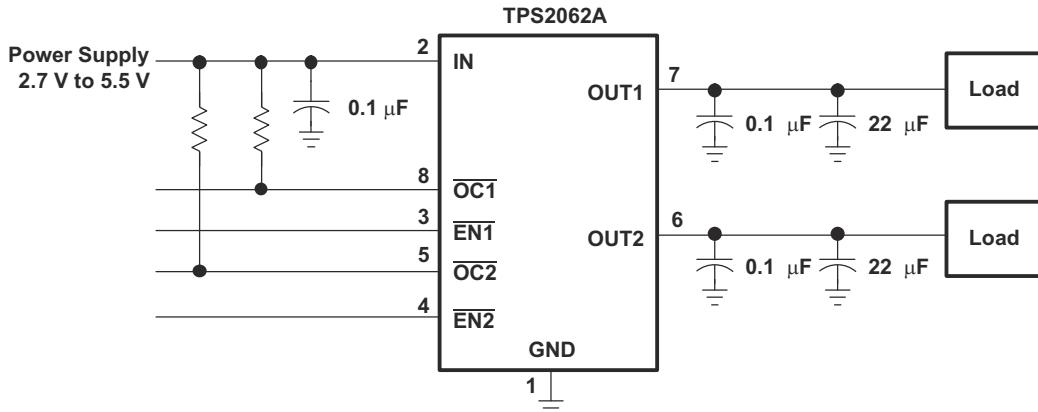


图 8-1. Typical Application

### 8.2 Input and Output Capacitance

Input and output capacitance improve the performance of the device; the actual capacitance must be optimized for the particular application. For all applications, a 0.01 μF to 0.1 μF ceramic bypass capacitor between IN and GND is recommended and must be placed as close to the device as possible for local noise de-coupling. This precaution reduces ringing on the input due to power-supply transients. Additional input capacitance may be needed on the input to reduce voltage overshoot from exceeding the absolute maximum voltage of the device during heavy transients.

Placing a high-value electrolytic capacitor on the output pin is recommended when the output load is heavy. Additionally, bypassing the output with a 0.01 μF to 0.1 μF ceramic capacitor improves the immunity of the device to short-circuit transients.

### 8.3 Power Dissipation and Junction Temperature

The low on-resistance of the N-channel MOSFETs allows the small surface-mount packages to pass large currents. It is good design practice to check power dissipation to ensure that the junction temperature of the device is within the recommended operating conditions. The below analysis gives an approximation for calculating junction temperature based on the power dissipation in the package. However, it is important to note that thermal analysis is strongly dependent on additional system level factors. Such factors include air flow, board layout, copper thickness and surface area, and proximity to other devices dissipating power. Good thermal design practice must include all system level factors in addition to individual component analysis.

The following procedure shows how to approximate the junction temperature rise due to power dissipation in a single channel. The TPS2062A/66A devices contain two channels, so the total device power must sum the power in each power switch.

Begin by determining the  $r_{DS(on)}$  of the N-channel MOSFET relative to the input voltage and operating temperature. Use the highest operating ambient temperature of interest and read  $r_{DS(on)}$  from the typical characteristics graph as an initial estimate. Power dissipation is calculated by:

$$P_D = r_{DS(on)} \times I_{OUT}^2$$

$$P_T = 2 \times P_D$$

Where:

$P_D$  = Power dissipation/channel (W)

$P_T$  = Total power dissipation for both channels (W)

$r_{DS(on)}$  = Power switch on-resistance ( $\Omega$ )

$I_{OUT}$  = Maximum current-limit threshold (A)

Finally, calculate the junction temperature:

$$T_J = P_T \times R_{\Theta JA} + T_A$$

Where:

$T_A$  = Ambient temperature °C

$R_{\Theta JA}$  = Thermal resistance (°C/W)

$P_T$  = Total power dissipation (W)

Compare the calculated junction temperature with the initial estimate. If they are not within a few degrees, repeat the calculation using the "refined"  $r_{DS(on)}$  from the previous calculation as the new estimate. Two or three iterations are generally sufficient to achieve the desired result. The final junction temperature is highly dependent on thermal resistance  $R_{\Theta JA}$ , and thermal resistance is highly dependent on the individual package and board layout. The "Dissipation Rating Table" at the beginning of this document provides example thermal resistances for specific packages and board layouts.

## 8.4 Universal Serial Bus (USB) Applications

One application for this device is for current-limiting in universal serial bus (USB) applications. The original USB interface was a 12-Mb/s or 1.5-Mb/s, multiplexed serial bus designed for low-to-medium bandwidth PC peripherals (for example, keyboards, printers, scanners, and mice). As the demand for more bandwidth increased, the USB 2.0 standard was introduced increasing the maximum data rate to 480-Mb/s. The four-wire USB interface is conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

USB data is a 3.3-V level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub across long cables. Each function must provide its own regulated 3.3 V from the 5-V input or its own internal power supply. The USB specification classifies two different classes of devices depending on its maximum current draw. A device classified as low-power can draw up to 100 mA as defined by the standard. A device classified as high-power can draw up to 500 mA. It is important that the minimum current limit threshold of the current-limiting power switch exceed the maximum current limit draw of the intended application. The latest USB standard must always be referenced when considering the current-limit threshold.

The USB specification defines two types of devices as hubs and functions. A USB hub is a device that contains multiple ports for different USB devices to connect and can be self-powered (SPH) or bus-powered (BPH). A function is a USB device that is able to transmit or receive data or control information over the bus. A USB function can be embedded in a USB hub. A USB function can be one of three types included in the list below.

- Low-power, bus-powered function
- High-power, bus-powered function
- Self-powered function

SPHs and BPHs distribute data and power to downstream functions. The TPS206x6A has higher current capability than required for a single USB port allowing it to power multiple downstream ports.

## 8.5 Self-powered and Bus-Powered Hubs

A SPH has a local power supply that powers embedded functions and downstream ports. This power supply must provide between 4.75 V to 5.25 V to downstream facing devices under full-load and no-load conditions. SPHs are required to have current-limit protection and must report overcurrent conditions to the USB controller. Typical SPHs are desktop PCs, monitors, printers, and stand-alone hubs.

A BPH obtains all power from an upstream port and often contains an embedded function. The hubs must power up with less than 100 mA. The BPH usually has one embedded function, and power is always available to the

controller of the hub. If the embedded function and hub require more than 100 mA on power up, the power to the embedded function may need to be kept off until enumeration is completed. This is accomplished by removing power or by shutting off the clock to the embedded function. Power switching the embedded function is not necessary if the aggregate power draw for the function and controller is less than 100 mA. The total current drawn by the bus-powered device is the sum of the current to the controller, the embedded function, and the downstream ports, and it is limited to 500 mA from an upstream port.

## 8.6 Low-Power Bus-Powered And High-Power Bus-Powered Functions

Both low-power and high-power bus-powered functions obtain all power from upstream ports. Low-power functions always draw less than 100 mA; high-power functions must draw less than 100 mA at power up and can draw up to 500 mA after enumeration. If the load of the function is more than the parallel combination of  $44\ \Omega$  and  $10\ \mu F$  at power up, the device must implement inrush current limiting.

## 8.7 USB Power-Distribution Requirements

USB can be implemented in several ways regardless of the type of USB device being developed. Several power-distribution features must be implemented.

- SPHs must:
  - Current-limit downstream ports
  - Report overcurrent conditions
- BPHs must:
  - Enable/disable power to downstream ports
  - Power up at <100 mA
  - Limit inrush current (<44  $\Omega$  and  $10\ \mu F$ )
- Functions must:
  - Limit inrush currents
  - Power up at <100 mA

The feature set of the TPS2062A/66A meets each of these requirements. The integrated current-limiting and overcurrent reporting is required by self-powered hubs. The logic-level enable and controlled rise times meet the need of both input and output ports on bus-powered hubs and the input ports for bus-powered functions.

## 9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[www.tij.co.jp](http://www.tij.co.jp) のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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### 9.5 用語集

#### テキサス・インスツルメンツ用語集

この用語集には、用語や略語の一覧および定義が記載されています。

## 10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

	Page
<b>Changes from Revision F (November 2008) to Revision G (June 2024)</b>	
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新.....	1
• 「消費電力定格」表を削除.....	1
• Updated 表 4-1 footnote about PowerPad .....	3
• Added セクション 5.3 .....	4
• Updated max UVLO for TPS2062A.....	4
• Updated max Supply current, high-level output values for TPS2062A.....	4
• Updated Overcurrent trip threshold to apply only to TPS2062ADRB, TPS2066ADRB, and TPS2066AD.....	4
• Updated セクション 7.3 .....	13
• Added セクション 7.3.1 .....	13
• Added セクション 7.3.2 .....	13

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS2062ADR	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2062A
TPS2062ADR.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2062A
TPS2062ADRBR	Active	Production	SON (DRB)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2062
TPS2062ADRBR.A	Active	Production	SON (DRB)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2062
TPS2062ADRBT	Active	Production	SON (DRB)   8	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2062
TPS2062ADRBT.A	Active	Production	SON (DRB)   8	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2062
TPS2066AD	Obsolete	Production	SOIC (D)   8	-	-	Call TI	Call TI	-40 to 125	2066A
TPS2066ADR	Obsolete	Production	SOIC (D)   8	-	-	Call TI	Call TI	-40 to 125	2066A
TPS2066ADRBR	Obsolete	Production	SON (DRB)   8	-	-	Call TI	Call TI	-40 to 125	2066
TPS2066ADRBT	Obsolete	Production	SON (DRB)   8	-	-	Call TI	Call TI	-40 to 125	2066

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

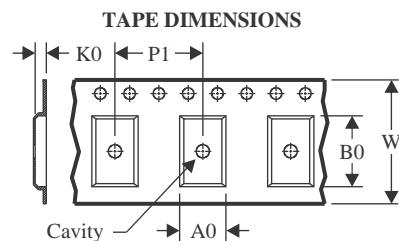
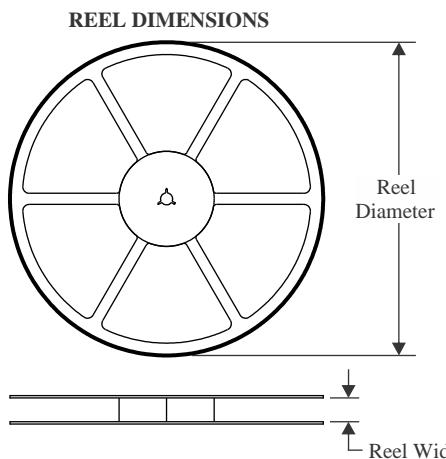
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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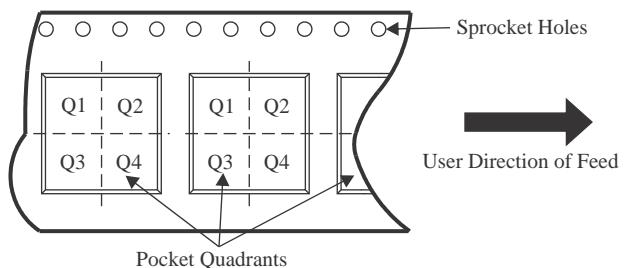
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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

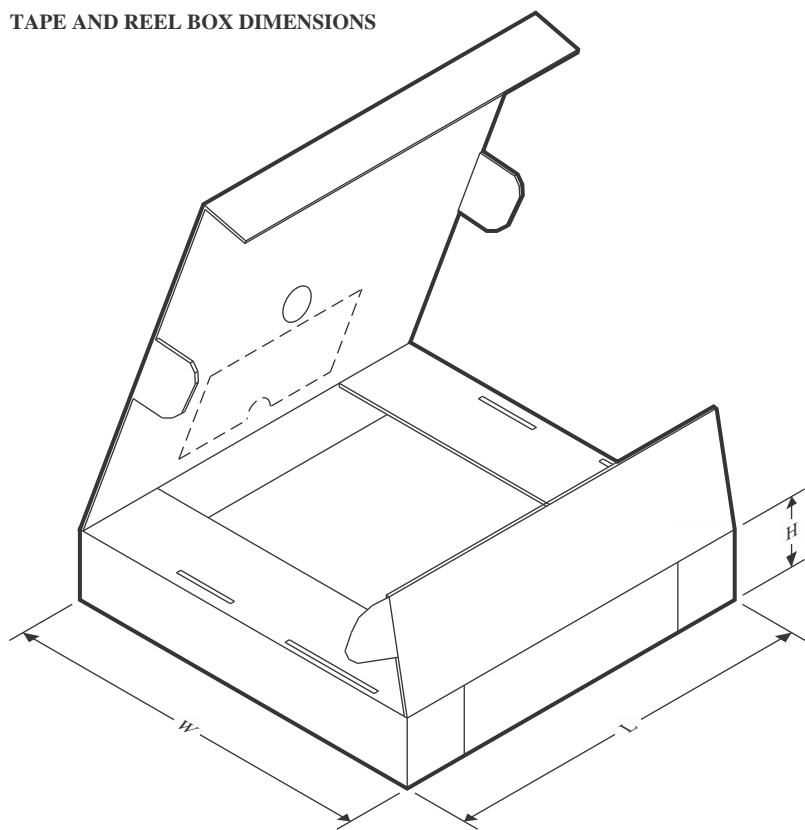
**TAPE AND REEL INFORMATION**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2062ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2062ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2062ADRB	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TPS2062ADRB	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2062ADR	SOIC	D	8	2500	353.0	353.0	32.0
TPS2062ADR	SOIC	D	8	2500	353.0	353.0	32.0
TPS2062ADRBR	SON	DRB	8	3000	346.0	346.0	35.0
TPS2062ADRBT	SON	DRB	8	250	200.0	183.0	25.0

## GENERIC PACKAGE VIEW

**DRB 8**

**VSON - 1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4203482/L

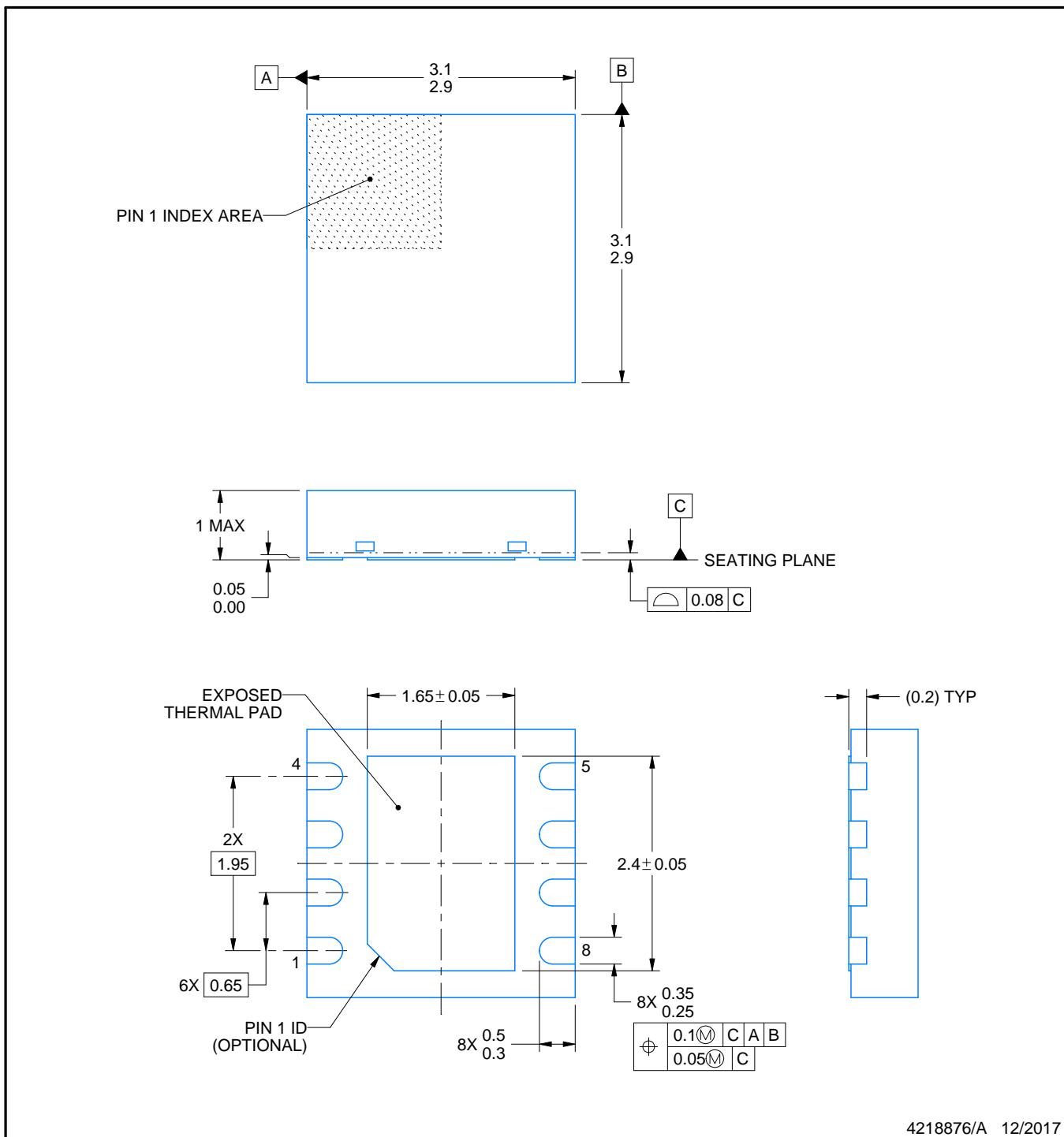


# PACKAGE OUTLINE

**DRB0008B**

**VSON - 1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



4218876/A 12/2017

**NOTES:**

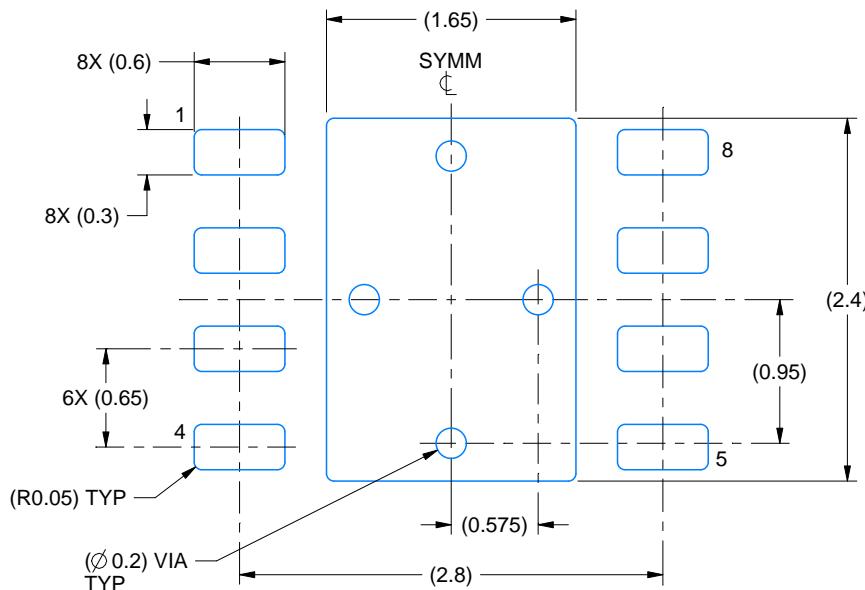
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

## EXAMPLE BOARD LAYOUT

**DRB0008B**

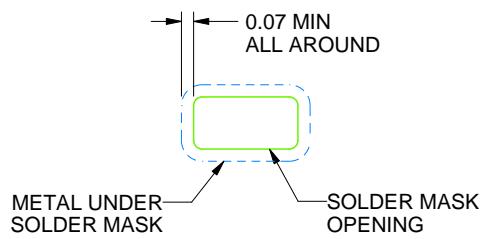
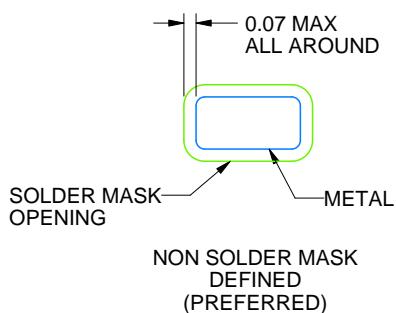
## VSON - 1 mm max height

## PLASTIC SMALL OUTLINE - NO LEAD



## LAND PATTERN EXAMPLE

SCALE:20X



## SOLDER MASK DETAILS

4218876/A 12/2017

#### NOTES: (continued)

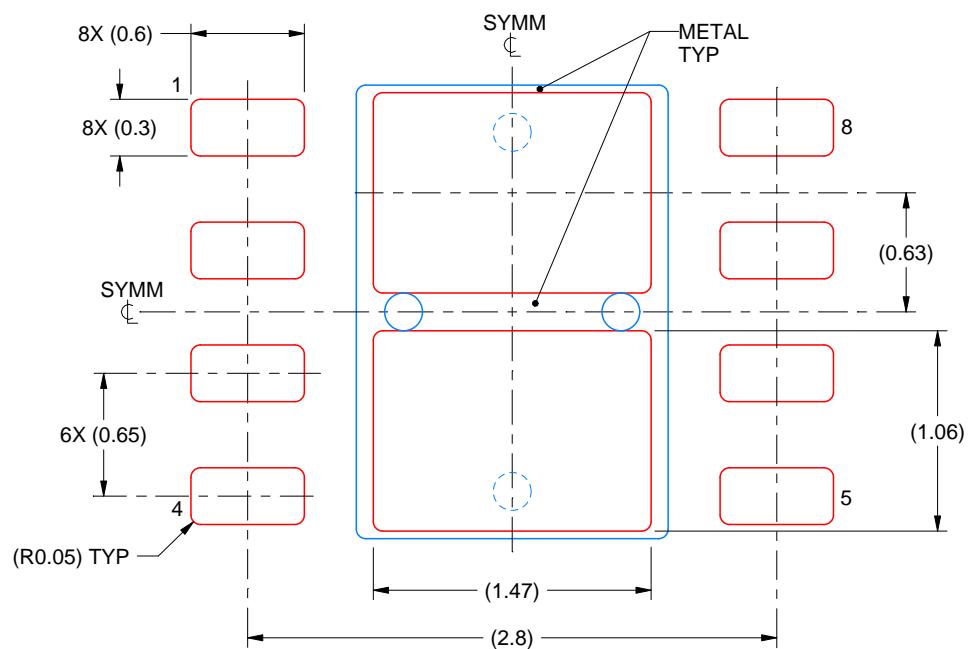
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

## EXAMPLE STENCIL DESIGN

**DRB0008B**

## VSON - 1 mm max height

### PLASTIC SMALL OUTLINE - NO LEAD



## SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
81% PRINTED SOLDER COVERAGE BY AREA  
SCALE:25X

4218876/A 12/2017

#### NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

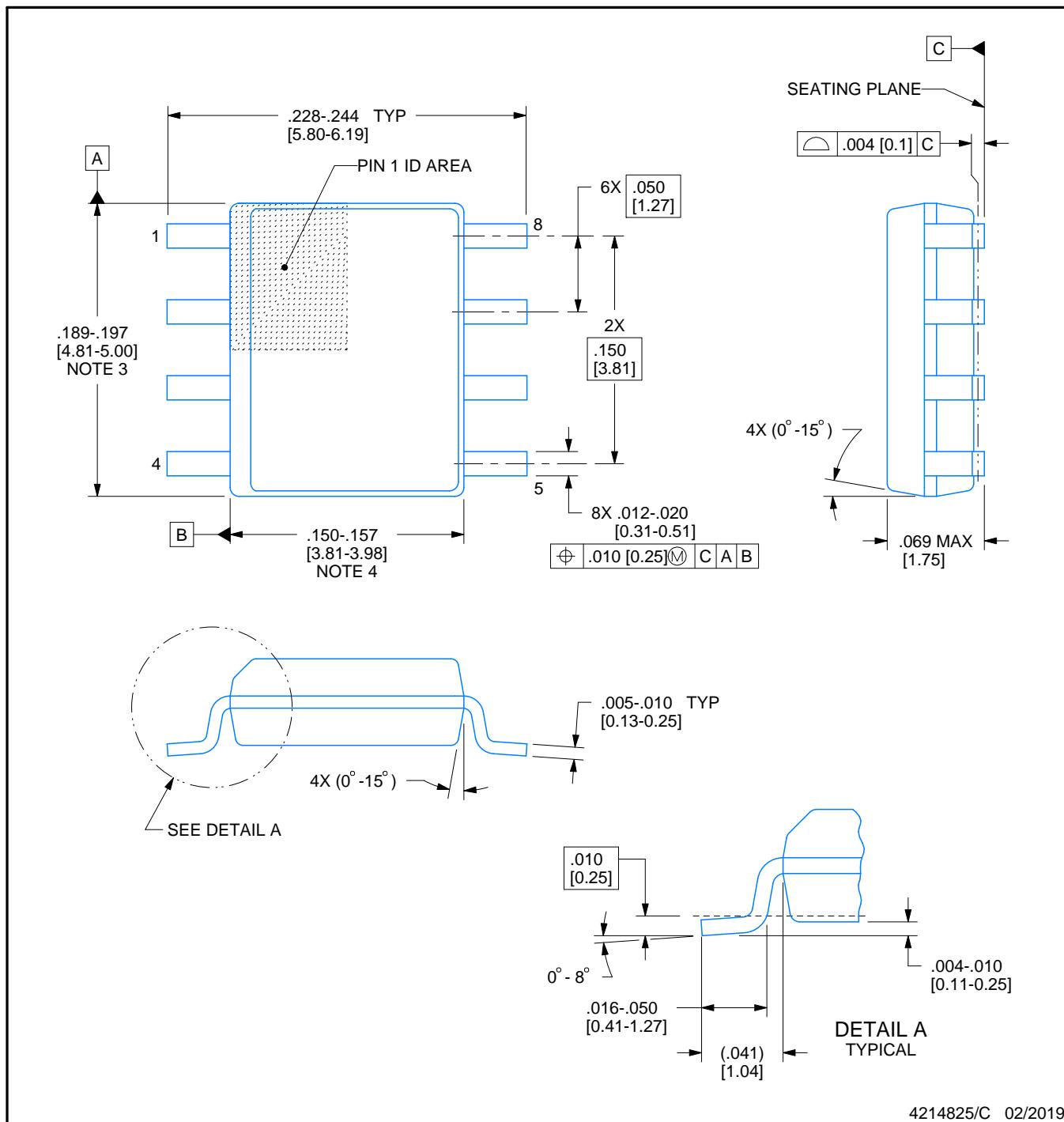


## PACKAGE OUTLINE

**D0008A**

## SOIC - 1.75 mm max height

## SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

## NOTES:

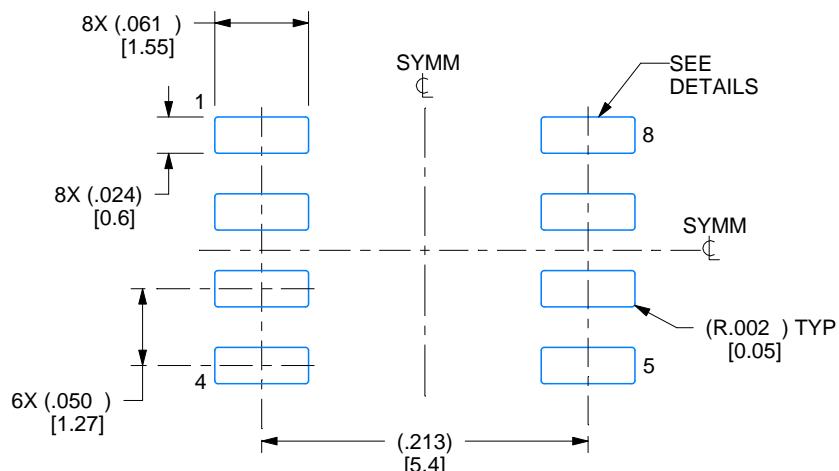
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

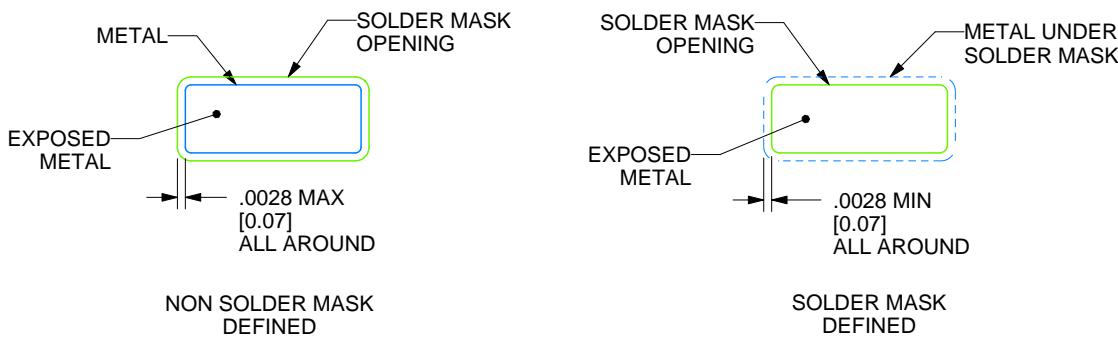
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

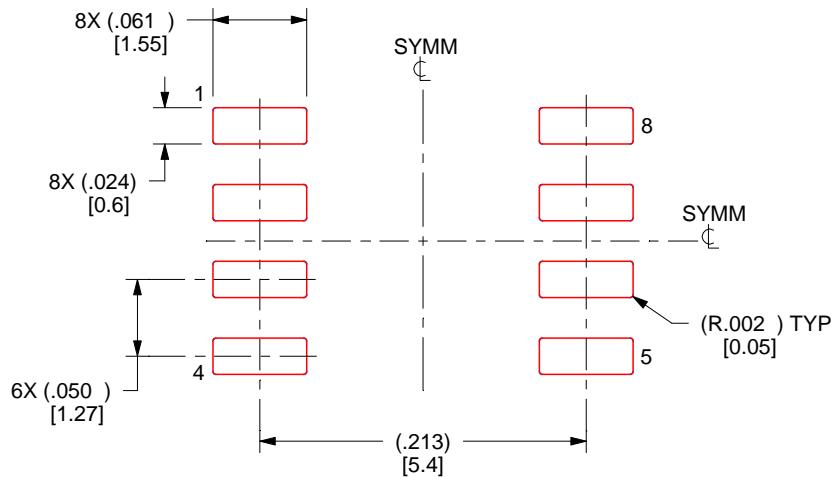
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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