TPS22971 3.6V、3A、6.7mΩオン抵抗、可変高速ターンオンおよびパワー・グッド搭載の負荷スイッチ

1 特長

- 入力電圧範囲: V_{IN} = 0.65V～3.6V
- オン抵抗
  - V_{IN} ≥ 1.8VにおいてR_{ON} = 6.7mΩ (標準値)
  - V_{IN} = 1.05VにおいてR_{ON} = 7.2mΩ (標準値)
  - V_{IN} = 0.65VにおいてR_{ON} = 8.9mΩ (標準値)
- 最大連続スイッチ電流(I_{MAX}): 3A
- ON状態(I_Q): 3.6V_{IN}において30µA (標準値)
- OFF状態(I_{SD}): 3.6V_{IN}において1µA (標準値)
- CTピンによりスルー・レートを変更可能
  - 高速ターンオン: V_{IN} = 1Vにおいて65µs以下
- スイッチ・オン後のパワー・グッド(PG)インジケータ
- 低いスレッショルド・イネーブル(ON): 0.9V (V_{IH})により、低電圧の制御ロジックを使用可能
- サーマル・シャットダウン(T_{SD})
- クイック出力放電(QOD): 150Ω (標準値)

2 アプリケーション

- ノートPC、タブレット
- 産業用PC
- スマートフォン
- テレコム
- ストレージ

3 概要

TPS22971は省スペースのシングル・チャネル負荷スイッチで、ターンオンのスルー・レートが制御され、変更可能で、またパワー・グッド・インジケータが組み込まれています。このデバイスにはNチャネルMOSFETが含まれており、0.65V～3.6Vの低い入力電圧範囲で動作し、最大3Aの連続電流をサポートできます。オン抵抗が6.7mΩと低いため、負荷スイッチでの電力損失と電圧降下が最小化されます。このスイッチは、オンおよびオフ入力(ON)により制御され、低電圧の制御信号と直接接続可能です。

TPS22971はデフォルトで、高速なターンオン時間によりスタートアップおよび待ち時間を最小にします。スルー・レートは変更可能で、スルー・レートを減らして突入電流を制限することもできます。パワー・グッド(PG)信号は、ゲートのスレッショルドを内部的に監視し、スイッチが完全にオンであることを示します。スイッチがディセーブルのときには、オンチップの150Ω抵抗により出力からグランドへ迅速に放電が行われ、フローティング状態になることを防止します。

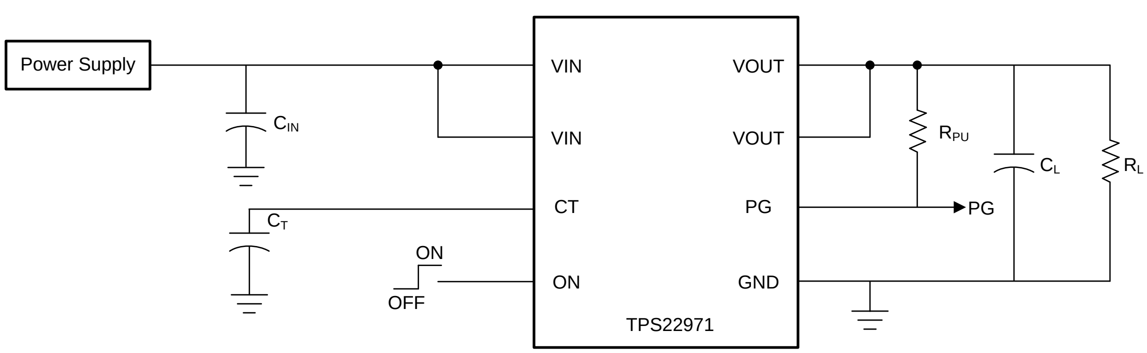
TPS22971は、超小型で省スペースの8ピンWCSPパッケージで供給され、-40℃～105℃の自由通気温度範囲で動作が規定されています。過熱が発生した場合、内蔵のサーマル・シャットダウンによりデバイスがオフになります。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TPS22971	DSBGA (8)	1.90mm×0.90mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

代表的なアプリケーション



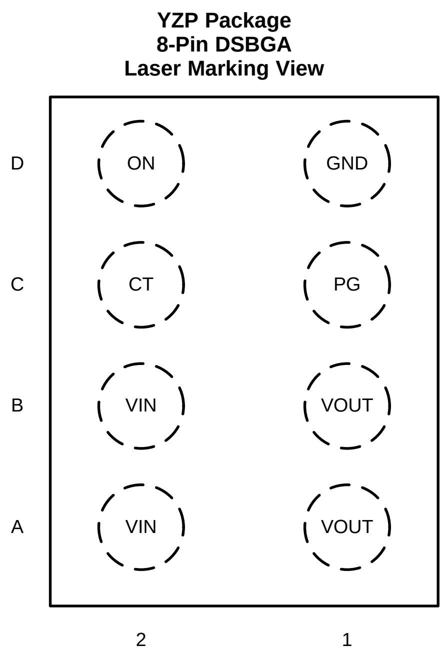
目次

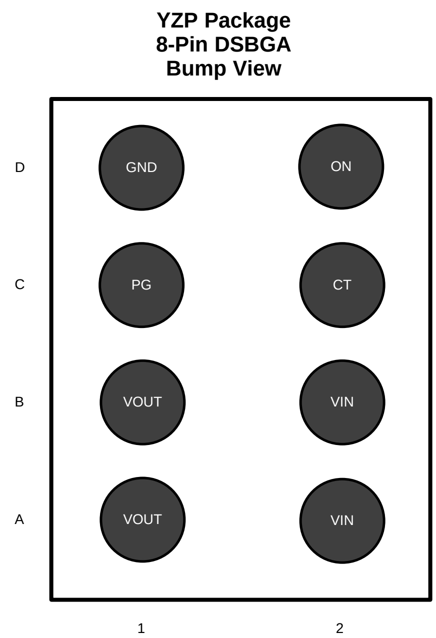
4 改訂履歴

2017年4月発行のものから更新	**Page**
• デバイスのステータスを「事前情報」から「量産データ」に 変更	1

Revision A (July 2017) から Revision B に変更	**Page**
• 「*製品情報*」表の型番からYZPTを 削除	1
• 「*特長*」の1.1µAを1µAに 変更	1
• 重複したパッケージの図を 削除	1

5 Pin Configuration and Functions





Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CT	C2	O	VOUT slew rate control. Adding capacitance from this pin to ground lowers the output slew rate
GND	D1	GND	Ground
ON	D2	I	Switch enable control input. Do not leave floating
PG	C1	O	Power Good Indication. Open drain releases when the switch is fully on
VOUT	A1, B1	O	Switch output
VIN	A2, B2	I	Switch input

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{IN}	Input voltage	–0.3	4	V
V_{OUT}	Output voltage	–0.3	4	V
V_{ON}	ON voltage	–0.3	4	V
V_{PG}	PG voltage	–0.3	4	V
I_{MAX}	Maximum continuous switch current		3	A
I_{PLS}	Maximum pulsed switch current, pulse < 300-µs, 2% duty cycle		4	A
T_J	Maximum junction temperature	Internally Limited		
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage	0.65	3.6	V
V_{OUT}	Output voltage		V_{IN}	V
V_{IH}	High-level input voltage, ON	0.9	3.6	V
V_{IL}	Low-level input voltage, ON	0	0.45	V
T_J	Operating temperature	–40	125	°C
T_A	Operating free-air temperature	–40	105	°C
C_T	CT pin capacitor voltage rating	7		V

6.4 Thermal Information

THERMAL METRIC[1]		TPS22971	UNIT
		YZP (DSBGA)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	130	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	51	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	50	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Unless otherwise noted, V_{IN} = 0.65 V to 3.6 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
I_Q	Quiescent current	V_{OUT} = Open, Switch enabled	V_{IN} > 1.2 V	–40°C to +85°C		30	65	µA
				–40°C to +105°C			75	
			V_{IN} ≤ 1.2 V	–40°C to +85°C		20	50	
				–40°C to +105°C			55	
I_{SD}	Shutdown current	V_{OUT} = GND, Switch disabled	V_{IN} > 1.8 V	–40°C to +85°C		1	7.5	µA
				–40°C to +105°C			18	
			V_{IN} ≤ 1.8 V	–40°C to +85°C		0.9	5.5	
				–40°C to +105°C			9.5	
R_{ON}	ON-resistance	I_{OUT} = –200 mA	V_{IN} ≥ 1.8 V	25°C		6.7	10	mΩ
				–40°C to +85°C			12	
				–40°C to +105°C			12	
			V_{IN} = 1.2 V	25°C		6.9	10	
				–40°C to +85°C			12	
				–40°C to +105°C			13	
			V_{IN} = 1.05 V	25°C		7.2	10.5	
				–40°C to +85°C			13	
				–40°C to +105°C			14	
			V_{IN} = 0.65 V	25°C		8.9	14	
				–40°C to +85°C			18	
				–40°C to +105°C			19	
R_{PD}	Output pull down resistance(1)	I_{OUT} = 3 mA, Switch disabled	V_{IN} = 3.6 V	–40°C to +105°C		150		Ω
			V_{IN} = 0.65 V	–40°C to +105°C		710		Ω
I_{ON}	ON input leakage current	V_{ON} =0 V to 3.6 V		–40°C to +105°C			0.1	µA
$I_{PG,LK}$	Leakage current into PG pin	V_{PG} = 0 V to 3.6 V	V_{ON} ≤ V_{IL}	–40°C to +105°C		0.1	8.5	µA
$V_{PG,OL}$	PG output low voltage	V_{PG} = 0 V to 3.6 V	V_{ON} ≥ V_{IH}, I_{PG} = 1 mA	–40°C to +105°C			0.2	V
T_{SD}	Thermal shutdown	T_J rising				170		°C
$T_{SD, HYS}$	Thermal shutdown hysteresis	T_J falling				30		°C

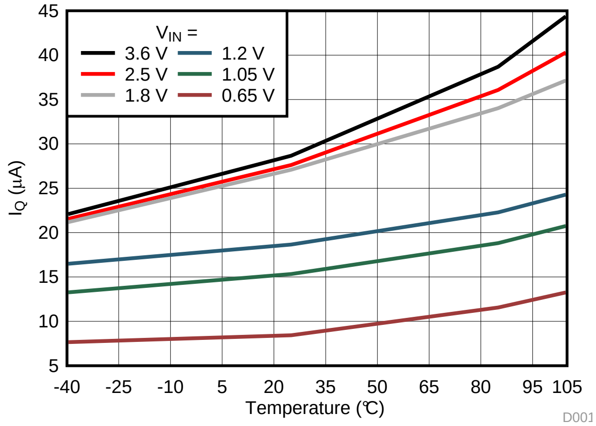
(1) See the *Quick Output Discharge (QOD)* section.

6.6 Switching Characteristics

All typical values are at 25°C unless otherwise noted

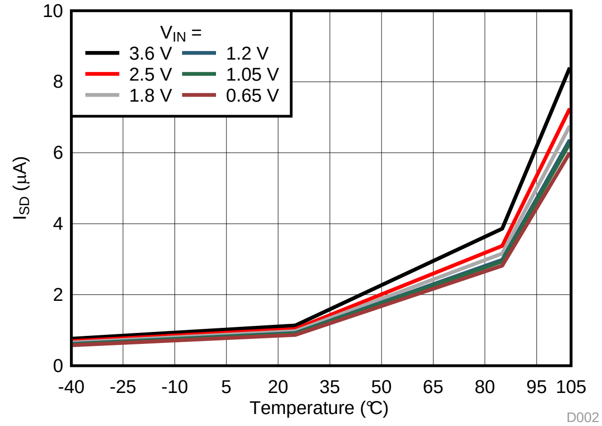
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN} = 3.6 V						
t_{ON}	Turn-On time	C_T = 0 pF		54		µs
		C_T = 1000 pF		198		
		C_T = 10000 pF		1520		
t_R	VOUT Rise time	C_T = 0 pF		35		
		C_T = 1000 pF		150		
		C_T = 10000 pF		1230		
$t_{PG,ON}$	PG Turn-On time	C_T = 0 pF		134		
		C_T = 1000 pF		314		
		C_T = 10000 pF		1990		
$t_{PG,OFF}$	PG Turn-Off time			1.9		
t_{OFF}	Turn-Off time			3.5		
t_F	VOUT Fall time	C_L = 0.1 µF, R_L = 10 Ω		2.1		
V_{IN} = 1.8 V						
t_{ON}	Turn-On time	C_T = 0 pF		41		µs
		C_T = 1000 pF		126		
		C_T = 10000 pF		857		
t_R	VOUT Rise time	C_T = 0 pF		21		
		C_T = 1000 pF		82		
		C_T = 10000 pF		628		
$t_{PG,ON}$	PG Turn-On time	C_T = 0 pF		105		
		C_T = 1000 pF		220		
		C_T = 10000pF		1230		
$t_{PG,OFF}$	PG Turn-Off time			0.8		
t_{OFF}	Turn-Off time			4.8		
t_F	VOUT Fall time	C_L = 0.1 µF, R_L = 10 Ω		2.1		
V_{IN} = 0.65 V						
t_{ON}	Turn-On time	C_T = 0 pF		54		µs
		C_T = 1000 pF		127		
		C_T = 10000 pF		720		
t_R	VOUT Rise time	C_T = 0 pF		21		
		C_T = 1000 pF		61		
		C_T = 10000 pF		386		
$t_{PG,ON}$	PG Turn-On time	C_T = 0 pF		165		
		C_T = 1000 pF		290		
		C_T = 10000 pF		1290		
$t_{PG,OFF}$	PG Turn-Off time			0.5		
t_{OFF}	Turn-Off time			55		
t_F	VOUT Fall time	C_L = 0.1 µF, R_L = 10 Ω		8		
V_{IN} = 1 V, T_A = 0°C to 85°C						
t_{ON}	Fast Turn-On time	C_T = 0 pF		30	65	µs

6.7 Typical DC Characteristics



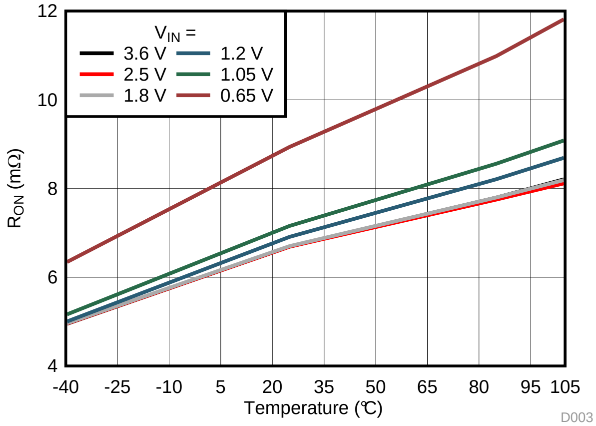
V_{ON} = 3.6 V I_{OUT} = 0

図 1. Quiescent Current vs Temperature



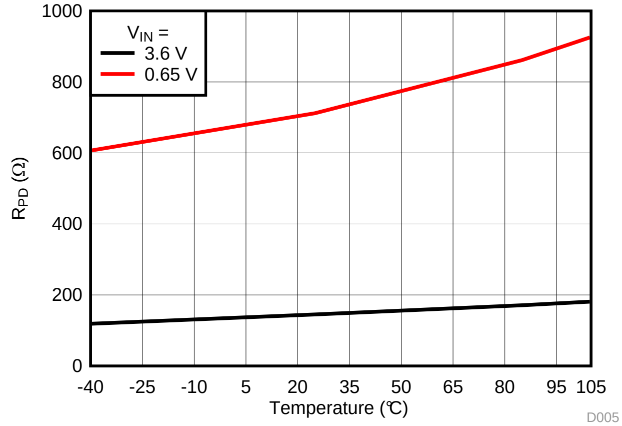
V_{ON} = 0 V V_{OUT} = 0

図 2. Input Shutdown Current vs Temperature



V_{ON} = 3.6 V I_{OUT} = -200 mA

図 3. On-Resistance vs Temperature



V_{ON} = 3.6 V Initially V_{OUT} = V_{IN}

図 4. Output Pull-Down Resistance vs Temperature

6.8 Typical AC Characteristics

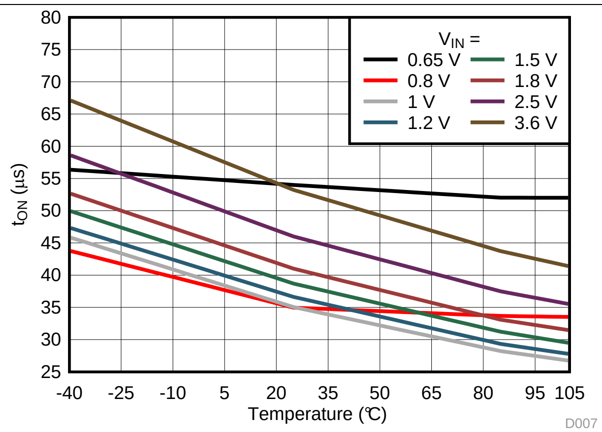
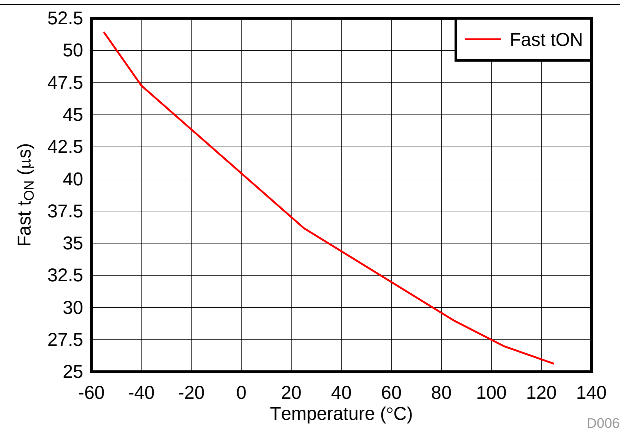


図 5. Turn-On Time vs Temperature



V_{IN} = 1V C_T = 0 pF C_L = 0.1 µF R_L = 10 Ω

図 6. Fast Turn-On Time vs Temperature

Typical AC Characteristics (continued)

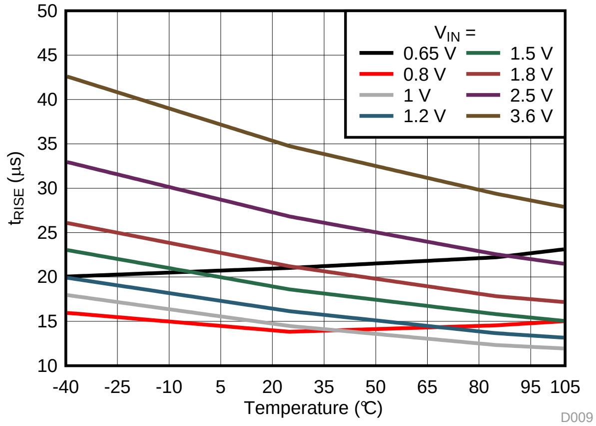


図 7. Rise Time vs Temperature

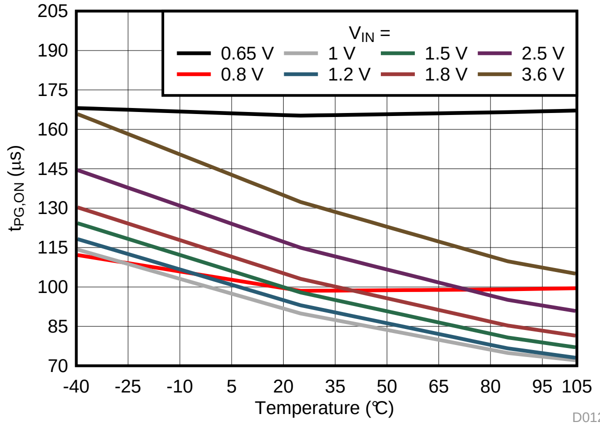


図 8. PG Turn-On Time vs Temperature

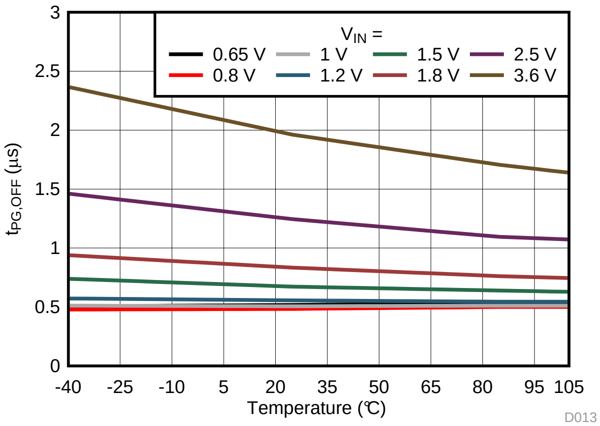


図 9. PG Turn-Off Time vs Temperature

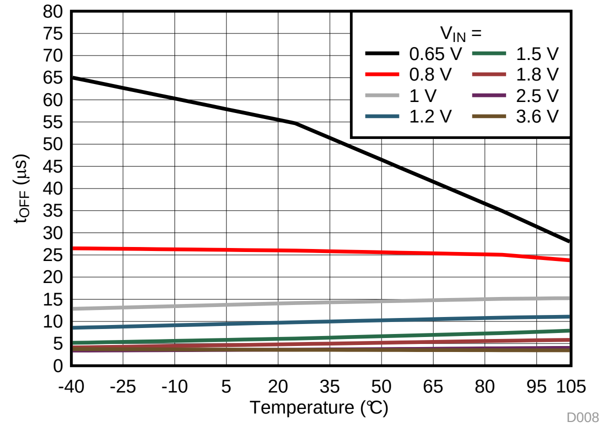
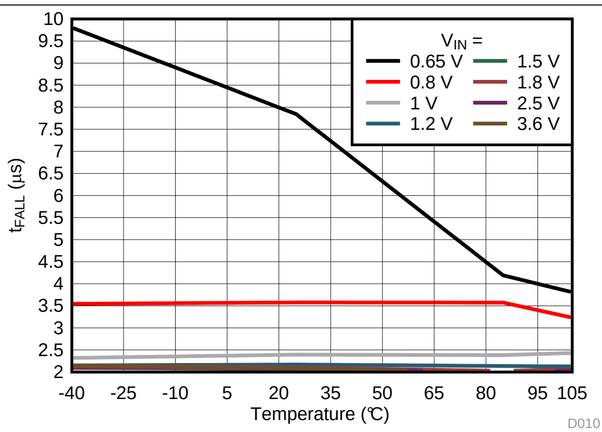
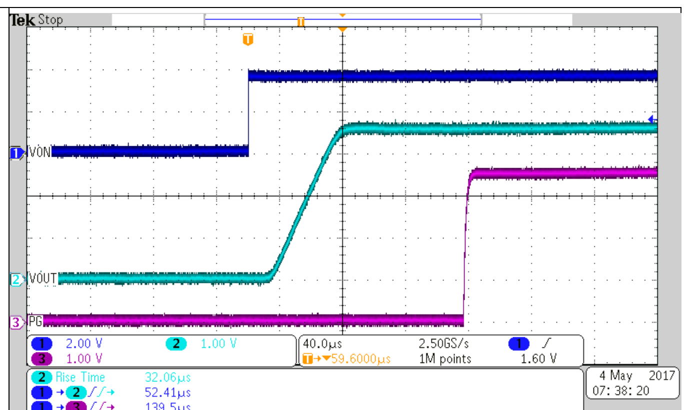


図 10. Turn-Off Time vs Temperature



R_L = 10 Ω C_L = 0.1 µF

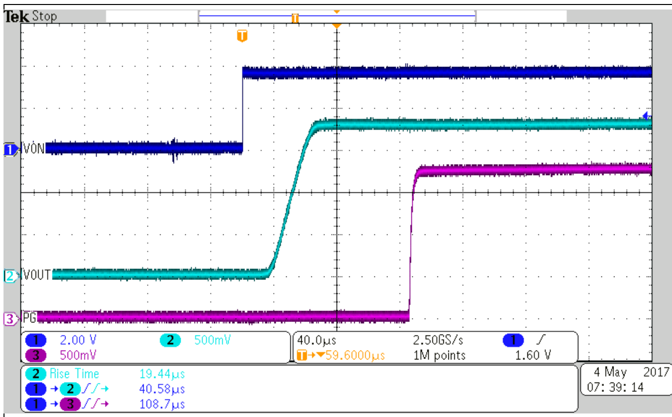
図 11. Fall Time vs Temperature



R_L = 10 Ω C_T = 0 pF
T_A = 25°C C_L = 0.1 µF

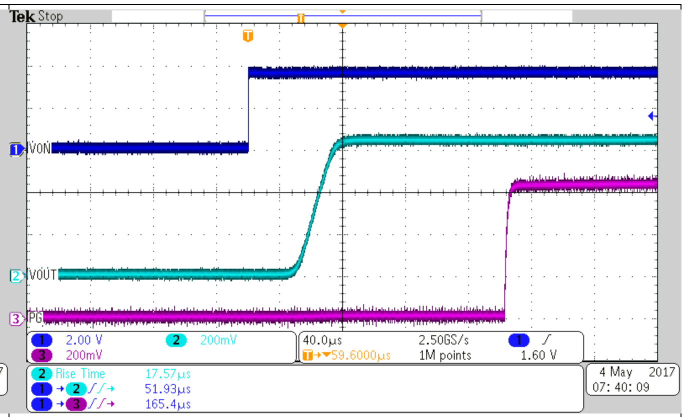
図 12. Turn-On Response at 3.6 V_{IN}

Typical AC Characteristics (continued)



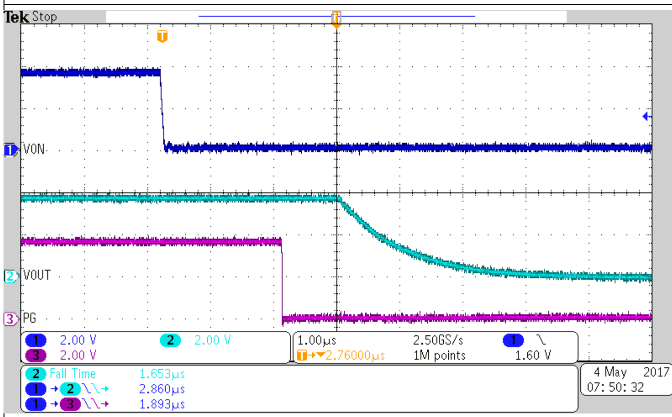
R_L = 10 Ω
T_A = 25°C
C_T = 0 pF
C_L = 0.1 µF

図 13. Turn-On Response at 1.8 V_{IN}



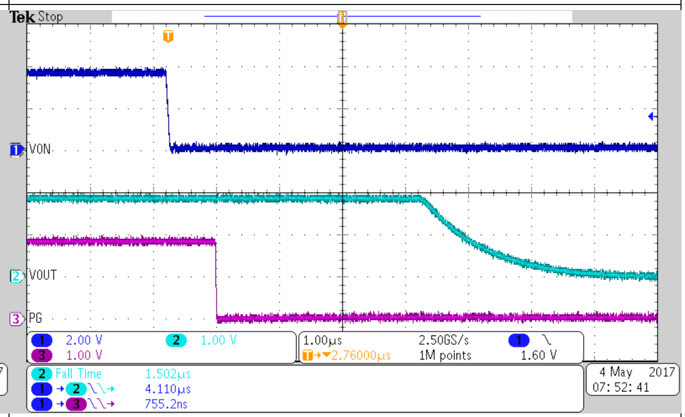
R_L = 10 Ω
T_A = 25°C
C_T = 0 pF
C_L = 0.1 µF

図 14. Turn-On Response at 0.65 V_{IN}



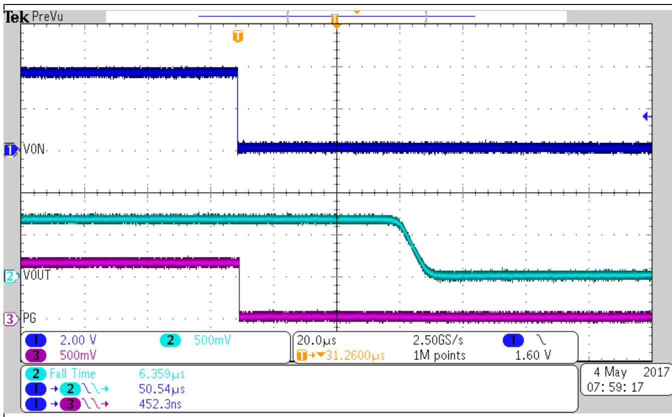
R_L = 10 Ω
T_A = 25°C
C_T = 0 pF
C_L = 0.1 µF

図 15. Turn-Off Response at 3.6 V_{IN}



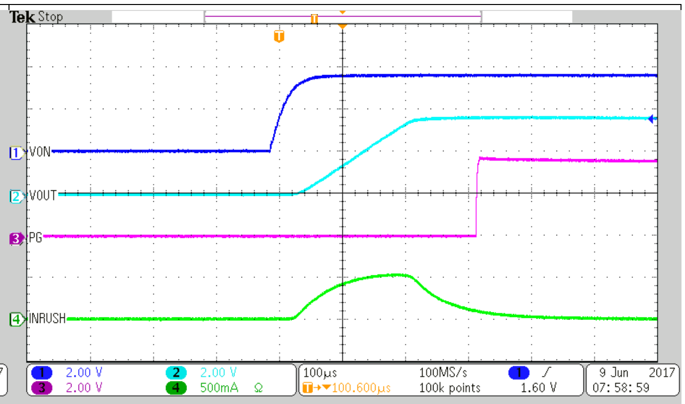
R_L = 10 Ω
T_A = 25°C
C_T = 0 pF
C_L = 0.1 µF

図 16. Turn-Off Response at 1.8 V_{IN}



R_L = 10 Ω
T_A = 25°C
C_{IN} = 0 pF
C_L = 0.1 µF

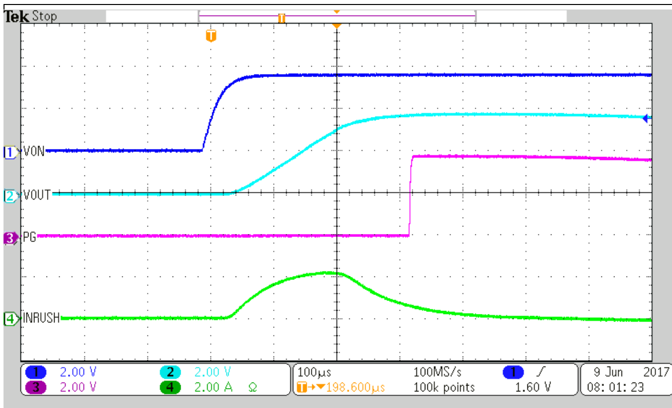
図 17. Turn-Off Response at 0.65 V_{IN}



C_T = 1000 pF
R_L = OPEN
C_L = 33 µF
T_A = 25°C

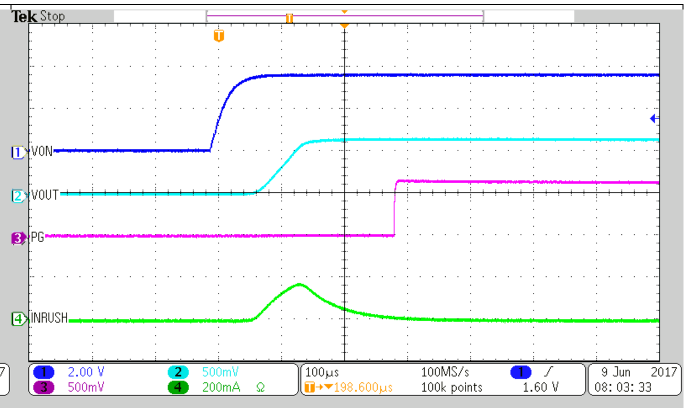
図 18. Low Inrush Current at 3.6 V_{IN}

Typical AC Characteristics (continued)



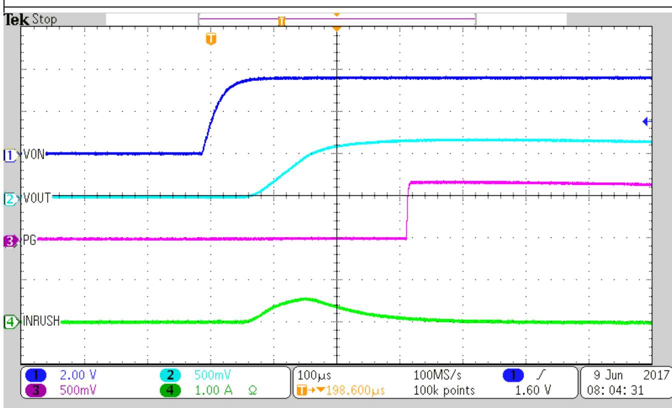
C_T = 1000 pF
R_L = OPEN
C_L = 133 µF
T_A = 25°C

図 19. High Inrush Current at 3.6 V_{IN}



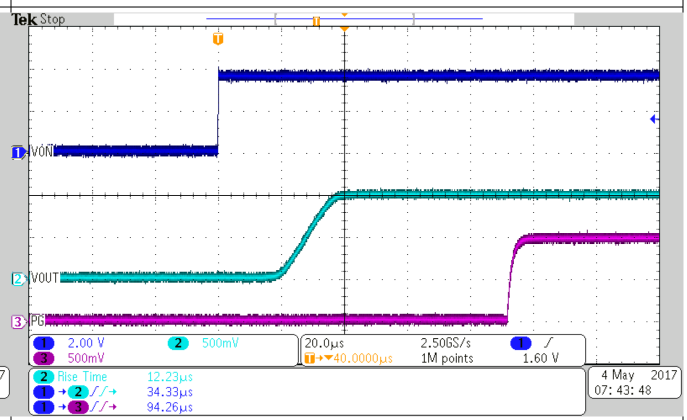
C_T = 1000 pF
R_L = OPEN
C_L = 33 µF
T_A = 25°C

図 20. Low Inrush Current at 0.65 V_{IN}



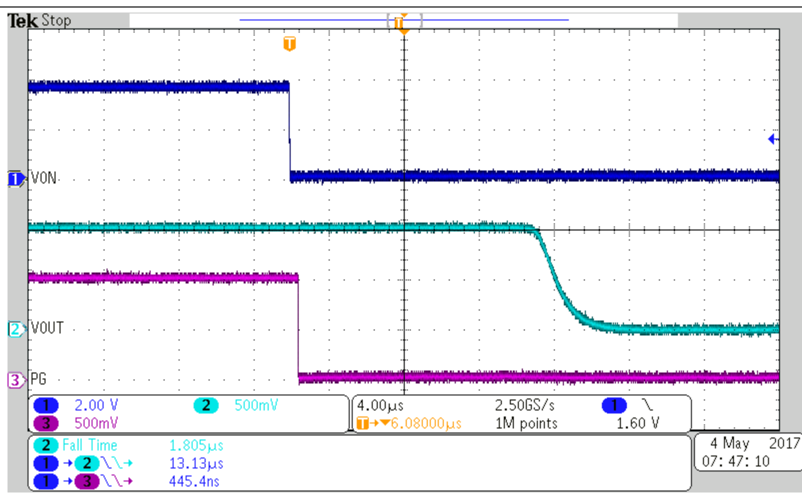
C_T = 1000 pF
R_L = OPEN
C_L = 133 µF
T_A = 25°C

図 21. High Inrush Current at 0.65 V_{IN}



C_T = 0 pF
R_L = 10 Ω
C_L = 0.1 µF
T_A = 25°C

図 22. Fast Turn-On Response



C_{IN} = 0 pF
R_L = 10 Ω
C_L = 0.1 µF
T_A = 25°C

図 23. Fast Turn-Off Response

7 Parameter Measurement Information

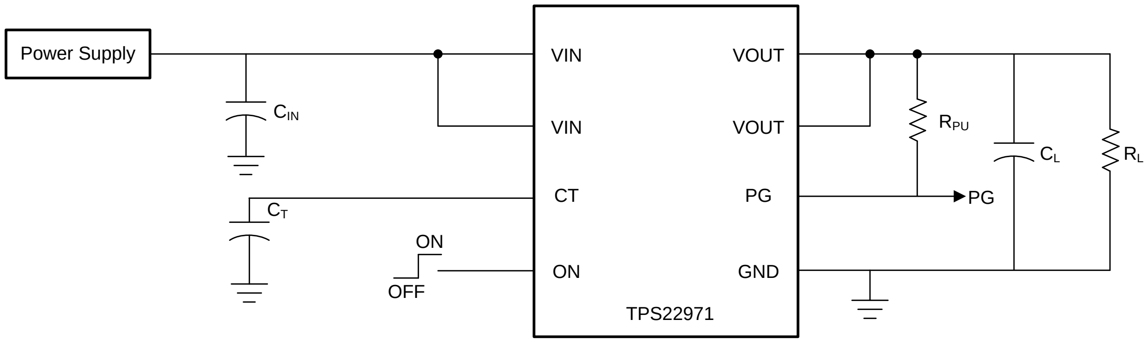


図 24. TPS22971 Test Circuit

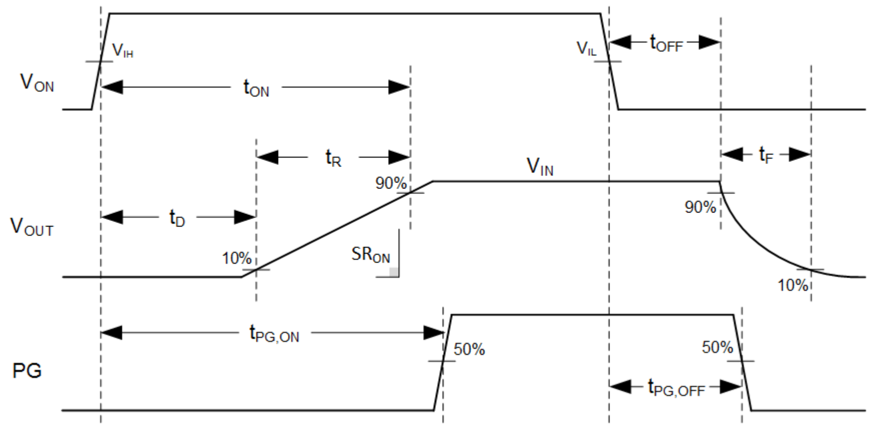


図 25. AC Timing Waveforms

8 Detailed Description

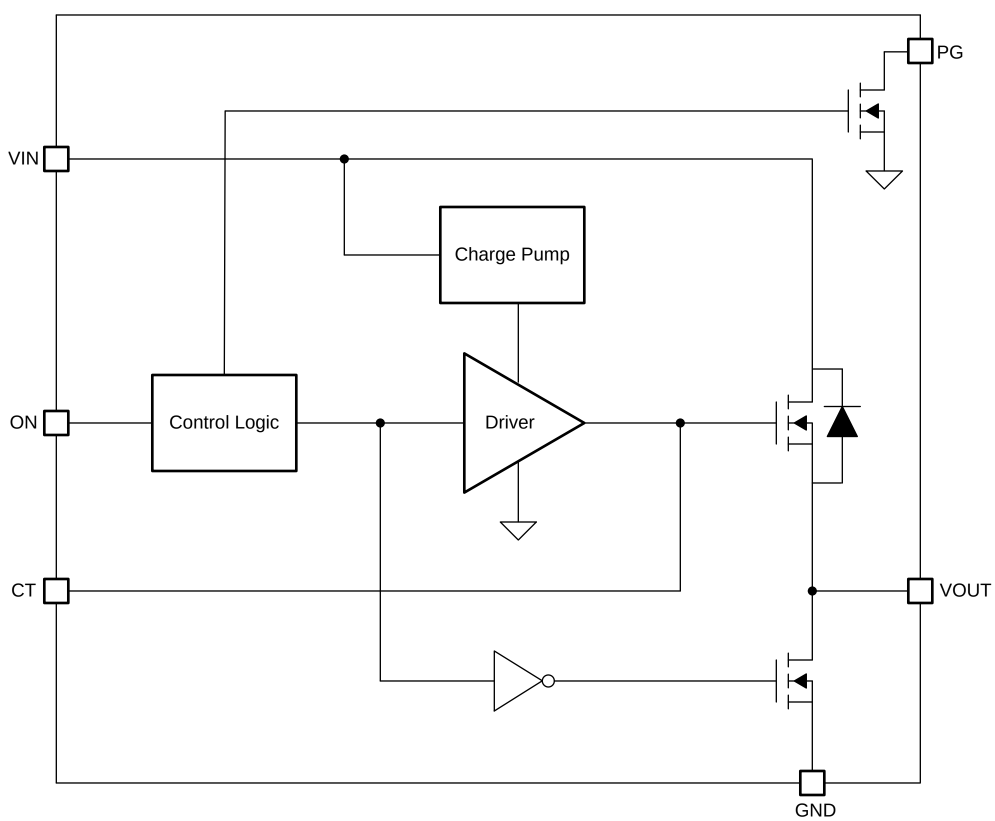
8.1 Overview

The TPS22971 is a single channel, 3-A load switch in a small, space-saving WCSP-8 package. This device implements a low resistance N-channel MOSFET with a controlled rise time for applications that need to limit the inrush current.

The controlled rise time for the device greatly reduces inrush current caused by large bulk load capacitances, thereby reducing or eliminating power supply droop. The adjustable slew rate through CT provides the design flexibility to trade off the inrush current and power up timing requirements. Integrated PG indicator notifies the system about the status of the load switch to facilitate seamless power sequencing.

This device is also designed to have very low leakage current during off state, which prevents downstream circuits from pulling high standby current from the supply. Integrated control logic, driver, power supply, and output discharge FET eliminates the need for additional external components, which reduces solution size and bill of materials (BOM) count.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 On and Off Control

The ON pin controls the state of the switch. Asserting ON high enables the switch. ON has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic. It can be used with any microcontroller with 1.2-V, 1.8-V, 2.5-V or 3.3-V GPIOs. This pin does not have an internal bias and must not be left floating for proper functionality.

Feature Description (continued)

8.3.2 Controlled Turn-On

The TPS22971 has controlled Turn-On for inrush current control. A capacitor to GND on the CT pin adjusts the slew rate. For a given input voltage and desired slew rate, 式 1 can be used to find the required CT value. For calculated CT values less than 220 pF, use 0 pF instead when solving for t_{ON} and $t_{PG,ON}$.

$$CT\left(VIN, SR\right) = \frac{\left(\frac{VIN}{SR} - \left(3.1 \times VIN\right) - 14.2\right) \times 800}{\left(\left(32.5 \times VIN\right) + 12.5\right)}$$

where
- CT is the capacitor on the CT pin (in pF)
- VIN is the input voltage (in V)
- SR is the desired slew rate (in V/µs) (1)

The CT value determined in 式 1 can be used to find the total Turn-On time, t_{ON}, in 式 2 or 式 3 depending on V_{IN}.

$$tON\left(VIN \geq 0.95\ V, CT\right) = \left(\left(15 + \left(33 \times VIN\right)\right) \times \frac{CT}{1000}\right) + \left(\left(3.9 \times VIN\right) + 35\right)$$ (2)

$$tON\left(VIN < 0.95\ V, CT\right) = \left(\left(45 + \left(33 \times VIN\right)\right) \times \frac{CT}{1000}\right) + \left(\left(3.9 \times VIN\right) + 55\right)$$

where
- tON is the Turn-On time (in µs)
- CT is the capacitor on the CT pin (in pF)
- VIN is the input voltage (in V) (3)

8.3.3 Power Good (PG)

The TPS22971 has a power good (PG) output signal to indicate the gate of the pass FET is driven high and the switch is fully on (full load ready). The signal is an active high and open drain output which can be connected to a voltage source through an external pull up resistor, R_{PU}. This voltage source can be V_{OUT} from the TPS22971 or another external voltage. 式 4 and 式 5 show the approximate equation for the relationship between CT setting, V_{IN} and PG Turn-On time ($t_{PG,ON}$):

$$tPG, ON\left(VIN \geq 0.95\ V, CT\right) = \left(\left(40 + \left(36 \times VIN\right)\right) \times \frac{CT}{1000}\right) + \left(\left(10.7 \times VIN\right) + 85\right)$$ (4)

$$tPG, ON\left(VIN < 0.95\ V, CT\right) = \left(\left(80 + \left(36 \times VIN\right)\right) \times \frac{CT}{1000}\right) + \left(\left(10.7 \times VIN\right) + 155\right)$$

where
- $t_{PG,ON}$ is the PG Turn-On time (in µs)
- V_{IN} is the input voltage (in V)
- C_T is the capacitance value on the CT pin (in pF) (5)

8.3.4 Quick Output Discharge (QOD)

The TPS22971 includes a QOD feature. When the switch is disabled, a discharge resistor is connected between VOUT and GND. This resistor has a typical value of 150 Ω and prevents the output from floating while the switch is disabled. The QOD pull-down resistance can vary with input voltage and temperature, see 図 4.

8.4 Device Functional Modes

表 1 lists the functional modes for the TPS22971.

表 1. Function Table

TPS22971			
ON-Pin	**V_{IN} to V_{OUT}**	**V_{OUT} to GND**	**PG to GND**
Below V_{IL}	OFF	ON	ON
Above V_{IH}	ON	OFF	OFF

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Thermal Consideration

It is recommended to limit the junction temperature (T_J) to below 125°C. To calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use 式 6 as a guideline:

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{\theta_{JA}} \tag{6}$$

where

- $P_{D(max)}$ is maximum allowable power dissipation
- $T_{J(max)}$ is maximum allowable junction temperature
- T_A is ambient temperature of the device
- Θ_{JA} is junction to air thermal impedance. See the *Thermal Information* section. This parameter is highly dependent upon board layout (6)

9.1.2 PG Pull Up Resistor

The PG output is an open drain signal which connects to a voltage source through a pull up resistor R_{PU}. The PG signal can be used to drive the enable pins of downstream devices, EN. PG is active high, and its voltage is given by 式 7.

$$V_{PG} = V_{OUT} - (I_{PG,LK} + I_{EN,LK}) \times R_{PU} \tag{7}$$

where

- V_{OUT} is the voltage where PG is tied to
- $I_{PG,LK}$ is the leakage current into PG pin
- $I_{EN,LK}$ is the leakage current into the EN pin driven by PG
- R_{PU} is the pull up resistance (7)

V_{PG} needs to be higher than $V_{IH,MIN}$ of the EN pin to be treated as logic high. The maximum R_{PU} is determined by 式 8.

$$R_{PU,MAX} = \frac{V_{OUT} - V_{IH,MIN}}{I_{PG,LK} + I_{EN,LK}} \tag{8}$$

When PG is disabled, with 1 mA current into PG pin (IPG = 1 mA), $V_{PG.OL}$ is less than 0.2 V and treated as logic low as long as $V_{IL,MAX}$ of the EN pin is greater than 0.2 V. The minimum R_{PU} is determined by 式 9.

$$R_{PU,MIN} = \frac{V_{OUT}}{I_{PG} + I_{EN,LK}} \tag{9}$$

R_{PU} can be chosen within the range defined by $R_{PU,MIN}$ and $R_{PU,MAX}$. R_{PU} = 10 kΩ is used for characterization.

9.1.3 Power Sequencing

The TPS22971 has an integrated power good indicator which can be used for power sequencing. As shown in 図 26, the switch to the second load is controlled by the PG signal from the first switch. This ensures that the power to load 2 is only enabled after the same power to load 1 is enabled after the first switch has turned on.

Application Information (continued)

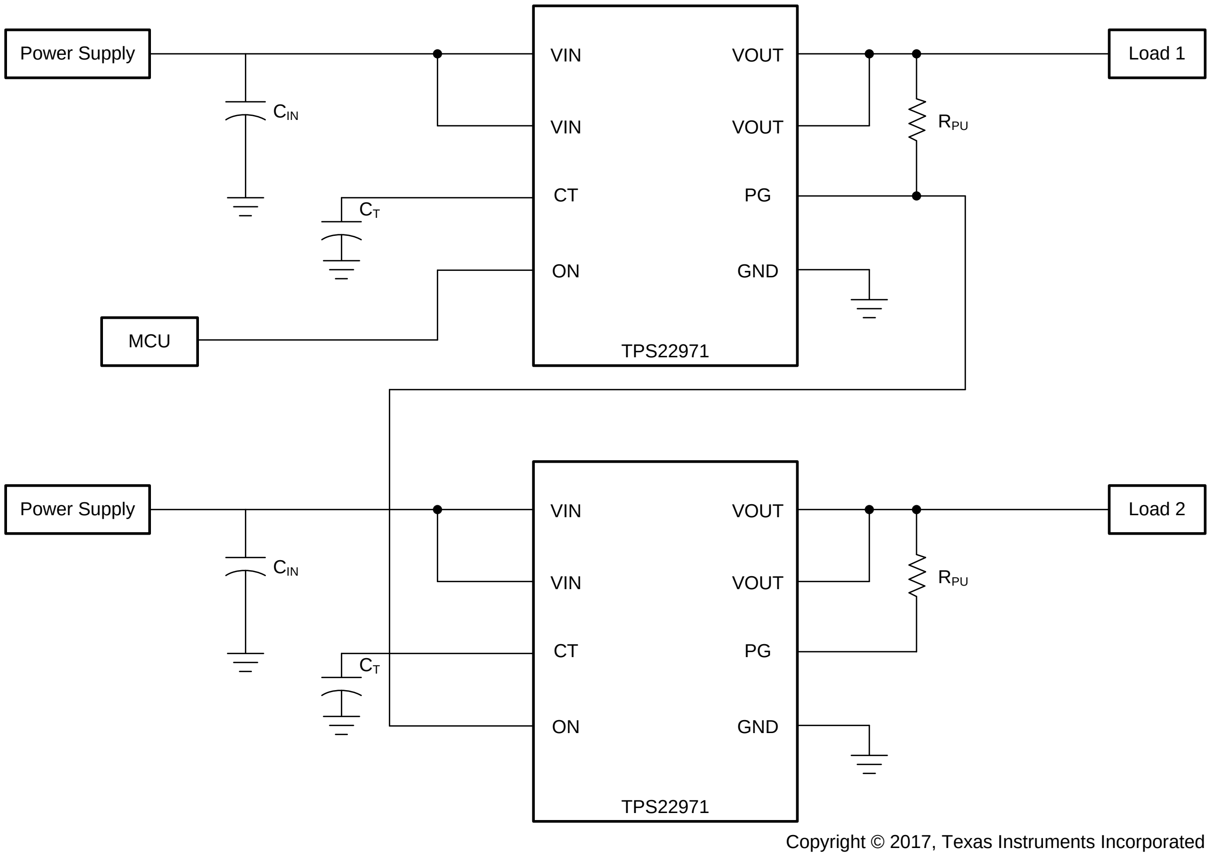


図 26. Power Sequencing

9.2 Typical Application

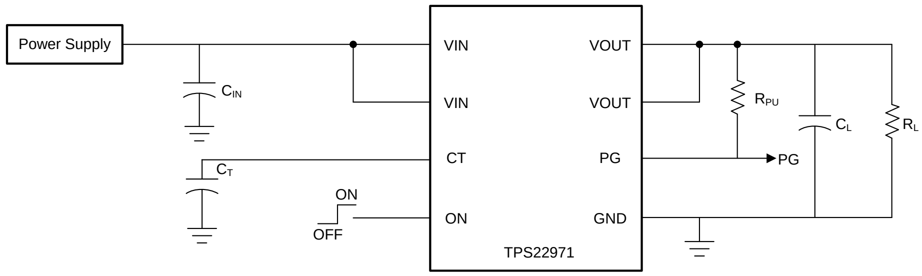


図 27. Typical Application Circuit

9.2.1 Design Requirements

For this design example, below, use the input parameters shown in 表 2.

表 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	3.6 V
I_{LOAD}	10 mA
Load Capacitance (C_L)	33 µF
Maximum Voltage Drop	1%
Maximum Inrush Current	630 mA

9.2.2 Detailed Design Procedure

9.2.2.1 Maximum Voltage Drop and On-Resistance

At 3.6-V input voltage, with a maximum voltage drop tolerance of 1%, the TPS22971 has a typical R_{ON} of 6.7 mΩ. The rail is supplying 10 mA of current; the voltage drop for a rail is calculated based on 式 10.

$$V_{DROP} = R_{ON} \times I_{LOAD} \tag{10}$$

$$V_{DROP} = 0.067\ \text{mV} \tag{11}$$

The maximum voltage drop is 1% which is 36 mV. The voltage drop caused by the load current across the on resistance is 0.067 mV.

9.2.2.2 Managing Inrush Current

When the switch is enabled, the output capacitors must be charged up from 0 V to V_{IN}. This charge arrives in the form of inrush current. Given a load capacitance (C_L) of 33 µF, an input voltage (V_{IN}) of 3.6V and a maximum inrush (I_{INRUSH}) of 630 mA, use 式 12 and 式 13 to solve for Slew Rate (SR).

$$SR = \frac{I_{INRUSH}}{C_L} \tag{12}$$

$$SR = 0.0191\ \text{V}/\mu\text{s} \tag{13}$$

Now that the desired slew rate has been calculated, use SR and V_{IN} in in 式 14 to calculate a CT capacitance value.

$$CT\left(VIN, SR\right) = 1007\ \text{pF} \tag{14}$$

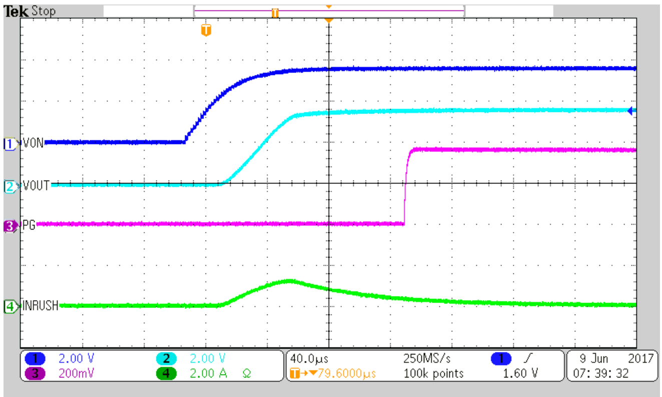
A capacitance value of 1007pF is a non-standard value therefore a 1000 pF CT capacitance is used moving forward.

The calculated CT value can be used with 式 2 and 式 4 to determine t_{ON} and $t_{PG,ON}$, respectively as shown in 式 15 and 式 16.

$$t_{ON}\left(VIN, CT\right) = 182.8\ \mu s \quad (15)$$

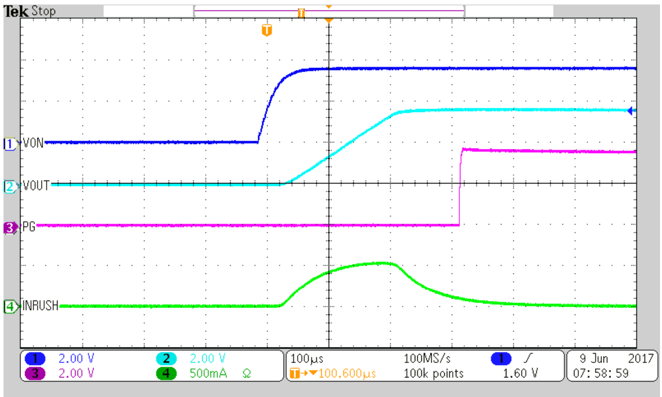
$$t_{PG, ON}\left(VIN, CT\right) = 293.1\ \mu s \quad (16)$$

9.2.3 Application Curves



V_{IN} = 3.6 V V_{ON} = 3.6 V C_{IN} = 1 µF
R_L = OPEN T_A = 25°C C_L = 33 µF

図 28. TPS22971 Inrush Current With C_T = 0 pF



V_{IN} = 3.6 V V_{ON} = 3.6 V C_{IN} = 1 µF
R_L = OPEN T_A = 25°C C_L = 33 µF

図 29. TPS22971 Inrush Current With C_T = 1000 pF

10 Power Supply Recommendations

The device is designed to operate from a VIN range of 0.65 V to 3.6 V. The V_{IN} power supply must be well regulated and placed as close to the device terminal as possible. The power supply must be able to withstand all transient load current steps. In most situations, using an input capacitance of 1 µF is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance may be required on the input.

The requirements for larger input capacitance can be mitigated by adding additional capacitance to the CT pin. This causes the load switch to turn on more slowly. Not only does this reduce transient inrush current, but it also gives the power supply more time to respond to the load current step.

11 Layout

11.1 Layout Guidelines

All traces must be as short as possible for best performance. Using wide traces for V_{IN}, V_{OUT}, and GND helps minimize the parasitic electrical effects along with minimizing the thermal impedance. The CT trace must be as short as possible to reduce parasitic capacitance.

11.2 Layout Example

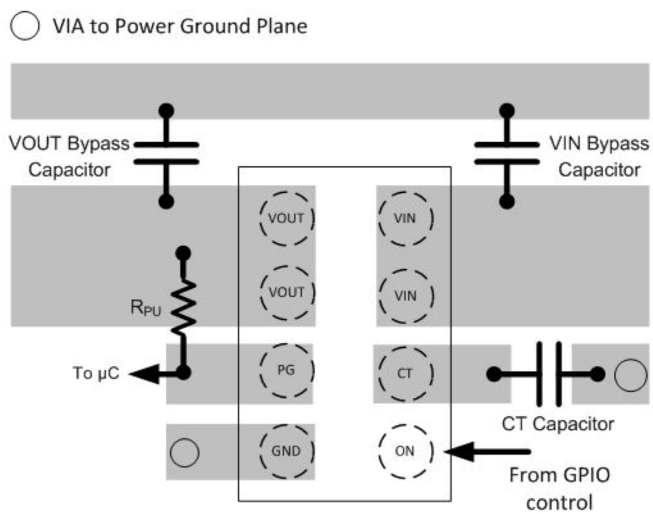


図 30. Package Layout Examples

12 デバイスおよびドキュメントのサポート

12.1 ドキュメントのサポート

12.1.1 関連資料

関連資料については、以下を参照してください。

『TPS22971 負荷スイッチ評価モジュール・ユーザー・ガイド』

12.2 ドキュメントの更新通知を受け取る方法

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12.3 コミュニティ・リソース

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12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS22971YZPR	Active	Production	DSBGA (YZP) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	1CKI
TPS22971YZPR.A	Active	Production	DSBGA (YZP) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 105	1CKI
TPS22971YZPT	Active	Production	DSBGA (YZP) | 8	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	1CKI
TPS22971YZPT.A	Active	Production	DSBGA (YZP) | 8	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 105	1CKI

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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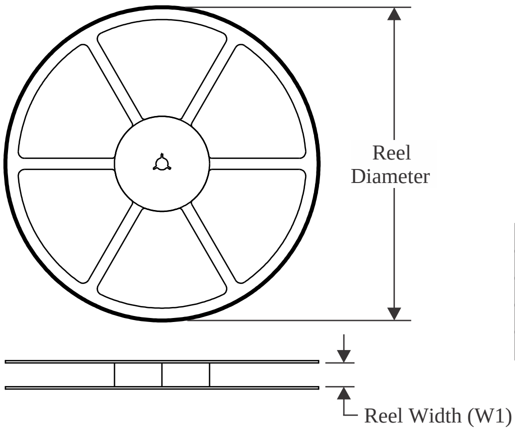
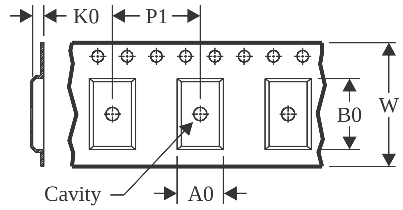
TAPE AND REEL INFORMATION

REEL DIMENSIONS

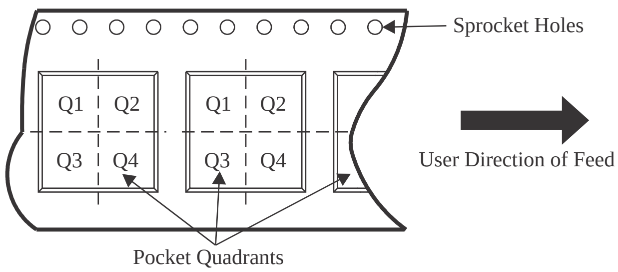


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

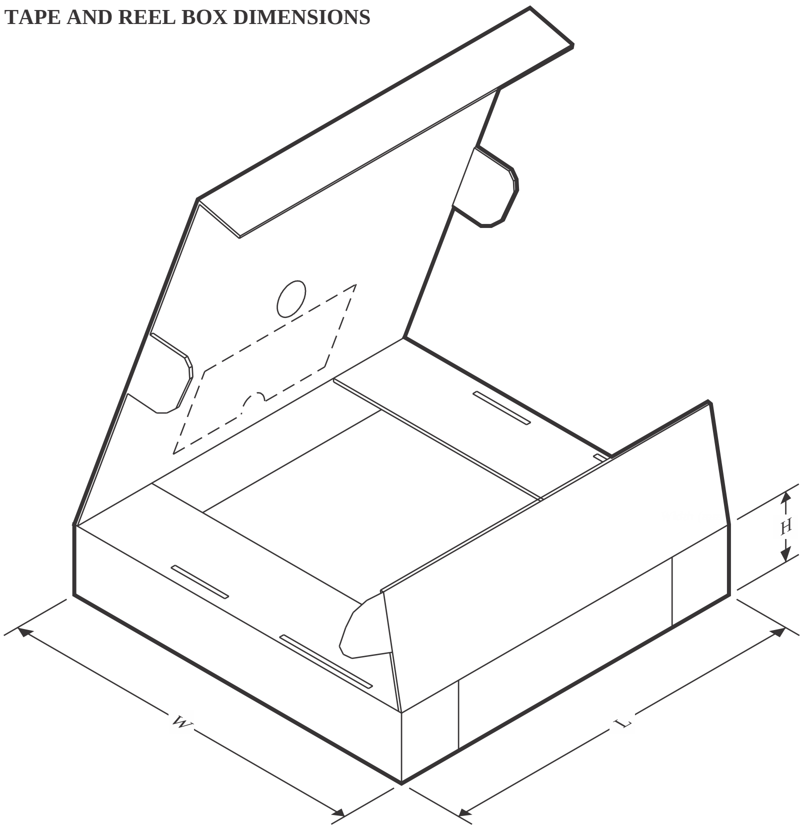
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

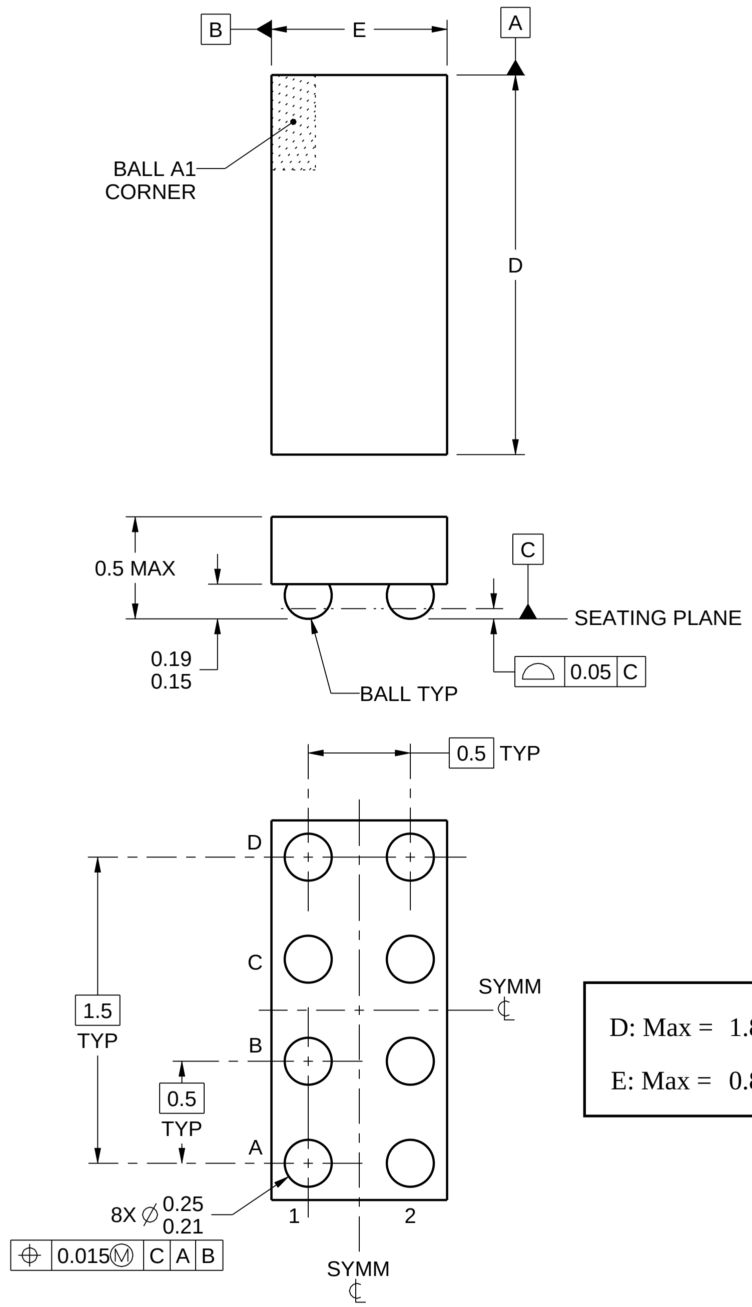
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22971YZPR	DSBGA	YZP	8	3000	180.0	8.4	1.02	2.02	0.63	2.0	8.0	Q1
TPS22971YZPR	DSBGA	YZP	8	3000	180.0	8.4	1.0	2.06	0.63	2.0	8.0	Q1
TPS22971YZPT	DSBGA	YZP	8	250	180.0	8.4	1.0	2.06	0.63	2.0	8.0	Q1
TPS22971YZPT	DSBGA	YZP	8	250	180.0	8.4	1.02	2.02	0.63	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22971YZPR	DSBGA	YZP	8	3000	182.0	182.0	20.0
TPS22971YZPR	DSBGA	YZP	8	3000	182.0	182.0	20.0
TPS22971YZPT	DSBGA	YZP	8	250	182.0	182.0	20.0
TPS22971YZPT	DSBGA	YZP	8	250	182.0	182.0	20.0



D: Max = 1.89 mm, Min = 1.83 mm	
E: Max = 0.89 mm, Min = 0.83 mm	

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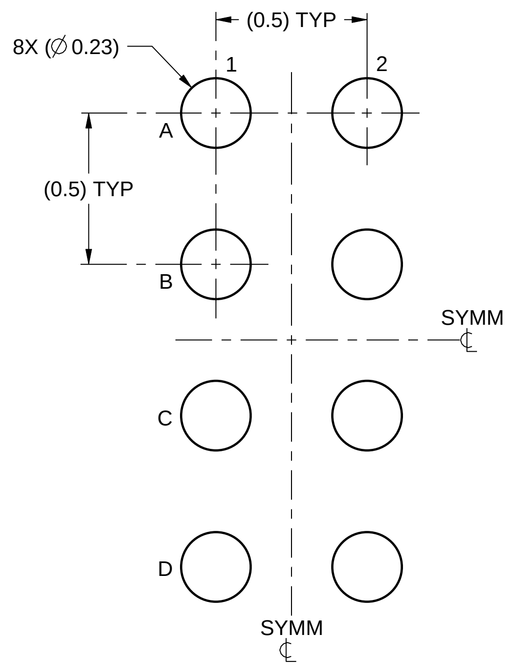
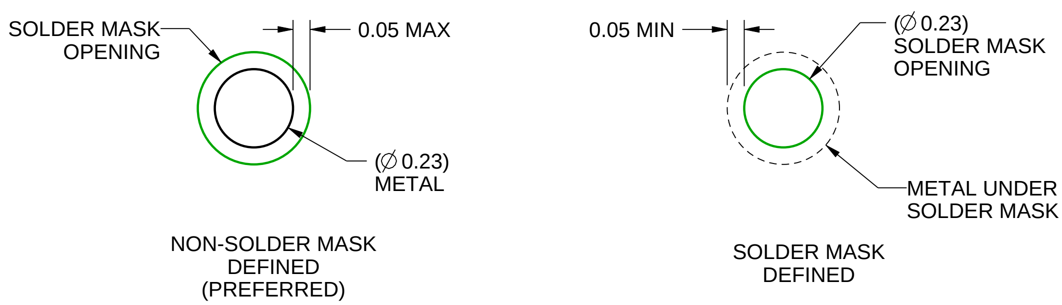
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

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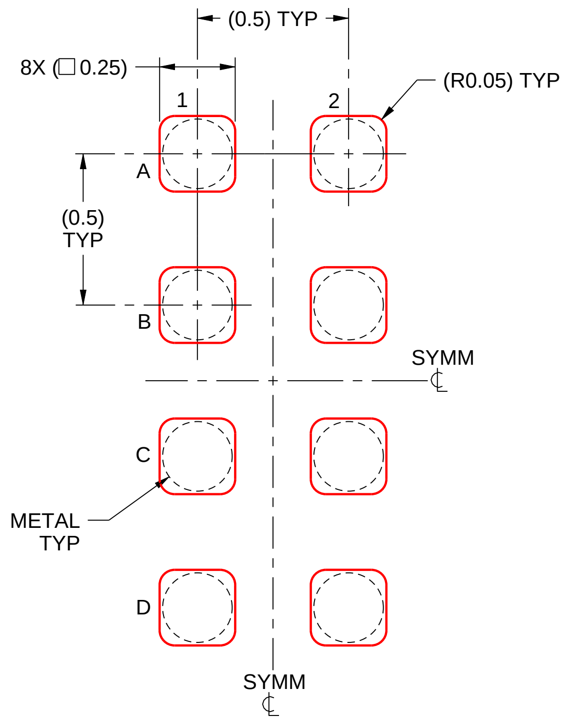
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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