TEXAS INSTRUMENTS
TPS25946
JAJSLP7B – MAY 2021 – REVISED APRIL 2022

TPS25946xx 双方向電流サポート付き 2.7V～23V、5.5A、28mΩ eFuse

1 特長

- 広い動作時入力電圧範囲:2.7V～23V
  - 絶対最大定格:28V
- 低いオン抵抗を持つバック・ツー・バック FET を内蔵: R_{ON} = 28.3mΩ (標準値)
  - オン状態での双方向電流フロー
  - オフ状態での逆電流ブロック
- 高速過電圧保護
  - 調整可能な過電圧誤動作防止 (OVLO) (1.2µs (標準値) の応答時間)
- 負荷電流監視出力 (ILM) による順方向の過電流保護
  - アクティブな電流制限応答
  - 調整可能なスレッショルド (I_{LIM}):0.5A～6A
    - 精度:±10% (I_{LIM} > 1A)
  - 可変の過渡ブランキング・タイマ (ITIMER)、最大 2 × I_{LIM} のピーク電流を許容
  - 出力負荷電流監視精度:±6% (I_{OUT} ≥ 1A)
- OUT ピンの短絡保護の高速トリップ応答
  - 応答時間 500ns (標準値)
  - 可変 (2 × I_{LIM}) および固定のスレッショルド
- アクティブ HIGH のイネーブル入力、低電圧誤動作防止 (UVLO) スレッショルドを設定可能
- 可変の出力スルー・レート (dVdt) 制御
- 過熱保護
- デジタル表示オプション:
  - 可変スレッショルド (PGTH) 付きのパワー・グッド表示 (PG) または
  - サプライ・グッド (SPLYGD) およびフォルト ($\overline{FLT}$) の表示
- UL 2367 認定
  - ファイル番号 E339631
  - R_{ILIM} ≥ 549Ω
- IEC 62368-1 CB 認証
- 小型サイズ:QFN 2mm × 2mm (0.45mm ピッチ)

2 アプリケーション

- USB On-The-Go (OTG)
- スマートフォン
- タブレット
- デジタル・カメラ
- POS 端末
- ワイヤレス・チャージャ

3 概要

TPS25946xx ファミリの eFuse は、小さなパッケージに搭載され、高度に統合された回路保護および電源管理ソリューションです。このデバイスは、非常に少ない数の外付け部品で複数の保護モードを提供し、過負荷、短絡、電圧サージ、および過剰な突入電流に対して堅牢な保護を行います。このデバイスにはバック・ツー・バック FET が内蔵されており、オン状態での双方向電流フローを実現しながら、オフ状態での双方向電流フローをブロックできるため、USB OTG (On-the-Go) アプリケーションに適しています。

出力のスルー・レートと突入電流は、単一の外付けコンデンサを使用して調整できます。入力が過電圧スレッショルド (調整可能) を上回った場合は、出力を遮断することにより負荷を入力過電圧状態から保護します。このデバイスは、電流をアクティブに制限することで、出力過負荷に対応します。出力電流制限スレッショルドおよび過渡過電流ブランキング・タイマは、ユーザーが調整可能です。電流制限制御ピンは、アナログ負荷電流モニタとしても機能します。

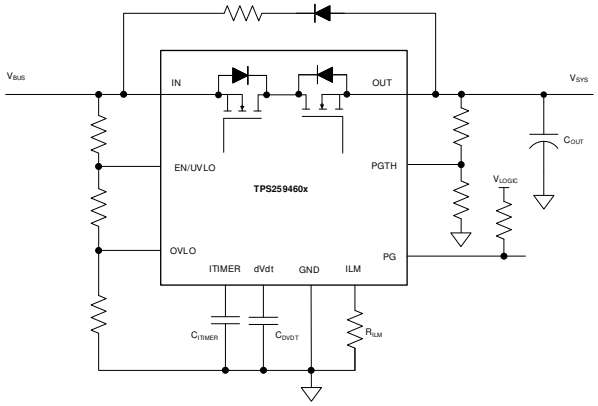
これらのデバイスは、2mm × 2mm、10 ピンの HotRod QFN パッケージで供給され、放熱性能の向上とシステムのフットプリントの削減に役立ちます。

これらのデバイスは、-40°C～+125°C の接合部温度範囲で動作が規定されています。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
TPS25946xxRPW	QFN (10)	2mm × 2mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (August 2021) to Revision B (April 2022)	Page
• UIL/IEC 認証ステータスを更新	1
• Corrected the ESD Ratings to show CDM testing was per JS-002	5
• Updated 表 8-3	25

Changes from Revision * (May 2021) to Revision A (August 2021)	Page
• ドキュメントに TPS259461 デバイスのバリエーションを追加	1
• Updated 式 9 and 式 12	32

5 Device Comparison Table

Part Number	Overvoltage Response	Overcurrent Response	PG Output	Adjustable PG Threshold	SPLYGD Output	$\overline{\text{FLT}}$ Output	Response To Fault
TPS259460ARPW	Adjustable OVLO	Active Current Limit	Y	Y	N	N	Auto-Retry
TPS259460LRPW							Latch-Off
TPS259461ARPW			N	N	Y	Y	Auto-Retry
TPS259461LRPW							Latch-Off

6 Pin Configuration and Functions

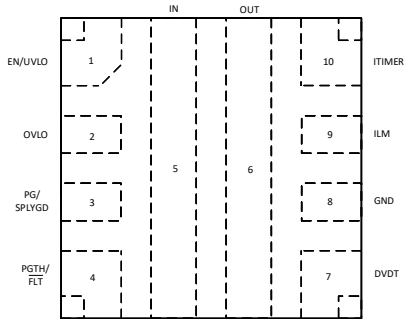


図 6-1. TPS25946xx RPW Package 10-Pin QFN Top View

表 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
EN/UVLO	1	Analog Input	Active High Enable for the device. A resistor divider on this pin from input supply to GND can be used to adjust the Undervoltage Lockout threshold. *Do not leave floating.* Refer to セクション 8.3.1 for details.
OVLO	2	Analog Input	A Resistor Divider on this pin from supply to GND can be used to adjust the Overvoltage Lockout threshold. This pin can also be used as an Active Low Enable for the device. *Do not leave floating.* Refer to セクション 8.3.2 for details.
PG	3	Digital Output	*TPS259460x:* Power Good indication. This pin is an Open Drain signal which is asserted High when the internal power path is fully turned ON and PGTH input exceeds a certain threshold. Refer to セクション 8.3.8 for more details.
SPLYGD			*TPS259461x:* Input Supply Good indication. This pin is an Open Drain signal which is asserted High when the input supply is valid and device has completed inrush sequence. Refer to セクション 8.3.9 for more details.
PGTH	4	Analog Input	*TPS259460x:* Power Good Threshold. Refer to セクション 8.3.8 for more details.
$\overline{\text{FLT}}$		Digital Output	*TPS259461x:* Active low Fault event indicator. This pin is an Open Drain signal which will be pulled low when a fault is detected. Refer to セクション 8.3.7 for more details.
IN	5	Power	Power input/output
OUT	6	Power	Power input/output
DVDT	7	Analog Output	A capacitor from this pin to GND sets the output turn on slew rate. Leave this pin floating for the fastest turn on slew rate. Refer to セクション 8.3.3.1 for details.
GND	8	Ground	This pin is the ground reference for all internal circuits and must be connected to system GND.
ILM	9	Analog Output	This pin is a dual function pin used to limit and monitor the output current. An external resistor from this pin to GND sets the output current limit threshold during start-up as well as steady state. The pin voltage can also be used as analog output load current monitor signal. *Do not leave floating.* Refer to セクション 8.3.3.2 for more details.
ITIMER	10	Analog Output	A capacitor from this pin to GND sets the overcurrent blanking interval during which the output current can temporarily exceed set current limit (but lower than fast-trip threshold) before the device overcurrent response takes action. Leave this pin open for fastest response to overcurrent events. Refer to セクション 8.3.3.2 for more details.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

Parameter		Pin	MIN	MAX	UNIT
V_{IN}	Maximum Input Voltage Range, –40°C ≤ T_J ≤ 125°C	IN	–0.3	28	V
V_{OUT}	Maximum Output Voltage Range, –40°C ≤ T_J ≤ 125°C	OUT	–0.3	min (28, V_{IN} + 21)	
	Maximum Output Voltage Range, –10°C ≤ T_J ≤ 125°C		–0.3	min (28, V_{IN} + 22)	
$V_{OUT,PLS}$	Minimum Output Voltage Pulse (< 1 µs)	OUT	–0.8		
$V_{EN/UVLO}$	Maximum Enable Pin Voltage Range	EN/UVLO	–0.3	6.5	V
V_{OVLO}	Maximum OVLO Pin Voltage Range	OVLO	–0.3	6.5	V
V_{dVdT}	Maximum dVdT Pin Voltage Range	dVdt	Internally Limited		V
V_{ITIMER}	Maximum ITIMER Pin Voltage Range	ITIMER	Internally Limited		V
V_{PG}	Maximum PG Pin Voltage Range (TPS259460x)	PG	–0.3	6.5	V
V_{PGTH}	Maximum PGTH Pin Voltage Range (TPS259460x)	PGTH	–0.3	6.5	V
V_{SPLYGD}	Maximum SPLYGD Pin Voltage Range (TPS259461x)	SPLYGD	–0.3	6.5	V
V_{FLTB}	Maximum $\overline{FLT}$ Pin Voltage Range (TPS259461x)	$\overline{FLT}$	–0.3	6.5	V
V_{ILM}	Maximum ILM Pin Voltage Range	ILM	Internally Limited		V
I_{MAX}	Maximum Continuous Switch Current	IN - OUT	Internally Limited		A
T_J	Junction temperature		Internally Limited		°C
T_{LEAD}	Maximum Lead Temperature			300	°C
T_{STG}	Storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Parameter		Pin	MIN	MAX	UNIT
V_{IN}	Input Voltage Range	IN	2.7	23	V
V_{OUT}	Output Voltage Range	OUT		min (23, V_{IN} + 20)	V
$V_{EN/UVLO}$	Enable Pin Voltage Range	EN/UVLO		5 (1)	V
V_{OVLO}	OVLO Pin Voltage Range	OVLO	0.5	1.5	V
V_{dVdT}	dVdt Capacitor Voltage Rating	dVdt	V_{IN} + 5 V		V
V_{PG}	PG Pin Voltage Range (TPS259460x)	PG		5	V
V_{PGTH}	PGTH Pin Voltage Range (TPS259460x)	PGTH		5	V
V_{SPLYGD}	SPLYGD Pin Voltage Range (TPS259461x)	SPLYGD		5	V
V_{FLTB}	$\overline{FLT}$ Pin Voltage Range (TPS259461x)	$\overline{FLT}$		5	V
V_{ITIMER}	ITIMER Pin Capacitor Voltage Rating	ITIMER	4		V
R_{ILM}	ILM Pin Resistance	ILM	549	6650	Ω
I_{MAX}	Continuous Switch Current, $T_J \leq 125°C$	IN - OUT		5.5	A
T_J	Junction temperature		–40	125	°C

(1) For supply voltages below 5V, it is okay to pull up the EN pin to IN directly. For supply voltages greater than 5V, it is recommended to use a pull-up resistor with a minimum value of 350 kΩ.

7.4 Thermal Information

THERMAL METRIC (1)		TPS25946xx RPW (QFN) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	41.7 (2)	°C/W
		74.5 (3)	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	20 (2)	°C/W
		27.6 (3)	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Based on simulations conducted with the device mounted on a custom 4-layer PCB (2s2p) with 8 thermal vias under device
(3) Based on simulations conducted with the device mounted on a JEDEC 4-layer PCB (2s2p) with no thermal vias under device

7.5 Electrical Characteristics

(Test conditions unless otherwise noted) –40°C ≤ T_J ≤ 125°C, V_{IN} = 12 V, OUT = Open, $V_{EN/UVLO}$ = 2 V, V_{OVLO} = 0 V, R_{ILM} = 549 Ω , dVdT = Open, ITIMER = Open, PGTH/$\overline{FLT}$ = Open, PG/SPLYGD = Open. All voltages referenced to GND.

Test Parameter	Description	MIN	TYP	MAX	UNITS
INPUT SUPPLY (IN)					
$V_{UVP(R)}$	IN Supply UVP Rising threshold	2.44	2.53	2.64	V
$V_{UVP(F)}$	IN Supply UVP Falling threshold	2.35	2.42	2.55	V
$I_{Q(ON)}$	IN Supply Quiescent Current		428	610	µA
$I_{Q(OFF)}$	IN Supply disabled State Current ($V_{SD(F)}$ < V_{EN} < $V_{UVLO(F)}$)		73	130	µA
I_{SD}	IN Supply Shutdown Current (V_{EN} < $V_{SD(F)}$)		4.4	28.7	µA
ON RESISTANCE (IN - OUT)					
R_{ON}	V_{IN} = 12 V, I_{OUT} = 3 A, T_J = 25°C		28.3		mΩ
	2.7 ≤ V_{IN} ≤ 23 V, I_{OUT} = 3 A, –40°C ≤ T_J ≤ 125°C			45	mΩ
ENABLE/UNDERVOLTAGE LOCKOUT (EN/UVLO)					
$V_{UVLO(R)}$	UVLO Rising threshold	1.183	1.20	1.223	V
$V_{UVLO(F)}$	UVLO Falling threshold	1.076	1.09	1.116	V
$V_{SD(F)}$	EN/UVLO Falling Threshold for lowest shutdown current	0.45	0.74		V
I_{ENLKG}	EN/UVLO leakage current	–0.1		0.1	µA
OVERVOLTAGE LOCKOUT (OVLO)					
$V_{OV(R)}$	OVLO Rising threshold	1.183	1.20	1.223	V
$V_{OV(F)}$	OVLO Falling threshold	1.076	1.09	1.116	V
I_{OVLKG}	OVLO pin leakage current, 0.5 V < V_{OVLO} < 1.5 V	–0.1		0.1	µA
OVERCURRENT PROTECTION (OUT)					
I_{LIM}	Overcurrent Threshold, R_{ILM} = 6.65 kΩ	0.425	0.500	0.575	A
	Overcurrent Threshold, R_{ILM} = 3.32 kΩ	0.850	1.007	1.150	A
	Overcurrent Threshold, R_{ILM} = 1.65 kΩ	1.800	2.028	2.200	A
	Overcurrent Threshold, R_{ILM} = 750 Ω	3.960	4.452	4.840	A
	Overcurrent Threshold, R_{ILM} = 549 Ω	5.400	6.068	6.600	A
I_{FLT}	Circuit Breaker Threshold, ILM Pin Open (Single point failure)		0.1		A
	Circuit Breaker Threshold, ILM Pin Shorted to GND (Single point failure)		1.1	2.1	A
I_{SCGain}	Scalable Fast Trip Threshold (I_{SC}) : I_{LIM} Ratio		201		%
I_{FT}	Fixed Fast-trip current threshold		22.2		A
V_{FB}	V_{OUT} threshold to exit Current Limit Foldback		1.9		V
OVERCURRENT FAULT TIMER (ITIMER)					
V_{INT}	ITIMER pin internal pull-up voltage	2.3	2.57	2.72	V
R_{ITIMER}	ITIMER pin internal pull-up resistance		15		kΩ
I_{ITIMER}	ITIMER pin internal discharge current, I_{OUT} > I_{LIM}	1.2	1.8	2.5	µA
ΔV_{ITIMER}	ITIMER discharge differential voltage threshold	1.286	1.51	1.741	V
OUTPUT LOAD CURRENT MONITOR (ILM)					
G_{IMON}	Analog Load Current Monitor Gain (I_{MON} : I_{OUT}), I_{OUT} = 0.5 A to 1 A, I_{OUT} < I_{LIM}	165	182	200	µA/A
	Analog Load Current Monitor Gain (I_{MON} : I_{OUT}), I_{OUT} = 1 A to 5.5 A, I_{OUT} < I_{LIM}	165	182	200	µA/A

7.5 Electrical Characteristics (continued)

(Test conditions unless otherwise noted) –40°C ≤ T_J ≤ 125°C, V_{IN} = 12 V, OUT = Open, $V_{EN/UVLO}$ = 2 V, V_{OVLO} = 0 V, R_{ILM} = 549 Ω , dVdT = Open, ITIMER = Open, PGTH/$\overline{FLT}$ = Open, PG/SPLYGD = Open. All voltages referenced to GND.

Test Parameter	Description	MIN	TYP	MAX	UNITS
POWER GOOD INDICATION (PG) - TPS259460x OR SUPPLY GOOD INDICATION (SPLYGD) - TPS259461x					
V_{PGD}	PG/SPLYGD pin voltage while de-asserted. V_{IN} < $V_{UVP(F)}$, V_{EN} < $V_{SD(F)}$, Weak pull-up (I_{PG} = 26 µA)		0.67	1	V
	PG/SPLYGD pin voltage while de-asserted, V_{IN} < $V_{UVP(F)}$, V_{EN} < $V_{SD(F)}$, Strong pull-up (I_{PG} = 242 µA)		0.79	1	V
	PG/SPLYGD pin voltage while de-asserted, V_{IN} > $V_{UVP(R)}$		0		V
I_{PGLKG}	PG/SPLYGD Pin leakage current, PG/SPLYGD asserted		0.9	3	µA
POWERGOOD THRESHOLD (PGTH) - TPS259460x					
$V_{PGTH(R)}$	PGTH Rising threshold	1.183	1.20	1.223	V
$V_{PGTH(F)}$	PGTH Falling threshold	1.076	1.09	1.116	V
$I_{PGTHLKG}$	PGTH leakage current	–0.1		0.3	µA
FAULT INDICATION ($\overline{FLT}$) - TPS259461x					
I_{FLTLKG}	$\overline{FLT}$ pin leakage current	–1		1	µA
R_{FLTB}	$\overline{FLT}$ pin pull-down resistance		12.3		Ω
OVERTEMPERATURE PROTECTION (OTP)					
TSD	Thermal Shutdown Rising Threshold, T_J ↑		154		°C
TSD_{HYS}	Thermal Shutdown Hysteresis, T_J ↓		10		°C
DVDT					
I_{dVdt}	dVdt Pin Charging Current	0.81	2.21	3.82	µA

7.6 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OVLO}	Overvoltage lock-out response time	V_{OVLO} > $V_{OV(R)}$ to V_{OUT} ↓		1.2		µs
t_{LIM}	Current limit response time	I_{OUT} > 1.2 × I_{LIM} & ITIMER expired to I_{OUT} settling to within 5 % of I_{LIM}		340		µs
t_{SC}	Scalable fast-trip response time	I_{OUT} > 3 × I_{LIM} to I_{OUT} ↓		500		ns
t_{FT}	Fixed fast-trip response time	I_{OUT} > I_{FT} to I_{OUT} ↓		500		ns
t_{RST}	Auto-Retry Interval after fault (TPS25946xA)			110		ms
t_{PGA}	PG Assertion de-glitch			12		µs
t_{PGD}	PG De-assertion de-glitch			12		µs

7.7 Switching Characteristics

The output rising slew rate is internally controlled and constant across the entire operating voltage range to ensure the turn on timing is not affected by the load conditions. The rising slew rate can be adjusted by adding capacitance from the dVdt pin to ground. As C_{dVdt} is increased it will slow the rising slew rate (SR). See Slew Rate and Inrush Current Control (dVdt) section for more details. The Turn-Off Delay and Fall Time, however, are dependent on the RC time constant of the load capacitance (C_{OUT}) and Load Resistance (R_L). The Switching Characteristics are only valid for the power-up sequence where the supply is available in steady state condition and the load voltage is completely discharged before the device is enabled.Typical Values are taken at T_J = 25°C unless specifically noted otherwise. R_L = 100 Ω, C_{OUT} = 1 µF

PARAMETER		V_{IN}	C_{dVdt} = Open	C_{dVdt} = 1800 pF	C_{dVdt} = 3300 pF	UNIT
SR_{ON}	Output Rising slew rate	2.7 V	12.14	0.87	0.5	V/ms
		12 V	28.1	1.09	0.61	
		23 V	44.78	1.25	0.71	
$t_{D,ON}$	Turn on delay	2.7 V	0.09	0.6	0.97	ms
		12 V	0.1	1.32	2.35	
		23 V	0.11	1.99	3.69	
t_R	Rise time	2.7 V	0.17	2.51	4.33	ms
		12 V	0.35	8.1	15.37	
		23 V	0.40	14.4	25.89	
t_{ON}	Turn on time	2.7 V	0.27	3.11	5.31	ms
		12 V	0.45	10.08	17.72	
		23 V	0.50	16.41	29.57	
$t_{D,OFF}$	Turn off delay	2.7 V	64.44	64.44	64.44	µs
		12 V	25.32	25.32	25.32	
		23 V	23.02	23.02	23.02	

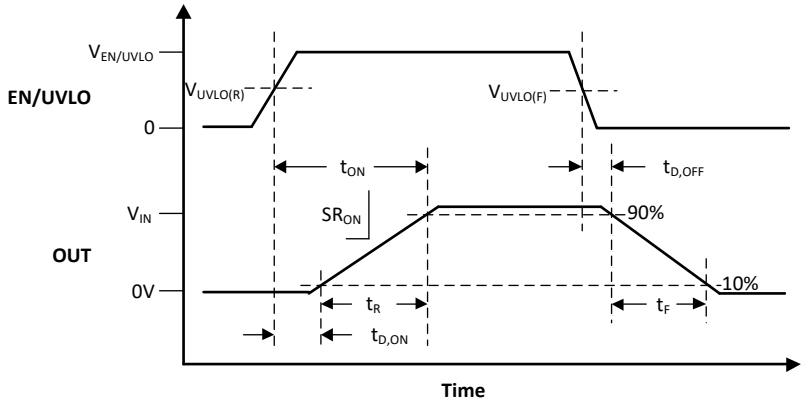


図 7-1. TPS25946xx Switching Times

7.8 Typical Characteristics

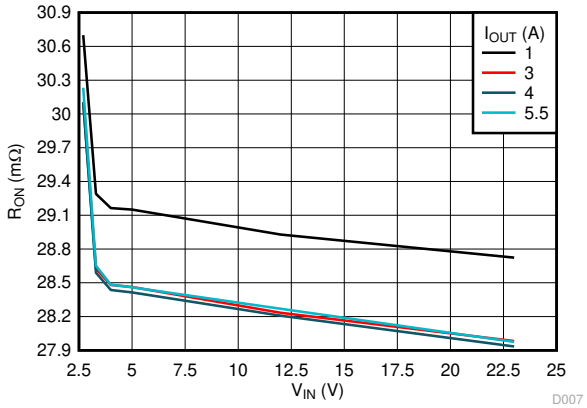


図 7-2. ON-Resistance vs Supply Voltage

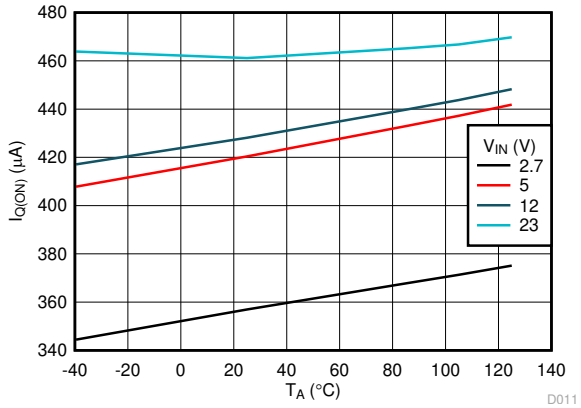


図 7-3. IN Quiescent Current vs Temperature

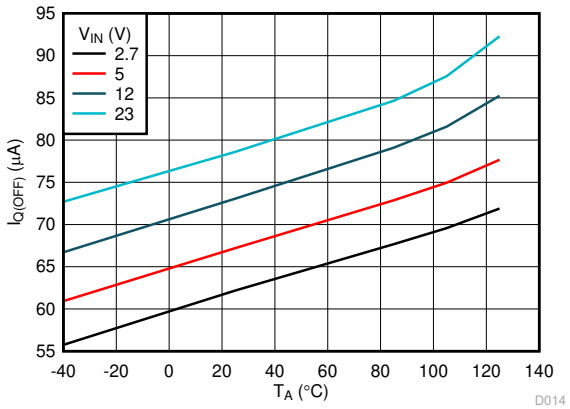


図 7-4. IN OFF State (UVLO) Current vs Temperature

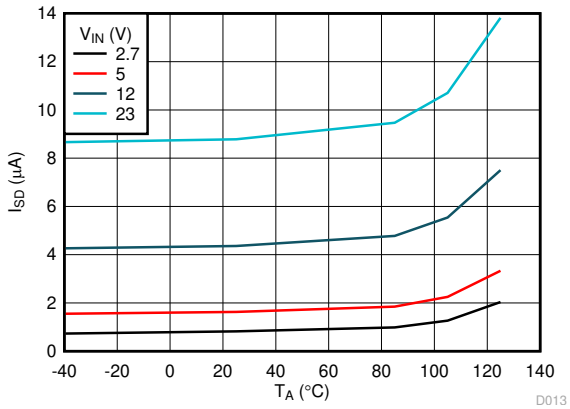


図 7-5. IN Shutdown Current vs Temperature

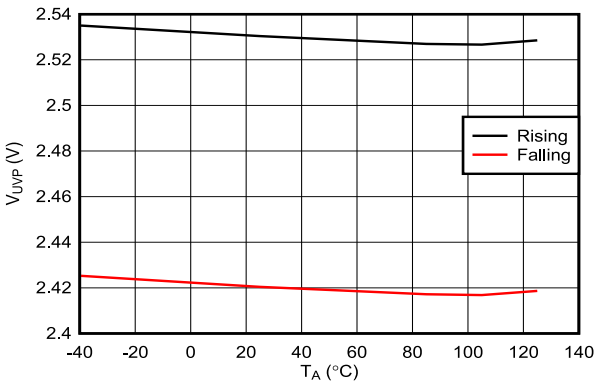


図 7-6. IN Undervoltage Threshold vs Temperature

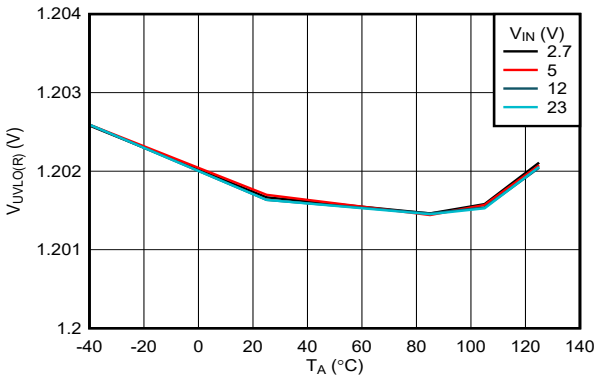


図 7-7. EN/UVLO Rising Threshold vs Temperature

7.8 Typical Characteristics (continued)

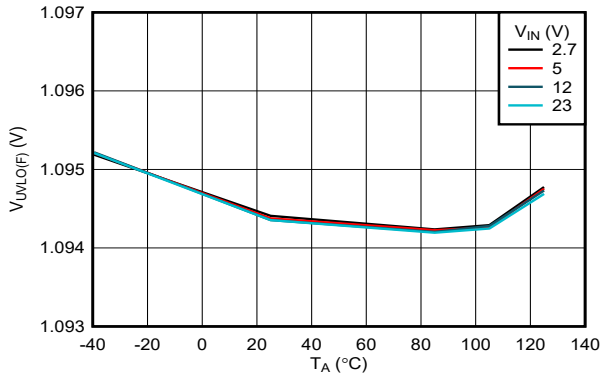


図 7-8. EN/UVLO Falling Threshold vs Temperature

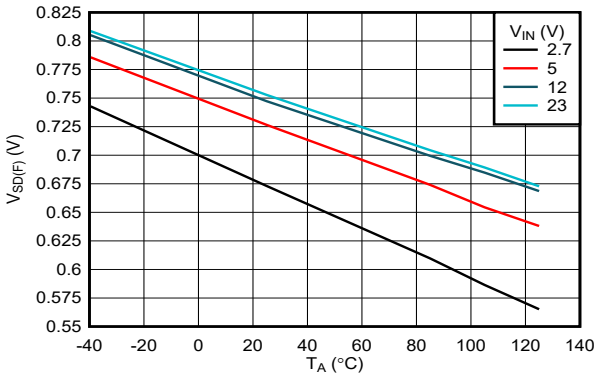


図 7-9. EN/UVLO Shutdown Falling Threshold vs Temperature

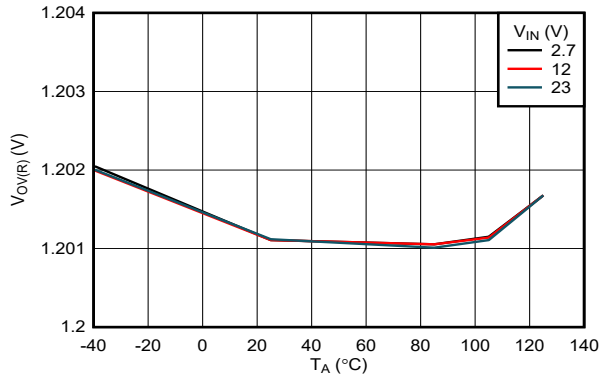


図 7-10. OVLO Rising Threshold vs Temperature

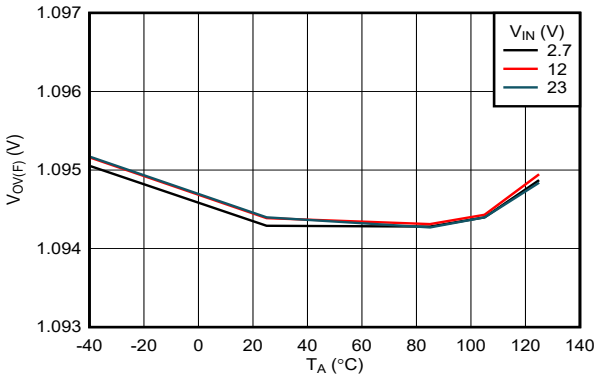


図 7-11. OVLO Falling Threshold vs Temperature

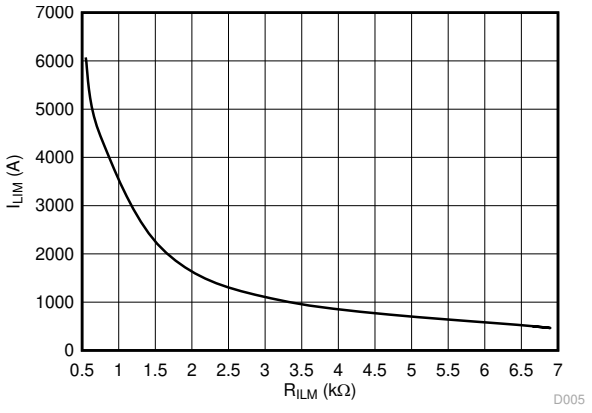


図 7-12. Overcurrent Threshold vs ILM Resistor

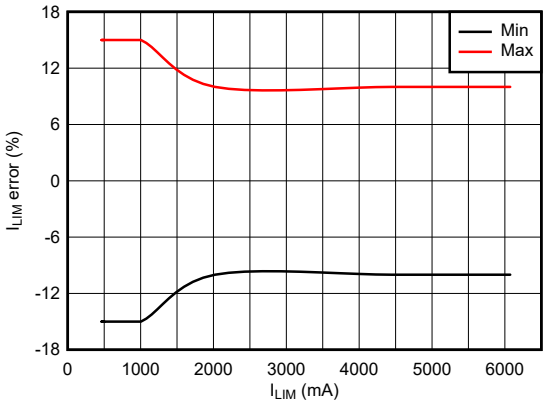


図 7-13. Overcurrent Threshold Accuracy (Across Process, Voltage, and Temperature)

7.8 Typical Characteristics (continued)

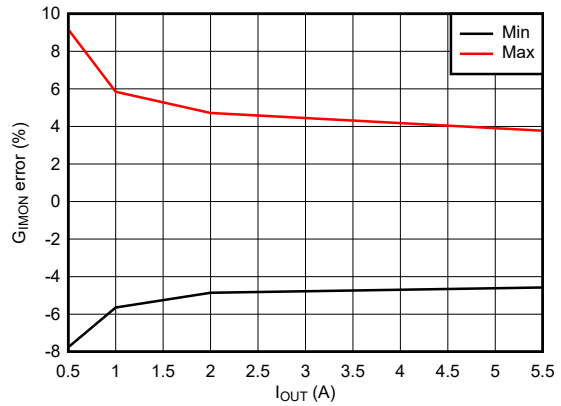


図 7-14. Analog Current Monitor Gain Accuracy

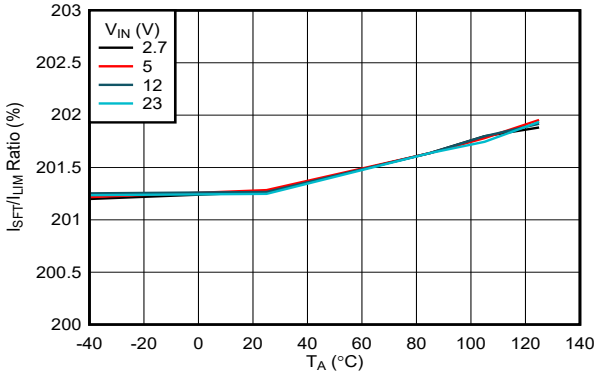


図 7-15. Scalable Fast-Trip Threshold: Current Limit Threshold (I_{LIM}) Ratio vs Temperature

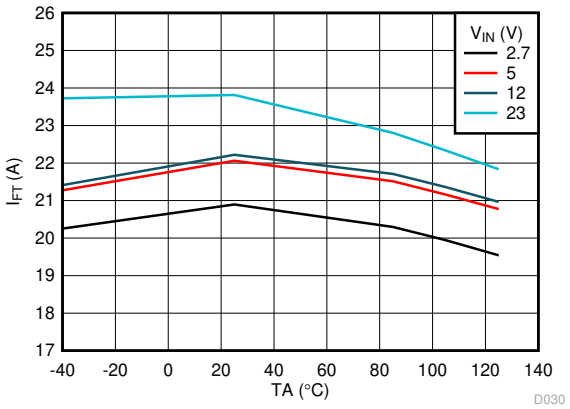


図 7-16. Steady State Fixed Fast-Trip Current Threshold vs Temperature

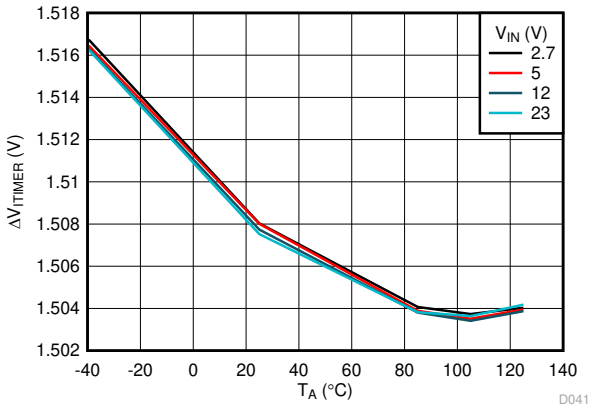


図 7-17. ITIMER Discharge Differential Voltage Threshold vs Temperature

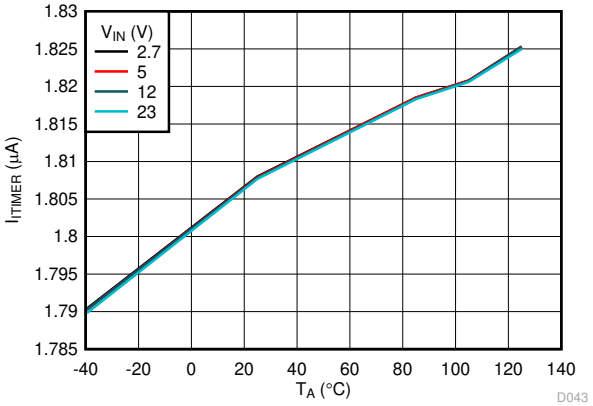


図 7-18. ITIMER Discharge Current vs Temperature

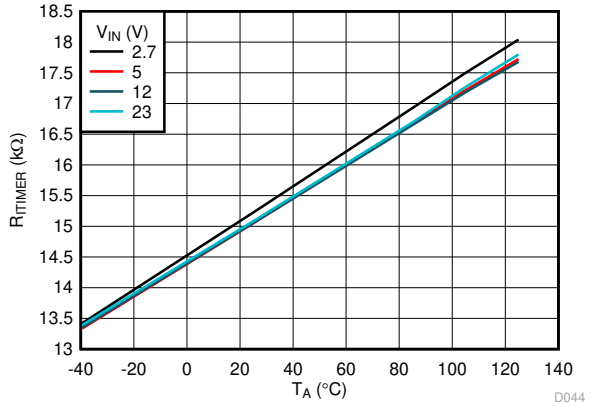


図 7-19. ITIMER Internal Pullup Resistance vs Temperature

7.8 Typical Characteristics (continued)

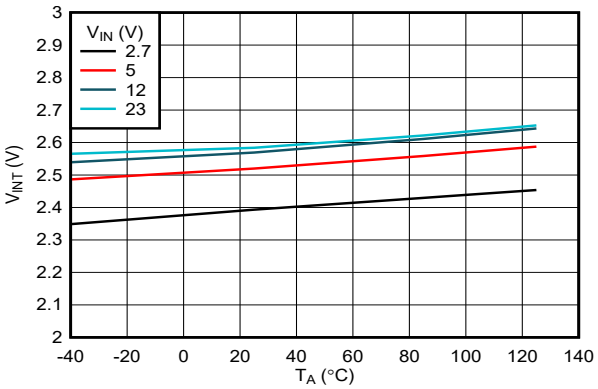


図 7-20. ITIMER Internal Pullup Voltage vs Temperature

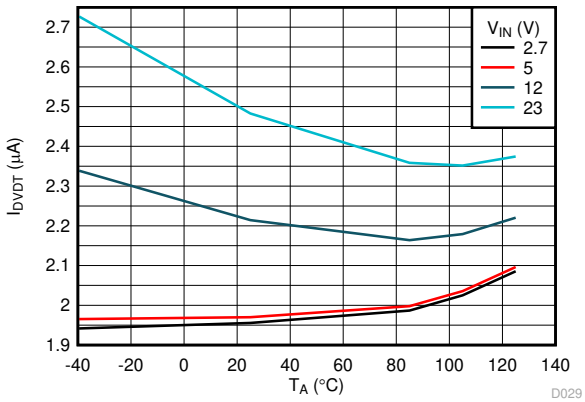


図 7-21. DVDT Charging Current vs Temperature

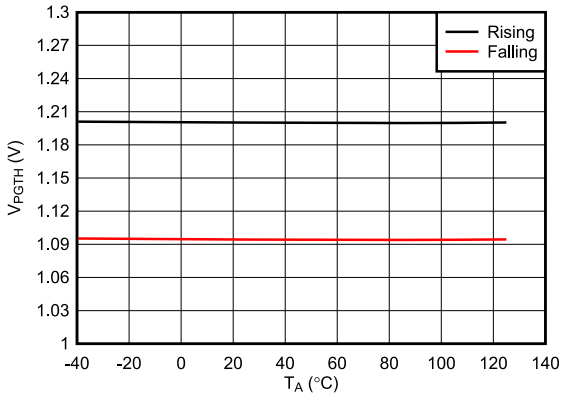


図 7-22. PGTH Threshold vs Temperature

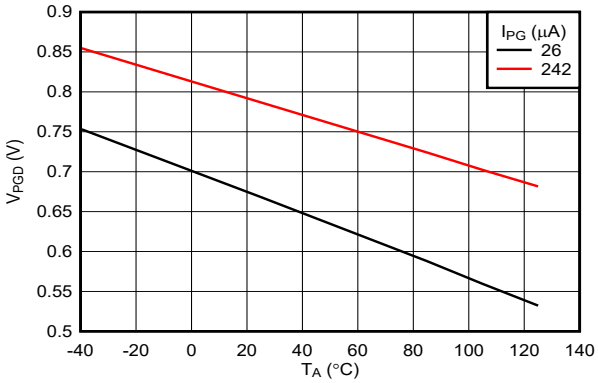


図 7-23. PG Low Voltage Without Input Supply vs Temperature

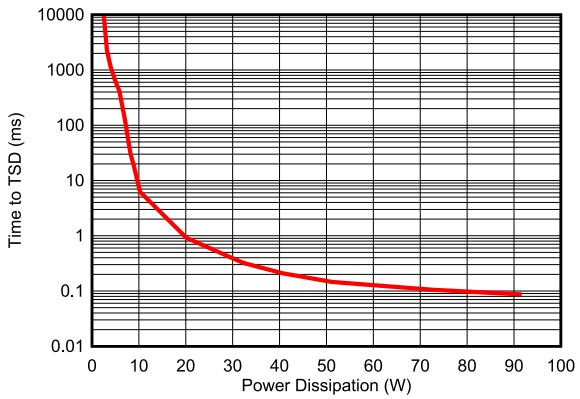


図 7-24. Time to Thermal Shut-Down During Inrush State

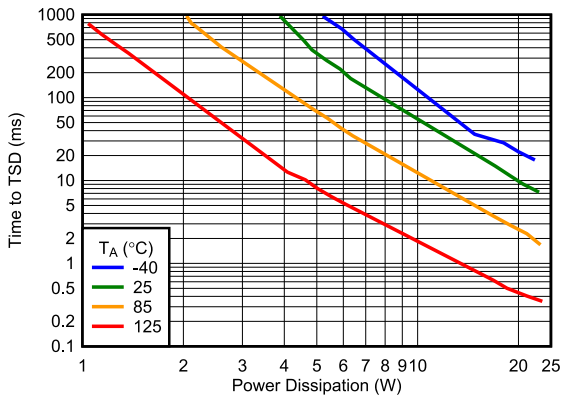
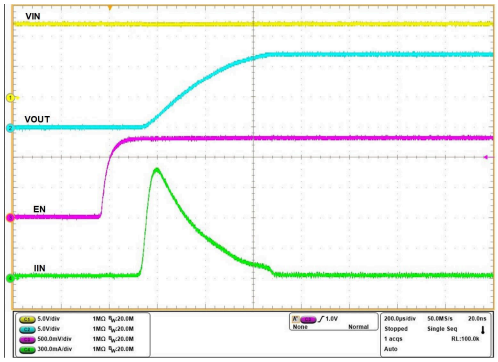


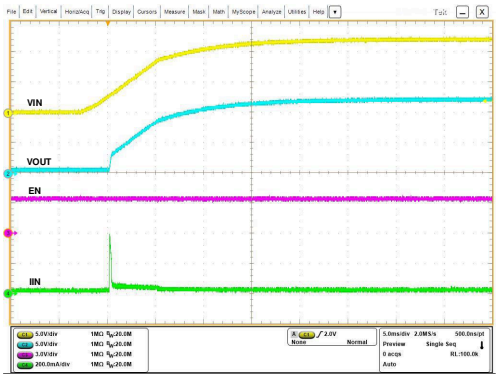
図 7-25. Time to Thermal Shut-Down During Steady State

7.8 Typical Characteristics (continued)



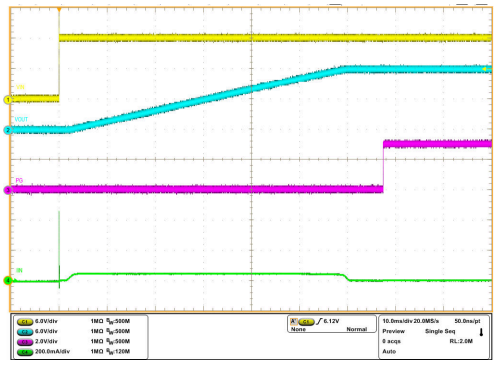
V_{IN} = 12 V, C_{OUT} = 30 µF, C_{dVdt} = Open, $V_{EN/UVLO}$ stepped up to 1.4 V

図 7-26. Start-Up with Enable



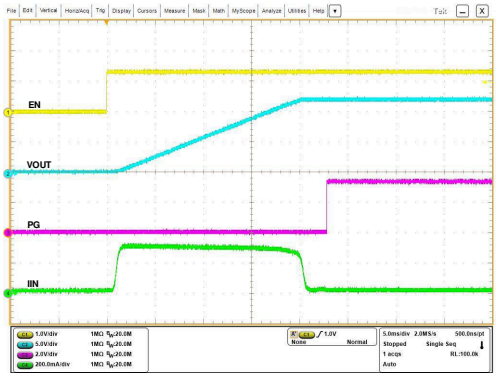
$V_{EN/UVLO}$ = 3.3 V, C_{OUT} = 30 µF, C_{dVdt} = Open, V_{IN} ramped up to 12 V

図 7-27. Start-Up with IN Supply



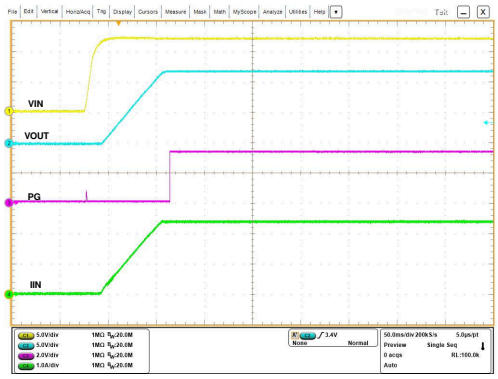
C_{OUT} = 220 µF, C_{dVdt} = 10 nF, EN/UVLO connected to IN through resistor ladder, 12 V hot-plugged to IN

図 7-28. IN Hot-Plug



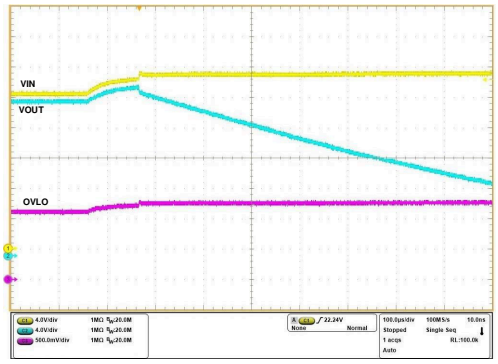
V_{IN} = 12 V, C_{OUT} = 470 µF, C_{dVdt} = 3300 pF, $V_{EN/UVLO}$ stepped up to 1.4 V

図 7-29. Inrush Current with Capacitive Load



V_{IN} = 12 V, C_{OUT} = 470 µF, R_{OUT} = 5 Ω, C_{dVdt} = 3300 pF, $V_{EN/UVLO}$ stepped up to 1.4 V

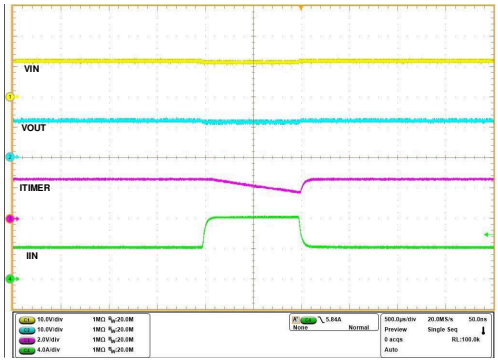
図 7-30. Inrush Current with Resistive and Capacitive Load



C_{OUT} = 220 µF, I_{OUT} = 4 A, V_{IN} Overvoltage threshold set to 22 V, V_{IN} ramped up from 20 V to 23 V

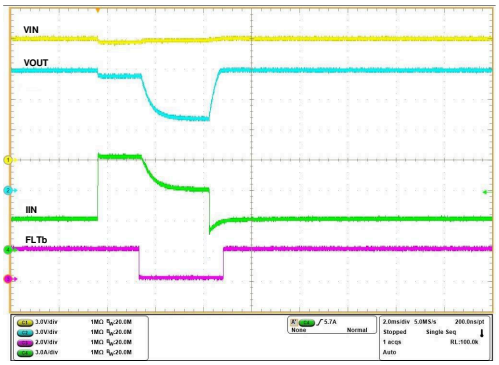
図 7-31. Overvoltage Lockout Response

7.8 Typical Characteristics (continued)



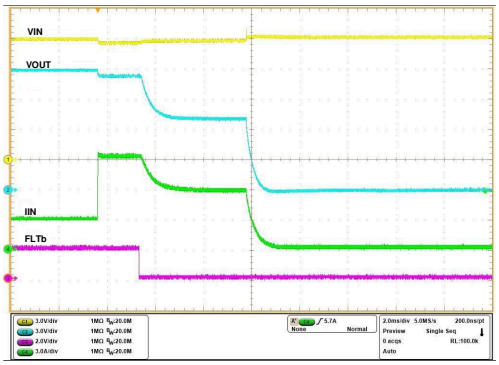
V_{IN} = 12 V, C_{ITIMER} = 2.2 nF, C_{OUT} = 470 µF, R_{ILM} = 549 Ω, I_{OUT} ramped from 4 A → 8 A→ 4 A within 1 ms

図 7-32. Transient Overcurrent Blanking Timer Response



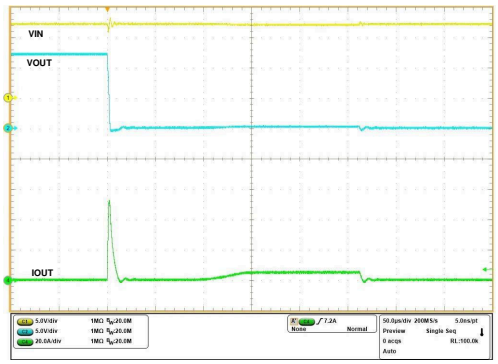
V_{IN} = 12 V, C_{ITIMER} = 2.2 nF, C_{OUT} = 220 µF, R_{ILM} = 549 Ω, I_{OUT} stepped from 3 A → 9 A → 3 A within 5 ms

図 7-33. Active Current Limit Response



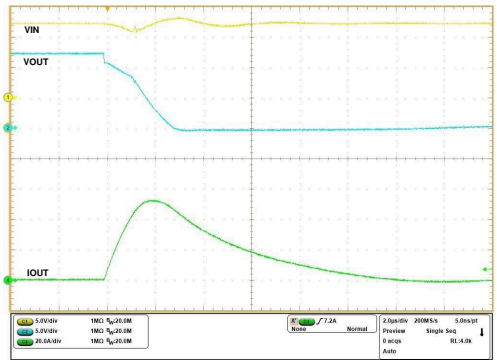
V_{IN} = 12 V, C_{ITIMER} = 2.2 nF, C_{OUT} = 220 µF, R_{ILM} = 549 Ω, I_{OUT} stepped from 3 A → 9 A

図 7-34. Active Current Limit Response Followed by TSD



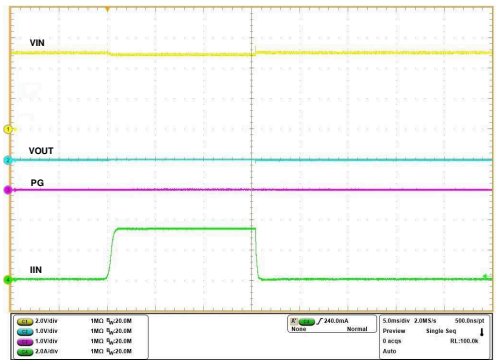
V_{IN} = 12 V, R_{ILM} = 549 Ω, $V_{EN/UVLO}$ = 3.3 V, OUT stepped from Open → Short-circuit to GND

図 7-35. OUT Pin Short-Circuit During Steady State



V_{IN} = 12 V, R_{ILM} = 549 Ω, $V_{EN/UVLO}$ = 3.3 V, OUT stepped from Open → Short-circuit to GND

図 7-36. OUT Pin Short-Circuit During Steady State (Zoomed In)



V_{IN} = 5 V, C_{OUT} = Open, OUT short-circuit to GND, R_{ILM} = 750 Ω, $V_{EN/UVLO}$ stepped from 0 V to 3.3 V

図 7-37. Power Up with OUT Pin Short-Circuit to GND

8 Detailed Description

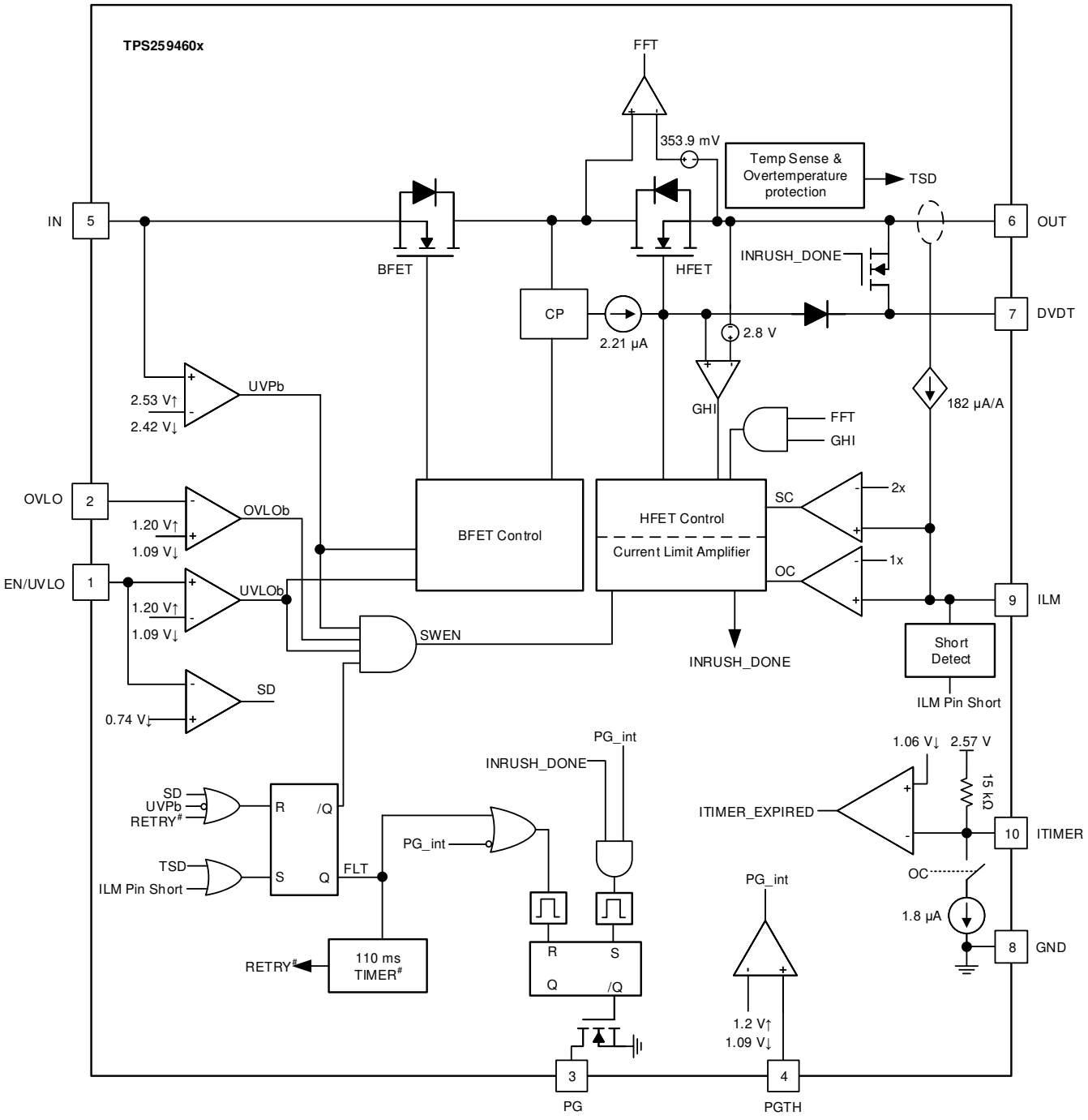
8.1 Overview

The TPS25946xx is an eFuse with integrated power path that is used to ensure safe power delivery in a system. The device starts its operation by monitoring the IN bus. When the input supply voltage (V_{IN}) exceeds the undervoltage protection threshold (V_{UVP}), the device samples the EN/UVLO pin. A high level (> V_{UVLO}) on this pin enables the internal power path (BFET + HFET) to start conducting and allow current to flow in both directions. When the IN supply voltage is insufficient (< V_{UVP}) or the EN/UVLO is held low (< V_{UVLO}), the internal power path is turned off, thereby blocking current flow in both directions.

After a successful start-up sequence, the device now actively monitors its IN voltage and load current from IN to OUT, and controls the internal HFET to ensure that the user adjustable overcurrent limit threshold (I_{LIM}) is not exceeded and overvoltage spikes are cut off after they cross the user adjustable overvoltage lockout threshold (V_{OVLO}). The device also provides fast protection against severe overcurrent during short-circuit events on OUT pin. This feature keeps the system safe from harmful levels of voltage and current. At the same time, a user adjustable overcurrent blanking timer allows the system to pass moderate transient peaks in the load current profile without tripping the eFuse. This ensures a robust protection solution against real faults which is also immune to transients, thereby ensuring maximum system uptime.

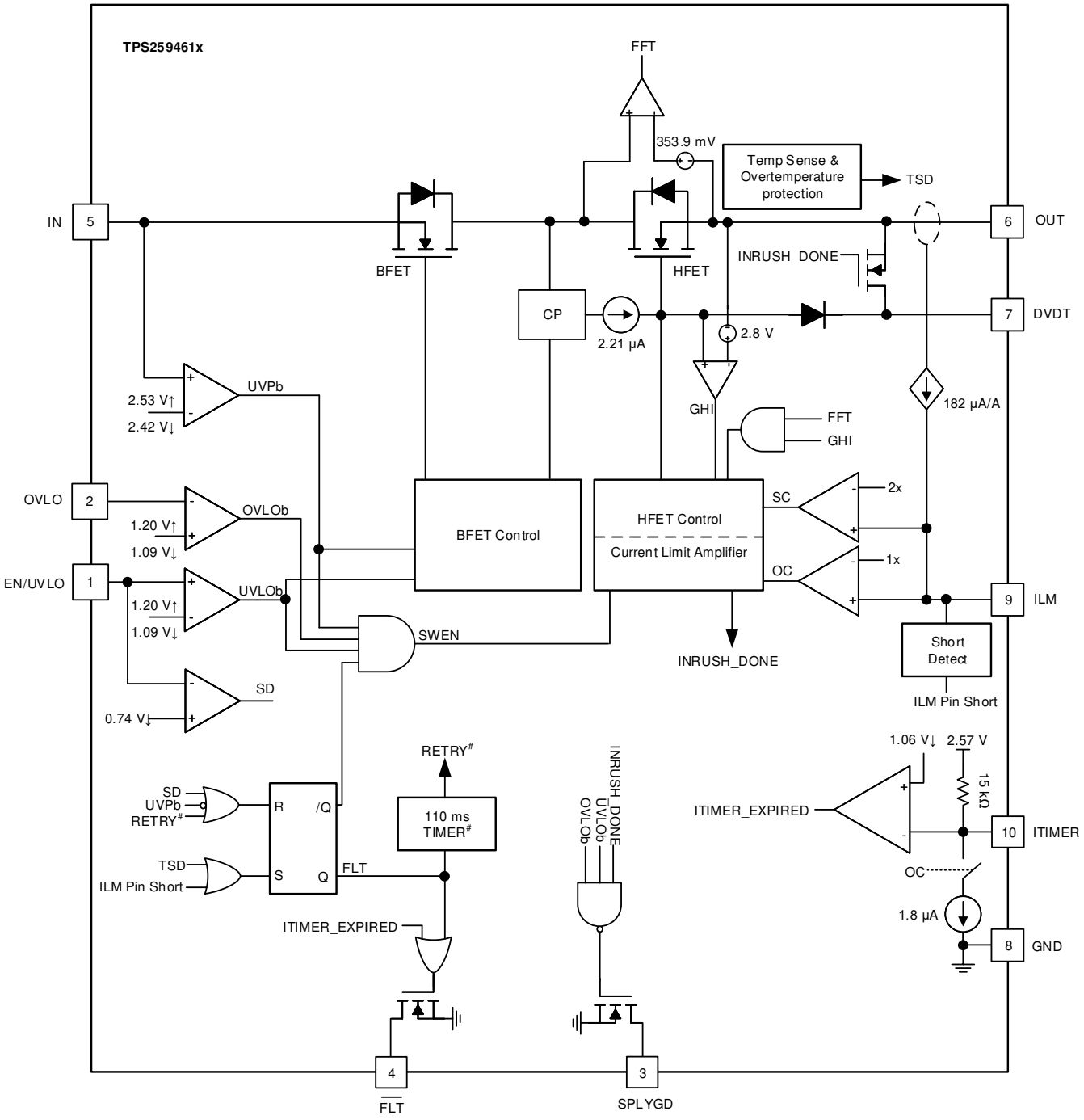
The device also has a built-in thermal sensor based shutdown mechanism to protect itself in case the device temperature (T_J) exceeds the recommended operating conditions.

8.2 Functional Block Diagram



Not applicable to Latch-off variants (TPS259460L)

図 8-1. TPS259460x Block Diagram



Not applicable to Latch-off variants (TPS259461L)

図 8-2. TPS259461x Block Diagram

8.3 Feature Description

The TPS25946xx eFuse is a compact, feature rich power management device that provides detection, protection and indication in the event of system faults.

8.3.1 Undervoltage Lockout (UVLO and UVP)

The TPS25946xx implements Undervoltage Protection on IN in case the applied voltage becomes too low for the system or device to properly operate. The Undervoltage Protection has a default lockout threshold of V_{UVP} which is fixed internally. Also, the UVLO comparator on the EN/UVLO pin allows the Undervoltage Protection threshold to be externally adjusted to a user defined value. The 図 8-3 and 式 1 show how a resistor divider can be used to set the UVLO set point for a given voltage supply.

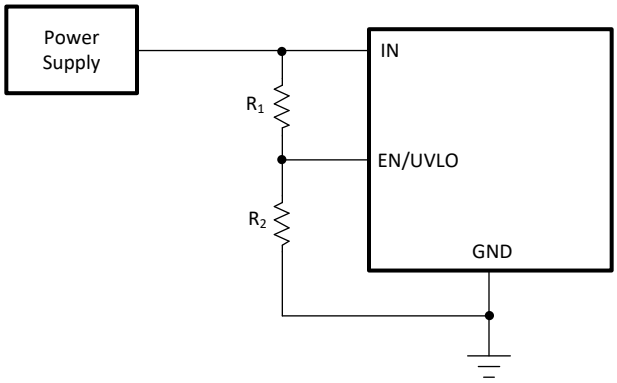


図 8-3. Adjustable Undervoltage Protection

$$V_{IN(UV)} = \frac{V_{UVLO} \times (R1 + R2)}{R2} \quad (1)$$

8.3.2 Overvoltage Lockout (OVLO)

The TPS25946xx allows the user to implement Overvoltage Lockout to protect the load from input overvoltage conditions. The OVLO comparator on the OVLO pin allows the Overvoltage Protection threshold to be adjusted to a user defined value. After the voltage at the OVLO pin crosses the OVLO rising threshold $V_{OV(R)}$, the device turns off the power to the output. Thereafter, the devices wait for the voltage at the OVLO pin to fall below the OVLO falling threshold $V_{OV(F)}$ before the output power is turned ON again. The rising and falling thresholds are slightly different to provide hysterisis. The 図 8-4 and 式 2 show how a resistor divider can be used to set the OVLO set point for a given voltage supply.

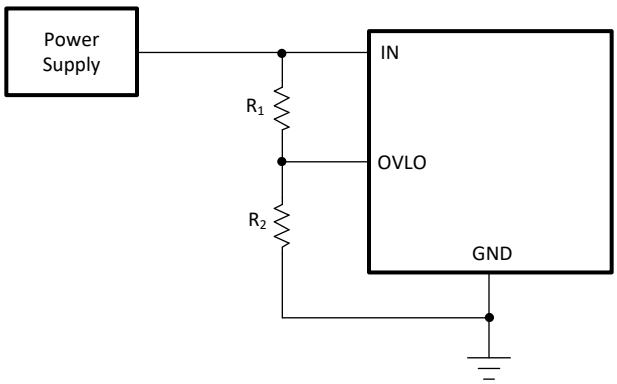


図 8-4. Adjustable Overvoltage Protection

$$V_{IN(OV)} = \frac{V_{OV} \times (R1 + R2)}{R2} \quad (2)$$

While recovering from a OVLO event, the TPS25946xx starts up with inrush control (dVdt).

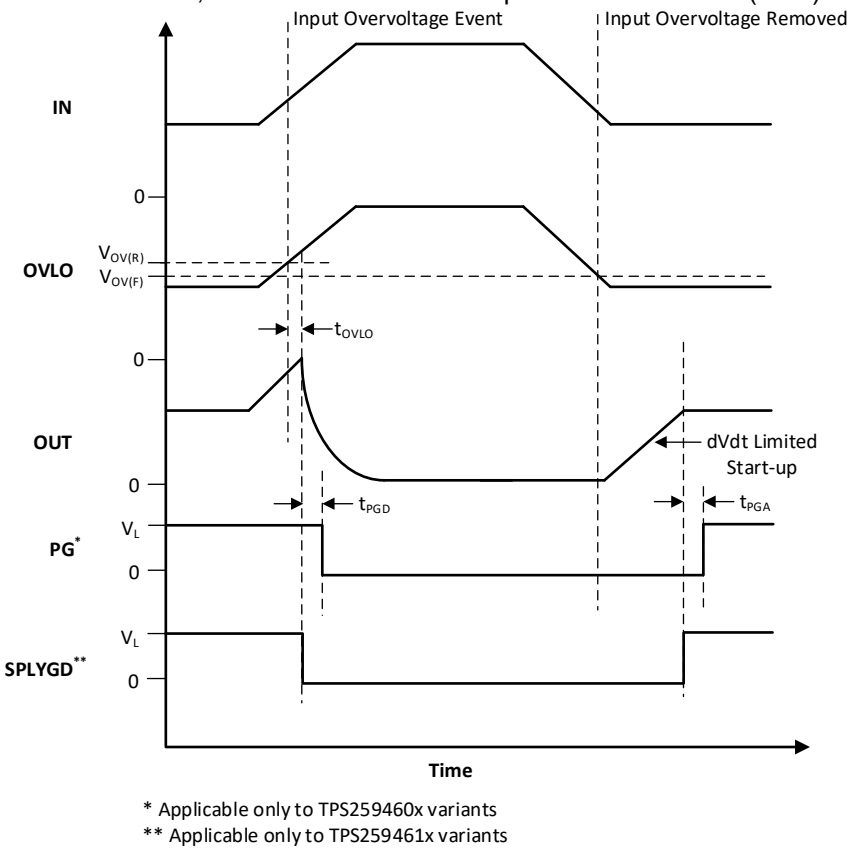


図 8-5. TPS25946xx Overvoltage Lockout and Recovery

8.3.3 Inrush Current, Overcurrent, and Short-Circuit Protection

TPS25946xx incorporates four levels of protection against overcurrent in forward direction (IN to OUT):

1. Adjustable slew rate (dVdt) for inrush current control
2. Adjustable threshold (I_{LIM}) for overcurrent protection during start-up or steady-state
3. Adjustable threshold (I_{SC}) for fast-trip response to severe overcurrent during start-up or steady-state
4. Fixed threshold (I_{FT}) for fast-trip response to quickly protect against hard output short-circuits during steady-state

8.3.3.1 Slew Rate (dVdt) and Inrush Current Control

During hot-plug events or while trying to charge a large output capacitance at start-up, there can be a large inrush current. If the inrush current is not managed properly, it can damage the input connectors and/or cause the system power supply to droop leading to unexpected restarts elsewhere in the system. The inrush current during turn-on is directly proportional to the load capacitance and rising slew rate. 式 3 can be used to find the slew rate (SR) required to limit the inrush current (I_{INRUSH}) for a given load capacitance (C_{OUT}):

$$SR\,(V/ms) = \frac{I_{INRUSH}\,(mA)}{C_{OUT}\,(\mu F)} \quad (3)$$

A capacitor can be connected to the dVdt pin to control the rising slew rate and lower the inrush current during turn-on. The required C_{dVdt} capacitance to produce a given slew rate can be calculated using 式 4.

$$C_{dVdt}\,(pF) = \frac{2000}{SR\,(V/ms)} \quad (4)$$

The fastest output slew rate is achieved by leaving the dVdt pin open.

Note

For C_{dVdt} > 10 nF, TI recommends to add a 100-Ω resistor in series with the capacitor on the dVdt pin.

8.3.3.2 Active Current Limiting

The TPS25946xx responds to output overcurrent conditions by actively limiting the current after a user adjustable transient fault blanking interval. When the load current exceeds the set overcurrent threshold (I_{LIM}) set by the ILM pin resistor (R_{ILM}), but stays lower than the short-circuit threshold (2 × I_{LIM}), the device starts discharging the ITIMER pin capacitor using an internal 1.8-µA pulldown current. If the load current drops below the overcurrent threshold before the ITIMER capacitor (C_{ITIMER}) discharges by ΔV_{ITIMER}, the ITIMER is reset by pulling it up to V_{INT} internally and the current limit action is not engaged. This allows short load transient pulses to pass through the device without getting current limited. If the overcurrent condition persists, the C_{ITIMER} continues to discharge and after it discharges by ΔV_{ITIMER}, the current limit starts regulating the HFET to actively limit the current to the set overcurrent threshold (I_{LIM}). At the same time, the C_{ITIMER} is charged up to V_{INT} again so that it is at its default state before the next overcurrent event. This ensures the full blanking timer interval is provided for every overcurrent event. 式 5 can be used to calculate the R_{ILM} value for a desired overcurrent threshold.

$$R_{ILM}\,(\Omega) = \frac{3334}{I_{LIM}\,(A)} \quad (5)$$

Note

1. The device offers overcurrent protection only in forward direction, that is from IN to OUT. There is no overcurrent protection from OUT to IN during ON state.
2. Leaving the ILM pin Open sets the current limit to nearly zero and results in the part entering current limit with the slightest amount of loading at the output.
3. The current limit circuit employs a foldback mechanism. The current limit threshold in the foldback region (0 V < V_{OUT} < V_{FB}) is lower than the steady state current limit threshold (I_{LIM}).
4. Shorting the ILM pin to ground at any point during normal operation is detected as a fault and the part shuts down. There is a minimum current (I_{FLT}) which the part allows in this condition before the pin short condition is detected.

The duration for which transients are allowed can be adjusted using an appropriate capacitor value from ITIMER pin to ground. The C_{ITIMER} value needed to set the desired transient overcurrent blanking interval can be calculated using 式 6 below.

$$t_{ITIMER}\,(ms) = \frac{\Delta V_{ITIMER}\,(V) \times C_{ITIMER}\,(nF)}{I_{ITIMER}\,(\mu A)} \quad (6)$$

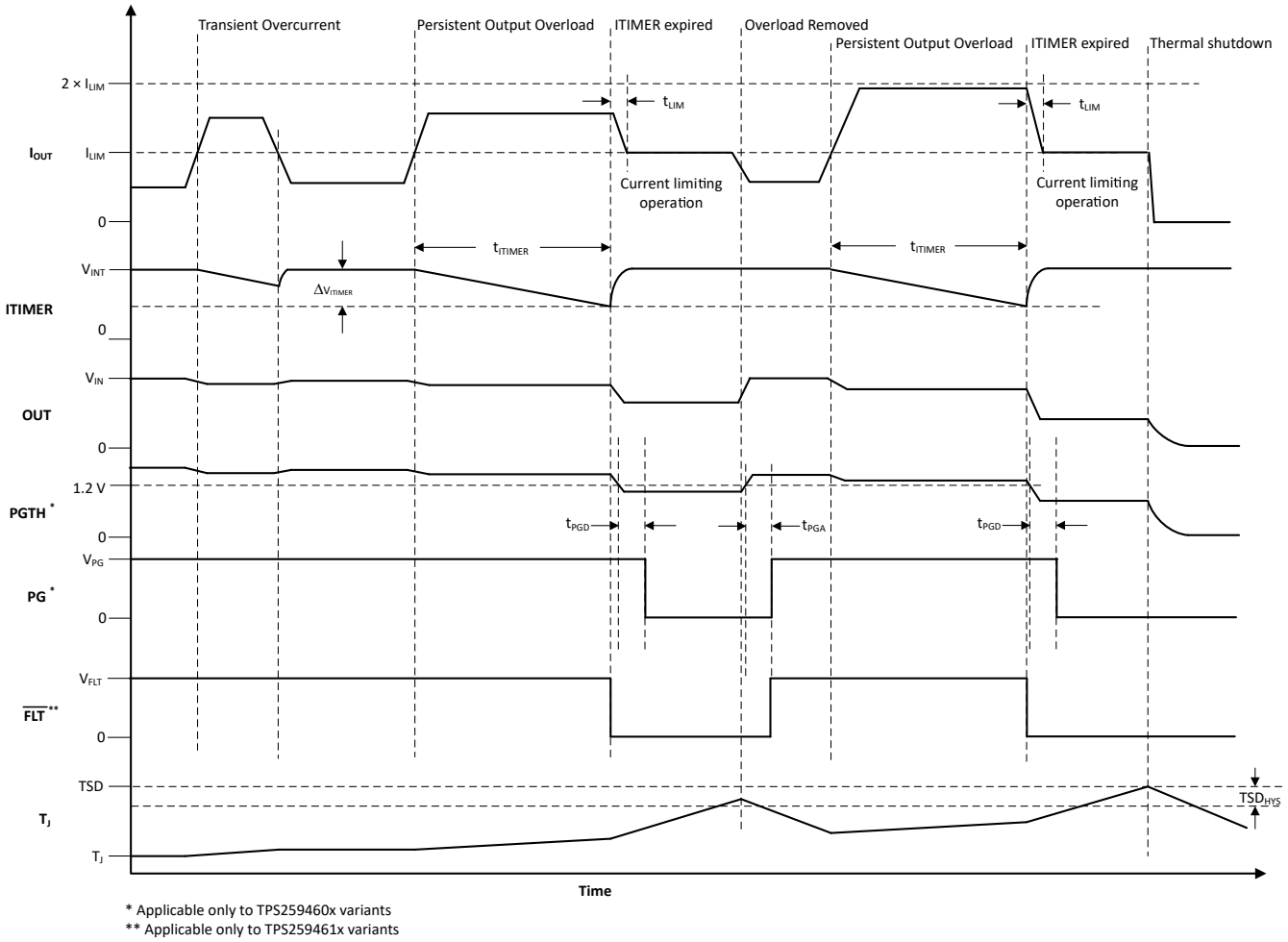


図 8-6. TPS25946xx Active Current Limit Response

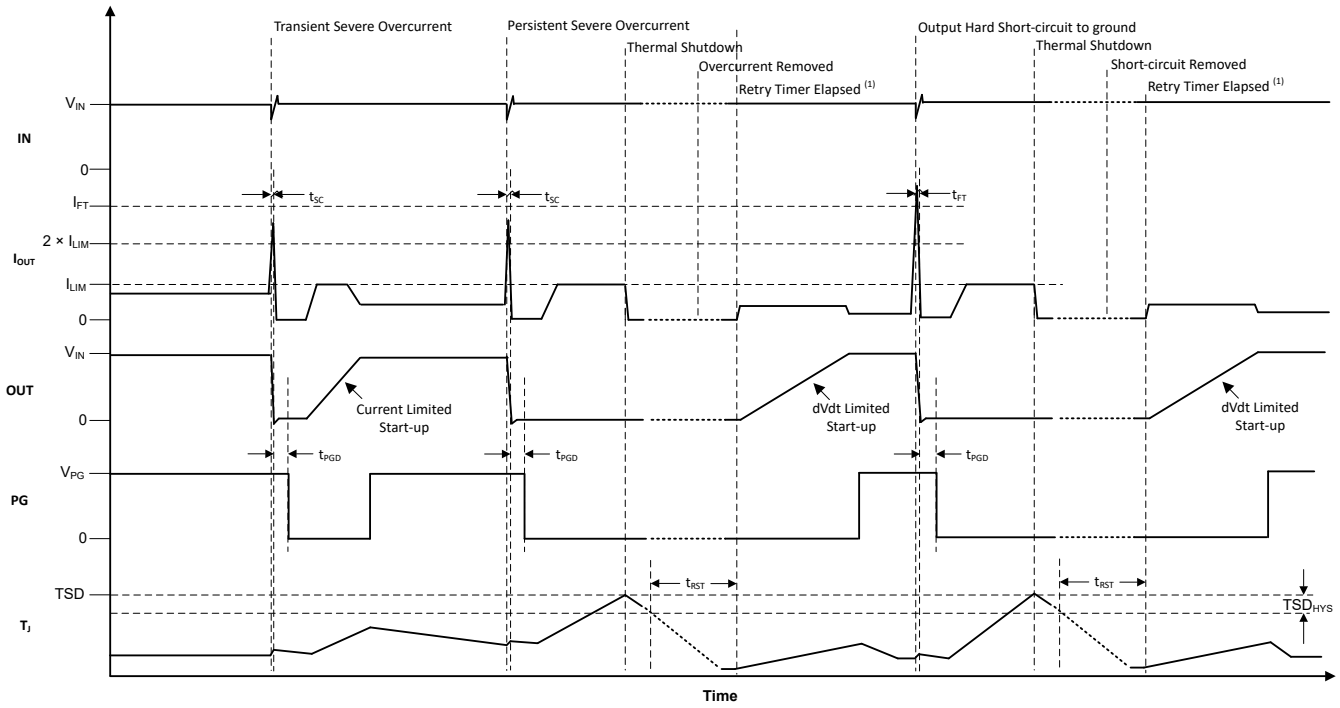
Note

1. Leave the ITIMER pin open to allow the part to limit the current with the minimum possible delay.
2. Shorting the ITIMER pin to ground results in minimum overcurrent response delay (similar to ITIMER pin open condition), but increases the device current consumption. This is not a recommended mode of operation.
3. Active current limiting based on R_{ILM} is active during start-up. In case the start-up current exceeds I_{LIM}, the device regulates the current to the set limit. However, during start-up the current limit is engaged without waiting for the ITIMER delay.
4. Increasing the C_{ITIMER} value extends the overcurrent blanking interval, but it also extends the time needed for the C_{ITIMER} to recharge up to V_{INT}. If the next overcurrent event occurs before the C_{ITIMER} is recharged fully, it takes less time to discharge to the ITIMER expiry threshold, thereby providing a shorter blanking interval than intended.

During active current limit, the output voltage drops resulting in increased device power dissipation across the HFET. If the device internal temperature (T_J) exceeds the thermal shutdown threshold (TSD), the HFET is turned off. After the part shuts down due to TSD fault, it either stays latched off (TPS25946xL variants) or restarts automatically after a fixed delay (TPS25946xA variants). See *Overtemperature Protection (OTP)* for more details on device response to overtemperature.

8.3.3.3 Short-Circuit Protection

During an short-circuit event on OUT pin, the current from IN to OUT increases very rapidly. When a severe overcurrent condition is detected, the TPS25946xx triggers a fast-trip response to limit the current through the device to a safe level. The internal fast-trip comparator employs a scalable threshold (I_{SC}) which is equal to 2 × I_{LIM}. This enables the user to adjust the fast-trip threshold rather than using a fixed threshold which can be too high for some low current systems. The device also employs a fixed fast-trip threshold (I_{FT}) to protect fast protection against hard short-circuits during steady state. The fixed fast-trip threshold is higher than the maximum recommended user adjustable scalable fast-trip threshold. After the current exceeds I_{SC} or I_{FT}, the HFET is turned off completely within t_{FT}. Thereafter, the devices tries to turn the HFET back on after a short de-glitch interval (30 µs) in a current limited manner instead of a dVdt limited manner. This ensures that the HFET has a faster recovery after a transient overcurrent event and minimizes the output voltage droop. However, if the fault is persistent, the device stays in current limit causing the junction temperature to rise and eventually enter thermal shutdown. See *Overtemperature Protection (OTP)* section for details on the device response to overtemperature.



(1) Applicable only to TPS259460A variants

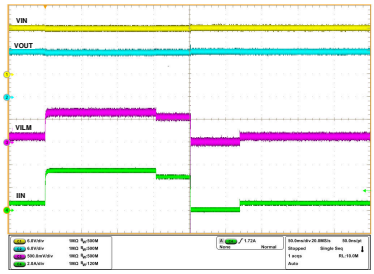
図 8-7. TPS25946xx Short-Circuit Response

8.3.4 Analog Load Current Monitor

The TPS25946xx allows the system to accurately monitor the load current by providing an analog current sense output on the ILM pin which is proportional to the current through the FET from IN to OUT. The user can sense the voltage (V_{ILM}) across the R_{ILM} to get a measure of the output load current.

$$I_{OUT}\,(A) = \frac{V_{ILM}\,(\mu V)}{R_{ILM}\,(\Omega) \times G_{IMON}\,(\mu A/A)} \tag{7}$$

The waveform below shows the ILM signal response to a load step at the output.



V_{IN} = 12 V, C_{OUT} = 22 µF, R_{ILM} = 1150 Ω, I_{OUT} varied dynamically between 0 A and 3.5 A

図 8-8. Analog Load Current Monitor Response

Note

1. The ILM pin is sensitive to capacitive loading. Careful design and layout is needed to ensure the parasitic capacitive loading on the ILM pin is < 50 pF for stable operation.
2. The ILM pin can only report the current flowing from IN to OUT and not from OUT to IN.

8.3.5 Reverse Current Protection

The TPS25946xx has integrated back-to-back MOSFETs connected in a common drain configuration. When the device is in powered down or disabled state, both the FETs are turned OFF, thereby blocking the current flow in forward as well as reverse direction.

8.3.6 Overtemperature Protection (OTP)

The TPS25946xx monitors the internal die temperature (T_J) at all times and shuts down the part as soon as the temperature exceeds a safe operating level (TSD), thereby protecting the device from damage. The device does not turn back on until the junction cools down sufficiently, that is the die temperature falls below (TSD – TSD_{HYS}).

When the TPS25946xL (latch-off variant) detects thermal overload, it is shut down and remain latched-off until the device is power cycled or re-enabled. When the TPS25946xA (auto-retry variant) detects thermal overload, it remains off until it has cooled down by TSD_{HYS}. Thereafter, the device remains off for an additional delay of t_{RST} after which it automatically retries to turn on if it is still enabled.

表 8-1. Thermal Shutdown

DEVICE	ENTER TSD	EXIT TSD
TPS25946xL (Latch-Off)	T_J ≥ TSD	T_J < TSD – TSD_{HYS} V_{IN} cycled to 0 V and then above $V_{UVP(R)}$ OR EN/UVLO toggled below $V_{SD(F)}$
TPS25946xA (Auto-Retry)	T_J ≥ TSD	T_J < TSD – TSD_{HYS} V_{IN} cycled to 0 V and then above $V_{UVP(R)}$ OR EN/UVLO toggled below $V_{SD(F)}$ OR t_{RST} timer expired

8.3.7 Fault Response and Indication ($\overline{FLT}$)

The following table summarizes the device response to various fault conditions. Additionally, an active low external fault indication ($\overline{FLT}$) pin is available on the TPS259461x variants.

表 8-2. Fault Summary

Event	Protection Response	Fault Latched Internally	$\overline{FLT}$ Pin Status(1)	$\overline{FLT}$ Assertion Delay(1)
Overtemperature	Shutdown	Y	L	
Undervoltage (UVP or UVLO)	Shutdown	N	H	
Input Overvoltage	Shutdown	N	H	
Transient Overcurrent (I_{LIM} < I_{OUT} < 2 × I_{LIM})	None	N	H	
Persistent Overcurrent in Forward Direction (IN to OUT)	Current Limit	N	L	t_{ITIMER}
OUT Pin Short-Circuit to GND	Circuit Breaker followed by Current Limit	N	H	
ILM Pin Open (During Steady State)	Shutdown	N	L	t_{ITIMER}
ILM Pin Shorted to GND	Shutdown	Y	L	t_{ITIMER}

(1) Applicable to TPS259461x variants only.

Faults which are latched internally can be cleared either by power cycling the part (pulling V_{IN} to 0 V) or by pulling the EN/UVLO pin voltage below V_{SD}. This also resets the t_{RST} timer for the TPS25946xA (auto-retry) variants.

During a latched fault, pulling the EN/UVLO just below the UVLO threshold has no impact on the device. This is true for both TPS25946xL (latch-off) and TPS25946xA (auto-retry) variants.

The TPS25946xA (auto-retry) variants restart automatically on expiry of the t_{RST} timer after a fault.

8.3.8 Power Good Indication (PG)

The TPS259460x variants provide an active high digital output (PG) which serves as a power good indication signal and is asserted high depending on the voltage at the PGTH pin along with the device state information. The PG is an open-drain pin and must be pulled up to an external supply.

After power up, PG is pulled low initially. The device initiates a inrush sequence in which the HFET is turned on in a controlled manner. When the HFET gate voltage reaches the full overdrive indicating that the inrush sequence is complete and the voltage at PGTH is above $V_{PGTH(R)}$, the PG is asserted after a de-glitch time (t_{PGA}).

PG is de-asserted if at any time during normal operation, the voltage at PGTH falls below $V_{PGTH(F)}$ or the device detects a fault (except overcurrent). The PG de-assertion de-glitch time is t_{PGD}.

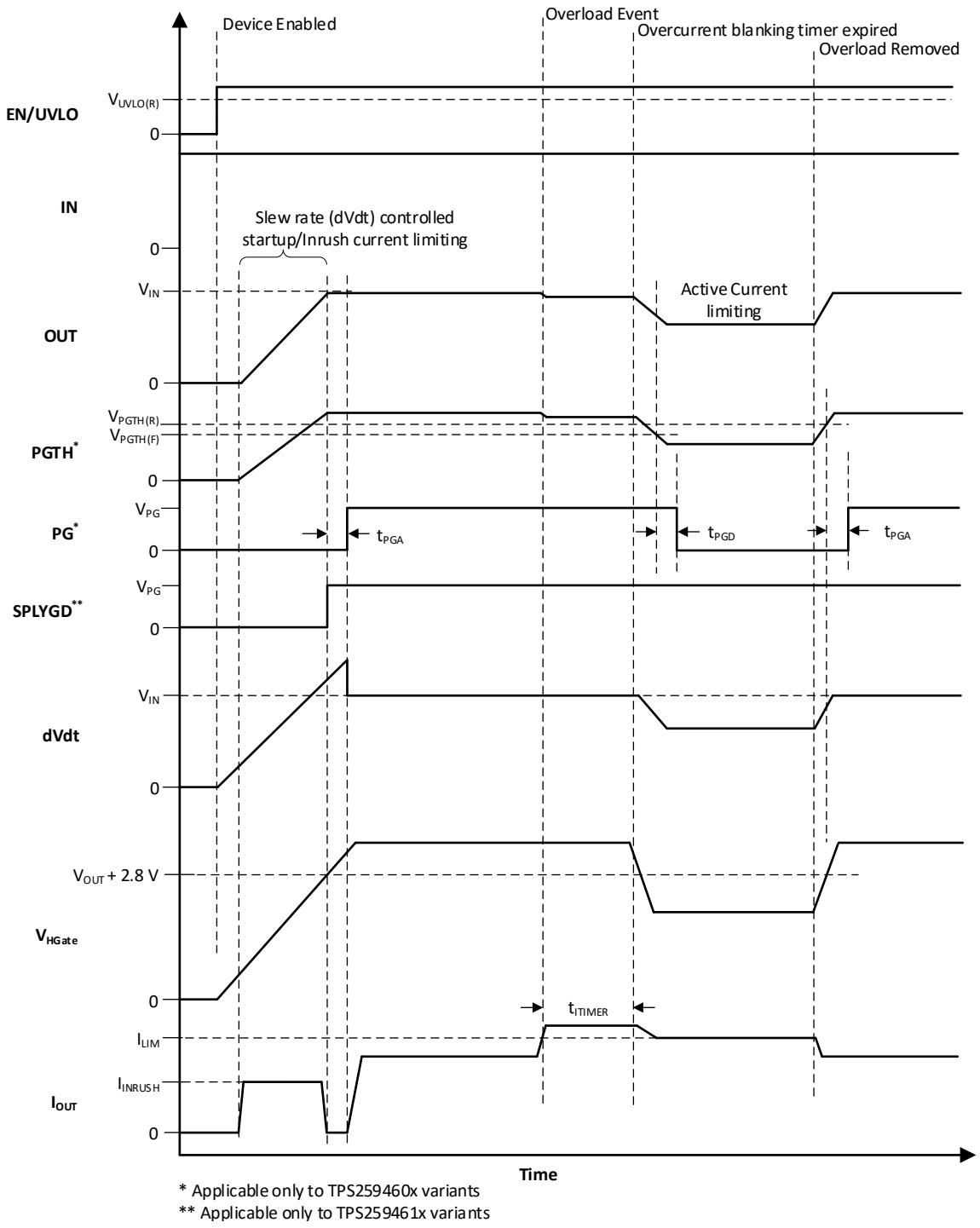


図 8-9. TPS259460x PG Timing Diagram

表 8-3. TPS259460x PG Indication Summary

Event	Protection Response	PG Pin Status	PG Delay
Undervoltage (UVP or UVLO)	Shutdown	L	
Overvoltage (OVLO)	Shutdown	L (If PGTH pin voltage < $V_{PGTH(F)}$)	t_{PGD}
Steady State	NA	H (If PGTH pin voltage > $V_{PGTH(R)}$) L (If PGTH pin voltage < $V_{PGTH(F)}$)	t_{PGA} t_{PGD}
Transient overcurrent	NA	H (If PGTH pin voltage > $V_{PGTH(R)}$) L (If PGTH pin voltage < $V_{PGTH(F)}$)	t_{PGA} t_{PGD}
Persistent overload in forward direction (IN to OUT)	Current Limiting	H (If PGTH pin voltage > $V_{PGTH(R)}$) L (If PGTH pin voltage < $V_{PGTH(F)}$)	t_{PGA} t_{PGD}
OUT Pin Short-Circuit to GND	Fast-trip followed by Current Limit	H (If PGTH pin voltage > $V_{PGTH(R)}$) L (If PGTH pin voltage < $V_{PGTH(F)}$)	t_{PGA} t_{PGD}
ILM Pin Open	Shutdown	L (If PGTH pin voltage < $V_{PGTH(F)}$)	t_{PGD}
ILM Pin Shorted to GND	Shutdown	L (If PGTH pin voltage < $V_{PGTH(F)}$)	t_{PGD}
Overtemperature	Shutdown	L	

When there is no supply to the device, the PG pin is expected to stay low. However, there is no active pulldown in this condition to drive this pin all the way down to 0 V. If the PG pin is pulled up to an independent supply which is present even if the device is unpowered, there can be a small voltage seen on this pin depending on the pin sink current, which is a function of the pullup supply voltage and resistor. Minimize the sink current to keep this pin voltage low enough not to be detected as a logic HIGH by associated external circuits in this condition.

8.3.9 Input Supply Good Indication (SPLYGD)

The TPS259461x variants provide an active high digital output (SPLYGD) which is asserted to indicate when the input supply is in a valid range (above UVP/UVLO and below OVLO thresholds) and the device has successfully completed its inrush sequence. This pin can be used as a supply valid status indication to the downstream load or system supervisor.

The SPLYGD pin is an open-drain signal which must be pulled up to an external supply.

After power up, SPLYGD pin is pulled low initially. The device initiates a inrush sequence in which the HFET is turned on in a controlled manner. When the FET gate voltage has reached the full overdrive indicating that the inrush sequence is complete and device is capable of delivering full power, the SPLYGD pin is asserted high. Thereafter, the SPLYGD pin is de-asserted only if the input supply becomes invalid (below UVP/UVLO or above OVLO thresholds). No load side events/faults have any control over the SPLYGD de-assertion.

表 8-4. TPS259461x SPLYGD Indication Summary

Event	SPLYGD Pin
Undervoltage (UVP or UVLO)	L
Overvoltage (OVLO)	L
Inrush	L
Steady State	H
Overcurrent	H
OUT Pin Short-Circuit to GND	H
ILM Pin Open	H
ILM Pin Shorted to GND	H
Overtemperature	H

When there is no supply to the device, the SPLYGD pin is expected to stay low. However, there is no active pulldown in this condition to drive this pin all the way down to 0 V. If the SPLYGD pin is pulled up to an independent supply which is present even if the device is unpowered, there can be a small voltage seen on this pin depending on the pin sink current, which is a function of the pullup supply voltage and resistor. Minimize the sink current to keep this pin voltage low enough not to be detected as a logic HIGH by associated external circuits in this condition.

8.4 Device Functional Modes

The device has one mode of operation that applies when operated within the Recommended Operating Conditions.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPS25946xx is a 2.7-V to 23-V, 5.5-A eFuse that is typically used for power rail protection applications. The device operates from 2.7 V to 23 V with adjustable overvoltage and undervoltage protection. The device provides ability to control inrush current and bidirectional current flow when enabled. The device can be used in a variety of applications such as smartphones, tablets, digital cameras, point of sales terminals, USB On-The-Go (OTG) enabled devices, wireless chargers, and so forth. The design procedure explained in the subsequent sections can be used to select the supporting component values based on the application requirement. Additionally, a spreadsheet design tool, *TPS25946xx Design Calculator*, is available in the web product folder.

9.1.1 Single Device, Self-Controlled

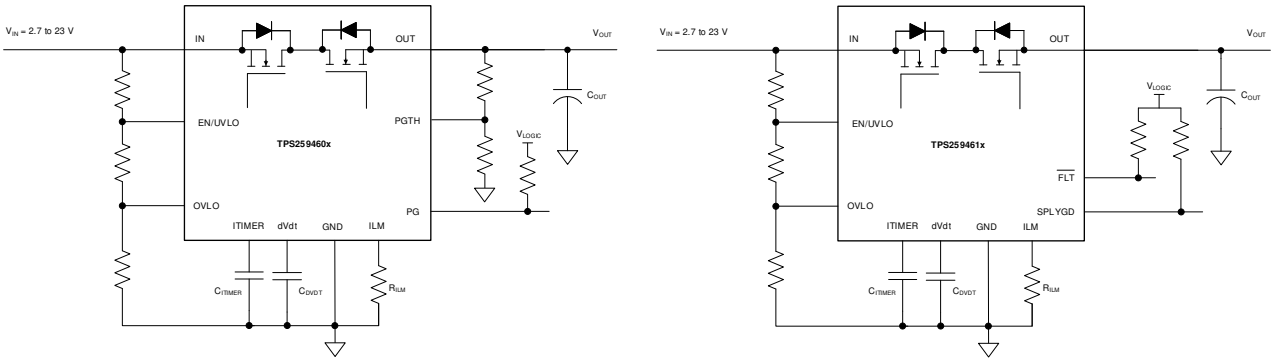


図 9-1. Single Device, Self-Controlled

Other Variations:

In a Host MCU controlled system, EN/UVLO or OVLO can also be driven from the host GPIO to control the device.

ILM pin can be connected to the MCU ADC input for current monitoring purpose.

Note

TI recommends to keep parasitic capacitance on ILM pin below 50 pF to ensure stable operation.

For TPS259460x variants, either V_{IN} or V_{OUT} can be used to drive the PGTH resistor divider depending on which supply must be monitored for power good indication.

9.2 Typical Application

Smartphones come equipped with USB OTG functionality that allows their USB port to be used not only for charging the phone battery but also allow the smartphone to act as a USB host and deliver power to external accessories such as headphones, pen drives, and so forth. Some smartphones also support a wireless charging path which can also be used to wirelessly share power to other devices. TPS25946xx can be used as a bi-directional power switch in such applications as shown in 図 9-2.

For the USB power path, when an external charger is connected at the port, TPS25946xx provides a conduction path from IN pin to OUT pin and the battery charger IC is configured to charge the battery and also power the

internal circuits. TPS25946xx also provides overvoltage and overcurrent protection in this case. In another use case scenario where an accessory such as headphone is connected to the USB port, the phone MCU detects this and the battery charger is configured in OTG boost mode to provide power from battery to the USB port. In this case, the TPS25946xx also needs to be turned on to establish the power path from OUT to IN. Before that, there must be a minimum voltage ($V_{UVP(R)}$) available at the IN pin. An series diode and resistor is added in parallel to the device to provide this initial bias voltage. Once MCU detects that the accessory is connected, it enables the TPS25946xx and establishes a low impedance power path capable of delivering high power to the accessory.

Similarly, the TPS25946xx also provides controlled bi-directional power flow in the wireless charging and power share sub-system.

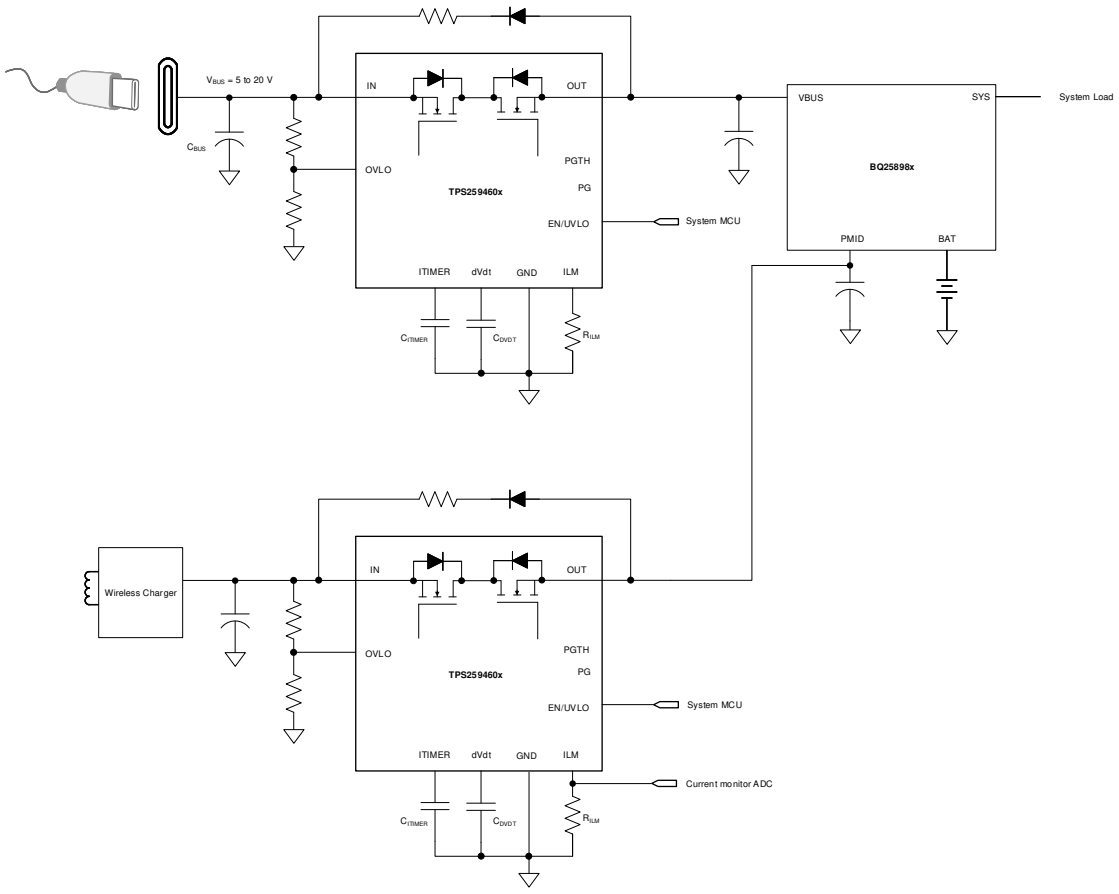
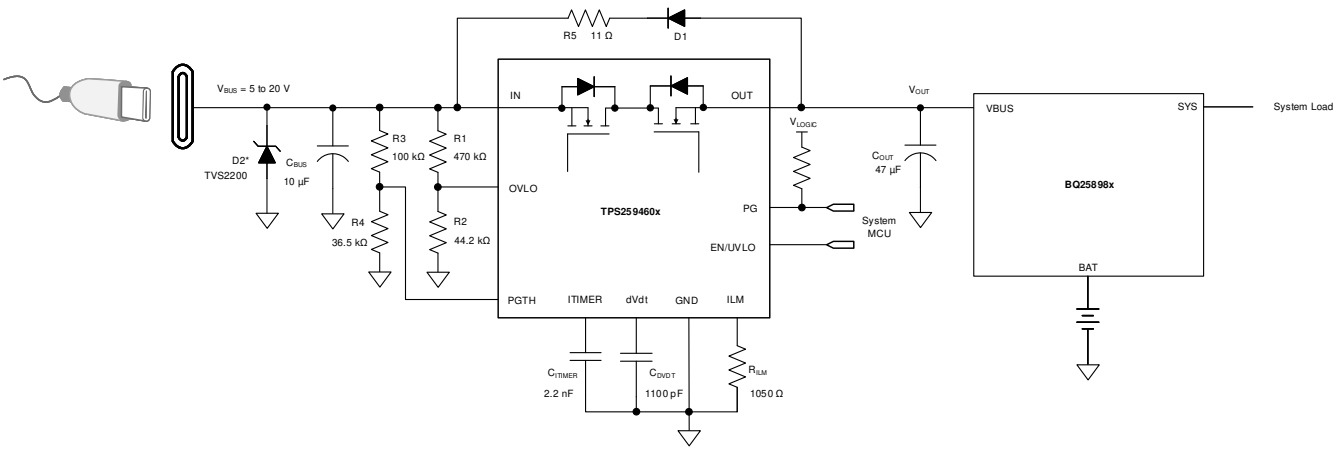


図 9-2. Smartphone Power Path Example



* Optional circuit components needed for transient protection. Please refer to *Transient Protection* section for details.

図 9-3. USB On-The-Go Port Protection Design Example

9.2.1 Design Requirements

表 9-1. Design Parameters

PARAMETER	VALUE
Bus voltage during charging (V_{IN})	9 V
Overvoltage protection threshold during charging ($V_{IN(OV)}$)	14 V
Bus power good threshold (V_{PG})	4.5 V
Max continuous charging current	3 A
Load transient blanking interval during charging (t_{ITIMER})	2 ms
Output capacitance (C_{OUT})	47 µF
Output rise time (t_R)	5 ms
Overcurrent threshold (I_{LIM}) during charging	3.25 A
Start-up load current supported during USB OTG operation (I_{LOAD})	100 mA
Fault response	Auto-retry

9.2.2 Detailed Design Procedure

9.2.2.1 Device Selection

TPS259460A variant is selected after refering to the *Device Comparison Table*.

9.2.2.2 Setting Overvoltage Threshold

The supply overvoltage threshold is set using the resistors, R1 and R2, whose values can be calculated using 式 8:

$$V_{IN(OV)} = \frac{V_{OV(R)} \times (R1 + R2)}{R2} \quad (8)$$

Where $V_{OV(R)}$ is the OVLO rising threshold. Because R1, R2 leak the current from input supply V_{IN}, these resistors must be selected based on the acceptable leakage current from input power supply V_{IN}. The current drawn by R1, R2 from the power supply is IR12 = V_{IN} / (R1 + R2). However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current, IR12, must be chosen to be 20 times greater than the leakage current expected on the OVLO pin.

From the device electrical specifications, OVLO leakage current is 0.1 µA (maximum), $V_{OV(R)}$ = 1.2 V. From design requirements, $V_{IN(OV)}$ = 14 V. To solve the equation, first choose the value of R1 = 470 kΩ and use the above equation to solve for R2 = 44.06 kΩ.

Using the closest standard 1% resistor values, we get R1 = 470 kΩ, R2 = 44.2 kΩ.

9.2.2.3 Setting Output Voltage Rise Time (t_R)

For a successful design, the junction temperature of device must be kept below the absolute maximum rating during both dynamic (start-up) and steady-state conditions. Dynamic power stresses often are an order of magnitude greater than the static stresses, so it is important to determine the right start-up time and inrush current limit required with system capacitance to avoid thermal shutdown during start-up.

The slew rate (SR) needed to achieve the desired output rise time can be calculated as:

$$\mathrm{SR\,(V/ms)} = \frac{\mathrm{V_{IN}\,(V)}}{\mathrm{t_R\,(ms)}} = \frac{9\ \mathrm{V}}{5\ \mathrm{ms}} = 1.8\ \mathrm{V/ms} \tag{9}$$

The C_{dVdt} needed to achieve this slew rate can be calculated as:

$$\mathrm{C_{dVdt}\,(pF)} = \frac{2000}{\mathrm{SR\,(V/ms)}} = \frac{2000}{1.8} = 1111\ \mathrm{pF} \tag{10}$$

Choose the nearest standard capacitor value as 1100 pF.

For this slew rate, the inrush current can be calculated as:

$$\mathrm{I_{INRUSH}\,(mA)} = \mathrm{SR\,(V/ms)} \times \mathrm{C_{OUT}\,(\mu F)} = 1.8 \times 47 = 84.6\ \mathrm{mA} \tag{11}$$

The average power dissipation inside the part during inrush can be calculated as:

$$\mathrm{PD_{INRUSH}\,(W)} = \frac{\mathrm{I_{INRUSH}\,(A)} \times \mathrm{V_{IN}\,(V)}}{2} = \frac{0.085 \times 9}{2} = 0.38\ \mathrm{W} \tag{12}$$

For the given power dissipation, the thermal shutdown time of the device must be greater than the ramp-up time t_R to avoid start-up failure. 図 9-4 shows the thermal shutdown limit, for 0.38 W of power, the shutdown time is over 100 ms which is very large as compared to t_R = 5 ms. Therefore, it is safe to use 5 ms as the start-up time for this application.

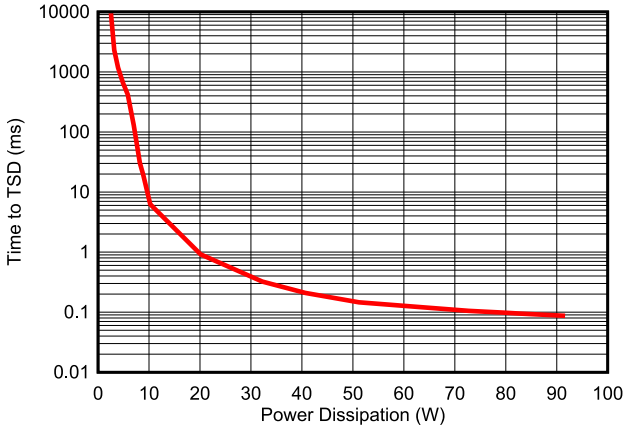


図 9-4. Thermal Shutdown Plot During Inrush

9.2.2.4 Setting Power Good Assertion Threshold

The Power Good assertion threshold can be set using the resistors R3 and R4 connected to the PGTH pin whose values can be calculated as:

$$V_{PG} = \frac{V_{PGTH(R)} \times (R3 + R4)}{R4} \quad (13)$$

Because R3 and R4 leak the current from the output rail V_{OUT}, these resistors must be selected to minimize the leakage current. The current drawn by R3 and R4 from the power supply is IR34 = V_{OUT} / (R3 + R4). However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current, IR34, must be chosen to be 20 times greater than the PGTH leakage current expected. From the device electrical specifications, PGTH leakage current is 1 µA (maximum), $V_{PGTH(R)}$ = 1.2 V and from design requirements, V_{PG} = 4.5 V. To solve the equation, first choose the value of R3 = 100 kΩ and calculate R4 = 36.4 kΩ. Choose nearest 1% standard resistor value as R4 = 36.5 kΩ.

9.2.2.5 Setting Overcurrent Threshold (I_{LIM})

The overcurrent protection (Circuit Breaker) threshold can be set using the R_{ILM} resistor whose value can be calculated as:

$$R_{ILM}\,(\Omega) = \frac{3334}{I_{LIM}\,(A)} = \frac{3334}{3.25\ A} = 1025.8\ \Omega \quad (14)$$

Choose nearest 1% standard resistor value as 1050 Ω.

9.2.2.6 Setting Overcurrent Blanking Interval (t_{ITIMER})

The overcurrent blanking timer interval can be set using the C_{ITIMER} capacitor whose value can be calculated as:

$$C_{ITIMER}\,(nF) = \frac{t_{ITIMER}\,(ms) \times I_{ITIMER}\,(\mu A)}{\Delta V_{ITIMER}\,(V)} = \frac{2 \times 1.8}{1.51} = 2.38\ nF \quad (15)$$

Choose nearest standard capacitor value as 2.2 nF.

9.2.2.7 Selecting External Bias Resistor (R5)

During OTG mode of operation, initially the TPS259460A is in OFF state. The initial bias voltage at the USB bus provided by external diode (D1) and resistor (R5) can be calculated as:

$$V_{BUS}\,(V) = V_{OUT}\,(V) - V_F\,(V) - I_{LOAD}\,(A) \times R5\,(\Omega)$$

Where

V_{OUT} = Voltage at OUT pin provided by the charger IC in OTG boost mode

V_F = diode forward voltage drop

I_{LOAD} = current drawn by USB powered peripheral initially

The bus voltage must be greater than $V_{UVP(R)}$ to ensure the TPS259460A can turn on and start delivering the full load current demanded by the USB peripheral. Putting the value of V_F = 0.4 V, V_{OUT} (minimum) = 4.5 V, $V_{UVP(R)}$ = 2.53 V, I_{LOAD} = 100 mA gives maximum value of R5 = 15.7 Ω. Choose value as 11 Ω.

Initial power dissipation across R5 can be calculated as:

$$PD\,(W) = I_{LOAD}\,(A) \times I_{LOAD}\,(A) \times R5\,(\Omega)$$

For I_{LOAD} = 100 mA and R5 = 11 Ω, the power dissipation in the resistor is 0.11 W. Choose a resistor with power rating higher than this value for safe operation. A 0.25-W resistor must be suitable for this application.

9.2.2.8 Selecting External Diode (D1)

1. Diode must have low forward voltage drop (V_F) to give more headroom to voltage at IN pin above V_{UVP}(R).
2. Diode must be able to support initial load current required by USB peripheral.
3. Diode must have small footprint.

9.2.3 Application Curve

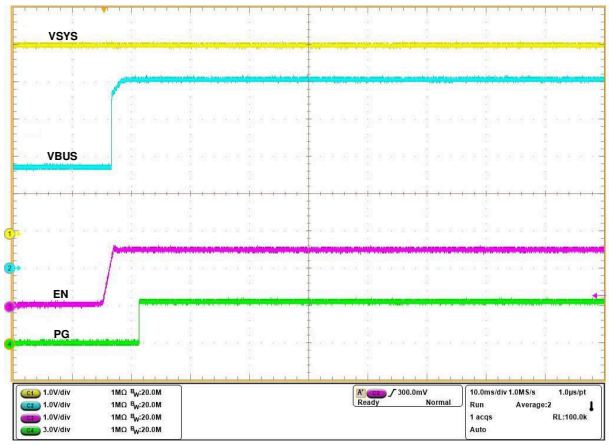


図 9-5. Power Up in OTG Mode

10 Power Supply Recommendations

The TPS25946xx devices are designed for a supply voltage range of 2.7 V ≤ V_{IN} ≤ 23 V. TI recommends an input ceramic bypass capacitor higher than 0.1 µF if the input supply is located more than a few inches from the device. The power supply must be rated higher than the set current limit to avoid voltage droops during overcurrent and short-circuit conditions.

10.1 Transient Protection

In the case of a short-circuit and overload current limit when the device interrupts current flow, the input inductance generates a positive voltage spike on the input, and the output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) is dependent on the value of inductance in series to the input or output of the device. Such transients can exceed the absolute maximum ratings of the device if steps are not taken to address the issue. Typical methods for addressing transients include:

- Minimize lead length and inductance into and out of the device.
- Use a large PCB GND plane.
- Connect a Schottky diode from the OUT pin ground to absorb negative spikes.
- Connect a low ESR capacitor larger than 1 µF at the OUT pin very close to the device.
- Use a low-value ceramic capacitor C_{IN} = 1 µF to absorb the energy and dampen the transients. The capacitor voltage rating must be at least twice the input supply voltage to be able to withstand the positive voltage excursion during inductive ringing.

  The approximate value of input capacitance can be estimated with 式 16:

$$V_{SPIKE\ (Absolute)} = V_{IN} + I_{LOAD} \times \sqrt{\frac{L_{IN}}{C_{IN}}} \tag{16}$$

  where

  – V_{IN} is the nominal supply voltage.
  – I_{LOAD} is the load current.
  – L_{IN} equals the effective inductance seen looking into the source.
  – C_{IN} is the capacitance present at the input.
- Some applications may require the addition of a Transient Voltage Suppressor (TVS) to prevent transients from exceeding the absolute maximum ratings of the device. In some cases, even if the maximum amplitude of the transients is below the absolute maximum rating of the device, a TVS can help to absorb the excessive energy dump and prevent it from creating very fast transient voltages on the input supply pin of the IC, which can couple to the internal control circuits and cause unexpected behavior.
- For applications such as USB-C ports where a powered cable can be plugged to the output of the device, there can be excess voltage stress from OUT to IN which exceeds the absolute maximum rating of the device. TI recommends to add a TVS diode from OUT to IN to clamp the voltage to a safe level.

The circuit implementation with optional protection components is shown in 図 10-1.

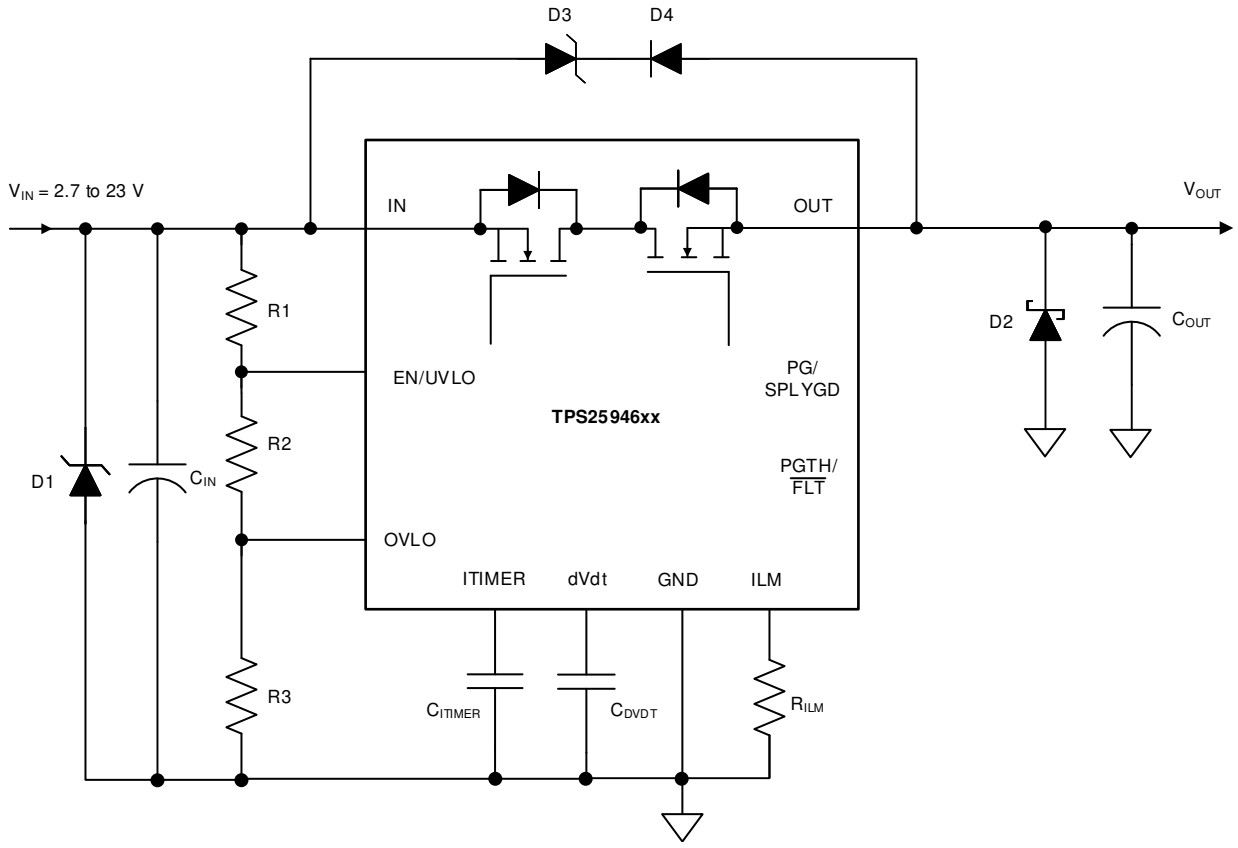


図 10-1. Circuit Implementation with Optional Protection Components

10.2 Output Short-Circuit Measurements

It is difficult to obtain repeatable and similar short-circuit testing results. The following contribute to variation in results:

- Source bypassing
- Input leads
- Circuit layout
- Component selection
- Output shorting method
- Relative location of the short
- Instrumentation

The actual short exhibits a certain degree of randomness because it microscopically bounces and arcs. Ensure that configuration and methods are used to obtain realistic results. Do not expect to see waveforms exactly like those in this data sheet because every setup is different.

11 Layout

11.1 Layout Guidelines

- For all applications, TI recommends a ceramic decoupling capacitor of 0.1 µF or greater between the IN terminal and GND terminal.
- The optimal placement of the decoupling capacitor is closest to the IN and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN terminal, and the GND terminal of the IC.
- High current-carrying power-path connections must be as short as possible and must be sized to carry at least twice the full-load current.
- The GND terminal must be tied to the PCB ground plane at the terminal of the IC with the shortest possible trace. The PCB ground must be a copper plane or island on the board. TI recommends to have a separate ground plane island for the eFuse. This plane doesn't carry any high currents and serves as a quiet ground reference for all the critical analog signals of the eFuse. The device ground plane must be connected to the system power ground plane using a star connection.
- The IN and OUT pins are used for heat dissipation. Connect to as much copper area on top and bottom PCB layers using as possible. Adding thermal vias on the under the device further helps to minimize the voltage gradient across the IN and OUT pads and distribute current uniformly through the device, which improves the on-resistance and current sense accuracy.
- Locate the following support components close to their connection pins:
  - R_{ILM}
  - C_{dVdT}
  - C_{ITIMER}
  - Resistors for the EN/UVLO, OVLO and PGTH pins
- Connect the other end of the component to the GND pin of the device with shortest trace length. The trace routing for the R_{ILM}, C_{ITIMER} and C_{dVdt} components to the device must be as short as possible to reduce parasitic effects on the current limit , overcurrent blanking interval and soft start timing. TI recommends to keep parasitic capacitance on ILM pin below 50 pF to ensure stable operation. These traces must not have any coupling to switching signals on the board.
- Because the bias current on ILM pin directly controls the overcurrent protection behavior of the device, the PCB routing of this node must be kept away from any noisy (switching) signals.
- Protection devices such as TVS, snubbers, capacitors, or diodes must be placed physically close to the device they are intended to protect. These protection devices must be routed with short traces to reduce inductance. For example, a protection Schottky diode is recommended to address negative transients due to switching of inductive loads. TI also recommends to add a ceramic decoupling capacitor of 1 µF or greater between OUT and GND. These components must be physically close to the OUT pins. Care must be taken to minimize the loop area formed by the Schottky diode/bypass-capacitor connection, the OUT pin and the GND terminal of the IC.

11.2 Layout Example

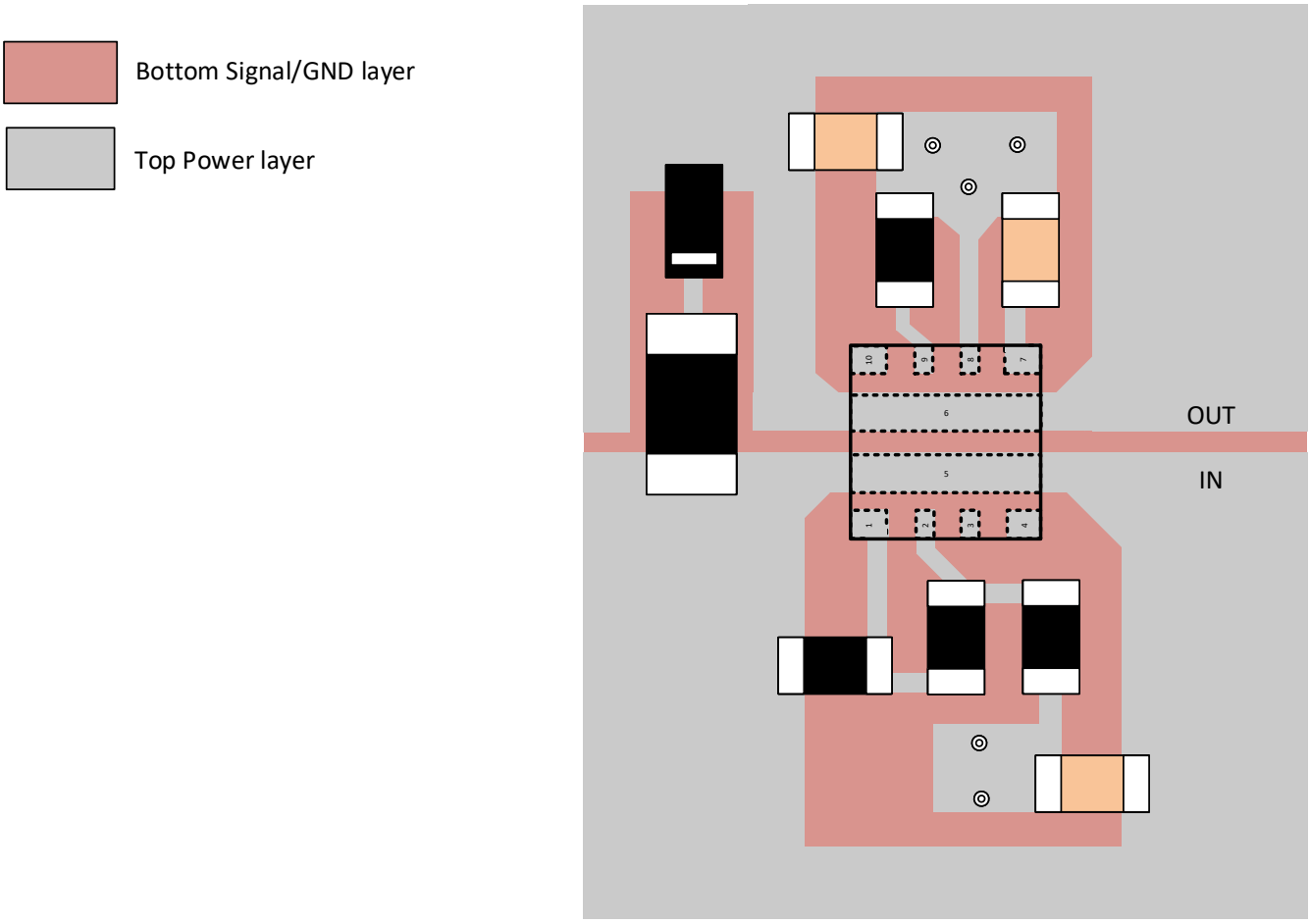


図 11-1. Layout Example

12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPS25946EVM eFuse Evaluation Board* user's guide
- Texas Instruments, *TPS25946xx Design Calculator*

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 サポート・リソース

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12.4 Trademarks

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS259460ARPWR	Active	Production	VQFN-HR (RPW) | 10	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2GKH
TPS259460ARPWR.A	Active	Production	VQFN-HR (RPW) | 10	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2GKH
TPS259460LRPWR	Active	Production	VQFN-HR (RPW) | 10	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2HCH
TPS259460LRPWR.A	Active	Production	VQFN-HR (RPW) | 10	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2HCH
TPS259461ARPWR	Active	Production	VQFN-HR (RPW) | 10	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2L6H
TPS259461ARPWR.A	Active	Production	VQFN-HR (RPW) | 10	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2L6H
TPS259461LRPWR	Active	Production	VQFN-HR (RPW) | 10	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2L7H
TPS259461LRPWR.A	Active	Production	VQFN-HR (RPW) | 10	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2L7H

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

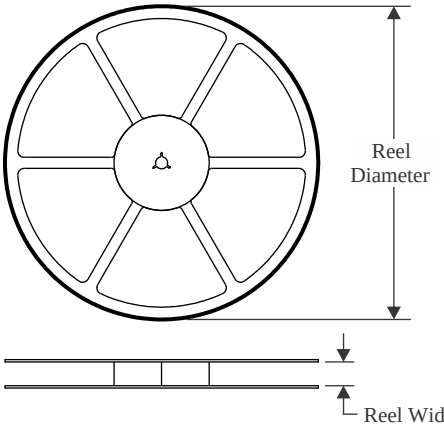
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

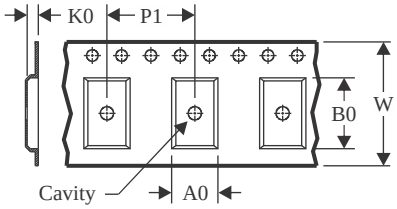
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

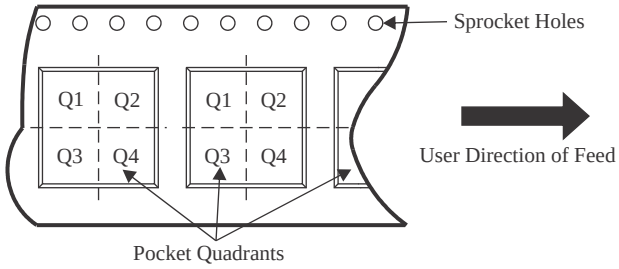


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

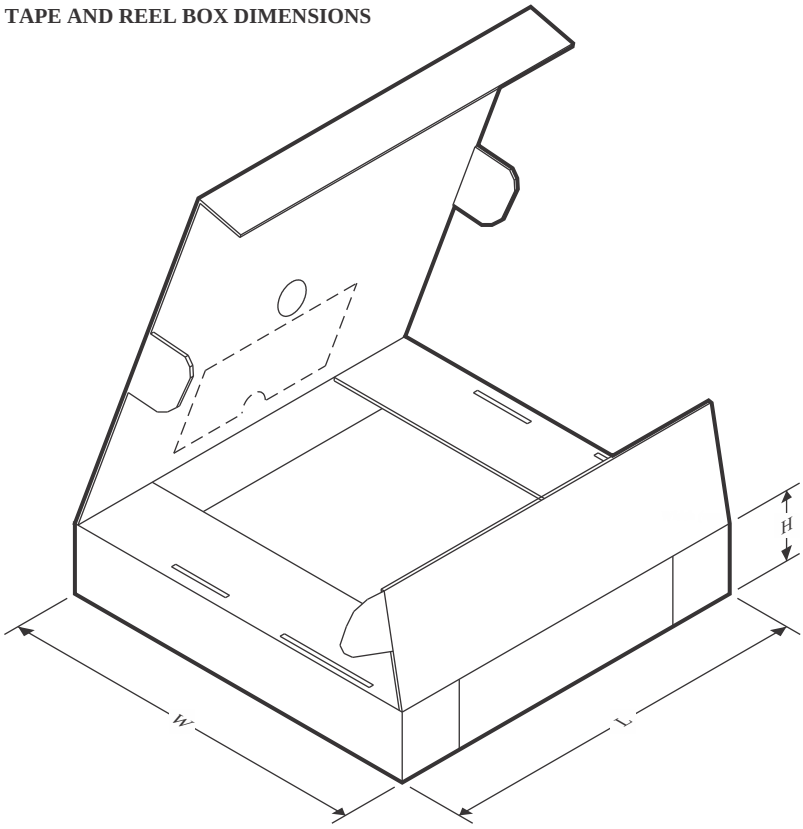
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS259460ARPWR	VQFN-HR	RPW	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259460LRPWR	VQFN-HR	RPW	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259461ARPWR	VQFN-HR	RPW	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259461LRPWR	VQFN-HR	RPW	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

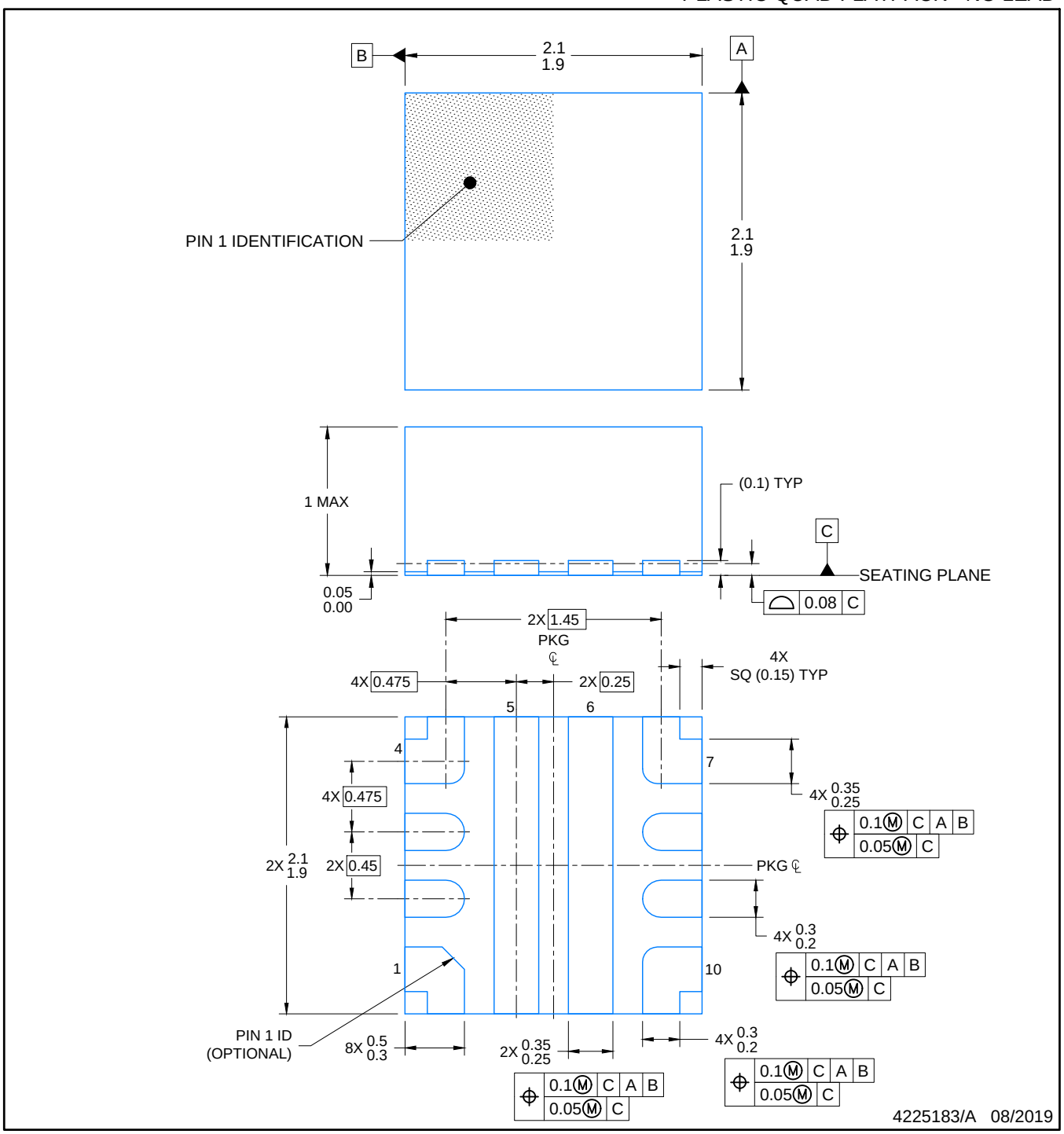
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS259460ARPWR	VQFN-HR	RPW	10	3000	210.0	185.0	35.0
TPS259460LRPWR	VQFN-HR	RPW	10	3000	210.0	185.0	35.0
TPS259461ARPWR	VQFN-HR	RPW	10	3000	210.0	185.0	35.0
TPS259461LRPWR	VQFN-HR	RPW	10	3000	210.0	185.0	35.0

PACKAGE OUTLINE

RPW0010A

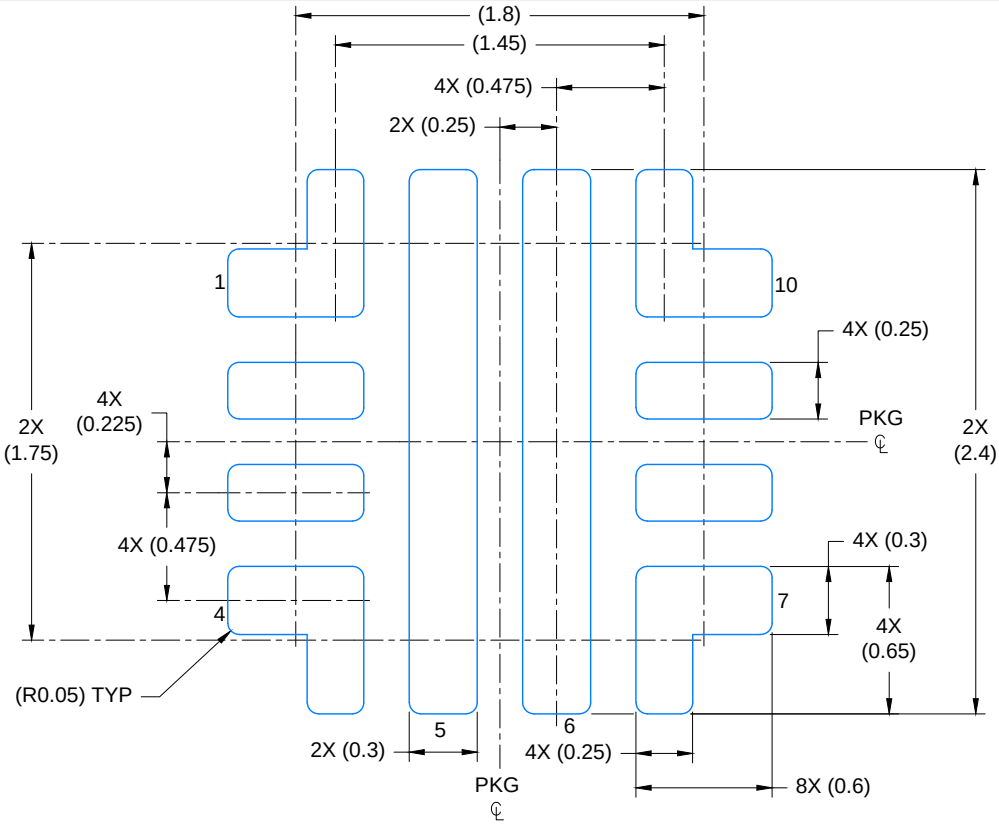
VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



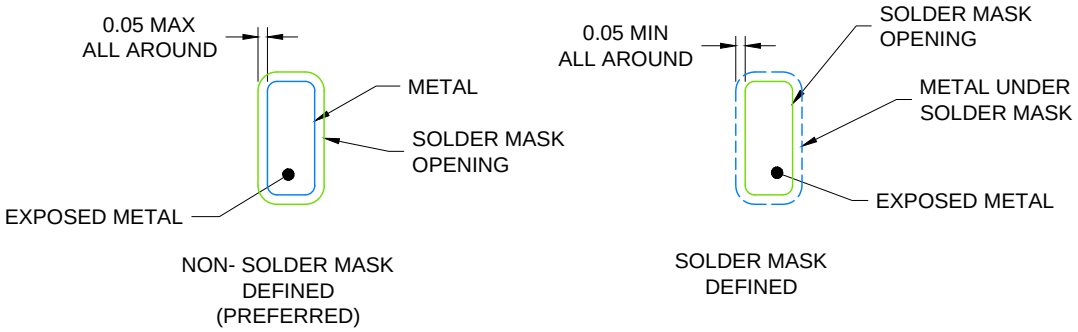
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE

SCALE: 30X



SOLDER MASK DETAILS

NOT TO SCALE

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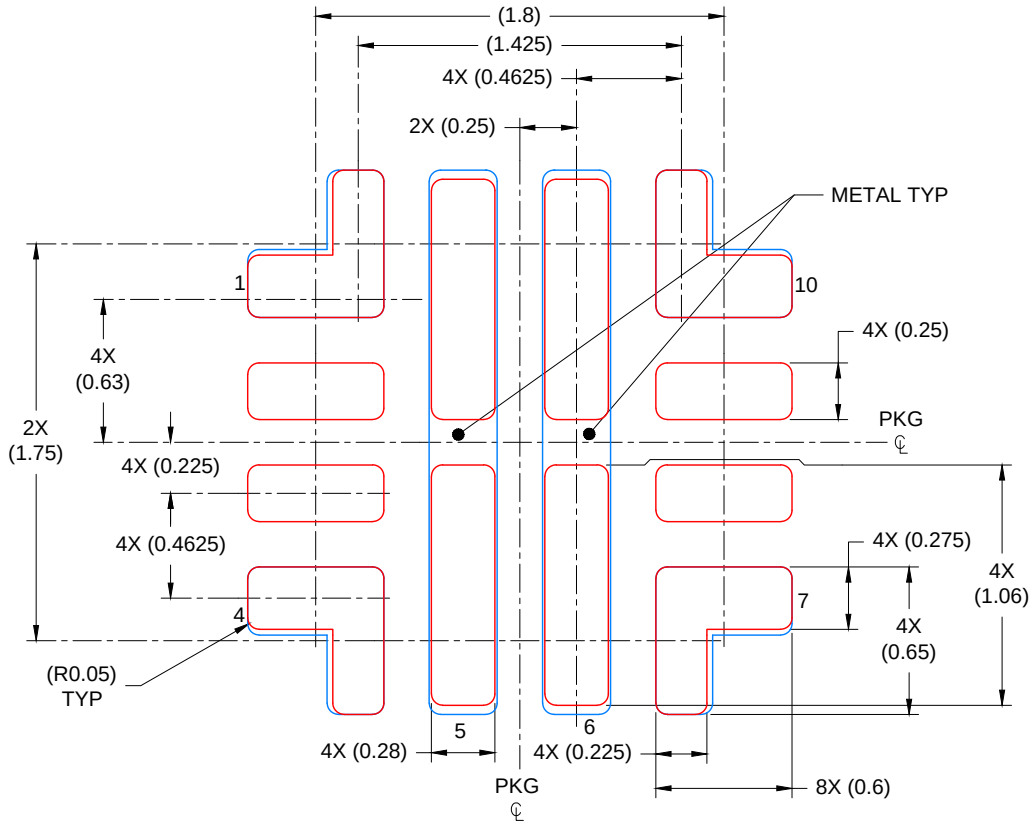
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.100 mm THICK STENCIL

PADS 1, 4,7 & 10: 93%; PADS 5 & 6: 82%
SCALE: 30X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月