

# TPS51206 2Aピーク・シンク/ソースDDRターミネーション・レギュレータ、DDR2/3/3L/4用のVTTREFバッファ付きリファレンス搭載

## 1 特長

- 入力電源電圧: 3.3Vレールと5Vレールをサポート
- VLDOIN入力電圧範囲: VTT+0.4V~3.5V
- VTTターミネーション・レギュレータ
  - 出力電圧範囲: 0.5V~0.9V
  - 2Aピークのシンクおよびソース電流
  - 10 $\mu$ FのMLCC出力コンデンサのみが必要
  - $\pm 20$ mV精度
- VTTREFバッファ付きリファレンス
  - VDDQ/2  $\pm 1\%$ 精度
  - 10mAのシンクおよびソース電流
- S3でHigh-Zをサポート、S4およびS5でソフトストップをサポート、S3およびS5入力付き
- 過熱保護
- 10ピン、2mm $\times$ 2mm SON (DSQ)パッケージ

## 2 アプリケーション

- DDR2、DDR3、DDR3L、DDR4メモリの電源
- SSTL\_18、SSTL\_15、SSTL\_135、HSTLのターミネーション
- テレコムおよびデータコム、GSM基地局、LCD-TVおよびPDP-TV、コピー機およびプリンタ、セットトップ・ボックス

## 3 概要

TPS51206デバイスは、シンクおよびソースのダブル・データ・レート(DDR)ターミネーション・レギュレータで、VTTREFバッファ付きリファレンス出力を搭載しています。低入力電圧、低コストで、外付け部品数の少ない、スペースの削減が重要なシステムに特化して設計されています。このデバイスは高速な過渡応答を維持し、1 $\times$ 10 $\mu$ Fのセラミック出力コンデンサしか必要としません。このデバイスはリモート・センシング機能をサポートし、DDR2、DDR3、Low-Power DDR3 (DDR3L)、DDR4 VTTバスのすべての電力要件を満たしています。VTT電流能力は $\pm 2$ Aピークです。このデバイスはDDRのすべての電力状態をサポートし、S3 (RAMへのサスペンド)状態でVTTをHigh-Zへ移行し、S4またはS5 (ディスクへのサスペンド)状態でVTTおよびVTTREFを放電します。

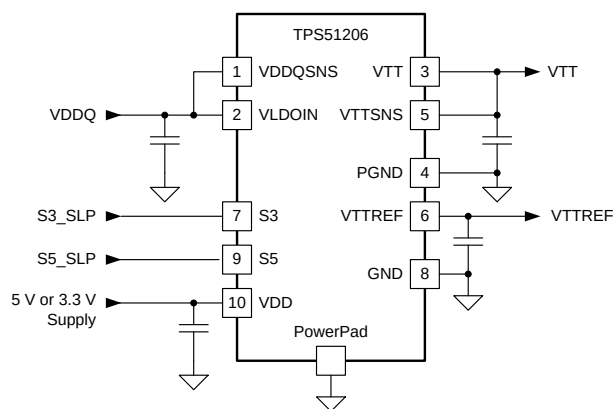
TPS51206デバイスは、10ピン、2mm $\times$ 2mmのSON (DSQ) PowerPAD™パッケージで供給され、-40°C~105°Cで動作が規定されています。

### 製品情報<sup>(1)</sup>

| 型番       | パッケージ    | 本体サイズ(公称)              |
|----------|----------|------------------------|
| TPS51206 | WSO (10) | 2.00mm $\times$ 2.00mm |

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

単純化したアプリケーションの図



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## 4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

### Revision D (March 2018) から Revision E に変更 Page

- 「概要」の「-40°C～85°Cで動作が規定」を「-40°C～105°Cで動作が規定」に変更 ..... [1](#)
- Changed maximum operating temperature from "85 °C" to "105 °C" in *Recommended Operating Conditions* table ..... [4](#)

### Revision C (August 2016) から Revision D に変更 Page

- 追加 VTTREF tolerance at 100  $\mu$ A condition ..... [5](#)

### Revision B (December 2014) から Revision C に変更 Page

- DDR4互換性への言及を 追加 ..... [1](#)
- 追加「[ドキュメントの更新通知を受け取る方法](#)」セクション ..... [19](#)
- 追加「[コミュニティ・リソース](#)」セクション ..... [19](#)

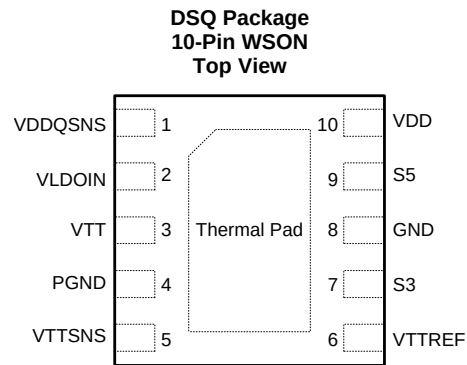
### Revision A (October 2013) から Revision B に変更 Page

- 「ピン構成および機能」セクション、「ESD定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクション 追加 ..... [1](#)

### 2011年UNDEFINED月発行のものから更新 Page

- 追加 minimum and maximum values to the wake up condition of the VDD UVLO threshold voltage specification ..... [5](#)

## 5 Pin Configuration and Functions



### Pin Functions

| PIN         |     | I/O | DESCRIPTION                                                                                                                           |
|-------------|-----|-----|---------------------------------------------------------------------------------------------------------------------------------------|
| NAME        | NO. |     |                                                                                                                                       |
| GND         | 8   | —   | Signal ground                                                                                                                         |
| PGND        | 4   | —   | Power GND for VTT LDO                                                                                                                 |
| S3          | 7   | I   | S3 signal input                                                                                                                       |
| S5          | 9   | I   | S5 signal input                                                                                                                       |
| VDD         | 10  | I   | Device power supply input (3.3 V or 5 V)                                                                                              |
| VDDQSNS     | 1   | I   | VDDQ sense input, reference input for VTTREF                                                                                          |
| VLDOIN      | 2   | I   | Power supply input for VTT/ VTTREF                                                                                                    |
| VTT         | 3   | O   | Power output for VTT LDO, need to connect 10- $\mu$ F or greater MLCC for stability. No maximum limit for VTT output capacitance.     |
| VTTREF      | 6   | O   | VTTREF buffered reference output. Connect to MLCC between 0.22- $\mu$ F and 1- $\mu$ F for stability. The VTTREF pin can not be open. |
| VTTSNS      | 5   | I   | VTT LDO voltage sense input                                                                                                           |
| Thermal Pad |     | —   | Solder to the ground plane for increased thermal performance.                                                                         |

## 6 Specifications

### 6.1 Absolute Maximum Ratings<sup>(1)</sup>

|                                                |                         | MIN  | MAX | UNIT |
|------------------------------------------------|-------------------------|------|-----|------|
| Input voltage <sup>(2)</sup>                   | VDD, S3, S5             | –0.3 | 7   | V    |
|                                                | VLDOIN, VTTSNS, VDDQSNS | –0.3 | 3.6 | V    |
|                                                | PGND                    | –0.3 | 0.3 |      |
| Output voltage <sup>(2)</sup>                  | VTT, VTTREF             | –0.3 | 3.6 |      |
| Operation junction temperature, T <sub>J</sub> |                         | –40  | 150 | °C   |
| Storage temperature, T <sub>stg</sub>          |                         | –55  | 150 | °C   |

- (1) Stresses beyond those listed under [Absolute Maximum Ratings<sup>\(1\)</sup>](#) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Conditions](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the network ground terminal unless otherwise noted.

### 6.2 ESD Ratings

|                    |                         |                                                                                | VALUE | UNIT |
|--------------------|-------------------------|--------------------------------------------------------------------------------|-------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±2000 | V    |
|                    |                         | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±500  |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

|                                                |                         | MIN  | NOM | MAX | UNIT |
|------------------------------------------------|-------------------------|------|-----|-----|------|
| Supply voltage                                 | VDD                     | 3.1  |     | 6.5 | V    |
| Input voltage range <sup>(1)</sup>             | S3, S5                  | –0.1 |     | 6.5 | V    |
|                                                | VLDOIN, VTTSNS, VDDQSNS | –0.1 |     | 3.5 |      |
|                                                | PGND                    | –0.1 |     | 0.1 |      |
| Output voltage range <sup>(1)</sup>            | VTT, VTTREF             | –0.1 |     | 3.5 | V    |
| Operating free-air temperature, T <sub>A</sub> |                         | –40  |     | 105 | °C   |

- (1) All voltage values are with respect to the network ground terminal unless otherwise noted.

### 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | TPS51206   | UNIT |
|-------------------------------|----------------------------------------------|------------|------|
|                               |                                              | DSQ (WSON) |      |
|                               |                                              | 10 PINS    |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 70.3       | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 46.3       |      |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 33.8       |      |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 2.9        |      |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 33.5       |      |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | 16.3       |      |

- (1) 従来および新しい熱測定値の詳細については、『Semiconductor and IC Package Thermal Metrics』アプリケーション・レポート (SPRA953)を参照してください。

## 6.5 Electrical Characteristics

Over operating free-air temperature range,  $V_{DD} = 5\text{ V}$ , VLDOIN is connected to VDDQSNS,  $V_{S3} = V_{S5} = 5\text{ V}$  (unless otherwise noted)

| PARAMETER                          |                                             | TEST CONDITION                                                                                                   | MIN             | TYP  | MAX    | UNIT             |
|------------------------------------|---------------------------------------------|------------------------------------------------------------------------------------------------------------------|-----------------|------|--------|------------------|
| <b>SUPPLY CURRENT</b>              |                                             |                                                                                                                  |                 |      |        |                  |
| $I_{VDD(S0)}$                      | VDD supply current, in S0                   | $T_A = 25^\circ\text{C}$ , No load, $V_{S3} = V_{S5} = 5\text{ V}$ , $V_{VDDQSNS} = 1.8\text{ V}$                |                 | 170  |        | $\mu\text{A}$    |
| $I_{VDD(S3)}$                      | VDD supply current, in S3                   | $T_A = 25^\circ\text{C}$ , No load, $V_{S3} = 0\text{ V}$ , $V_{S5} = 5\text{ V}$ , $V_{VDDQSNS} = 1.8\text{ V}$ |                 | 80   |        | $\mu\text{A}$    |
| $I_{VDDSDN}$                       | VDD shutdown current, in S4 and S5          | $T_A = 25^\circ\text{C}$ , No load, $V_{S3} = V_{S5} = 0\text{ V}$ , $V_{VDDQSNS} = 1.8\text{ V}$                |                 |      | 1      | $\mu\text{A}$    |
| $I_{VLDOIN(S0)}$                   | VLDOIN supply current, in S0                | $T_A = 25^\circ\text{C}$ , No load, $V_{S3} = V_{S5} = 5\text{ V}$ , $V_{LDION} = 1.8\text{ V}$                  |                 |      | 5      | $\mu\text{A}$    |
| $I_{VLDOIN(S3)}$                   | VLDOIN supply current, in S3                | $T_A = 25^\circ\text{C}$ , No load, $V_{S3} = 0\text{ V}$ , $V_{S5} = 5\text{ V}$ , $V_{LDION} = 1.8\text{ V}$   |                 |      | 5      | $\mu\text{A}$    |
| $I_{VLDOINSDN}$                    | VLDOIN shutdown current, in S4 and S5       | $T_A = 25^\circ\text{C}$ , No load, $V_{S3} = V_{S5} = 0\text{ V}$ , $V_{LDION} = 1.8\text{ V}$                  |                 |      | 5      | $\mu\text{A}$    |
| <b>VTTREF OUTPUT</b>               |                                             |                                                                                                                  |                 |      |        |                  |
| $V_{VTTREF}$                       | Output voltage                              |                                                                                                                  | $V_{VDDQSNS}/2$ |      |        | V                |
| $V_{VTTREFTOL}$                    | Output voltage tolerance to $V_{VDDQSNS}$   | $ I_{VTTREF}  \leq 10\text{ mA}$ , $1.5\text{ V} \leq V_{VDDQSNS} \leq 1.8\text{ V}$                             | 49%             |      | 51%    |                  |
|                                    |                                             | $ I_{VTTREF}  \leq 10\text{ mA}$ , $1.2\text{ V} \leq V_{VDDQSNS} < 1.5\text{ V}$                                | 48.75%          |      | 51.25% |                  |
|                                    |                                             | $ I_{VTTREF}  \leq 100\text{ }\mu\text{A}$ , $1.2\text{ V} \leq V_{VDDQSNS} \leq 1.8\text{ V}$                   | 49%             |      | 51%    |                  |
| $I_{VTTREFSRC}$                    | Source current                              | $V_{VDDQSNS} = 1.8\text{ V}$ , $V_{VTTREF} = 0\text{ V}$                                                         | 10              |      |        | mA               |
| $I_{VTTREFSNK}$                    | Sink current                                | $V_{VDDQSNS} = 0\text{ V}$ , $V_{VTTREF} = 1.8\text{ V}$                                                         | 10              |      |        | mA               |
| $I_{VTTREFDIS}$                    | VTTREF Discharge current                    | $T_A = 25^\circ\text{C}$ , $V_{S3} = V_{S5} = 0\text{ V}$ , $V_{VTTREF} = 0.5\text{ V}$                          |                 | 1.3  |        | mA               |
| <b>VTT OUTPUT</b>                  |                                             |                                                                                                                  |                 |      |        |                  |
| $V_{VTT}$                          | Output voltage                              |                                                                                                                  | $V_{VDDQSNS}/2$ |      |        | V                |
| $V_{VTTTOL}$                       | Output voltage tolerance to $V_{VDDQSNS}/2$ | $ I_{VTT}  \leq 10\text{ mA}$ , $1.4\text{ V} \leq V_{VDDQSNS} \leq 1.8\text{ V}$                                | -20             |      | 20     | mV               |
|                                    |                                             | $ I_{VTT}  < 1\text{ A}$ , $1.4\text{ V} \leq V_{VDDQSNS} \leq 1.8\text{ V}^{(1)}$                               | -30             |      | 30     |                  |
|                                    |                                             | $ I_{VTT}  < 2\text{ A}$ , $1.4\text{ V} \leq V_{VDDQSNS} \leq 1.8\text{ V}^{(1)}$                               | -40             |      | 40     |                  |
|                                    |                                             | $ I_{VTT}  \leq 10\text{ mA}$ , $1.2\text{ V} \leq V_{VDDQSNS} \leq 1.4\text{ V}$                                | -20             |      | 20     |                  |
|                                    |                                             | $ I_{VTT}  < 1\text{ A}$ , $1.2\text{ V} \leq V_{VDDQSNS} \leq 1.4\text{ V}^{(1)}$                               | -30             |      | 30     |                  |
|                                    |                                             | $ I_{VTT}  < 1.5\text{ A}$ , $1.2\text{ V} \leq V_{VDDQSNS} < 1.4\text{ V}^{(1)}$                                | -40             |      | 40     |                  |
| $I_{VTTCLSRC}$                     | Source current limit                        | $V_{VDDQSNS} = 1.8\text{ V}$ , $V_{VTT} = V_{VTTNS} = 0.7\text{ V}$                                              | 2               |      |        | A                |
| $I_{VTTCLSNK}$                     | Sink current limit                          | $V_{VDDQSNS} = 1.8\text{ V}$ , $V_{VTT} = V_{VTTNS} = 1.1\text{ V}$                                              | 2               |      |        | A                |
| $I_{VTTLK}$                        | Leakage current                             | $T_A = 25^\circ\text{C}$ , $V_{S3} = 0\text{ V}$ , $V_{S5} = 5\text{ V}$ , $V_{VTT} = V_{VTTREF}$                |                 |      | 5      | $\mu\text{A}$    |
| $I_{VTTNSBIAS}$                    | VTTNS input bias current                    | $V_{S3} = 5\text{ V}$ , $V_{S5} = 5\text{ V}$ , $V_{VTTNS} = V_{VTTREF}$                                         | -0.1            |      | 0.1    | $\mu\text{A}$    |
| $I_{VTTNSLK}$                      | VTTNS leakage current                       | $V_{S3} = 0\text{ V}$ , $V_{S5} = 5\text{ V}$ , $V_{VTTNS} = V_{VTTREF}$                                         | -0.1            |      | 0.1    | $\mu\text{A}$    |
| $I_{VTTDIS}$                       | VTT Discharge current                       | $T_A = 25^\circ\text{C}$ , $V_{S3} = V_{S5} = V_{VDDQSNS} = 0\text{ V}$ , $V_{VTT} = 0.5\text{ V}$               |                 | 7    |        | mA               |
| <b>VDDQ INPUT</b>                  |                                             |                                                                                                                  |                 |      |        |                  |
| $I_{VDDQSNS}$                      | VDDQSNS input current                       | $V_{VDDQSNS} = 1.8\text{ V}$                                                                                     |                 | 30   |        | $\mu\text{A}$    |
| <b>UVLO/LOGIC THRESHOLD</b>        |                                             |                                                                                                                  |                 |      |        |                  |
| $V_{VDDUV}$                        | VDD UVLO threshold voltage                  | Wake up                                                                                                          | 2.67            | 2.90 | 3.00   | V                |
|                                    |                                             | Hysteresis                                                                                                       |                 | 0.2  |        |                  |
| $V_{LL}$                           | S3 and S5 low-level voltage                 |                                                                                                                  |                 |      | 0.5    | V                |
| $V_{LH}$                           | S3 and S5 high-level voltage                |                                                                                                                  | 1.8             |      |        | V                |
| $V_{LHYS}$                         | S3 and S5 hysteresis voltage                |                                                                                                                  |                 | 0.3  |        | V                |
| $I_{LHLK}$                         | S3 and S5 input leak current                |                                                                                                                  | -1              |      | 1      | $\mu\text{A}$    |
| <b>OVER-TEMPERATURE PROTECTION</b> |                                             |                                                                                                                  |                 |      |        |                  |
| $T_{OTP}$                          | Over temperature protection                 | Shutdown temperature <sup>(1)</sup>                                                                              |                 | 150  |        | $^\circ\text{C}$ |
|                                    |                                             | Hysteresis <sup>(1)</sup>                                                                                        |                 | 10   |        |                  |

(1) Ensured by design. Not production tested.

## 6.6 Typical Characteristics

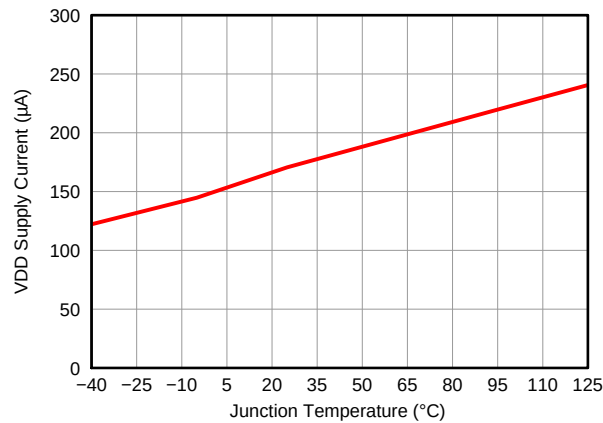


图 1. VDD Supply Current vs. Junction Temperature

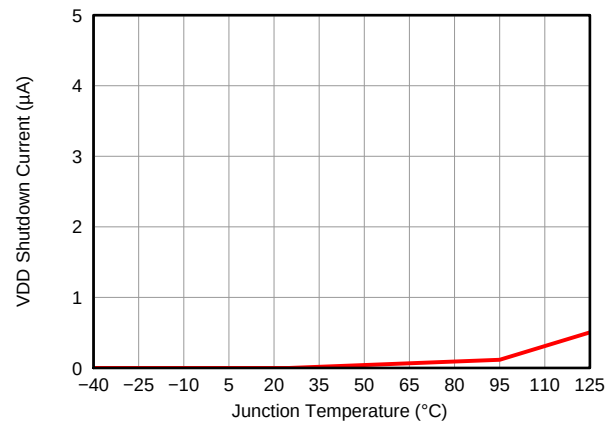


图 2. VDD Shutdown Current vs. Junction Temperature

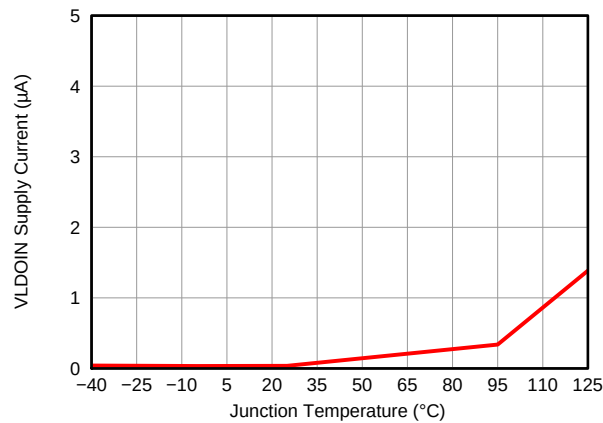


图 3. VLDOIN Supply Current vs. Junction Temperature

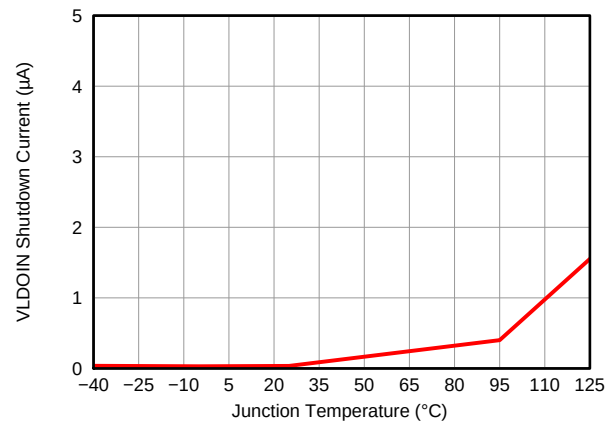


图 4. VLDOIN Shutdown Current vs. Junction Temperature

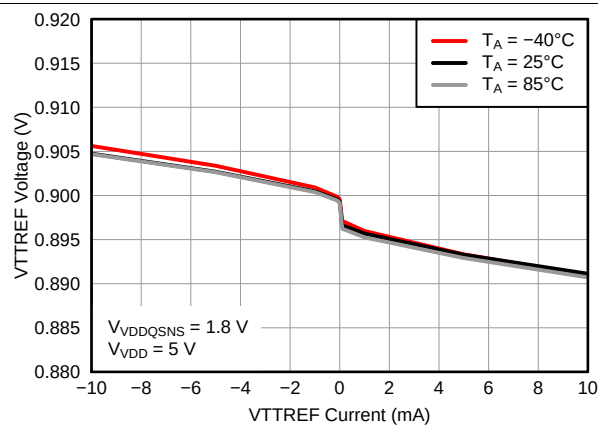


图 5. VTTREF Load Regulation (0.9 V)

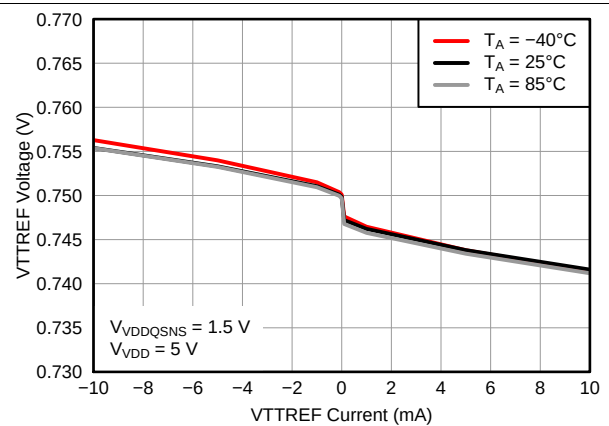


图 6. VTTREF Load Regulation (0.75 V)

## Typical Characteristics (continued)

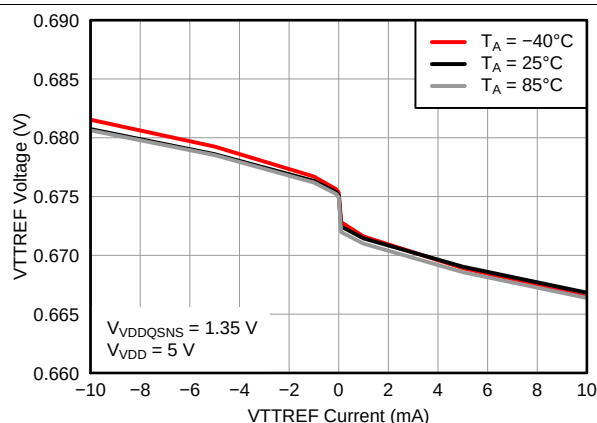


图 7. VTTREF Load Regulation (0.675 V)

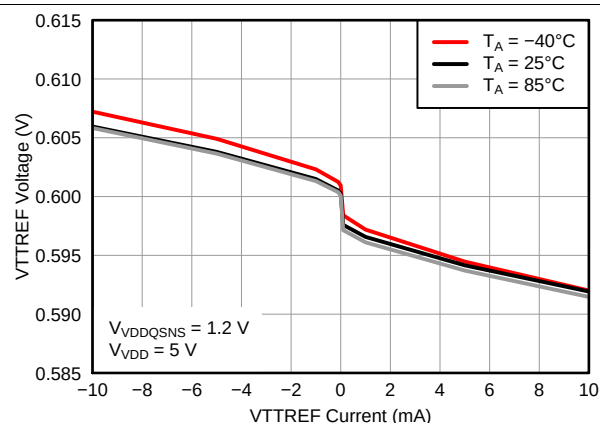


图 8. VTTREF Load Regulation (0.6 V)

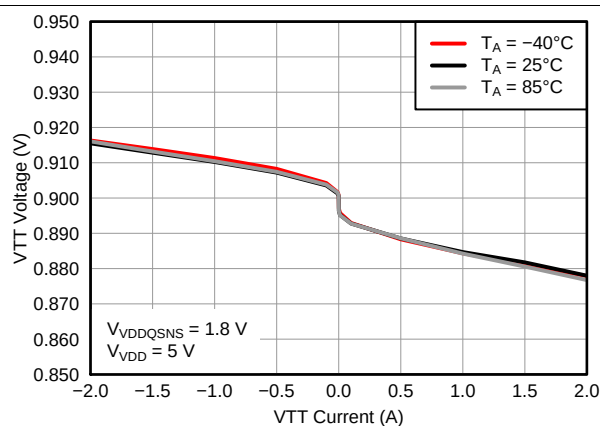


图 9. VTT Load Regulation (0.9 V)

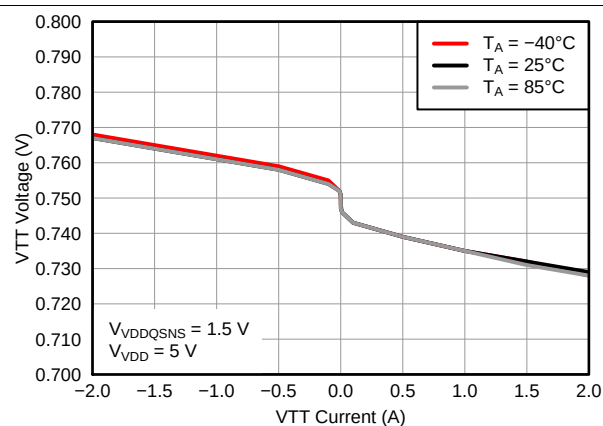


图 10. VTT Load Regulation (0.75 V)

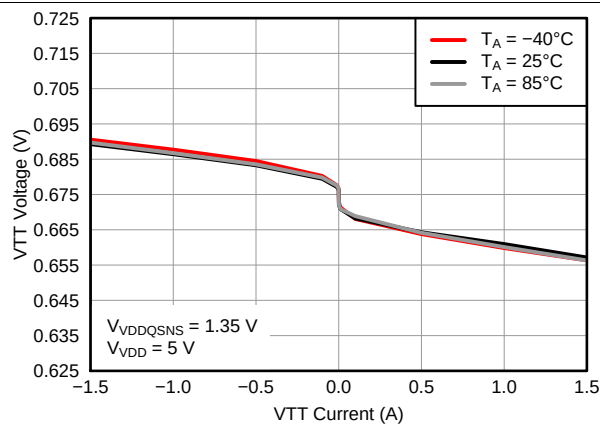


图 11. VTT Load Regulation (0.675 V)

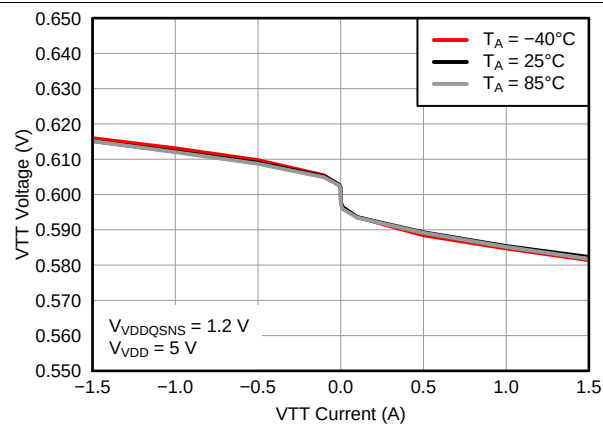


图 12. VTT Load Regulation (0.6 V)

## Typical Characteristics (continued)

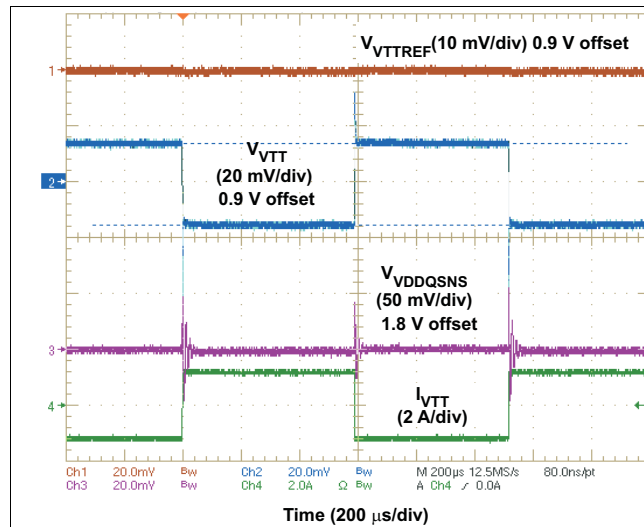


FIG 13. VTT Load Transient Response (0.9 V)

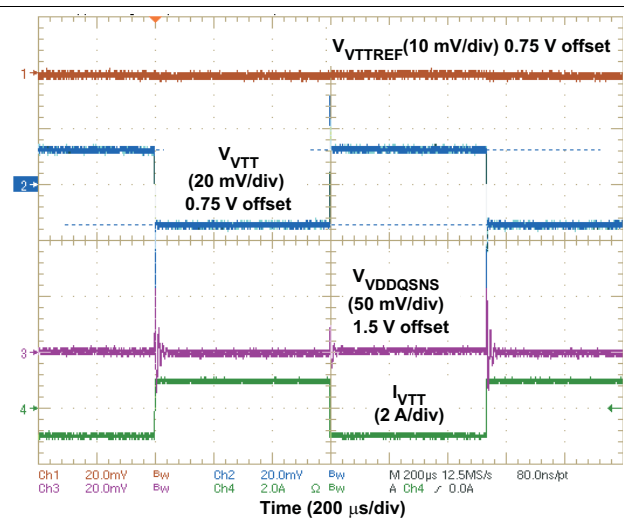


FIG 14. VTT Load Transient Response (0.75 V)

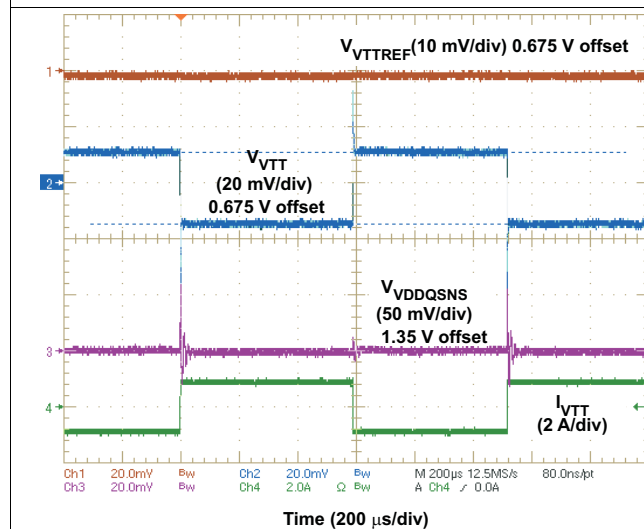


FIG 15. VTT Load Transient Response (0.675 V)

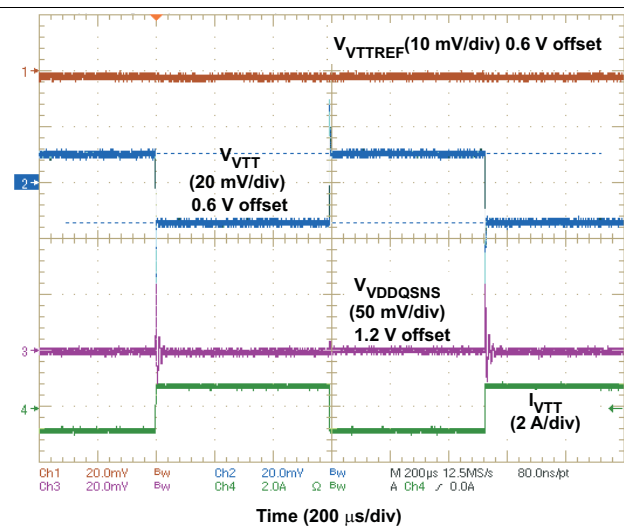


FIG 16. VTT Load Transient Response (0.6 V)

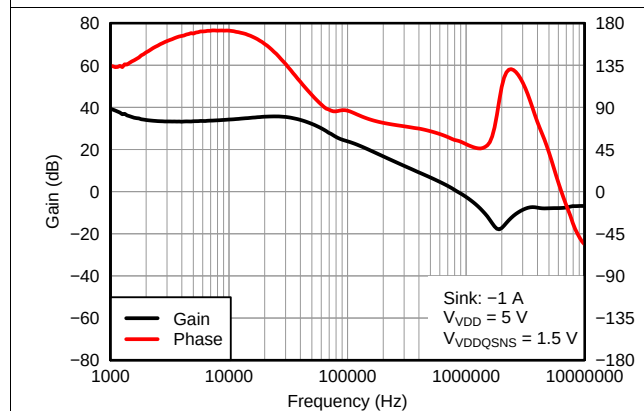


FIG 17. VTT (Sink: -1 A) Bode Plot (0.75 V)

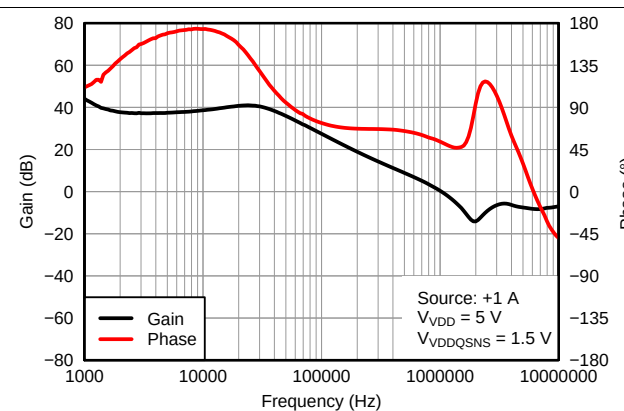


FIG 18. VTT (Source: +1 A) Bode Plot (0.75 V)



## Typical Characteristics (continued)

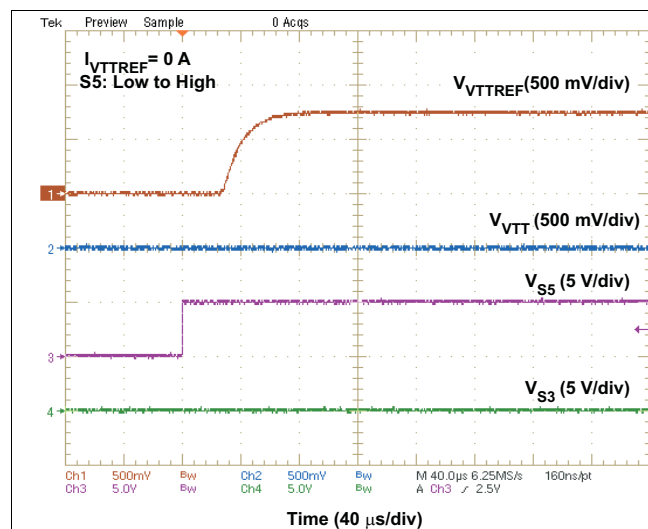


Figure 19. Start-Up Waveforms (S5: Low to High)

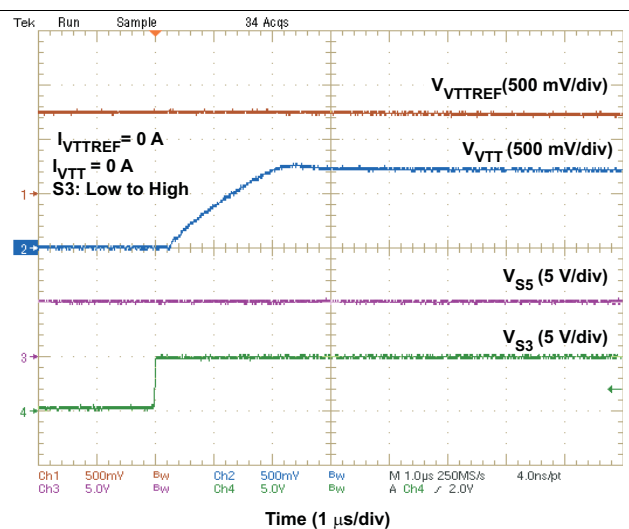


Figure 20. Start-Up Waveforms (S3: Low to High)

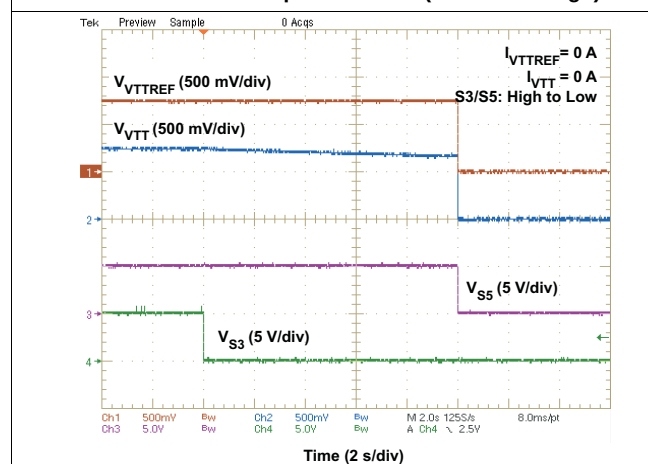


Figure 21. Shutdown Waveforms (S3/ S5: High to Low)

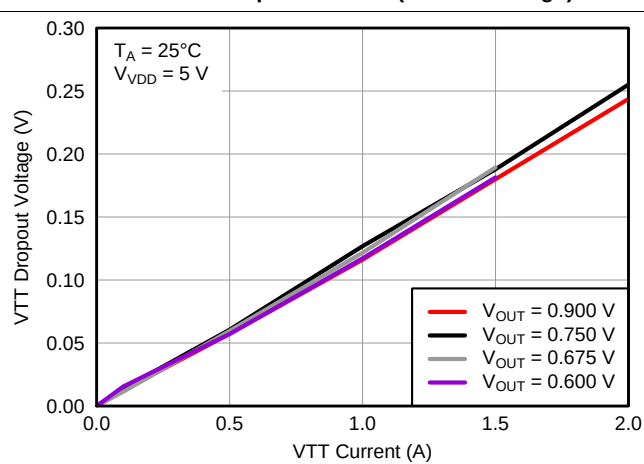


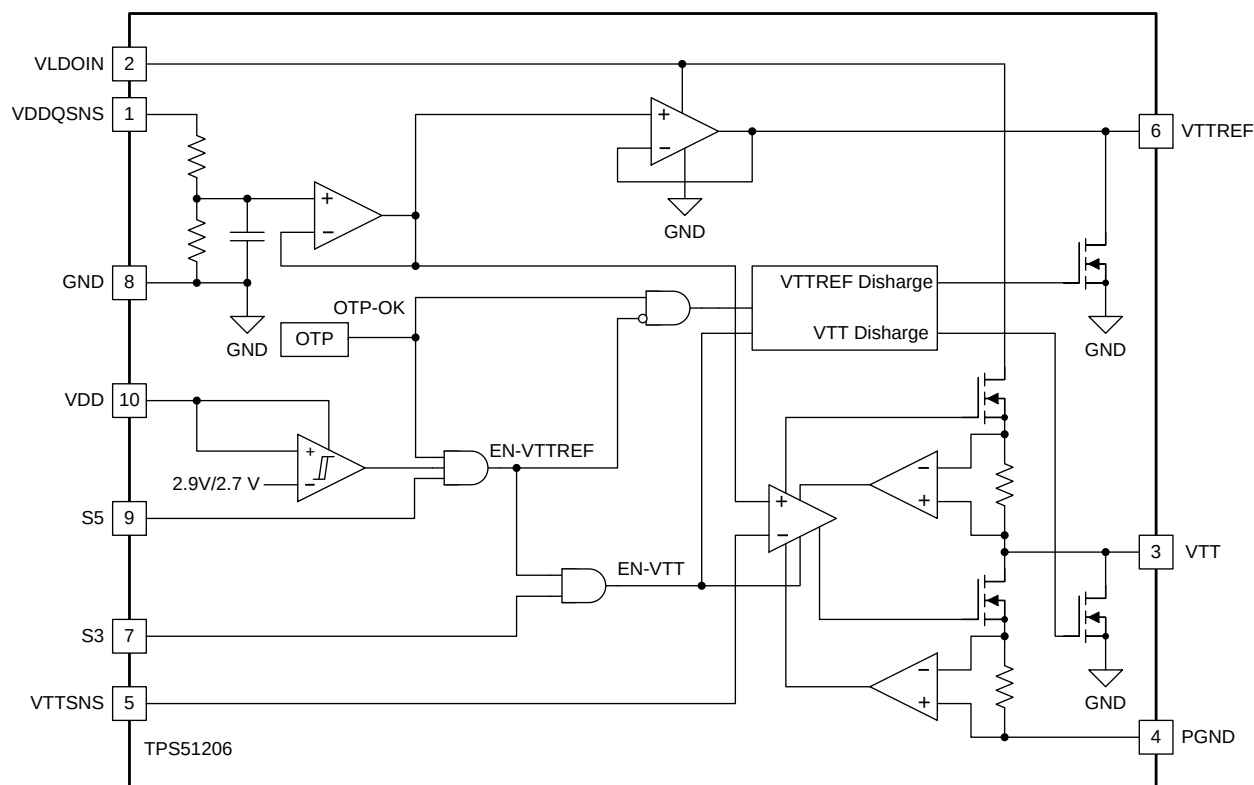
Figure 22. VTT Dropout Voltage

## 7 Detailed Description

### 7.1 Overview

The TPS51206 device is a sink or source double data rate (DDR) termination regulator with VTTREF buffered reference output.

### 7.2 Functional Block Diagram



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### 7.3 Feature Description

#### 7.3.1 VTT Sink and Source Regulator

The TPS51206 device is a sink or source tracking termination regulator specifically designed for low input voltage, low cost, and low external component count systems where space is a key application parameter. The device integrates a high-performance, low-dropout (LDO) linear regulator (VTT) that has ultimate fast response to track  $\frac{1}{2}$  VDDQSNS within 40 mV at all conditions, and its current capability is 2 A for both sink and source directions. A 10- $\mu$ F (or greater) ceramic capacitor(s) need to be attached close to the VTT terminal for stable operation. A grade of X5R or better is recommended. To achieve tight regulation with minimum effect of trace resistance, the remote sensing terminal, VTTSNS, should be connected to the positive terminal of the output capacitor(s) as a separate trace from the high current path from the VTT pin.

The device has a dedicated pin, VLDOIN, for VTT power supply to minimize the LDO power dissipation on user application. The minimum VLDOIN voltage is 0.4 V above the  $\frac{1}{2}$  VDDQSNS voltage.

#### 7.3.2 VTTREF

The VTTREF pin includes 10 mA of sink or source current capability, and tracks  $\frac{1}{2}$  of VDDQSNS with  $\pm 1\%$  accuracy. The VTTREF pin can not be open. A 0.22- $\mu$ F ceramic capacitor needs to be attached close to the VTTREF terminal for stable operation; X5R or better grade is recommended.

## Feature Description (continued)

### 7.3.3 VDD Undervoltage Lockout Protection

The TPS51206 device input voltage (VDD) includes undervoltage lockout protection (UVLO). When the VDD pin voltage is lower than UVLO threshold voltage, VTT and VTTREF are shut off. This is non-latch protection.

### 7.3.4 VTT Current Limit

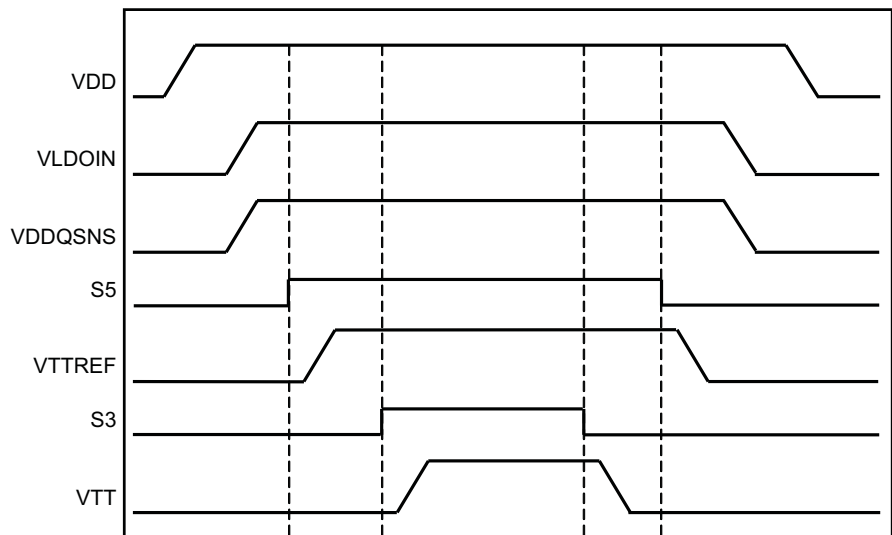
The TPS51206 device has VTT sink and source current limit capability. When the VTT current is higher than 2 A, the current is limited and VTT voltage is out of regulation. When the current is below 2 A, the VTT voltage is in regulation. This is non-latch protection.

### 7.3.5 Overtemperature Protection

This device features internal temperature monitoring. If the temperature exceeds the threshold value, VTT and VTTREF are shut off. This is a non-latch protection.

### 7.3.6 Power On and Off Sequence

Figure 23 is the recommended power on and off sequence. During power on, it is allowed to turn on VDD, S3 and S5 first, then turn on VLDOIN and VDDQSNS. During power off, it is allowed to turn off VDD, S3 and S5 first, then turn off VLDOIN and VDDQSNS.



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Figure 23. Typical Timing Diagram

## 7.4 Device Functional Modes

### 7.4.1 Power State Control

The TPS51206 device has two input pins, S3 and S5, to provide simple control of the power state. 表 1 describes S3 and S5 terminal logic state and corresponding state of VTTREF and VTT outputs. VTT is turn-off and placed to high impedance (High-Z) state in S3. The VTT output is floated and does not sink or source current in this state. When both S5 and S3 pins are LOW, the power state is set to S4 and S5. In S4 and S5 state, all the outputs are turn-off and discharged to GND.

**表 1. S3 and S5 Control Table**

| STATE     | S3 | S5 | VTTREF         | VTT            |
|-----------|----|----|----------------|----------------|
| S0        | HI | HI | ON             | ON             |
| S3        | LO | HI | ON             | OFF(High-Z)    |
| S4 and S5 | LO | LO | OFF(Discharge) | OFF(Discharge) |

## 8 Application and Implementation

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

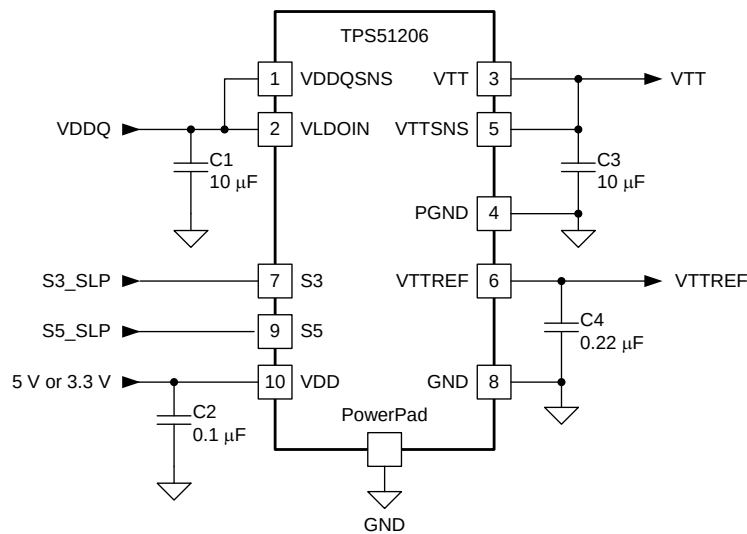
### 8.1 Application Information

The TPS51206 device is typically used as a sink and source tracking termination regulator which converts a voltage from VTT+0.4 V to 3.5 V

### 8.2 Typical Applications

#### 8.2.1 VLDOIN = VDDQ Configuration

Figure 24 shows an application diagram for a configuration where VLDOIN and VDDQ are connected.



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Figure 24. VLDOIN = VDDQ Configuration

#### 8.2.1.1 Design Requirements

Table 2. Design Parameters

| PARAMETER            | EXAMPLE VALUE |
|----------------------|---------------|
| Supply Voltage (VDD) | 3.3 V or 5 V  |
| VLDOIN = VDDQ        | 1.5 V         |
| Output Current       | ±2 A          |

### 8.2.1.2 Detailed Design Procedure

表 3. VLDOIN = VDDQ Configuration Components

| REFERENCE DESIGNATOR | SPECIFICATION                         | MANUFACTURER | PART NUMBER   |
|----------------------|---------------------------------------|--------------|---------------|
| C1, C3               | 10 $\mu$ F, 6.3 V, X5R, 1608 (0603)   | Taiyo Yuden  | JMK107BJ106MA |
| C2                   | 0.1 $\mu$ F, 6.3 V, X5R, 1005 (0402)  | Taiyo Yuden  | JWK105BJ104MP |
| C4                   | 0.22 $\mu$ F, 6.3 V, X5R, 1005 (0402) | Taiyo Yuden  | JMK105BJ224KV |

#### 8.2.1.2.1 VDD Capacitor

Add a ceramic capacitor, with a value 0.1  $\mu$ F (or greater) and X5R grade (or better), placed close to the VDD terminal, to stabilize the bias supply voltage from any parasitic impedance from the power supply rail.

#### 8.2.1.2.2 VLDOIN Capacitor

Depending on the trace impedance between the VLDOIN bulk power supply to the device, a transient increase of source current is supplied mostly by the charge from the VLDOIN input capacitor. Use a 10- $\mu$ F (or greater) and X5R grade (or better) ceramic capacitor to supply this transient charge.

#### 8.2.1.2.3 VTTREF Capacitor

Add a ceramic capacitor, with a value 0.22  $\mu$ F and X5R grade (or better), placed close to the VTTREF terminal for stable operation.

#### 8.2.1.2.4 VTT Capacitor

For stable operation, a 10- $\mu$ F (or greater) and X5R (or better) grade ceramic capacitor(s) need to be attached close to the VTT terminal. This capacitor is recommended to minimize any additional equivalent series resistance (ESR) and/or equivalent series inductance (ESL) of ground trace between the PGND terminal and the VTT capacitor(s).

#### 8.2.1.2.5 VTTSNS Connection

To achieve tight regulation with minimum effect of trace resistance, a remote sensing terminal, the VTTSNS pin should be connected to the positive terminal of the VTT pin output capacitor(s) as a separate trace from the high-current path from VTT. Consider adding a low-pass R-C filter at the VTTSNS pin in case the ESR of the VTT output capacitor(s) is larger than 2 m $\Omega$ . The R-C filter time constant should be approximately the same or slightly lower than the time constant of the VTT output capacitance and ESR.

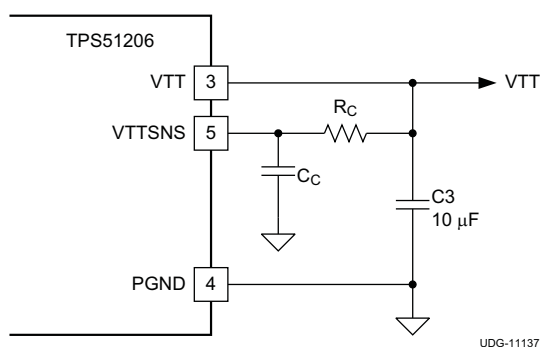
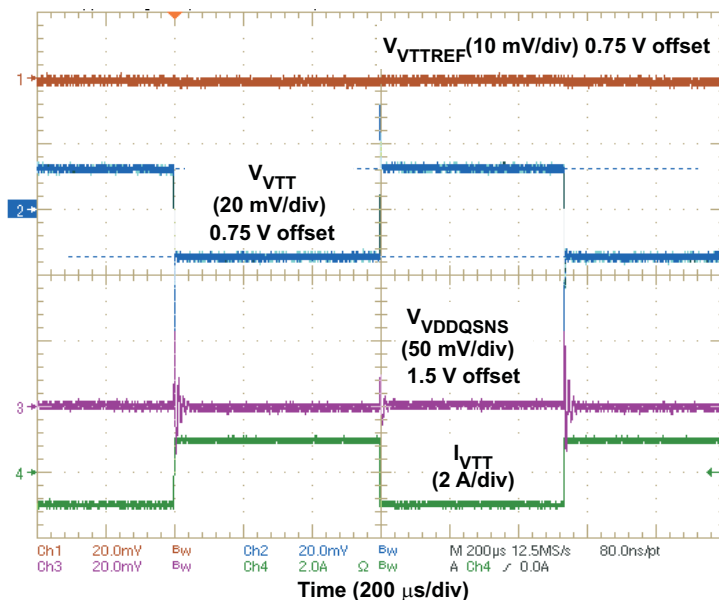


图 25. R-C Filter for VTTSNS

#### 8.2.1.2.6 VDDQSNS Connection

VDDQSNS is a reference input of the VTTREF and VTT. Trace should be routed away from noise-generating lines.

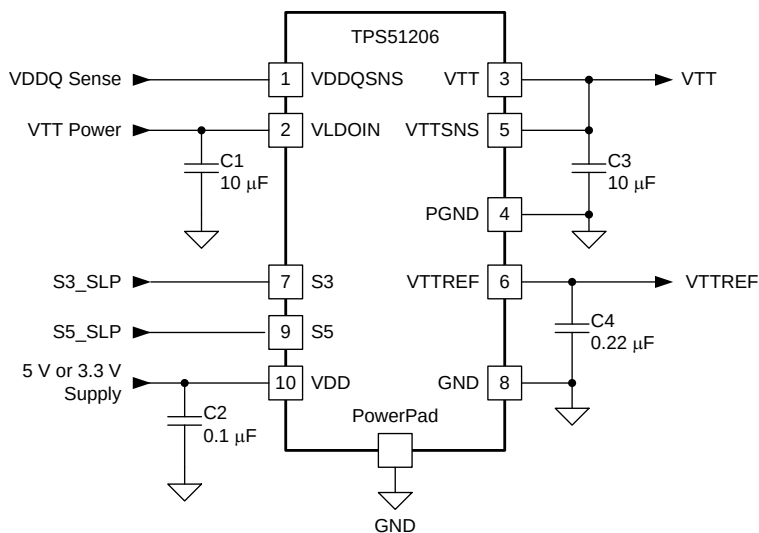
### 8.2.1.3 Application Curves



✎ 26. VTT Load Transient Response (0.75 V)

### 8.2.2 VLDOIN Separated from VDDQ Configuration

✎ 27 shows an application diagram for a configuration where VLDOIN and VDDQ are separated.



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✎ 27. VLDOIN Separated from VDDQ Configuration

### 8.2.2.1 Design Requirements

表 4. Design Parameters

| PARAMETER            | EXAMPLE VALUE |
|----------------------|---------------|
| Supply Voltage (VDD) | 3.3 V or 5 V  |
| VLDOIN = VDDQ        | 1.5 V         |
| Output Current       | ±2 A          |

### 8.2.2.2 Detailed Design Procedure

表 5. VLDOIN Separated from VDDQ Configuration Components

| REFERENCE DESIGNATOR | SPECIFICATION                        | MANUFACTURER | PART NUMBER   |
|----------------------|--------------------------------------|--------------|---------------|
| C1, C3               | 10 $\mu$ F, 6.3V, X5R, 1608 (0603)   | Taiyo Yuden  | JMK107BJ106MA |
| C2                   | 0.1 $\mu$ F, 6.3V, X5R, 1005 (0402)  | Taiyo Yuden  | JWK105BJ104MP |
| C3                   | 10 $\mu$ F, 6.3V, X5R, 1608 (0603)   | Taiyo Yuden  | JMK107BJ106MA |
| C4                   | 0.22 $\mu$ F, 6.3V, X5R, 1005 (0402) | Taiyo Yuden  | JMK105BJ224KV |

### 8.2.2.3 Application Curves

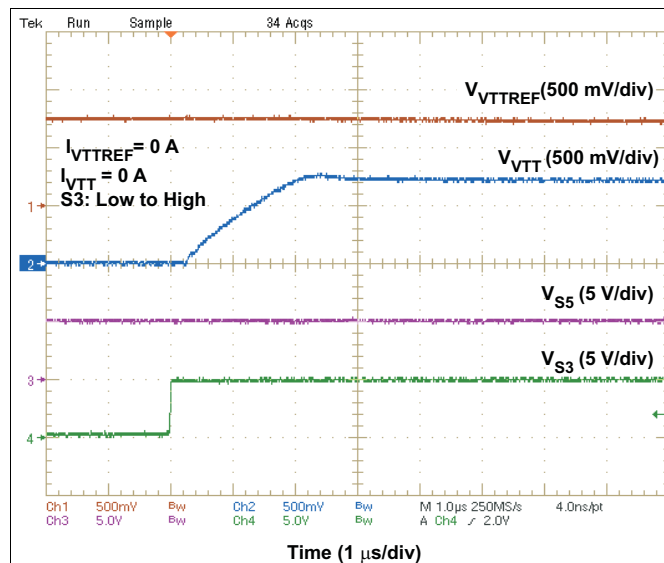


图 28. Start-Up Waveforms (S3: Low to High)

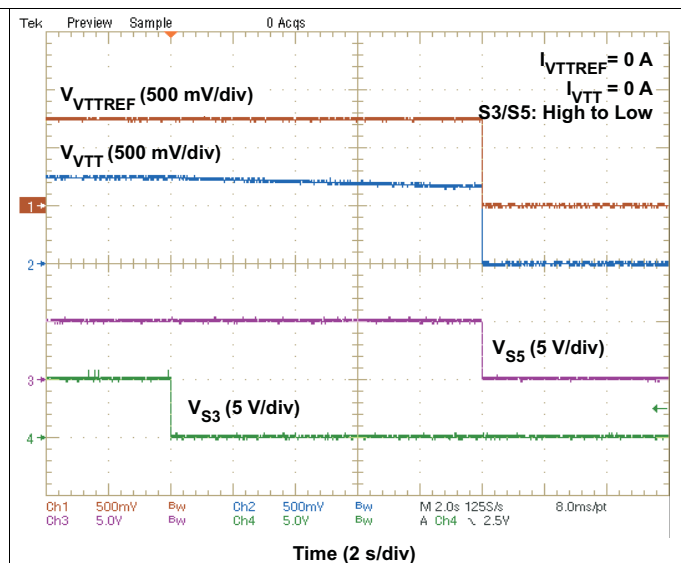


图 29. Shutdown Waveforms (S3 / S5: High to Low)



## 9 Power Supply Recommendations

TPS51206 device is designed for a sink / source double data rate (DDR) termination regulator with VTTREF buffered reference output. Supply input voltage (VDD) supports 3.3-V rail and 5-V rail; VLDOIN input voltage supports VTT+0.4 V to 3.5 V.

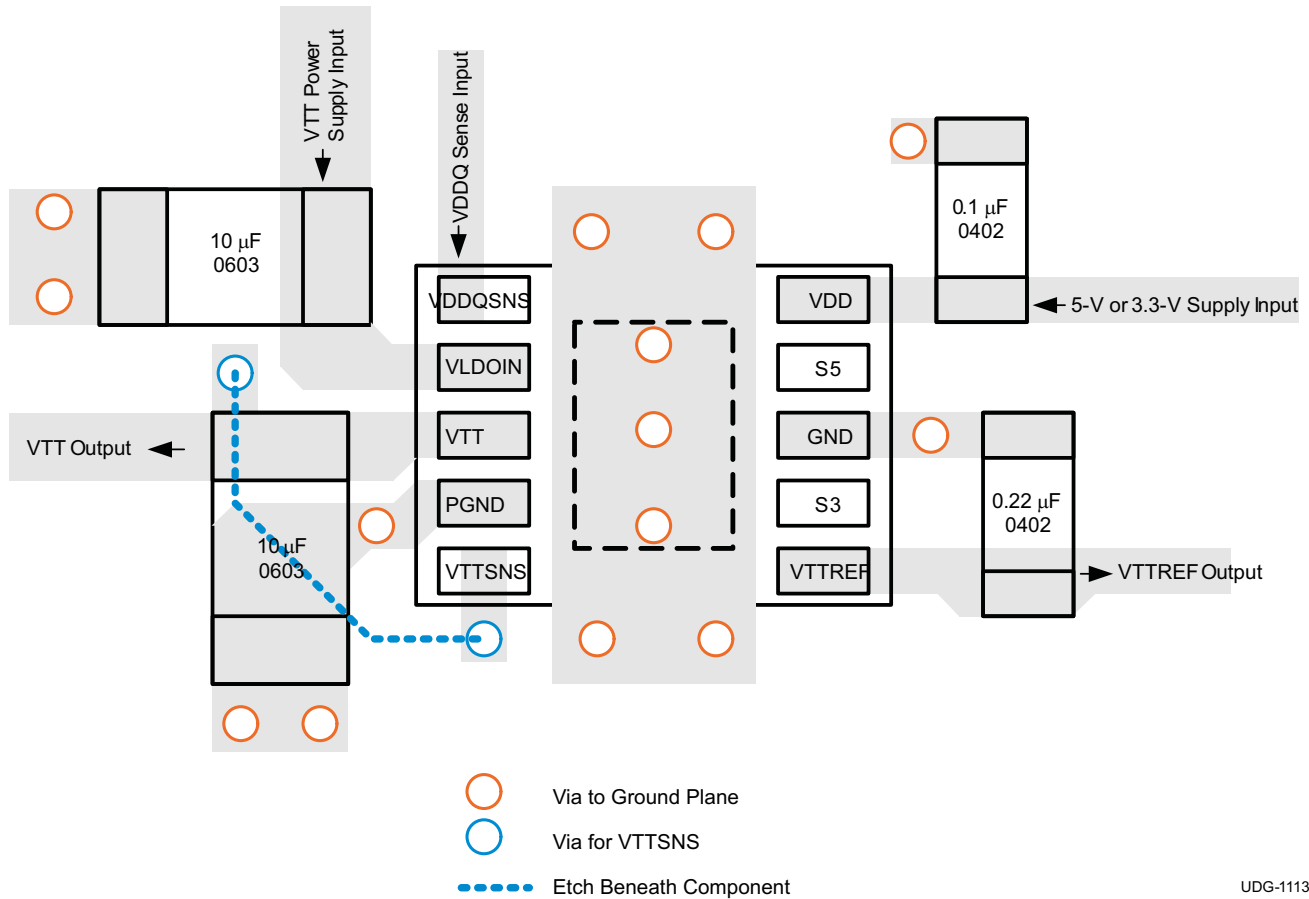
## 10 Layout

### 10.1 Layout Guidelines

Consider the following before beginning a TPS51206 device layout design.

- The input bypass capacitor for VLDOIN should be placed as close as possible to the terminal with short and wide connections.
- The output capacitor for VTT should be placed close to the terminals (VTT and PGND) with short and wide connection in order to avoid additional ESR and/or ESL trace inductance.
- VTTSNS should be connected to the positive node of VTT output capacitor(s) as a separate trace from the high current VTT power trace. In addition, VTTSNS trace should be routed away from high current trace, on the separate layer is recommended. This configuration is strongly recommended to avoid additional ESR and/or ESL. If sensing the voltage at the point of the load is required, it is recommended to attach the output capacitor(s) at that point. In addition, it is recommended to minimize any additional ESR and/or ESL of ground trace between the GND pin and the VTT capacitor(s).
- The GND pin (and the negative node of the VTTREF output capacitor) and PGND pins (and the negative node of the VTT output capacitor) should be connected to the internal system ground planes (for better result, use at least two internal ground planes) with multiple vias. Use as many vias as possible to reduce the impedance between GND pin or PGND pin and the system ground plane.
- In order to effectively remove heat from the package, properly prepare the thermal land. Apply solder directly to the package thermal pad. The wide traces of the component and the side copper connected to the thermal land pad help to dissipate heat. Numerous vias 0.33 mm in diameter connected from the thermal land to the internal/solder side ground plane(s) should also be used to help dissipation. Consult the [TPS51206-EVM User's Guide](#) for more detailed layout recommendations.

## 10.2 Layout Example



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**图 30. PCB Layout Guideline**

## 10.3 Thermal Considerations

Because the TPS51206 device is a linear regulator, the VTT current flows in both source and sink directions, thereby dissipating power from the device. When the device is sourcing current, the voltage difference between  $V_{VLDOIN}$  and  $V_{VTT}$  times  $I_{VTT}$  (VTT current) current becomes the power dissipation as shown in 式 1.

$$P_{DISS(src)} = (V_{VLDOIN} - V_{VTT}) \times I_{VTT(src)} \quad (1)$$

In this case, if the VLDOIN pin is connected to an alternative power supply lower than the VDDQ voltage, overall power loss can be reduced. For the sink phase, VTT voltage is applied across the internal LDO regulator, and the power dissipation can be calculated by 式 2.

$$P_{DISS(snk)} = V_{VTT} \times I_{VTT(snk)} \quad (2)$$

Maximum power dissipation allowed by the package is calculated by 式 3.

$$P_{PKG} = \frac{T_{J(max)} - T_{A(max)}}{\theta_{JA}}$$

where

- $T_{J(max)}$  is 125°C
  - $T_{A(max)}$  is the maximum ambient temperature in the system
  - $\theta_{JA}$  is the thermal resistance from junction to ambient
- (3)

## 11 デバイスおよびドキュメントのサポート

### 11.1 デバイス・サポート

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### 11.3 コミュニティ・リソース

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### 11.6 Glossary

[SLYZ022](#) — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

## 12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

## PACKAGING INFORMATION

| Orderable part number        | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">TPS51206DSQR</a> | Active        | Production           | WSO (DSQ)   10 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 105   | 1206                |
| TPS51206DSQR.B               | Active        | Production           | WSO (DSQ)   10 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 105   | 1206                |
| TPS51206DSQRG4               | Active        | Production           | WSO (DSQ)   10 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 105   | 1206                |
| TPS51206DSQRG4.B             | Active        | Production           | WSO (DSQ)   10 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 105   | 1206                |
| <a href="#">TPS51206DSQT</a> | Active        | Production           | WSO (DSQ)   10 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 105   | 1206                |
| TPS51206DSQT.B               | Active        | Production           | WSO (DSQ)   10 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 105   | 1206                |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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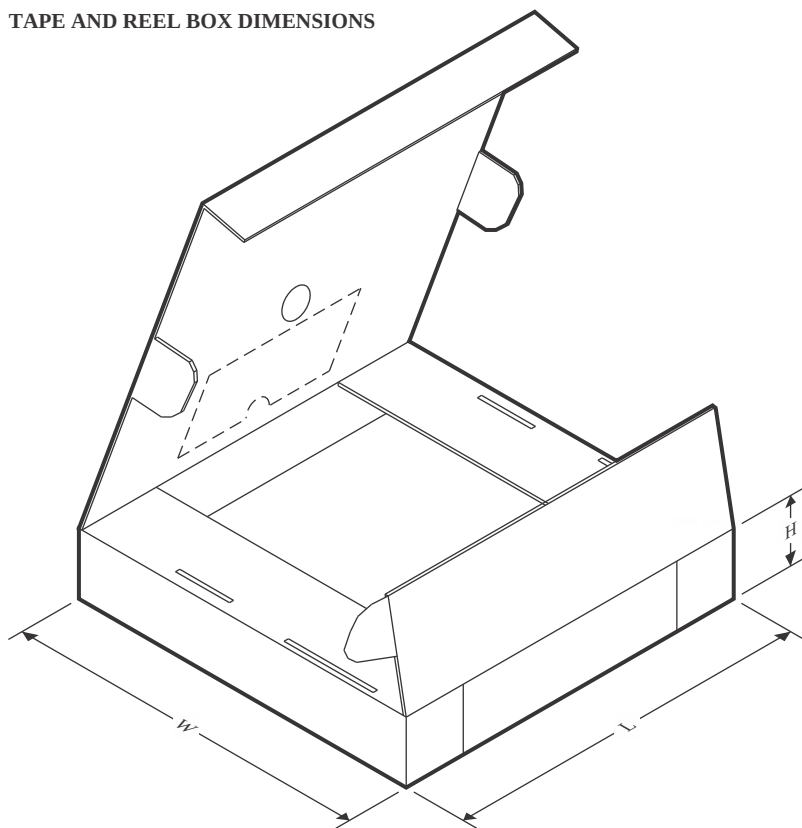
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS51206DSQR   | WSO          | DSQ             | 10   | 3000 | 180.0              | 8.4                | 2.3     | 2.3     | 1.15    | 4.0     | 8.0    | Q2            |
| TPS51206DSQRG4 | WSO          | DSQ             | 10   | 3000 | 180.0              | 8.4                | 2.3     | 2.3     | 1.15    | 4.0     | 8.0    | Q2            |
| TPS51206DSQT   | WSO          | DSQ             | 10   | 250  | 180.0              | 8.4                | 2.3     | 2.3     | 1.15    | 4.0     | 8.0    | Q2            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS51206DSQR   | WSN          | DSQ             | 10   | 3000 | 213.0       | 191.0      | 35.0        |
| TPS51206DSQRG4 | WSN          | DSQ             | 10   | 3000 | 210.0       | 185.0      | 35.0        |
| TPS51206DSQT   | WSN          | DSQ             | 10   | 250  | 210.0       | 185.0      | 35.0        |





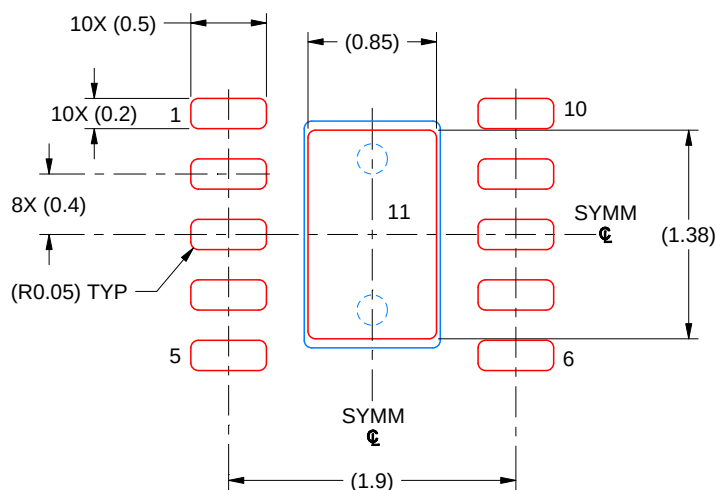


## EXAMPLE STENCIL DESIGN

DSQ0010A

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 MM THICK STENCIL  
SCALE: 20X

EXPOSED PAD 11  
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4218906/A 04/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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