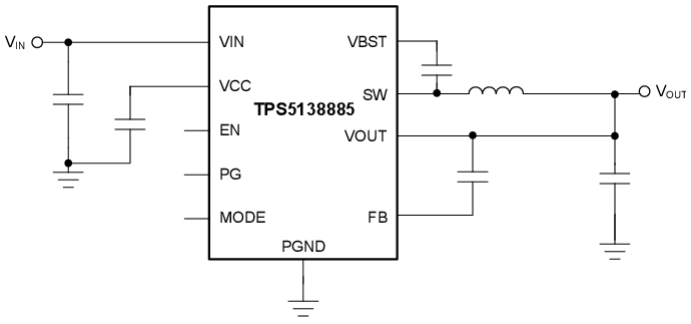
TPS513885 5.5V～24V、12A、同期整流降圧コンバータ

1 特長

- 入力電圧範囲:5.5V～24V
- 5.15V 出力電圧
- 9.2mΩ および 4.5mΩ FET を内蔵
- 12A の連続出力電流をサポート
- 90uA 低静止時電流
- 出力電圧精度:±1.0% (25℃)
- D-CAP3™ 制御モード アーキテクチャによる高速過渡応答
- POSCAP およびすべての MLCC 出力コンデンサをサポート
- 動的変更により選択可能な Eco-mode と Out-of-Audio™モード
- システム スタンバイ中の ULQ™バッテリ寿命延長機能
- 出力放電機能を内蔵
- パワーグッド インジケータを内蔵
- 560kHz と 920kHz のスイッチング周波数を選択可能
- 固定ソフトスタート時間:0.9ms
- 大きいデューティ サイクル動作
- サイクル単位の過電流保護および負の過電流保護
- ラッチ付きの出力 OV および UV 保護
- ラッチなしの UVLO および OT 保護
- 動作時接合部温度:-20℃～125℃
- 13 ピン 3.0mm × 4.0mm HotRod™ VQFN パッケージ
- WEBENCH® Power Designer により、TPS513885 を使用するカスタム設計を作成

2 アプリケーション

- ノート PC およびデスクトップ PC
- ウルトラブック、ハンドヘルド タブレット
- 産業用 PC 、シングル ボード コンピュータ
- 非軍事用ドローン
- 分散電源システム



概略回路図

3 概要

このデバイスは、モノリシック 12A 同期整流降圧コンバータであり、高効率を実現する MOSFET が内蔵されており、また、必要な外付け部品数が最小であるため、スペースの制約が厳しい電力システムでも使いやすくなっています。

TPS513885 は、内部補償を使用して高速な過渡応答と非常に優れたラインおよび負荷レギュレーションを実現する D-CAP3 制御モードを採用しています。ULQ (超低静止電流) バッテリ寿命延長機能は、低消費電力動作で長いバッテリ寿命の実現に非常に有益です。デューティ比の大きい動作により、入力電圧が低いときは負荷過渡性能が大幅に向上します。

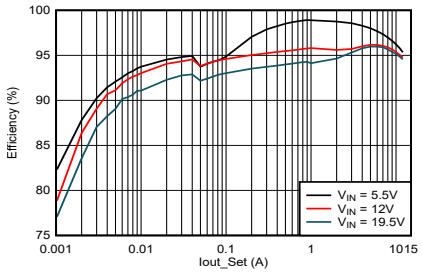
EN ピンは、軽負荷動作のための Eco-Mode または Out-of-Audio (OOA) モードを設定するのに利用できます。Eco-mode は、軽負荷動作時に高効率を維持します。OOA モードは、効率の低下を最小限に抑えながら、スイッチング周波数を可聴周波数より高く維持します。コンバータが動作中であっても、EN ピンを動的にトグルできます。

TPS513885 はパワーグッド インジケータを内蔵しており、出力放電機能を備えています。TPS513885 は、OVP、UVP、OCP、OTP、UVLO などの保護機能一式を搭載しています。このデバイスは、13 ピン 3.0mm × 4.0mm HotRod パッケージで供給され、-20℃～125℃の接合部温度で動作が規定されています。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
TPS513885	VAB (VQFN-HR、13)	4mm × 3 mm

(1) 詳細については、セクション 10 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



効率と出力電流との関係、560kHz、Eco モード

Table of Contents

4 Pin Configuration and Functions

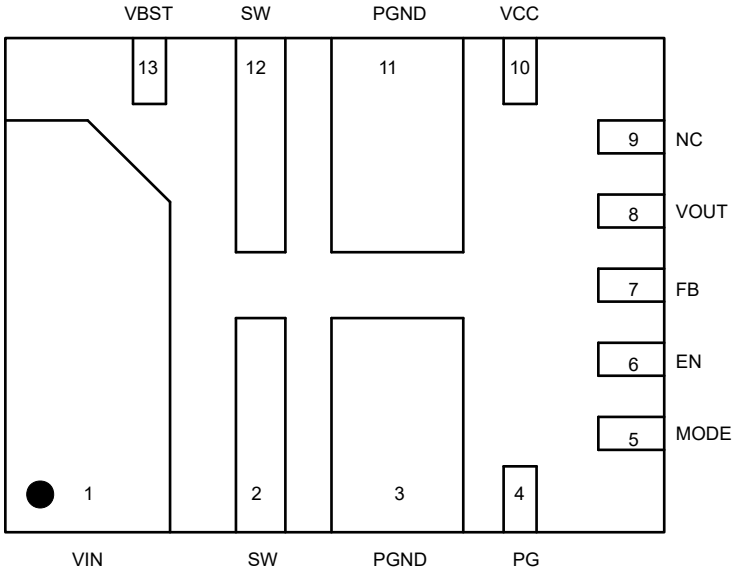


図 4-1. 13-Pin VQFN-HR, VAB Package (Top View)

表 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
VIN	1	P	Input voltage supply pin for the control circuitry. Connect the input decoupling capacitors between VIN and PGND.
SW	2,12	O	Switching node connection to the inductor and bootstrap capacitor for buck. This pin voltage swings from a diode voltage below the ground up to input voltage of buck.
PGND	3,11	G	Power GND terminal for the controller circuit and the internal circuitry.
PG	4	O	Power good indicator pin. This pin asserts low if the output voltage of buck is out of range due to thermal shutdown, dropout, over-voltage, EN shutdown or during slow start.
MODE	5	I	Mode selection pin. Pull MODE pin to voltage larger than 1V, connect the pin to EN or VCC for 560kHz operation. Pull MODE pin low to GND for 920kHz operation.
EN	6	I	Enable input of buck converter. The EN pin is also used to select light load operation mode. Pull EN above 2.2V for Eco-mode. Pull EN between 1V to 1.6V for OOA mode.
FB	7	I	Converter feedback input, can be used for feedforward compensation to improve load transient performance.
VOUT	8	I	Output pin. Connect to the output of the buck regulator. The pin also provides the bypass input for internal VCC LDO.
NC	9	—	Not connected.
VCC	10	O	Internal 5V LDO output. Power supply for internal analog circuits and driving. Decouple this pin to ground with a 2.2µF ceramic capacitor.
VBST	13	I	Boot-strap pin. Supply high side gate driver. Connect a 0.1µF ceramic capacitor between this pin and the SW pin.

(1) I = input, O = output, P = power, G = ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	VIN	–0.3	28	V
	VBST	–0.3	32	V
	VBST-SW	–0.3	6	V
	EN, MODE, FB	–0.3	6	V
	VOUT	–0.3	6.5	V
	PGND	–0.3	0.3	V
Output voltage	SW	–1	28	V
	SW (10ns transient)	–3	28	V
	PG, VCC	–0.3	6	V
T_J	Operating junction temperature	–20	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	VIN	4.5	24	V
	VBST	–0.3	29.5	V
	VBST-SW	–0.3	5.5	V
	EN, MODE, FB, VOUT	–0.3	5.5	V
	PGND	–0.3	0.3	V
Output voltage	SW	–1	24	V
	PG,VCC	–0.3	5.5	V
I_{OUT}	Output current		12	A
T_J	Operating junction temperature	–20	125	°C

5.4 Thermal Information

THERMAL METRIC[1]		TPS513885 VAB (VQFN) 13 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	53.8	°C/W
$R_{\theta JA\_effective}$	Junction-to-ambient thermal resistance (4-layer custom board)[2]	26.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.
(2) The effective $R_{\theta JA}$ is simulated based on TPS513885EVM.

5.5 Electrical Characteristics

T_J = –20°C to 125°C, V_{IN} = 12V, unless otherwise noted.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
VIN	Input voltage range		5.5		24	V
I_{VIN}	Non-switching supply current	No load, V_{EN} = 5V, non-switching		90		µA
I_{VINSDN}	Shutdown supply current	No load, V_{EN} = 0V		3		µA
VCC OUTPUT						
V_{CC}	VCC output voltage	V_{IN} > 5.2V, I_{VCC} ≤ 1 mA, Bypasss switch off	4.6	4.9	5.2	V
OUTPUT VOLTAGE						
V_{OUT} V	Output voltage	T_J = 25°C	5.1	5.15	5.2	V
		T_J = –20°C to 125°C	5.07	5.15	5.23	V
DUTY CYCLE and FREQUENCY CONTROL						
F_{SW}	Switching frequency	CCM operation, MODE > 1V		560		kHz
		CCM operation, MODE < 0.4V		920		kHz
$t_{ON(MIN)}$	SW minumum on time[1]			60		ns
$t_{OFF(MIN)}$	SW minimum off time[1]			130		ns
OOA Function						
T_{OOA}	Mode Operation Period		22	30	42	us
MOSFET and DRIVERS						
$R_{DS(ON)H}$	High side switch resistance	T_J = 25°C		9.2		mΩ
$R_{DS(ON)L}$	Low side switch resistance	T_J = 25°C		4.5		mΩ
OUTPUT DISCHARGE and SOFT START						
R_{DIS}	Discharge resistance	V_{EN} = 0V		50		Ω
t_{SS}	Soft-start time	Internal soft-start time		0.9		ms
POWER GOOD						
t_{PGDLY}	PG delay rising	PG from low to high		160		us
	PG delay falling	PG from high to low		30		us
V_{PGTH}	PG threshold	VFB falling (fault)		83		%
		VFB rising (good)		90		%
		VFB rising (fault)		120		%
		VFB falling (good)		115		%

5.5 Electrical Characteristics (続き)

T_J = –20°C to 125°C, V_{IN} = 12V, unless otherwise noted.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{PG_L}	PG sink current capability	I_{OL} = 4mA			0.4	V
I_{PGLK}	PG leak current	V_{PGOOD} = 5.5V			1	µA
CURRENT LIMIT						
I_{OCL}	Overcurrent threshold (valley)	Valley current limit on LS FET, T_J = 25°C	12.5	14	16	A
	Overcurrent threshold (peak)	Peak current limit on HS FET, T_J = 25°C		22		A
I_{NOCL}	Negative over current threshold	Sinking current limit on LS FET, OOA operation		5.5		A
LOGIC THRESHOLD						
V_{ENH}	EN high-level input voltage	T_J = 25°C	1			V
V_{ENL}	EN low-level input voltage	T_J = 25°C			0.4	V
I_{EN}	Enable internal pull down current	V_{EN} = 0.3V		2		µA
$V_{EN(OOA)}$	OOA mode for EN pin		1		1.6	V
$V_{EN(ECO)}$	Eco-mode for EN pin		2.2		5.5	V
$V_{MODE(560k)}$	Mode threshold high-level	T_J = 25°C	1			V
$V_{MODE(920k)}$	Mode threshold low-level	T_J = 25°C			0.4	V
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	OVP trip threshold			120		%
t_{OVPDLY}	OVP prop deglitch			256		us
V_{UVP}	UVP trip threshold			60		%
t_{UVPDLY}	UVP prop deglitch			200		us
UVLO						
V_{UVLO}	VIN UVLO threshold	Wake up		4.25	4.45	V
		Shutdown	3.4	3.6		V
		Hysteresis		0.65		V
OVERTEMPERATURE PROTECTION						
T_{OTP}	OTP trip threshold(1)	Shutdown temperature		160		°C
T_{OTPHSY}	OTP hysteresis(1)	Hysteresis		20		°C

(1) Specified by design. Not production tested.

5.6 Typical Characteristics

T_J = –20°C to 125°C, V_{IN} = 12V, unless otherwise noted.

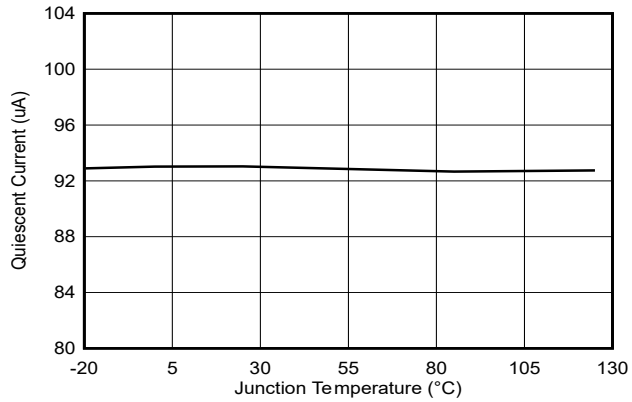


図 5-1. Supply Current vs Junction Temperature

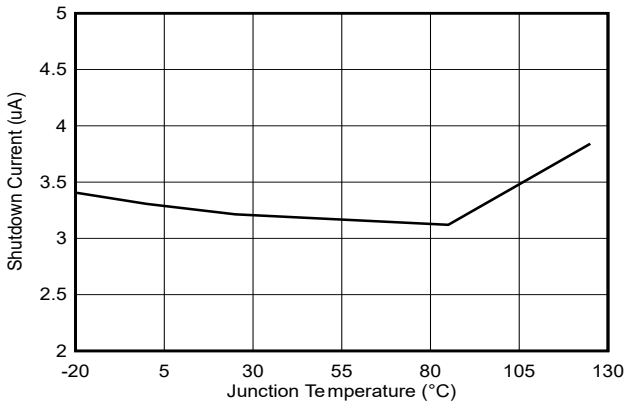


図 5-2. Shutdown Current vs Junction Temperature

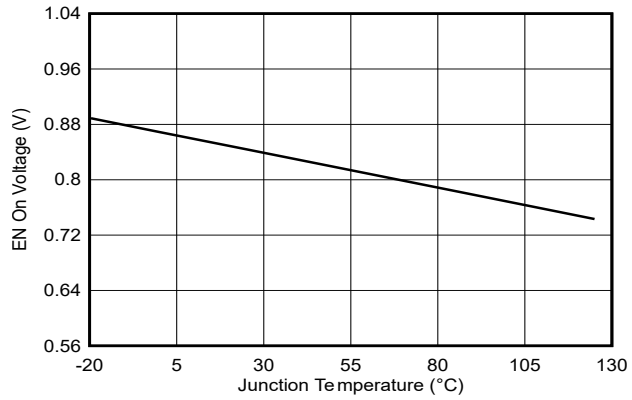


図 5-3. Enable On Voltage vs Junction Temperature

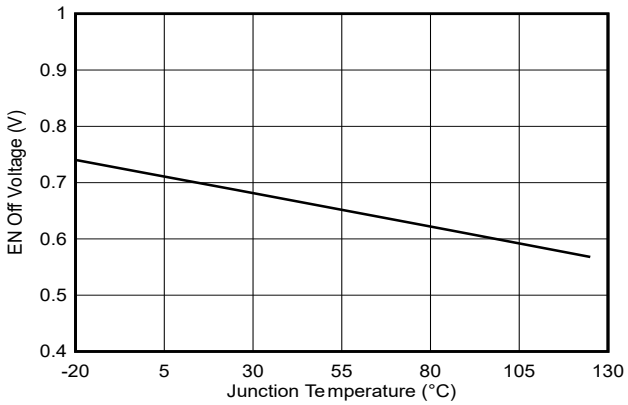


図 5-4. Enable Off Voltage vs Junction Temperature

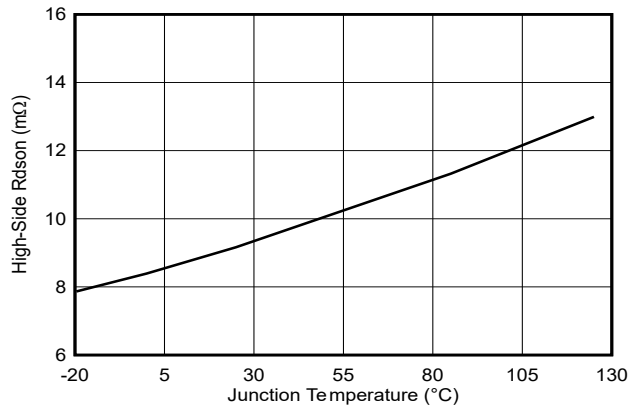


図 5-5. High-Side $R_{DS(on)}$ vs Junction Temperature

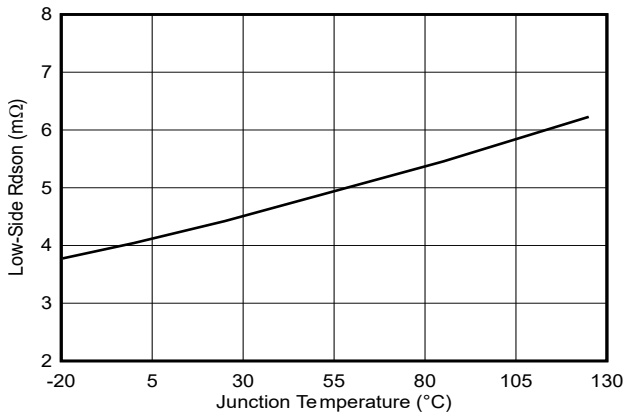


図 5-6. Low-Side $R_{DS(on)}$ vs Junction Temperature

5.6 Typical Characteristics (continued)

T_J = –20°C to 125°C, V_{IN} = 12V, unless otherwise noted.

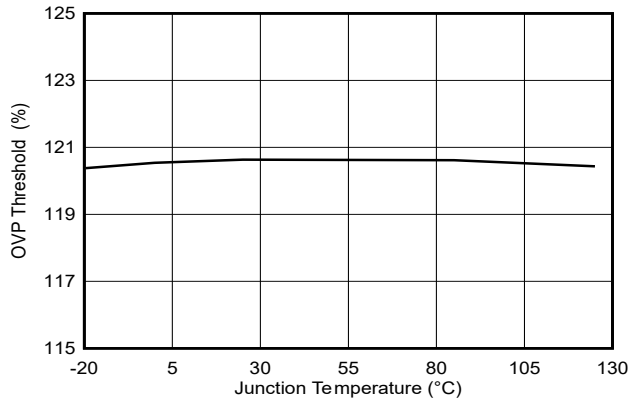


図 5-7. OVP Threshold vs Junction Temperature

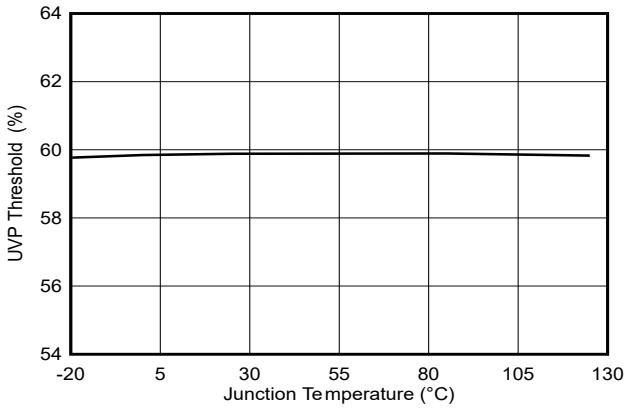


図 5-8. UVP Threshold vs Junction Temperature

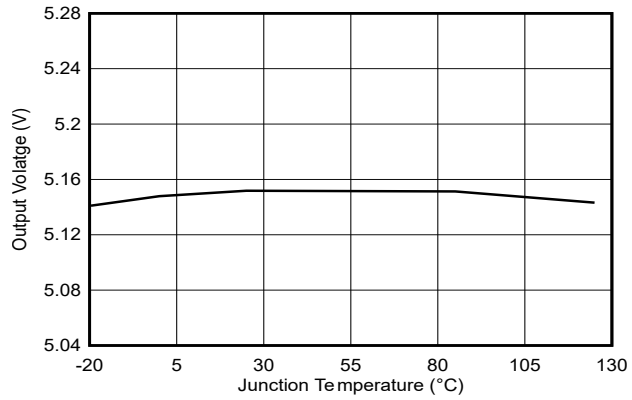


図 5-9. Output Voltage vs Junction Temperature

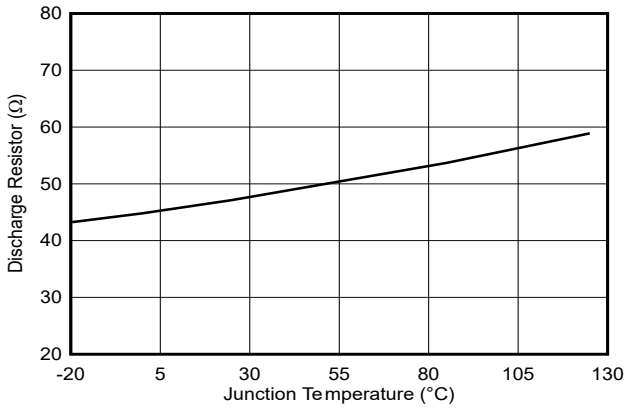


図 5-10. Discharge Resistor vs Junction Temperature

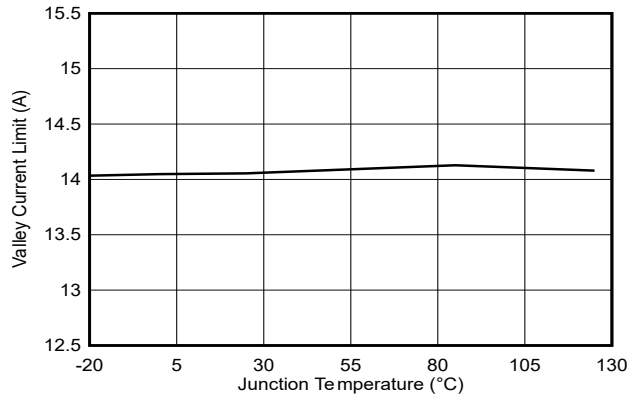


図 5-11. Valley Current Limit vs Junction Temperature

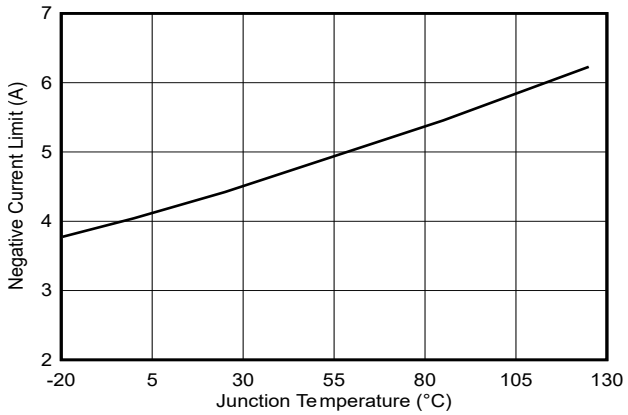


図 5-12. Negative Current Limit vs Junction Temperature

5.6 Typical Characteristics (continued)

T_J = –20°C to 125°C, V_{IN} = 12V, unless otherwise noted.

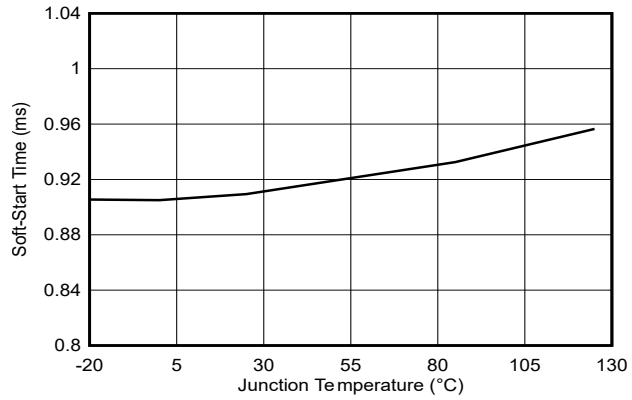


図 5-13. Soft-Start Time vs Junction Temperature

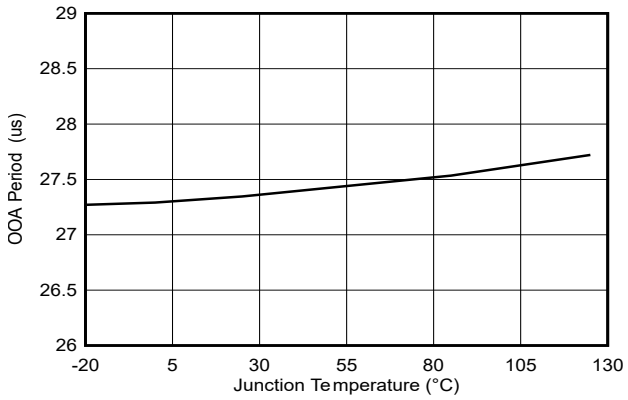


図 5-14. OOA Period vs Junction Temperature

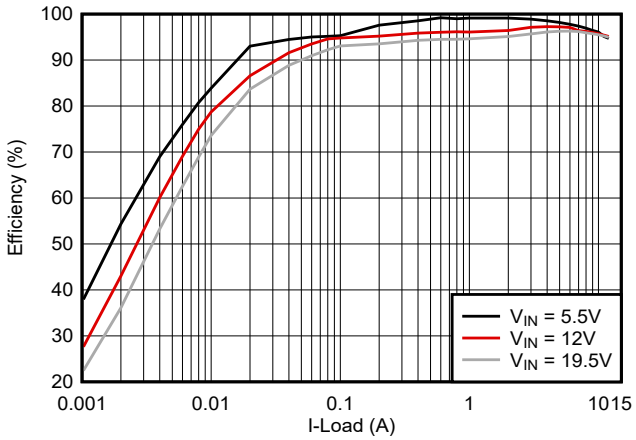


図 5-15. Efficiency vs Load Current, 560kHz, OOA Mode

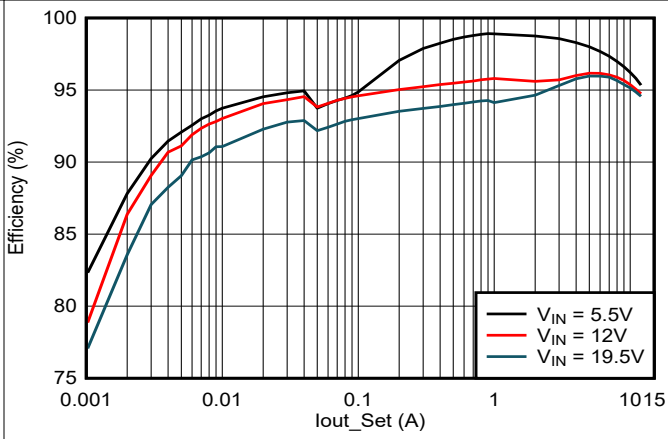


図 5-16. Efficiency vs Load Current, 560kHz, Eco-mode

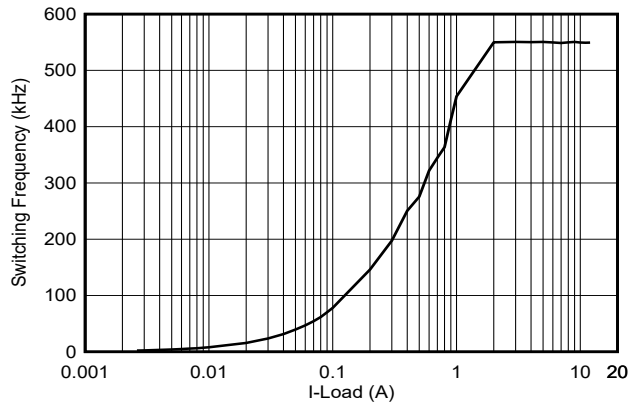


図 5-17. Switching Frequency vs Load Current, F_{SW} = 560kHz, ECO

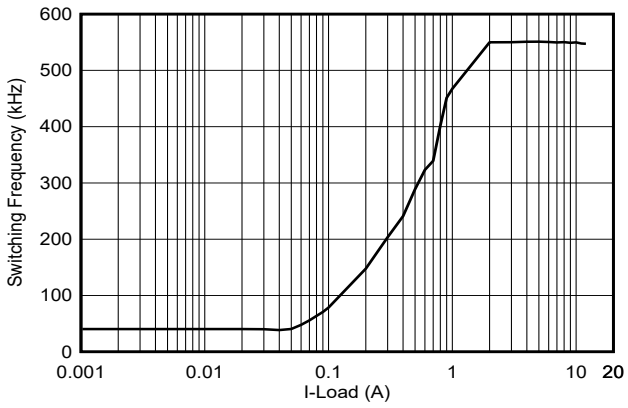


図 5-18. Switching Frequency vs Load Current, F_{SW} = 560kHz, OOA

6 Detailed Description

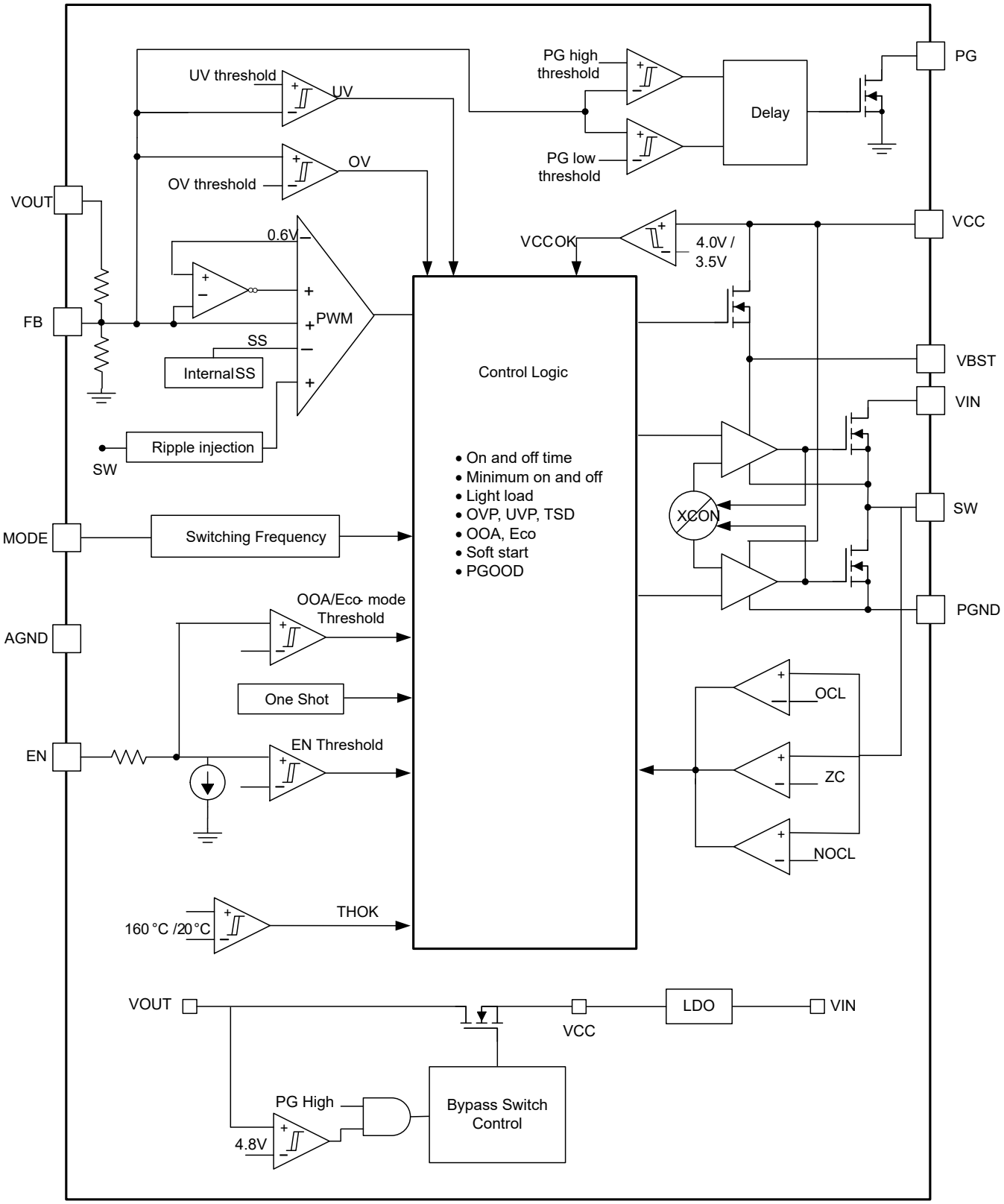
6.1 Overview

TPS513885 is 12A, integrated FET, synchronous step-down converters which can operate from 5.5V to 24V input voltage (VIN). TPS513885 is with fixed 5.15V output voltage. The device has 9.2mΩ and 4.5mΩ integrated MOSFETs that enable high efficiency up to 12A. The device employs D-CAP3 control mode that provides fast transient response with no external compensation components and an accurate feedback voltage. The control topology provides seamless transition between CCM operating mode at higher load condition and DCM, Eco-mode operation at lighter load condition. DCM, Eco-mode allows the TPS513885 to maintain high efficiency at light load. TPS513885 also has selectable Out-of-Audio (OOA) mode to maintain a minimum of 25kHz switching frequency that is above audible range (20Hz – 20kHz). D-CAP3 control mode allows the use of low equivalent series resistance (ESR) output capacitors such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors.

TPS513885 has 5V internal VCC LDO that creates bias for all internal circuitry. The undervoltage lockout (UVLO) circuit monitors the VCC pin voltage to protect the internal circuitry from low input voltages. TPS513885 has an internal pulldown current source on the EN pin, require external pullup circuit to enable buck converter.

TPS513885 features light load operation mode dynamic change by adjusting EN voltage level, which allows the device to change state between OOA Mode and Eco-mode dynamically. TPS513885 supports selectable 560kHz or 920kHz switching frequency by setting MODE pin voltage before soft start. The internal soft-start time is fixed 0.9ms to simplify the design circuit and reduce the external components.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 PWM Operation and D-CAP3™ Control Mode

The main control loop of the buck is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP3 control mode. The D-CAP3 control mode combines adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. The D-CAP3 control mode is stable even with virtually no ripple at the output. The TPS513885 also includes an error amplifier that makes the output voltage high accurate.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after an internal one-shot timer expires. This one-shot duration is set proportional to the converter input voltage, V_{IN}, and is inversely proportional to the output voltage, V_{OUT}, to maintain a pseudo-fixed frequency over the input voltage range, hence called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ripple generation circuit is added to the reference voltage to emulate the output ripple. This action enables the use of very low-ESR output capacitors such as multi-layered ceramic caps (MLCC). No external current sense network or loop compensation is required for D-CAP3 control mode.

For any control topology that is compensated internally, there is a range of the output filter the control topology can support. The output filter used with the TPS513885 is a low-pass L-C circuit. This L-C filter has a double-pole frequency calculated in 式 1.

$$f_P = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} \quad (1)$$

At low frequencies, the overall loop gain is set by the external output set-point resistor divider network and the internal gain of the TPS513885. The low-frequency L-C double pole has a 180 degree lag in-phase. At the output filter frequency, the gain rolls off at a –40dB per decade rate and the phase drops rapidly. The internal ripple generation network introduces a mid-frequency zero that reduces the gain roll off from –40dB to –20dB per decade and increases the phase to 90 degree one decade above the zero frequency. The inductor and capacitor selected for the output filter must be such that the double pole is placed close enough to the mid-frequency zero so that the phase boost provided by this mid-frequency zero provides adequate phase margin for the stability requirement. The crossover frequency of the overall system must usually be targeted to be less than one-third of the switching frequency (F_{SW}).

6.3.2 VCC Switchover Function

VCC switchover function is designed to bypass internal 5V LDO with the power from VOUT and enhance light load efficiency. The VCC switchover is a seamless behavior of regulator and does not need any additional configuration.

The VCC pin switchover function is asserted when two conditions are present:

- PGOOD is not pulled low
- VOUT voltage is higher than 4.8V

In this switchover condition, one thing occurs: the VCC output is connected to VOUT by internal switchover MOSFET.

6.3.3 Soft Start

The TPS513885 has an internal 0.9ms soft start. When the EN pin becomes high, the internal soft-start function begins ramping up the reference voltage to the PWM comparator. If the output capacitor is prebiased at start-up, the device initiates switching and starts ramping up only after the internal reference voltage becomes greater than the feedback voltage VFB. This scheme makes sure that the converters ramp up smoothly into regulation point.

6.3.4 Large Duty Operation

The TPS513885 can support large duty operation by the internal T_{ON} extension function. When V_{IN}/V_{OUT} < 1.18 and the V_{FB} keeps lower than internal V_{REF}, the switching frequency is allowed to smoothly drop to make T_{ON} extended to implement the large duty operation and also improve the performance of the load transient performance. The TPS513885 can support up to 98% duty cycle operation.

6.3.5 Power Good

The Power-Good (PGOOD) pin is an open-drain output. TI recommends a pullup resistor of 100kΩ to pull the voltage up to VCC. After V_{FB} is between 90% and 115% of the target output voltage, the PGOOD is pulled high after a 200us de-glitch time. The PGOOD pin is pulled low when:

- FB pin voltage is lower than 83% or greater than 120% of reference voltage
- In OVP, UVP, or thermal shutdown event
- During the soft-start period

6.3.6 Overcurrent Protection and Undervoltage Protection

The TPS513885 has overcurrent protection and undervoltage protection. The output overcurrent protection (OCP) is implemented using a cycle-by-cycle low-side MOSFET valley current detection and high-side MOSFET peak current detection. The switching current is monitored by measuring the MOSFET drain to source voltage. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on-time of the high-side FET switch, the switch current increases at a linear rate determined by Vin, Vout, the on-time, and the output inductor value. During the on-time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current I_{OUT}. If the monitored current is above the OCL level, the converter maintains low-side FET on and delays the creation of a new pulse, even the voltage feedback loop requires one, until the current level becomes OCL level or lower. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of overcurrent protection. When the load current is higher than the $I_{OCL(VALLEY)}$ added by one half of the peak-to-peak inductor ripple current, or higher than $I_{OCL(PEAK)}$ subtracted by one half of the peak-to-peak inductor ripple current, the OCP is triggered and the output current is being limited, the output voltage tends to drop because the load demand is higher than what the converter can support. When the output voltage falls below 60% of the target voltage, the UVP comparator detects the fall, and the device is shut off after a wait time of 200µs. This protection is a latched function. The fault latching can be reset by EN going low or VCC power cycling.

The TPS513885 also implements negative overcurrent protection, which can prevent inductor current runaway when IC works in OOA mode. When the inductor valley current hits the negative overcurrent threshold (I_{NOCL} = –5.5A typical), the low-side FET turns off, then high-side FET turns on.

6.3.7 Overvoltage Protection

The TPS513885 has an overvoltage protection feature, which has the same implementation. When the output voltage becomes higher than 120% of the target voltage, the OVP comparator output goes high, and the output discharges and latches after a wait time of 256µs. This function is a latching operation, so this function needs to reset by EN going low or VIN power cycling.

6.3.8 UVLO Protection

The VIN undervoltage lockout (UVLO) protection monitors the VIN pin voltage to protect the internal circuitry from low input voltage. When the VIN voltage is lower than the UVLO threshold voltage, the device shuts off and outputs are discharged to prevent misoperation of the device. The converter begins operation again when the input voltage exceeds the threshold by a hysteresis of 650mV (typical). This protection is a non-latch protection.

6.3.9 Output Voltage Discharge

TPS513885 has a 50ohm discharge switch that discharges the output VOUT through the Vout pin during any event of fault like output overvoltage, output undervoltage, TSD, or if the VIN voltage is below the UVLO and when the EN pin voltage is below the turn-on threshold.

6.3.10 Thermal Shutdown

The TPS513885 monitors the internal die temperature. If the temperature exceeds the threshold value (typically 160°C), the device is shut off and the output is discharged. This protection is a non-latch protection. The device restarts operation when the temperature goes below the thermal shutdown threshold.

6.4 Device Functional Modes

6.4.1 Light Load Operation

The TPS513885 has the EN pin that can control two different states of operation at light load. Pull the EN above 2.2V for Eco-mode. Pull the EN between 1V to 1.6V for OOA mode. The EN pin can be toggled dynamically, even when the converter is in operation.

6.4.2 Advanced Eco-mode Control

The advanced Eco-mode control schemes to maintain high light load efficiency. As the output current decreases from heavy load conditions, the inductor current is also reduced and eventually comes to a point where the rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode. The on-time is kept almost the same as in continuous conduction mode so that discharging the output capacitor with smaller load current to the level of the reference voltage takes longer. This action makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high. Use 式 2 to calculate the light load current where the transition to Eco-mode operation happens ($I_{OUT(LL)}$).

$$I_{OUT(LL)} = \frac{1}{2 \times L_{OUT} \times F_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (2)$$

After identifying the application requirements, design the output inductance (L_{OUT}) so that the inductor peak-to-peak ripple current is approximately between 20% and 40% of $I_{OUT(max)}$ (peak current in the application). Sizing the inductor properly so that the valley current does not hit the negative low-side current limit is important.

6.4.3 Out-of-Audio™ Mode

Out-of-Audio (OOA) mode is a unique control feature that keeps the switching frequency above audible frequency with minimum reduction in efficiency. This mode prevents audio noise generation from the output capacitors and inductor. During Out-of-Audio operation, the OOA control circuit monitors the states of both high-side and low-side MOSFETs and forces them to switch. When both high-side and low-side MOSFETs are off for more than 30µs during a light-load condition, the low-side FET discharges until output voltage drops to trigger the high-side FET on or inductor current hits negative OC limit.

If the EN pin is selected to operate in OOA mode, when the device works at light load, the minimum switching frequency is above 20kHz, which avoids the audible noise in the system. When the device works in OOA mode, TI recommends setting the valley value of inductor current above –3A by choosing the appropriate inductor.

6.4.4 Mode Selection

TPS513885 has a MODE pin that can be used to select 560kHz or 920kHz switching frequency. The device reads the voltage on the MODE pin during start-up and latches onto one of the MODE options listed below in 表 6-1.

表 6-1. MODE Pin Settings

VOLTAGE ON MODE	RECOMMENDED DESIGN	FREQUENCY (kHz)
> 1V	Pull high to VCC/EN	560
< 0.4V	Pull low to GND	920

図 6-1 shows the typical start-up sequence of the device after the enable signal crosses the EN turn-on threshold. After the voltage on VCC crosses the rising UVLO threshold, finishing the frequency selection takes about 104µs. The output voltage starts ramping after the mode selection.

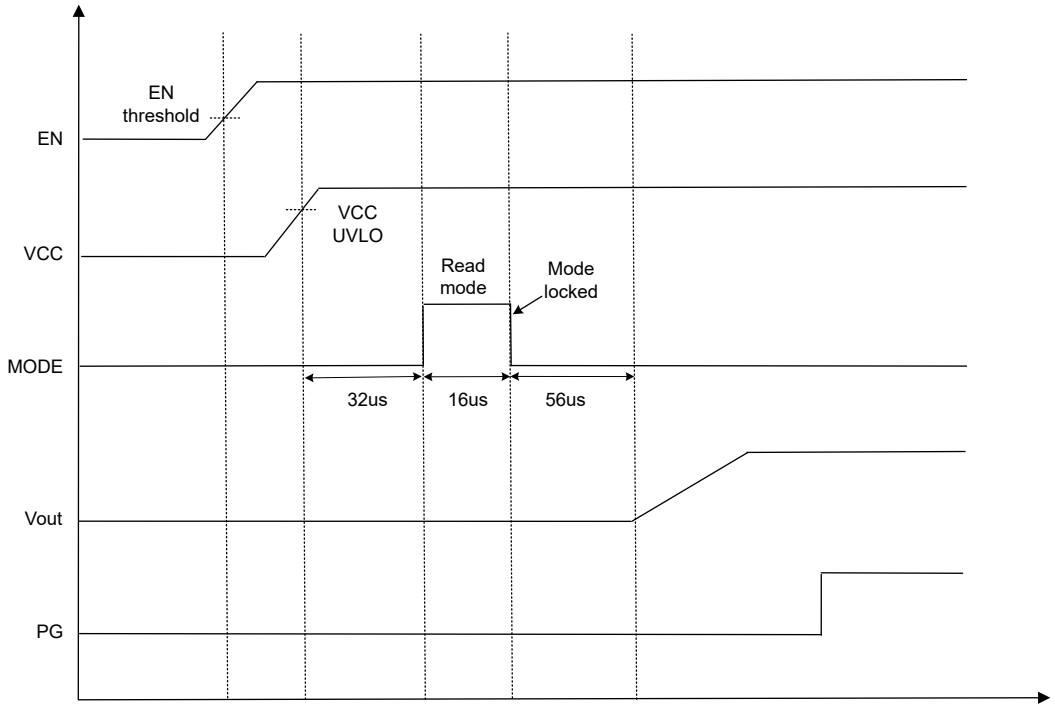


図 6-1. Power-Up Sequence

6.4.5 Standby Operation

The TPS513885 can be placed in standby mode by pulling the EN pin low. The device operates with a shutdown current of 3µA when in standby condition. EN pin is pulled low internally. When floating, the part is disabled by default.

7 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Application Information

The schematic in 図 7-1 shows a typical application for TPS513885 with 5.15V output. This design converts an input voltage range of 5.5V to 24V down to 5.15V with a maximum output current of 12A.

7.2 Typical Application

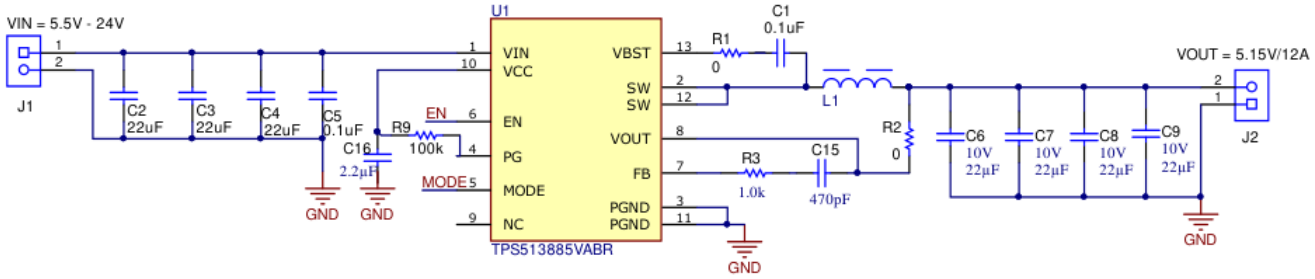


図 7-1. 5.15V, 12A Reference Design

7.2.1 Design Requirements

表 7-1 lists the design parameters for this example.

表 7-1. Design Parameters

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
V_{OUT}	Output voltage			5.15		V
I_{OUT}	Output current			12		A
V_{IN}	Input voltage		5.5	19.5	24	V
$V_{OUT(ripple)}$	Output voltage ripple	0A – 12A loading		40		mV_{P-P}
F_{SW}	Switching frequency			560		kHz
	Light load operating mode			Eco-mode		
T_A	Ambient temperature			25		°C

7.2.2 Detailed Design Procedure

7.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS513885 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance

- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

7.2.2.2 External Component Selection

7.2.2.2.1 VOUT and FB Pin Configuration

As TPS513885 is with fixed 5.15V output voltage, there is no need to configure the feedback resistor and only connect the output terminal to VOUT pin directly. A feedforward compensation can be used to improve load transient performance.

7.2.2.2.2 MODE Selection

The switching frequency is set by the voltage configured on the MODE pin. See 表 6-1 for possible MODE pin configurations. For this design example, the switching frequency is about 560KHz.

7.2.2.2.3 Inductor Selection

The inductor ripple current is filtered by the output capacitor. A higher inductor ripple current means the output capacitor must have a ripple current rating higher than the inductor ripple current. See 表 7-2 for recommended inductor values.

Use 式 3 and 式 4 to calculate the RMS and peak currents through the inductor. Make sure that the inductor is rated to handle these currents.

$$I_{L(rms)} = \sqrt{I^2{}_{OUT} + \frac{1}{12} \times \left[\frac{V_{OUT} \times \left(V_{IN(max)} - V_{OUT}\right)}{V_{IN(max)} \times L_{OUT} \times F_{SW}}\right]^2} \quad (3)$$

$$I_{L(peak)} = I_{OUT} + \frac{I_{OUT(ripple)}}{2} \quad (4)$$

Under transient and short-circuit conditions, the inductor current can increase up to the current limit of the device, choosing an inductor with a saturation current higher than the peak current under current limit condition is safe.

7.2.2.2.4 Output Capacitor Selection

After selecting the inductor, the output capacitor must be optimized. In D-CAP3 control mode, the regulator reacts within one cycle to the change in the duty cycle, so good transient performance can be achieved without needing large amounts of output capacitance. The recommended output capacitance range is given in the following table. Ceramic capacitors have very low ESR, otherwise the maximum ESR of the capacitor must be less than $V_{OUT(ripple)}/I_{OUT(ripple)}$.

表 7-2. Recommended Component Values

V_{OUT} (V)	F_{sw} (kHz)	L_{OUT} (µH)	$C_{OUT(min)}$ (µF)	$C_{OUT(max)}$ (µF)	R_{FF} (kΩ)	C_{FF} (pF)
5.15	560	1.5	88	198	1	470
5.15	920	1.5	44	88	1	100

7.2.2.2.5 Input Capacitor Selection

The TPS513885 requires input decoupling capacitors on power supply input pin VIN, and the bulk capacitors are needed depending on the application. Use 式 5 to calculate the minimum input capacitance required.

$$C_{IN(min)} = \frac{I_{OUT} \times V_{OUT}}{V_{IN(ripple)} \times V_{IN} \times F_{SW}} \quad (5)$$

TI recommends using a high-quality X5R or X7R input decoupling capacitors of nominal 44µF/35V on the input voltage pin VIN. The voltage rating on the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the application. Use 式 6 to calculate the input ripple current:

$$I_{CIN(rms)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN(min)}} \times \frac{\left(V_{IN(min)} - V_{OUT}\right)}{V_{IN(min)}}} \quad (6)$$

7.2.3 Application Curves

図 7-2 through 図 7-19 apply to the circuit of 図 7-1. V_{IN} = 12V, F_{SW} = 560kHz, T_A = 25°C, unless otherwise specified.

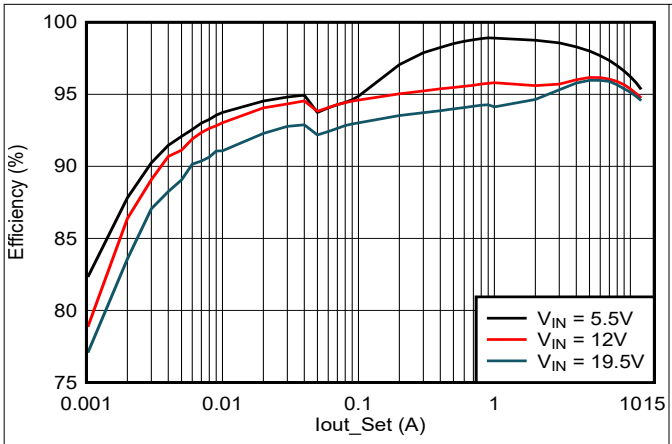


図 7-2. Efficiency Curve (ECO)

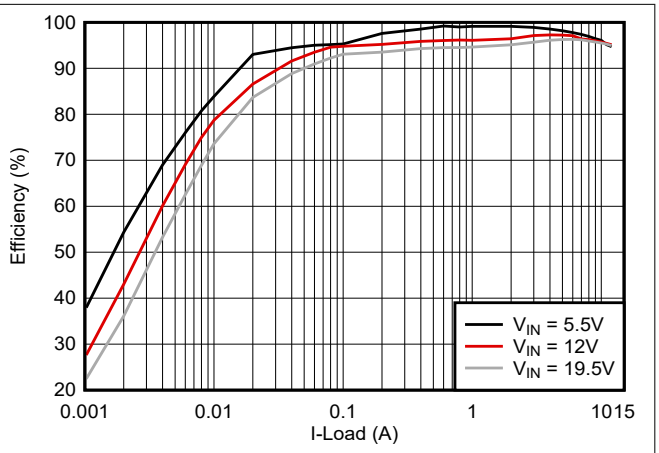


図 7-3. Efficiency Curve (OOA)

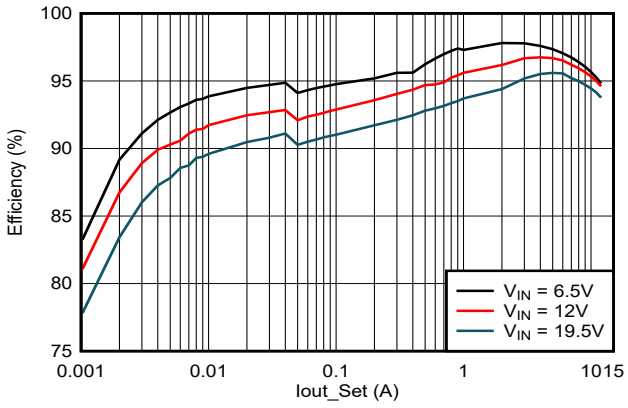


図 7-4. Efficiency Curve (ECO, F_{SW} = 920kHz)

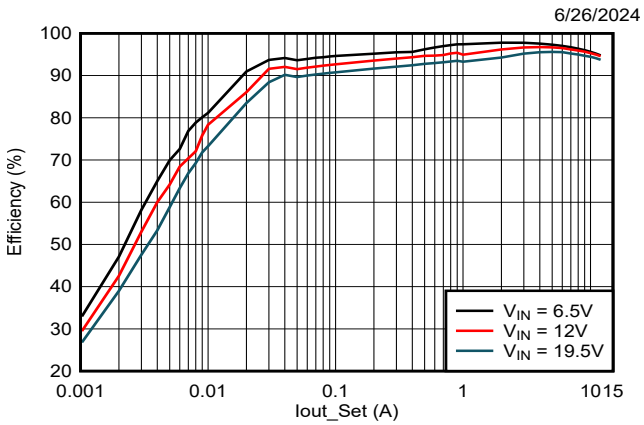


図 7-5. Efficiency Curve (OOA, F_{SW} = 920kHz)

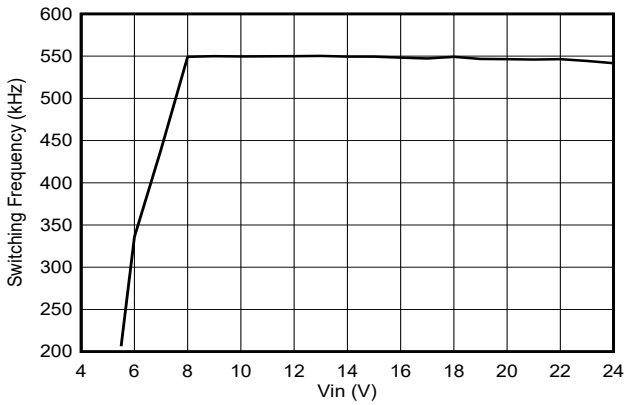


図 7-6. Switching Frequency vs Input Voltage, I_{OUT} = 6A

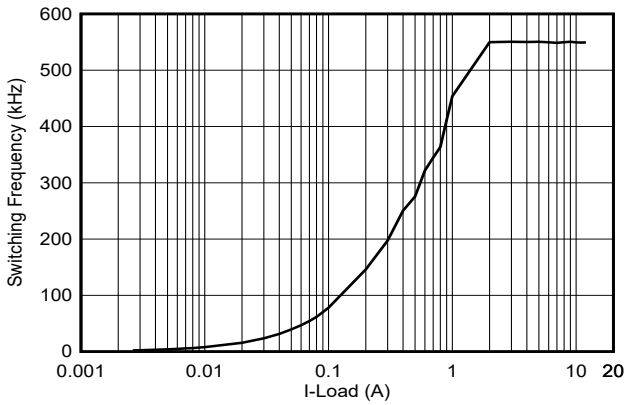


図 7-7. Switching Frequency vs Output Load (ECO)

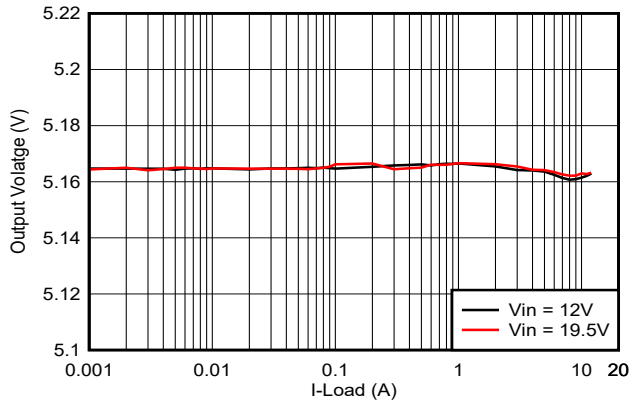


図 7-8. Load Regulation, V_{in} = 12V / 19.5V

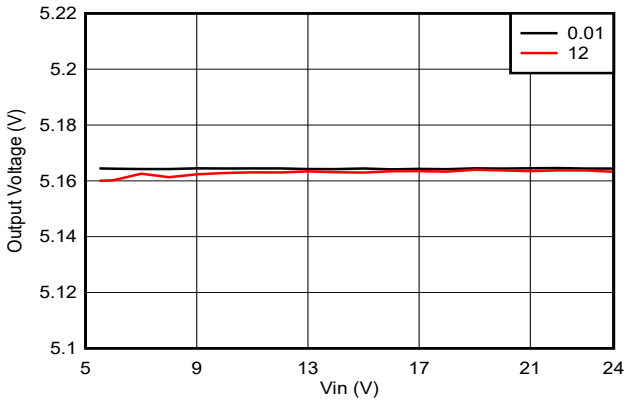


図 7-9. Line Regulation, I_{OUT} = 0.01A / 12A

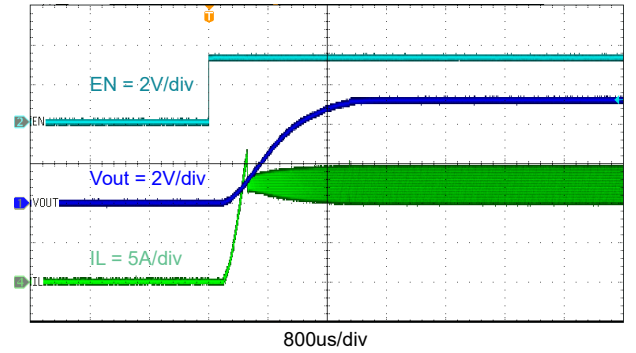


図 7-10. Start-Up Through EN, I_{OUT} = 12A

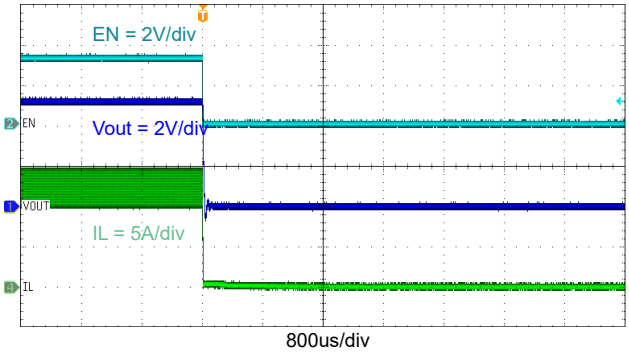


図 7-11. Shutdown Through EN, I_{OUT} = 12A

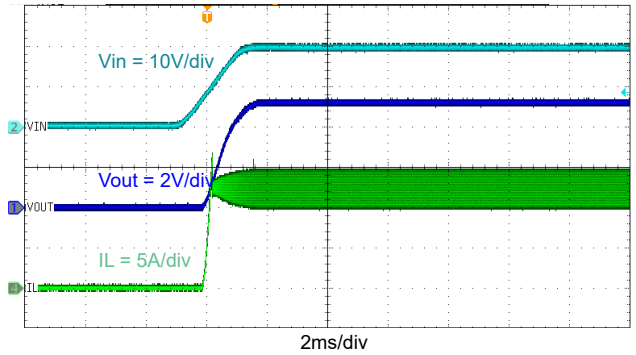


図 7-12. Start-Up Relative to VIN Rising, I_{OUT} = 12A

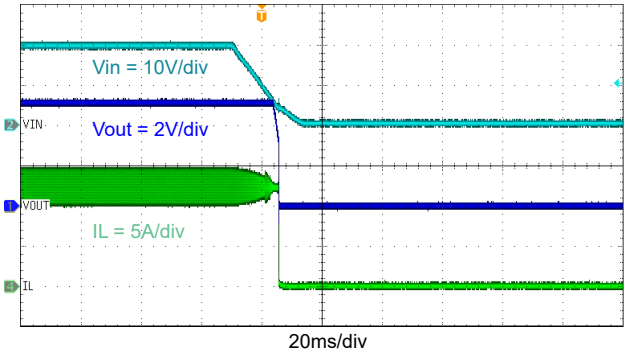


図 7-13. Shutdown Relative to VIN Falling, I_{OUT} = 5A

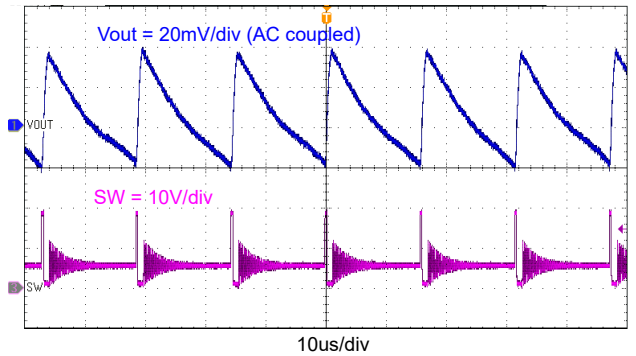


図 7-14. Output Voltage Ripple, I_{OUT} = 0.1A

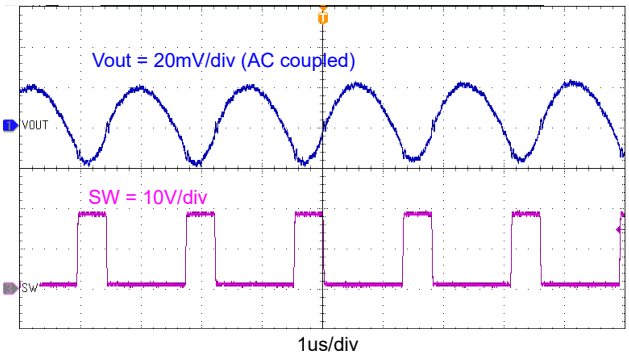


図 7-15. Output Voltage Ripple, I_{OUT} = 6A

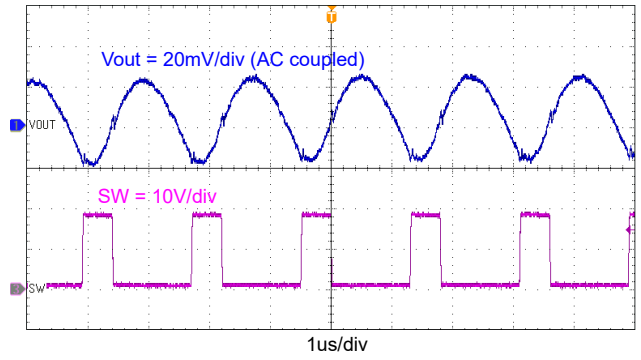


図 7-16. Output Voltage Ripple, I_{OUT} = 12A

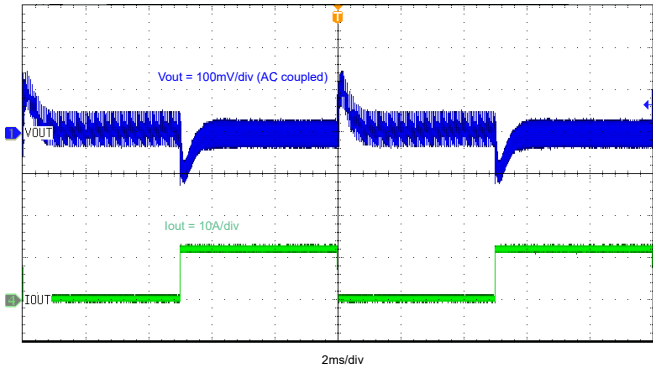


図 7-17. Transient Response, 0A to 12A, Slew Rate = 1.6A/µs

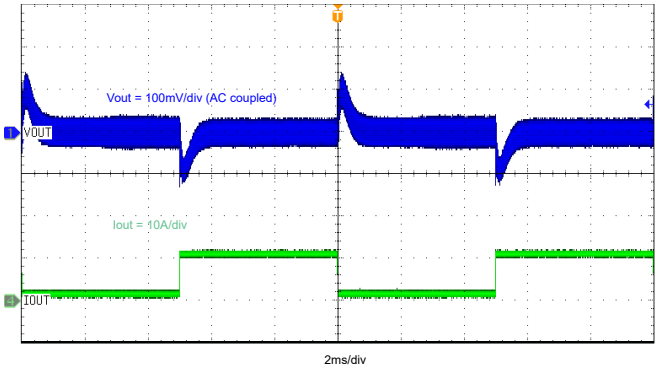


図 7-18. Transient Response, 1.2A to 10.8A, Slew Rate = 1.6A/µs

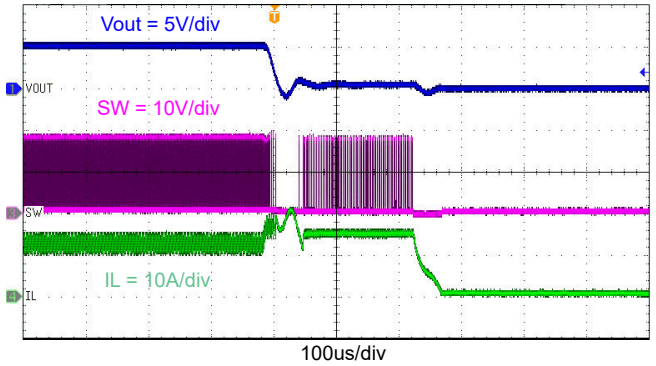


図 7-19. Normal Operation to Output Hard Short

7.3 Power Supply Recommendations

The TPS513885 is intended to be powered by a well-regulated DC voltage. The input voltage range is 5.5V to 24V. The TPS513885 is a buck converter. The input supply voltage must be greater than the desired output voltage for proper operation. Input supply current must be appropriate for the desired output current. If the input voltage supply is located far away from the TPS513885 circuit, TI recommends some additional input bulk capacitance. Typical values are 100µF to 470µF.

7.4 Layout

7.4.1 Layout Guidelines

- Make note that the PCB layout of any DC/DC converter is critical to the excellent performance of the design. Bad PCB layout can disrupt the operation of a good schematic design. Even if the converter regulates correctly, bad PCB layout can mean the difference between a robust design and one that cannot be mass produced. Furthermore, the EMI performance of the converter is dependent on the PCB layout to a great extent. In a buck converter, the most critical PCB feature is the loop formed by the input capacitors and power ground. This loop carries large transient currents that can cause large transient voltages when reacting with the trace inductance. These unwanted transient voltages disrupt the proper operation of the converter. Because of this fact, the traces in this loop must be wide and short, and the loop area as small as possible to reduce the parasitic inductance.
- Use a four-layer PCB for good thermal performance and with maximum ground plane. 3-inch × 2.75-inch, top and bottom layer PCB with 2oz copper is used as example.
- Place the decoupling capacitors right across VIN and VCC as close as possible.
- Place output inductors and capacitors with IC at the same layer. The SW routing must be as short as possible to minimize EMI, and must be a width plane to carry big current. Enough vias must be added to the PGND connection of output capacitors and also as close to the output pin as possible.
- Place BST resistor and capacitor with IC at the same layer, close to BST and SW plane. TI recommends > 10-mil width trace to reduce line parasitic inductance.
- Make feedback 10 mil and routed away from the switching node, BST node, or other high speed digital signal.
- Make VIN trace wide to reduce the trace impedance and provide enough current capability.
- Place multiple vias under the device near VIN and PGND and near input capacitors to reduce parasitic inductance and improve thermal performance.

7.4.2 Layout Example

図 7-20 shows the recommended top-side layout. Component reference designators are the same as the circuit shown in *TPS513885 Step-Down Converter Evaluation Module* EVM user's guide.

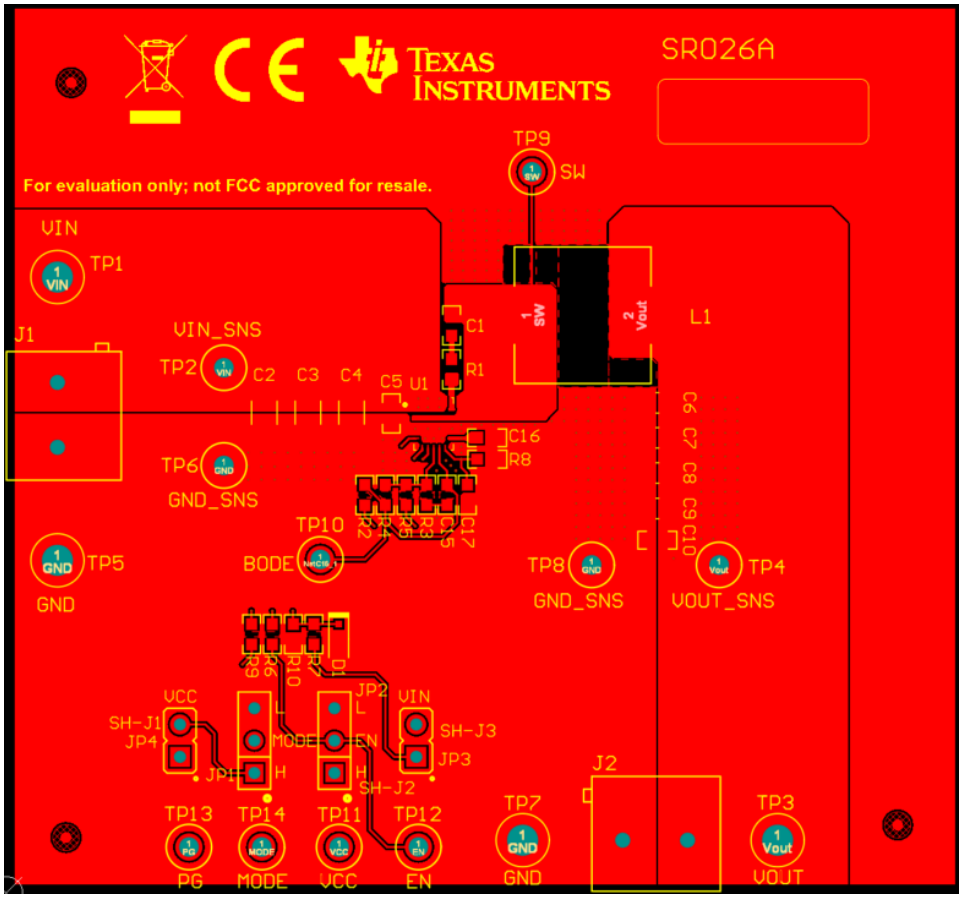


図 7-20. Top-Side Layout

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS513885 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

Texas Instruments, *TPS513885 Step-Down Converter Evaluation Module* EVM user's guide

8.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.4 サポート・リソース

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8.6 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.7 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (June 2024) to Revision B (December 2024)	Page
• Updated specifications in the *Electrical Characteristics* table	5
• Updated the *Functional Block Diagram*	11

Changes from Revision * (May 2024) to Revision A (June 2024)	Page
• ドキュメントのステータスを「事前情報」から「量産データ」に変更	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS513885VABR	Active	Production	VQFN-HR (VAB) | 13	4000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-20 to 125	513885
TPS513885VABR.A	Active	Production	VQFN-HR (VAB) | 13	4000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-20 to 125	513885

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

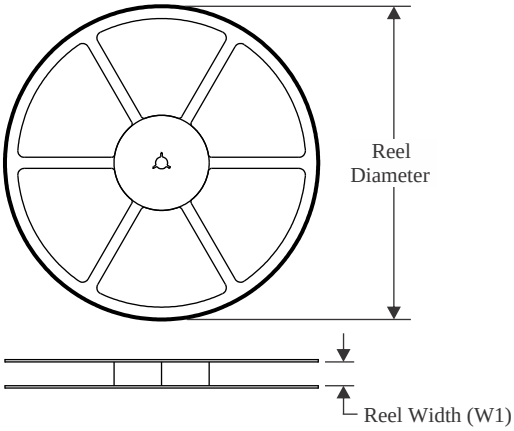
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

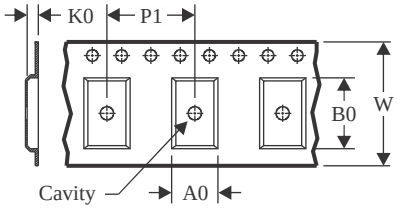
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

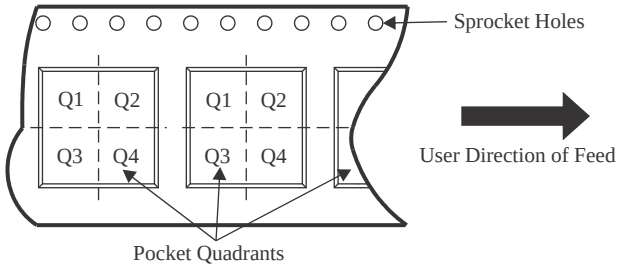


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

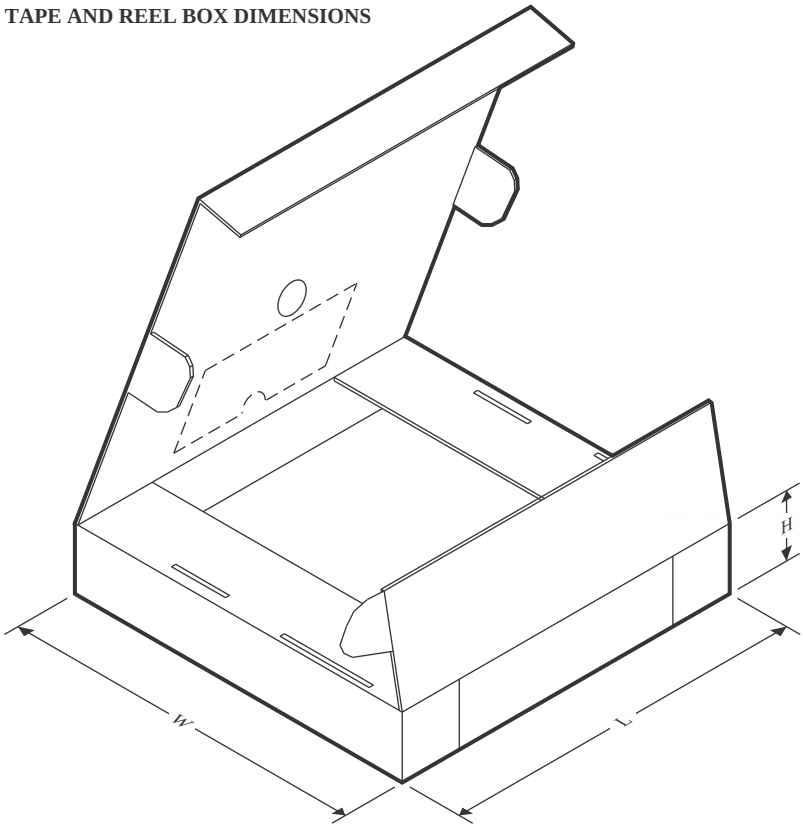
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS513885VABR	VQFN-HR	VAB	13	4000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

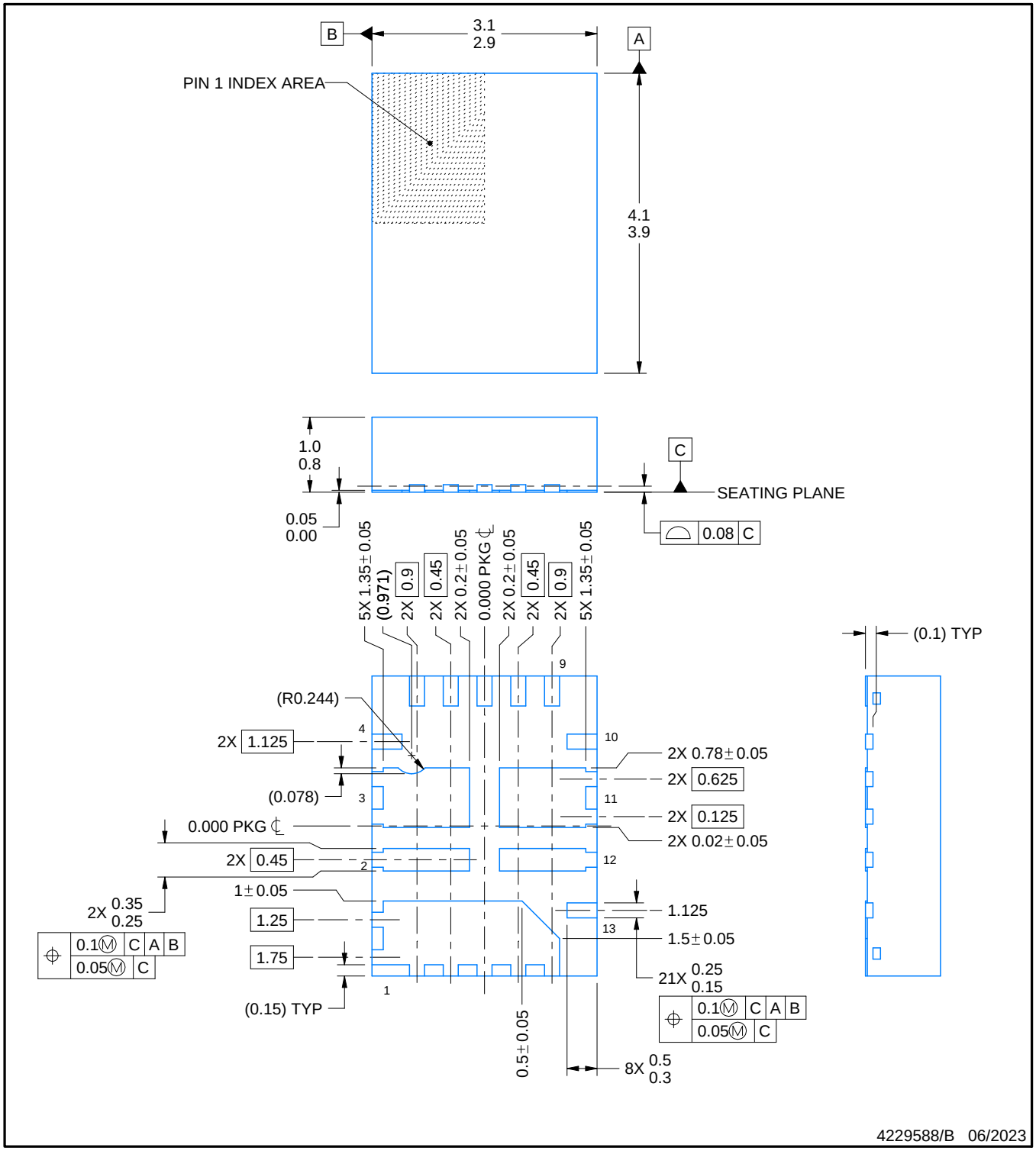
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS513885VABR	VQFN-HR	VAB	13	4000	367.0	367.0	35.0

PACKAGE OUTLINE

VAB0013A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4229588/B 06/2023

NOTES:

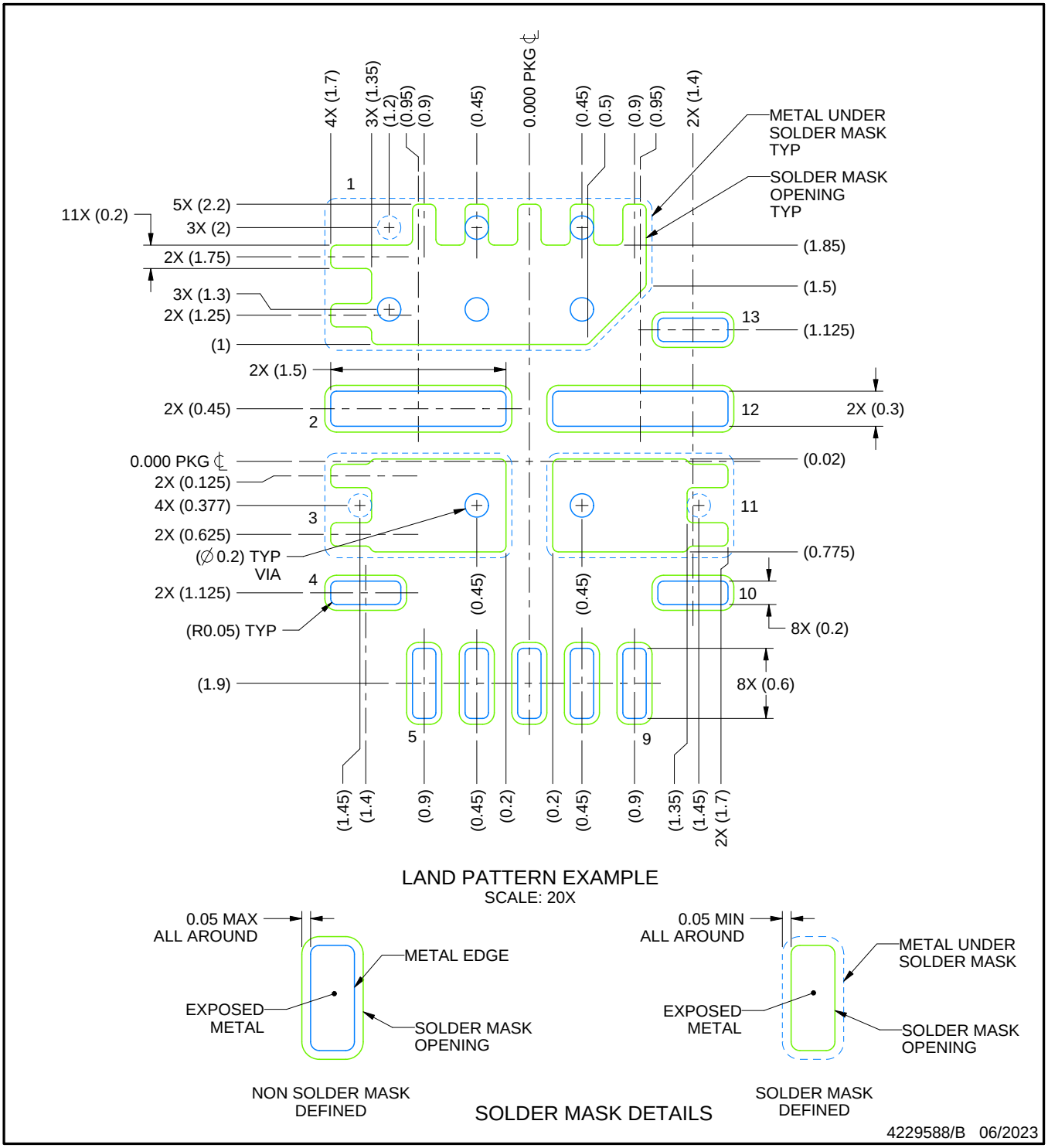
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

VAB0013A

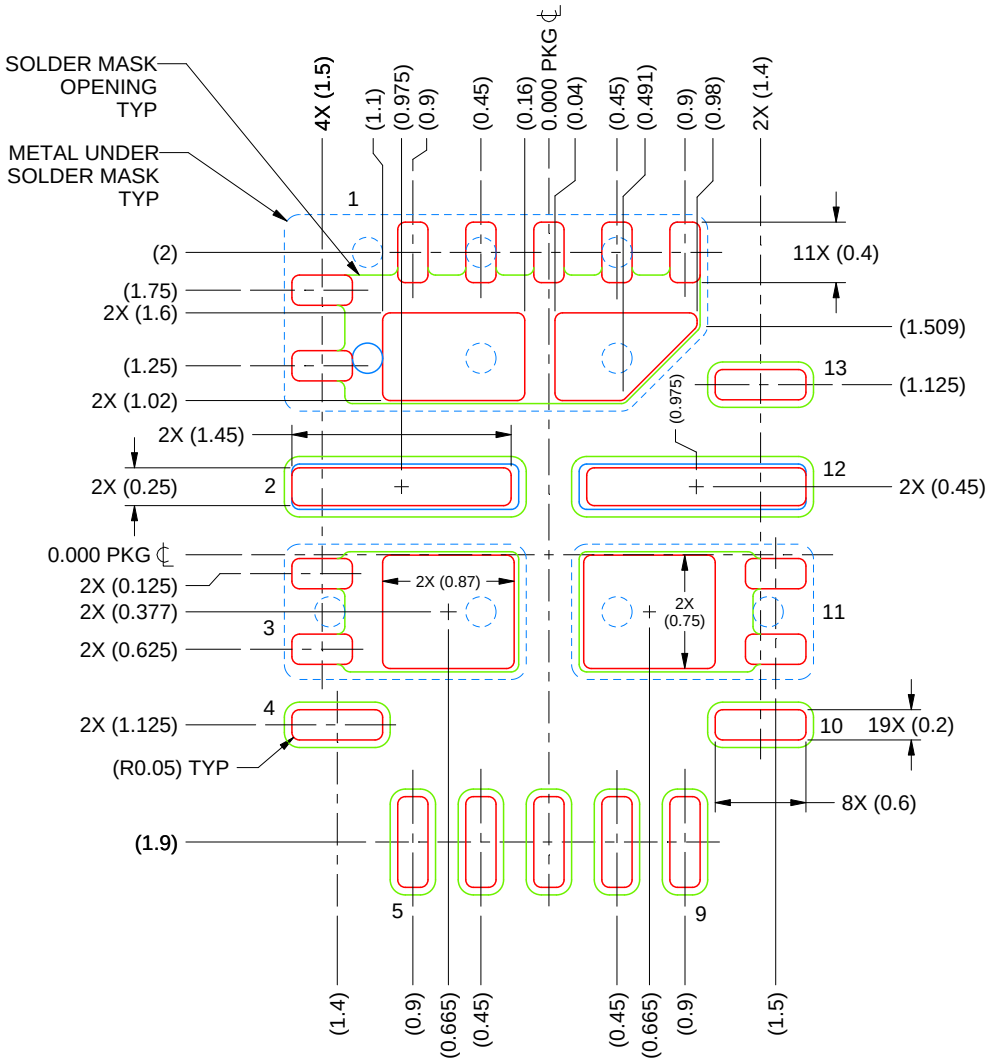
VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 20X

SOLDER COVERAGE BY AREA UNDER PACKAGE
PIN 1: 64%
PIN 2 & 12: 80%
PIN 3 & 11: 77%

4229588/B 06/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月