TPS53119 広入力電圧範囲、Eco-Mode、同期整流降圧型コントローラ

1 特長

- 変換入力電圧範囲: 3V～26V
- VDD 入力電圧範囲：4.5V～25V
- 出力電圧範囲：0.6V～5.5V
- 0.6V (±0.8%) の基準電圧を内蔵
- LDO リニア電圧レギュレータを内蔵
- 自動スキップ Eco-Mode™によって軽負荷時の効率を向上
- D-CAP™モード (負荷ステップ応答 100ns)
- 8 つの周波数設定から選択可能なアダプティブ・オン時間制御アーキテクチャ
- 4700ppm/°C の $R_{DS(on)}$ 電流センシング
- 内部電圧サーボ・ソフト・スタートを 0.7ms、1.4ms、2.8ms、5.6ms から選択可能
- プリチャージ・スタートアップ機能
- 出力放電内蔵
- オープン・ドレインのパワー・グッド出力
- ブースト・スイッチ内蔵
- OVP/UVP/OCP 内蔵
- サーマル・シャットダウン (非ラッチ)
- 3mm×3mmの 16 ピン VQFN (RGT) パッケージ
- WEBENCH® Power Designer により、TPS53119 を使用するカスタム設計を作成

2 アプリケーション

- ストレージ
- サーバー
- 多機能プリンタ
- 組み込みコンピューティング

3 概要

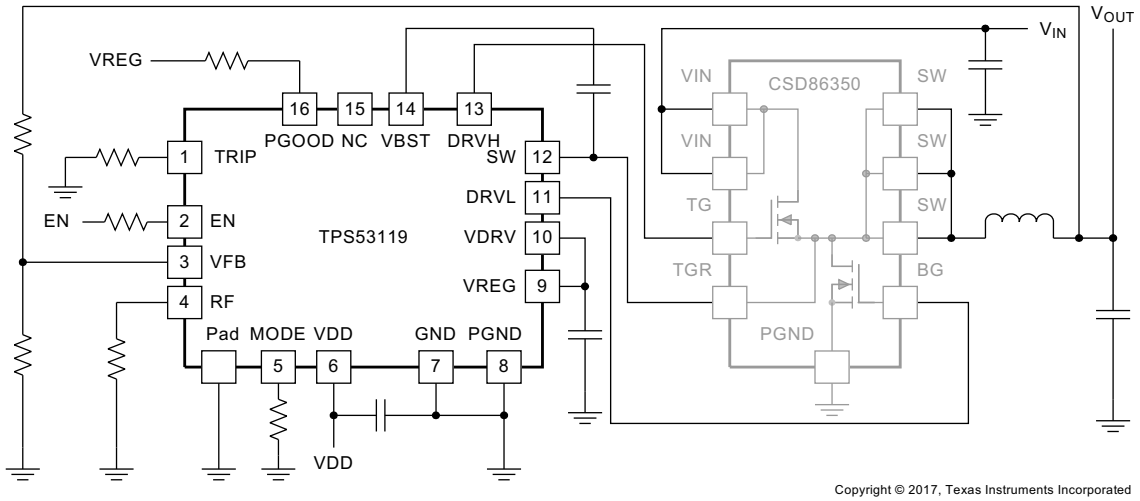
TPS53119デバイスは、アダプティブ・オンタイムD-CAPモード制御に対応した小型のシングル・バック・コントローラです。低出力電圧で高電流のPCシステム電源レールや、民生用デジタル機器で使用される同様のポイント・オブ・ロード(POL)電源に適しています。小型のパッケージと最小限のピン数でPCB上のスペースを削減し、専用のENピンと選択可能な設定済み周波数によって電源設計を簡素化できます。軽負荷状態でのスキップ・モード、強力なゲート・ドライバ、およびローサイドFETの$R_{DS(on)}$電流センシングにより、幅広い負荷範囲にわたって低損失、高効率を実現します。変換入力電圧 (ハイサイド FET のドレイン電圧) の範囲は 4.5V～25V、出力電圧範囲は 0.6V～5.5V です。TPS53119 は 16 ピン VQFN パッケージで供給され、-20℃～+85℃ で仕様が規定されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TPS53119	VQFN (16)	3.00mm×3.00mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

概略回路図



目次

4 改訂履歴

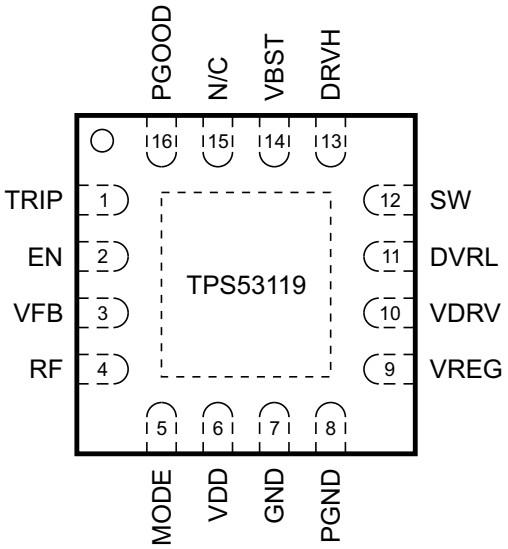
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2017年12月発行のものから更新 **Page**

- WEBENCH へのリンク 追加 ... 1
- Added "Repetitive spikes up to 9 V can be tolerated for up to 50 ns." to Note 2 of *Absolute Maximum Ratings*. ... 4

5 Pin Configuration and Functions

RGT Package
16-Pin VQFN With Exposed Thermal Pad
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
DRVH	13	O	High-side MOSFET driver output. The SW node referenced floating driver. The gate drive voltage is defined by the voltage across VBST to SW node bootstrap flying capacitor.
DRVL	11	O	Synchronous MOSFET driver output. The PGND referenced driver. The gate drive voltage is defined by VDRV voltage.
EN	2	I	Enable pin. Place a 1-kΩ resistor in series with this pin if the source voltage is higher than 5.5 V.
GND	7	G	Ground pin. This is the ground of internal analog circuitry. Connect to GND plane at single point.
MODE	5	I	Soft-start and skip/CCM selection. Connect a resistor to select soft-start time using Table 1. The soft-start time is detected and stored into internal register during start-up.
NC	15	–	No connection.
PAD	–	–	Thermal pad. Use five vias to connect to GND plane.
PGOOD	16	O	Open-drain power-good flag. Provides 1-ms start-up delay after the VFB pin voltage falls within specified limits. When VFB goes out specified limits PGOOD goes low after a 2-µs delay.
PGND	8	G	Power ground. Connect to GND plane.
RF	4	I	Switching frequency selection. Connect a resistor to GND or VREG to select switching frequency using Table 2. The switching frequency is detected and stored during the start-up.
SW	12	P	Output of converted power. Connect this pin to the output inductor.
TRIP	1	I	OCL detection threshold setting pin —10 µA at room temp, 4700 ppm/°C current is sourced and set the OCL trip voltage as follows: $V_{OCL} = V_{TRIP} / 8$ ($V_{TRIP} \leq 3$ V, $V_{OCL} \leq 375$ mV)
VBST	14	P	Supply input for high-side FET gate driver (boost terminal). Connect a capacitor from this pin to SW node. Internally connected to VREG through bootstrap MOSFET switch.
VDD	6	P	Controller power supply input. The input range is from 4.5 V to 25 V.
VDRV	10	I	Gate drive supply voltage input. Connect to VREG if using LDO output as gate-drive supply.
VFB	3	I	Output feedback input. Connect this pin to V_{OUT} through a resistor divider.
VREG	9	O	6.2-V LDO output. This is the supply of internal analog circuitry and driver circuitry.

(1) I=Input, O=Output, P=Power, G=Ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Input voltage	VBST		–0.3	35	V
	VBST(2)		–0.3	7	
	VDD		–0.3	26	
	SW	DC	–2	28	
		Pulse < 20 ns, E = 5 µJ		–7	
	VDRV, EN, TRIP, VFB, RF, MODE		–0.3	7	
Output voltage	DRVH		–2	35	V
	DRVH(2)		–0.3	7	
	DRVL, VREG		–0.5	7	
	PGOOD		–0.3	7	
Junction temperature, T_J				150	°C
Storage temperature, T_{stg}			–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltage values are with respect to the SW terminal. Repetitive spikes up to 9 V can be tolerated for up to 50 ns.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	VBST	–0.1	34.5	V
	VDD	4.5	25	
	SW	–1	28	
	VBST(1)	–0.1	6.5	
	EN, TRIP, VFB, RF, VDRV, MODE	–0.1	6.5	
Output voltage	DRVH	–1	34.5	V
	DRVH(1)	–0.1	6.5	
	DRVL, VREG	–0.3	6.5	
	PGOOD	–0.1	6.5	
Operating free-air temperature, T_A		–20	85	°C

(1) Voltage values are with respect to the SW terminal.

6.4 Thermal Information

THERMAL METRIC[1]		TPS53119 RGT (VQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	51.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	85.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	19.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range, VDD = 12 V (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{VDD}	VDD supply current	VDD current, T_A = 25°C, no load, V_{EN} = 5 V, V_{VFB} = 0.630 V		420	590	µA
I_{VDDSDN}	VDD shutdown current	VDD current, T_A = 25°C, no load, V_{EN} = 0 V			10	µA
INTERNAL REFERENCE VOLTAGE						
V_{VFB}	VFB regulation voltage	VFB voltage, CCM condition[1]		600		mV
V_{VFB}	VFB regulation voltage	T_A = 25°C	597	600	603	mV
		0°C ≤ T_A ≤ 85°C	595.2	600	604.8	
		–20°C ≤ T_A ≤ 85°C	592	600	608	
I_{VFB}	VFB input current	V_{VFB} = 0.63 V, T_A = 25°C		0.002	0.2	µA
OUTPUT DRIVERS						
R_{DRVH}	DRVH resistance	Source, I_{DRVH} = –50 mA		1.5	3	Ω
		Sink, I_{DRVH} = 50 mA		0.7	1.8	
R_{DRVL}	DRVL resistance	Source, I_{DRVL} = –50 mA		1	2.2	Ω
		Sink, I_{DRVL} = 50 mA		0.5	1.2	
t_{DEAD}	Dead time	DRVH-off to DRVL-on	7	17	30	ns
		DRVL-off to DRVH-on	10	22	35	
LDO OUTPUT						
V_{VREG}	LDO output voltage	0 mA ≤ I_{VREG} ≤ 50 mA	5.76	6.2	6.67	V
I_{VREG}	LDO output current[1]	Maximum current allowed from LDO			50	mA
V_{DO}	LDO dropout voltage	V_{VDD} = 4.5 V, I_{VREG} = 50 mA			364	mV
BOOT STRAP SWITCH						
V_{FBST}	Forward voltage	$V_{VREG-VBST}$, I_F = 10 mA, T_A = 25°C		0.1	0.2	V
I_{VBSTLK}	VBST leakagecurrent	V_{VBST} = 23 V, V_{SW} = 17 V, T_A = 25°C		0.01	1.5	µA
DUTY AND FREQUENCY CONTROL						
$t_{OFF(min)}$	Minimum off-time	T_A = 25°C	150	260	400	ns
$t_{ON(min)}$	Minimum ON-time	V_{IN} = 17 V, V_{OUT} = 0.6 V, R_{RF} = 0 Ω to VREG, T_A = 25°C[1]		35		ns
SOFT START						
t_{SS}	Internal soft-start time	0 V ≤ V_{OUT} ≤ 95%, R_{MODE} = 39 kΩ		0.7		ms
		0 V ≤ V_{OUT} ≤ 95%, R_{MODE} = 100kΩ		1.4		
		0 V ≤ V_{OUT} ≤ 95%, R_{MODE} = 200 kΩ		2.8		
		0 V ≤ V_{OUT} ≤ 95%, R_{MODE} = 470 kΩ		5.6		

(1) Ensured by design. Not production tested.

Electrical Characteristics (continued)

over operating free-air temperature range, VDD = 12 V (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
POWER GOOD						
V_{THPG}	PG threshold	PG in from lower	92.5%	96%	98.5%	
		PG in from higher	108%	111%	114%	
		PG hysteresis	2.5%	5%	7.8%	
R_{PG}	PG transistor on-resistance		15	30	50	Ω
$t_{PG(del)}$	PG delay after soft start		0.8	1	1.2	ms
LOGIC THRESHOLD AND SETTING CONDITIONS						
V_{EN}	EN voltage threshold enable	–20°C ≤ T_A ≤ 85°C	1.8			V
		0°C ≤ T_A ≤ 85°C	1.7			
	EN voltage threshold disable				0.5	
I_{EN}	EN input current	V_{EN} = 5 V			1	µA
f_{SW}	Switching frequency	R_{RF} = 0 Ω to GND, T_A = 25°C (2)	200	250	300	kHz
		R_{RF} = 187 kΩ to GND, T_A = 25°C (2)	250	300	350	
		R_{RF} = 619 kΩ to GND, T_A = 25°C (2)	350	400	450	
		R_{RF} = open, T_A = 25°C (2)	450	500	550	
		R_{RF} = 866 kΩ to V_{REG}, T_A = 25°C (2)	580	650	720	
		R_{RF} = 309 kΩ to V_{REG}, T_A = 25°C (2)	670	750	820	
		R_{RF} = 124 kΩ to V_{REG}, T_A = 25°C (2)	770	850	930	
		R_{RF} = 0 Ω to V_{REG}, T_A = 25°C (2)	880	970	1070	
VO DISCHARGE						
I_{Dischg}	VO discharge current	V_{EN} = 0 V, V_{SW} = 0.5 V	5	13		mA
PROTECTION: CURRENT SENSE						
I_{TRIP}	TRIP source current	V_{TRIP} = 1 V, T_A = 25°C	9	10	11	µA
TC_{ITRIP}	TRIP current temp. coef.	T_A = 25°C (1)		4700		ppm/°C
V_{TRIP}	Current limit threshold setting range	$V_{TRIP-GND}$ voltage	0.2		3	V
V_{OCL}	Current limit threshold	V_{TRIP} = 3 V	355	375	395	mV
		V_{TRIP} = 1.6 V	185	200	215	
		V_{TRIP} = 0.2 V	17	25	33	
V_{OCLN}	Negative current limit threshold	V_{TRIP} = 3 V	–406	–375	–355	mV
		V_{TRIP} = 1.6 V	–215	–200	–185	
		V_{TRIP} = 0.2 V	–33	–25	–17	
$V_{AZC(adj)}$	Auto zero cross adjustable range	Positive	3	15		mV
		Negative		–15	–3	
PROTECTION: UVP AND OVP						
V_{OVP}	OVP trip threshold voltage	OVP detect	115%	120%	125%	
$t_{OVP(del)}$	OVP propagation delay time	VFB delay with 50-mV overdrive		1		µs
V_{UVP}	Output UVP trip threshold voltage	UVP detect	65%	70%	75%	
$t_{UVP(del)}$	Output UVP propagation delay time		0.8	1	1.2	ms
$t_{UVP(en)}$	Output UVP enable delay time	from EN to UVP workable, R_{MODE} = 39 kΩ	2	2.55	3	ms
UVLO						
V_{UVVREG}	VREG UVLO threshold	Wake up	4	4.18	4.5	V
		Hysteresis		0.25		
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold	Shutdown temperature (1)		145		°C
		Hysteresis (1)		10		

(2) Not production tested. Test conditions are V_{IN} = 12 V, V_{OUT} = 1.1 V, I_{OUT} = 10 A and using the application circuit shown in Figure 18 and Figure 22.

6.6 Typical Characteristics

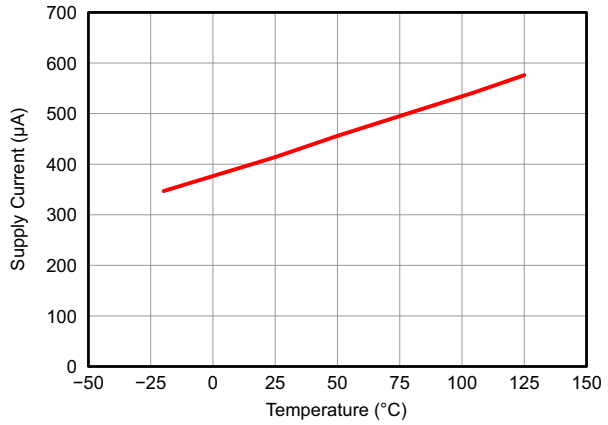


Figure 1. VDD Supply Current vs Temperature

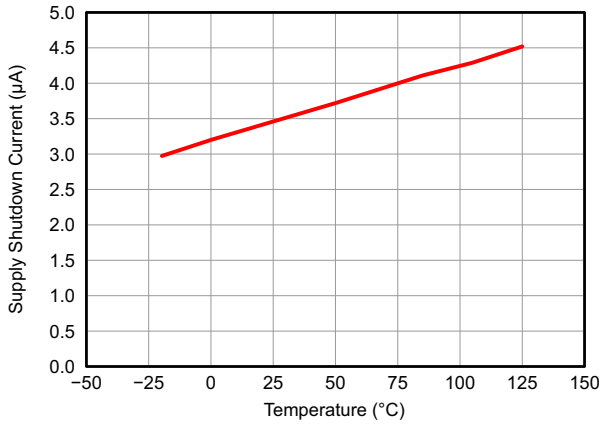


Figure 2. VDD Shutdown Current vs Temperature

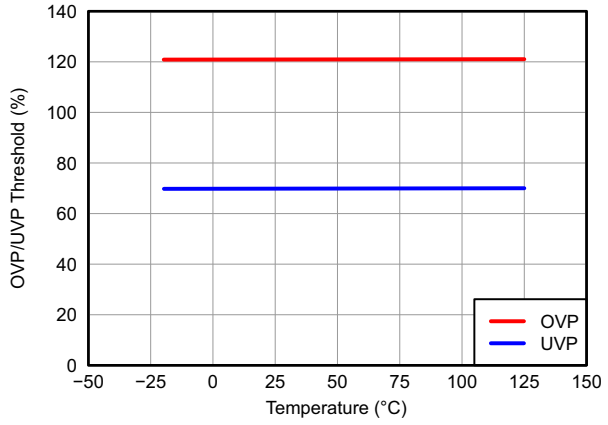


Figure 3. OVP/UVP Threshold vs Temperature

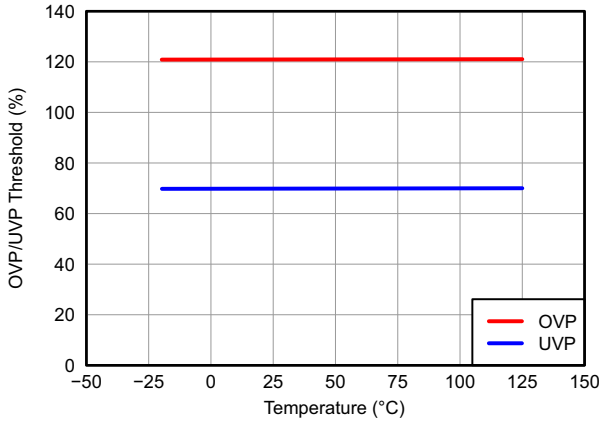


Figure 4. TRIP Pin Current vs Temperature

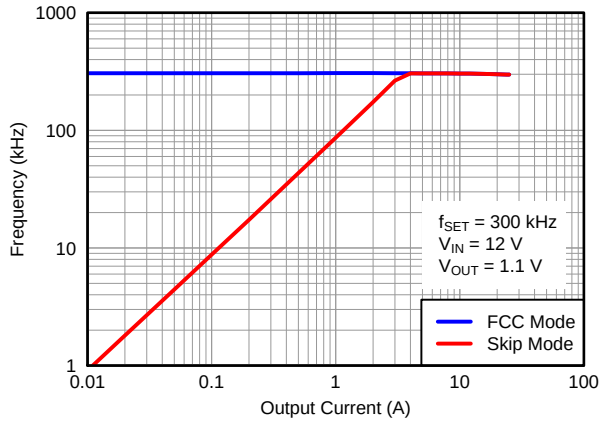


Figure 5. Switching Frequency vs Output Current

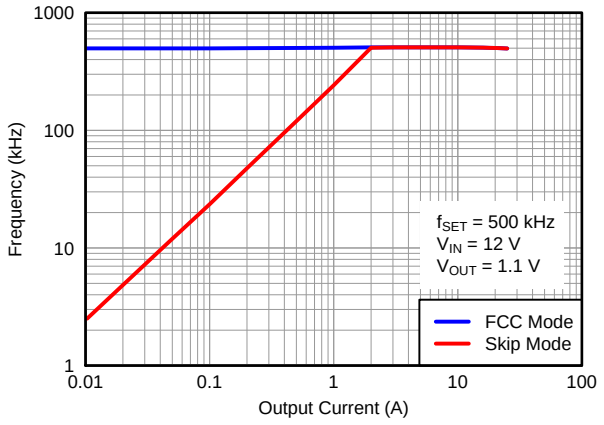


Figure 6. Switching Frequency vs Output Current

Typical Characteristics (continued)

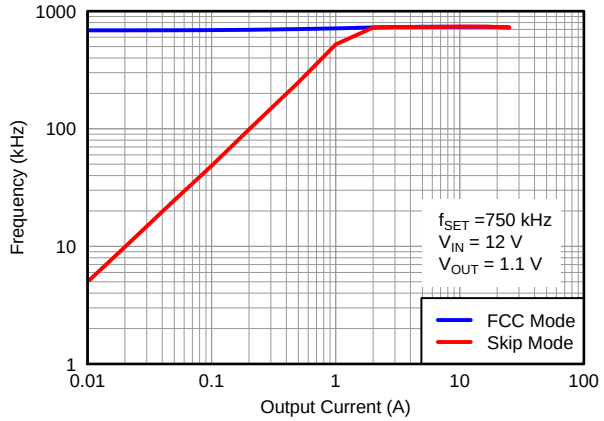


Figure 7. Switching Frequency vs Output Current

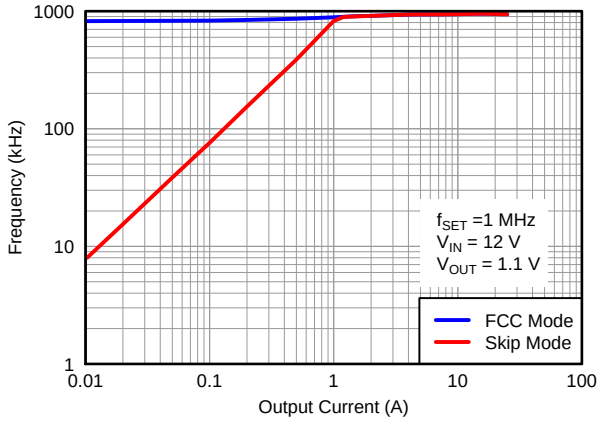


Figure 8. Switching Frequency vs Output Current

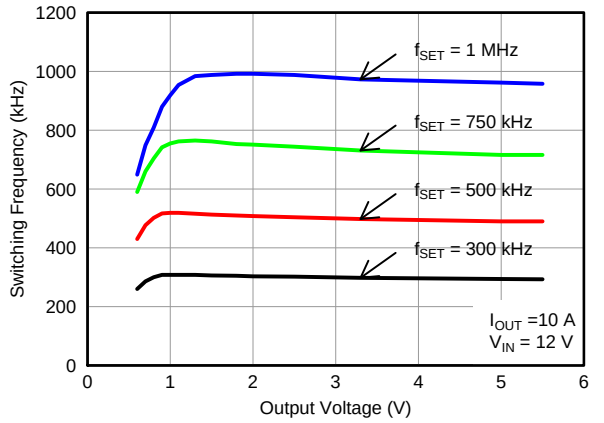


Figure 9. Switching Frequency vs Output Voltage

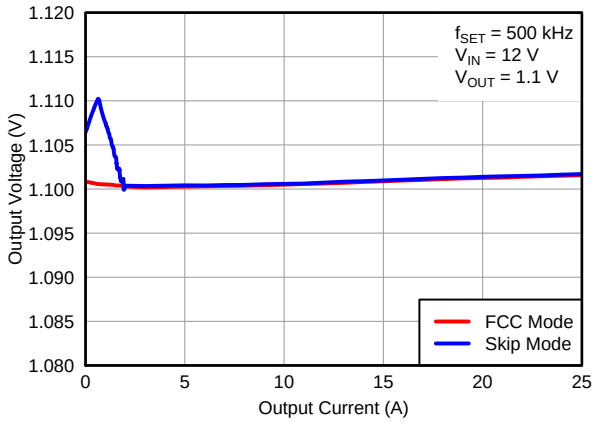


Figure 10. Output Voltage vs Output Current

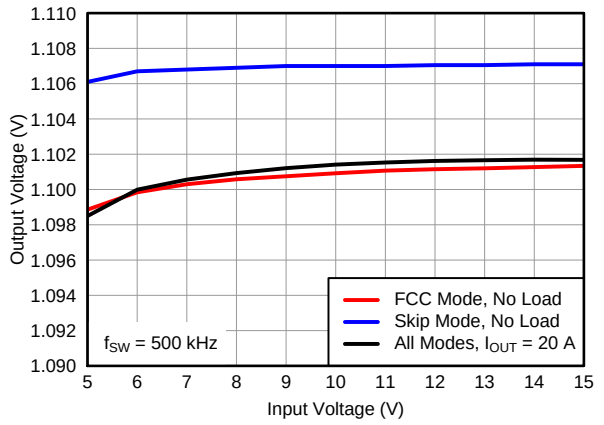


Figure 11. Output Voltage vs Input Voltage

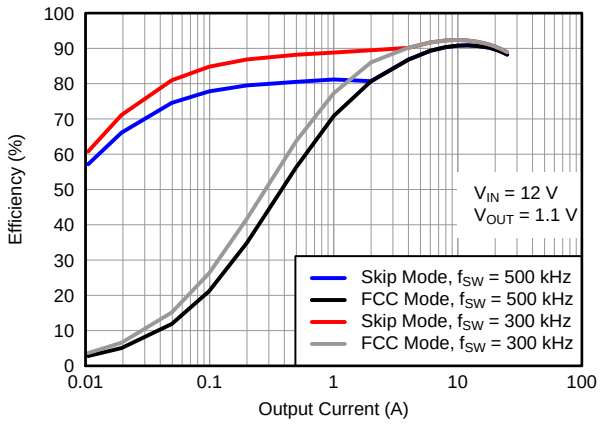


Figure 12. Efficiency vs Output Current

Typical Characteristics (continued)

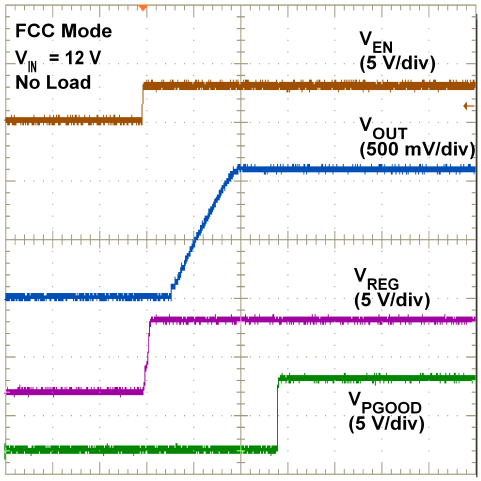


Figure 13. Start-Up Waveform

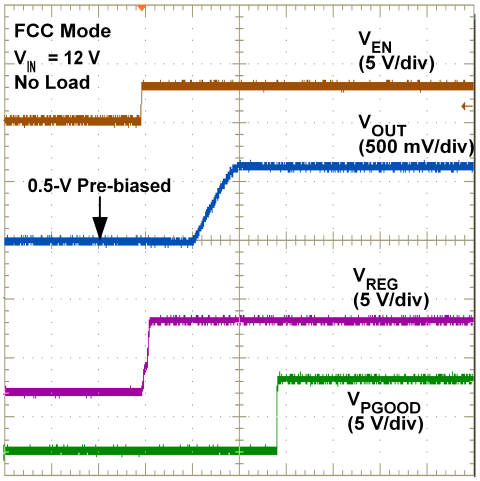


Figure 14. Prebias Start-Up Waveform

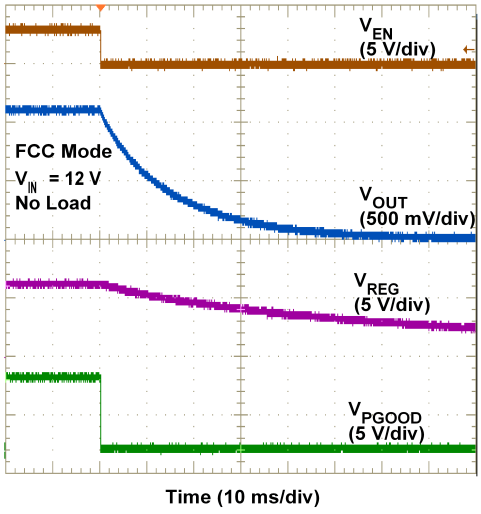


Figure 15. Turnoff Waveform

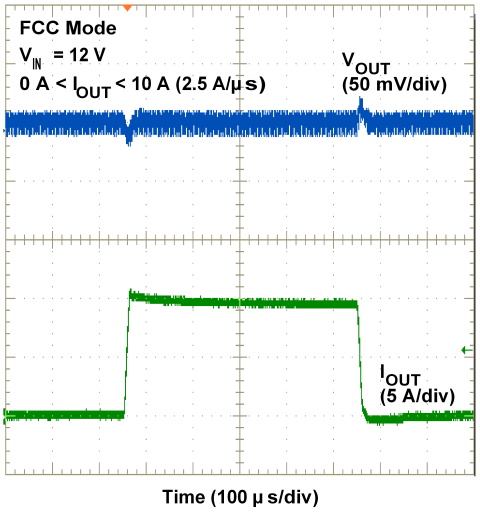


Figure 16. Load Transient Response

7 Detailed Description

7.1 Overview

The TPS53119 is a high-efficiency, single-channel, synchronous buck regulator controller suitable for low output voltage point-of-load applications in computing and similar digital consumer applications. The device features proprietary D-CAP mode control combined with an adaptive ON-time architecture. This combination is ideal for building modern low duty ratio, ultra-fast load step response DC–DC converters. The output voltage ranges from 0.6 V to 5.5 V. The conversion input voltage range is from 3 V up to 26 V. The D-CAP mode uses the ESR of the output capacitors to sense the device current. One advantage of this control scheme is that it does not require an external phase compensation network. This allows a simple design with a low external component count. Eight preset switching frequency values can be chosen using a resistor connected from the RF pin to ground or VREG. Adaptive ON-time control tracks the preset switching frequency over a wide input and output voltage range while allowing the switching frequency to increase at the step-up of the load.

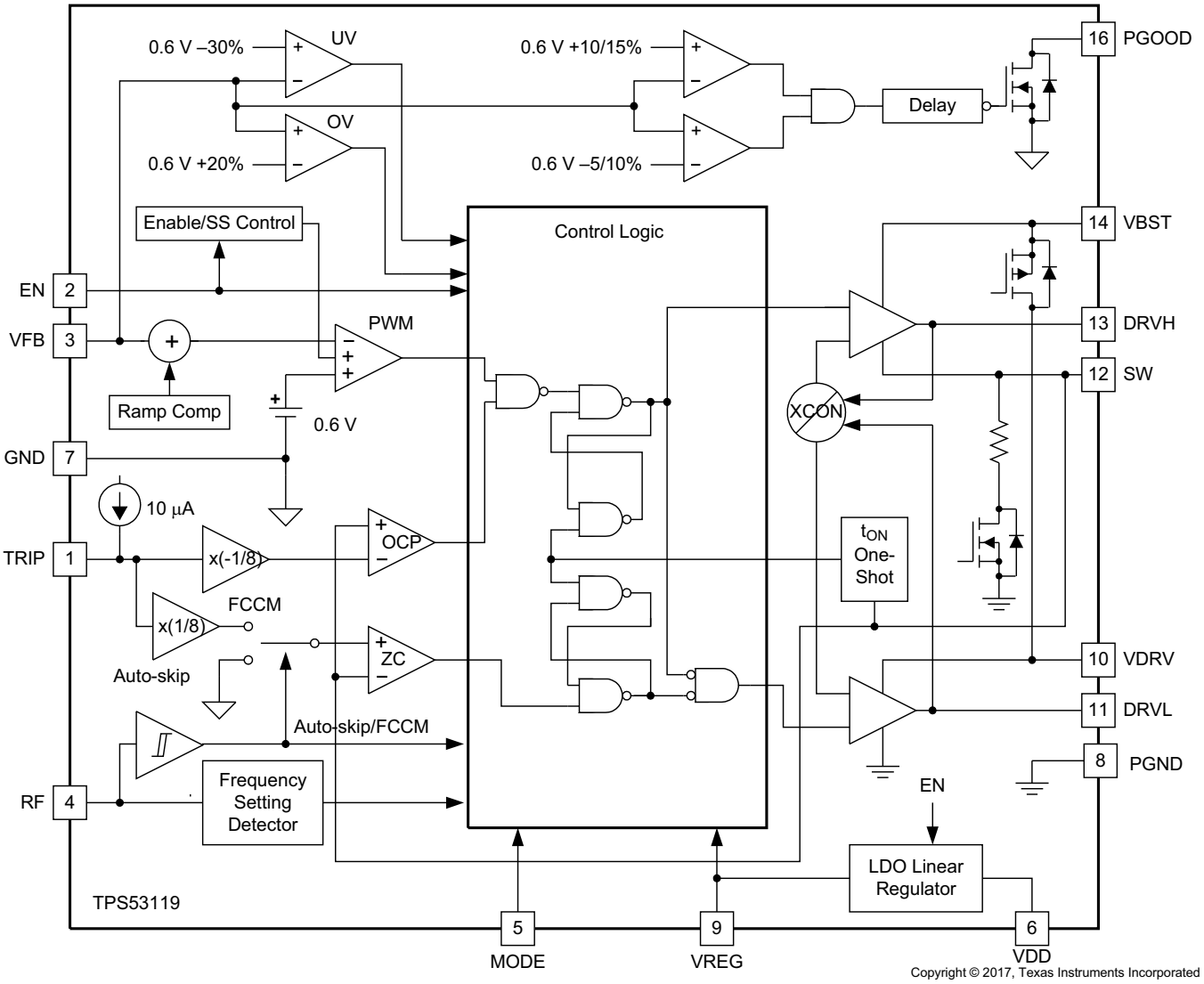
The TPS53119 has a MODE pin to select between auto-skip mode and forced continuous conduction mode (FCCM) for light load conditions. The MODE pin also sets the selectable soft-start time ranging from 0.7 ms to 5.6 ms as shown in Table 1. The strong gate drivers allow low $R_{DS(on)}$ FETs for high-current applications.

When the device starts (either by EN or VDD UVLO), the TPS53119 sends out a current that detects the resistance connected to the MODE pin to determine the soft-start time. After that (and before V_{OUT} starts to ramp up) the MODE pin becomes a high-impedance input to determine skip mode or FCCM mode operation. When the voltage on the MODE pin is higher than 1.3 V, the converter enters into FCCM mode. If the voltage on MODE pin is less than 1.3 V, then the converter operates in skip mode.

TI recommends connection of the MODE pin to the PGOOD pin if FCCM mode is desired. In this configuration, the MODE pin is connected to the GND potential through a resistor when the device is detecting the soft-start time, thus correct soft-start time is used. The device starts up in skip mode and only after the PGOOD pin goes high does the device enter into FCCM mode. When the PGOOD pin goes high there is a transition between skip mode and FCCM. A minimum off-time of 60 ns on DRVL is provided to avoid a voltage spike on the DRVL pin caused by parasitic inductance of the driver loop and gate capacitance of the low-side MOSFET.

For proper operation, the MODE pin must not be connected directly to a voltage source.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable and Soft-Start

When the EN pin voltage rises above the enable threshold voltage (typically 1.4 V), the controller enters its start-up sequence. The internal LDO regulator starts immediately and regulates to 6.2 V at the VREG pin. The controller then uses the first 250 µs to calibrate the switching frequency setting resistance attached to the RF pin and stores the switching frequency code in internal registers. However, switching is inhibited during this phase. In the second phase, an internal DAC starts ramping up the reference voltage from 0 V to 0.6 V. Depending on the MODE pin setting, the ramping up time varies from 0.7 ms to 5.6 ms. Smooth and constant ramp-up of the output voltage is maintained during start-up regardless of load current.

Table 1. Soft-Start and MODE

MODE SELECTION	ACTION	SOFT-START TIME (ms)	R_{MODE} (kΩ)
Auto skip	Pulldown to GND	0.7	39
		1.4	100
		2.8	200
		5.6	475
Forced CCM(1)	Connect to PGOOD	0.7	39
		1.4	100
		2.8	200
		5.6	475

(1) Device goes into forced CCM after PGOOD becomes high.

When the EN voltage is higher than 5.5 V, a 1-kΩ series resistor is needed for the EN pin.

7.3.2 Adaptive ON-Time D-CAP Control and Frequency Selection

The TPS53119 does not have a dedicated oscillator that determines switching frequency. However, the device operates with pseudo-constant frequency by feed-forwarding the input and output voltages into the ON-time one-shot timer. The adaptive ON-time control adjusts the ON-time to be inversely proportional to the input voltage and proportional to the output voltage ($t_{ON} \propto V_{OUT}/V_{IN}$).

This makes the switching frequency fairly constant in steady-state conditions over a wide input voltage range. The switching frequency is selectable from eight preset values by a resistor connected between the RF pin and GND or between the RF pin and the VREG pin as shown in Table 2. Leaving the resistance open sets the switching frequency to 500 kHz.

Table 2. Resistor and Switching Frequency

RESISTOR (R_{RF}) CONNECTIONS	SWITCHING FREQUENCY (kHz)
0 Ω to GND	250
187 kΩ to GND	300
619 kΩ to GND	400
Open	500
866 kΩ to VREG	650
309 kΩ to VREG	750
124 kΩ to VREG	850
0 Ω to VREG	970

The OFF-time is modulated by a PWM comparator. The VFB node voltage (the mid-point of resistor divider) is compared to the internal 0.6-V reference voltage added with a ramp signal. When both signals match, the PWM comparator asserts a *set* signal to terminate the OFF-time (turn off the low-side MOSFET and turn on high-side MOSFET). The *set* signal is valid if the inductor current level is below the OCP threshold, otherwise the off time is extended until the current level falls below the threshold.

7.3.3 Small Signal Model

From small-signal loop analysis, a buck converter using D-CAP mode can be simplified as shown in Figure 17.

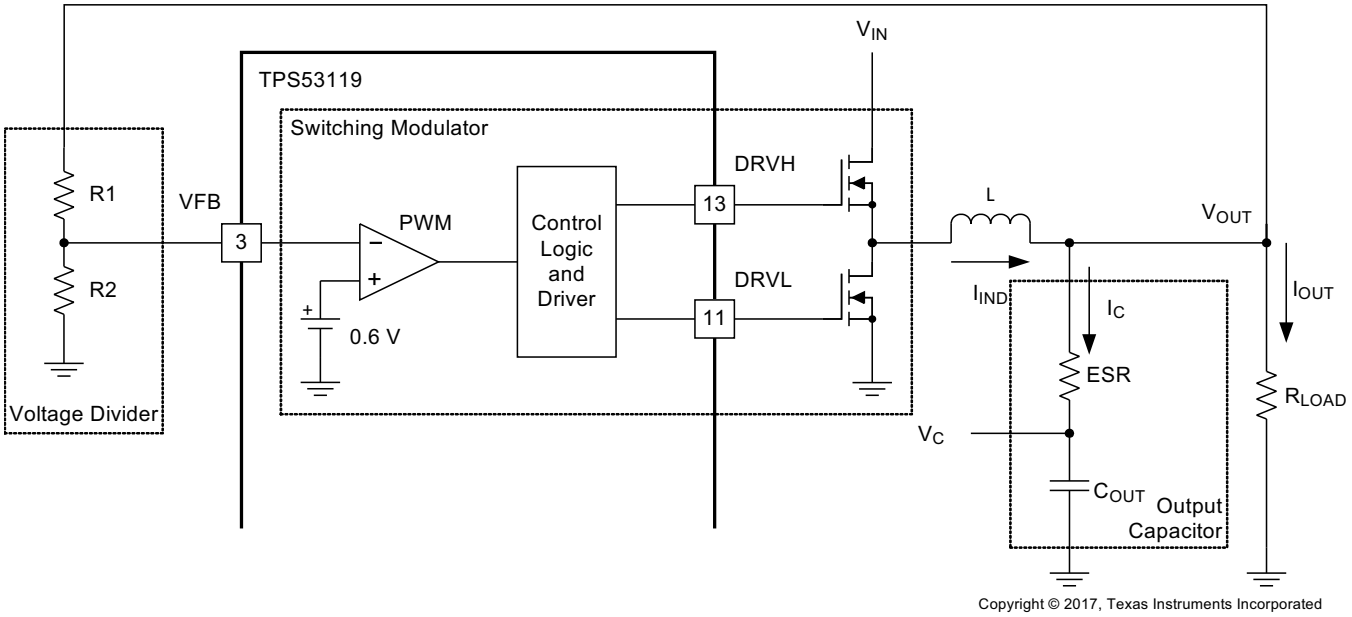


Figure 17. Simplified Modulator Model

The output voltage is compared with the internal reference voltage (ramp signal is ignored here for simplicity). The PWM comparator determines the timing to turn on the high-side MOSFET. The gain and speed of the comparator can be assumed high enough to keep the voltage at the beginning of each on cycle substantially constant.

$$H(s) = \frac{1}{s \times ESR \times C_{OUT}} \quad (1)$$

For the loop stability, the 0-dB frequency, f_0, defined below must be lower than ¼ of the switching frequency.

$$f_0 = \frac{1}{2\pi \times ESR \times C_{OUT}} \leq \frac{f_{SW}}{4} \quad (2)$$

According to Equation 2, the loop stability of D-CAP mode modulator is mainly determined by the capacitor chemistry. For example, specialty polymer capacitors (SP-CAP) have an output capacitance on the order of several 100 µF and ESR in range of 10 mΩ. These yields an f_0 on the order of 100 kHz or less and a more stable loop. However, ceramic capacitors have an f_0 at more than 700 kHz, and require special care when used with this modulator. An application circuit for ceramic capacitor is described in *External Parts Selection With All Ceramic Output Capacitors*.

7.3.4 Ramp Signal

The TPS53119 adds a ramp signal to the 0.6-V reference in order to improve jitter performance. As described in *Small Signal Model*, the feedback voltage is compared with the reference information to keep the output voltage in regulation. By adding a small ramp signal to the reference, the S/N ratio at the onset of a new switching cycle is improved. Therefore the operation becomes less jittery and more stable. The ramp signal is controlled to start with –7 mV at the beginning of an on-cycle and becomes 0 mV at the end of an off-cycle in steady-state.

During skip mode operation, when the switching frequency is lower than 70% of the nominal frequency (because of longer OFF-time), the ramp signal exceeds 0 mV at the end of the OFF-time but is clamped at 3 mV to minimize DC offset.

7.3.5 Adaptive Zero Crossing

The TPS53119 has an adaptive zero crossing circuit which performs optimization of the zero inductor current detection at skip mode operation. This function pursues ideal low-side MOSFET turning off timing and compensates inherent offset voltage of the Z-C comparator and delay time of the Z-C detection circuit. It prevents SW-node swing-up caused by too late detection and minimizes diode conduction period caused by too early detection. As a result, better light load efficiency is delivered.

7.3.6 Output Discharge Control

When EN becomes low, the TPS53119 discharges output capacitor using internal MOSFET connected between the SW pin and the PGND pin while the high-side and low-side MOSFETs are maintained in the *OFF* state. The typical discharge resistance is 40 Ω. The soft discharge occurs only as EN becomes low. After VREG becomes low, the internal MOSFET turns off, and the discharge function becomes inactive.

7.3.7 Low-Side Driver

The low-side driver is designed to drive high-current low-$R_{DS(on)}$ N-channel MOSFETs. The drive capability is represented by its internal resistance, which is 1 Ω for VDRV to DRVL and 0.5 Ω for DRVL to GND. A dead time to prevent shoot through is internally generated between high-side MOSFET off to low-side MOSFET on, and low-side MOSFET off to high-side MOSFET on. The bias voltage VDRV can be delivered from 6.2-V VREG supply or from external power source from 4.5 V to 6.5 V. The instantaneous drive current is supplied by an input capacitor connected between the VDRV and PGND pins.

The average low-side gate drive current is calculated in Equation 3.

$$I_{GL} = C_{GL} \times V_{VDRV} \times f_{SW} \quad (3)$$

When VDRV is supplied by external voltage source, the device continues to be supplied by the VREG pin. There is no internal connection from VDRV to VREG.

7.3.8 High-Side Driver

The high-side driver is designed to drive high current, low $R_{DS(on)}$ N-channel MOSFETs. When configured as a floating driver, the bias voltage is delivered from the VDRV pin supply. The average drive current is calculated using Equation 4.

$$I_{GH} = C_{GH} \times V_{VDRV} \times f_{SW} \quad (4)$$

The instantaneous drive current is supplied by the flying capacitor between VBST and SW pins. The drive capability is represented by internal resistance, which is 1.5 Ω for VBST to DRVH and 0.7 Ω for DRVH to SW.

The driving power which needs to be dissipated from TPS53119 package.

$$P_{DRV} = (I_{GL} + I_{GH}) \times V_{VDRV} \quad (5)$$

7.3.9 Power Good

The TPS53119 has a power-good output that indicates *high* when switcher output is within the target. The power-good function is activated after soft-start has finished. If the output voltage becomes within +10% or –5% of the target value, internal comparators detect power-good state and the power-good signal becomes high after a 1-ms internal delay. If the output voltage goes outside of +15% or –10% of the target value, the power-good signal becomes low after two microsecond (2-µs) internal delay. The power-good output is an open-drain output and must be pulled up externally.

In order for the PGOOD logic to be valid, the VDD input must be higher than 1 V. To avoid invalid PGOOD logic before the TPS53119 is powered up, TI recommends that the PGOOD pin be pulled up to VREG (either directly or through a resistor divider if a different pullup voltage is desired) because VREG remains low when the device is powered off. The pullup resistance can be chosen from a standard resistor value between 1 kΩ and 100 kΩ.

7.3.10 Current Sense and Overcurrent Protection

TPS53119 has cycle-by-cycle overcurrent limiting control. The inductor current is monitored during the *OFF* state and the controller maintains the *OFF* state during the period in that the inductor current is larger than the overcurrent trip level. In order to provide both good accuracy and cost-effective solution, TPS53119 supports temperature compensated MOSFET $R_{DS(on)}$ sensing. The TRIP pin should be connected to GND through the trip voltage setting resistor, R_{TRIP}. The TRIP terminal sources I_{TRIP} current, which is 10 µA typically at room temperature, and the trip level is set to the OCL trip voltage V_{TRIP} as shown in Equation 6.

NOTE

The V_{TRIP} is limited up to approximately 3 V internally.

$$V_{TRIP}\left(mV\right) = R_{TRIP}\left(k\Omega\right) \times I_{TRIP}\left(\mu A\right) \tag{6}$$

The inductor current is monitored by the voltage between GND pin and SW pin so that SW pin should be connected to the drain terminal of the low-side MOSFET properly. I_{TRIP} has 4700-ppm/°C temperature slope to compensate the temperature dependency of the $R_{DS(on)}$. The GND pin is used as the positive current-sensing node. The GND pin should be connected to the proper current sensing device, (for example, the source terminal of the low-side MOSFET.)

As the comparison is done during the *OFF* state, V_{TRIP} sets the valley level of the inductor current. Thus, the load current at the overcurrent threshold, I_{OCP}, can be calculated as shown in Equation 7.

$$I_{OCP} = \frac{V_{TRIP}}{\left(8 \times R_{DS(on)}\right)} + \frac{I_{IND(ripple)}}{2} = \frac{V_{TRIP}}{\left(8 \times R_{DS(on)}\right)} + \frac{1}{2 \times L \times f_{SW}} \times \frac{\left(V_{IN} - V_{OUT}\right) \times V_{OUT}}{V_{IN}} \tag{7}$$

In an overcurrent condition, the current to the load exceeds the current to the output capacitor thus the output voltage tends to fall down. Eventually, it crosses the undervoltage protection threshold and shuts down. After a hiccup delay (16 ms with 0.7-ms sort start), the controller restarts. If the overcurrent condition remains, the procedure is repeated and the device enters hiccup mode.

During the CCM, the negative current limit (NCL) protects the external FET from carrying too much current. The NCL detect threshold is set as the same absolute value as positive OCL but negative polarity.

NOTE

The threshold still represents the valley value of the inductor current.

7.3.11 Overvoltage and Undervoltage Protection

TPS53119 monitors a resistor divided feedback voltage to detect overvoltage and undervoltage. When the feedback voltage becomes lower than 70% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins counting. After 1 ms, TPS53119 latches OFF both high-side and low-side MOSFETs drivers. The controller restarts after a hiccup delay (16 ms with 0.7-ms soft-start). This function is enabled 1.5-ms after the soft-start is completed.

When the feedback voltage becomes higher than 120% of the target voltage, the OVP comparator output goes high and the circuit latches OFF the high-side MOSFET driver and latches ON the low-side MOSFET driver. The output voltage decreases. If the output voltage reaches UV threshold, then both high-side MOSFET and low-side MOSFET driver will be OFF and the device restarts after an hiccup delay. If the OV condition remains, both high-side MOSFET and low-side MOSFET driver remains OFF until the OV condition is removed.

7.3.12 UVLO Protection

The TPS53119 uses VREG undervoltage lockout protection (UVLO). When the VREG voltage is lower than 3.95 V, the device shuts off. When the VREG voltage is higher than 4.2 V, the device restarts. This is non-latch protection.

7.3.13 Thermal Shutdown

The TPS53119 uses temperature monitoring. If the temperature exceeds the threshold value (typically 145°C), the device is shut off. This is non-latch protection.

7.4 Device Functional Modes

7.4.1 Light Load Condition in Auto-Skip Operation

While the MODE pin is pulled low through R_{MODE}, TPS53119 automatically reduces the switching frequency at light load conditions to maintain high efficiency. Detailed operation is described as follows. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to the point that its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The synchronous MOSFET is turned off when this zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode (DCM). The ON-time is kept almost the same as it was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. The transition point to the light load operation $I_{O(LL)}$ (that is, the threshold between continuous and discontinuous conduction mode) can be calculated as shown in Equation 8.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (8)$$

where

- f_{SW} is the PWM switching frequency

Switching frequency versus output current in the light load condition is a function of L, V_{IN} and V_{OUT}, but it decreases almost proportionally to the output current from the $IO_{(LL)}$ given in Equation 8. For example, it is 60 kHz at $IO_{(LL)}$ / 5 if the frequency setting is 300 kHz.

7.4.2 Forced Continuous Conduction Mode

When the MODE pin is tied to PGOOD through a resistor, the controller keeps continuous conduction mode (CCM) in light load condition. In this mode, switching frequency is kept almost constant over the entire load range, which is suitable for applications need tight control of the switching frequency at a cost of lower efficiency.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS53119 device is a small-sized, single-buck controller with adaptive ON-time DCAP mode control.

8.2 Typical Applications

8.2.1 Typical Application With Power Block

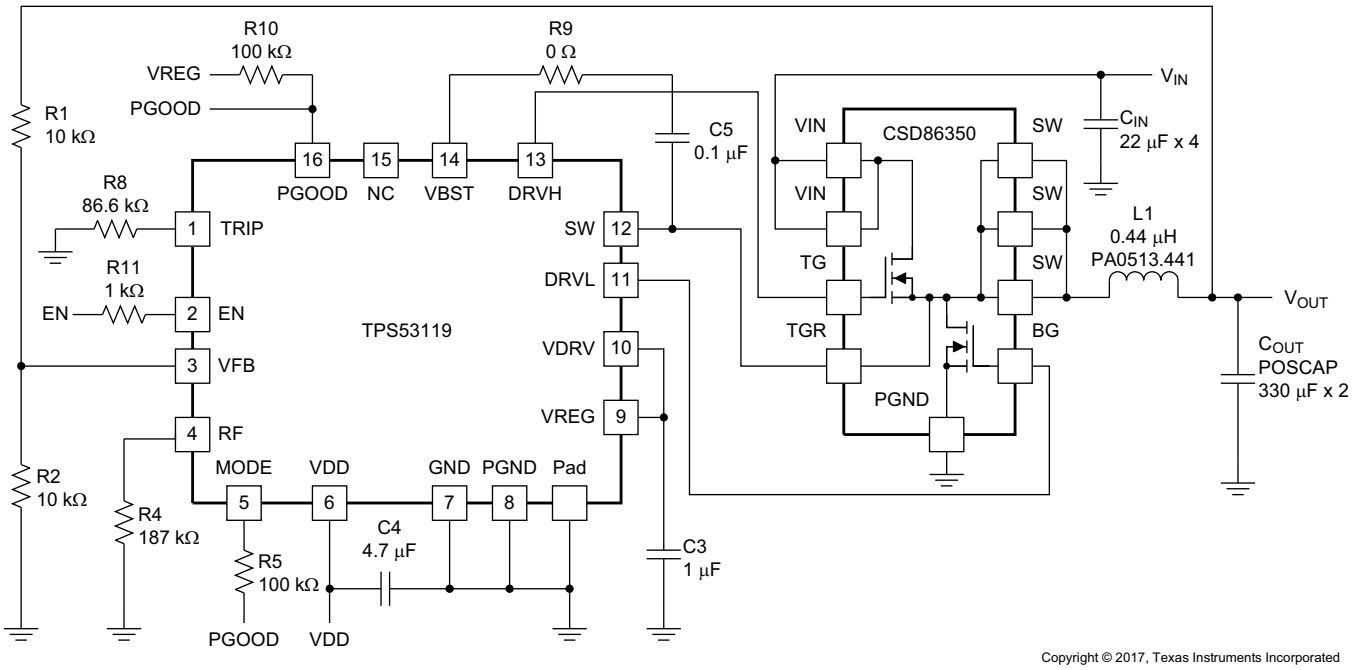


Figure 18. Typical Application Circuit Diagram With Power Block

Typical Applications (continued)

8.2.1.1 Design Requirements

This design uses the parameters listed in Table 3.

Table 3. Design Specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{IN}	Voltage range		5	12	18	V
I_{MAX}	Maximum input current	V_{IN} = 5 V, I_{OUT} = 25 A		10		A
	No load input current	V_{IN} = 12 V, I_{OUT} = 0 A with auto-skip mode		1		mA
OUTPUT CHARACTERISTICS						
V_{OUT}	Output voltage			1.2		V
	Output voltage regulation	Line regulation, 5 V ≤ V_{IN} ≤ 14 V with FCCM		0.2%		
		Load regulation, V_{IN} = 12 V, 0 A ≤ I_{OUT} ≤ 25 A with FCCM		0.5%		
V_{RIPPLE}	Output voltage ripple	V_{IN} = 12 V, I_{OUT} = 25 A with FCCM		10		mV_{PP}
I_{LOAD}	Output load current		0		25	A
I_{OVER}	Output overcurrent			32		
t_{SS}	Soft-start time			1		ms
SYSTEMS CHARACTERISTICS						
f_{SW}	Switching frequency			500		kHz
η	Peak efficiency	V_{IN} = 12 V, V_{OUT} = 1.2 V, I_{OUT} = 4 A		91%		
	Full load efficiency	V_{IN} = 12 V, V_{OUT} = 1.2 V, I_{OUT} = 8 A		91.5%		
T_A	Operating temperature			25		°C

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS53119 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.1.2.2 External Components Selection

Selecting external components is a simple process using D-CAP mode.

1. Choose the Inductor

   The inductance should be determined to give the ripple current of approximately ¼ to ½ of maximum output current. Larger ripple current increases output ripple voltage and improves the signal-to-noise ratio and helps stable operation.

$$L = \frac{1}{I_{IND(ripple)} \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} = \frac{3}{I_{OUT(max)} \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} \quad (9)$$

   The inductor also requires a low DCR to achieve good efficiency. It also requires enough room above the peak inductor current before saturation. The peak inductor current can be estimated in Equation 10.

$$I_{IND(peak)} = \frac{V_{TRIP}}{8 \times R_{DS(on)}} + \frac{1}{L \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} \quad (10)$$

2. Choose the Output Capacitor

   When organic semiconductor capacitors or specialty polymer capacitors are used, for loop stability, capacitance and ESR should satisfy Equation 2. For jitter performance, Equation 11 is a good starting point to determine ESR.

$$ESR = \frac{V_{OUT} \times 10\,mV \times (1 - D)}{0.6\,V \times I_{IND(ripple)}} = \frac{10\,mV \times L \times f_{SW}}{0.6\,V} = \frac{L \times f_{SW}}{60} \ (\Omega) \quad (11)$$

   where

   - D is the duty factor
   - the required output ripple slope is approximately 10 mV per t_{SW} (switching period) in terms of VFB terminal voltage

3. Determine the Value of R1 and R2

   The output voltage is programmed by the voltage-divider resistor, R1 and R2 shown in Figure 17. R1 is connected between the VFB pin and the output, and R2 is connected between the VFB pin and GND. Recommended R2 value is between 10 kΩ and 20 kΩ. Determine R1 using Equation 12.

$$R1 = \frac{V_{OUT} - \left(\frac{I_{IND(ripple)} \times ESR}{2}\right) - 0.6}{0.6} \times R2 \quad (12)$$

8.2.1.3 Application Curves

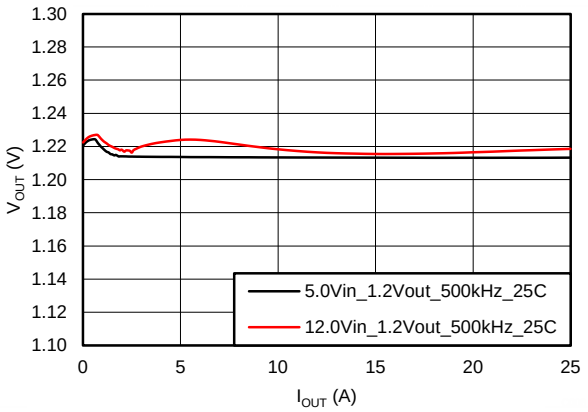


Figure 19. Load Regulation Performance

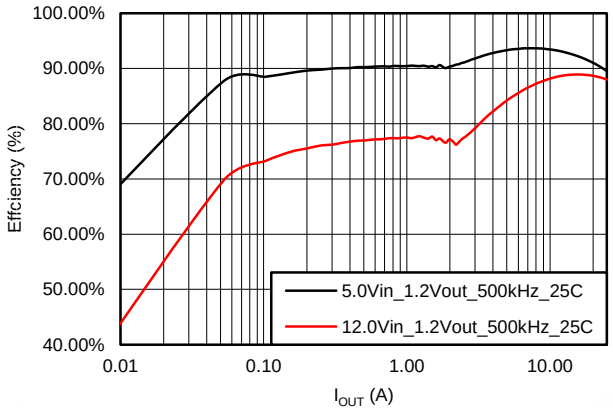


Figure 20. Efficiency Performance

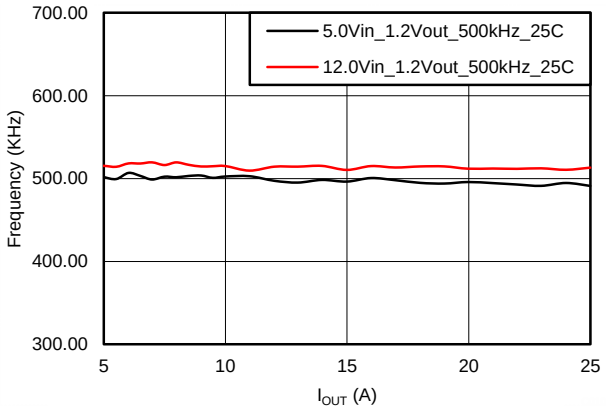


Figure 21. Switching Frequency Performance

8.2.2 Typical Application With Ceramic Output Capacitors

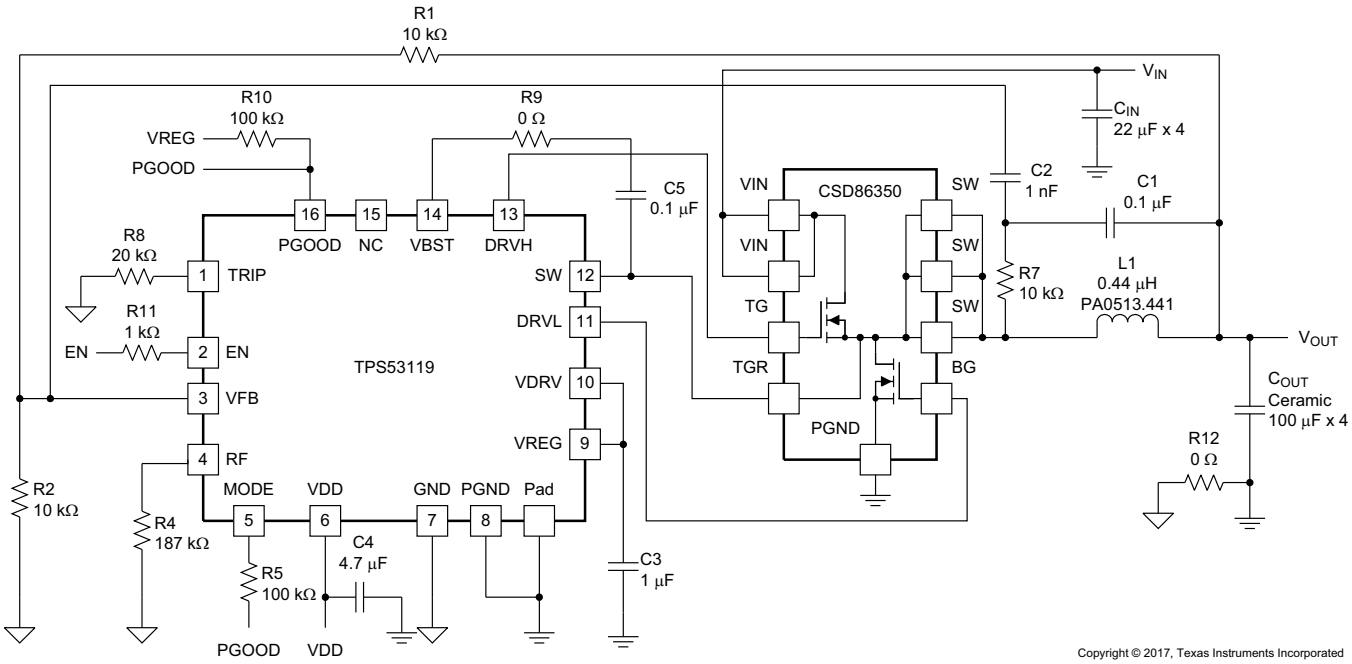


Figure 22. Typical Application Circuit Diagram With Ceramic Output Capacitors

8.2.2.1 Design Requirements

This design uses the parameters listed in Table 4.

Table 4. Design Specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{IN}	Voltage range		5	12	18	V
I_{MAX}	Maximum input current	V_{IN} = 5 V, I_{OUT} = 8 A		2.5		A
	No load input current	V_{IN} = 12 V, I_{OUT} = 0 A with auto-skip mode		1		mA
OUTPUT CHARACTERISTICS						
V_{OUT}	Output voltage			1.2		V
	Output voltage regulation	Line regulation, 5 V ≤ V_{IN} ≤ 14 V with FCCM		0.2%		
		Load regulation, V_{IN} = 12 V, 0 A ≤ I_{OUT} ≤ 8 A with FCCM		0.5%		
V_{RIPPLE}	Output voltage ripple	V_{IN} = 12 V, I_{OUT} = 8 A with FCCM		10		mV_{PP}
I_{LOAD}	Output load current		0		8	A
I_{OVER}	Output overcurrent			25		
t_{SS}	Soft-start time			1		ms
SYSTEMS CHARACTERISTICS						
f_{SW}	Switching frequency			500	1000	kHz
η	Peak efficiency	V_{IN} = 12 V, V_{OUT} = 1.2 V, I_{OUT} = 4 A		91%		
	Full load efficiency	V_{IN} = 12 V, V_{OUT} = 1.2 V, I_{OUT} = 8 A		91.5%		
T_A	Operating temperature			25		°C

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 External Parts Selection With All Ceramic Output Capacitors

When a ceramic output capacitor is used, the stability criteria in Equation 2 cannot be satisfied. The ripple injection approach as shown in Figure 22 is implemented to increase the ripple on the VFB pin and make the system stable. C2 can be fixed at 1 nF. The value of C1 can be selected between 10 nF to 200 nF.

The increased ripple on the VFB pin causes the increase of the VFB DC value. The AC ripple coupled to the VFB pin has two components, one coupled from SW node and the other coupled from V_{OUT} and they can be calculated using Equation 13 and Equation 14.

$$V_{INJ(SW)} = \frac{(V_{IN} - V_{OUT})}{R7 \times C1} \times \frac{D}{f_{SW}} \quad (13)$$

$$V_{INJ(OUT)} = ESR \times I_{IND(ripple)} + \frac{I_{IND(ripple)}}{8 \times C_{OUT} \times f_{SW}} \quad (14)$$

The DC value of VFB can be calculated by Equation 15.

$$V_{FB} = 0.6 + \frac{\left(V_{INJ(SW)} + V_{INJ(OUT)}\right)}{2} \quad (15)$$

And the resistor divider value can be determined by Equation 16.

$$R1 = \frac{(V_{OUT} - V_{FB})}{V_{FB}} \times R2 \quad (16)$$

8.2.2.3 Application Curves

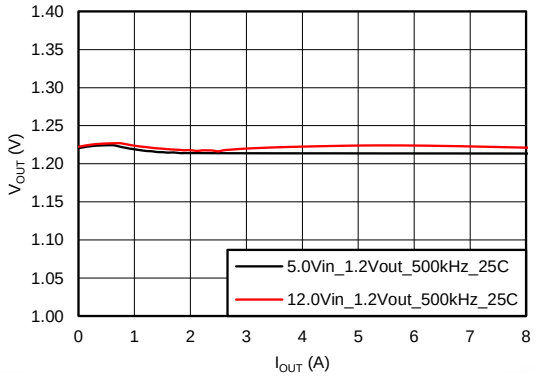


Figure 23. Load Regulation Performance

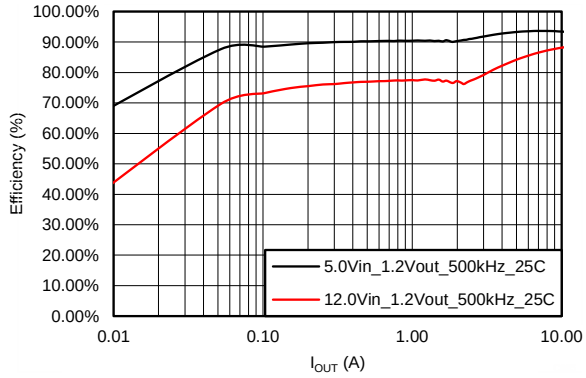


Figure 24. Efficiency Performance

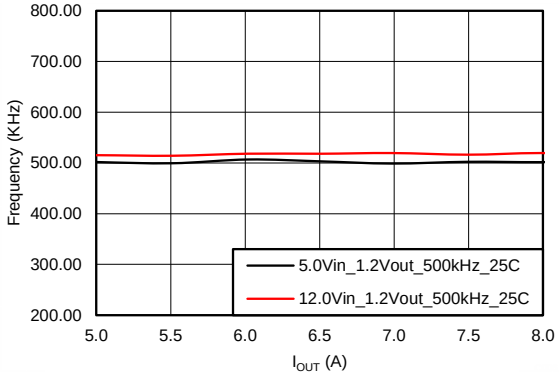


Figure 25. Switching Frequency Performance

9 Power Supply Recommendations

The TPS53119 is a small-sized single-buck controller with adaptive ON-time D-CAP mode control. The device is suitable for low output voltage, high current, PC system power rail and similar point-of-load (POL) power supplies in digital consumer products.

10 Layout

10.1 Layout Guidelines

Certain points must be considered before starting a layout work using the TPS53119.

- Inductors, V_{IN} capacitors, V_{OUT} capacitors and MOSFETs are the power components and must be placed on one side of the PCB (solder side). Place other small signal components on another side (component side). Insert at least one inner plane, connected to power ground, in order to shield and isolate the small signal traces from noisy power lines.
- Place all sensitive analog traces and components such as VFB, PGOOD, TRIP, MODE, and RF away from high-voltage switching nodes such as SW, DRVL, DRVH or VBST to avoid coupling. Use internal layers as ground planes and shield feedback trace from power traces and components.
- The DC–DC converter has several high-current loops. The area of these loops must be minimized in order to suppress generating switching noise.
  - The most important loop to minimize the area of is the path from the V_{IN} capacitors through the high and low-side MOSFETs, and back to the capacitors through ground. Connect the negative node of the V_{IN} capacitors and the source of the low-side MOSFET at ground as close as possible.
  - The second important loop is the path from the low-side MOSFET through inductor and V_{OUT} capacitors, and back to source of the low-side MOSFET through ground. Connect source of the low-side MOSFET and negative node of VOUT capacitors at ground as close as possible.
  - The third important loop is of gate driving system for the low-side MOSFET. To turn on the low-side MOSFET, high current flows from VDRV capacitor through gate driver and the low-side MOSFET, and back to negative node of the capacitor through ground. To turn off the low-side MOSFET, high current flows from gate of the low-side MOSFET through the gate driver and PGND of the device, and back to source of the low-side MOSFET through ground. Connect negative node of VDRV capacitor, source of the low-side MOSFET and PGND of the device at ground as close as possible.
- Because the TPS53119 controls output voltage referring to voltage across V_{OUT} capacitor, the high-side resistor of the voltage divider should be connected to the positive node of V_{OUT} capacitor at the regulation point. Connect the low-side resistor to the GND (analog ground of the device). The trace from these resistors to the VFB pin must be short and thin. Place on the component side and avoid vias between these resistors and the device.
- Connect the overcurrent setting resistors from the TRIP pin to GND and make the connections as close as possible to the device. The trace from TRIP pin to resistor and from resistor to GND should avoid coupling to a high-voltage switching node.
- Connect the frequency setting resistor from RF pin to GND, or to the PGOOD pin and make the connections as close as possible to the device. The trace from the RF pin to the resistor and from the resistor to GND should avoid coupling to a high-voltage switching node.
- Connect all GND (analog ground of the device) trace together and connect to power ground or ground plane with a single via or trace or through a 0-Ω resistor at a quiet point
- Connections from gate drivers to the respective gate of the high-side or the low-side MOSFET should be as short as possible to reduce stray inductance. Use 0.65 mm (25 mils) or wider traces of at least 0.5 mm (20 mils) diameter along this trace.
- The PCB trace defined as switch node, which connects to source of high-side MOSFET, drain of low-side MOSFET, and high-voltage side of the inductor, must be as short and wide as possible.
- Connect the ripple injection V_{OUT} signal (V_{OUT} side of the C1 capacitor in Figure 22) from the terminal of ceramic output capacitor. The AC-coupling capacitor (C7 in Figure 22) can be placed near the device.

10.2 Layout Example

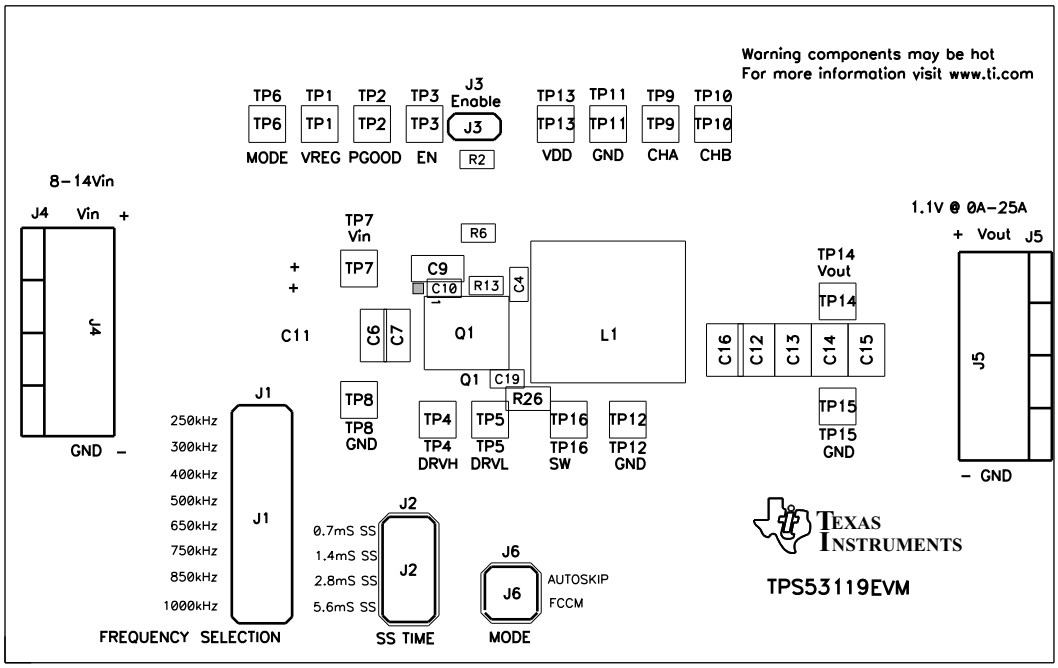


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Figure 26. TPS53119EVM-690 Top Layer Assembly Drawing, Top View

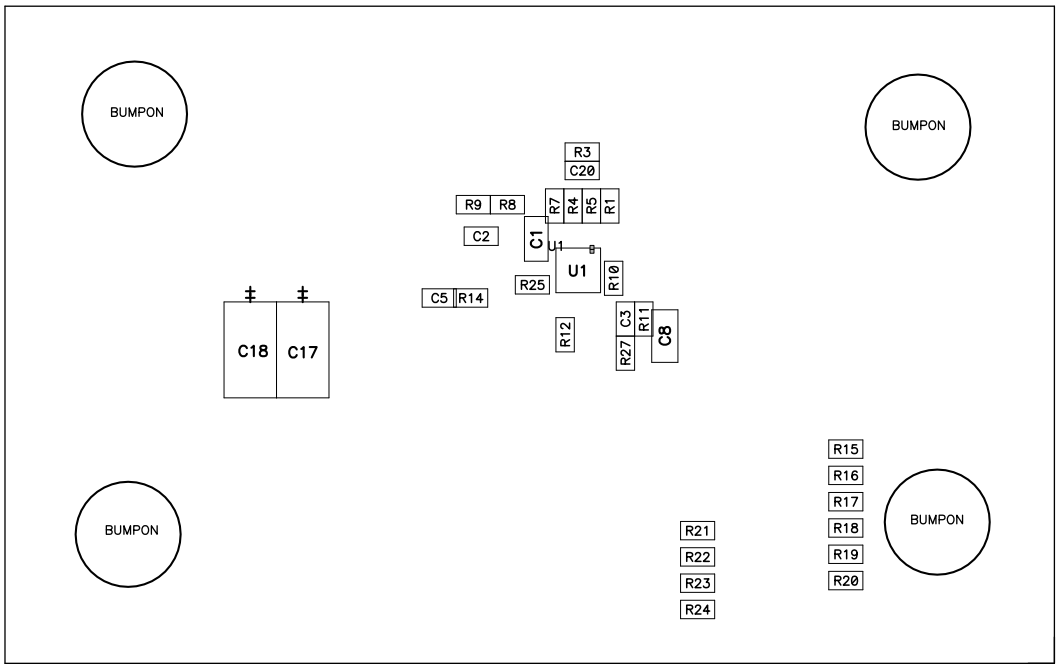

Figure 27. TPS53119EVM-690 Bottom Assembly Drawing, Bottom View

Layout Example (continued)

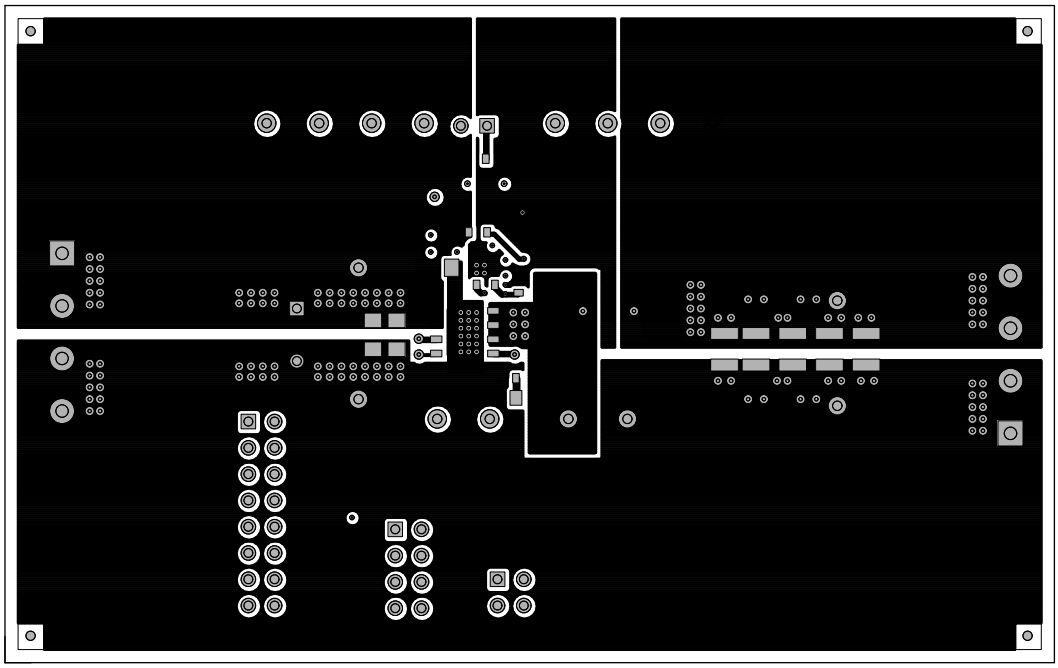

Figure 28. TPS53119EVM-690 Top Copper, Top View

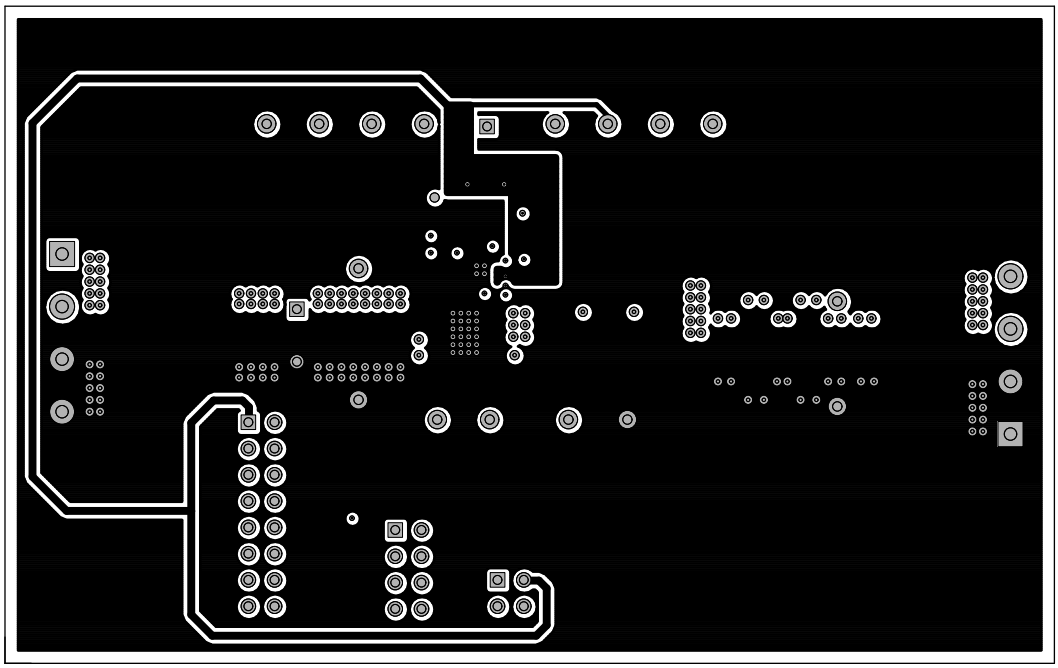

Figure 29. TPS53119EVM-690 Layer-2 Copper, Top View

Layout Example (continued)

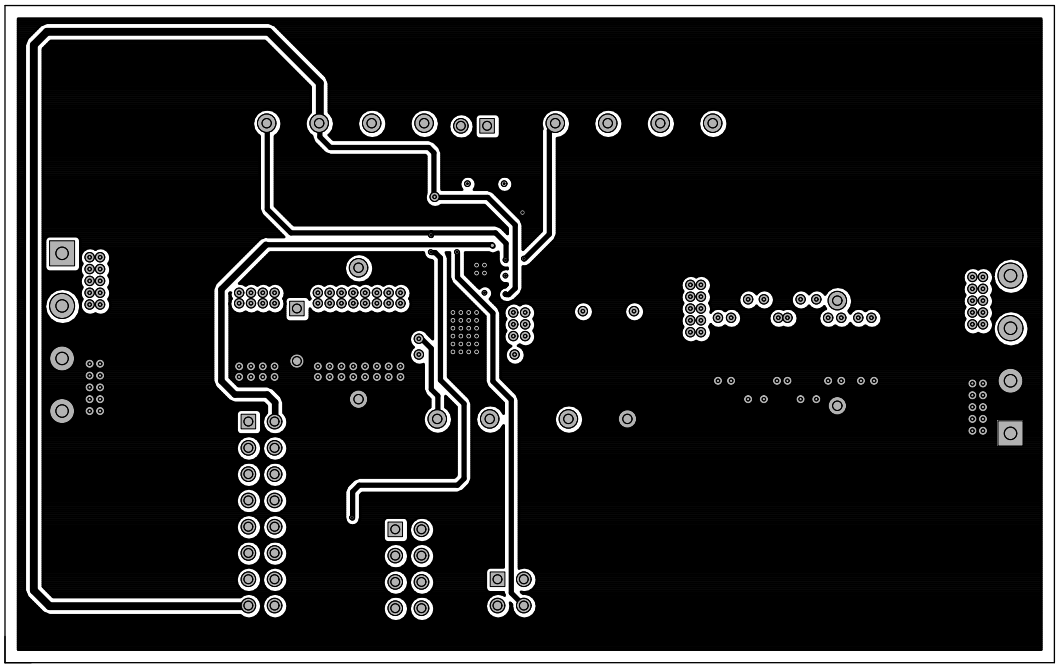

Figure 30. TPS53119EVM-690 Layer-3 Copper, Top View

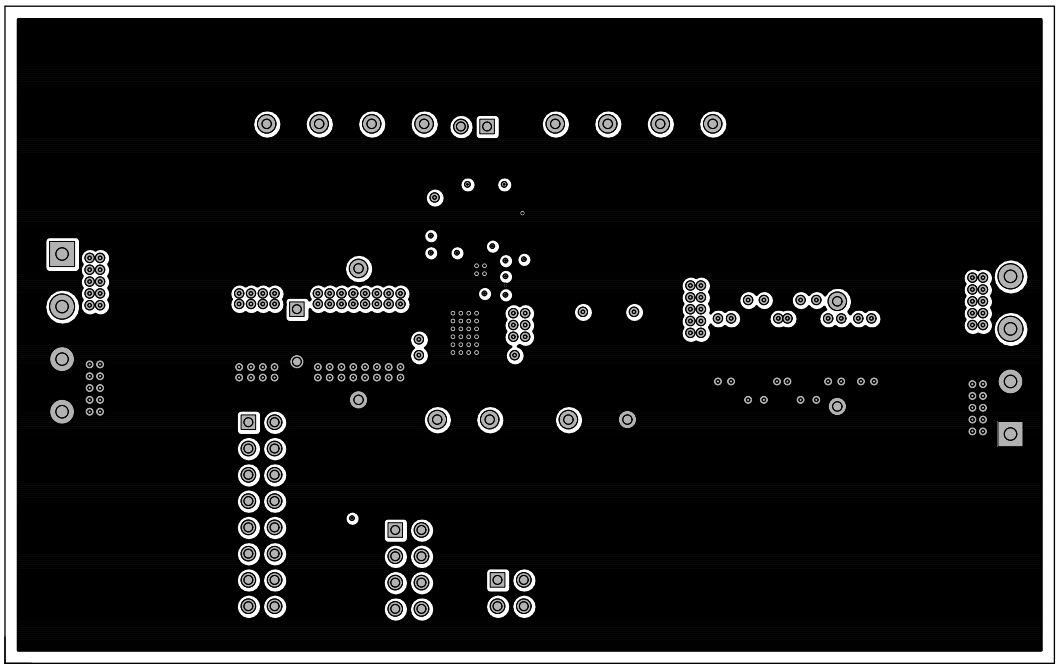

Figure 31. TPS53119EVM-690 Layer-4 Copper, Top View

Layout Example (continued)

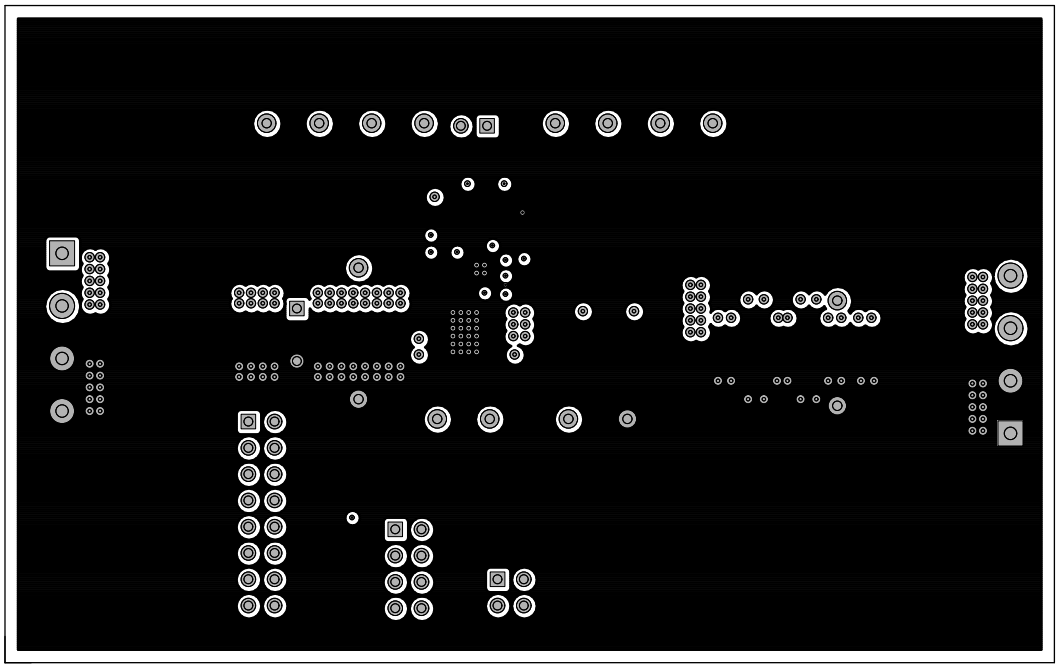

Figure 32. TPS53119EVM-690 Layer-5 Copper, Top View

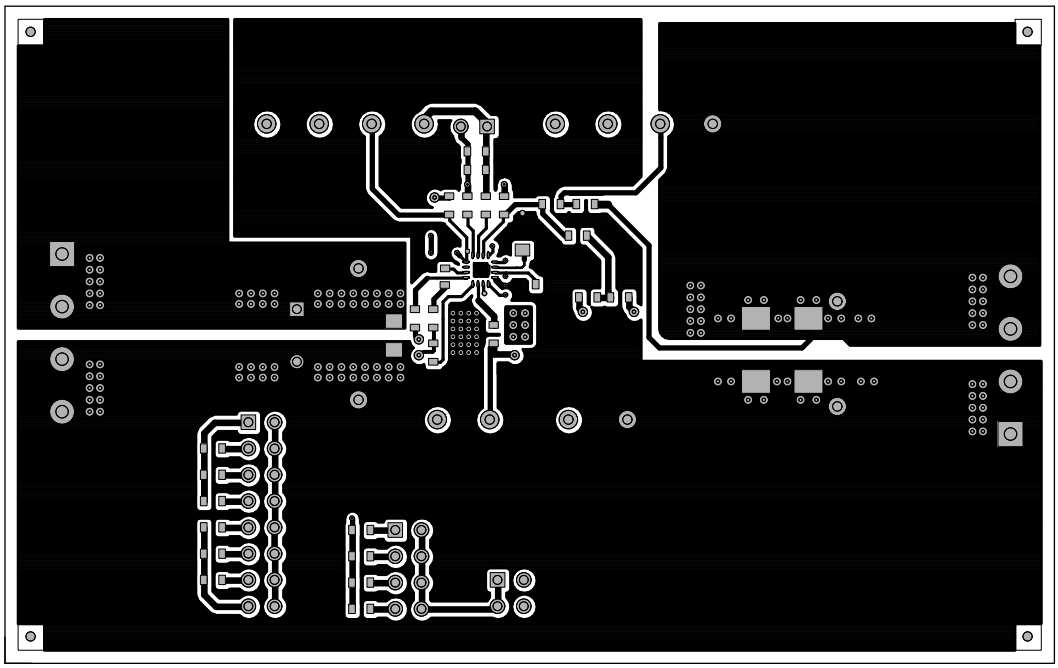

Figure 33. TPS53119EVM-690 Bottom Layer Copper, Top View

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 開発サポート

11.1.1.1 WEBENCH®ツールによるカスタム設計

ここをクリックすると、WEBENCH® Power Designer により、TPS53119 デバイスを使用するカスタム設計を作成できます。

1. 最初に、入力電圧(V_{IN})、出力電圧(V_{OUT})、出力電流(I_{OUT})の要件を入力します。
2. オプティマイザのダイヤルを使用して、効率、占有面積、コストなどの主要なパラメータについて設計を最適化します。
3. 生成された設計を、テキサス・インスツルメンツが提供する他の方式と比較します。

WEBENCH Power Designerでは、カスタマイズされた回路図と部品リストを、リアルタイムの価格と部品の在庫情報と併せて参照できます。

通常、次の操作を実行可能です。

- 電気的なシミュレーションを実行し、重要な波形と回路の性能を確認する。
- 熱シミュレーションを実行し、基板の熱特性を把握する。
- カスタマイズされた回路図やレイアウトを、一般的なCADフォーマットで出力する。
- 設計のレポートをPDFで印刷し、設計を共有する。

WEBENCHツールの詳細は、www.ti.com/WEBENCHでご覧になれます。

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS53119RGTR	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-20 to 85	53119
TPS53119RGTR.A	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-20 to 85	53119
TPS53119RGTT	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-20 to 85	53119
TPS53119RGTT.A	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-20 to 85	53119

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

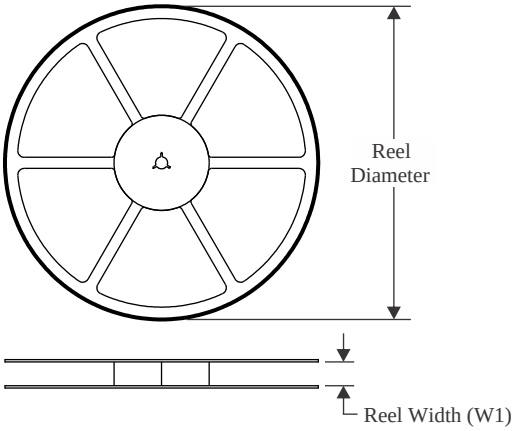
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

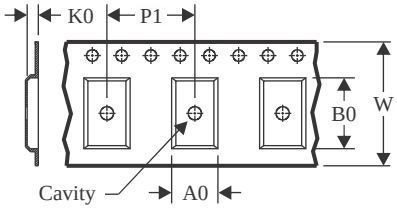
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

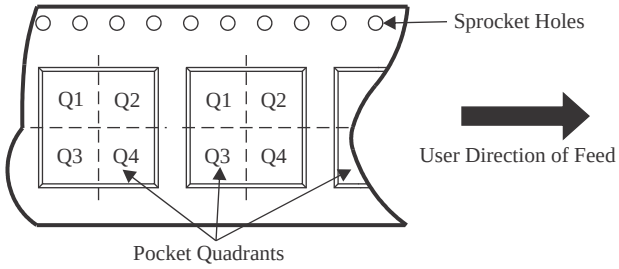


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

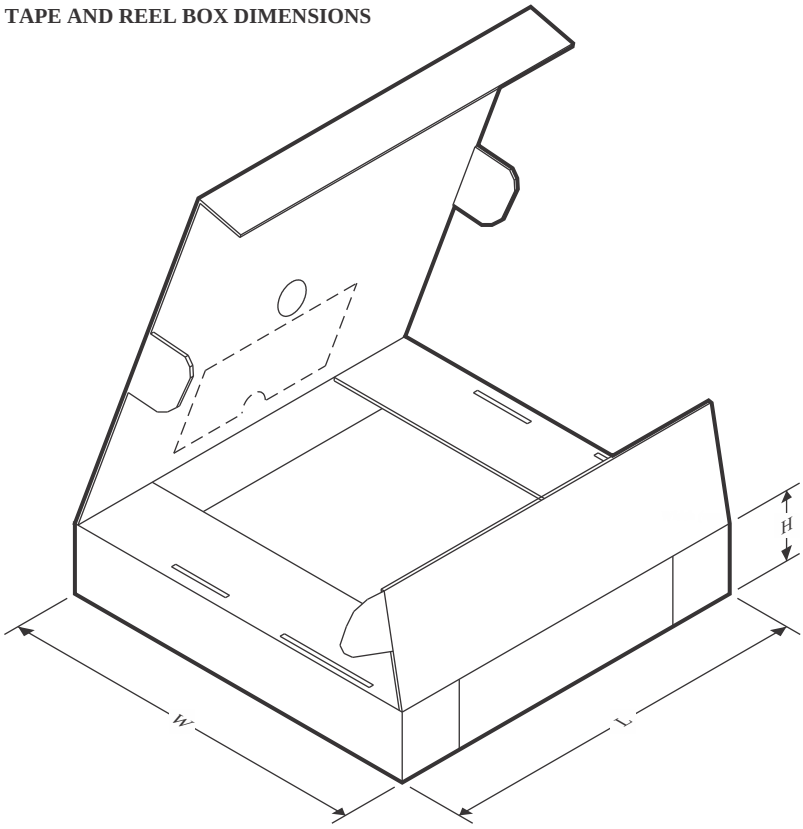
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS53119RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS53119RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

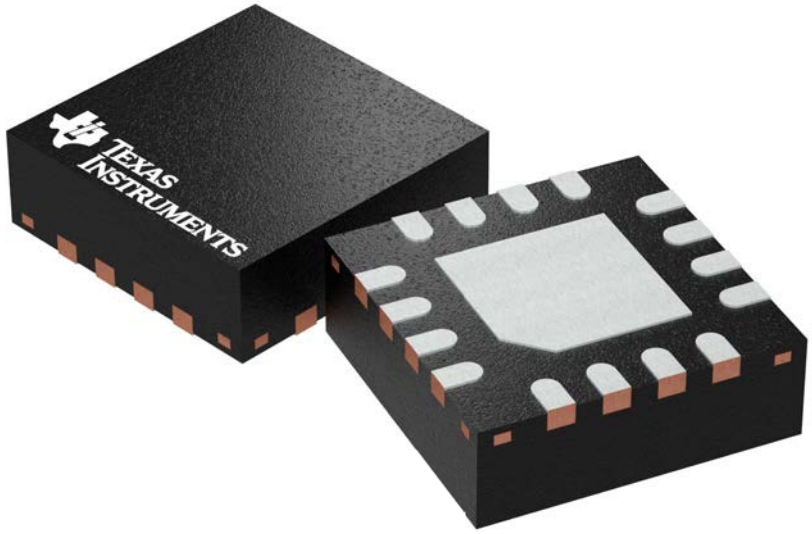


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS53119RGTR	VQFN	RGT	16	3000	346.0	346.0	33.0
TPS53119RGTT	VQFN	RGT	16	250	210.0	185.0	35.0

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



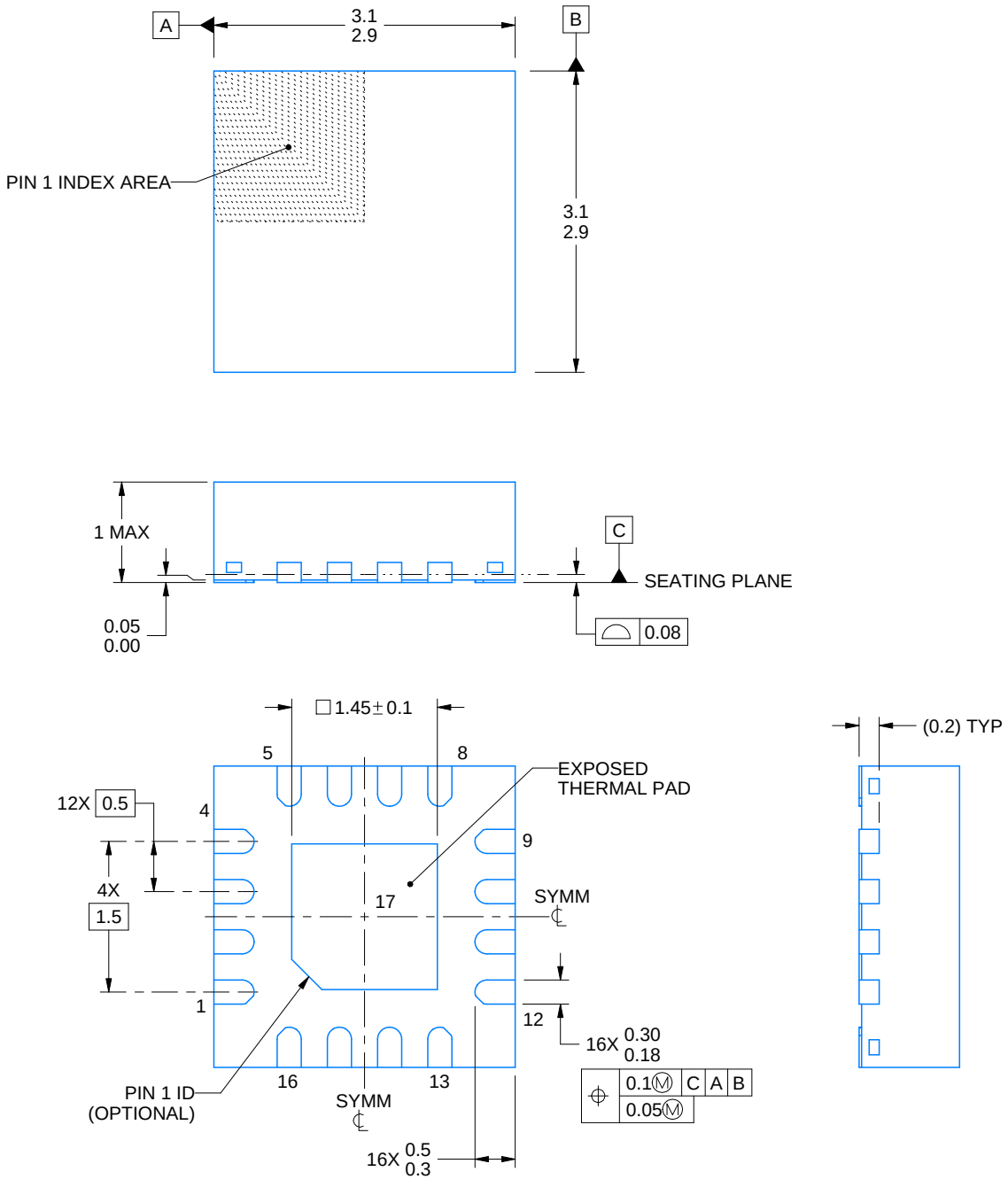
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

RGT0016A

PACKAGE OUTLINE

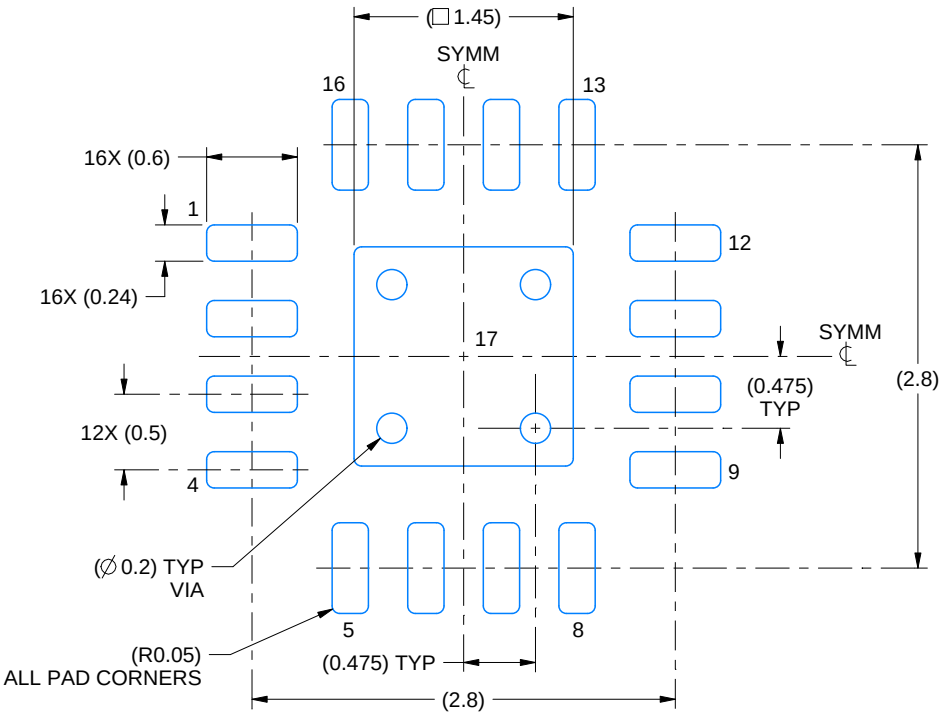
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

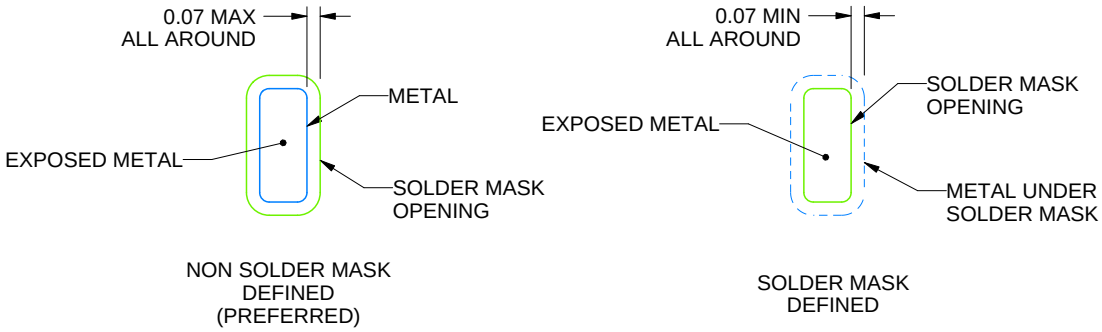


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Reference JEDEC registration MO-220



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

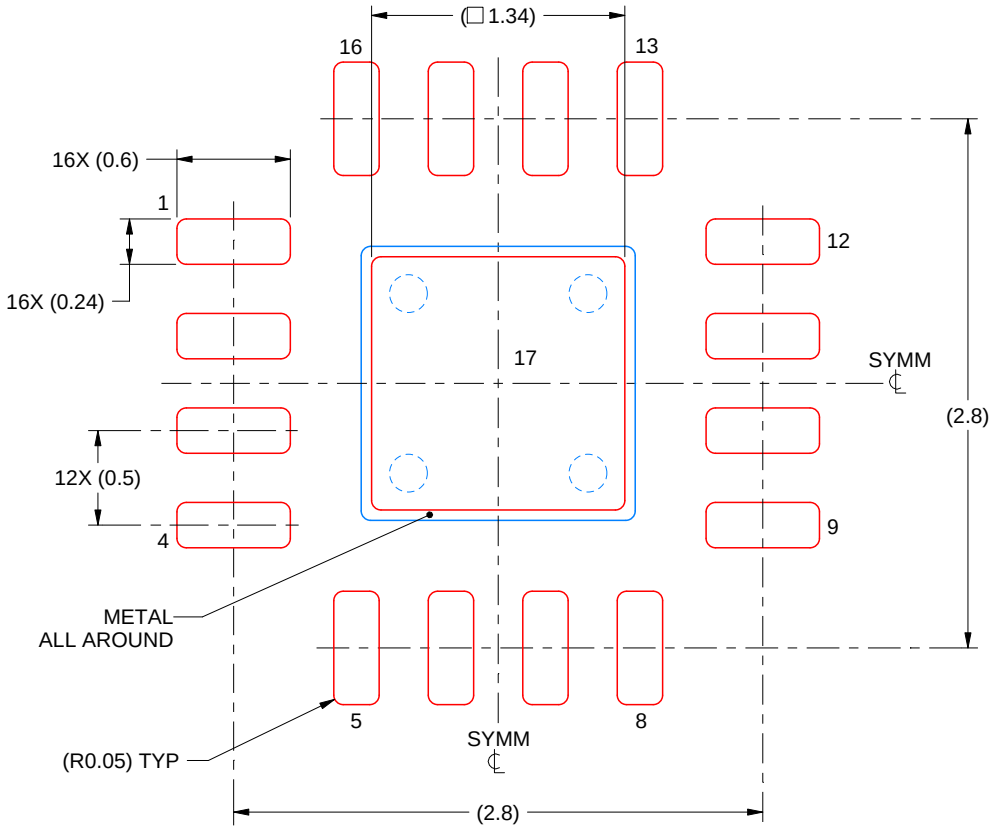


SOLDER MASK DETAILS

4219032/A 02/2017

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
86% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219032/A 02/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月