TPS565201 4.5V～17V入力、5A、同期整流降圧型電圧コンバータ

1 特長

- 最大出力電流 5A
- 31mΩおよび16mΩのFETを内蔵
- D-CAP2™モード制御による高速過渡応答
- 入力電圧範囲: 4.5V～17V
- 出力電圧範囲: 0.76V～7V
- 軽負荷で高い効率を実現するパルス・スキップ Eco-mode™
- 500kHzのスイッチング周波数
- 1µA未満のシャットダウン電流
- 1%の帰還電圧精度
- プリバイアス出力電圧からのスタートアップ
- サイクルごとの電流制限
- Hiccupモードによる過電流保護
- 非ラッチのUVP、UVLO、およびTSD保護

2 アプリケーション

- デジタル・テレビ用電源
- 高精細 Blu-ray™ディスク・プレイヤー
- ネットワーク・ホーム・ターミナル
- デジタル・セットトップ・ボックス（STB）
- 監視機器

3 概要

TPS565201は単純で使いやすい、5Aの同期整流降圧型コンバータです。

このデバイスは最小の外付け部品数で動作し、スタンバイ電流が低くなるよう最適化されています。

このスイッチ・モード電源(SMPS)デバイスは、D-CAP2™制御を採用して、高速な過渡応答を実現しており、外付けの補償部品が必要ありません。また、D-CAP2により、低い等価直列抵抗(ESR)の特化ポリマー・コンデンサやセラミック出力コンデンサを使用できます。

TPS565201はパルス・スキップ・モードで動作し、軽負荷での動作時に高い効率を維持します。

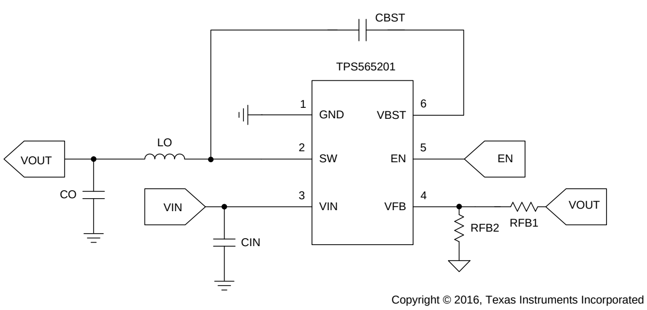
TPS565201デバイスは6ピンの1.6mm×2.9mm SOT (DDC)パッケージで供給され、-40℃～125℃の接合部温度範囲で動作します。

製品情報(1)

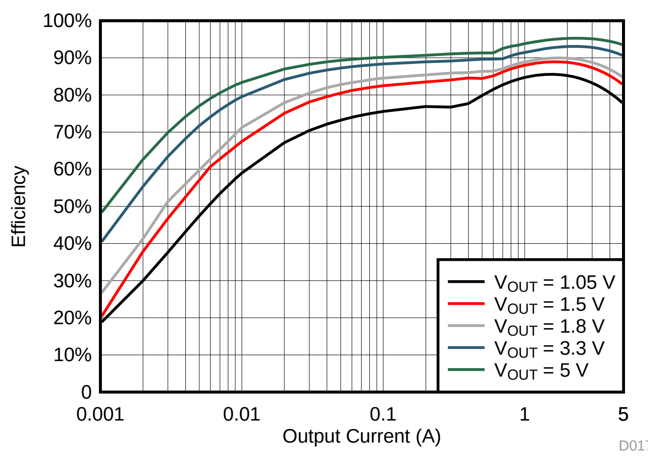
型番	パッケージ	本体サイズ(公称)
TPS565201	DDC (6)	1.60mm×2.90mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

概略回路図



TPS565201の効率



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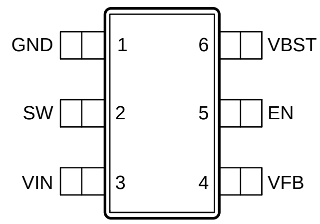
4 改訂履歴

日付	改訂内容	注
2017年9月	*	初版

5 Pin Configuration and Functions

DDC Package
6-Pin SOT
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	1	—	Ground pin. Source terminal of low-side power NFET as well as the ground terminal for controller circuit. Connect sensitive VFB to this GND at a single point.
SW	2	O	Switch node connection between high-side NFET and low-side NFET.
VIN	3	I	Input voltage supply pin. The drain terminal of high-side power NFET.
VFB	4	I	Converter feedback input. Connect to output voltage with feedback resistor divider.
EN	5	I	Enable input control. Active high and must be pulled up to enable the device.
VBST	6	O	Supply input for the high-side NFET gate drive circuit. Connect 0.1 µF capacitor between VBST and SW pins.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VIN, EN	–0.3	19	V
	VBST	–0.3	25	V
	VBST (10 ns transient)	–0.3	27	V
	VBST (vs SW)	–0.3	6.5	V
	VFB	–0.3	6.5	V
	SW	–2	19	V
	SW (10 ns transient)	–3.5	21	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Supply input voltage range		4.5		17	V
V_I	Input voltage range	VBST	–0.1		23	V
		VBST (10 ns transient)	–0.1		26	
		VBST (vs SW)	–0.1		6.0	
		EN	–0.1		17	
		VFB	–0.1		5.5	
		SW	–1.8		17	
		SW (10 ns transient)	–3.5		20	
T_J	Operating junction temperature		–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS565201	UNIT
		DDC (SOT)	
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	95.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	35.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	16.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_J = –40°C to 125°C, V_{IN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{VIN}	Operating – non-switching supply current	V_{IN} current, EN = 5 V, V_{FB} = 1 V		320	510	µA
I_{VINSDN}	Shutdown supply current	V_{IN} current, EN = 0 V		0.8	5	µA
LOGIC THRESHOLD						
V_{ENH}	EN high-level input voltage		1.6			V
V_{ENL}	EN low-level input voltage				0.8	V
R_{EN}	EN pin resistance to GND	V_{EN} = 12 V	120	245	400	kΩ
V_{FB} VOLTAGE AND DISCHARGE RESISTANCE						
V_{FBTH}	V_{FB} threshold voltage		753	760	767	mV
I_{VFB}	V_{FB} input current	V_{FB} = 0.8 V. T_A = 25°C		0	±0.1	µA
MOSFET						
$R_{DS(on)h}$	High-side switch resistance	T_A = 25°C, V_{BST} – V_{SW} = 5.5 V		31		mΩ
$R_{DS(on)l}$	Low-side switch resistance	T_A = 25°C		16		mΩ
CURRENT LIMIT						
I_{OCL}	Current limit		5.3	6.7	8	A
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold (1)	Shutdown temperature		172		°C
		Hysteresis		38		
ON-TIME TIMER CONTROL						
$t_{OFF(MIN)}$	Minimum off time	V_{FB} = 0.61 V		236	280	ns
SOFT START						
t_{SS}	Soft-start time	Internal soft-start time		1.0		ms
FREQUENCY						
F_{sw}	Switching frequency	V_{IN} = 12 V, V_O = 5 V, CCM mode		500		kHz
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{UVP}	Output UVP threshold	Hiccup detect (H > L)		65		%
T_{HICCUP_WAIT}	Hiccup on time			1.8		ms
T_{HICCUP_RE}	Hiccup time before restart			14.9		ms
UVLO						
UVLO	UVLO threshold	Wake up VIN voltage		4.0	4.3	V
		Shutdown VIN voltage	3.3	3.6		
		Hysteresis VIN voltage (1)		0.4		

(1) Not production tested.

6.6 Typical Characteristics

V_{IN} = 12 V (unless otherwise noted)

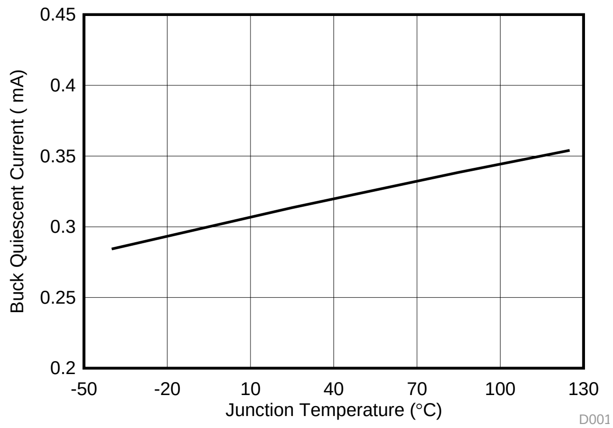


Figure 1. TPS565201 Supply Current vs Junction Temperature

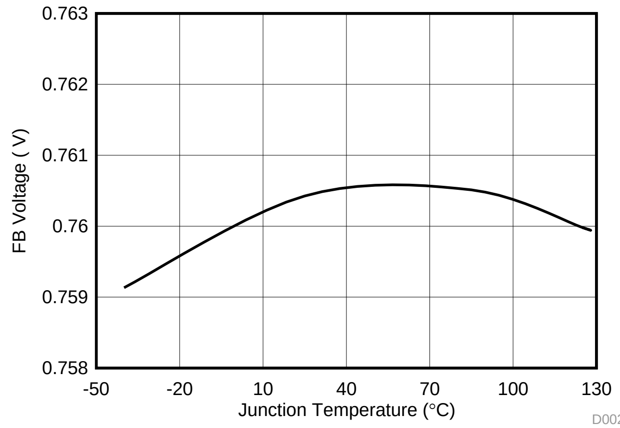


Figure 2. VFB Voltage vs Junction Temperature

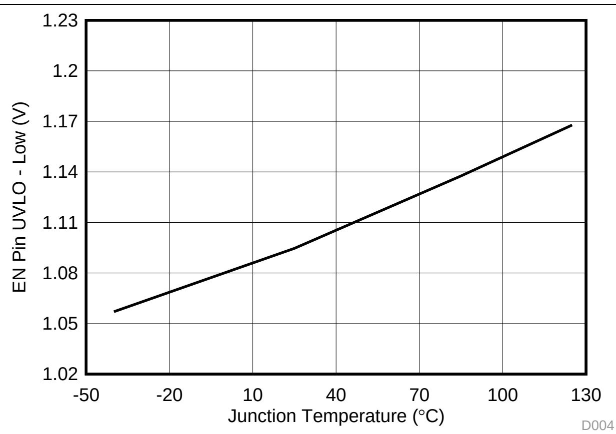


Figure 3. EN Pin UVLO Low Voltage vs Junction Temperature

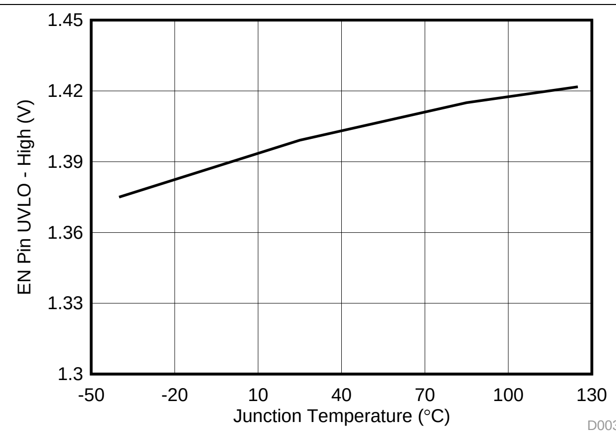


Figure 4. TPS565201 EN Pin UVLO High Voltage vs Junction Temperature

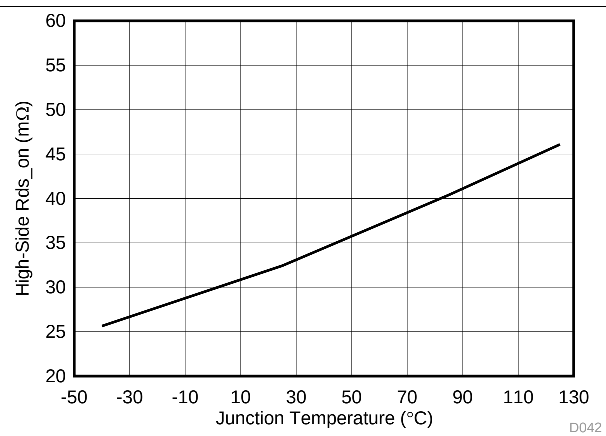


Figure 5. TPS565201 High-Side $R_{ds\text{-}On}$ vs Junction Temperature

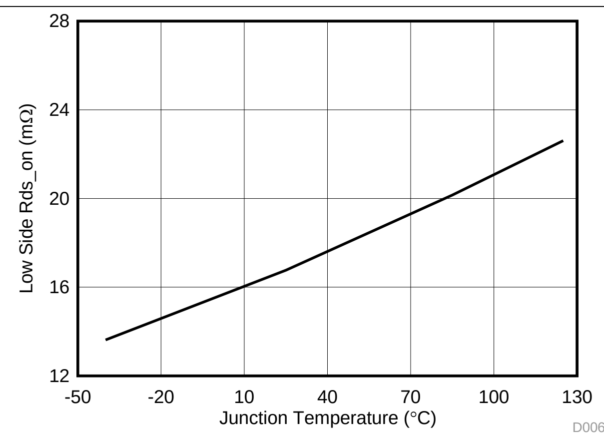


Figure 6. Low-Side $R_{ds\text{-}On}$ vs Junction Temperature

Typical Characteristics (continued)

V_{IN} = 12 V (unless otherwise noted)

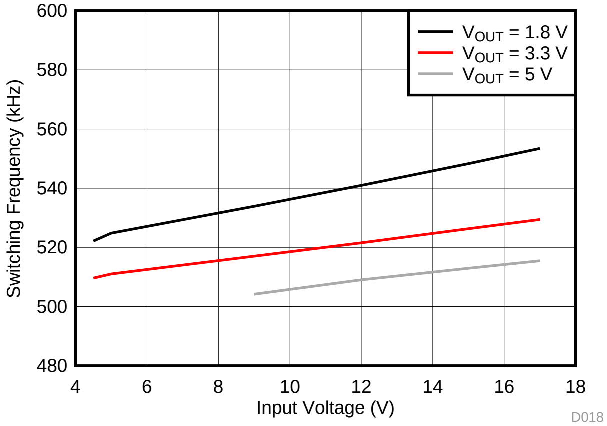


Figure 7. TPS565201 Switching Frequency vs Input Voltage

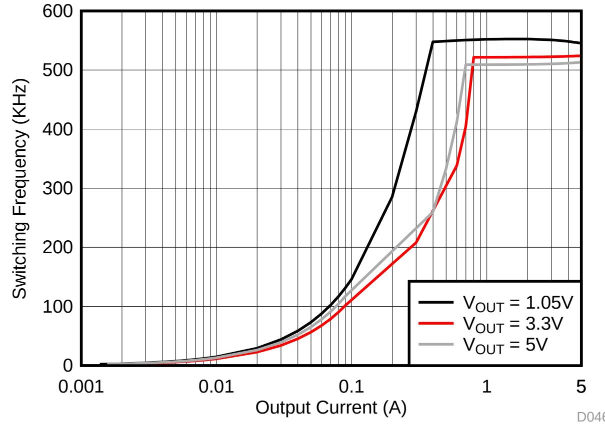
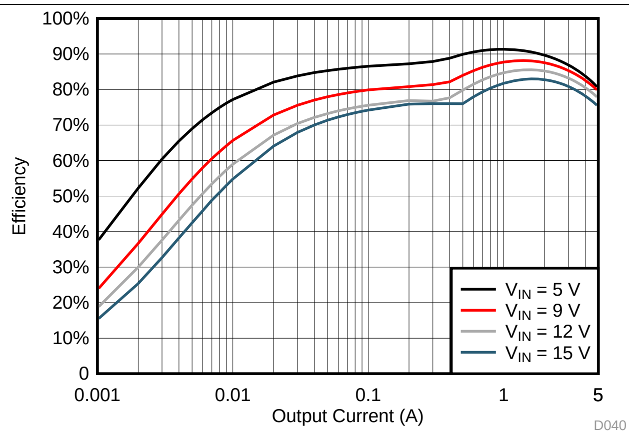
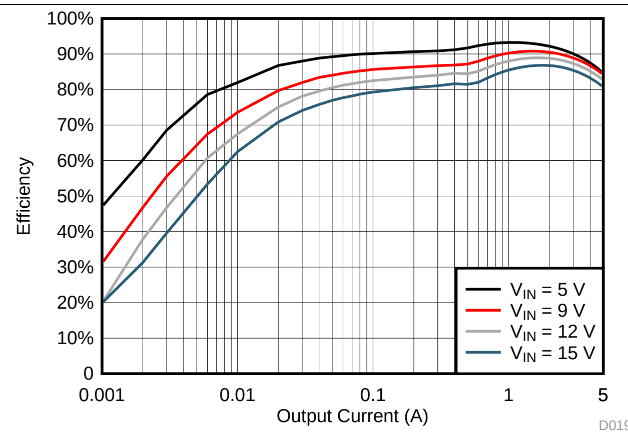


Figure 8. TPS565201 Switching Frequency vs Output Current



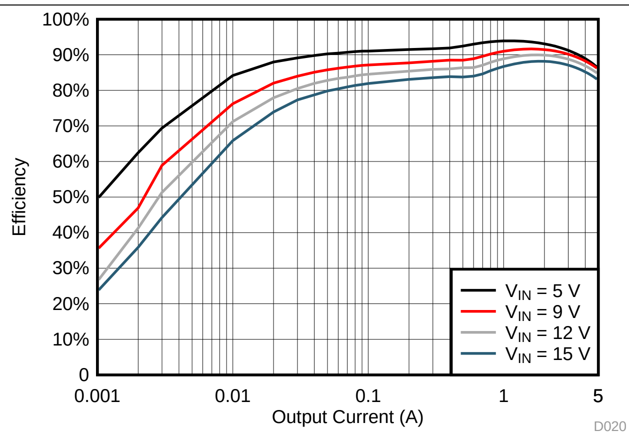
V_{OUT} = 1.05 V L = 2.2 µH

Figure 9. TPS565201 Efficiency vs Output Current



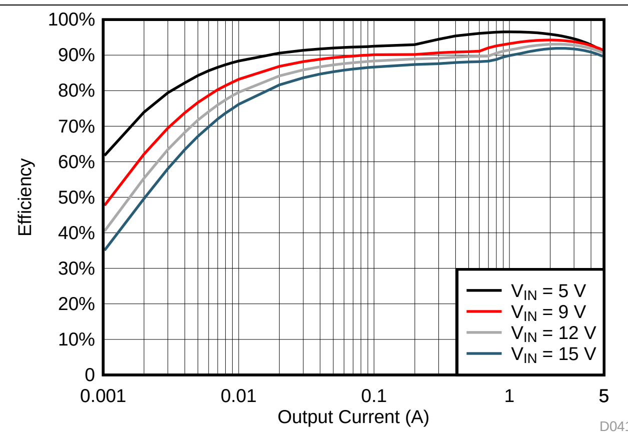
V_{OUT} = 1.5 V L = 2.2 µH

Figure 10. TPS565201 Efficiency vs Output Current



V_{OUT} = 1.8 V L = 2.2 µH

Figure 11. TPS565201 Efficiency vs Output Current

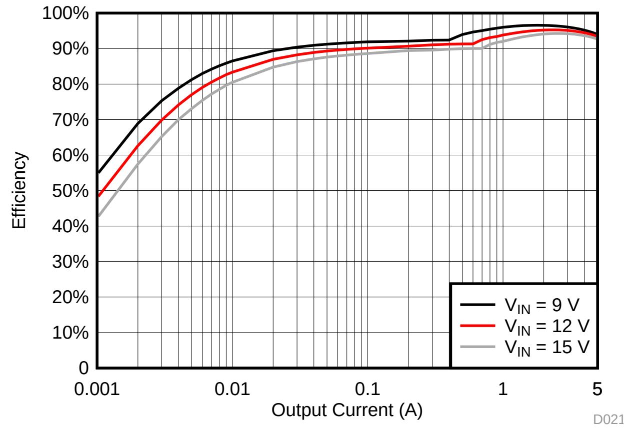


V_{OUT} = 3.3 V L = 2.2 µH

Figure 12. TPS565201 Efficiency vs Output Current

Typical Characteristics (continued)

V_{IN} = 12 V (unless otherwise noted)



V_{OUT} = 5 V L = 3.3 µH

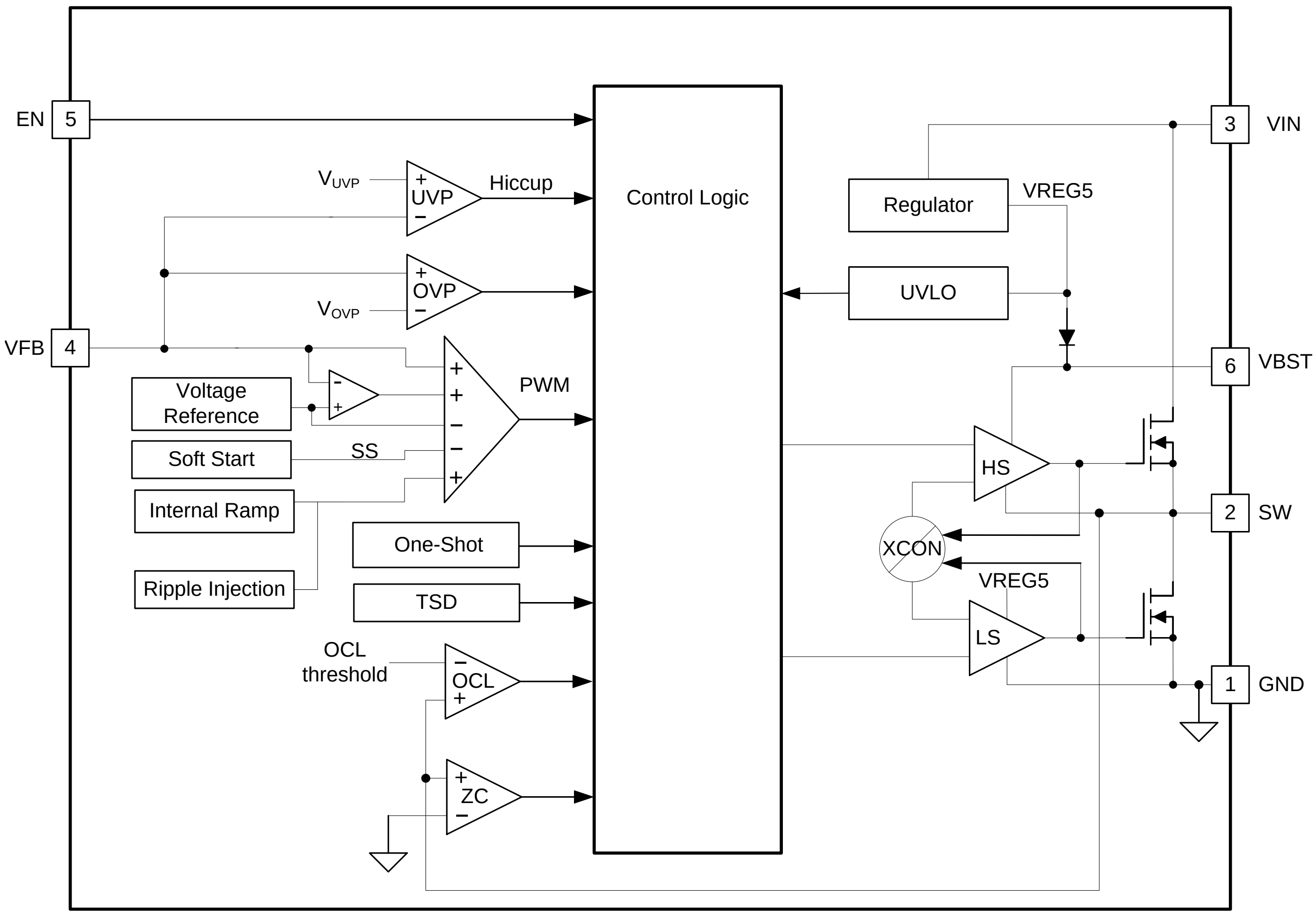
Figure 13. TPS565201 Efficiency vs Output Current

7 Detailed Description

7.1 Overview

The TPS565201 is a 5-A synchronous step-down converter. The proprietary D-CAP2™ mode control supports low ESR output capacitors such as specialty polymer capacitors and multi-layer ceramic capacitors without complex external compensation circuits. The fast transient response of D-CAP2™ mode control can reduce the output capacitance required to meet a specific level of performance.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Adaptive On-Time Control and PWM Operation

The main control loop of the TPS565201 is adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2™ mode control. The D-CAP2™ mode control combines adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with low-ESR ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one-shot timer expires. This one shot duration is set inversely proportional to the converter input voltage, V_{IN}, and proportional to the output voltage V_O, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An ripple is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2™ mode control.

7.3.2 Pulse Skip Mode

The TPS565201 is designed with Eco-mode™ to maintain high light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to point that its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases the converter runs into discontinuous conduction mode. The on-time is kept almost the same as it was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. This makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high. The transition point to the light load operation IOUT(LL) current can be calculated in Equation 1.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (1)$$

7.3.3 Soft Start and Pre-Biased Soft Start

The TPS565201 has an internal 1.0-ms soft-start. When the EN pin becomes high, the internal soft-start function begins ramping up the reference voltage to the PWM comparator.

If the output capacitor is pre-biased at startup, the device initiates switching and starts ramping up only after the internal reference voltage becomes greater than the feedback voltage V_{FB}. This scheme ensures that the converter ramps up smoothly into regulation point.

Feature Description (continued)

7.3.4 Current Protection

The output over-current limit (OCL) is implemented using a cycle-by-cycle valley detect control circuit. The inductor current is monitored during the OFF state by measuring the low-side FET drain to source voltage, which is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on time of the high-side FET switch, the switch current increases at a linear rate determined by V_{IN}, V_{OUT}, and the output inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current I_{OUT}. If the monitored current is above the OCL level, the converter maintains low-side FET on and delays the creation of a new set pulse, even the voltage feedback loop requires one, until the current level becomes OCL level or lower. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of over-current protection. The load current is higher than the over-current threshold by one half of the peak-to-peak inductor ripple current. Also, when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. This may cause the output voltage to fall. When the VFB voltage falls below the UVP threshold voltage, the UVP comparator detects it. And then, the device shuts down after the UVP delay time (typically 24 µs) and re-starts after the hiccup time (typically 14.9 ms).

When the over current condition is removed, the output voltage returns to the regulated value.

7.3.5 Undervoltage Lockout (UVLO) Protection

UVLO protection monitors input voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. This protection is non-latching.

7.3.6 Thermal Shutdown

The device monitors the temperature of itself. If the temperature exceeds the threshold value (typically 172°C), the device is shut off. This is a non-latch protection.

7.4 Device Functional Modes

7.4.1 Normal Operation

When the input voltage is above the UVLO threshold and the EN voltage is above the enable threshold, the TPS565201 operates in the normal switching mode. Normal continuous conduction mode (CCM) occurs when the minimum switch current is above 0 A. In CCM, the TPS565201 operates at a quasi-fixed frequency of 500 kHz.

7.4.2 Eco-mode™ Operation

When the TPS565201 is in the normal CCM operating mode and the switch current falls to 0 A, the TPS565201 begins operating in pulse skipping eco-mode. Each switching cycle is followed by a period of energy saving sleep time. The sleep time ends when the VFB voltage falls below the eco-mode threshold voltage. As the output current decreases, the perceived time between switching pulses increases.

7.4.3 Standby Operation

When the TPS565201 is operating in either normal CCM or Eco-mode™, it may be placed in standby by asserting the EN pin low.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The device is a typical step-down DC-DC converter for converting a higher dc voltage to a lower dc voltage with a maximum available output current of 5 A. The following design procedure can be used to select component values for the TPS565201. Alternately, the WEBENCH® software may be used to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

8.2 Typical Application

The application schematic in Figure 14 shows the TPS565201 4.5-V to 17-V input, 1.05-V output converter design meeting the requirements for 5-A output. This circuit is available as the evaluation module (EVM). The sections provide the design procedure.

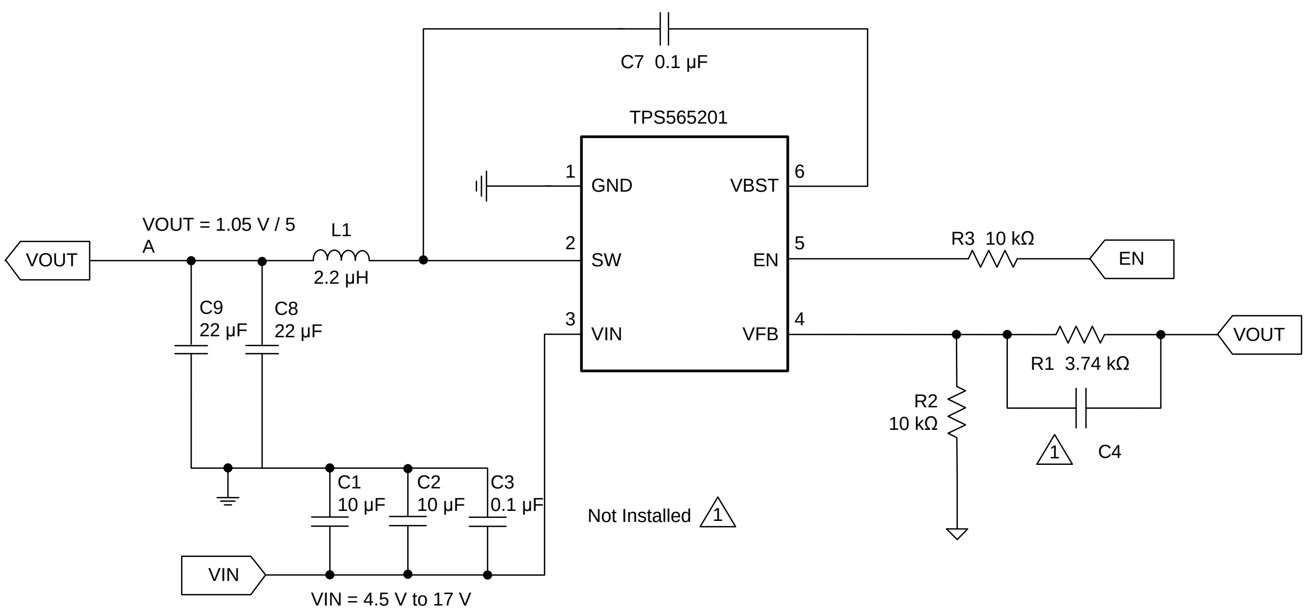


Figure 14. TPS565201 1.05-V, 5-A Reference Design

Typical Application (continued)

8.2.1 Design Requirements

Table 1 shows the design parameters for this application.

Table 1. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage range	4.5 to 17 V
Output voltage	1.05 V
Transient response, 1-A/us slew rate	ΔVout = ±5%
Input ripple voltage	400 mV
Output ripple voltage	20 mV
Output current rating	5 A
Operating frequency	550 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. TI recommends to use 1% tolerance or better divider resistors. Start by using Equation 2 to calculate V_{OUT}.

To improve efficiency at very light loads consider using larger value resistors. However, using too high of resistance causes the circuit to be more susceptible to noise; and, voltage errors from the VFB input current will be more noticeable.

$$V_{OUT} = 0.760 \times \left(1 + \frac{R1}{R2}\right) \quad (2)$$

8.2.2.2 Output Filter Selection

The LC filter used as the output filter has double pole at:

$$f_P = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \quad (3)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the device. The low frequency phase is 180°. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. D-CAP2 introduces a high frequency zero that reduces the gain roll off to –20 dB per decade and increases the phase to 90° one decade above the zero frequency. The inductor and capacitor for the output filter must be selected so that the double pole of Equation 3 is located below the high frequency zero but close enough that the phase boost provided be the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in Table 2.

Table 2. Recommended Component Values

OUTPUT VOLTAGE (V)	R1 (kΩ)	R2 (kΩ)	L1 (µH)			C8 + C9 (µF)
			MIN	TYP	MAX	
1	3.09	10.0	1.0	2.2	4.7	20 to 68
1.05	3.74	10.0	1.0	2.2	4.7	20 to 68
1.2	5.76	10.0	1.0	2.2	4.7	20 to 68
1.5	9.53	10.0	1.5	2.2	4.7	20 to 68
1.8	13.7	10.0	1.5	2.2	4.7	20 to 68
2.5	22.6	10.0	2.2	2.2	4.7	20 to 68
3.3	33.2	10.0	2.2	2.2	4.7	20 to 68
5	54.9	10.0	3.3	3.3	4.7	20 to 68
6.5	75	10.0	3.3	3.3	4.7	20 to 68

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using Equation 4, Equation 5, and Equation 6. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current.

Use 550 kHz for f_{SW}. Make sure the chosen inductor is rated for the peak current of Equation 5 and the RMS current of Equation 7.

$$I_{P\text{-}P} = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{SW}} \tag{4}$$

$$I_{PEAK} = I_O + \frac{I_{P-P}}{2} \tag{5}$$

$$I_{LO(RMS)} = \sqrt{I_O^{\,2} + \frac{1}{12} I_{P-P}^{\,2}} \tag{6}$$

For this design example, the calculated peak current is 5.4 A and the calculated RMS current is 5 A. The inductor used is a WE 744311220 with a peak current rating of 13 A and an RMS current rating of 9 A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS565201 is intended for use with ceramic or other low ESR capacitors. Recommended values range from 20 µF to 68 µF. Use Equation 7 to determine the required RMS current rating for the output capacitor.

$$I_{CO(RMS)} = \frac{V_{OUT} \times \left(V_{IN} - V_{OUT}\right)}{\sqrt{12} \times V_{IN} \times L_O \times f_{SW}} \tag{7}$$

For this design two TDK C3216X5R0J226M 22-µF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.229 A.

8.2.2.3 Input Capacitor Selection

The TPS565201 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. TI recommends a ceramic capacitor over 10 µF for the decoupling capacitor. An additional 0.1-µF capacitor (C3) from pin 3 to ground is optional to provide additional high frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage.

8.2.2.4 Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the VBST to SW pin for proper operation. TI recommends to use a ceramic capacitor.

8.2.3 Application Curves

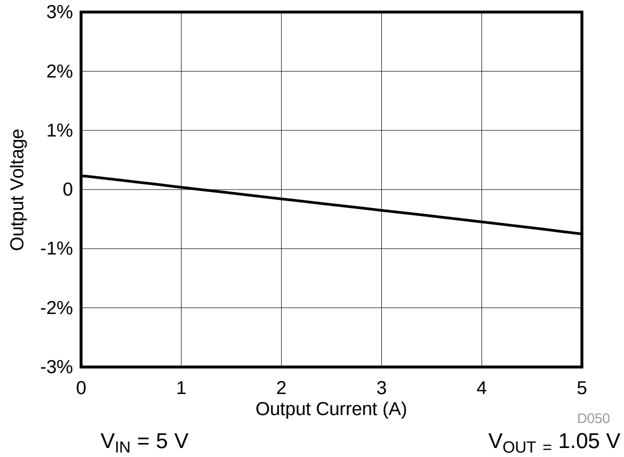


Figure 15. Load Regulation, V_{IN} = 5 V

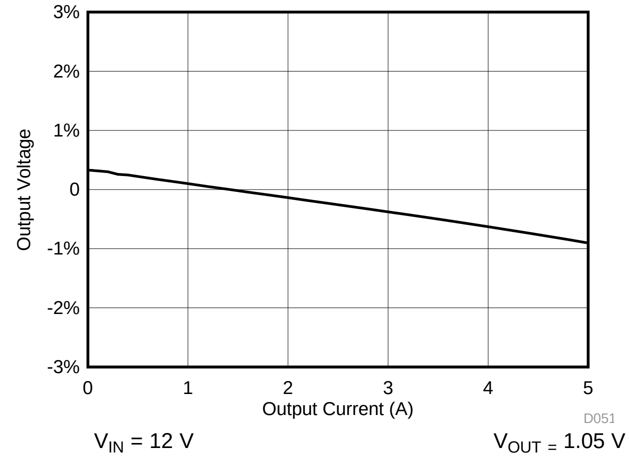


Figure 16. Load Regulation, V_{IN} = 12 V

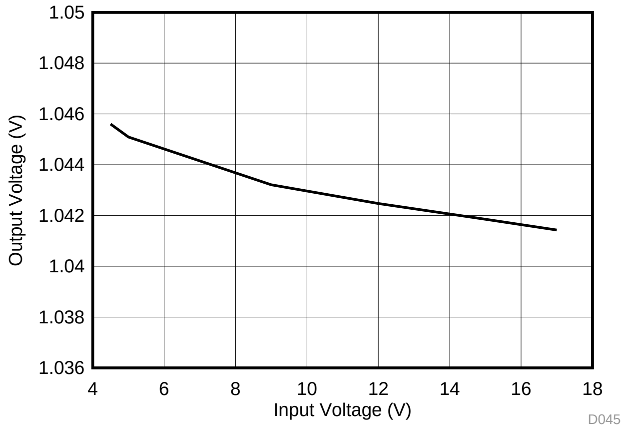


Figure 17. Line Regulation

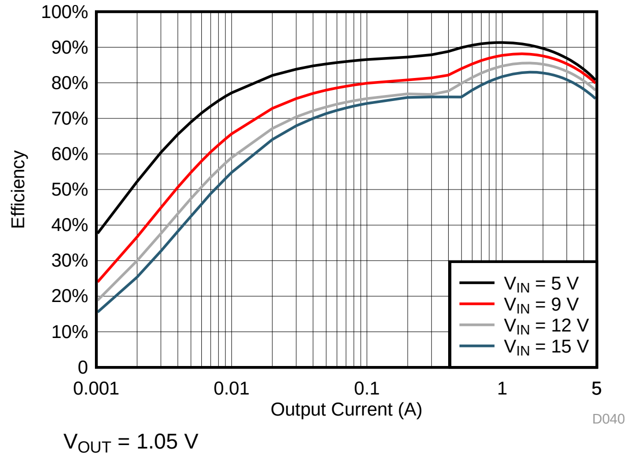


Figure 18. Efficiency vs Output Current

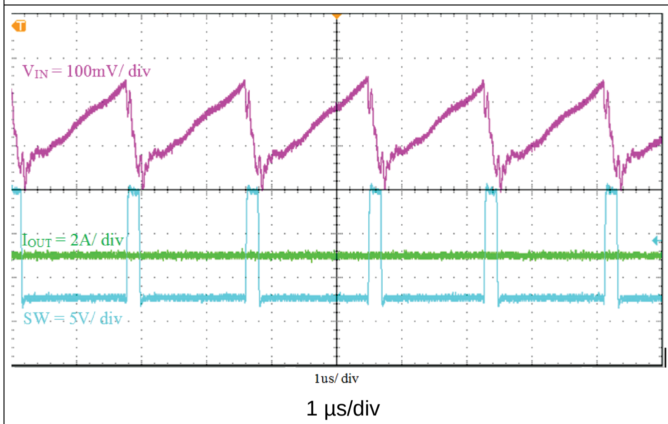


Figure 19. TPS565201 Input Voltage Ripple

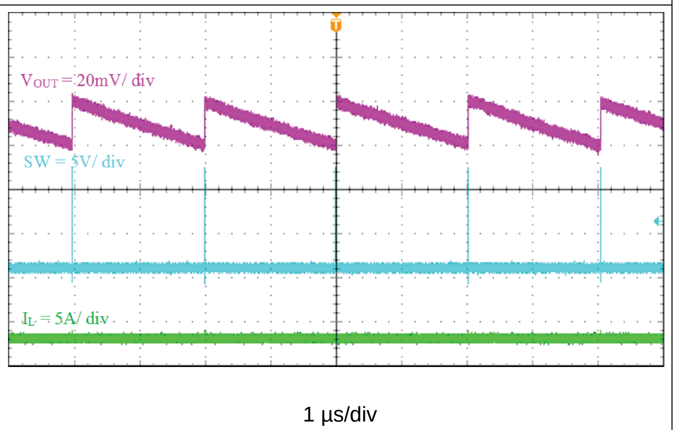
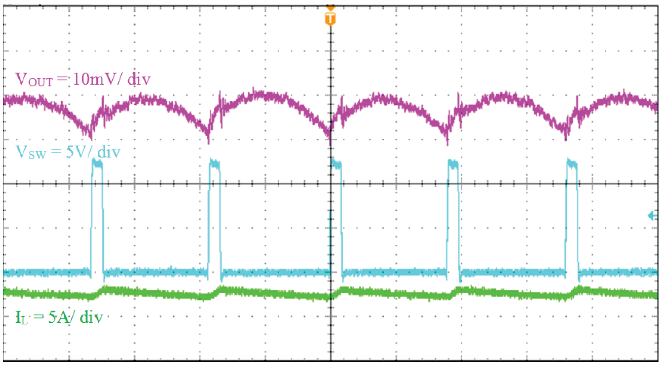
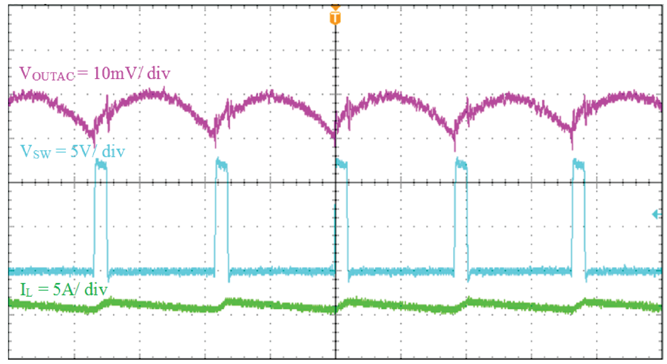


Figure 20. TPS565201 Output Voltage Ripple, No Load



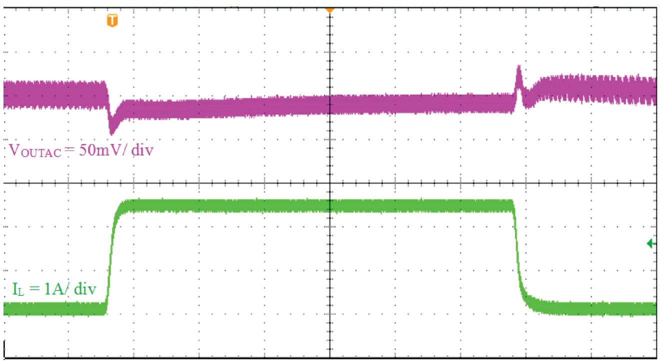
1 µs/div

Figure 21. TPS565201 Output Voltage Ripple, I_{OUT} 2.5 A



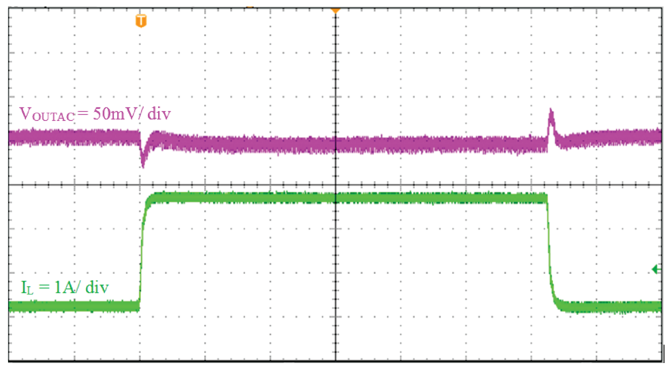
1 µs/div

Figure 22. TPS565201 Output Voltage Ripple, I_{OUT} 5 A



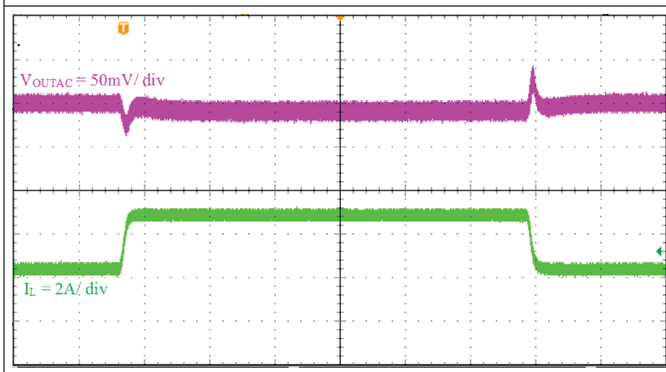
100 µs/div

Figure 23. TPS565201 Transient Response 0.1 to 2.5 A



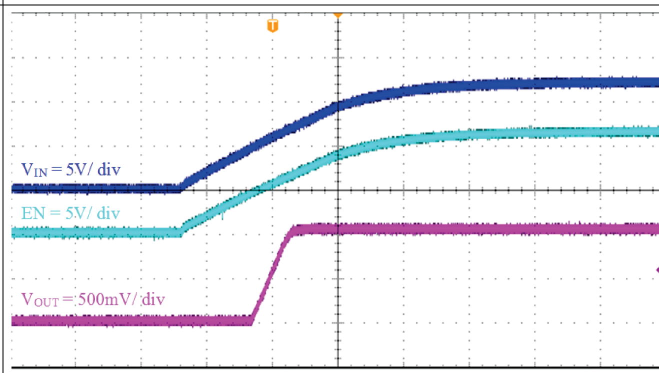
100 µs/div

Figure 24. TPS565201 Transient Response, 1.25 to 3.75 A



100 µs/div

Figure 25. TPS565201 Transient Response, 2.5 to 5 A



2 ms/div

Figure 26. TPS565201 Startup Relative to V_{IN}

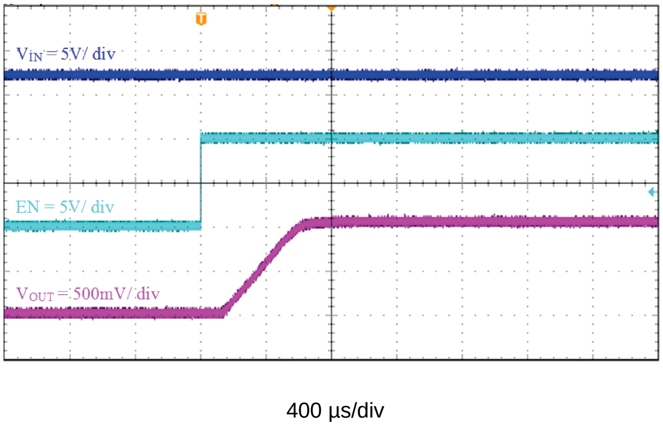


Figure 27. TPS565201 Startup Relative to EN

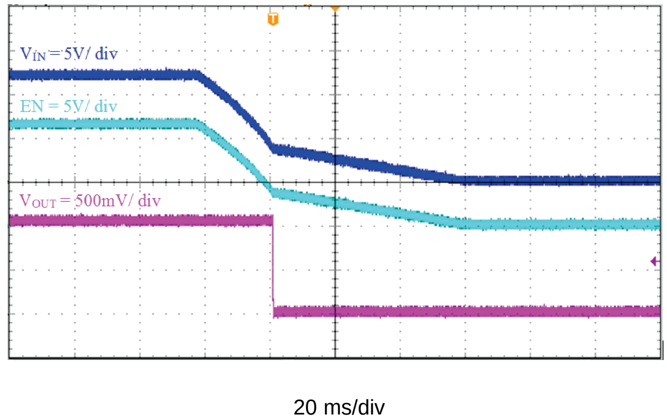


Figure 28. TPS565201 Shutdown Relative to V_{IN}

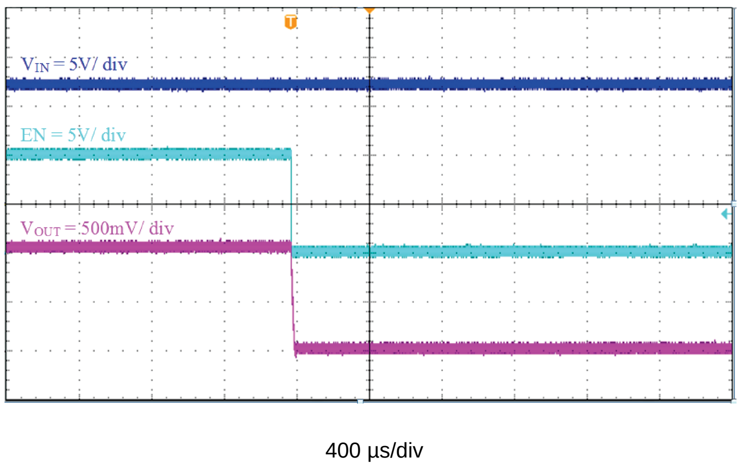


Figure 29. TPS565201 Shutdown Relative to EN

9 Power Supply Recommendations

The TPS565201 is designed to operate from input supply voltage in the range of 4.5 V to 17 V. Buck converters require the input voltage to be higher than the output voltage for proper operation. The maximum recommended operating duty cycle is 83%. Using that criteria, the minimum recommended input voltage is V_O / 0.83.

10 Layout

10.1 Layout Guidelines

1. VIN and GND traces should be as wide as possible to reduce trace impedance. The wide areas are also of advantage from the view point of heat dissipation.
2. The input capacitor and output capacitor should be placed as close to the device as possible to minimize trace impedance.
3. Provide sufficient vias for the input capacitor and output capacitor.
4. Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
5. Do not allow switching current to flow under the device.
6. A separate VOUT path should be connected to the upper feedback resistor.
7. Make a Kelvin connection to the GND pin for the feedback path.
8. Voltage feedback loop should be placed away from the high-voltage switching trace, and preferably has ground shield.
9. The trace of the VFB node should be as small as possible to avoid noise coupling.
10. The GND trace between the output capacitor and the GND pin should be as wide as possible to minimize its trace impedance.

10.2 Layout Example

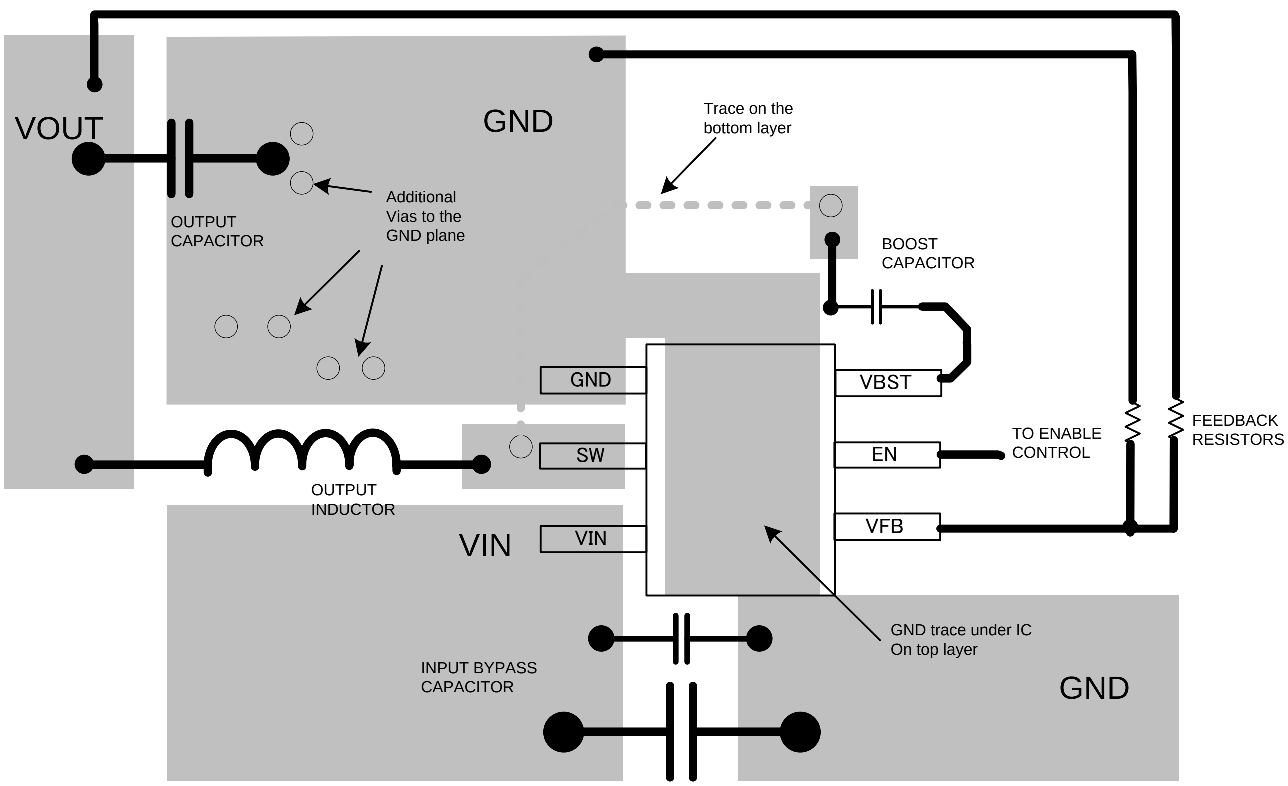


Figure 30. TPS565201 Layout Example

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントの更新通知を受け取る方法

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11.2 コミュニティ・リソース

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11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS565201DDCR	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5201
TPS565201DDCR.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5201
TPS565201DDCT	Active	Production	SOT-23-THIN (DDC) | 6	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5201
TPS565201DDCT.A	Active	Production	SOT-23-THIN (DDC) | 6	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5201

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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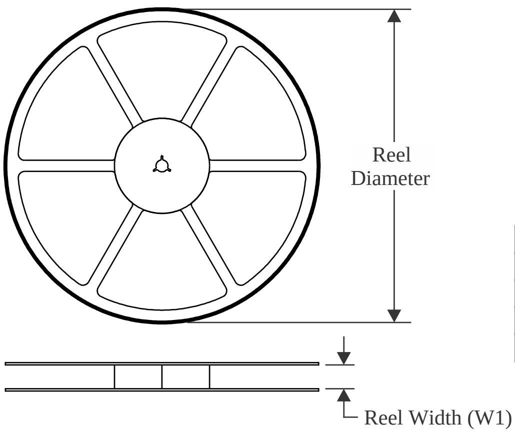
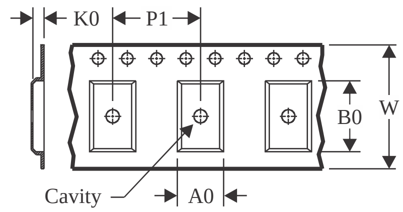
TAPE AND REEL INFORMATION

REEL DIMENSIONS

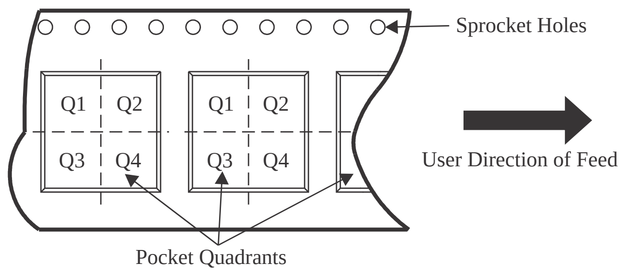


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

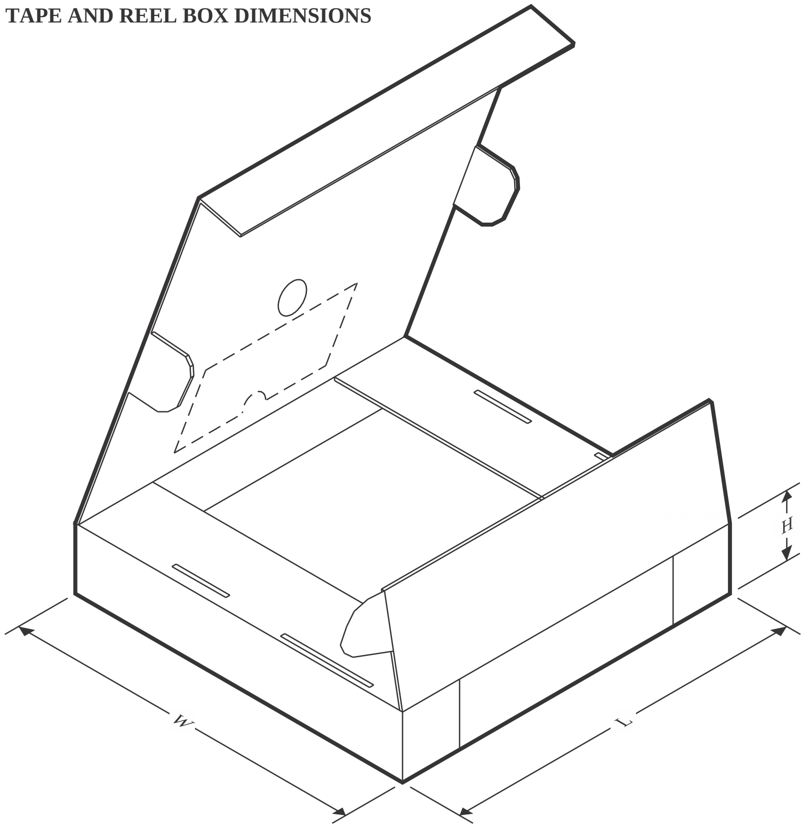
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

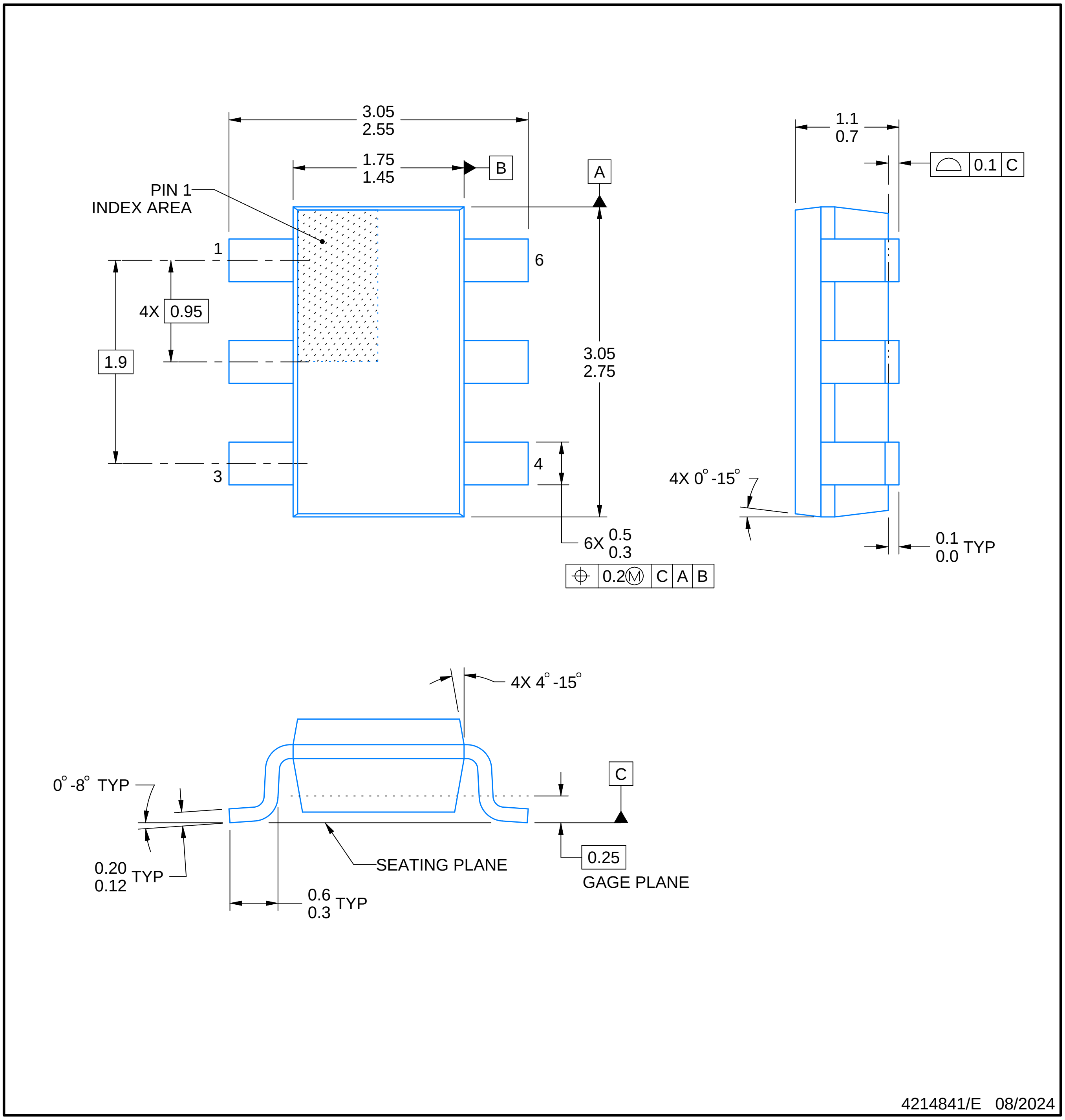
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS565201DDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS565201DDCR	SOT-23-THIN	DDC	6	3000	180.0	9.5	3.17	3.1	1.1	4.0	8.0	Q3
TPS565201DDCT	SOT-23-THIN	DDC	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



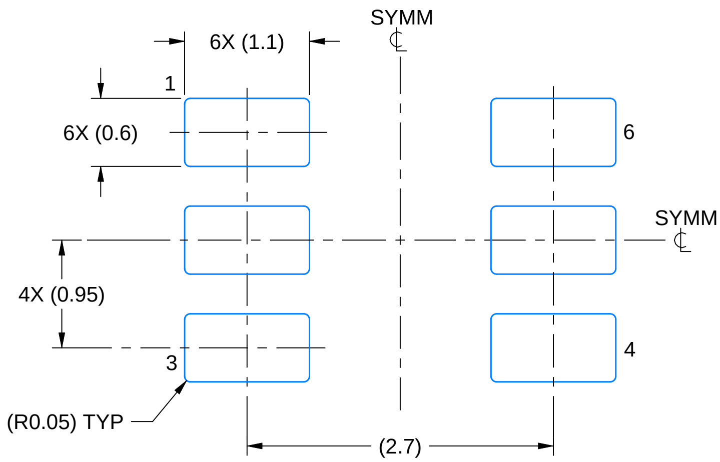
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS565201DDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
TPS565201DDCR	SOT-23-THIN	DDC	6	3000	184.0	184.0	19.0
TPS565201DDCT	SOT-23-THIN	DDC	6	250	210.0	185.0	35.0

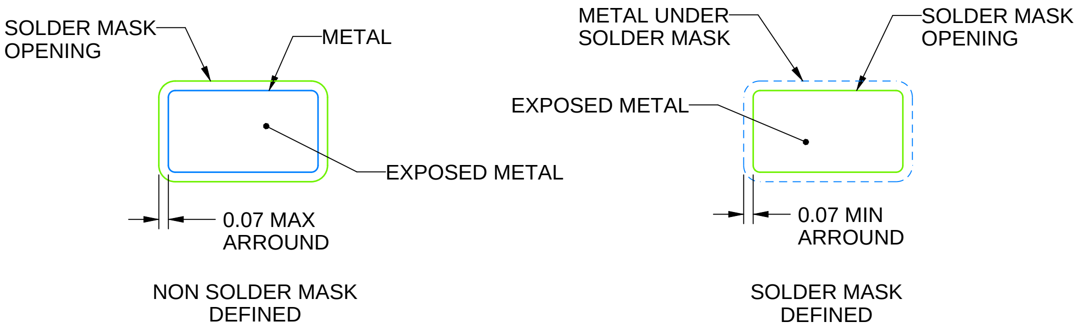


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X

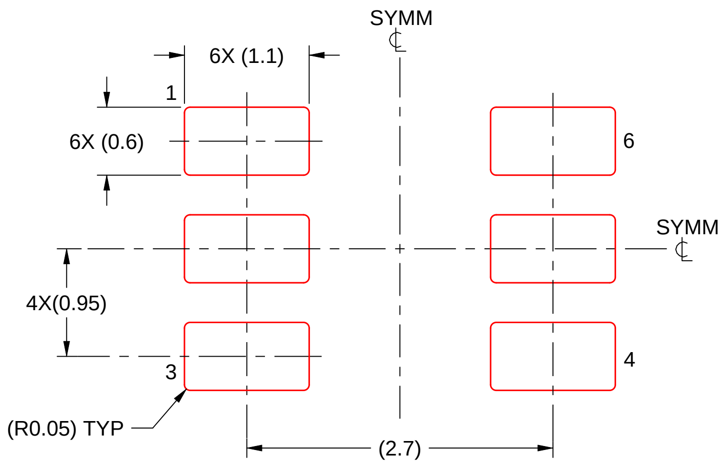


SOLDERMASK DETAILS

4214841/E 08/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214841/E 08/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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