TEXAS INSTRUMENTS
TPS62150, TPS62150A, TPS62151, TPS62152, TPS62153
JAJSBM1E – NOVEMBER 2011 – REVISED OCTOBER 2021

TPS6215x 3V～17V、1A 降圧コンバータ、3mm × 3mm QFN パッケージ

1 特長

- DCS-Control™ トポロジ
- 入力電圧範囲:3V～17V
- 最大 1A の出力電流
- 出力電圧を 0.9V～6V の範囲で調整可能
- ピンにより出力電圧を選択可能 (公称値、+5%)
- ソフトスタートとトラッキングをプログラム可能
- パワーセーブ・モードへのシームレスな移行
- 静止電流:17μA (標準値)
- 動作周波数を選択可能
- パワー・グッド出力
- 100% デューティ・サイクル・モード
- 短絡保護
- 過熱保護
- TPS62130 および TPS62140 とピン互換
- 3mm × 3mm の VQFN-16 パッケージで供給
- TPS82150 モジュールを使って設計を迅速化

2 アプリケーション

- 標準の 12V レール電源
- 単一または複数のリチウムイオン・バッテリからの POL 電源
- ソリッドステート・ドライブ
- 組み込みシステム
- LDO の置き換え
- モバイル PC、タブレット、モデム、カメラ
- サーバー、マイクロサーバー
- データ端末、ePOS (販売時点情報管理)

3 概要

TPS6215x ファミリは、使いやすい同期整流降圧 DC/DC コンバータで、電力密度の高いアプリケーション向けに最適化されています。スイッチング周波数が標準値で 2.5MHz と高いため、小型のインダクタを使用でき、また、DCS-Control トポロジの採用によって、高速な過渡応答および高精度の出力電圧が得られます。

3V～17V の広い入力電圧範囲で動作するため、このデバイスは、リチウムイオンや他のバッテリ、および 12V の中間電力レールで動作するシステムに理想的です。このデバイスは、0.9V～6V の出力電圧で、最大 1A の連続出力電流を供給できます (100%デューティ・サイクル・モードの場合)。ソフトスタート・ピンを使って出力電圧のスタートアップ・ランプを制御できるため、スタンドアロン電源としても、またトラッキング構成でも動作できます。イネーブル (EN) ピンとオープン・ドレインのパワーグッド (PG) ピンを設定することにより、電源シーケンスも可能です。

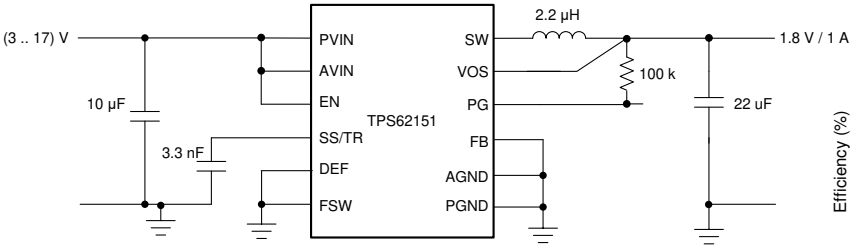
パワーセービング・モードでは、このデバイスは VIN から約 17μA の静止電流を消費します。負荷が小さい時には自動的かつシームレスにパワーセーブ・モードへ移行するため、負荷範囲全体にわたって高い効率が維持されます。シャットダウン・モードではデバイスがオフになり、シャットダウン時の消費電流は 2μA 未満です。

このデバイスには可変出力電圧と固定出力電圧のバージョンがあり、3 × 3mm (RGT) の 16 ピン VQFN パッケージで供給されます。

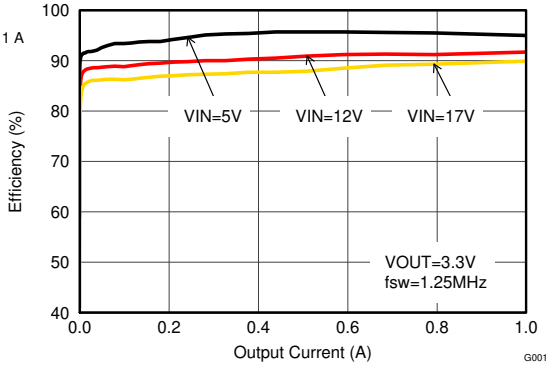
製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
TPS6215X	VQFN (16)	3.00mm × 3.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



代表的なアプリケーション回路図



効率と出力電流との関係

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

Table of Contents

1 特長 1
2 アプリケーション 1
3 概要 1
4 Revision History 2
5 Device Comparison Table 3
6 Pin Configuration and Functions 3
7 Specifications 4
7.1 Absolute Maximum Ratings(1) 4
7.2 ESD Ratings 4
7.3 Recommended Operating Conditions 4
7.4 Thermal Information 4
7.5 Electrical Characteristics 5
7.6 Typical Characteristics 6
8 Detailed Description 7
8.1 Overview 7
8.2 Functional Block Diagrams 7
8.3 Feature Description 8
8.4 Device Functional Modes 10
9 Application and Implementation 12
9.1 Application Information 12
9.2 Typical Application 12
9.3 System Examples 24
10 Power Supply Recommendations 27
11 Layout 28
11.1 Layout Guidelines 28
11.2 Layout Example 28
12 Device and Documentation Support 30
12.1 Device Support 30
12.2 Documentation Support 30
12.3 Receiving Notification of Documentation Updates 30
12.4 サポート・リソース 30
12.5 Trademarks 30
12.6 Electrostatic Discharge Caution 30
12.7 Glossary 30
13 Mechanical, Packaging, and Orderable Information 31

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (September 2016) to Revision E (October 2021)	Page
• TPS82150 製品ページへのリンクを追加	1
• 文書全体にわたって表、図、相互参照の採番方法を更新	1

Changes from Revision C (November 2014) to Revision D (September 2016)	Page
• 「*特長*」のリストに「TPS62130 および TPS62140 とピン互換」を追加	1
• Changed the T_J MAX value From: 125°C To: 150°C in the *Absolute Maximum Rating*	4
• Changed the *セクション 7.4* values	4
• Changed (T_J = –40°C to 85°C) To: (T_J = –40°C to 125°C) in the *セクション 7.5* conditions	5
• Added a test condition for IQ at TA = -40°C to +85°C in the *セクション 7.5*	5
• Added 表 8-1 and 表 8-2	8
• Added indicators (C1, C3, and C5) for capacitances to 図 9-1	12
• Added Switching Frequency graphs for 1.0-V, 1.8-V, and 5.0-V applications (図 9-18 through 図 9-25)	18
• Changed *Layout Example*	28

Copyright © 2022 Texas Instruments Incorporated

5 Device Comparison Table

PART NUMBER	OUTPUT VOLTAGE	POWER GOOD LOGIC LEVEL (EN = LOW)
TPS62150	Adjustable	High Impedance
TPS62150A	Adjustable	Low
TPS62151	1.8 V	High Impedance
TPS62152	3.3 V	High Impedance
TPS62153	5.0 V	High Impedance

6 Pin Configuration and Functions

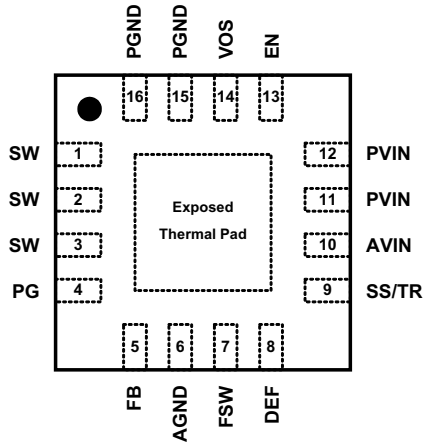


図 6-1. 16-Pin VQFN With Thermal Pad RGT Package (Top View)

表 6-1. Pin Functions

PIN(1)		I/O	DESCRIPTION
NO.	NAME		
1,2,3	SW	O	Switch node, which is connected to the internal MOSFET switches. Connect the inductor between SW and output capacitor.
4	PG	O	Output power good (high = V_{OUT} ready, low = V_{OUT} below nominal regulation); open drain (requires pullup resistor)
5	FB	I	Voltage feedback of the adjustable version. Connect a resistive voltage divider to this pin. It is recommended to connect FB to AGND on fixed output voltage versions for improved thermal performance.
6	AGND		Analog Ground. Must be connected directly to the exposed thermal pad and common ground plane.
7	FSW	I	Switching Frequency Select (low is approximately 2.5 MHz, high is approximately 1.25 MHz(2) for typical operation)(3)
8	DEF	I	Output Voltage Scaling (low = nominal, high = nominal + 5%)(3)
9	SS/TR	I	Soft-Start / Tracking Pin. An external capacitor connected to this pin sets the internal voltage reference rise time. It can be used for tracking and sequencing.
10	AVIN	I	Supply voltage for control circuitry. Connect to same source as PVIN.
11,12	PVIN	I	Supply voltage for power stage. Connect to same source as AVIN.
13	EN	I	Enable input (high = enabled, low = disabled)(3)
14	VOS	I	Output voltage sense pin and connection for the control loop circuitry
15,16	PGND		Power Ground. Must be connected directly to the exposed thermal pad and common ground plane.
	Exposed Thermal Pad		Must be connected to AGND (pin 6), PGND (pin 15,16), and common ground plane. See the *Layout Example*. Must be soldered to achieve appropriate power dissipation and mechanical reliability.

(1) For more information about connecting pins, see セクション 8 and セクション 9.
(2) Connect FSW to V_{OUT} or PG in this case.
(3) An internal pulldown resistor keeps logic level low, if pin is floating.

Copyright © 2022 Texas Instruments Incorporated

7 Specifications

7.1 Absolute Maximum Ratings(1)

over operating junction temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Pin voltage(2)	AVIN, PVIN	–0.3	20	V
	EN, SS/TR	–0.3	V_{IN} + 0.3	
	SW	–0.3	V_{IN} + 0.3	
	DEF, FSW, FB, PG, VOS	–0.3	7	
Power-good sink current	PG		10	mA
Temperature	Operating junction temperature, T_J	–40	150	°C
	Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground terminal.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply Voltage, V_{IN} (at AVIN and PVIN)	3		17	V
Operating junction temperature, T_J	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS6215x RGT 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	45	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	53.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	17.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	4.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

Copyright © 2022 Texas Instruments Incorporated

7.5 Electrical Characteristics

over operating junction temperature (T_J = –40°C to 125°C), typical values at V_{IN} = 12 V and T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
SUPPLY							
V_{IN}	Input voltage range(1)			3		17	V
I_Q	Operating quiescent current	EN = High, I_{OUT} = 0 mA, device not switching			17	30	µA
			T_A = –40°C to +85°C		17	25	
I_{SD}	Shutdown current(2)	EN = Low			1.5	25	µA
			T_A = –40°C to +85°C		1.5	4	
V_{UVLO}	Undervoltage lockout threshold	Falling input voltage (PWM mode operation)		2.6	2.7	2.8	V
		Hysteresis			200		mV
T_{SD}	Thermal shutdown temperature				160		°C
	Thermal shutdown hysteresis				20		
CONTROL (EN, DEF, FSW, SS/TR, PG)							
V_H	High level input threshold voltage (EN, DEF, FSW)			0.9	0.65		V
V_L	Low level input threshold voltage (EN, DEF, FSW)				0.45	0.3	V
I_{LKG}	Input leakage current (EN, DEF, FSW)	EN = V_{IN} or GND; DEF, FSW = V_{OUT} or GND			0.01	1	µA
V_{TH_PG}	Power-good threshold voltage	Rising (%V_{OUT})		92%	95%	98%	
		Falling (%V_{OUT})		87%	90%	94%	
V_{OL_PG}	Power-good output low voltage	I_{PG} = –2 mA			0.07	0.3	V
I_{LKG_PG}	Input leakage current (PG)	V_{PG} = 1.8 V			1	400	nA
$I_{SS/TR}$	SS/TR pin source current			2.3	2.5	2.7	µA
POWER SWITCH							
$r_{DS(on)}$	High-side MOSFET ON-resistance	V_{IN} ≥ 6 V			90	170	mΩ
		V_{IN} = 3 V			120		
	Low-side MOSFET ON-resistance	V_{IN} ≥ 6 V			40	70	mΩ
		V_{IN} = 3 V			50		
I_{LIMF}	High-side MOSFET forward current limit(3)	V_{IN} = 12 V, T_A = 25°C		1.4	1.7	2.2	A
OUTPUT							
I_{LKG_FB}	Input leakage current (FB)	TPS62150, V_{FB} = 0.8 V			1	100	nA
V_{OUT}	Output voltage range (TPS62150)	V_{IN} ≥ V_{OUT}		0.9		6.0	V
	DEF (output voltage programming)	DEF = 0 (GND)			V_{OUT}		
		DEF = 1 (V_{OUT})			V_{OUT} + 5%		
	Initial output voltage accuracy(4)	PWM mode operation, V_{IN} ≥ V_{OUT} + 1 V		785.6	800	814.4	mV
		PWM mode operation, V_{IN} ≥ V_{OUT} + 1 V, T_A = –10°C to 85°C		788.0	800	812.8	
		Power Save Mode operation, C_{OUT} = 22 µF		781.6	800	822.4	
	Load regulation(5)	V_{IN} = 12 V, V_{OUT} = 3.3 V, PWM mode operation			0.05		%/A
	Line regulation(5)	3 V ≤ V_{IN} ≤ 17 V, V_{OUT} = 3.3 V, I_{OUT} = 1 A, PWM mode operation			0.02		%/V

(1) The device is still functional down to undervoltage lockout (see parameter V_{UVLO}).
(2) Current into AVIN+PVIN pins
(3) This is the static current limit. It can be temporarily higher in applications due to internal propagation delay (see セクション 8.4.4).

Copyright © 2022 Texas Instruments Incorporated

(4) This is the accuracy provided at the FB pin for the adjustable V_{OUT} version (line and load regulation effects are not included). For the fixed voltage versions, the (internal) resistive divider is included.
(5) Line and load regulation depend on external component selection and layout (see 図 9-16 and 図 9-17).

7.6 Typical Characteristics

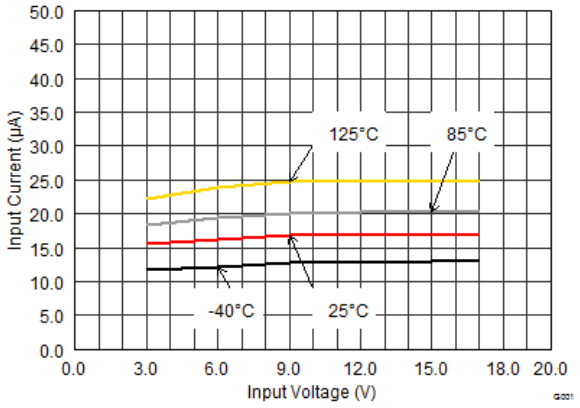


図 7-1. Quiescent Current

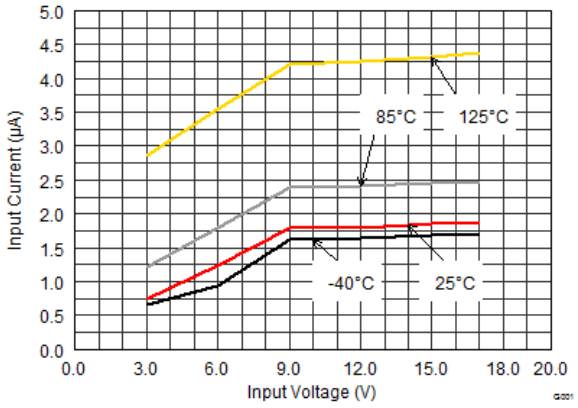


図 7-2. Shutdown Current

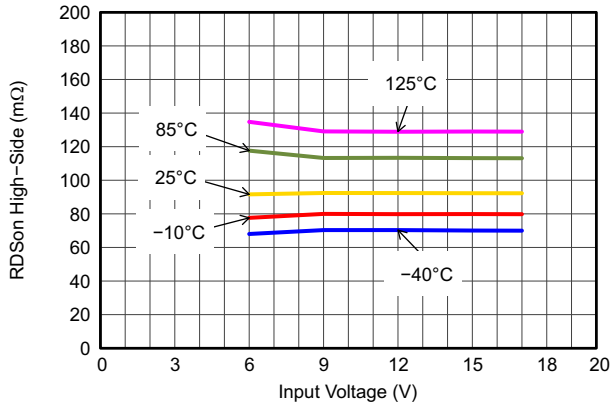


図 7-3. High-Side Switch Resistance

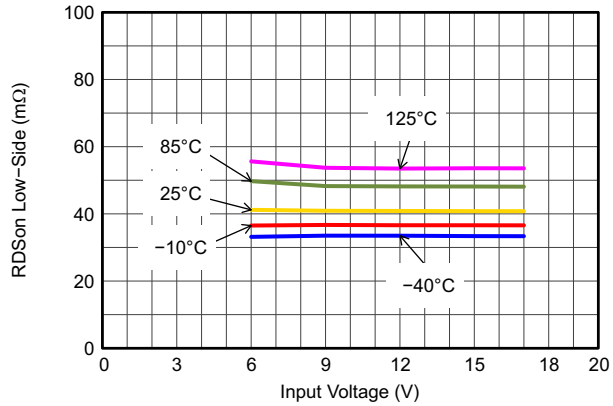


図 7-4. Low-Side Switch Resistance

Copyright © 2022 Texas Instruments Incorporated

8 Detailed Description

8.1 Overview

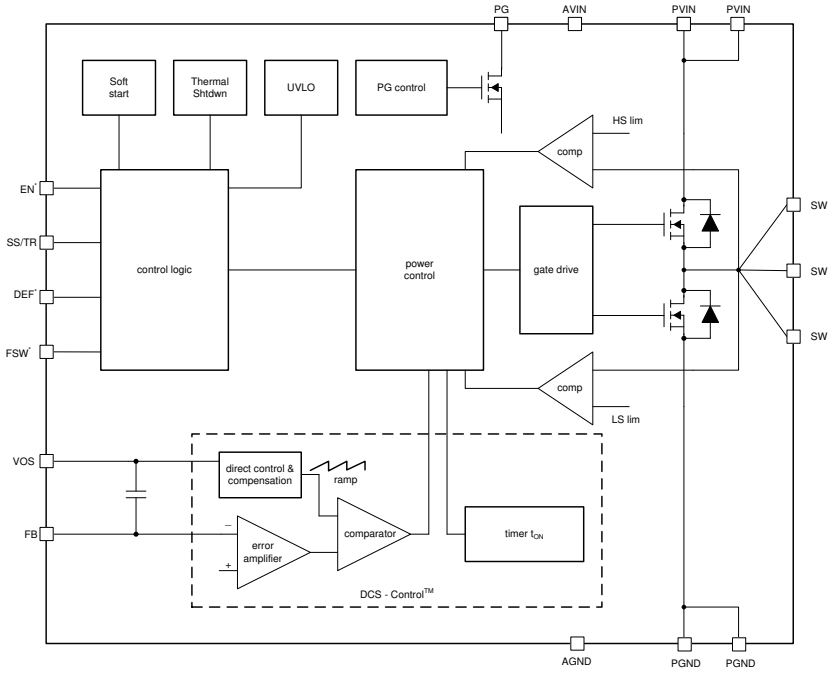
The TPS6215x synchronous switched-mode power converter is based on DCS-Control topology, an advanced regulation topology that combines the advantages of hysteretic, voltage-mode, and current-mode control, including an ac loop directly associated with the output voltage. This control loop takes information about output voltage changes and feeds that information directly to a fast comparator stage. It sets the switching frequency, which is constant for steady-state operating conditions, and provides immediate response to dynamic load changes. To get accurate dc load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low-ESR capacitors.

The DCS-Control topology supports pulse-width modulation (PWM) mode for medium and heavy load conditions and a power-save mode at light loads. During PWM, it operates at its nominal switching frequency in continuous-conduction mode. This frequency is typically about 2.5 MHz or 1.25 MHz, with a controlled frequency variation depending on the input voltage. If the load current decreases, the converter enters power-save mode to sustain high efficiency down to very light loads. In power-save mode, the switching frequency decreases linearly with the load current. Because DCS-Control topology supports both operation modes within a single building block, the transition from PWM to power-save mode is seamless without effects on the output voltage.

Fixed-output voltage versions provide the smallest solution size and lowest current consumption, requiring only three external components. An internal current limit supports nominal output currents of up to 1 A.

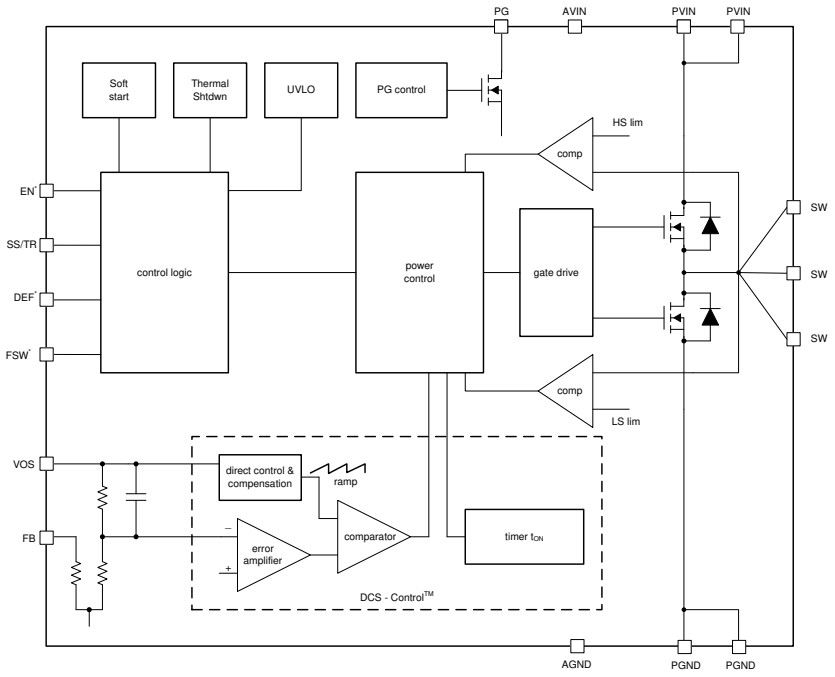
The TPS6215x offers both excellent dc voltage and superior load transient regulation, combined with very low output voltage ripple, minimizing interference with RF circuits.

8.2 Functional Block Diagrams



*This pin is connected to a pulldown resistor internally (see セクション 8.3)

図 8-1. TPS62150 (Adjustable Output Voltage)



*This pin is connected to a pulldown resistor internally (see セクション 8.3)

図 8-2. TPS62151, TPS62152, TPS62153 (Fixed Output Voltage)

8.3 Feature Description

8.3.1 Enable / Shutdown (EN)

When Enable (EN) is set high, the device starts operation. Shutdown is forced if EN is pulled low with a shutdown current of typically 1.5 µA. During shutdown, the internal power MOSFETs as well as the entire control circuitry are turned off. The internal resistive divider pulls down the output voltage smoothly. The EN signal must be set externally to high or low. An internal pulldown resistor of about 400 kΩ is connected and keeps EN logic low, if low is set initially and then the pin gets floating. It is disconnected if the pin is set high.

Connecting the EN pin to an appropriate output signal of another power rail provides sequencing of multiple power rails.

8.3.2 Soft Start or Tracking (SS/TR)

The internal soft-start circuitry controls the output voltage slope during start-up. This avoids excessive inrush current and ensures a controlled output-voltage rise time. It also prevents unwanted voltage drops from high-impedance power sources or batteries. When EN is set to start device operation, the device starts switching after a delay of about 50 µs, and V_{OUT} rises with a slope controlled by an external capacitor connected to the SS/TR pin. See 図 9-34 and 図 9-35 for typical start-up operation.

Using a very small capacitor (or leaving the SS/TR pin disconnected) provides fastest start-up behavior. There is no theoretical limit for the longest start-up time. The TPS6215x can start into a pre-biased output. During monotonic pre-biased start-up, both the power MOSFETs are not allowed to turn on until the internal ramp of the device sets an output voltage above the pre-bias voltage. If the device is set to shutdown (EN = GND), undervoltage lockout, or thermal shutdown, an internal resistor pulls the SS/TR pin down to ensure a proper low level. Returning from those states causes a new start-up sequence as set by the SS/TR connection.

A voltage supplied to SS/TR can be used for tracking a master voltage. The output voltage follows this voltage in both directions, up and down (see セクション 9).

8.3.3 Power Good (PG)

The TPS6215x has a built-in power-good (PG) function to indicate whether the output voltage has reached its appropriate level or not. One use of the PG signal can be for start-up sequencing of multiple rails. The PG pin is

Copyright © 2022 Texas Instruments Incorporated

an open-drain output that requires a pullup resistor (to any voltage below 7 V). It can sink 2 mA of current and maintain its specified logic-low level. With the TPS62150, it is high impedance when the device is turned off due to EN, UVLO, or thermal shutdown. The TPS62150A features PG = low in this case and can be used to actively discharge V_{OUT} (see 図 9-39). VIN must remain present for the PG pin to stay low. See the *TPS62130A Differences to TPS62130 Application Report* for application details. If not used, the PG pin should be connected to GND but can be left floating.

表 8-1. Power Good Pin Logic Table (TPS62150)

DEVICE STATE		PG LOGIC STATUS	
		HIGH IMPEDANCE	LOW
Enable (EN = high)	$V_{FB} \geq V_{TH_PG}$	√	
	$V_{FB} \leq V_{TH_PG}$		√
Shutdown (EN = low)		√	
UVLO	$0.7\ V < V_{IN} < V_{UVLO}$	√	
Thermal Shutdown	$T_J > T_{SD}$	√	
Power Supply Removal	$V_{IN} < 0.7\ V$	√	

表 8-2. Power Good Pin Logic Table (TPS62150A)

DEVICE STATE		PG LOGIC STATUS	
		HIGH IMPEDANCE	LOW
Enable (EN = high)	$V_{FB} \geq V_{TH_PG}$	√	
	$V_{FB} \leq V_{TH_PG}$		√
Shutdown (EN = low)			√
UVLO	$0.7\ V < V_{IN} < V_{UVLO}$		√
Thermal Shutdown	$T_J > T_{SD}$		√
Power Supply Removal	$V_{IN} < 0.7\ V$	√	

8.3.4 Pin-Selectable Output Voltage (DEF)

Setting the DEF pin to high increases the output voltage of the TPS62150x devices by 5% above the nominal voltage [1]. When DEF is low, the device regulates to the nominal output voltage. Increasing the nominal voltage allows adapting the power supply voltage to the variations of the application hardware. More detailed information on voltage margining using the TPS62150x device is in *Voltage Margining Using the TPS62130 Application Report*. The pin has an internally connected pulldown resistor of about 400 kΩ to ensure a proper logic level if the pin is high-impedance or floating after an initially low setting. Setting the pin high disconnects the resistor.

8.3.5 Frequency Selection (FSW)

To get high power density with a very small solution size, a high switching frequency allows the use of small external components for the output filter. However, switching losses increase with the switching frequency. If efficiency is the key parameter, more than solution size, the switching frequency can be set to half (1.25 MHz typical) by pulling FSW to High. It is mandatory to start with FSW = low to limit inrush current, which connecting FSW to V_{OUT} or PG can accomplish. Running with lower frequency produces higher efficiency, but also creates higher output-voltage ripple. Pull FSW to low for high-frequency operation (2.5 MHz typical). To get low ripple and full output current at the lower switching frequency, the recommended minimum inductor value is 2.2 µH. An application can change the switching frequency during operation, if needed. An internally-connected pulldown resistor of about 400 kΩ on this pin acts the same way as one on the DEF pin (see セクション 8.3.4).

8.3.6 Undervoltage Lockout (UVLO)

If the input voltage drops, the undervoltage lockout prevents faulty operation of the device by switching off both the power FETs. The typical undervoltage-lockout threshold setting is 2.7 V. The device is fully operational for

[1] Maximum allowed voltage is 7 V. Therefore, the recommended connection for DEF is to V_{OUT}, not V_{IN}.

Copyright © 2022 Texas Instruments Incorporated

voltages above the UVLO threshold and turns off if the input voltage trips the threshold. The converter starts operation again once the input voltage exceeds the threshold by a hysteresis of typically 200 mV.

8.3.7 Thermal Shutdown

An internal temperature sensor monitors the junction temperature (T_J) of the device. If T_J exceeds 160°C (typ.), the device goes into thermal shutdown. Both the high-side and low-side power FETs turn off and PG goes into the high-impedance state. When T_J decreases below the hysteresis level, the converter resumes normal operation, beginning with soft start. To avoid unstable conditions, the device implements a hysteresis of typically 20°C on the thermal shutdown temperature.

8.4 Device Functional Modes

8.4.1 Pulse-Width Modulation (PWM) Operation

The TPS6215x operates using pulse-width modulation in continuous-conduction mode (CCM) with a nominal switching frequency of 2.5 MHz or 1.25 MHz, selectable with the FSW pin. The frequency variation in the PWM mode is controlled and depends on V_{IN}, V_{OUT}, and the inductance. The device operates in PWM mode as long the output current is higher than half the inductor ripple current. To maintain high efficiency at light loads, the device enters power-save mode at the boundary of discontinuous conduction mode (DCM). This happens if the output current becomes smaller than half the inductor ripple current.

8.4.2 Power-Save Mode Operation

The TPS6215x enters its built-in power-save mode seamlessly if the load current decreases. This secures a high efficiency in light load operation. The device remains in power-save mode as long as the inductor current is discontinuous.

In power-save mode, the switching frequency decreases linearly with the load current, maintaining high efficiency. The transition into and out of power-save mode happens within the entire regulation scheme and is seamless in both directions.

TPS6215x includes a fixed on-time circuitry. An estimate for this on-time, in steady-state operation with F_{SW} = low, is:

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times 400\ \text{ns} \tag{1}$$

For very small output voltages, an absolute minimum on-time of about 80 ns is kept to limit switching losses. The operating frequency is thereby reduced from its nominal value, which keeps efficiency high. Also, the off-time can reach its minimum value at high duty cycles. The output voltage remains regulated in such cases. Using t_{ON}, the typical peak inductor current in power-save mode is approximated by:

$$I_{LPSM(peak)} = \frac{(V_{IN} - V_{OUT})}{L} \times t_{ON} \tag{2}$$

When V_{IN} decreases to typically 15% above V_{OUT}, the TPS62150x device does not enter power-save mode, regardless of the load current. The device maintains output regulation in PWM mode.

8.4.3 100% Duty-Cycle Operation

The duty cycle of the buck converter is given by D = V_{OUT} / V_{IN} and increases as the input voltage comes close to the output voltage. In this case, the device starts 100% duty cycle operation turning on the high-side switch 100% of the time. The high-side switch stays turned on as long as the output voltage is below the internal set

Copyright © 2022 Texas Instruments Incorporated

point. This allows the conversion of small input-to-output voltage differences, for example, for longest operation time of battery-powered applications. In 100% duty cycle mode, the low-side FET is switched off.

The minimum input voltage to maintain output voltage regulation, depending on the load current and the output voltage level, is calculated as:

$$V_{IN(min)} = V_{OUT(min)} + I_{OUT} \times \left(R_{DS(on)} + R_L\right) \quad (3)$$

where

- I_{OUT} is the output current
- $R_{DS(on)}$ is the on-state resistance of the high-side FET
- R_L is the dc resistance of the inductor

8.4.4 Current-Limit and Short-Circuit Protection

The TPS6215x devices have protection against heavy-load and short-circuit events. At heavy loads, the current limit determines the maximum output current. If the current limit is reached, the high-side FET is turned off. Avoiding shoot-through current, then the low-side FET switches on to allow the inductor current to decrease. The low-side current limit is typically 1.2 A. The high-side FET turns on again only if the current in the low-side FET has decreased below the low-side current-limit threshold.

The output current of the device is limited by the current limit (see セクション 7.5). Due to internal propagation delay, the actual current can exceed the static current limit during that time. The dynamic current limit is calculated as follows:

$$I_{peak(typ)} = I_{LIMF} + \frac{V_L}{L} \times t_{PD} \quad (4)$$

where

- I_{LIMF} is the static current limit, specified in the セクション 7.5
- V_L is the voltage across the inductor ($V_{IN} – V_{OUT}$)
- L is the inductor value
- t_{PD} is the internal propagation delay

The current limit can exceed static values, especially if the input voltage is high and the application uses very small inductances. Calculate the peak current in the dynamic high-side switch using the following equation:

$$I_{peak(typ)} = I_{LIMF} + \frac{\left(V_{IN} - V_{OUT}\right)}{L} \times 30\ ns \quad (5)$$

Copyright © 2022 Texas Instruments Incorporated

9 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The TPS6215x devices are a switched-mode step-down converters, able to convert a 3-V to 17-V input voltage into a 0.9-V to 6-V output voltage, providing up to 1 A. They require a minimum number of external components. Apart from the LC output filter and the input capacitors, only the TPS62150 device needs an additional resistive divider to set the output voltage level.

9.2 Typical Application

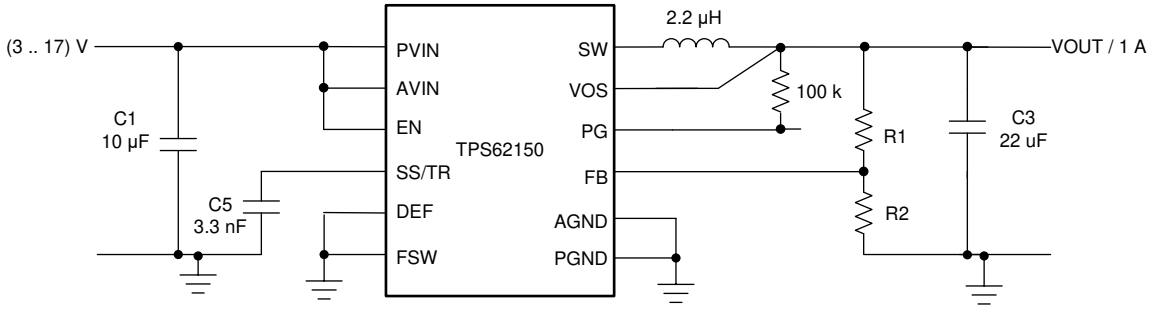


図 9-1. A Typical 1-A Step-Down Converter

9.2.1 Design Requirements

The following design guideline provides a component selection to operate the device within the recommended operating conditions. Using the FSW pin, the design can be optimized for highest efficiency or smallest solution size and lowest output-voltage ripple. For highest efficiency set F_{SW} = high, and the device operates at the lower switching frequency. For smallest solution size and lowest output voltage ripple set F_{SW} = low, and the device operates with higher switching frequency. The typical values for all measurements are V_{IN} = 12 V, V_{OUT} = 3.3 V, and T = 25°C, using the external components of 表 9-1.

The component selection used for measurements is given as follows:

表 9-1. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER(1)
IC	17-V, 1-A step-down converter, QFN	TPS62150RGT, Texas Instruments
L1	2.2-µH, 3.1-A, 0.165-in × 0.165-in (4.19-mm × 4.19-mm)	XFL4020-222MEB, Coilcraft
C1	10-µF, 25-V, ceramic, 1210	Standard
C3	22-µF, 6.3-V, ceramic, 0805	Standard
C5	3300-pF, 25-V, ceramic, 0603	
R1	Depending on V_{OUT}	
R2	Depending on V_{OUT}	
R3	100-kΩ, chip, 0603, 1/16-W, 1%	Standard

(1) See *Third-Party Products* disclaimer

Copyright © 2022 Texas Instruments Incorporated

9.2.2 Detailed Design Procedure

9.2.2.1 Programming the Output Voltage

The output voltage of the TPS62150 (TPS62150A) is adjustable and the TPS62151, TPS62152, and TPS62153 are programmed to fixed output voltages. For fixed output versions, the FB pin is pulled down internally and can be left floating. It is recommended to connect the FB pin to AGND to decrease thermal resistance. The adjustable version can be programmed for output voltages from 0.9 V to 6 V by using a resistive divider from V_{OUT} to AGND. The voltage at the FB pin is regulated to 800 mV. The value of the output voltage is set by the selection of the resistive divider from 式 6. It is recommended to choose resistor values which allow a current of at least 2 µA, meaning the value of R2 should not exceed 400 kΩ. Lower resistor values are recommended for highest accuracy and most robust design. For applications requiring lowest current consumption, the use of fixed-output-voltage versions is recommended.

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \tag{6}$$

In case of an open on the FB pin, the device clamps the output voltage at the VOS pin internally to about 7.4 V.

9.2.2.2 External Component Selection

The external components must fulfill the needs of the application, but also the stability criteria for the control loop of the device. The TPS6215x device is optimized to work within a range of external components. Consider the inductance and capacitance of the LC output filters in conjunction, creating the double pole responsible for the corner frequency of the converter (see セクション 9.2.2.4). 表 9-2 can be used to simplify the output filter component selection. Checked cells represent combinations that are proven for stability by simulation and lab test. Further combinations should be checked for each individual application. See the *Optimizing the TPS62130/40/50/60 Output Filter Application Report* for details.

表 9-2. L-C Output Filter Combinations

	4.7 µF(1)	10 µF	22 µF	47 µF	100 µF	200 µF	400 µF
0.47 µH							
1 µH			√	√	√	√	
2.2 µH		√	√(2)	√	√	√	
3.3 µH		√	√	√	√		
4.7 µH							

(1) The values in the table are nominal values. The effective capacitance was considered to vary by +20% and -50%.
(2) This LC combination is the standard value, and is recommended for most applications.

The TPS6215x device can operate with an inductor as low as 1 µH or 2.2 µH. F_{SW} should be set low in this case. However, for applications running with the low-frequency setting (F_{SW} = high) or with low input voltages, 3.3 µH is recommended.

9.2.2.2.1 Inductor Selection

The inductor selection is affected by several effects like inductor ripple current, output ripple voltage, PWM-to-PSM transition point, and efficiency. In addition, the inductor selected must be rated for appropriate saturation current and dc resistance (DCR). 式 7 and 式 8 calculate the maximum inductor current under static load conditions.

$$I_{L(max)} = I_{OUT(max)} + \frac{\Delta I_{L(max)}}{2} \tag{7}$$

Copyright © 2022 Texas Instruments Incorporated

$$\Delta I_{L(max)} = V_{OUT} \times \left(\frac{1 - \frac{V_{OUT}}{V_{IN(max)}}}{L_{(min)} \times f_{SW}} \right) \quad (8)$$

where

- I_L(max) is the maximum inductor current
- ΔI_L is the peak-to-peak inductor ripple current
- L(min) is the minimum effective inductor value
- f_{SW} is the actual PWM switching frequency

Calculating the maximum inductor current using the actual operating conditions gives the minimum required saturation current of the inductor. An added margin of about 20% is recommended. A larger inductor value is also useful to get lower ripple current, but increases the transient response time and size as well. The following inductors have been used with the TPS6215x device and are recommended for use:

表 9-3. List of Inductors

TYPE	INDUCTANCE [µH]	SATURATION CURRENT [A](1)	DIMENSIONS [L × W× H, mm	MANUFACTURER(2)
XFL4020-222ME_	2.2 µH, ±20%	3.5	4 × 4 × 2.1	Coilcraft
XFL3012-222MEC	2.2 µH, ±20%	1.6	3 × 3 × 1.2	Coilcraft
XFL3012-332MEC	2.2 µH, ±20%	1.4	3 × 3 × 1.2	Coilcraft
VLS252012T-2R2M1R3	2.2 µH, ±20%	1.3	2.5 × 2 × 1.2	TDK
LPS3015-332	2.2 µH, ±20%	1.4	3 × 3 × 1.4	Coilcraft
744025003	2.2 µH, ±20%	1.5	2.8 × 2.8 × 2.8	Wuerth
PSI25201B-2R2MS	2.2 µH, ±20%	1.3	2 × 2.5 × 1.2	Cyntec
NR3015T-2R2M	2.2 µH, ±20%	1.5	3 × 3 × 1.5	Taiyo Yuden

(1) Lower of I_{RMS} at 40°C rise or I_{SAT} at 30% drop.
(2) See the *Third Party Disclaimer*.

$$I_{load(PSM)} = \frac{1}{2} \Delta I_L \quad (9)$$

Using 式 9, this current level can be adjusted by changing the inductor value.

9.2.2.2.2 Capacitor Selection

9.2.2.2.2.1 Output Capacitor

The recommended value for the output capacitor is 22 µF. The architecture of the TPS6215x device allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output-voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, it is recommended to use X7R or X5R dielectric. Using a higher value of output capacitance can have some advantages, like smaller voltage ripple and a tighter dc output accuracy in power-save mode (see the *Optimizing the TPS62130/40/50/60 Output Filter Application Report*).

Note

In power-save mode, the output-voltage ripple depends on the output capacitance, the ESR of the output capacitor, and the peak inductor current. Using ceramic capacitors provides small ESR and low ripple.

Copyright © 2022 Texas Instruments Incorporated

9.2.2.2.2 Input Capacitor

For most applications, 10 µF is sufficient and is recommended, though a larger value reduces input-current ripple further. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. A low-ESR multilayer ceramic capacitor is recommended for best filtering and should be placed between PVIN and PGND as close as possible to those pins. Even though AVIN and PVIN must be supplied from the same input source, it is recommended to place a capacitance of 0.1 µF from AVIN to AGND, to avoid potential noise coupling. An RC, low-pass filter from PVIN to AVIN may be used but is not required.

9.2.2.2.3 Soft-Start Capacitor

A capacitance connected between the SS/TR pin and AGND allows a user-programmable start-up slope of the output voltage. A constant-current source supplies 2.5 µA to charge the external capacitance. The capacitor required for a given soft-start ramp time for the output voltage is given by:

$$C_{SS} = t_{SS} \times \frac{2.5\ \mu A}{1.25\ V} \quad [F] \tag{10}$$

where

- C_{SS} is the capacitance (F) required at the SS/TR pin
- t_{SS} is the desired soft-start ramp time (s)

Note

DC bias effect: High capacitance ceramic capacitors have a DC bias effect, which has a strong influence on the final effective capacitnace. Therefore, selecting the right capacitor value requires careful choice. Package size and voltage rating in combination with delectric material are responsible for differences betweeen the rated capacitor value and the effective capacitance.

9.2.2.3 Tracking Function

If a tracking function is desired, the SS/TR pin can be used for this purpose by connecting it to an external tracking voltage. The output voltage tracks that voltage. If the tracking voltage is between 50 mV and 1.2 V, the FB pin will track the SS/TR pin voltage as described in 式 11 and shown in 図 9-2.

$$V_{FB} \approx 0.64 \times V_{SS/TR} \tag{11}$$

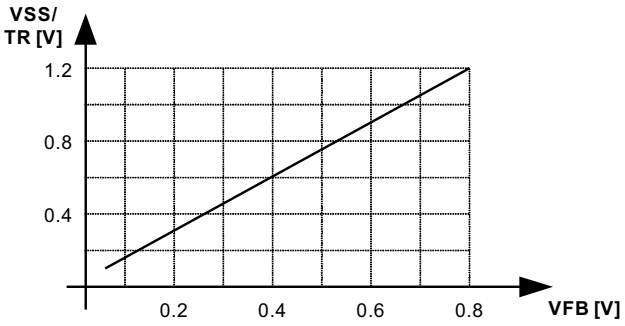


図 9-2. Voltage Tracking Relationship

Once the SS/TR pin voltage reaches about 1.2 V, the internal voltage is clamped to the internal feedback voltage and device goes to normal regulation. This works for rising and falling tracking voltages with the same behavior, as long as the input voltage is inside the recommended operating conditions. For decreasing SS/TR pin voltage,

Copyright © 2022 Texas Instruments Incorporated

the device does not sink current from the output. So, the resulting decrease of the output voltage may be slower than the SS/TR pin voltage if the load is light. When driving the SS/TR pin with an external voltage, do not exceed the voltage rating of the SS/TR pin, which is V_{IN} + 0.3 V.

If the input voltage drops into undervoltage lockout or even down to zero, the output voltage goes to zero, independent of the tracking voltage. 図 9-3 shows how to connect devices to get ratiometric and simultaneous sequencing by using the tracking function.

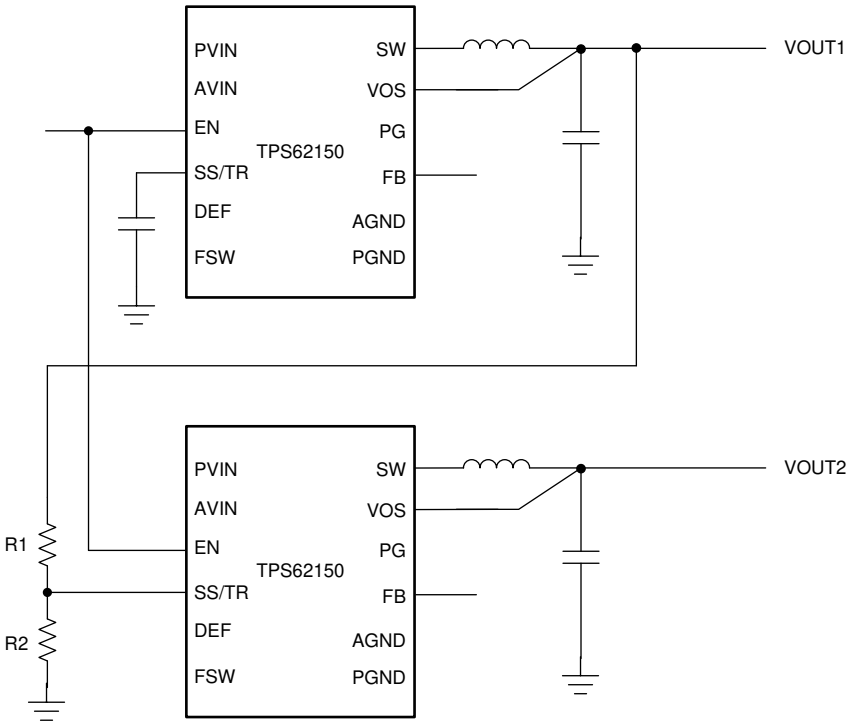


図 9-3. Schematic for Ratiometric and Simultaneous Start-Up

The resistive divider of R1 and R2 can be used to change the ramp rate of VOUT2 faster, slower, or the same as that of VOUT1.

A sequential start-up is achieved by connecting the PG pin of VOUT1 to the EN pin of VOUT2. A ratiometric start-up sequence happens if both supplies share the same soft-start capacitor. 式 10 calculates the soft-start time, though the SS/TR current must be doubled. Details about these and other tracking and sequencing circuits are found in *Sequencing and Tracking With the TPS621-Family and TPS821-Family Application Report*.

Note

If the voltage at the FB pin is below its typical value of 0.8 V, the output voltage accuracy can have a wider tolerance than specified.

9.2.2.4 Output Filter and Loop Stability

The devices of the TPS6215x family are internally compensated to be stable with L-C filter combinations corresponding to a corner frequency to be calculated with 式 12:

Copyright © 2022 Texas Instruments Incorporated

$$f_{LC} = \frac{1}{2\pi\sqrt{L \times C}} \quad (12)$$

Proven nominal values for inductance and ceramic capacitance are given in 表 9-2 and are recommended for use. Different values can work, but care must be taken on the loop stability, which is affected. More information, including a detailed L-C stability matrix, can be found in the *Optimizing the TPS62130/40/50/60 Output Filter Application Report*.

The TPS6215x devices, both fixed and adjustable versions, include an internal 25-pF feedforward capacitor, connected between the VOS and FB pins. This capacitor impacts the frequency behavior and sets a pole and zero in the control loop with the resistors of the feedback divider, per equations 式 13 and 式 14:

$$f_{zero} = \frac{1}{2\pi \times R_1 \times 25\ pF} \quad (13)$$

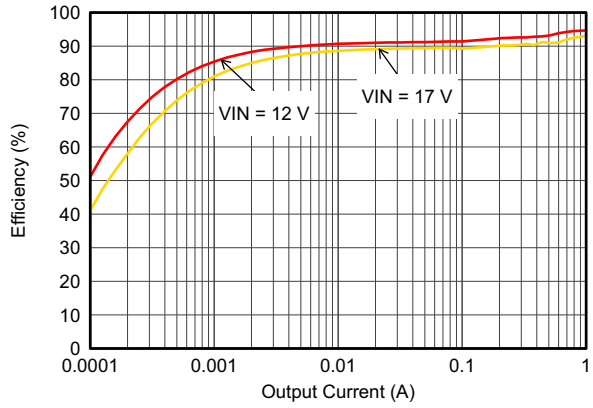
$$f_{pole} = \frac{1}{2\pi \times 25\ pF} \times \left(\frac{1}{R_1} + \frac{1}{R_2} \right) \quad (14)$$

Though the TPS6215x devices are stable without the pole and zero being in a particular location, adjusting their location to the specific needs of the application can provide better performance in power-save mode and/or improved transient response. An external feedforward capacitor can also be added. A more-detailed discussion on the optimization for stability versus transient response can be found in the *Optimizing Transient Response of Internally Compensated dc-dc Converters With Feedforward Capacitor* and *Using a Feedforward Capacitor to Improve Stability and Bandwidth of TPS62130/40/50/60/70* application reports.

Copyright © 2022 Texas Instruments Incorporated

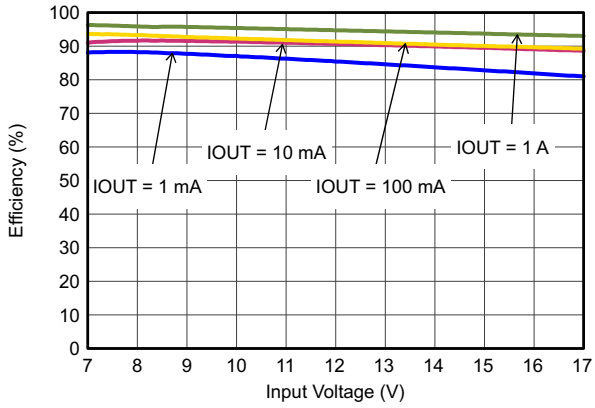
9.2.3 Application Curves

V_{IN}= 12 V, V_{OUT} = 3.3 V, T_A = 25°C, (unless otherwise noted)



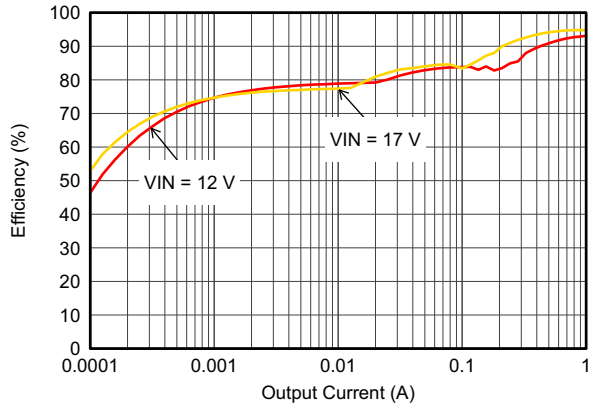
V_{OUT} = 5 V

図 9-4. Efficiency With 1.25 MHz



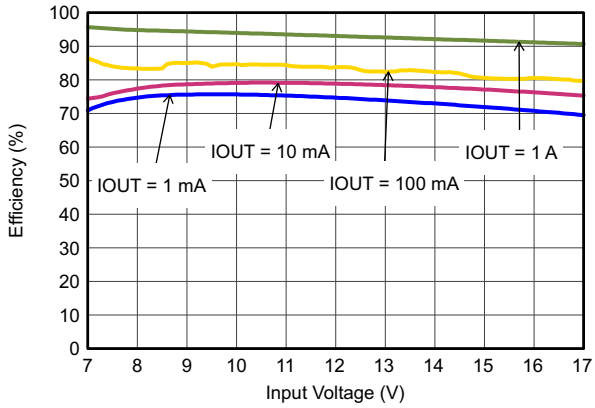
V_{OUT} = 5 V

図 9-5. Efficiency With 1.25 MHz



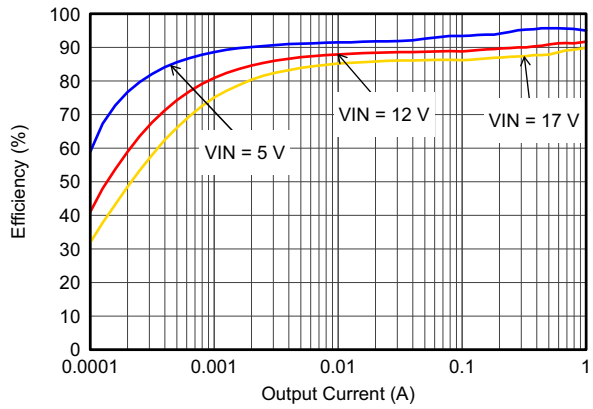
V_{OUT} = 5 V

図 9-6. Efficiency With 2.5 MHz



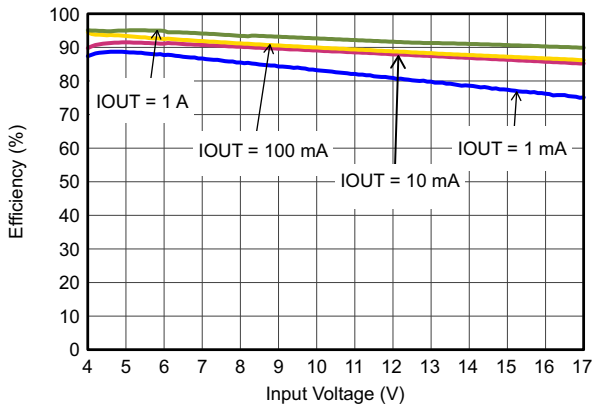
V_{OUT} = 5 V

図 9-7. Efficiency With 2.5 MHz



V_{OUT} = 3.3 V

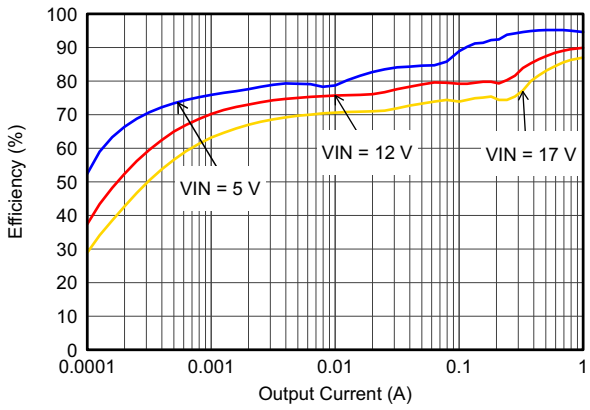
図 9-8. Efficiency With 1.25 MHz



V_{OUT} = 3.3 V

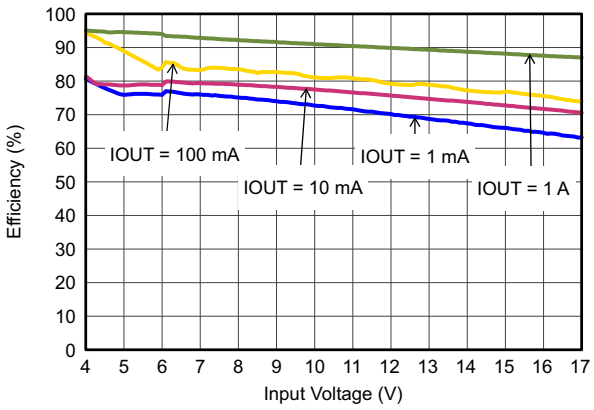
図 9-9. Efficiency With 1.25 MHz

Copyright © 2022 Texas Instruments Incorporated



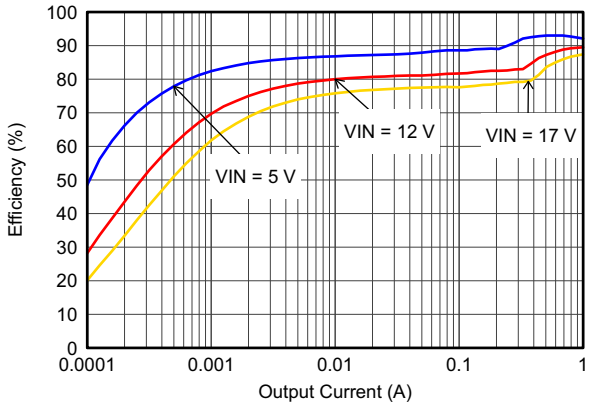
V_{OUT} = 3.3 V

図 9-10. Efficiency With 2.5 MHz



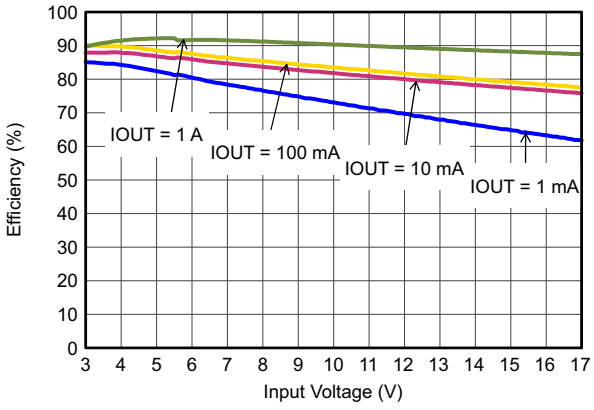
V_{OUT} = 3.3 V

図 9-11. Efficiency With 2.5 MHz



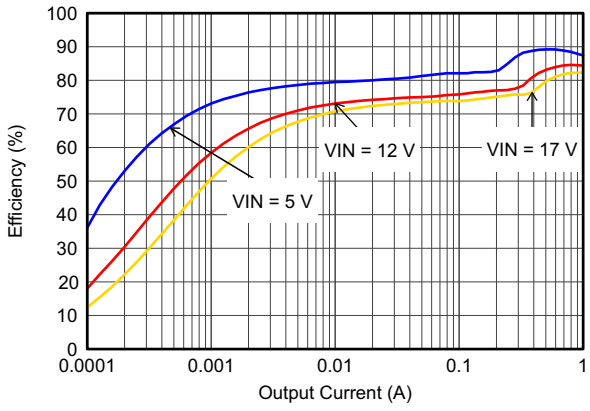
V_{OUT} = 1.8 V

図 9-12. Efficiency With 1.25 MHz



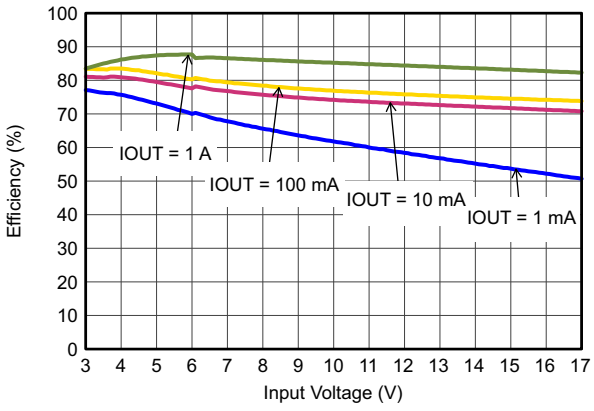
V_{OUT} = 1.8 V

図 9-13. Efficiency With 1.25 MHz



V_{OUT} = 0.9 V

図 9-14. Efficiency With 1.25 MHz



V_{OUT} = 0.9 V

図 9-15. Efficiency With 1.25 MHz

Copyright © 2022 Texas Instruments Incorporated

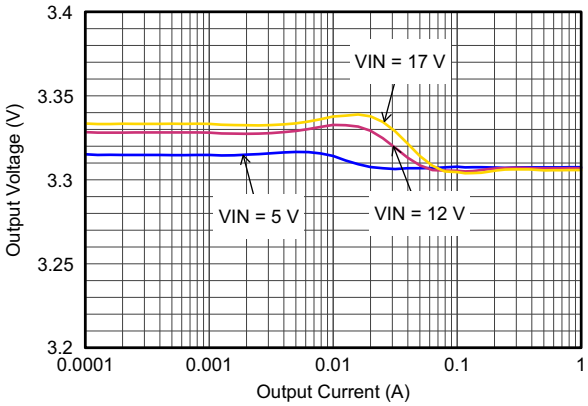


図 9-16. Output Voltage Accuracy (Load Regulation)

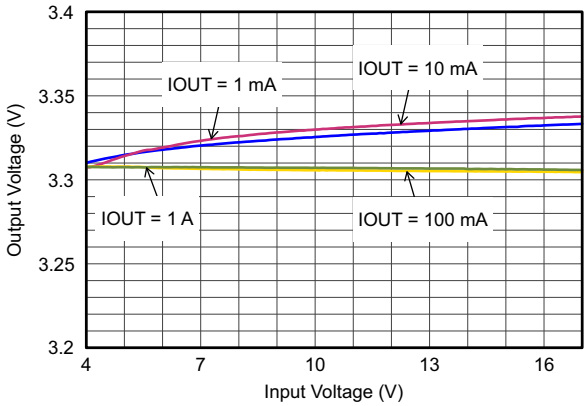
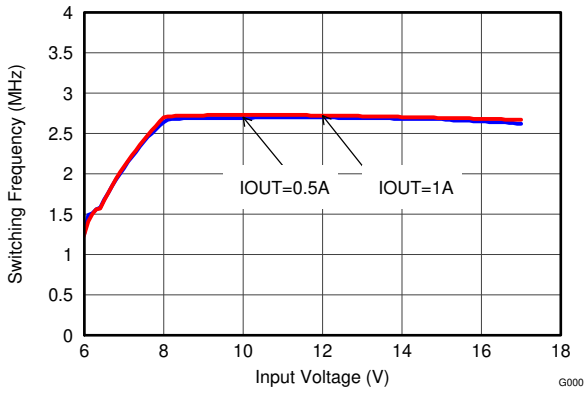
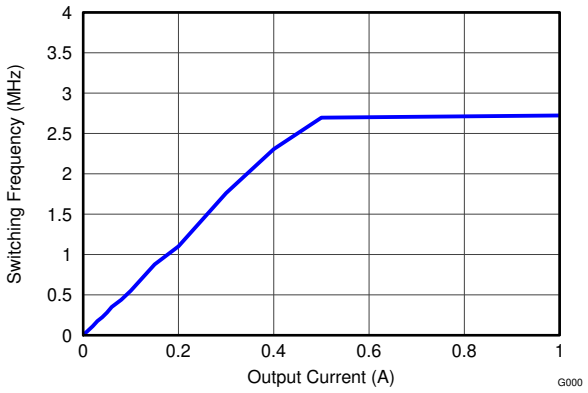


図 9-17. Output Voltage Accuracy (Line Regulation)



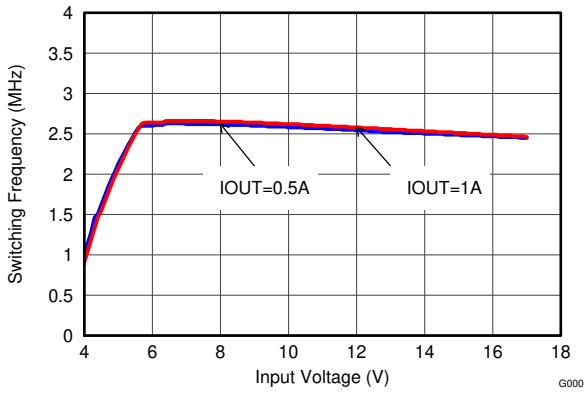
F_{SW} = low V_{OUT} = 5 V

図 9-18. Switching Frequency vs Input Voltage



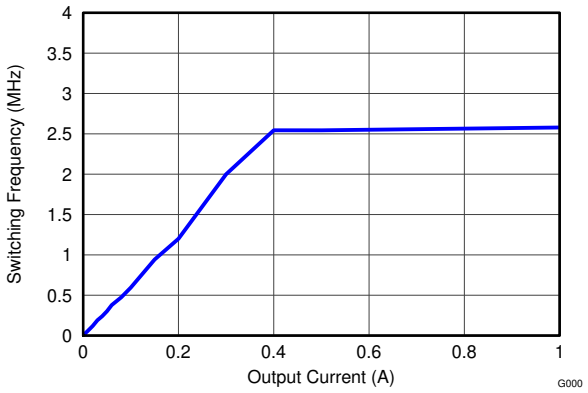
F_{SW} = low V_{OUT} = 0.9 V

図 9-19. Switching Frequency vs Output Current



F_{SW} = low V_{OUT} = 3.3 V

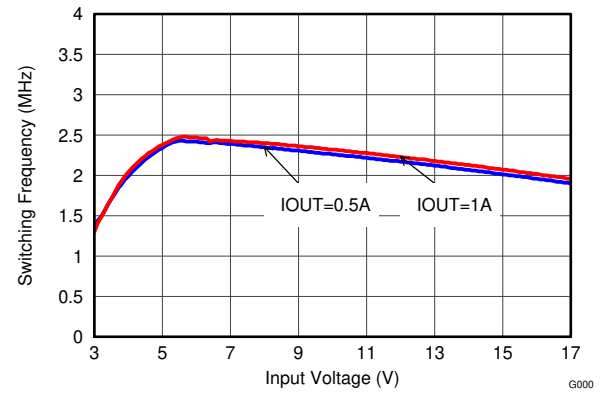
図 9-20. Switching Frequency vs Input Voltage



F_{SW} = low V_{OUT} = 3.3 V

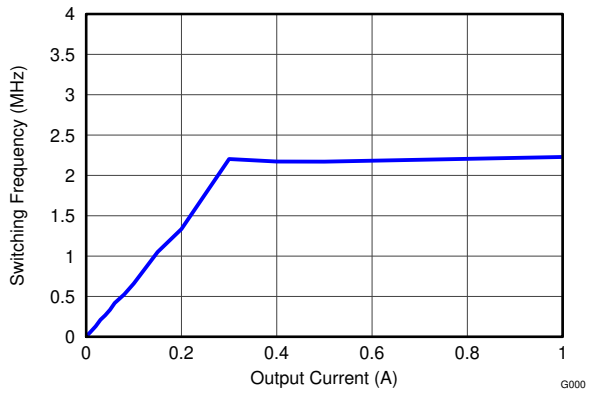
図 9-21. Switching Frequency vs Output Current

Copyright © 2022 Texas Instruments Incorporated



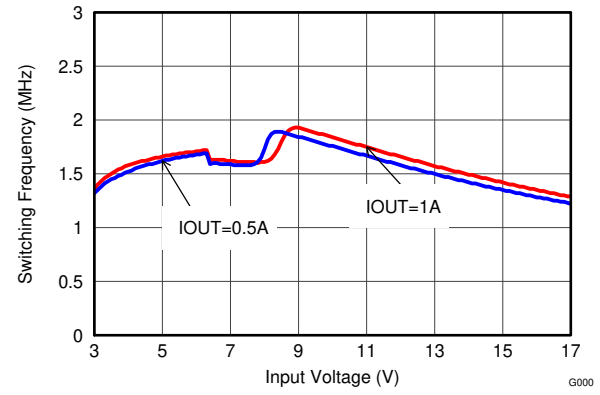
F_{SW} = low V_{OUT} = 1.8 V

図 9-22. Switching Frequency vs Input Voltage



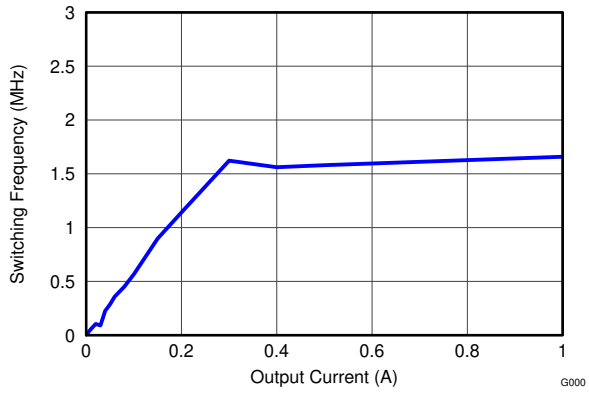
F_{SW} = low V_{OUT} = 1.8 V

図 9-23. Switching Frequency vs Output Current



F_{SW} = low V_{OUT} = 1 V

図 9-24. Switching Frequency vs Input Voltage



F_{SW} = low V_{OUT} = 1 V

図 9-25. Switching Frequency vs Output Current

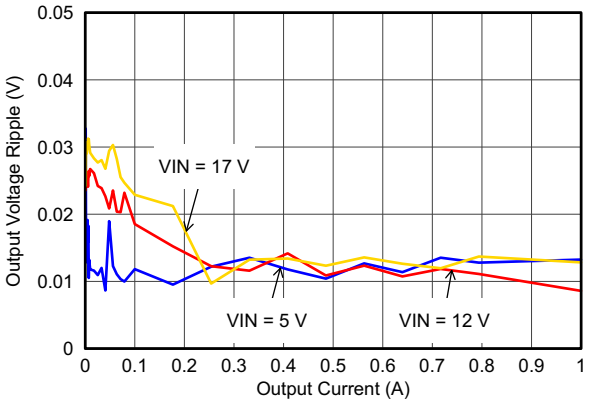


図 9-26. Output Voltage Ripple

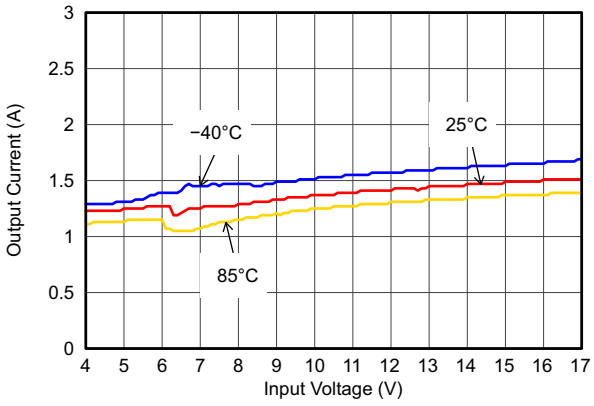
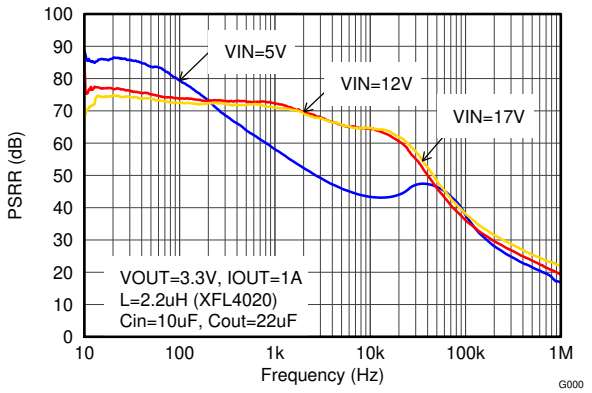
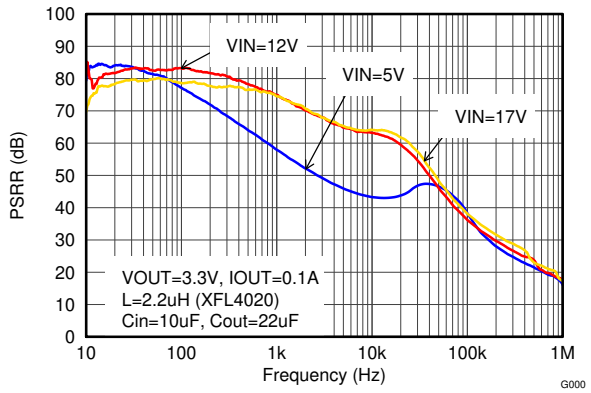


図 9-27. Maximum Output Current



I_{OUT} = 1 A f_{SW}= 2.5 MHz

図 9-28. Power-Supply Rejection Ratio



I_{OUT} = 0.1 A f_{SW} = 2.5 MHz

図 9-29. Power-Supply Rejection Ratio

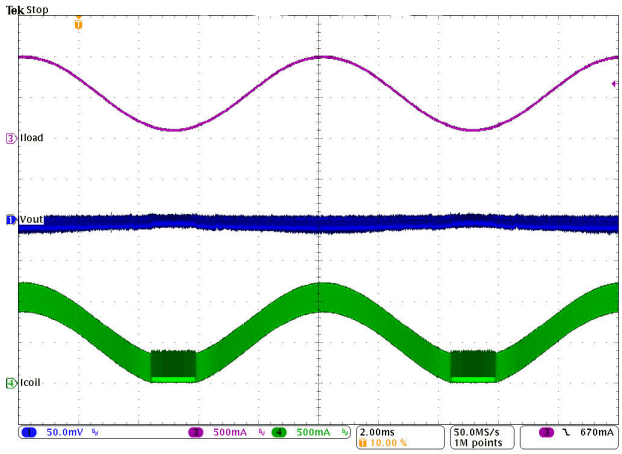


図 9-30. PWM-to-PSM Transition

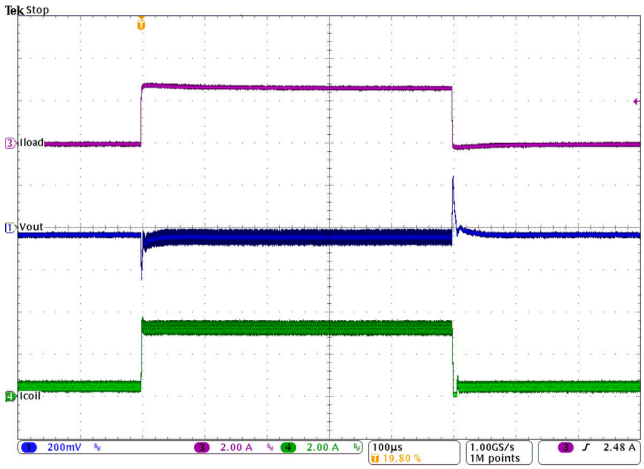


図 9-31. Load Transient Response

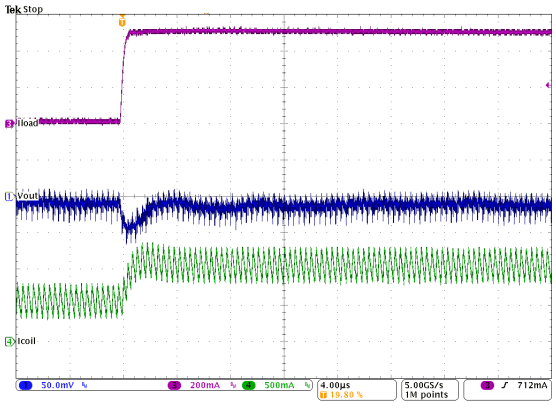


図 9-32. Load Transient Response, Rising Edge

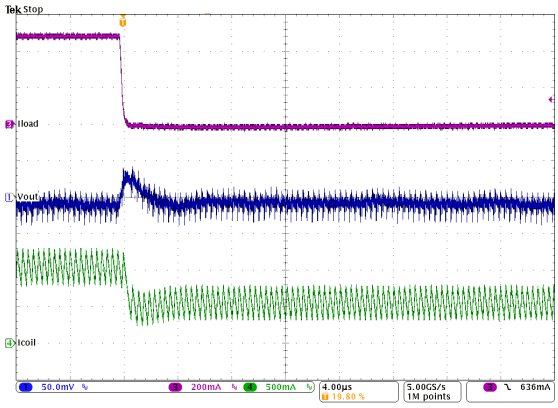


図 9-33. Load Transient Response, Falling Edge

Copyright © 2022 Texas Instruments Incorporated

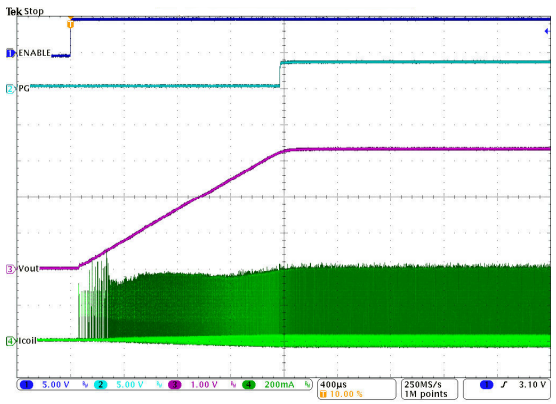


図 9-34. Start-Up Into 100 mA

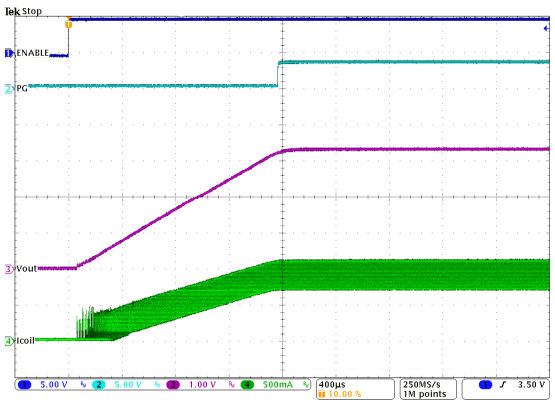
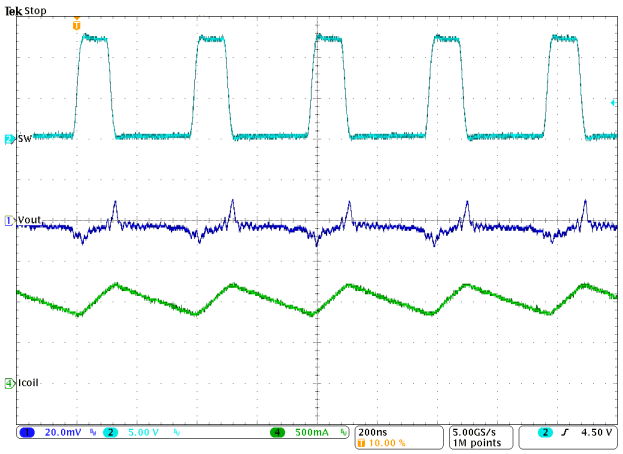
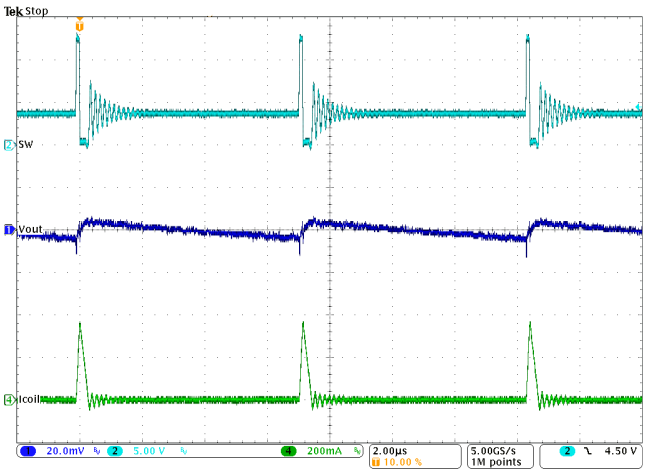


図 9-35. Start-Up Into 1 A



I_{OUT} = 1 A

図 9-36. Typical Operation in PWM Mode



I_{OUT} = 10 mA

図 9-37. Typical Operation in Power-Save Mode

9.3 System Examples

9.3.1 LED Power Supply

The TPS62150 can be used as a power supply for power LEDs. The FB pin can be easily set down to lower values than nominal by using the SS/TR pin. With that, the voltage drop on the sense resistor is low to avoid excessive power loss. Because this pin provides 2.5 µA, the feedback pin voltage can be adjusted by an external resistor per 式 15. This drop, proportional to the LED current, is used to regulate the output voltage (anode voltage) to a proper level to drive the LED. Both analog and PWM dimming are supported with the TPS62150. 図 9-38 shows an application circuit, tested with analog dimming:

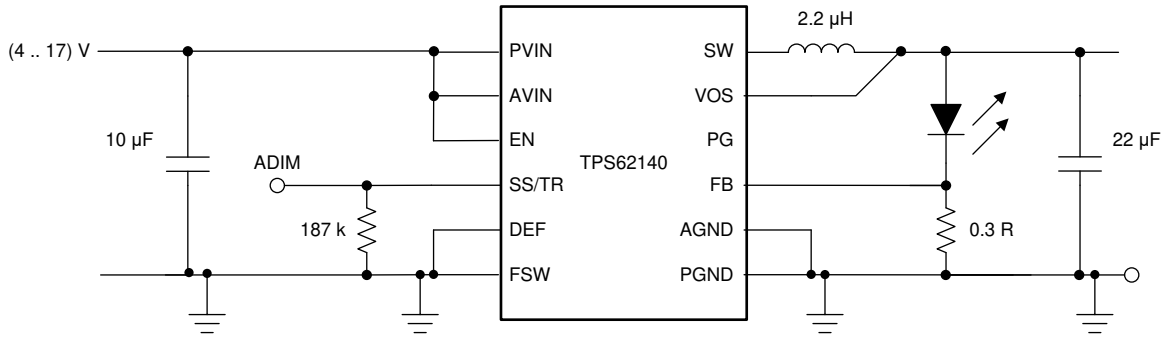


図 9-38. Single Power-LED Supply

The resistor at SS/TR sets the FB voltage to a level of about 300 mV, with a value calculated from 式 15.

$$V_{FB} = 0.64 \times 2.5\ \mu A \times R_{SS/TR} \quad (15)$$

The device now supplies a constant current, set by the resistor at the FB pin, by regulating the output voltage accordingly. The forward voltage requirement of the LED determines the minimum input voltage rating. More information is available in the *Using the TPS62150 as Step-Down LED Driver With Dimming Application Report*.

9.3.2 Active Output Discharge

The TPS62150A device pulls the PG pin Low when the device is shut down by EN, UVLO, or thermal shutdown. Connecting PG to V_{OUT} through a resistor can be used to discharge V_{OUT} in those cases (see 図 9-39). The discharge rate can be adjusted by R3, which is also used to pull up the PG pin in normal operation. For reliability, keep the maximum current into the PG pin less than 10 mA.

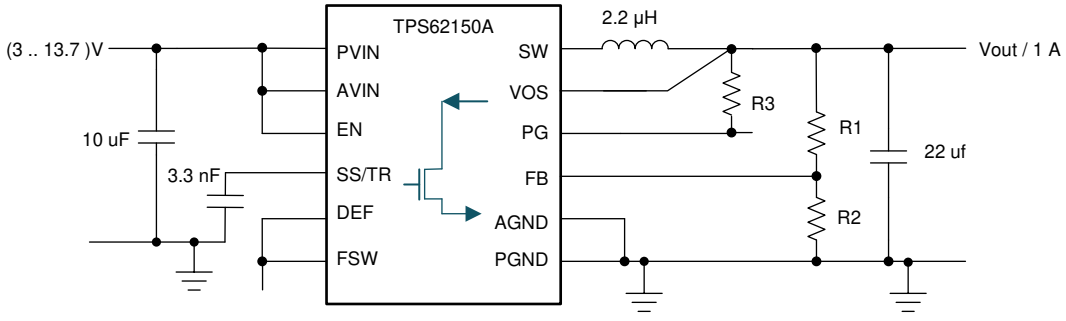


図 9-39. Discharge V_{OUT} Through PG Pin with TPS62150A

Copyright © 2022 Texas Instruments Incorporated

9.3.3 Inverting Power Supply

The TPS6215x device can be used as an inverting power supply by rearranging external circuitry as shown in 図 9-40. As the former GND node now represents a voltage level below system ground, the voltage difference between V_{IN} and V_{OUT} must be limited for operation to the maximum supply voltage of 17 V (see 式 16).

$$V_{IN} + \left|V_{OUT}\right| \le V_{IN\,max} \tag{16}$$

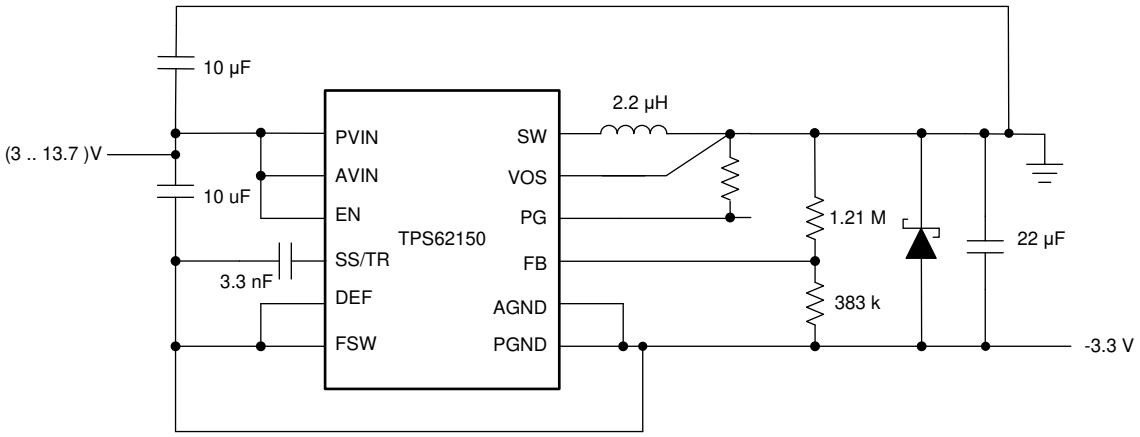


図 9-40. –3.3-V Inverting Power Supply

The transfer function of the inverting power supply configuration differs from the buck-mode transfer function, additionally incorporating a right half-plane zero. The loop stability must be adapted, and an output capacitance of at least 22 µF is recommended. A detailed design example is given in the *Using the TPS6215x in an Inverting Buck-Boost Topology Application Report*.

9.3.4 Various Output Voltages

The following example circuits show how to use the various devices and configure the external circuitry to furnish different output voltages at 1 A.

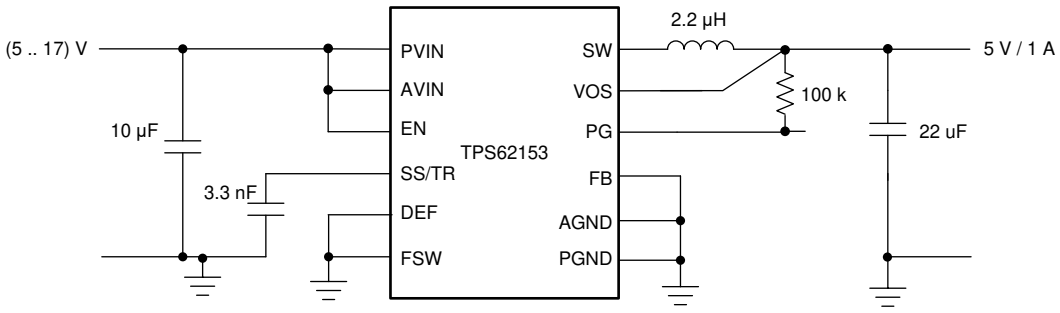


図 9-41. 5-V, 1-A Power Supply

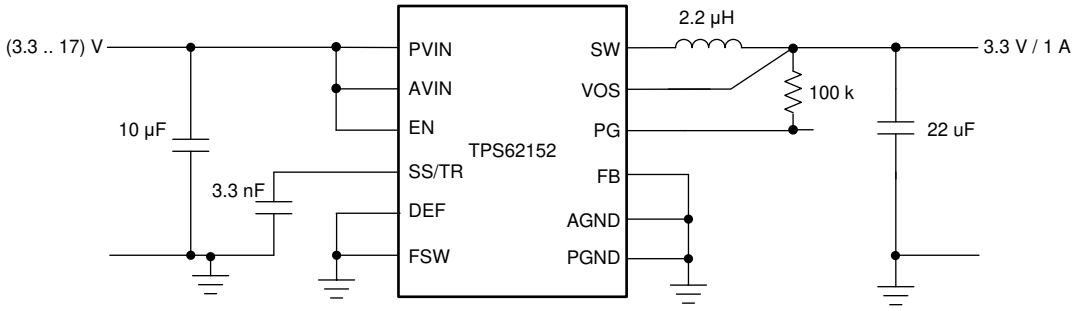


図 9-42. 3.3-V, 1-A Power Supply

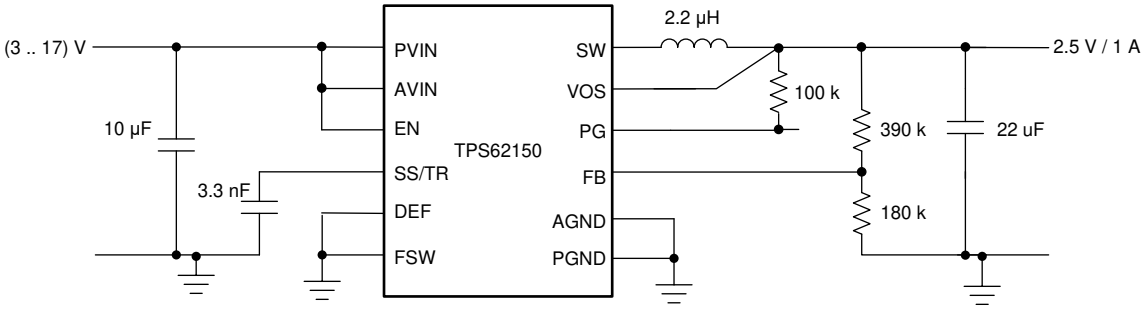


図 9-43. 2.5-V, 1-A Power Supply

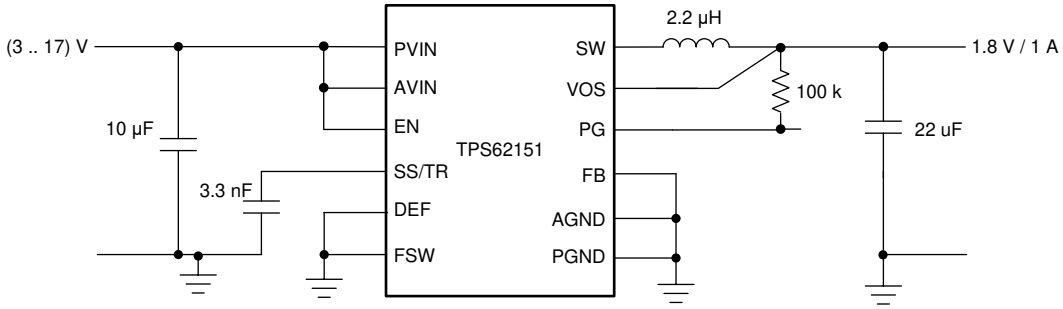


図 9-44. 1.8-V, 1-A Power Supply

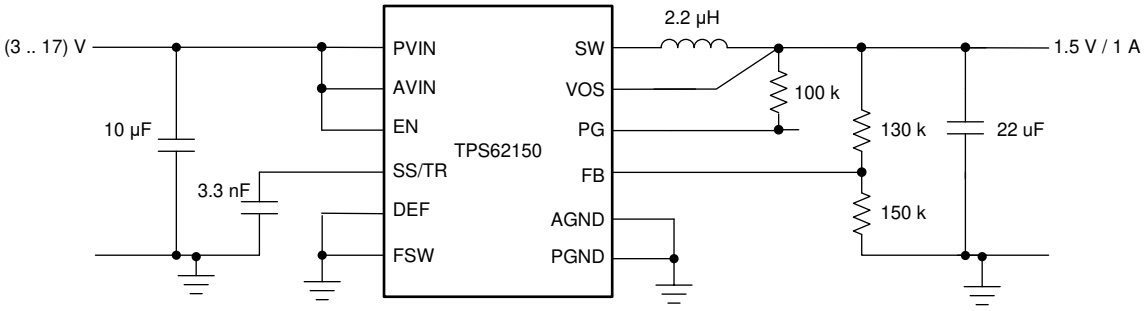


図 9-45. 1.5-V, 1-A Power Supply

Copyright © 2022 Texas Instruments Incorporated

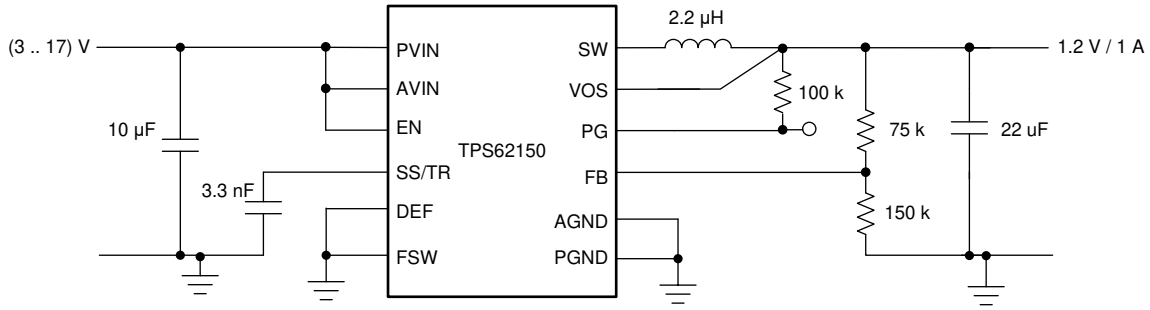


図 9-46. 1.2-V, 1-A Power Supply

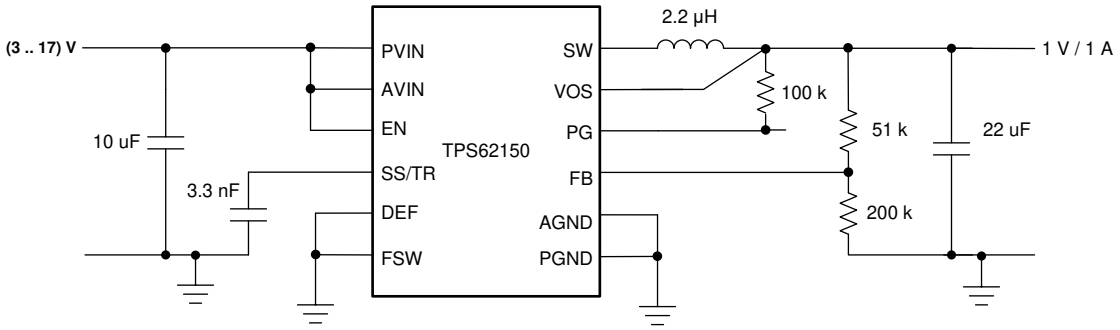


図 9-47. 1-V, 1-A Power Supply

10 Power Supply Recommendations

The TPS6215x devices are designed to operate from a 3-V to 17-V input voltage supply. The output current of the input power supply must be rated according to the output voltage and the output current of the power rail application.

Copyright © 2022 Texas Instruments Incorporated

11 Layout

11.1 Layout Guidelines

Proper layout is critical for the operation of a switched-mode power supply, even more at high switching frequencies. Therefore, the PCB layout of the TPS6215x device demands careful attention to ensure operation and to get the performance specified. A poor layout can lead to issues like poor regulation (both line and load), stability and accuracy weaknesses, increased EMI radiation, and noise sensitivity.

See 図 11-1 for the recommended layout of the TPS6215x device, which is designed for common external ground connections. Both AGND (pin 6) and PGND (pins 15 and 16) are directly connected to the exposed thermal pad. On the PCB, the direct common-ground connection of AGND and PGND to the exposed thermal pad and the system ground (ground plane) is mandatory. Also, connect VOS (pin 14) in the shortest way to V_{OUT} at the output capacitor. To avoid noise coupling into the VOS line, this connection should be separated from the V_{OUT} power line and plane as shown in セクション 11.2.

Provide low-inductance and -resistance paths for loops with high di/dt. Paths conducting the switched load current should be as short and wide as possible. Provide low-capacitance paths (with respect to all other nodes) for wires with high dv/dt. The input and output capacitance should be placed as close as possible to the IC pins, and parallel wiring over long distances as well as narrow traces should be avoided. Loops which conduct an alternating current should outline an area as small as possible, as this area is proportional to the energy radiated.

Sensitive nodes like FB (pin 5) and VOS (pin 14) must be connected with short wires and not near high dv/dt signals [for example, SW (pins 1, 2, and 3)]. As FB and VOS pins carry information about the output voltage, they should be connected as closely as possible to the actual output voltage (at the output capacitor). The capacitor on SS/TR (pin 9) and on AVIN (pin 19), as well as the FB resistors, R1 and R2, should be kept close to the IC and connect directly to those pins and the system ground plane.

The exposed thermal pad must be soldered to the circuit board for mechanical reliability and to achieve adequate power dissipation.

The recommended layout is implemented on the EVM and shown in its Users Guide, SLVU437. Additionally, the EVM Gerber data are available for download here, SLVC394.

11.2 Layout Example

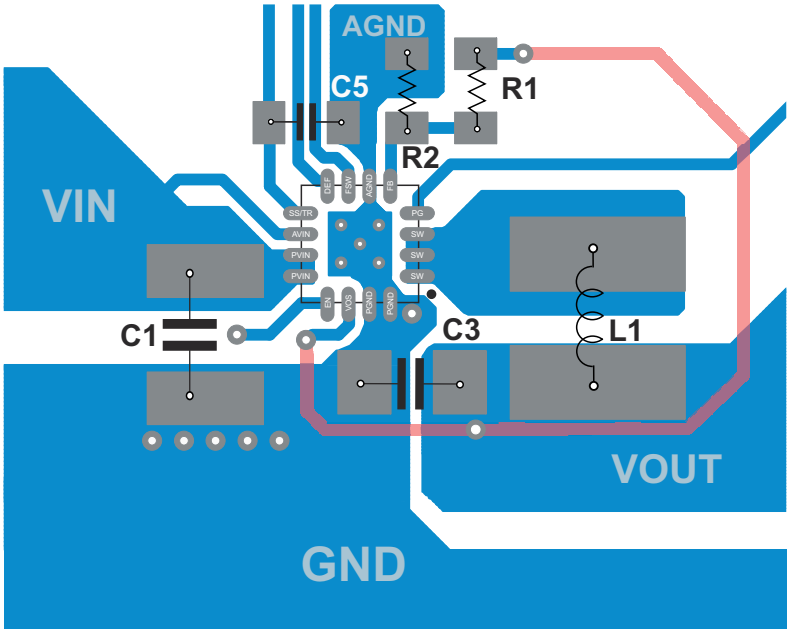


図 11-1. TPS6215x Example Layout

Copyright © 2022 Texas Instruments Incorporated

11.2.1 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks, and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB by soldering the exposed thermal pad
- Introducing airflow in the system

For more details on how to use the thermal parameters, see the *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* and *Semiconductor and IC Package Thermal Metrics* application reports.

The TPS6215x devices are designed for a maximum operating junction temperature (T_J) of 125°C. Therefore, the maximum output power is limited by the power losses that can be dissipated over the actual thermal resistance, given by the package and the surrounding PCB structures. Because the thermal resistance of the package is fixed, increasing the size of the surrounding copper area and improving the thermal connection to the IC can reduce the thermal resistance. To get improved thermal behavior, it is recommended to use top-layer metal to connect the device with wide and thick metal lines. Internal ground layers can connect to vias directly under the IC for improved thermal performance.

If short-circuit or overload conditions are present, the device is protected by limiting internal power dissipation.

Copyright © 2022 Texas Instruments Incorporated

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation, see the following:

- *Optimizing Transient Response of Internally Compensated dc-dc Converters With Feedforward Capacitor*, SLVA289
- *Using the TPS62150 as Step-Down LED Driver With Dimming*, SLVA451
- *Optimizing the TPS62130/40/50/60/70 Output Filter*, SLVA463
- *Using a Feedforward Capacitor to Improve Stability and Bandwidth of TPS62130/40/50/60/70*, SLVA466
- *Using the TPS6215x in an Inverting Buck-Boost Topology*, SLVA469
- *TPS62130/40/50 Sequencing and Tracking*, SLVA470
- *Voltage Margining Using the TPS62130*, SLVA489
- *TPS62130EVM-505, TPS62140EVM-505, and TPS62150EVM-505 Evaluation Modules User's Guide*, SLVU437
- *Semiconductor and IC Package Thermal Metrics*, SPRA953
- *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs*, SZZA017

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

12.5 Trademarks

DCS-Control™ and TI E2E™ are trademarks of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

Copyright © 2022 Texas Instruments Incorporated

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

Copyright © 2022 Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62150ARGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PA8I	Samples
TPS62150ARGTT	ACTIVE	VQFN	RGT	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PA8I	Samples
TPS62150RGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUA	Samples
TPS62150RGTT	ACTIVE	VQFN	RGT	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUA	Samples
TPS62151RGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QWO	Samples
TPS62151RGTT	ACTIVE	VQFN	RGT	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QWO	Samples
TPS62152RGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QWP	Samples
TPS62152RGTT	ACTIVE	VQFN	RGT	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QWP	Samples
TPS62153RGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QWQ	Samples
TPS62153RGTT	ACTIVE	VQFN	RGT	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QWQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

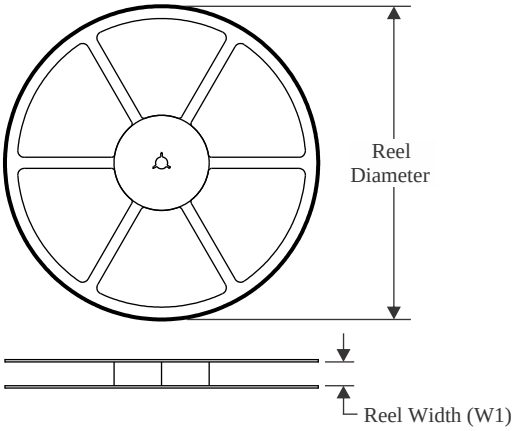
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

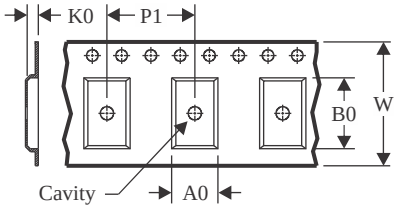
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

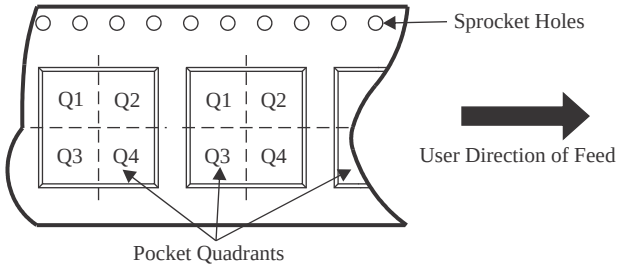


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

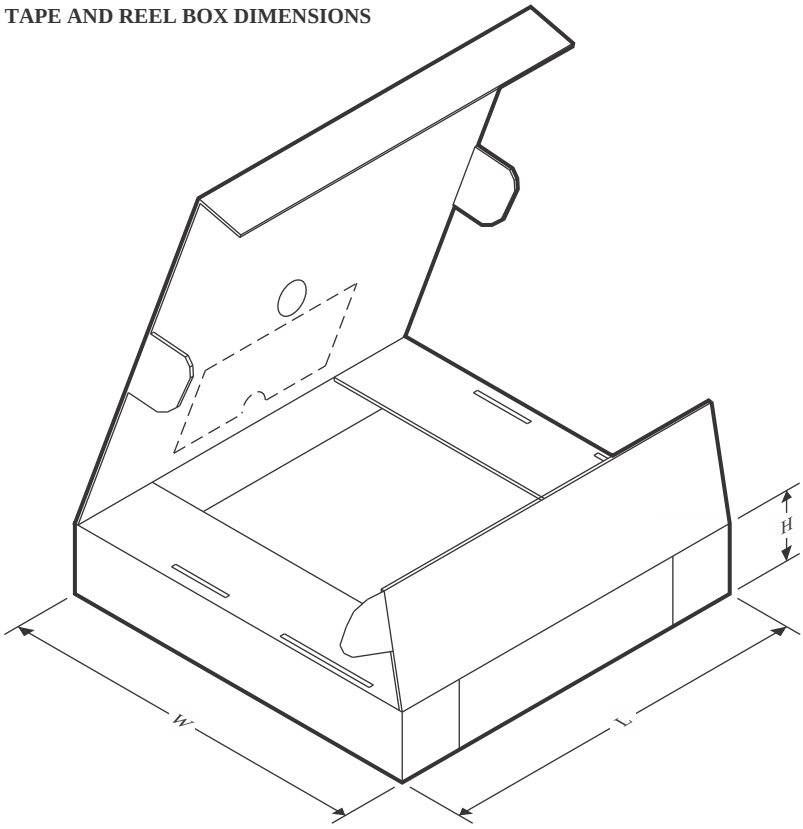
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62150ARGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62150ARGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62150RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62150RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62151RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62151RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62152RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62152RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62153RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62153RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

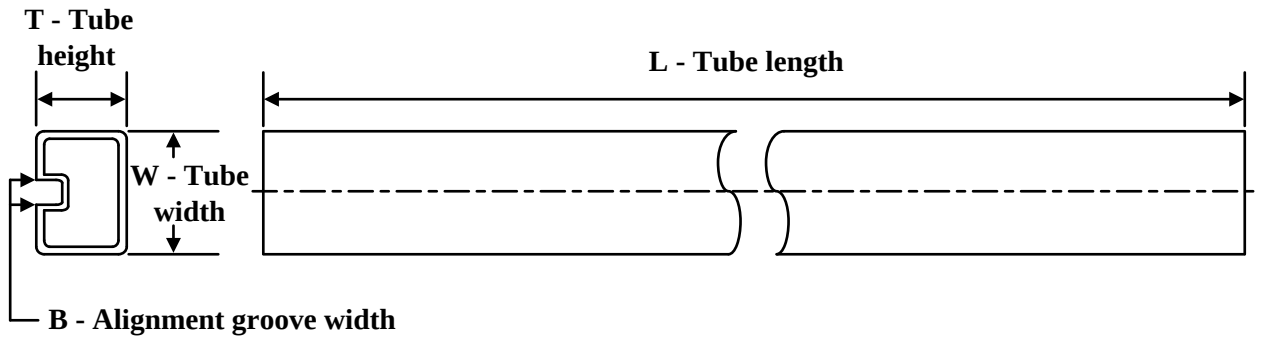
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62150ARGTR	VQFN	RGT	16	3000	367.0	367.0	35.0
TPS62150ARGTT	VQFN	RGT	16	250	210.0	185.0	35.0
TPS62150RGTR	VQFN	RGT	16	3000	552.0	346.0	36.0
TPS62150RGTT	VQFN	RGT	16	250	210.0	185.0	35.0
TPS62151RGTR	VQFN	RGT	16	3000	367.0	367.0	35.0
TPS62151RGTT	VQFN	RGT	16	250	210.0	185.0	35.0
TPS62152RGTR	VQFN	RGT	16	3000	367.0	367.0	35.0
TPS62152RGTT	VQFN	RGT	16	250	210.0	185.0	35.0
TPS62153RGTR	VQFN	RGT	16	3000	367.0	367.0	35.0
TPS62153RGTT	VQFN	RGT	16	250	210.0	185.0	35.0

TUBE

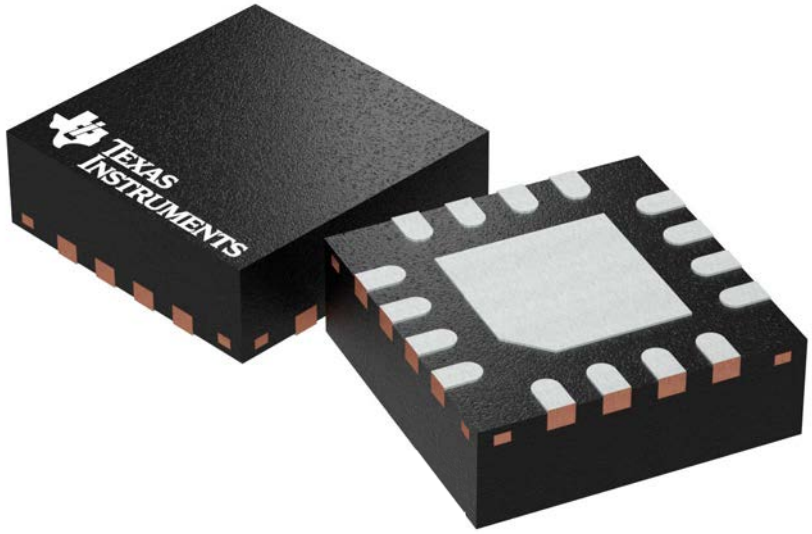


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS62150ARGTR	RGT	VQFN	16	3000	381	4.83	2286	0
TPS62150ARGTT	RGT	VQFN	16	250	381	4.83	2286	0
TPS62150RGTR	RGT	VQFN	16	3000	381	4.83	2286	0
TPS62150RGTT	RGT	VQFN	16	250	381	4.83	2286	0
TPS62151RGTR	RGT	VQFN	16	3000	381	4.83	2286	0
TPS62151RGTT	RGT	VQFN	16	250	381	4.83	2286	0
TPS62152RGTR	RGT	VQFN	16	3000	381	4.83	2286	0
TPS62152RGTT	RGT	VQFN	16	250	381	4.83	2286	0
TPS62153RGTR	RGT	VQFN	16	3000	381	4.83	2286	0
TPS62153RGTT	RGT	VQFN	16	250	381	4.83	2286	0

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



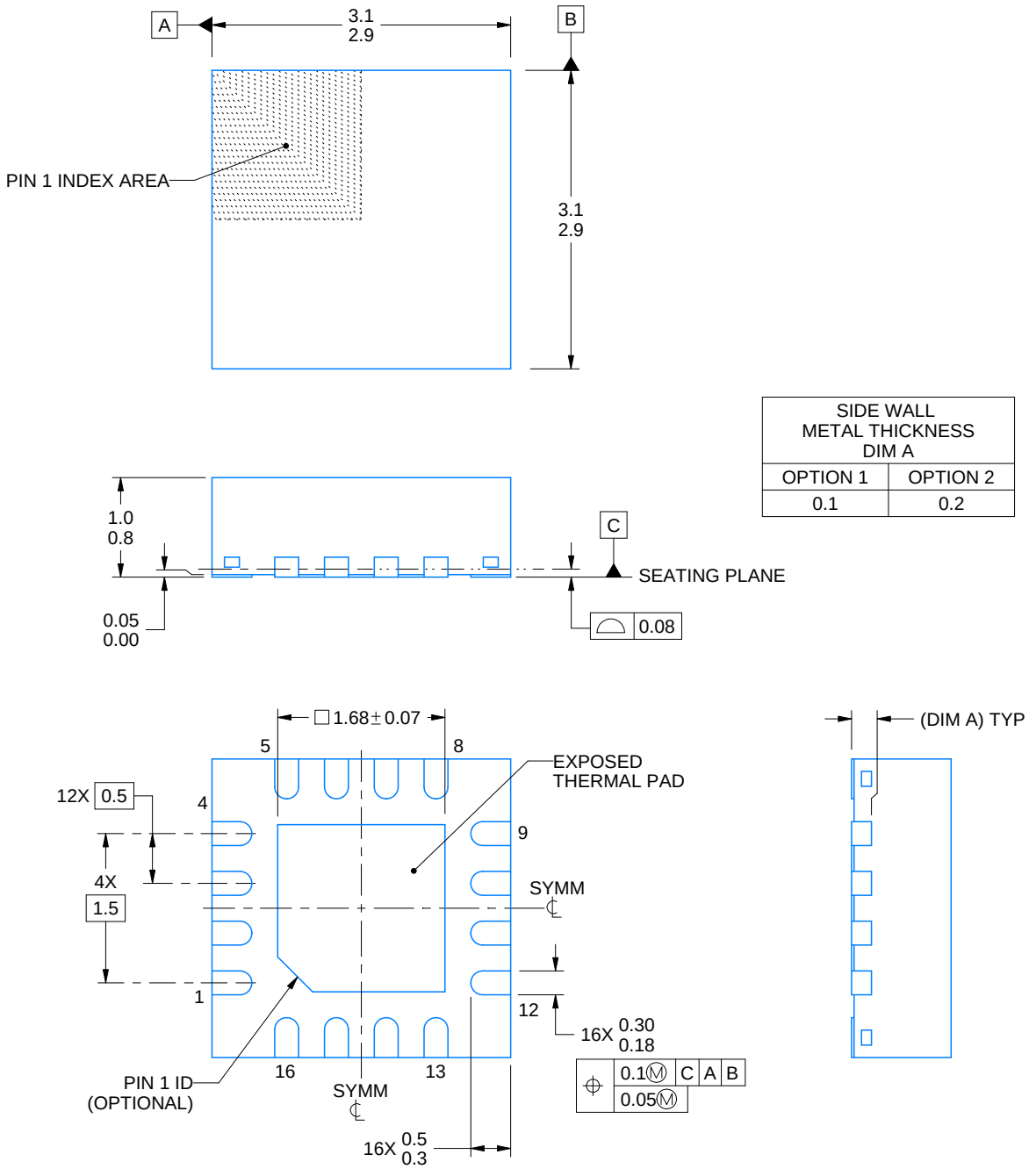
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RGT0016C

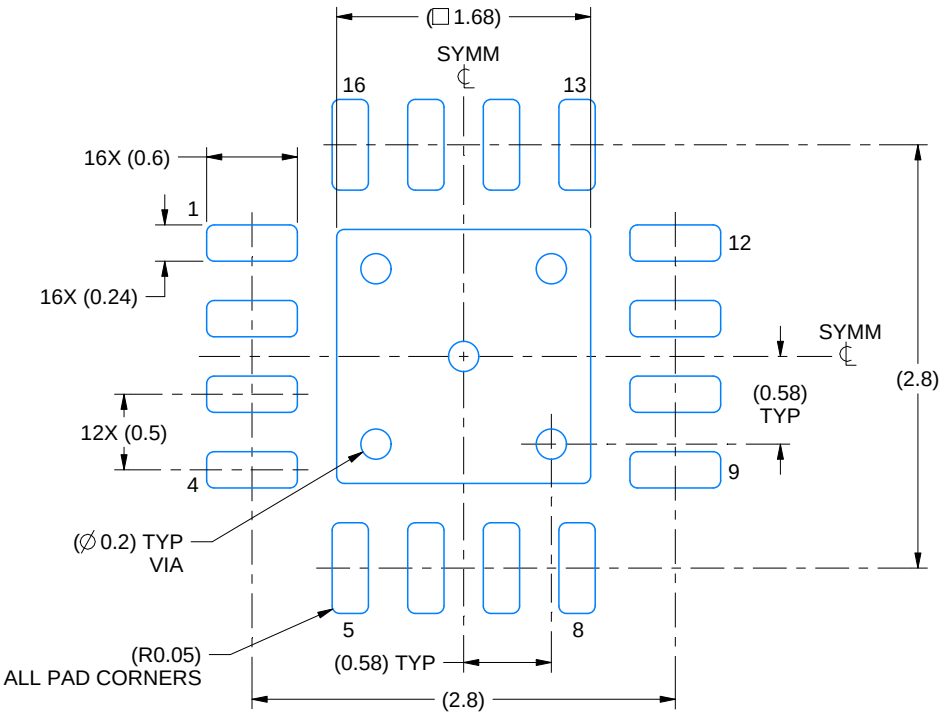
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

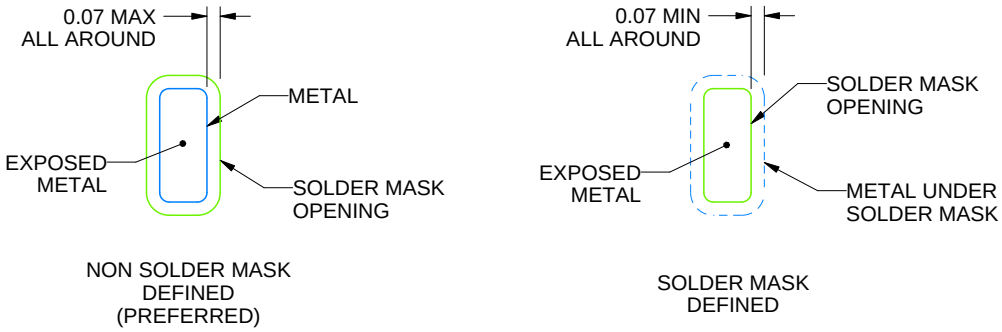


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

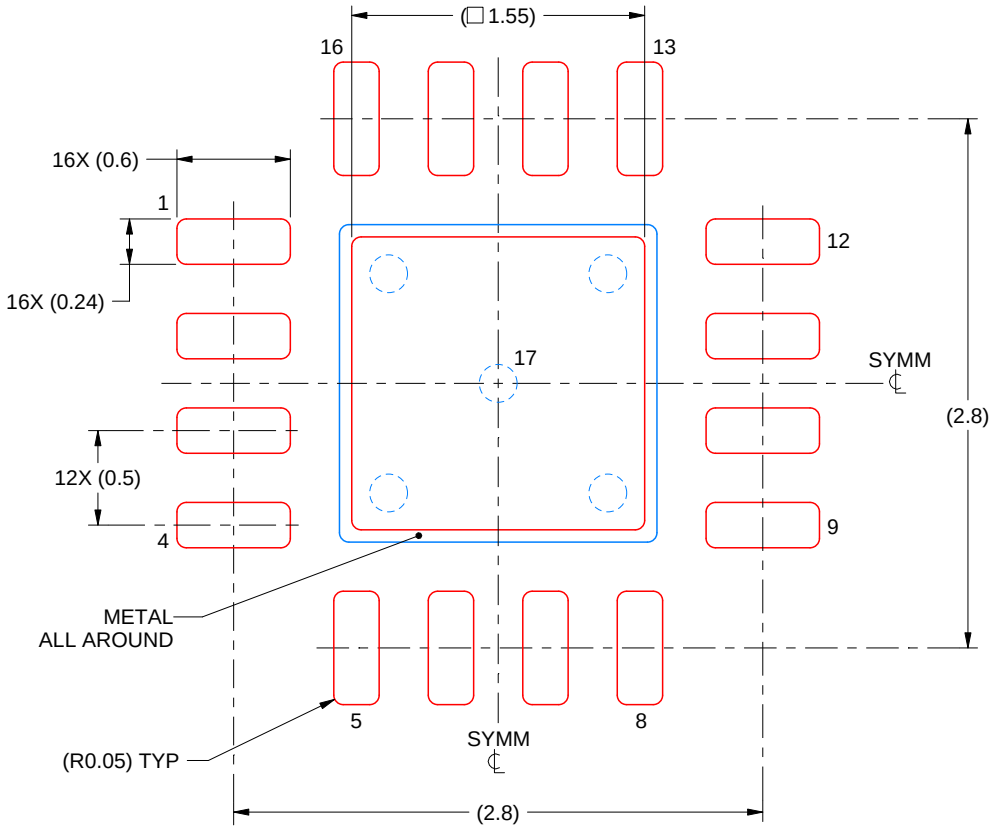


SOLDER MASK DETAILS

4222419/D 04/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4222419/D 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス· デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated