



TPS628301, TPS628302, TPS628303, TPS628304

JAJSL7A – FEBRUARY 2023 – REVISED OCTOBER 2023

TPS62830x、2.25V～5.5V 入力、1、2、3、4A、出力精度 1% の降圧コンバータ、小型 WQFN パッケージおよび SOT583 パッケージで供給

1 特長

- インダクタ内蔵パワー・モジュールとして供給
- 2.25V～5.5V の入力電圧範囲
- 0.5V～4.5V の可変出力電圧
- 1% の FB 電圧精度 ($-40^{\circ}\text{C} \sim 125^{\circ}\text{C T}_J$)
- 2.0MHz のスイッチング周波数
- 35mΩ および 18mΩ のパワー MOSFET を内蔵
- DCS-Control トポロジ
- EMI 性能の最適化
- CISPR 11/32 準拠が容易
 - オンチップのノイズ・フィルタリング・コンデンサを内蔵
 - CISPR に準拠した測定値を使用可能
- 優れた過度応答
- 導通モード選択用 MODE ピン
- 1.2V GPIO をサポート
- 100% デューティ・サイクル動作による最小のドロップアウト電圧
- アクティブ出力放電
- パワー・グッド出力
- サーマル・シャットダウン保護機能
- ヒカップまたはラッチオフ OCP/OVP
- PSpice と SIMPLIS のモデルを使用可能
- WEBENCH® Power Designer により、TPS62830x を使用するカスタム設計を作成

2 アプリケーション

- ソリッドステート・ドライブ (SSD)
- ポータブル・エレクトロニクス
- アナログ・セキュリティおよび IP ネットワーク・カメラ
- 産業用 PC
- ファクトリ・オートメーションおよび制御
- ASIC、SoC、MCU の電源
- 一般的なポイント・オブ・ロード (POL)

3 概要

TPS62830x は、静止電流が小さく、使いやすい同期整流降圧型 DC/DC コンバータ・ファミリです。TPS62830x は DCS-Control トポロジをベースとしており、出力静電容量が小さく、高速過渡応答を実現します。内部基準電圧により、最低 0.5V まで出力電圧をレギュレートでき、接合部温度が $-40^{\circ}\text{C} \sim 125^{\circ}\text{C}$ の範囲で 1% の高い帰還電圧精度を維持します。このファミリは 2 つのパッケージで供給され、各パッケージのデバイスはピン互換です。

TPS62830x には、デバイスの動作モードを制御する MODE ピンがあります。パワーセーブ・モードは、非常に軽い負荷まで高効率を維持し、システムのバッテリー動作時間を延ばします。出力電圧のリプルを最小限に抑え、スイッチング周波数をほぼ一定に保つよう、強制 PWM モードは連続導通モードを維持します。このデバイスは、パワー・グッド信号と、適切に制御された内部ソフトスタート回路を備えています。TPS62830x は 100% モードで動作可能です。フォルト保護の目的で、TPS62830x は HICCUP (ヒカップ、間欠型) 短絡保護機能やサーマル・シャットダウン機能を搭載しています。1 つのデバイス・オプションには、短絡および過電圧インシデントに対するラッチオフ保護機能があります。このファミリは 2 つのパッケージで供給されます。8 ピンの $1.0\text{mm} \times 2.0\text{mm}$ QFN パッケージは最高の電力密度設計を実現し、8 ピンの $1.6\text{mm} \times 2.1\text{mm}$ SOT583 パッケージは組み立てやすい設計を実現します。

パッケージ情報

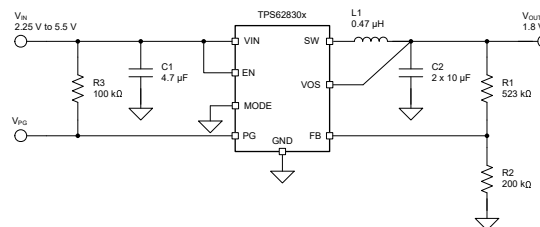
部品番号	パッケージ (1)	パッケージ・サイズ (2)
TPS62830x	RZE (WQFN, 8)	$1\text{mm} \times 2\text{mm}$
	DRL (SOT583, 8)	$2.1\text{mm} \times 1.6\text{mm}$

- 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
- パッケージ・サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます

製品情報

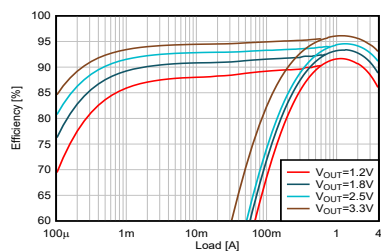
部品番号 (1)	出力電流	OCP モード
TPS62830xA	1A, 2A, 3A, 4A	ヒカップ
TPS62830xB	3A	OCP/OVP ラッチオフ

- 「デバイスのオプション」表を参照してください。



代表的なアプリケーション回路図





$V_{IN} = 5V$ での効率

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4 Revision History

Changes from Revision * (February 2023) to Revision A (October 2023)	Page
• ドキュメントのステータスを「事前情報」から「量産データ」に変更.....	1

5 Device Options

PART NUMBER	OUTPUT CURRENT	OCP MODE	PACKAGE	OUTPUT VOLTAGE
TPS628301ARZER	1 A	Hiccup	WQFN-HR	Adjustable ⁽²⁾
TPS628302ARZER	2 A			
TPS628303ARZER	3 A			
TPS628304ARZER	4 A			
TPS628301ADRLR	1 A		SOT583	
TPS628302ADRLR	2 A			
TPS628303ADRLR	3 A			
TPS628304ADRLR	4 A			
TPS628303BDRLR	3 A	OCP/OVP Latch-off ⁽¹⁾		

(1) For other output current versions with OCP/OVP Latch-off, please contact Marketing for availability.

(2) For fixed output voltage versions, please contact Marketing for availability.

6 Pin Configuration and Functions

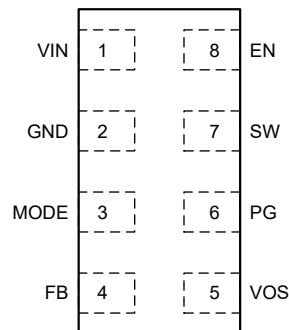


图 6-1. RZE Package 8-Pin WQFN Top View

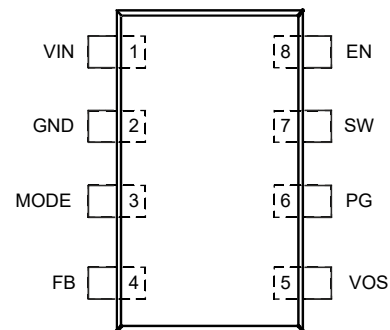


图 6-2. DRL Package 8-Pin SOT Top View

表 6-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
VIN	1	PWR	Input voltage pin. Connect the input capacitor as close as possible between V_{IN} and GND.
GND	2		Ground pin.
MODE	3	I	The device runs in PSM/PWM mode when this pin is pulled low and in forced-PWM mode when pulled high. This event can also be done when the device is in-operation. Do not leave this pin floating.
FB	4	I	Feedback pin. Connect the resistive output voltage divider to this pin.
VOS	5	I	Output voltage sense pin. This pin must be connected directly after the inductor.
PG	6	O	Power good open-drain output pin. The pullup resistor can be connected to voltages up to 5.5 V. If unused, leave this pin floating.
SW	7	PWR	Switch pin of the power stage
EN	8	I	Device enable pin. To enable the device, this pin must be pulled high. Pulling this pin low disables the device. Do not leave this pin unconnected.

(1) I = input, O = output, PWR = power

7 Specifications

7.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
Voltage ⁽²⁾	V _{IN} , EN, MODE, FB, PG	−0.3	6	V
Voltage ⁽²⁾	SW (DC)	−0.3	V _{IN} + 0.3	V
Voltage ⁽²⁾	SW (AC, < 10 ns) ⁽³⁾	−2.5	10	V
T _J	Operating junction temperature	−40	150	°C
T _{stg}	Storage temperature	−65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltage values are with respect to the network ground terminal.
- (3) While switching

7.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	± 2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	± 500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{IN}	Input voltage range	2.25		5.5	V
V _{OUT}	Output voltage range	0.5		4.5	V
C _{IN}	Effective input capacitance ⁽¹⁾	3			μF
L	Nominal output inductor	0.24	0.47	1.0	μH
C _{OUT}	Effective output capacitance ⁽¹⁾	12		200	μF
I _{OUT}	Output current range; TPS628301			1	A
I _{OUT}	Output current range; TPS628302			2	A
I _{OUT}	Output current range; TPS628303			3	A
I _{OUT}	Output current range; TPS628304 ⁽²⁾			4	A
I _{PG}	Power Good input current capability			1	mA
T _J	Operating junction temperature	−40		125	°C

- (1) The values given for all the capacitors in the table are effective capacitance, which includes the DC bias effect. Due to the DC bias effect of ceramic capacitors, the effective capacitance is lower than the nominal value when a voltage is applied. Please check the manufacturer's DC bias curves for the effective capacitance vs DC voltage applied.
- (2) Lifetime is reduced when operating continuously at I_{OUT} = 4 A and the junction temperature > 105°C.

7.4 Thermal Information Discrete

THERMAL METRIC ⁽¹⁾		TPS62830xRZE		TPS62830xDRL		UNIT
		8 pin-WQFN		8 pin-SOT583		
		JEDEC	EVM	JEDEC	EVM	
R _{θJA}	Junction-to-ambient thermal resistance	105.7	77.6	110.9	80	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	90.9	n/a ⁽²⁾	41.4	n/a ⁽²⁾	°C/W
R _{θJB}	Junction-to-board thermal resistance	30.7	n/a ⁽²⁾	22.2	n/a ⁽²⁾	°C/W
ψ _{JT}	Junction-to-top characterization parameter	2.7	2.8	0.8	1.3	°C/W

THERMAL METRIC ⁽¹⁾		TPS62830xRZE		TPS62830xDRL		UNIT
		8 pin-WQFN		8 pin-SOT583		
		JEDEC	EVM	JEDEC	EVM	
Ψ _{JB}	Junction-to-board characterization parameter	30.7	44.7	22.1	28.2	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) report.

(2) Not applicable to an EVM.

7.5 Electrical Characteristics

$T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{IN} = 2.25\text{ V}$ to 5.5 V . Typical values are at $T_J = 25^{\circ}\text{C}$ and $V_{IN} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Operating quiescent current	$EN = V_{IN}$, $I_{OUT} = 0\text{ mA}$, $V_{OUT} = 1.8\text{ V}$, MODE = GND, device not switching		7	17	μA
I_{SD}	V_{IN} shutdown supply current	$EN = \text{low}$, $T_J = -40^{\circ}\text{C}$ to 85°C		100	700	nA
$V_{UVLO(+)}$	Rising UVLO threshold voltage (V_{IN})		2.05	2.15	2.25	V
$V_{UVLO(hys)}$	UVLO hysteresis (V_{IN})		90	120		mV
THERMAL SHUTDOWN						
$T_{J(SD)}$	Thermal shutdown threshold	T_J rising		150		°C
$T_{J(HYS)}$	Thermal shutdown hysteresis			20		°C
LOGIC PINS						
$V_{EN(+)}$	High-level input voltage (EN)		0.8			V
$V_{EN(-)}$	Low-level input voltage (EN)				0.35	V
$V_{MODE(+)}$	High-level input voltage (MODE)		0.8			V
$V_{MODE(-)}$	Low-level input voltage (MODE)				0.35	V
$I_{EN(LKG)}$	EN Input leakage current	$V_{EN} = \text{HIGH}$		10	100	nA
$I_{MODE(LKG)}$	MODE Input leakage current	$V_{MODE} = \text{HIGH}$		10	100	nA
STARTUP						
t_{SS}	Internal fixed soft-start time	From $V_{OUT} = 0$ to $V_{OUT} = 95\%$	180	300	440	μs
$t_{d(EN)}$	Enable delay time	From EN HIGH to device starts switching		120	220	μs
REFERENCE VOLTAGE						
V_{FB}	Feedback voltage accuracy	PWM mode	495	500	505	mV
V_{FB}	Feedback voltage accuracy	PWM mode	-1		+1	%
V_{FB}	Feedback voltage accuracy	PFM mode, $C_{OUT,eff} \geq 15\text{ }\mu\text{F}$, $L = 0.47\text{ }\mu\text{H}$	-1		+2	%
$I_{FB(LKG)}$	FB input leakage current, adjustable version	$V_{FB} = 0.5\text{ V}$		10	70	nA
$I_{VOS(LKG)}$	VOS input leakage current	$V_{EN} = \text{low}$		100	500	nA
POWER GOOD						
$V_{PG,UV(+)}$	Rising power good threshold voltage (output undervoltage)	Power Good low, V_{FB} rising	94	96	98	%
$V_{PG,UV(-)}$	Falling power good threshold voltage (output undervoltage)	Power Good high, V_{FB} falling	90	92	94	%
$V_{PG,OV(+)}$	Rising power good threshold voltage (output overvoltage)	Power Good high, V_{FB} rising	108	110	112	%
$V_{PG,OV(-)}$	Falling power good threshold voltage (output overvoltage)	Power Good low, V_{FB} falling	102.5	105	107	%
$t_{d(PG)}$	Power good delay at start up	Low-to-high transition on the PG pin at start up		128		μs
$t_{d(PG)}$	Power good deglitch delay during operation	High-to-low or low-to-high transition on the PG pin	30	45	60	μs
$I_{PG(LKG)}$	PG pin Leakage current when open drain output is high	$V_{PG} = 5.0\text{ V}$		10	100	nA
$V_{PG,OL}$	PG pin low-level output voltage	$I_{PG} = 1\text{ mA}$			0.4	V
POWER STAGE						
$R_{DS(on)(HS)}$	High-side MOSFET on-resistance	$V_{IN} \geq 5\text{ V}$		35	57	m Ω

7.5 Electrical Characteristics (続き)

$T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{IN} = 2.25\text{ V}$ to 5.5 V . Typical values are at $T_J = 25^{\circ}\text{C}$ and $V_{IN} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{DS(on)}$	Low-side MOSFET on-resistance		18	29	mΩ
f_{SW}	Switching frequency, PWM mode		2.0		MHz
OVERCURRENT PROTECTION					
$I_{HS(OC)}$	High-side peak current limit	TPS628301	1.8	2.1	2.6
$I_{HS(OC)}$	High-side peak current limit	TPS628302	2.7	3.3	3.9
$I_{HS(OC)}$	High-side peak current limit	TPS628303	4.0	4.6	5.4
$I_{HS(OC)}$	High-side peak current limit	TPS628304	5.0	5.9	7.0
$I_{LS(NOC)}$	Low-side negative current limit	Sinking current limit on LS FET	-1.8		A
OUTPUT DISCHARGE					
I_{DIS}	Output discharge current on SW pin	$V_{IN} > 2\text{ V}$, $V_{SW} = 0.4\text{ V}$, $EN = \text{LOW}$	75	400	mA
OUTPUT OVP					
V_{OVP}	Overvoltage-protection (OVP) threshold voltage	V_{FB} rising; devices with OVP feature only	108	110	112
$t_d(\text{OVP})$	OVP delay	Devices with OVP feature only	35		μs

7.6 Typical Characteristics

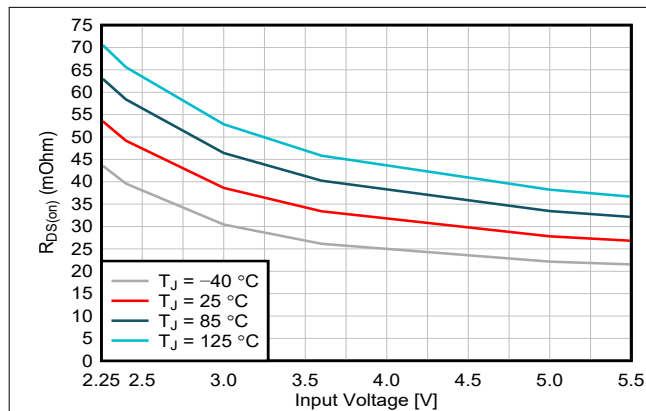


図 7-1. High-Side FET On-Resistance

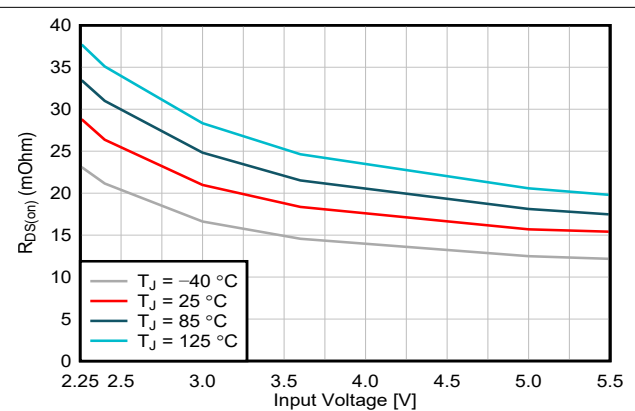


図 7-2. Low-Side FET On-Resistance

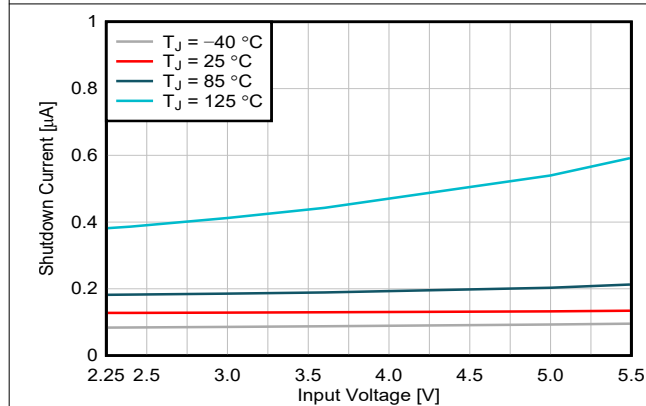


図 7-3. Shutdown Current

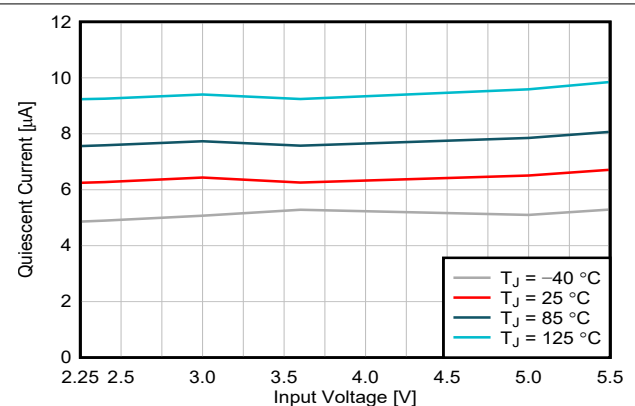


図 7-4. Quiescent Current

8 Detailed Description

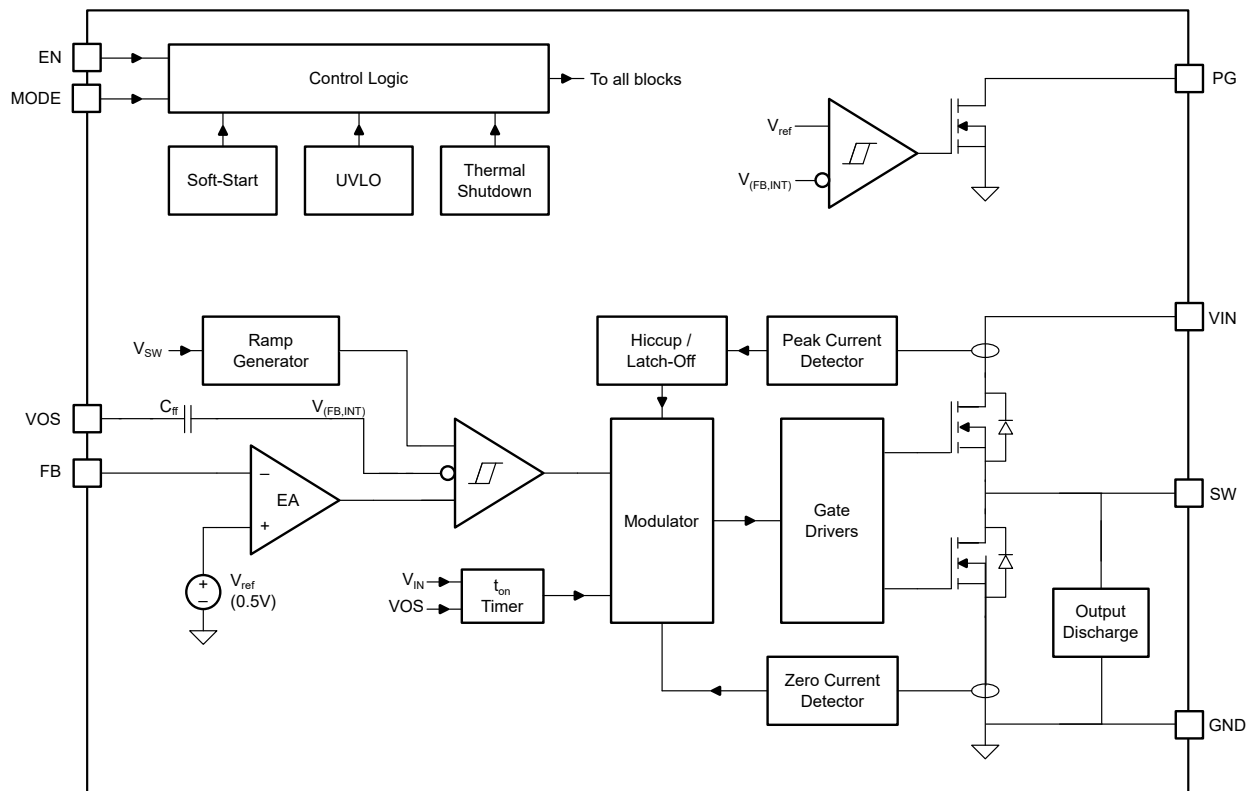
8.1 Overview

The TPS62830x is a family of low-voltage step-down converters available in 1-, 2-, 3- and 4-A versions. These devices use a DCS-Control scheme which transitions seamlessly from pulse-width modulation (PWM) at medium and high output currents to pulsed-frequency modulation (PFM) at low output currents. During PWM operation, the devices switch at 2 MHz; during PFM operation, the switching frequency varies with the load current and reduces as the load current decreases. For applications that require the lowest possible output voltage ripple and/or a constant switching frequency, a high logic level on the MODE pin forces the devices to use PWM under all load conditions (at the expense of lower efficiency at low output currents). An external resistor-divider sets the output voltage anywhere from 0.5 V to 4.5 V and the nominal switching frequency is 2 MHz with a controlled variation over the input voltage range.

Device variants are available that support both hiccup and latch-off protection behavior.

The TPS62830x devices offer two significant advantages compared to previous devices in this series: Transient performance is much better, due to the quick reaction of a fast comparator in both PFM and PWM modes, and EMI is much lower, thanks to an on-chip decoupling capacitor and an optimized gate driver.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Pulse Width Modulation (PWM) Operation

If the MODE pin is LOW and at load currents larger than half the inductor ripple current, the device operates in pulse width modulation in continuous conduction mode (CCM) as shown in [Figure 8-1](#). The PWM operation is based on an adaptive constant on-time control with stabilized switching frequency. To achieve a stable switching frequency in a steady state condition, the on-time is calculated as:

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \times 500ns \quad (1)$$

If the MODE pin is HIGH, the converter maintains a forced-PWM operation for all load currents.

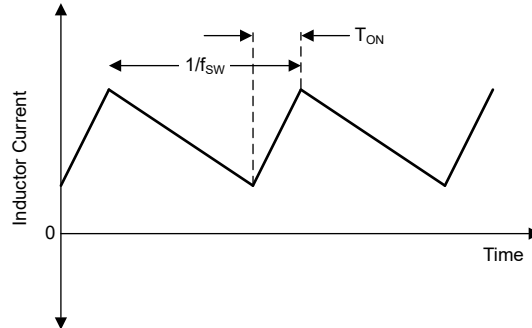


図 8-1. Continuous Conduction Mode (PWM-CCM) Current Waveform

8.3.2 Power Save Mode (PSM) Operation

To maintain high efficiency at light loads, the device enters power save mode (PSM) at the boundary to discontinuous conduction mode (DCM). This event happens when the output current becomes smaller than half of the ripple current of the inductor. The device operates with a fixed on-time, and the switching frequency decreases proportional to the load current as shown in 図 8-2. It can be calculated as:

$$f_{PSM} = \frac{2 \times I_{OUT}}{T_{ON}^2 \times \frac{V_{IN}}{V_{OUT}} \left[\frac{V_{IN} - V_{OUT}}{L} \right]} \quad (2)$$

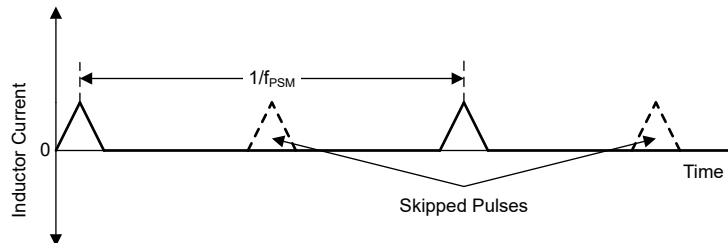


図 8-2. Discontinuous Conduction Mode (PSM-DCM) Current Waveform

In PSM, the output voltage rises slightly above the nominal target, which can be minimized using larger output capacitance. At duty cycles larger than 90%, the device does not enter PSM and maintains output regulation in PWM mode.

8.3.3 Start-Up and Soft Start

When the EN voltage goes High, the device starts loading the default values into the device registers. This action typically is done within 120 μs. After that, the internal soft-start circuitry controls the output voltage during start-up. This control avoids excessive inrush current and makes sure of a controlled output voltage ramp. This control also prevents unwanted voltage drops from high-impedance power sources or batteries. Finally, the PG signal has a delay up to 180 μs at start-up. 図 8-3 shows a start-up sequence, where the EN pin is pulled up to VIN.

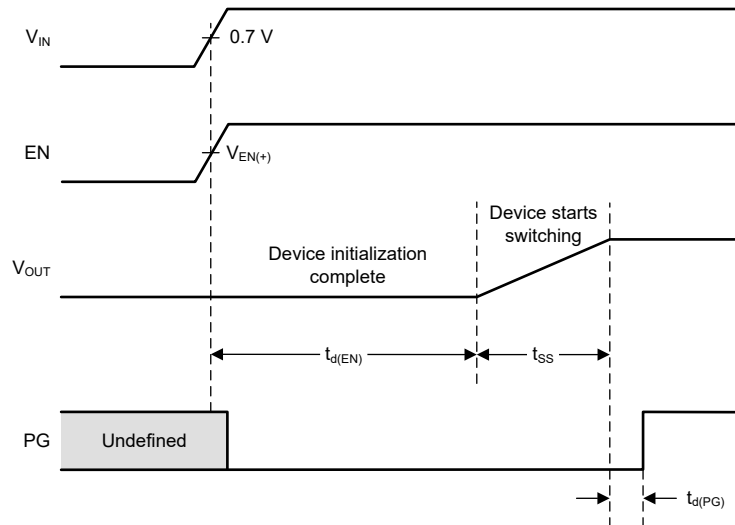


図 8-3. Start-Up Timing When EN is Pulled Up to VIN

図 8-4 shows a start-up sequence, where an external signal is connected to the EN pin.

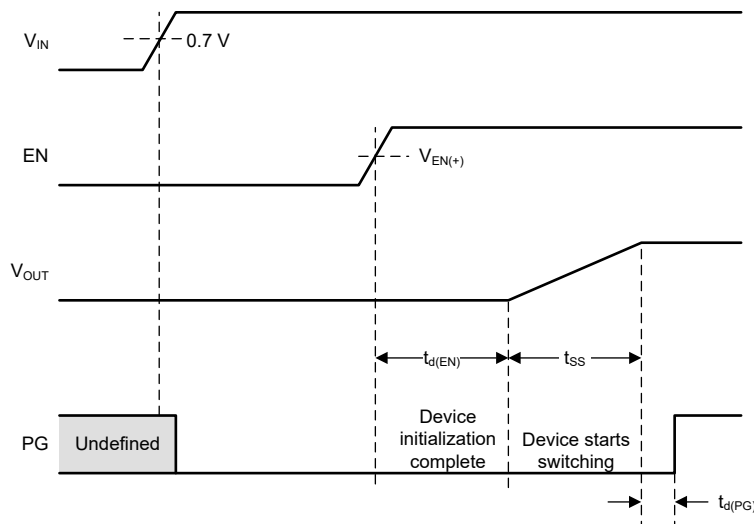


図 8-4. Start-Up Timing When an External Signal is Connected to the EN Pin

The TPS62830x can start into a prebiased output if enabled for the first time. For a new prebiased operation, a power cycle is needed to disable the active output discharge. 図 8-5 shows a start-up into a prebiased output voltage.

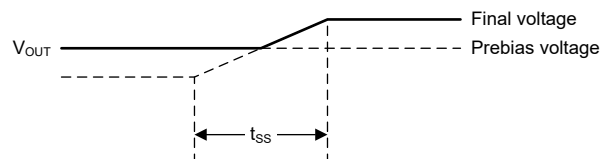


図 8-5. Start-Up into a Prebiased Output

8.3.4 Switch Cycle-by-Cycle Current Limit

All the devices in the family have a cycle-by-cycle current limit function. When the device detects that the current in the high-side FET exceeds the high-side current limit, either due to a heavy load or a short circuit condition, it immediately turns off the high-side FET and turns on the low-side FET. The high-side FET turns on again at the start of the next switching cycle. Note that because of the propagation delay in the current limit comparator (typically 60ns), the current flowing in the high-side FET when the device detects a current limit condition may be slightly higher than the current limit specified in the device's Electrical Characteristics.)

Devices with an 'A' suffix in their part number respond to repeated current limit events with hiccup behavior (see [セクション 5](#)).

Devices with an 'B' suffix in their part number respond to repeated current limit events with latch-up behavior (see [セクション 5](#)).

8.3.5 Short-Circuit Protection

In devices with hiccup protection, when a current limit event occurs for 32 consecutive switching cycles (about 16 μ s), the device turns off the high-side FET for about 9.6 ms, during which time the inductor current decays through the low-side FET's body diode. After 9.6 ms has expired, the device automatically starts switching again, beginning with a soft-start condition. The device alternates between bursts of switching cycles and 9.6-ms pauses for as long as the overload condition on the output exists.

In devices with latch-off protection, When a current limit event occurs for 32 consecutive switching cycles (about 16 μ s), the device stops switching and latches off the high-side and low-side FETs. To recover normal operation after a latched short-circuit event, you must cycle V_{IN} or EN.

In devices with latch-off protection, there is also an OVP protection circuit that uses the PG window comparator. An OVP event is detected when the FB voltage is approximately $110\% \times (0.5V)$ for a period longer than the deglitch time of 35 μ s. In this case, the converter de-asserts the PG signal and performs the overvoltage protection function. The converter latches off both high-side and low-side FET and remains in this state. To recover normal operation after a latched short-circuit event, you must cycle V_{IN} or EN.

8.3.6 Undervoltage Lockout

The undervoltage lockout (UVLO) function prevents misoperation of the device if the input voltage drops below the UVLO threshold.

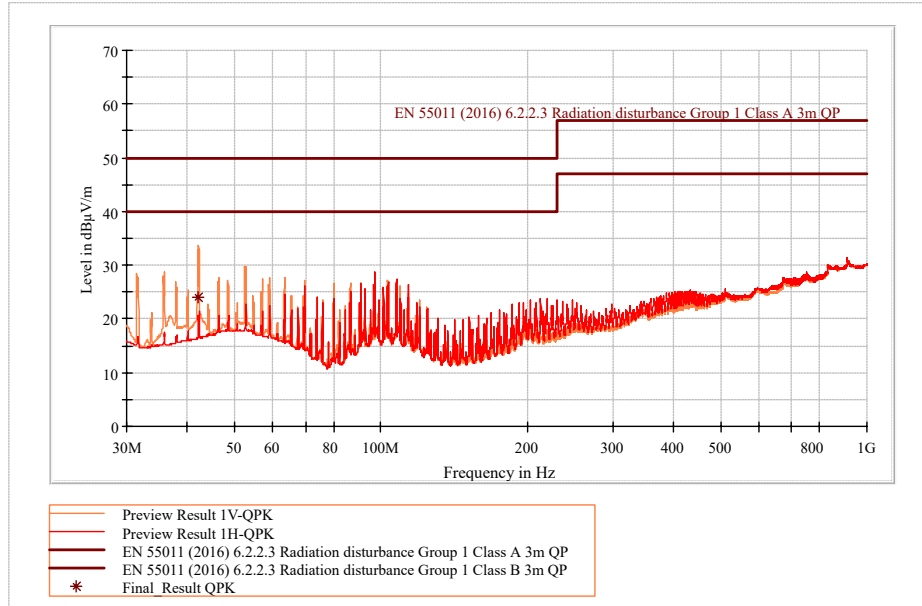
8.3.7 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds 150°C (typical), the device goes in thermal shutdown with a hysteresis of typically 20°C. After T_J has decreased enough, the device resumes normal operation.

8.3.8 Optimized EMI Performance

TPS62830x devices incorporate advanced techniques to minimize Electromagnetic Interference (EMI) and makes complying with stringent EMI standards simple. By integrating capacitors directly onto the silicon, parasitic elements are reduced and loop area is minimized, effectively reducing high-frequency noise emissions primarily above 450 MHz. The on-chip capacitors make sure low-inductance paths for high-frequency AC switching current and damping voltage ringing.

Additionally to the on-chip capacitors, the gate driver has been improved with advanced slew rate control mechanisms and by smoothing the supply voltage. The switch node voltage is controlled in a way to reduce sharp edges and minimize voltage overshoot, consequently diminishing EMI.



The above plot is measured on the EVM with the TPS628304ARZER and standard BOM. There is no notable difference on EMI performance between available packages.

$I_{OUT} = 4\text{ A}$

$V_{IN} = 5.5\text{ V}$

$V_{OUT} = 1.8\text{ V}$

8-6. Radiated EMI Performance (CISPR11 Radiated Emission Test with Class A and Class B Limits)

8.4 Device Functional Modes

8.4.1 Enable, Disable, and Output Discharge

The device starts operation when Enable (EN) is set High. The input threshold levels are typically 0.8 V for rising and 0.35 V for falling signals. Do not leave EN floating. Shutdown is forced if EN is pulled Low with a shutdown current of typically 100 nA. During shutdown, the internal power MOSFETs as well as the entire control circuitry are turned off and the output voltage is actively discharged through the SW pin by a current sink. Therefore V_{IN} must remain present for the discharge to function.

8.4.2 Minimum Duty Cycle and 100% Mode Operation

There is no limitation for small duty cycles because, even at very low duty cycles, the switching frequency is reduced as needed to always make sure of a proper regulation.

If the output voltage (V_{OUT}) comes close to the input voltage (V_{IN}), the device enters 100% mode. While the high-side switch is constantly turned on, the low-side switch is switched off. This action is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The difference between V_{IN} and V_{OUT} is determined by the voltage drop across the high-side FET and the DC resistance of the inductor. The minimum V_{IN} that is needed to maintain a specific V_{OUT} value is estimated as:

$$V_{IN,min} = V_{OUT} + I_{OUT,MAX} \times (R_{DS(on)} + R_L) \quad (3)$$

where

- $V_{IN,min}$ = Minimum input voltage to maintain an output voltage
- $I_{OUT,MAX}$ = Maximum output current
- $R_{DS(on)}$ = High-side FET ON-resistance
- R_L = Inductor ohmic resistance (DCR)

8.4.3 Power Good

The TPS62830x has a built-in power-good (PG) function. The PG pin goes high impedance when the output voltage has reached its nominal value. Otherwise, including when disabled, in UVLO or in thermal shutdown, PG is Low (see 表 8-1). The PG function is formed with a window comparator, which has an upper and lower voltage threshold. The PG pin is an open-drain output and is specified to sink up to 1 mA. The power-good output requires a pullup resistor connecting to any voltage rail less than 5.5 V.

表 8-1. PG Pin Logic

DEVICE CONDITIONS		LOGIC STATUS	
		HIGH Z	LOW
Enable	EN = High, $V_{FB} \geq 0.48$ V	√	
	EN = High, $V_{FB} \leq 0.56$ V		√
	EN = High, $V_{FB} \leq 0.525$ V	√	
	EN = High, $V_{FB} \geq 0.55$ V		√
Shutdown	EN = Low		√
Thermal shutdown	$T_J > T_{JSD}$		√
UVLO	$0.7 \text{ V} < V_{IN} < V_{UVLO}$		√
Power supply removal	$V_{IN} < 0.7$ V	√	

The PG signal can be used for sequencing of multiple rails by connecting it to the EN pin of other converters. Leave the PG pin unconnected when not used. The PG rising edge and falling edge has a 40-μs blanking time, as shown in 図 8-7. At start-up the delay of PG signal is typically 125-μs after softstart is finished.

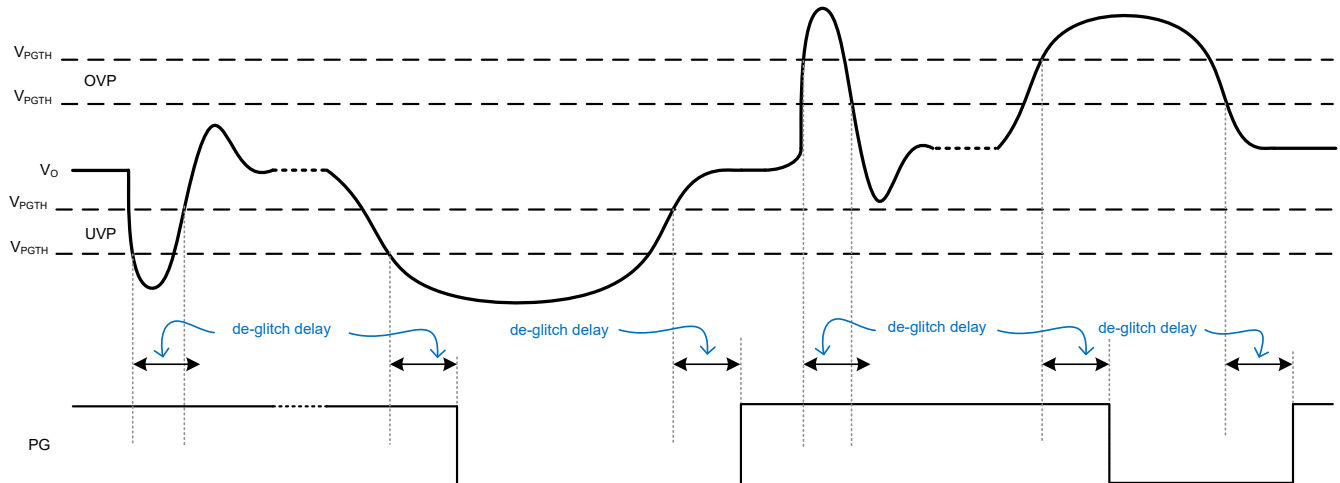


図 8-7. Power-Good Behavior

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

9.2 Typical Application

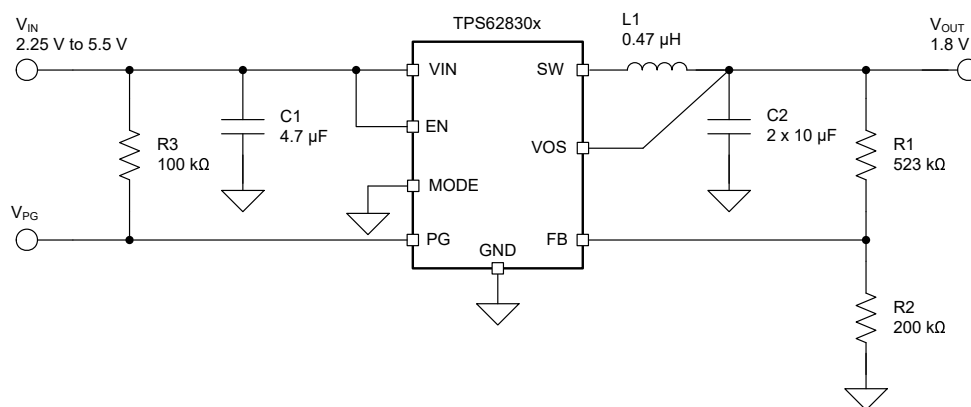


図 9-1. Typical Application of TPS62830x (Optimized for Design Size)

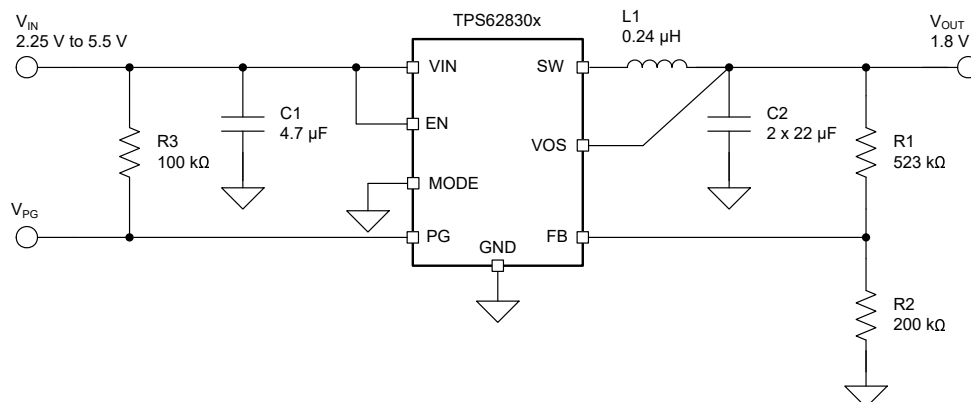


図 9-2. Typical Application of TPS62830x (Optimized for Transient Response)

9.2.1 Design Requirements

For this design example, use the parameters listed in 表 9-1 as the input parameters.

表 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	2.25 V to 5.5 V
Output voltage	1.8 V
Output ripple voltage	< 15 mV

表 9-2 lists the components used for the example.

表 9-2. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
C1	4.7 μF, Ceramic capacitor, 6.3 V, X7R, size 0603, JMK107BB7475KA-T	Taiyo Yuden
C2	2 × 10 μF, Ceramic capacitor, 10 V, X7R, size 0603, GRM188Z71A106KA73D	Murata
L1	0.47 μH, Power inductor, XGL4015-471ME	Coilcraft
R1	Depending on the output voltage, 1%, size 0402	Std
R2	200 kΩ, Chip resistor, 1/16 W, 1%, size 0402	Std
R3	100 kΩ, Chip resistor, 1/16 W, 1%, size 0402	Std

9.2.2 Detailed Design Procedure

9.2.2.1 Custom Design With WEBENCH® Tools

[Click here](#) to create a custom design using the TPS62830x device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.2.2 Setting The Output Voltage

The output voltage is set by an external resistor divider according to 式 4:

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) = R2 \times \left(\frac{V_{OUT}}{0.5V} - 1 \right) \quad (4)$$

R2 can be any value between 200 kΩ and 600 kΩ to achieve high efficiency at light load while providing acceptable noise sensitivity.

9.2.2.3 Inductor Selection

The main parameter for the inductor selection is the inductor value and then the saturation current of the inductor. To calculate the maximum inductor current under static load conditions, 式 5 and 式 6 are given.

$$I_{L,MAX} = I_{OUT,MAX} + \frac{\Delta I_L}{2} \quad (5)$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}} \quad (6)$$

where:

- $I_{OUT,MAX}$ = Maximum output current
- ΔI_L = Inductor current ripple
- f_{SW} = Switching frequency
- L = Inductor value

TI recommends to choose a saturation current for the inductor that is approximately 20% to 30% higher than $I_{L,MAX}$. In addition, DC resistance and size must also be taken into account when selecting an appropriate inductor. Finally, for better transient response performance, TI recommends a smaller inductance value. 表 9-3 lists recommended inductors.

表 9-3. List of Recommended Inductors

INDUCTANCE [μ H]	CURRENT RATING [A]	DIMENSIONS [mm]	MAX. DC RESISTANCE [m Ω]	MFR PART NUMBER ⁽¹⁾
0.47	4.4	4.0 × 4.0 × 1.6	7.5	XGL4015-471ME, Coilcraft
	4.8	2.0 × 1.6 × 1.0	22	HTEN20161T-R47MDR, Cyntec
	4.8	2.0 × 1.6 × 1.0	22	CIGT201610EHR47MNE, Samsung
	5.1	2.0 × 1.6 × 1.0	34	TFM201610ALM-R47MTAA, TDK
0.24	4.8	2.0 × 1.25 × 0.8	17	LSCNE2012HKTR24MD, Taiyo Yuden
	4.7	2.0 × 1.6 × 1.0	19	CIGT201610LHR24MNE, Samsung
	4.7	2.0 × 1.6 × 1.0	20	DFE201610E-R24M, MuRata
	3.6	2.0 × 1.6 × 0.8	23	CIGT201608LMR24MNE, Samsung

(1) See the [Third-party Products Disclaimer](#).

9.2.2.4 Output Capacitor Selection

The inductor and the output capacitor together provide a low-pass filter. To simplify this process, 表 9-5 outlines possible inductor and capacitor value combinations for most applications. Cells with the (✓) mark represent combinations that are proven for stability by simulation and lab test. additionally, cells with the (+) mark represent combinations that are proven for stability by simulation only. Check further combinations for each individual application.

The DCS-Control scheme of the TPS62830x allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. To keep low resistance up to high frequencies and to get narrow capacitance variation with temperature, TI recommends using X7R or X5R dielectrics. At light load currents, the converter operates in Power Save Mode and the output voltage ripple is dependent on the output capacitor value. A larger output capacitors can be used reducing the output voltage ripple. Considering the DC-bias derating the capacitance, the recommended minimum effective output capacitance is 12 μ F when using a 0.47- μ H or larger inductor. When using a 0.24- μ H or lower inductor, the recommended minimum effective output capacitance is 22 μ F. 表 9-6 lists recommended capacitors.

表 9-4. Matrix of Output Capacitor and Inductor Combinations (TPS628301 and TPS628302)

V_{OUT} [V]	NOMINAL L [μ H] ⁽²⁾	NOMINAL C_{OUT} [μ F] ⁽³⁾		
		2 × 10 or 22	2 × 22 or 47	100
$0.5 \leq V_{OUT} \leq 1.8$	0.47	✓ ⁽¹⁾	✓	+
	1.0	+	+	
$1.8 < V_{OUT}$	0.47		✓ ⁽¹⁾	+
	1.0	+	+	

表 9-5. Matrix of Output Capacitor and Inductor Combinations (TPS628303 and TPS628304)

V_{OUT} [V]	NOMINAL L [μ H] ⁽²⁾	NOMINAL C_{OUT} [μ F] ⁽³⁾		
		2 × 10 or 22	2 × 22 or 47	100
$0.5 \leq V_{OUT} \leq 1.8$	0.47	✓ ⁽¹⁾	✓	+
	0.24	+	✓	+
$1.8 < V_{OUT}$	0.47		✓ ⁽¹⁾	+
	0.24		✓	+

(1) This LC combination is the standard value and recommended for most applications.

(2) Inductor tolerance and current derating is anticipated. The effective inductance can vary by 20% and –30%.

- (3) Capacitance tolerance and bias voltage derating is anticipated. The effective capacitance can vary by 20% and –50%.

表 9-6. List of Recommended Capacitors

NOMINAL CAPACITANCE [μF]	VOLTAGE RATING [V]	DIMENSIONS [mm]	MFR PART NUMBER ⁽¹⁾
10	6.3	2.0 × 1.5 × 1.25	MSASJ21GAB7106MTNA01, Taiyo Yuden
10	10	2.0 × 1.25 × 1.25	C2012X7R1A106K125AC, TDK
10	10	1.6 × 0.8 × 0.8	GRM188Z71A106KA73#, MuRata
10	10	1.6 × 0.8 × 0.8	C1608X5R1A106K080AC, TDK
22	10	2.0 × 1.25 × 1.25	GRM21BZ71A226ME15#, MuRata
22	10	1.6 × 0.8 × 0.8	C1608X5R1A226M080AC, TDK

9.2.2.5 Input Capacitor Selection

The input capacitor is the low-impedance energy source for the converter, which helps provide stable operation. Because the buck converter has a pulsating input current, a low ESR ceramic input capacitor is required for best input voltage filtering to minimize input voltage spikes. Place the capacitor between VIN and GND pins and as close as possible to those pins.

For most applications, a minimum effective input capacitance of 3 μF is sufficient, though a larger value reduces input current ripple and is recommended. When operating from a high impedance source, a larger input buffer capacitor ≥10 μF is recommended to avoid voltage drops during start-up and load transients. Additionally, small de-coupling capacitors can also be used in case of noise at the input if the device. The input capacitor can be increased without any limit for better input voltage filtering.

表 9-7 shows a list of recommended capacitors.

表 9-7. List of Recommended Capacitors

NOMINAL CAPACITANCE [μF]	VOLTAGE RATING [V]	DIMENSIONS [mm]	MFR PART NUMBER ⁽¹⁾
4.7	6.3	1.6 × 0.8 × 0.8	MSASJ168BB7475MTNA01, Taiyo Yuden
4.7	10	2.0 × 1.25 × 1.25	C2012X7R1A475K125AC, TDK
10	10	1.6 × 0.8 × 0.8	GRM188Z71A106KA73#, MuRata

- (1) See the [Third-party Products Disclaimer](#)

9.2.3 Application Curves

$T_A = 25^\circ\text{C}$, $V_{IN} = 5\text{ V}$, $V_{OUT} = 1.8\text{ V}$, BOM = 表 9-2 unless otherwise noted.

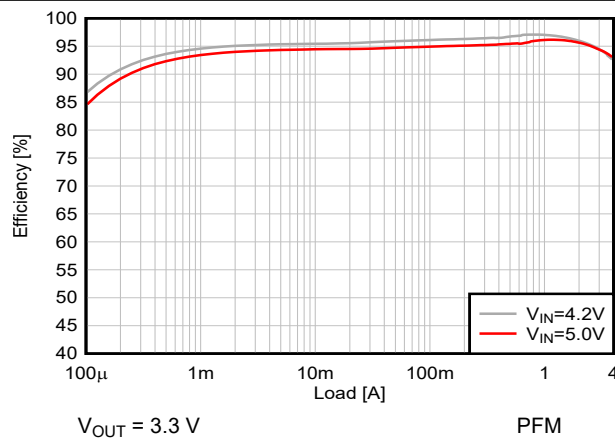


図 9-3. Efficiency versus Output Current

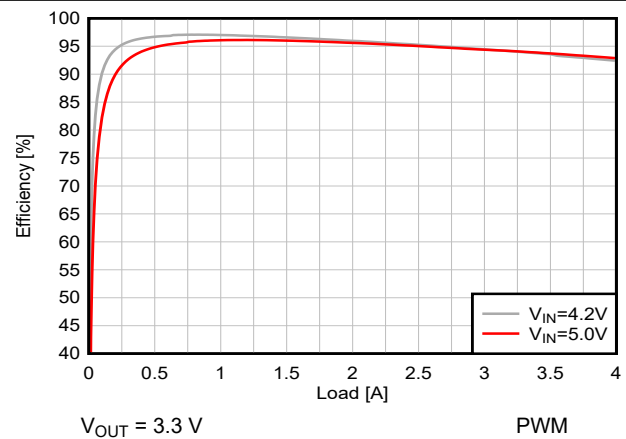


図 9-4. Efficiency versus Output Current

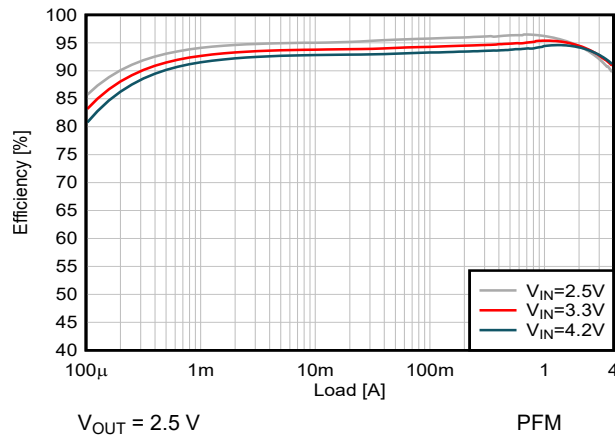


図 9-5. Efficiency versus Output Current

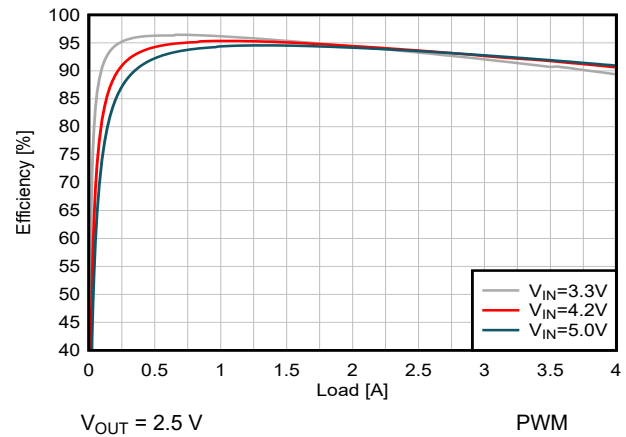


図 9-6. Efficiency versus Output Current

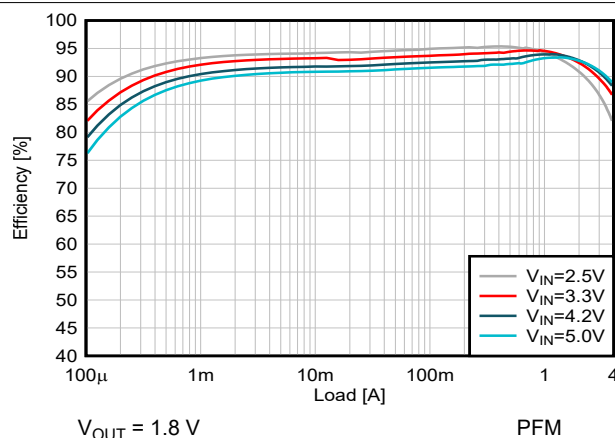


図 9-7. Efficiency versus Output Current

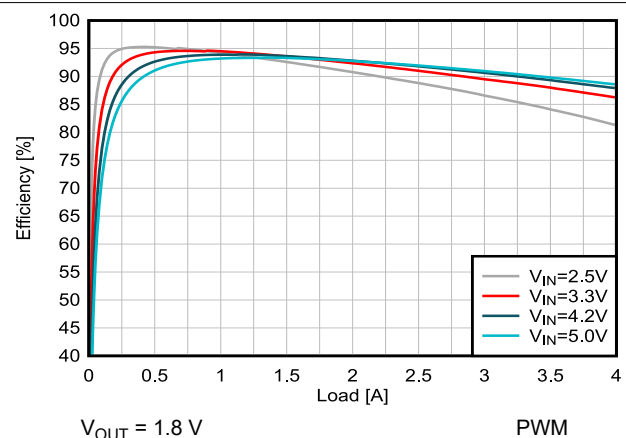


図 9-8. Efficiency versus Output Current

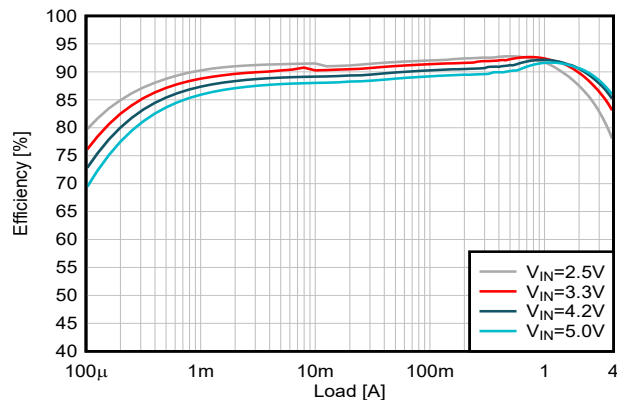


図 9-9. Efficiency versus Output Current

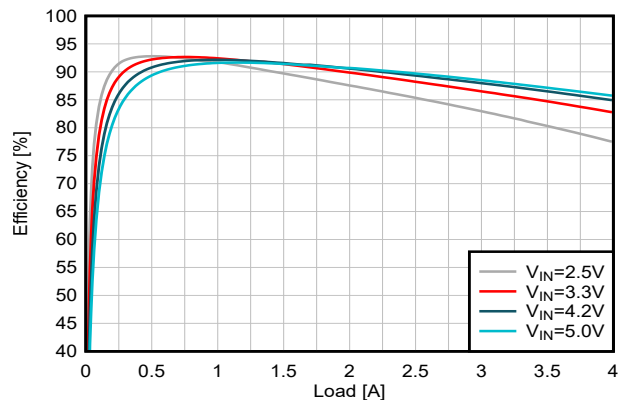


図 9-10. Efficiency versus Output Current

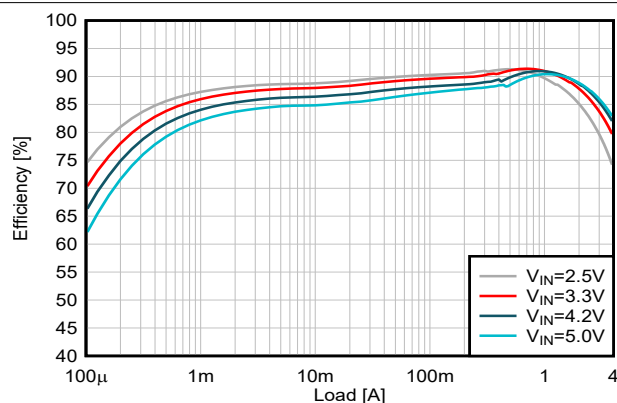


図 9-11. Efficiency versus Output Current

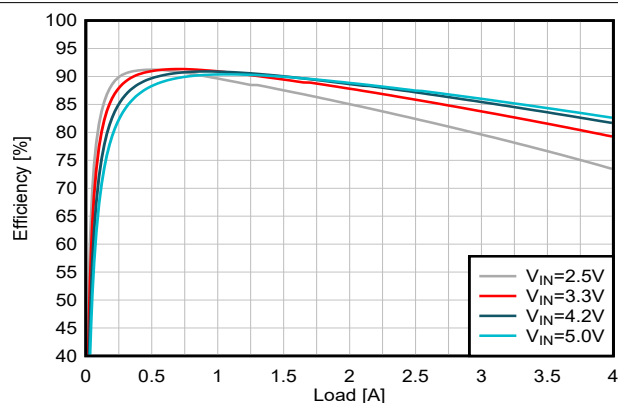


図 9-12. Efficiency versus Output Current

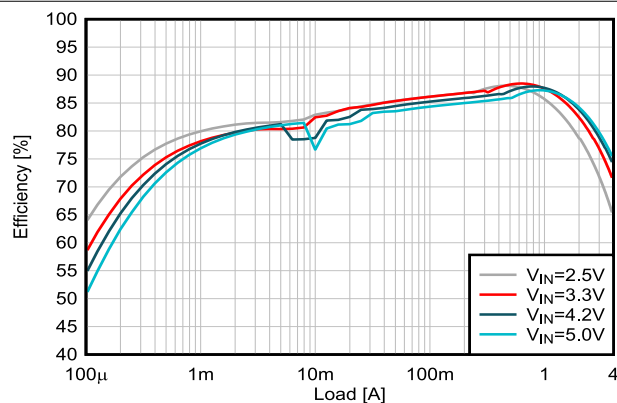


図 9-13. Efficiency versus Output Current

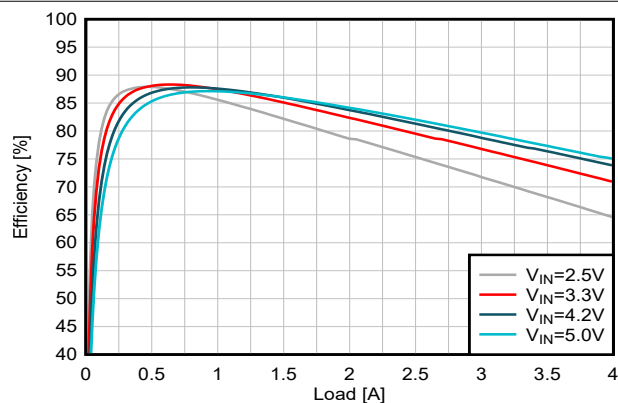
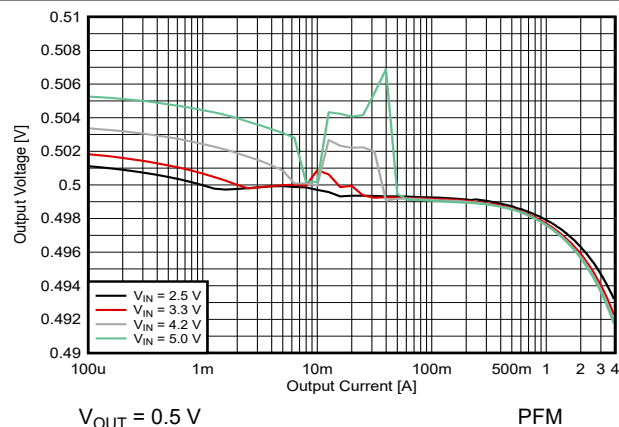
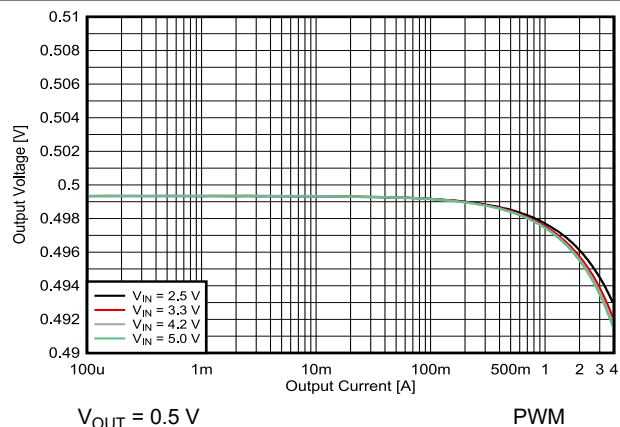


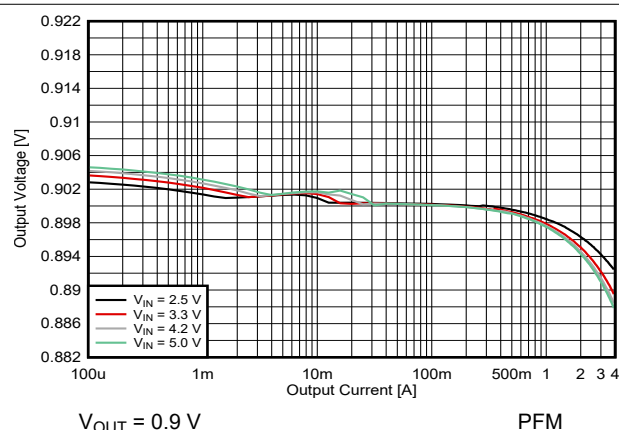
図 9-14. Efficiency versus Output Current



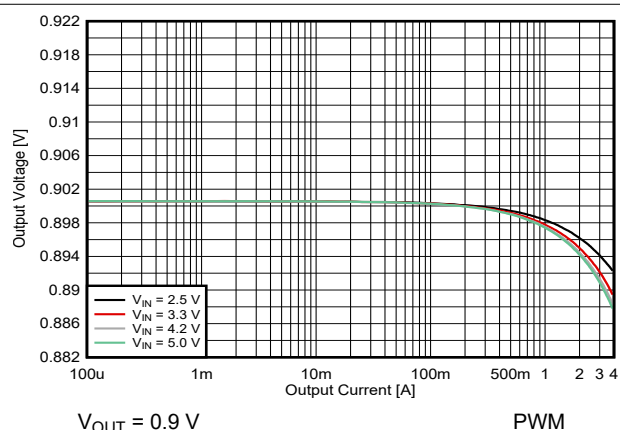
9-15. Output Voltage versus Output Current



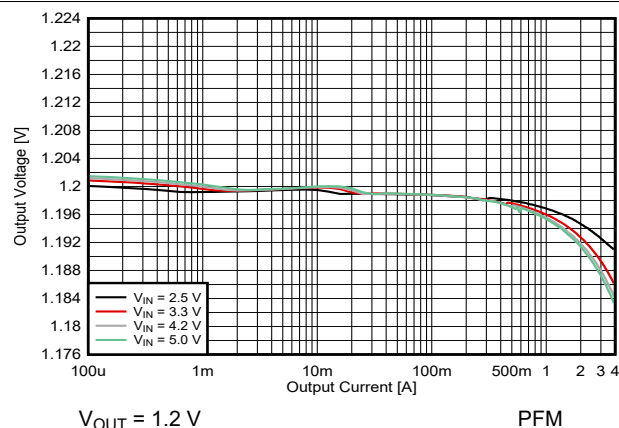
9-16. Output Voltage versus Output Current



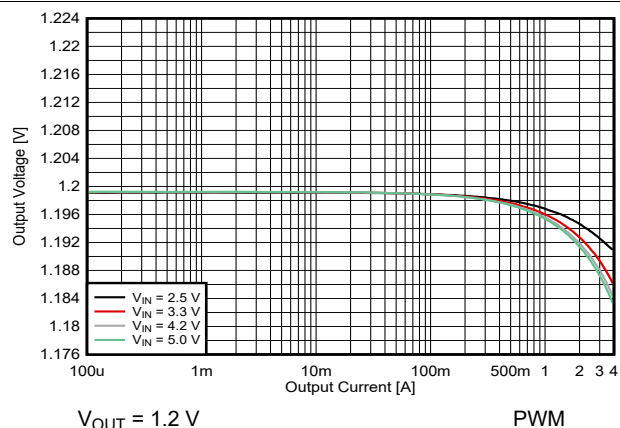
9-17. Output Voltage versus Output Current



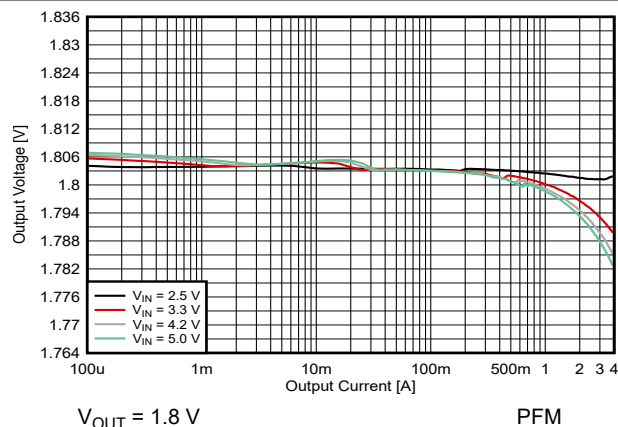
9-18. Output Voltage versus Output Current



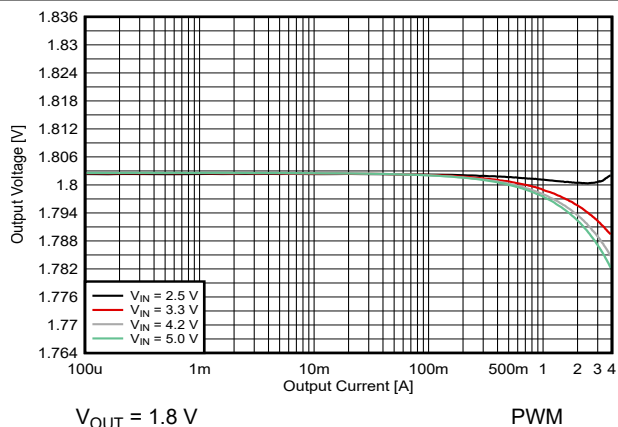
9-19. Output Voltage versus Output Current



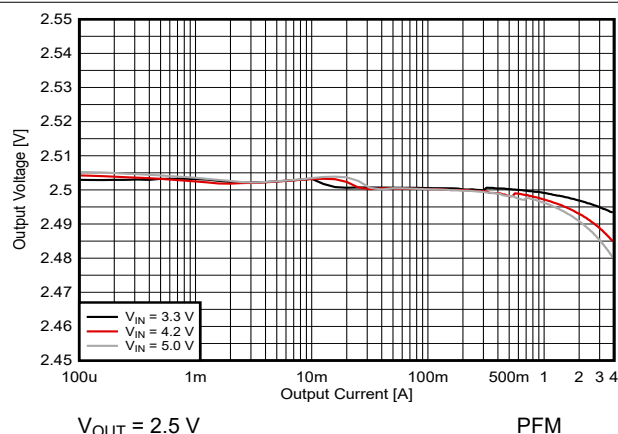
9-20. Output Voltage versus Output Current



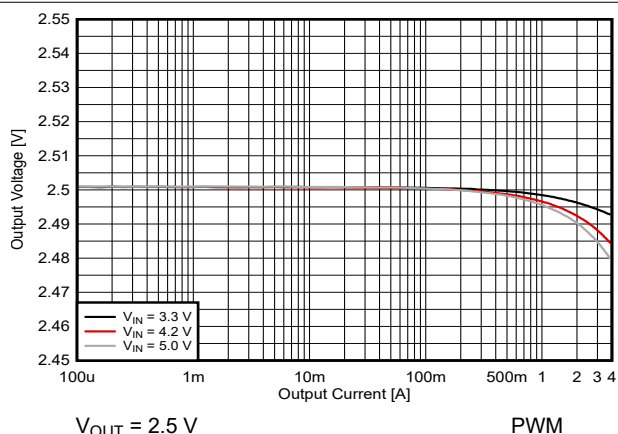
9-21. Output Voltage versus Output Current



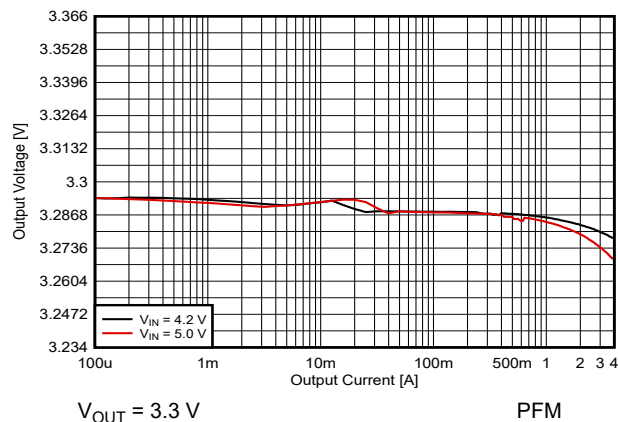
9-22. Output Voltage versus Output Current



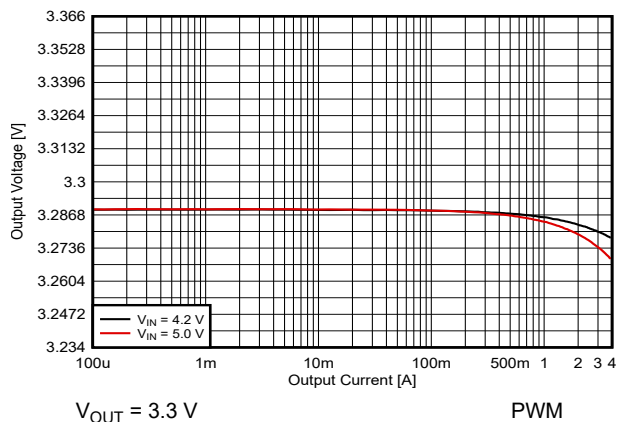
9-23. Output Voltage versus Output Current



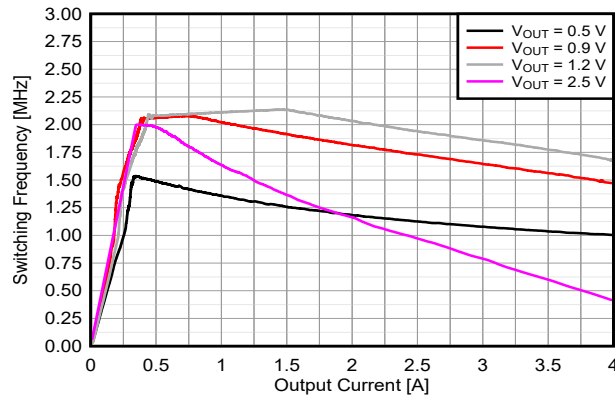
9-24. Output Voltage versus Output Current



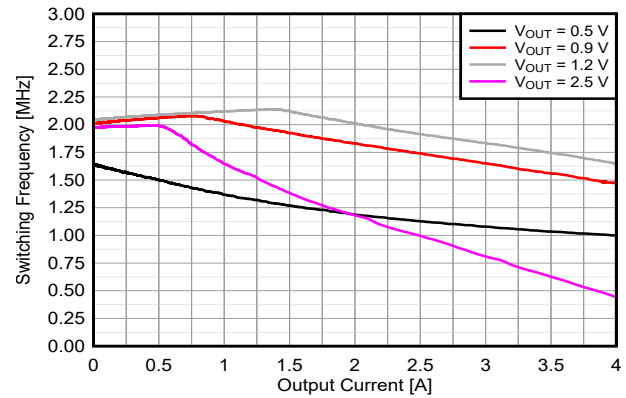
9-25. Output Voltage versus Output Current



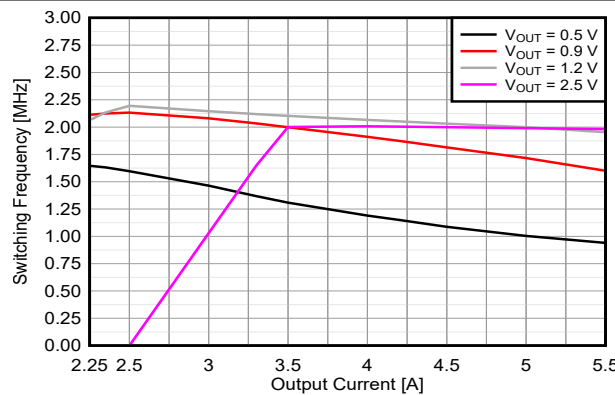
9-26. Output Voltage versus Output Current



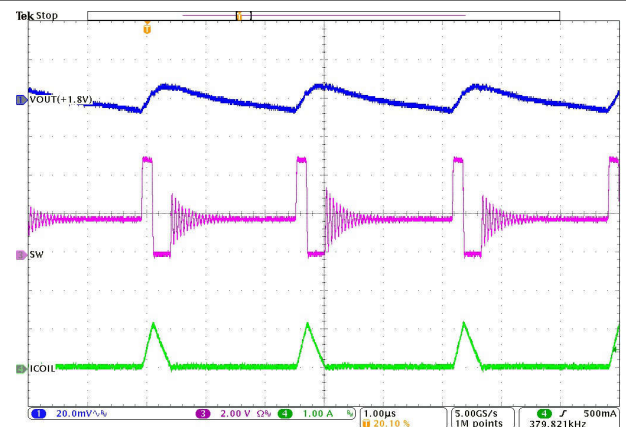
9-27. Switching Frequency versus Output Current



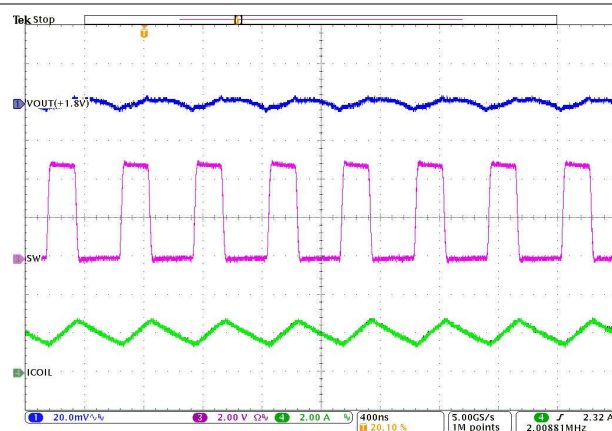
9-28. Switching Frequency versus Output Current



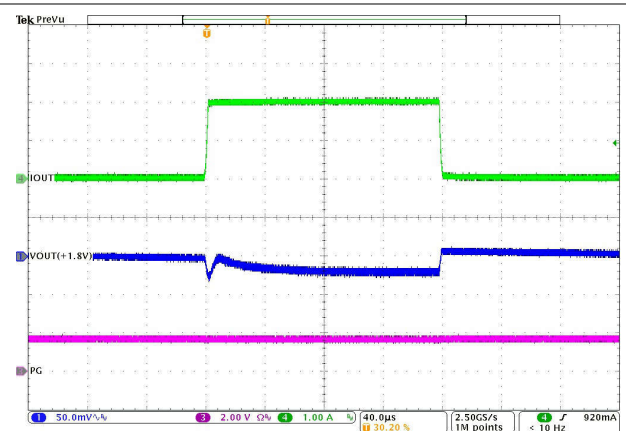
9-29. Switching Frequency versus Input Voltage



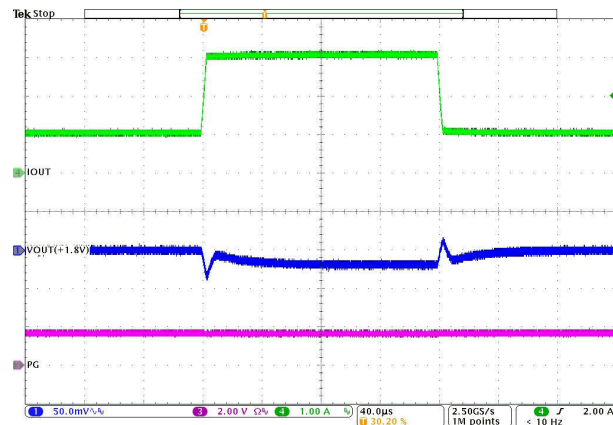
9-30. Output Voltage Ripple



9-31. Output Voltage Ripple

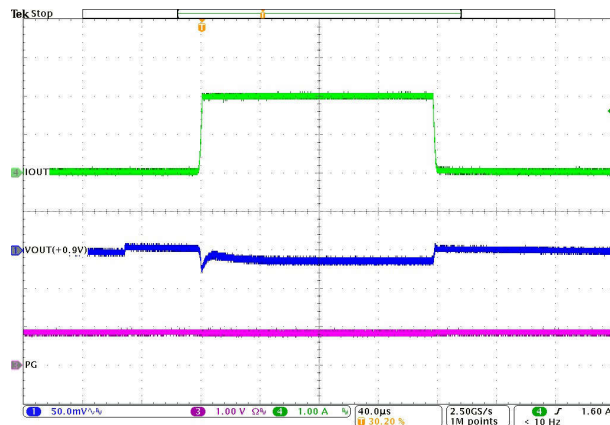


9-32. Load Transient



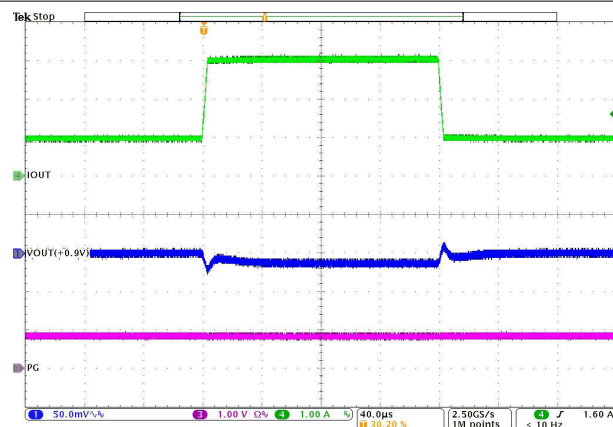
$I_{OUT} = 1\text{ A to }3\text{ A}$ PWM Slew rate = $1\text{ A}/\mu\text{s}$

図 9-33. Load Transient



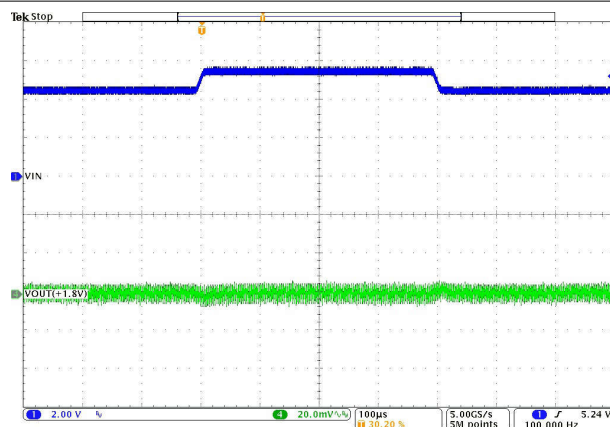
$V_{IN} = 3.3\text{ V}$ PFM $I_{OUT} = 1\text{ mA to }2\text{ A}$
 $V_{OUT} = 0.9\text{ V}$ Transient BoM Slew rate = $1\text{ A}/\mu\text{s}$

図 9-34. Load Transient



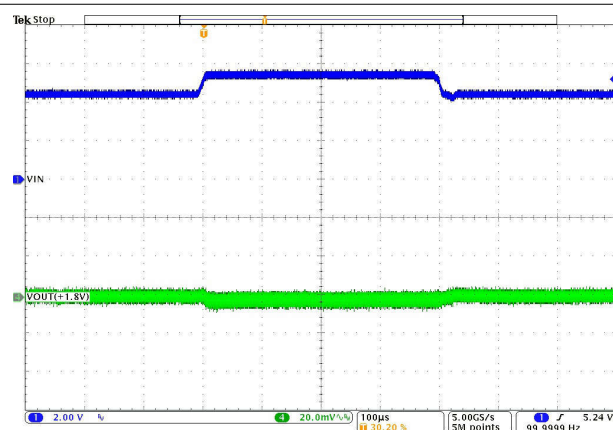
$V_{IN} = 3.3\text{ V}$ PWM $I_{OUT} = 1\text{ A to }3\text{ A}$
 $V_{OUT} = 0.9\text{ V}$ Transient BoM Slew rate = $1\text{ A}/\mu\text{s}$

図 9-35. Load Transient



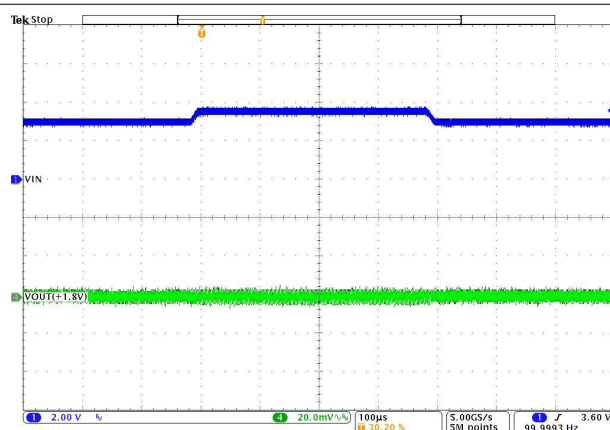
$V_{IN} = 4.5\text{ V to }5.5\text{ V}$ PFM $I_{OUT} = 100\text{ mA}$

図 9-36. Line Transient



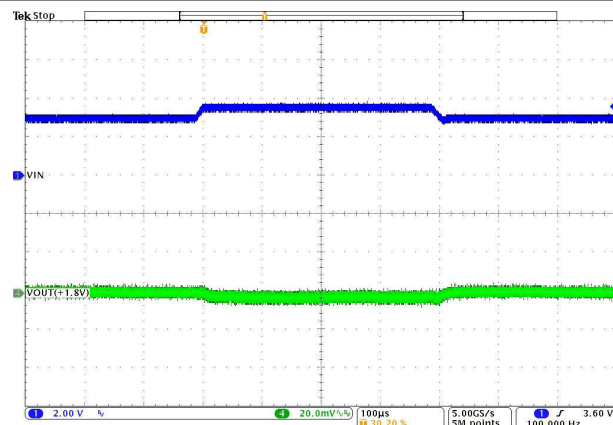
$V_{IN} = 4.5\text{ V to }5.5\text{ V}$ PWM $I_{OUT} = 2.0\text{ A}$

図 9-37. Line Transient



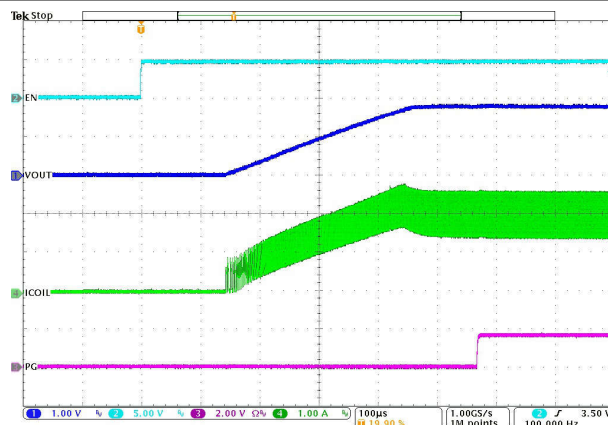
$V_{IN} = 3.0\text{ V to }3.6\text{ V}$ PFM $I_{OUT} = 100\text{ mA}$

図 9-38. Line Transient



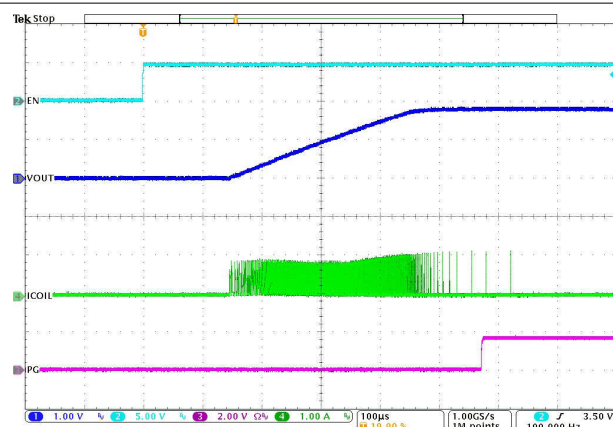
$V_{IN} = 3.0\text{ V to } 3.6\text{ V}$ PWM $I_{OUT} = 2.0\text{ A}$

図 9-39. Line Transient



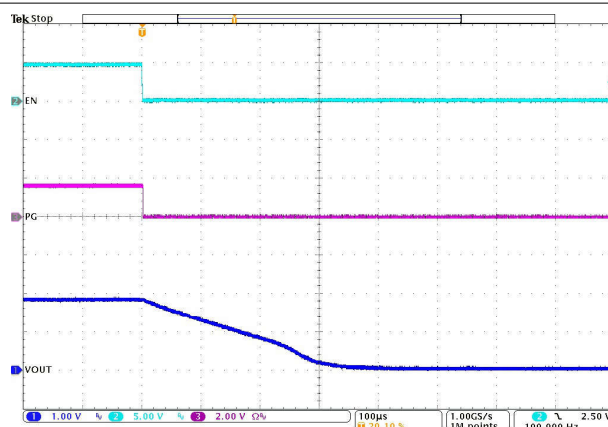
$I_{OUT} = 2.0\text{ A}$ PFM or PWM $T_A = 25\text{ }^{\circ}\text{C}$

図 9-40. Start-Up With Load



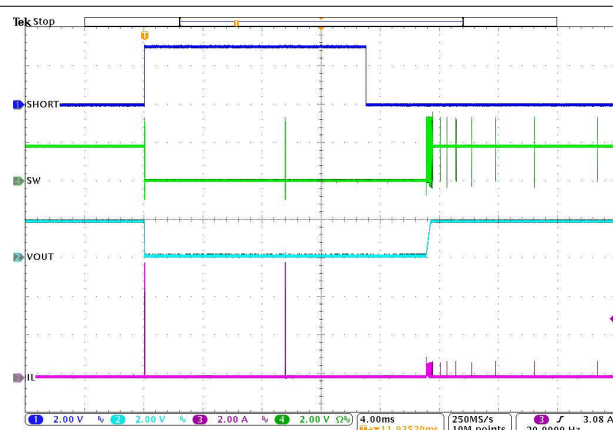
$I_{OUT} = 0\text{ mA}$ PFM or PWM $T_A = 25\text{ }^{\circ}\text{C}$

図 9-41. Start-Up With No Load



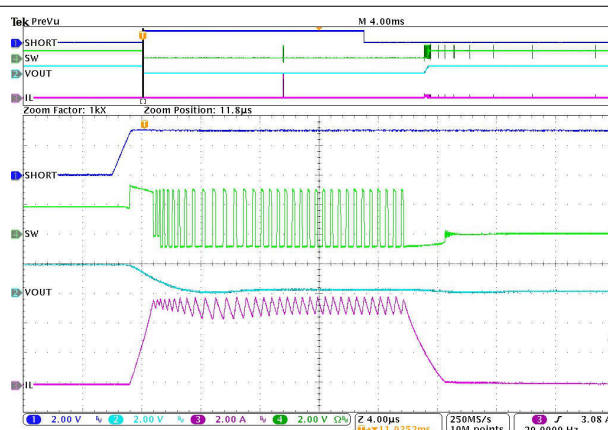
$I_{OUT} = 0\text{ mA}$ PFM $T_A = 25\text{ }^{\circ}\text{C}$

図 9-42. Disable, Active Output Discharge at No Load



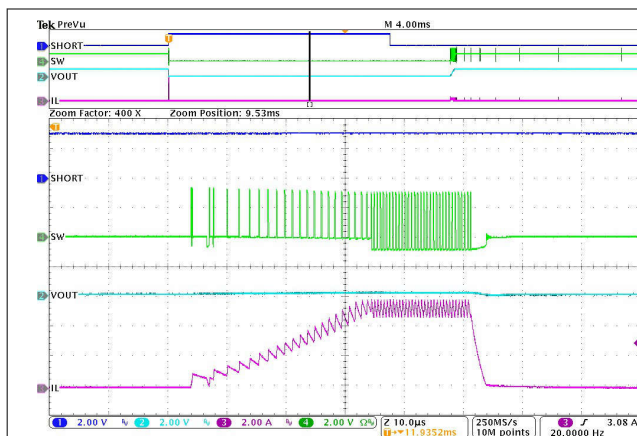
PFM or PWM $T_A = 25\text{ }^{\circ}\text{C}$

図 9-43. HICCUP Short-Circuit Protection



PFM or PWM $T_A = 25\text{ }^{\circ}\text{C}$

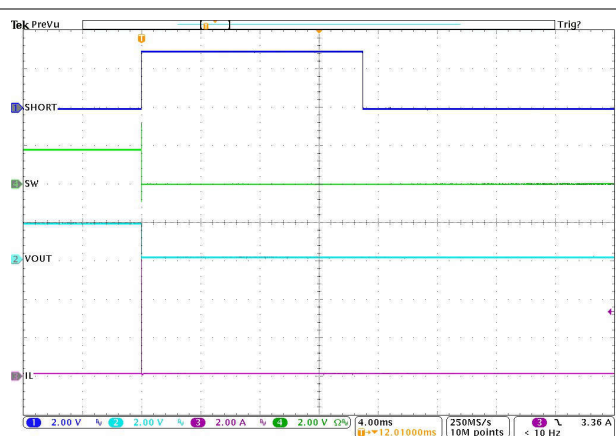
図 9-44. HICCUP Short-Circuit Protection (Zoom In)



PFM or PWM

$T_A = 25^\circ\text{C}$

9-45. HICCUP Short-Circuit Protection (Zoom In - Second Hiccup)

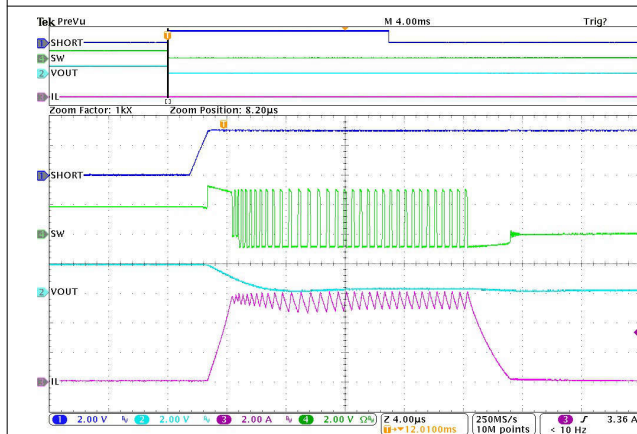


PFM or PWM

TPS628303BDRL

$T_A = 25^\circ\text{C}$

9-46. Latch-off Short-Circuit Protection

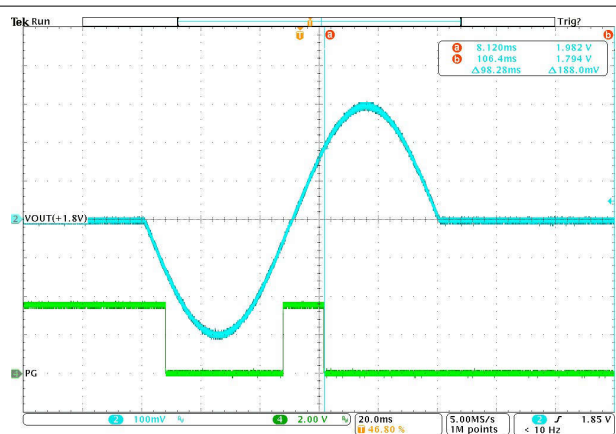


PFM or PWM

TPS628303BDRL

$T_A = 25^\circ\text{C}$

9-47. Latch-off Short-Circuit Protection (Zoom In)



PFM or PWM

TPS628303BDRLR

$T_A = 25^\circ\text{C}$

9-48. Latch-off Overvoltage Protection

9.3 Power Supply Recommendations

The TPS62830x family does not have special requirements for the input power supply and is designed to operate from an input voltage supply range from 2.25 V to 5.5 V. The output current of the input power supply must be rated according to the supply voltage, output voltage, and output current of the device.

9.4 Layout

9.4.1 Layout Guidelines

The printed-circuit-board (PCB) layout is an important step to maintain the high performance of the device. See [Layout Example](#) for the recommended low EMI PCB layout.

- Place the input and output capacitors and the inductor as close as possible to the IC. This action keeps the power traces short. Routing these power traces direct and wide results in low trace resistance and low parasitic inductance.
- Connect the low side of the input and output capacitors properly to the GND pin to avoid a ground potential shift.

- Take special care to avoid noise being induced. The sense traces connected to FB is a signal trace. Keep these traces away from SW nodes. The connection of the output voltage trace for the FB resistors must be made at the output capacitor.
- Refer to [Layout Example](#) for an example of component placement, routing, and thermal design with good EMI performance.

9.4.2 Layout Example

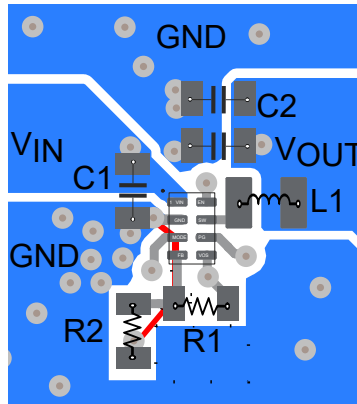


図 9-49. PCB Layout Recommendation (RZE Package)

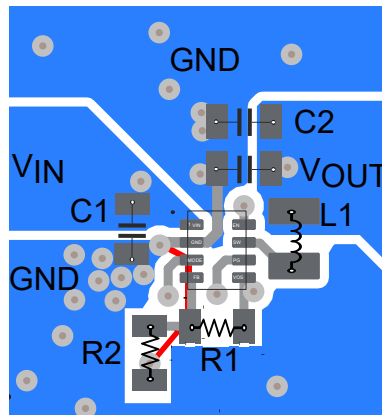


図 9-50. PCB Layout Recommendation (DRL Package)

9.4.2.1 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component.

Two basic approaches for enhancing thermal performance are:

- Improving the power dissipation capability of the PCB design
- Introducing airflow in the system

The Thermal Data section in [Thermal Information](#) provides the thermal metric of the device on the EVM after considering the PCB design of real applications. The big copper planes connecting to the pads of the IC on the PCB improve the thermal performance of the device. For more details on how to use the thermal parameters, see the Thermal Characteristics application notes, [Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs](#) and [Semiconductor and IC Package Thermal Metrics](#).

10 Device and Documentation Support

10.1 Device Support

10.1.1 サード・パーティ製品に関する免責事項

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10.1.2 Development Support

10.1.2.1 Custom Design With WEBENCH® Tools

[Click here](#) to create a custom design using the TPS62830x device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs](#) application note
- Texas Instruments, [Semiconductor and IC Package Thermal Metrics](#) application note

10.3 サポート・リソース

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この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS628301ADRLR	ACTIVE	SOT-5X3	DRL	8	4000	RoHS & Green	Call TI SN	Level-1-260C-UNLIM	-40 to 125	01A	Samples
TPS628301ARZER	ACTIVE	WQFN-HR	RZE	8	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	01A	Samples
TPS628302ADRLR	ACTIVE	SOT-5X3	DRL	8	4000	RoHS & Green	Call TI SN	Level-1-260C-UNLIM	-40 to 125	02A	Samples
TPS628302ARZER	ACTIVE	WQFN-HR	RZE	8	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	02A	Samples
TPS628303ADRLR	ACTIVE	SOT-5X3	DRL	8	4000	RoHS & Green	Call TI SN	Level-1-260C-UNLIM	-40 to 125	03A	Samples
TPS628303ARZER	ACTIVE	WQFN-HR	RZE	8	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	03A	Samples
TPS628303BDRLR	ACTIVE	SOT-5X3	DRL	8	4000	RoHS & Green	Call TI SN	Level-1-260C-UNLIM	-40 to 125	03B	Samples
TPS628304ADRLR	ACTIVE	SOT-5X3	DRL	8	4000	RoHS & Green	Call TI SN	Level-1-260C-UNLIM	-40 to 125	04A	Samples
TPS628304ARZER	ACTIVE	WQFN-HR	RZE	8	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	04A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

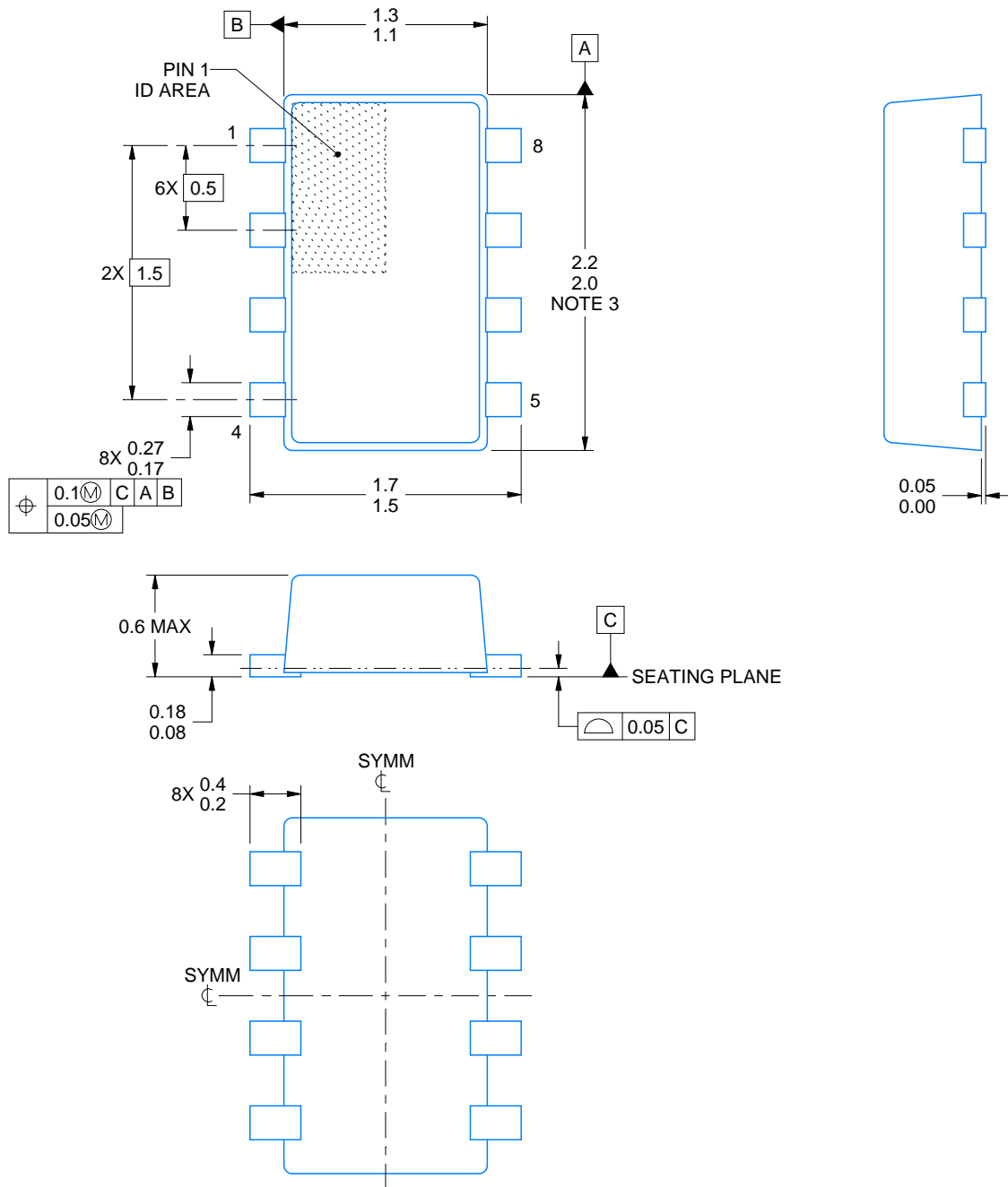
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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NOTES:

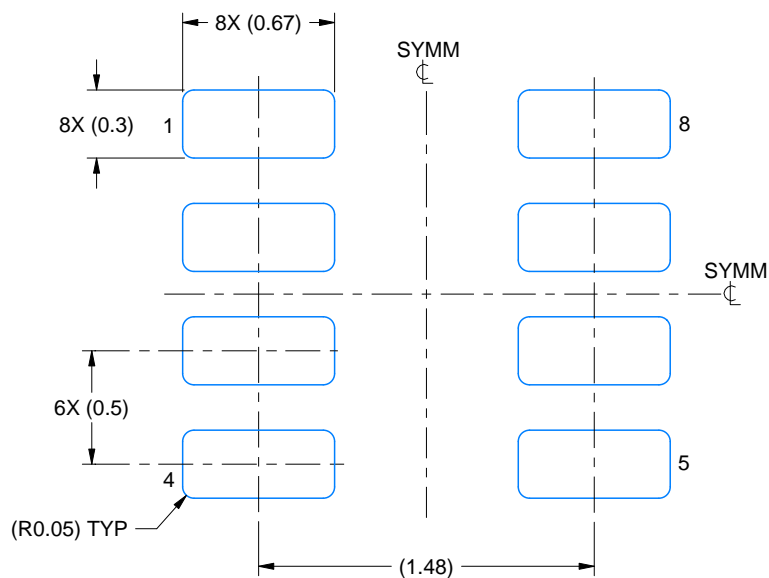
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC Registration MO-293, Variation UDAD

EXAMPLE BOARD LAYOUT

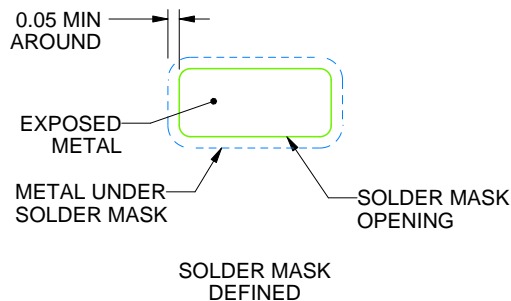
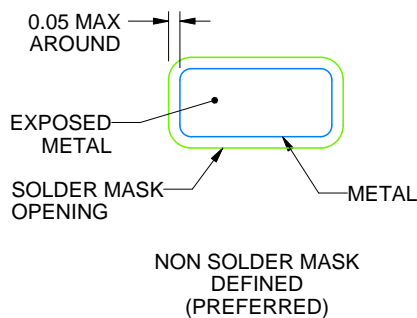
DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDERMASK DETAILS

4224486/E 12/2021

NOTES: (continued)

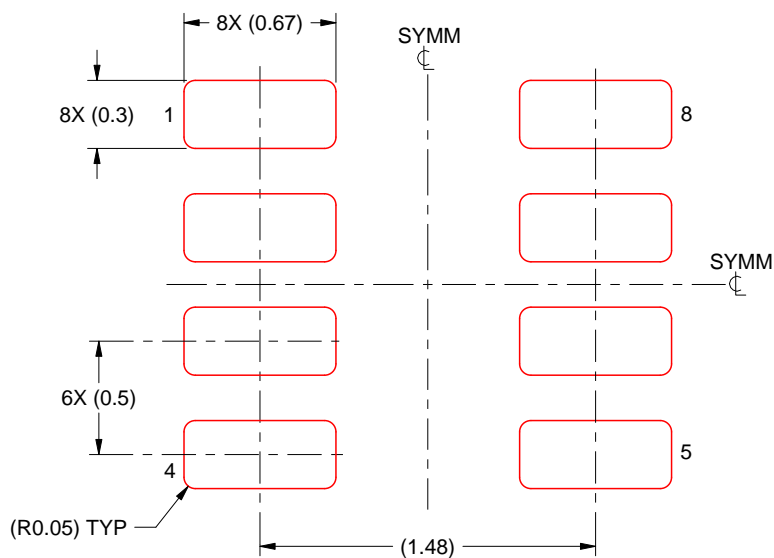
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE

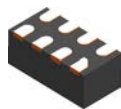


SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4224486/E 12/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

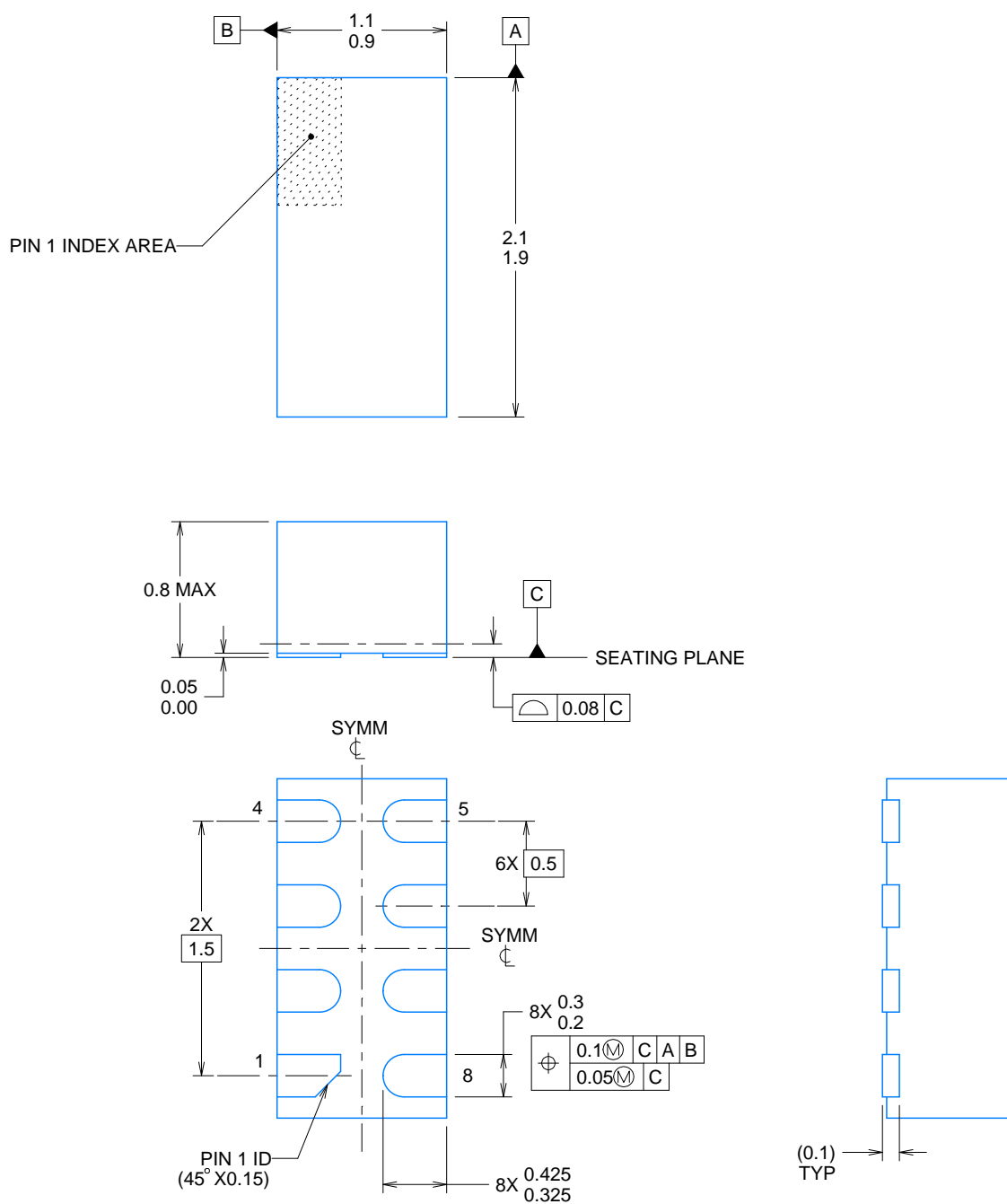


RZE0008A

PACKAGE OUTLINE

WQFN-HR - 0.8mm max height

QFN (PLASTIC QUAD FLATPACK - NO LEAD)



4228328/A 12/2021

NOTES:

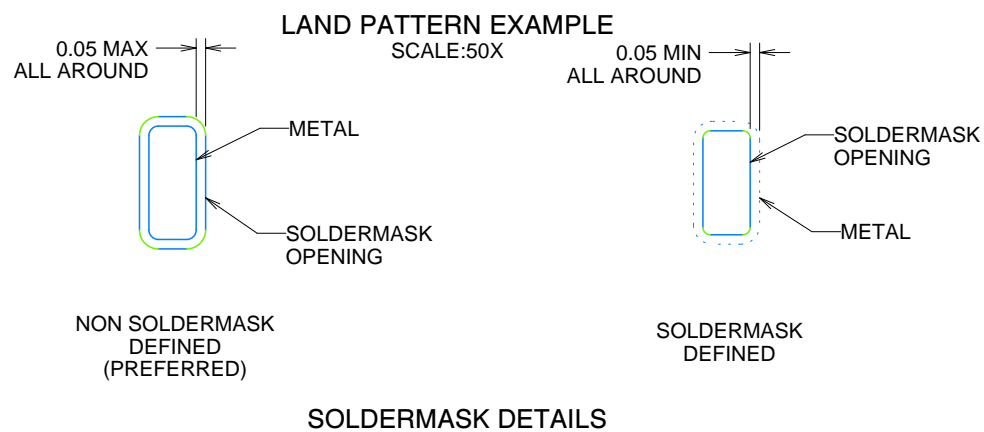
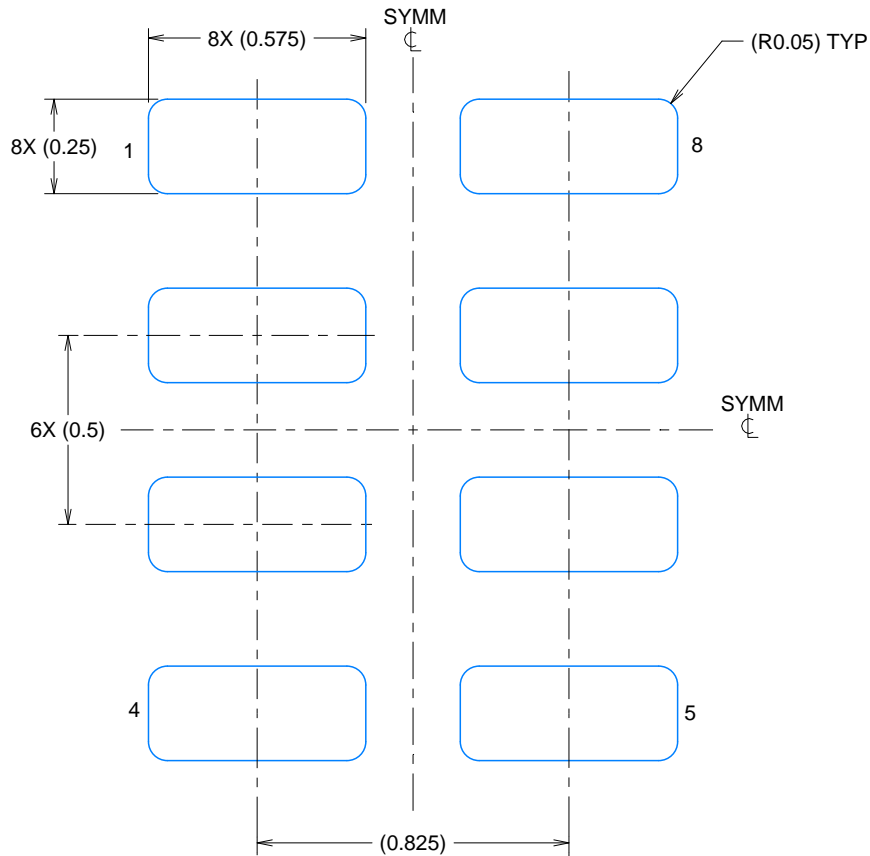
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

RZE0008A

WQFN-HR - 0.8mm max height

QFN (PLASTIC QUAD FLATPACK - NO LEAD)



4228328/A 12/2021

NOTES: (continued)

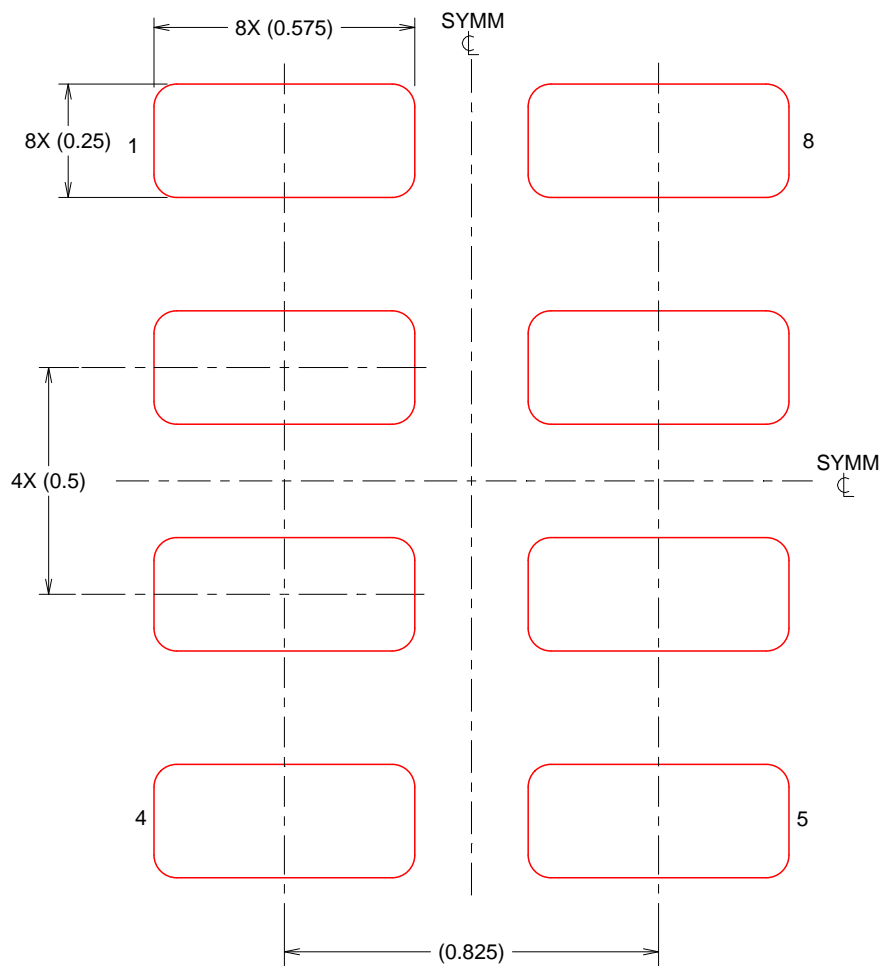
3. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/sluea271).

EXAMPLE STENCIL DESIGN

RZE0008A

WQFN-HR - 0.8mm max height

QFN (PLASTIC QUAD FLATPACK - NO LEAD)



SOLDERPASTE EXAMPLE
BASED ON 0.1mm THICK STENCIL

SCALE:60X

4228328/A 12/2021

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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