

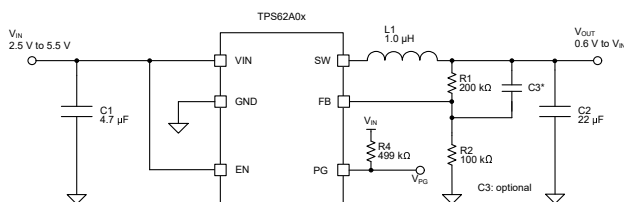
# TPS62A0x、TPS62A0xA、TPS62A02Nx、1A および 2A 高効率同期整流降圧コンバータ、SOT-563 および SOT-23 パッケージ

## 1 特長

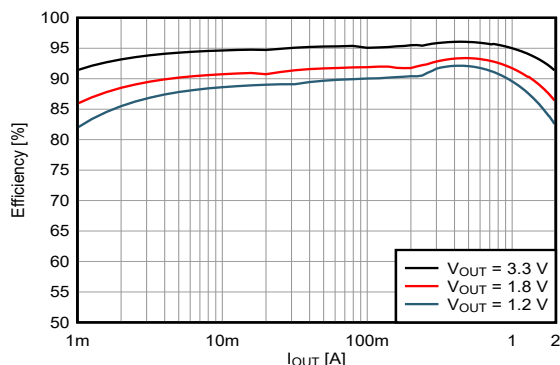
- 入力電圧範囲: 2.5V~5.5V
- 調整可能な出力電圧範囲: 0.6V~ $V_{IN}$
- 180m $\Omega$ /120m $\Omega$  低  $R_{DS(ON)}$  スイッチ (1A DRL)
- 100m $\Omega$ /67m $\Omega$  低  $R_{DS(ON)}$  スイッチ (1A DDC、2A)
- < 23 $\mu$ A の静止電流
- タイミング精度: 1% (0°C~125°C)
- 100% モード動作
- 2.4MHz のスイッチング周波数
- パワーセーブモードまたは PWM オプションが利用可能
- パワーグッド出力ピン (オプション)
- 短絡保護 (HICCUP)
- ソフトスタートアップを内蔵
- アクティブ出力放電
- サーマルシャットダウン保護機能
- TLV62585 (DRL) とピン互換
- TLV62569 (DDC) とピン互換

## 2 アプリケーション

- セットトップボックス、TV アプリケーション
- IP ネットワークカメラ、多機能プリンタ
- ワイヤレスルータ、ソリッドステートドライブ
- バッテリ駆動アプリケーション
- 汎用 POL (ポイントオブロード) 電源



代表的なアプリケーション



5V<sub>IN</sub> での効率と出力電流との関係 (TPS62A02x)

## 3 概要

TPS62A0x デバイスファミリは同期整流降圧型 DC/DC コンバータで、高効率と小型の設計サイズ向けに最適化されています。このデバイスには、最大 2A の出力電流を供給できるスイッチが内蔵されています。中負荷から高負荷では、デバイスはパルス幅変調 (PWM) モードで、2.4MHz のスイッチング周波数で動作します。軽負荷時には、デバイスは自動的にパワーセーブモード (PSM) へ移行し、負荷電流範囲の全体にわたって高い効率を維持します。シャットダウン時には、消費電流も最小限に抑えられます。このデバイスファミリの TPS62A0xA のバリエーションでは、負荷電流範囲全体にわたって強制 PWM で動作します。

TPS62A0x デバイスは、外付けの分圧抵抗によって出力電圧を変更できます。内部のソフトスタート回路により、スタートアップ時の突入電流が制限されます。過電流保護、サーマルシャットダウン保護、パワーグッド (オプション) など、その他の機能も組み込まれています。本デバイスは SOT563 および SOT23-6 パッケージで供給されます。

### パッケージ情報

部品番号	パッケージ (1)	パッケージサイズ (2)
TPS62A01x	DRL (SOT-563, 6)	1.60mm × 1.60mm
	DDC (SOT-23, 6)	2.90mm × 2.80mm
TPS62A02x	DRL (SOT-563, 6)	1.60mm × 1.60mm
	DDC (SOT-23, 6)	2.90mm × 2.80mm
TPS62A02Nx	DRL (SOT-563, 6)	1.60mm × 1.60mm

- (1) 詳細については、[セクション 11](#) を参照してください。
- (2) パッケージサイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。

### 製品情報

部品番号 (1)	動作モード	出力電流	ピン 6
TPS62A01	PSM, PWM	1A	PG
TPS62A01A	FPWM		
TPS62A02	PSM, PWM	2A	OUT
TPS62A02A	FPWM		
TPS62A02N	PSM, PWM		
TPS62A02NA	FPWM		

- (1) 「製品比較」表を参照してください。



## Table of Contents

<b>1 特長</b> .....	1	7.4 Device Functional Modes.....	9
<b>2 アプリケーション</b> .....	1	<b>8 Application and Implementation</b> .....	11
<b>3 概要</b> .....	1	8.1 Application Information.....	11
<b>4 Device Comparison Table</b> .....	3	8.2 Typical Application.....	11
<b>5 Pin Configuration and Functions</b> .....	3	8.3 Power Supply Recommendations.....	17
<b>6 Specifications</b> .....	4	8.4 Layout.....	17
6.1 Absolute Maximum Ratings.....	4	<b>9 Device and Documentation Support</b> .....	19
6.2 ESD Ratings.....	4	9.1 Device Support.....	19
6.3 Recommended Operating Conditions.....	4	9.2 ドキュメントの更新通知を受け取る方法.....	19
6.4 Thermal Information.....	4	9.3 サポート・リソース.....	19
6.5 Electrical Characteristics.....	5	9.4 Trademarks.....	19
6.6 Typical Characteristics.....	7	9.5 静電気放電に関する注意事項.....	19
<b>7 Detailed Description</b> .....	8	9.6 用語集.....	19
7.1 Overview.....	8	<b>10 Revision History</b> .....	20
7.2 Functional Block Diagram.....	8	<b>11 Mechanical, Packaging, and Orderable Information</b> .....	20
7.3 Feature Description.....	8		

## 4 Device Comparison Table

Device Number	Output Current	Package	Operation Mode	Pin 6
TPS62A01DRLR	1A	SOT-563, 6	PSM, PWM	PG
TPS62A01ADRLR			FPWM	
TPS62A02DRLR	2A		PSM, PWM	OUT
TPS62A02ADRLR			FPWM	
TPS62A02NDRLR	1A	SOT-23, 6	PSM, PWM	PG
TPS62A02NADRLR			FPWM	
TPS62A01PDDCR	2A		PSM, PWM	PG
TPS62A01APDDCR			FPWM	
TPS62A02PDDCR	1A	PSM, PWM	PG	
TPS62A02APDDCR		FPWM		

## 5 Pin Configuration and Functions

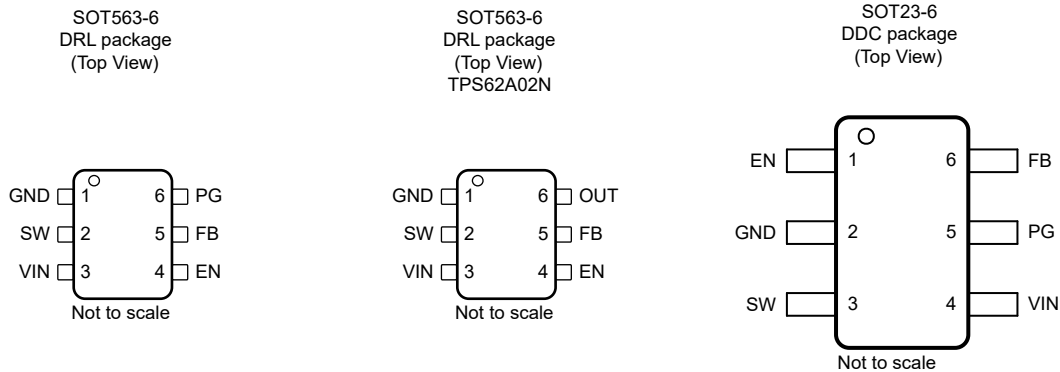


图 5-1. 6-Pin DRL SOT-563 Package (Top View), 6-Pin DDC SOT-23 Package (Top View)

表 5-1. Pin Functions

Name	Pin Number		Type <sup>(1)</sup>	Description
	SOT563-6	SOT23-6		
EN	4	1	I	Device enable logic input. Logic high enables the device. Logic low disables the device and turns the device into shutdown. Do not leave the pin floating.
FB	5	6	I	Feedback pin for the internal control loop. Connect this pin to an external feedback divider.
GND	1	2	G	Ground pin.
PG	6	5	O	Power-good open-drain output pin. The pullup resistor cannot be connected to any voltage higher than 5.5V. If unused, leave the pin open or connect to GND.
OUT <sup>(2)</sup>		/	I	Output voltage sense pin.
SW	2	3	O	Switch pin connected to the internal FET switches and inductor terminal. Connect the inductor of the output filter to this pin.
VIN	3	4	I	Input voltage pin. Connect the input capacitor as close as possible between $V_{IN}$ and GND.

(1) I = Input, O = Output, G = Ground.

(2) Only for TPS62A0xN versions.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT
Pin voltage <sup>(2)</sup>	VIN, EN, PG	-0.3	6.5	V
	SW, DC	-0.3	V <sub>IN</sub> + 0.3	V
	SW, transient < 10 ns	-3.0	10	V
	FB	-0.3	3	V
T <sub>J</sub>	Operating junction temperature	-40	150	°C
T <sub>stg</sub>	Storage temperature	-55	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltage values are with respect to the network ground terminal.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup>	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>IN</sub>	Input supply voltage range	2.5		5.5	V
V <sub>OUT</sub>	Output voltage range	0.6		V <sub>IN</sub>	V
I <sub>OUT</sub>	Output current range	0		1	A
I <sub>OUT</sub>	Output current range <sup>(1)</sup>	0		2	A
L	Effective inductance		1.0		μH
C <sub>OUT</sub>	Output capacitance	V <sub>OUT</sub> < 1.2 V	44		μF
C <sub>OUT</sub>	Output capacitance	1.2 V ≤ V <sub>OUT</sub> < 1.8 V	22		μF
C <sub>OUT</sub>	Output capacitance	V <sub>OUT</sub> ≥ 1.8 V	10		μF
I <sub>PG</sub>	Power Good input current capability	0		1	mA
T <sub>J</sub>	Operating junction temperature	-40		125	°C

- (1) Operating continuously at 2-A with input voltages < 3.3V or at ambient temperatures > 85 °C might result in thermal shutdown, per EVM measurements.

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS62A0x	TPS62A0x	UNIT
		DRL	DDC	
		6 PINS	6 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	157.3	132.1	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	92.2	74.9	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	45.6	45.5	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	4.0	25.5	°C/W

## 6.4 Thermal Information (続き)

THERMAL METRIC <sup>(1)</sup>		TPS62A0x	TPS62A0x	UNIT
		DRL	DDC	
		6 PINS	6 PINS	
$\Psi_{JB}$	Junction-to-board characterization parameter	45.0	45.1	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) report.

## 6.5 Electrical Characteristics

$T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{IN} = 2.5\text{ V}$  to  $5.5\text{ V}$ . Typical values are at  $T_J = 25^\circ\text{C}$  and  $V_{IN} = 5\text{ V}$  (unless otherwise noted)

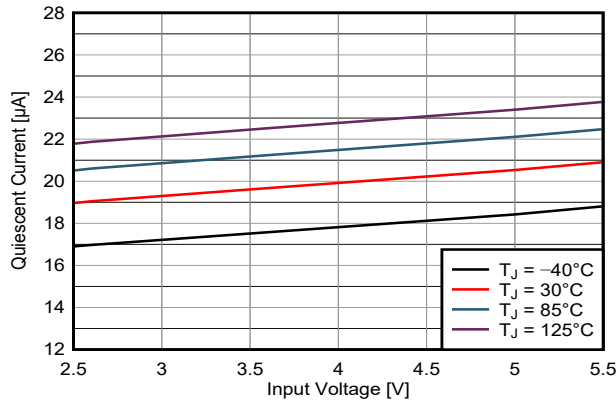
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY</b>						
$I_{Q(VIN)}$	VIN quiescent current	Non-switching; $V_{EN} = \text{High}$ ; $V_{FB} = 610\text{ mV}$ ; TPS62A01xDRL		20		$\mu\text{A}$
$I_{Q(VIN)}$	VIN quiescent current	Non-switching; $V_{EN} = \text{High}$ ; $V_{FB} = 610\text{ mV}$ ; TPS62A01xDDC; TPS62A02		23		$\mu\text{A}$
$I_{SD(VIN)}$	VIN shutdown supply current	$V_{EN} = \text{Low}$		0.01	2	$\mu\text{A}$
<b>UVLO</b>						
$V_{UVLO(R)}$	VIN UVLO rising threshold	$V_{IN}$ rising	2.3	2.4	2.5	V
$V_{UVLO(F)}$	VIN UVLO falling threshold	$V_{IN}$ falling	2.2	2.3	2.4	V
<b>ENABLE</b>						
$V_{EN(R)}$	EN voltage rising threshold	EN rising; enable switching	1.2			V
$V_{EN(F)}$	EN voltage falling threshold	EN falling, disable switching			0.4	V
$V_{EN(LKG)}$	EN Input leakage current	$V_{EN} = 5\text{ V}$			100	nA
<b>REFERENCE VOLTAGE</b>						
$V_{FB}$	FB voltage	$T_J = 0^\circ\text{C}$ to $125^\circ\text{C}$ , PWM mode	594	600	606	mV
$V_{FB}$	FB voltage	PWM mode	591	600	609	mV
$I_{FB(LKG)}$	FB input leakage current	$V_{FB} = 0.6\text{ V}$			100	nA
<b>SWITCHING FREQUENCY</b>						
$f_{SW(FCCM)}$	Switching frequency, FPWM operation	$V_{IN} = 5\text{ V}$ ; $V_{OUT} = 1.8\text{ V}$		2400		kHz
<b>STARTUP</b>						
	Internal fixed soft-start time	From EN = High to $V_{FB} = 0.56\text{ V}$			1	ms
<b>POWER STAGE</b>						
$R_{DS(on)(HS)}$	High-side MOSFET on-resistance	TPS62A01xDRL; $V_{IN} = 5\text{ V}$		180		m $\Omega$
$R_{DS(on)(LS)}$	Low-side MOSFET on-resistance	TPS62A01xDRL; $V_{IN} = 5\text{ V}$		120		m $\Omega$
$R_{DS(on)(HS)}$	High-side MOSFET on-resistance	$V_{IN} = 5\text{ V}$ ; TPS62A01xDDC; TPS62A02		100		m $\Omega$
$R_{DS(on)(LS)}$	Low-side MOSFET on-resistance	$V_{IN} = 5\text{ V}$ ; TPS62A01xDDC; TPS62A02		67		m $\Omega$
<b>OVERCURRENT PROTECTION</b>						
$I_{HS(OC)}$	High-side peak current limit	TPS62A01	1.3	1.8		A
$I_{LS(OC)}$	Low-side valley current limit	TPS62A01		1.8		A
$I_{HS(OC)}$	High-side peak current limit	TPS62A02	2.7	3.4		A
$I_{LS(OC)}$	Low-side valley current limit	TPS62A02xDRL		4.2		A
$I_{LS(OC)}$	Low-side valley current limit	TPS62A02xDDC		3.15		A
<b>POWER GOOD</b>						
$V_{PGTH}$	Power Good threshold	PG low, FB falling		93.5		%
$V_{PGTH}$	Power Good threshold	PG high, FB rising		96		%
	PG delay falling			35		$\mu\text{s}$
	PG delay rising			10		$\mu\text{s}$
$I_{PG(LKG)}$	PG pin Leakage current when open drain output is high	$V_{PG} = 5\text{ V}$			100	nA
	PG pin output low-level voltage	$I_{PG} = 1\text{ mA}$			400	mV

## 6.5 Electrical Characteristics (続き)

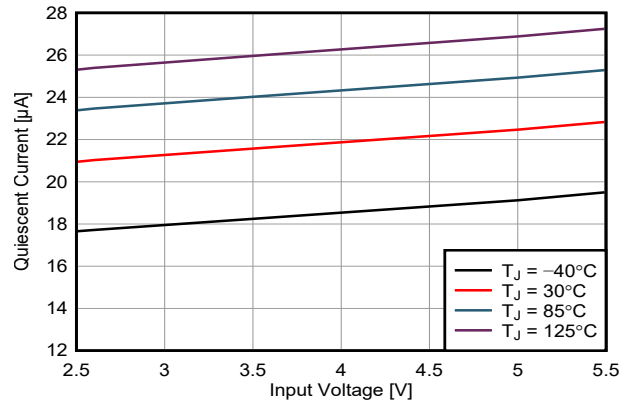
$T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $V_{IN} = 2.5\text{ V}$  to  $5.5\text{ V}$ . Typical values are at  $T_J = 25^{\circ}\text{C}$  and  $V_{IN} = 5\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OUTPUT DISCHARGE</b>					
Output discharge current on SW pin	$V_{IN} = 3\text{ V}$ , $V_{OUT} = 2.0\text{ V}$ ; TPS62A01xDRL		60		mA
Output discharge current on SW pin	$V_{IN} = 3\text{ V}$ , $V_{OUT} = 2.0\text{ V}$ ; TPS62A01xDDC; TPS62A02		76		mA
<b>THERMAL SHUTDOWN</b>					
$T_{J(SD)}$	Thermal shutdown threshold	Temperature rising	170		$^{\circ}\text{C}$
$T_{J(HYS)}$	Thermal shutdown hysteresis		20		$^{\circ}\text{C}$

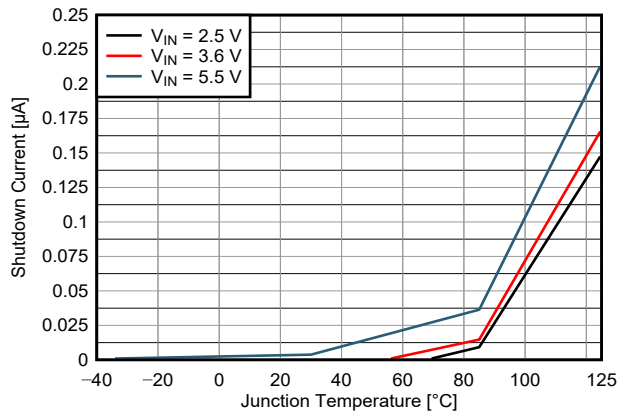
## 6.6 Typical Characteristics



**図 6-1. Quiescent Current vs Input Voltage (TPS62A01)**



**図 6-2. Quiescent Current vs Input Voltage (TPS62A02)**



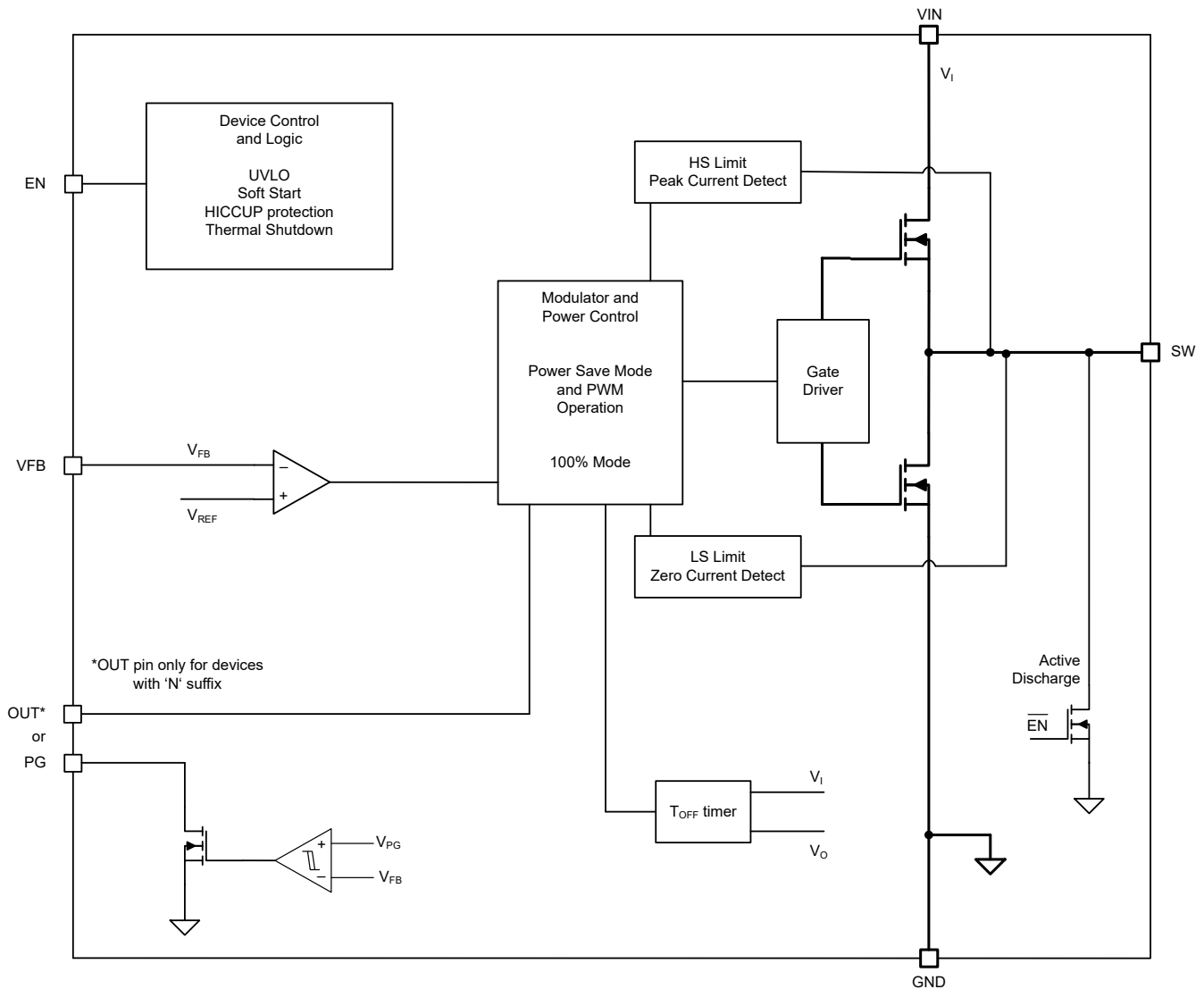
**図 6-3. Shutdown Current vs Junction Temperature**

## 7 Detailed Description

### 7.1 Overview

The TPS62A0x is a high-efficiency synchronous step-down converter. The device operates with an adaptive off time with a peak current control scheme. The device operates typically at 2.4MHz frequency pulse width modulation (PWM) at moderate to heavy load currents. Based on the  $V_{IN}/V_{OUT}$  ratio, a simple circuit sets the required off time for the low-side MOSFET, making the switching frequency relatively constant regardless of the variation of the input voltage, output voltage, and load current.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 Power Save Mode

The device automatically enters power save mode to improve efficiency at light load when the inductor current becomes discontinuous. In power save mode, the converter reduces the switching frequency and minimizes current consumption. In power save mode, the output voltage rises slightly above the nominal output voltage. This effect is minimized by increasing the output capacitor or adding a feedforward capacitor.

### 7.3.2 100% Duty Cycle Low Dropout Operation

The device offers low input-to-output voltage difference by entering 100% duty cycle mode. In this mode, the high-side MOSFET switch is constantly turned on and the low-side MOSFET is switched off. The minimum input voltage to maintain output regulation, depending on the load current and output voltage, is calculated as:

$$V_{IN(MIN)} = V_{OUT} + I_{OUT} \times (R_{DS(ON)} + R_L) \quad (1)$$

where

- $R_{DS(ON)}$  = High-side FET on-resistance
- $R_L$  = Inductor ohmic resistance (DCR)

### 7.3.3 Soft Start

After enabling the device, internal soft-start circuitry ramps up the output voltage, which reaches the nominal output voltage during start-up time, avoiding excessive inrush current and creating a smooth voltage rise slope. Internal soft-start circuitry also prevents excessive voltage drops of primary cells and rechargeable batteries with high internal impedance.

The TPS62A0x is able to start into a prebiased output capacitor. The converter starts with the applied bias voltage and ramps the output voltage to the nominal value.

### 7.3.4 Switch Current Limit and Short-Circuit Protection (HICCUP)

The switch current limit prevents the device from high inductor current and drawing excessive current from the battery or input rail. Due to internal propagation delay, the AC peak current can exceed the static current limit during that time. Excessive current can occur with a shorted or saturated inductor, an overload or shorted output circuit condition. If the inductor current reaches the threshold  $I_{LIM}$ , the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp down the inductor current with an adaptive off time.

When this switch current limit is triggered 32 times, the device stops switching to protect the output. The device then automatically starts a new start-up after a typical delay time of 100 $\mu$ s has passed. This is named HICCUP short-circuit protection. The device repeats this mode until the high load condition disappears. HICCUP protection is also enabled during the start-up.

### 7.3.5 Undervoltage Lockout

To avoid misoperation of the device at low input voltages, an undervoltage lockout (UVLO) is implemented, which shuts down the device at voltages lower than  $V_{UVLO}$ .

### 7.3.6 Thermal Shutdown

The device goes into thermal shutdown and stops switching when the junction temperature exceeds  $T_{JSD}$ . When the device temperature falls below the threshold by 20°C, the device returns to normal operation automatically.

## 7.4 Device Functional Modes

### 7.4.1 Enable and Disable

The device is enabled by setting the EN input to a logic High. Accordingly, a logic Low disables the device. If the device is enabled, the internal power stage starts switching and regulates the output voltage to the set point voltage. The EN input must be terminated and not be left floating.

### 7.4.2 Power Good

The TPS62A0x (except devices with 'N' suffix) has a built-in power-good (PG) feature to indicate whether the output voltage has reached the target and the device is ready. The PG signal can be used for start-up sequencing of multiple rails. The PG pin is an open-drain output that requires a pullup resistor to any voltage up to the recommended input voltage level. PG is low when the device is turned off due to EN, UVLO (undervoltage lockout), or thermal shutdown. VIN must remain present for the PG pin to stay low. If not used, the power-good

can be tie to GND or left open. The PG indicator has a de-glitch to avoid the signal indicating glitches or transient responses from the loop.

**表 7-1. Power-Good indicator Functional Table**

Logic Signals				PG Status
$V_I$	EN Pin	Thermal Shutdown	$V_O$	
$V_I > UVLO$	HIGH	NO	$V_O$ on target	High Impedance
			$V_O < target$	LOW
		YES	LOW	
	LOW	YES	x	LOW
	LOW	x	x	LOW
$V_I < 1.8V$	x	x	x	Undefined

## 8 Application and Implementation

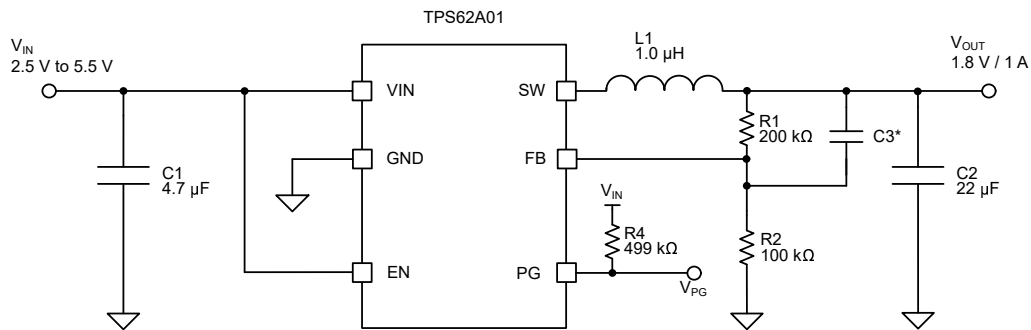
### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

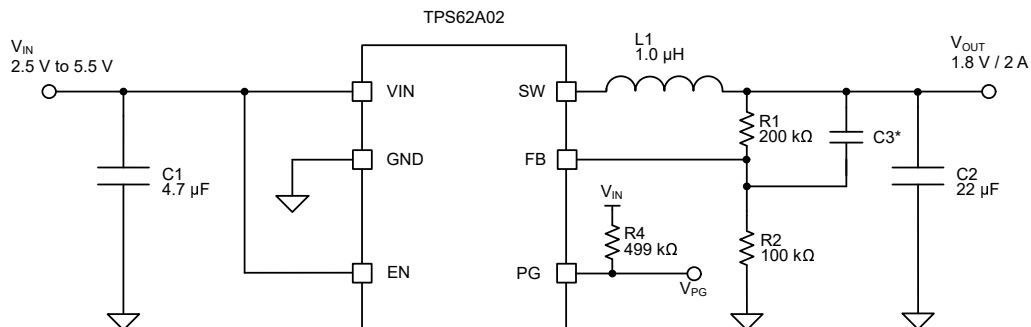
### 8.1 Application Information

The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

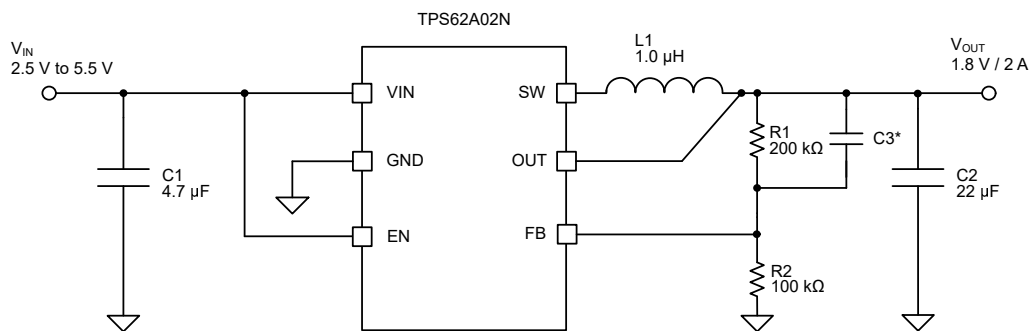
### 8.2 Typical Application



8-1. TPS62A01 Typical Application Circuit



8-2. TPS62A02 Typical Application Circuit



8-3. TPS62A02N Typical Application Circuit

\*C3 is optional

### 8.2.1 Design Requirements

For this design example, use the parameters listed in 表 8-1 as the input parameters

**表 8-1. Design Parameters**

Design Parameter	Example Value
Input voltage	2.5V to 5.5V
Output voltage	1.8V
Maximum output current	1.0A, 2.0A

表 8-2 lists the components used for the example.

**表 8-2. List of Components**

Reference	Description	Manufacturer <sup>(1)</sup>
C1	4.7μF, Ceramic Capacitor, 10V, X7R, size 0805, GRM21BR71A475KA73L	Murata
C2	22μF, Ceramic Capacitor, 10V, X7R, size 0805, GRM21BZ71A226KE15L	Murata
L1	1μH, Power Inductor, DFE252012F-1R0M (1A) / XGL3520-102MEC (2A)	Murata / Coilcraft
R1, R2	Chip resistor, 1%, size 0603	Std.
C3	Optional, 120pF if needed	Std.

(1) See the *Third-Party Products Disclaimer*.

### 8.2.2 Detailed Design Procedure

#### 8.2.2.1 Setting the Output Voltage

The output voltage is set by an external resistor divider according to 式 2.

$$R1 = R2 \times \left( \frac{V_{OUT}}{V_{FB}} - 1 \right) = R2 \times \left( \frac{V_{OUT}}{0.6V} - 1 \right) \quad (2)$$

R2 must not be higher than 100kΩ to provide acceptable noise sensitivity.

#### 8.2.2.2 Output Filter Design

The inductor and output capacitor together provide a low-pass filter. To simplify this process, 表 8-3 outlines possible inductor and capacitor value combinations. Checked cells represent combinations that are proven for stability by simulation and lab test. Check further combinations for each individual application.

**表 8-3. Matrix of Output Capacitor and Inductor Combinations for TPS62A01 and TPS62A02**

V <sub>OUT</sub> [V]	L [μH] <sup>(1)</sup>	C <sub>OUT</sub> [μF] <sup>(2)</sup>		
		10	22	2 × 22
0.6 ≤ V <sub>OUT</sub> < 1.2	1		+	++ <sup>(3)</sup>
1.2 ≤ V <sub>OUT</sub> < 1.8			++ <sup>(3)</sup>	+
1.8 ≤ V <sub>OUT</sub>		+(4)	++ <sup>(3)</sup>	+

(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by +20% and –30%.

(2) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by +20% and –50%.

(3) This LC combination is the standard value and recommended for most applications.

(4) The minimum C<sub>OUT</sub> of 10μF does not support an additional feedforward capacitor.

A 0.47μH inductor can also be used with the same recommended output capacitors for the TPS62A02x. In case a lower output ripple is desired, higher output capacitance can help reduce the ripple.

### 8.2.2.3 Input and Output Capacitor Selection

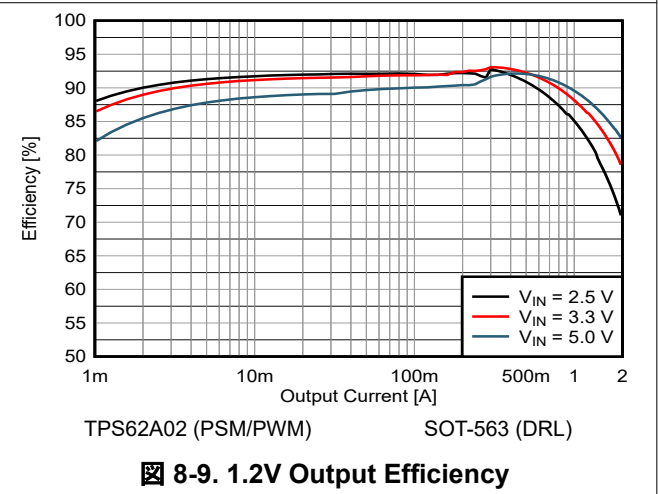
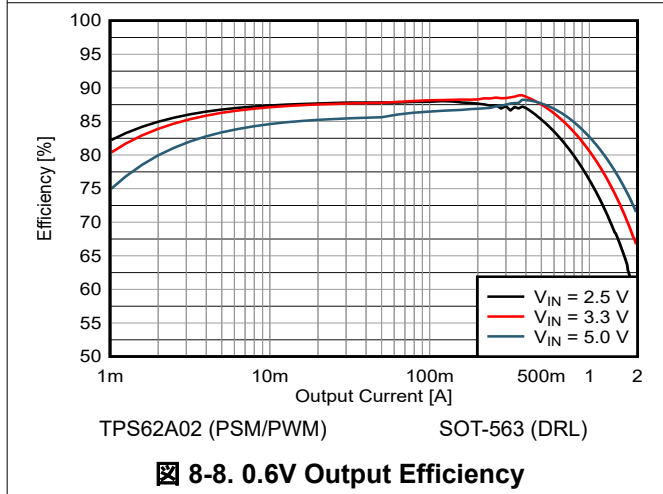
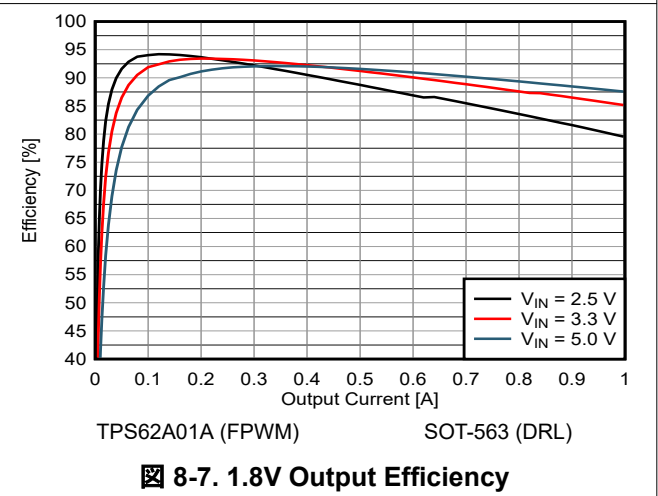
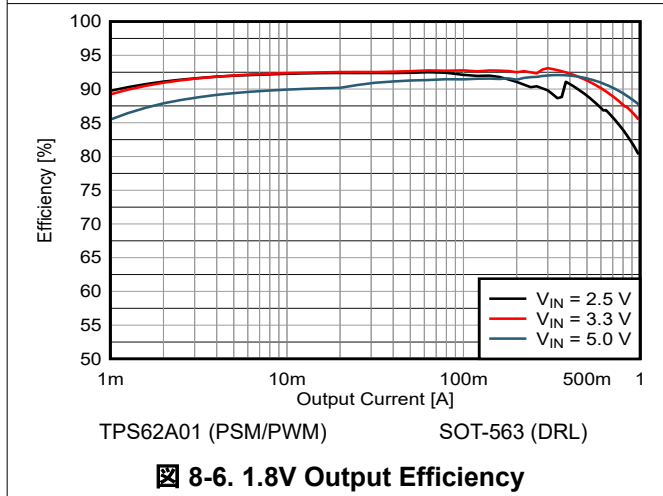
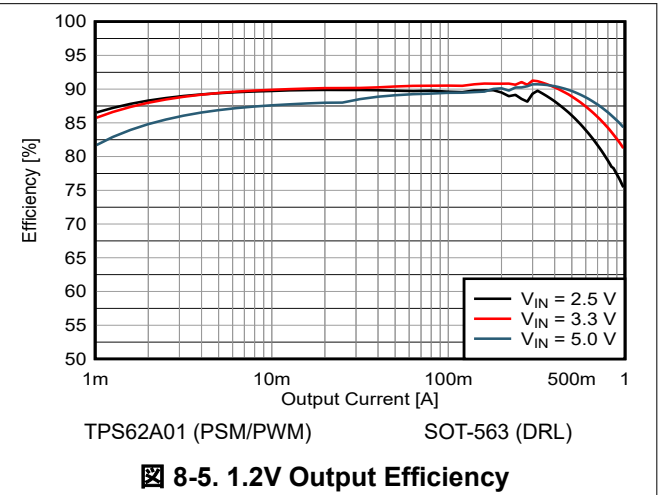
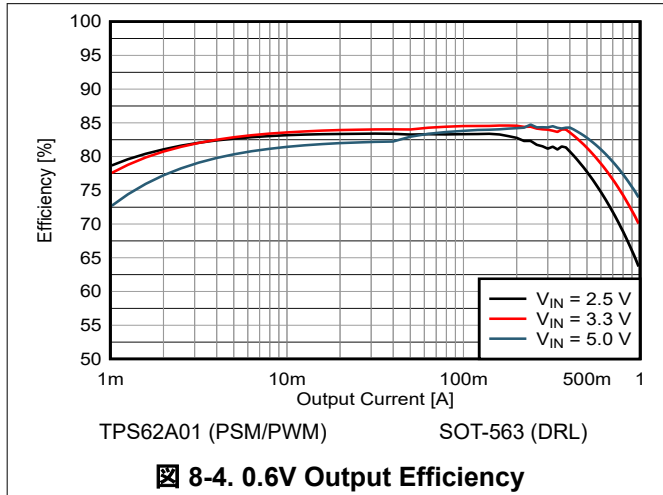
The architecture of the TPS62A0x allows use of tiny ceramic-type output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are thus recommended. To keep resistance up to high frequencies and to achieve narrow capacitance variation with temperature, TI recommends to use X7R or X5R dielectric.

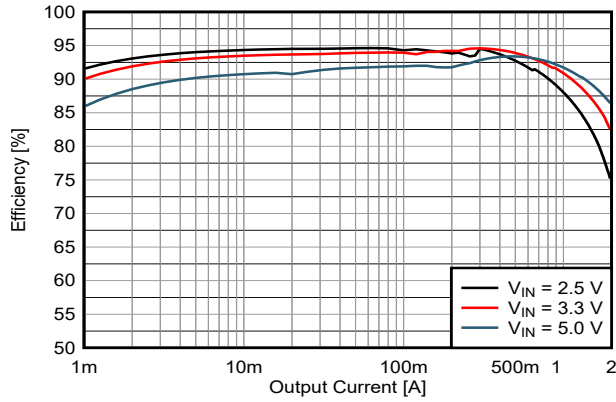
The input capacitor is the low impedance energy source for the converter that helps provide stable operation. TI recommends a low-ESR multilayer ceramic capacitor for best filtering. For most applications, a 4.7 $\mu$ F input capacitor is sufficient; a larger value reduces input voltage ripple.

The TPS62A0x is designed to operate with an output capacitor of 10 $\mu$ F to 47 $\mu$ F, depending on the selected output voltage, as outlined in [表 8-3](#).

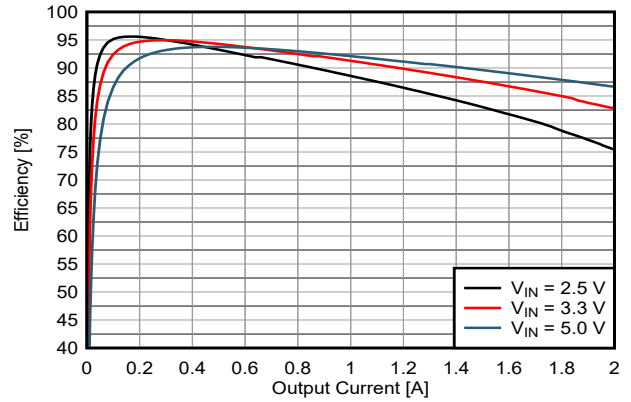
A feedforward capacitor reduces the output ripple in PSM and improves the load transient response. A 120pF capacitor is good for the 1.8V output typical application.

### 8.2.3 Application Curves

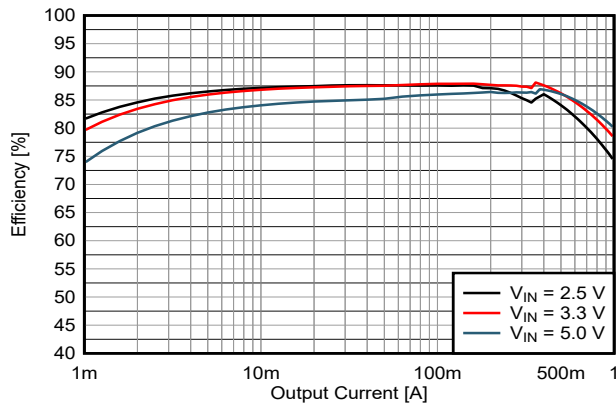




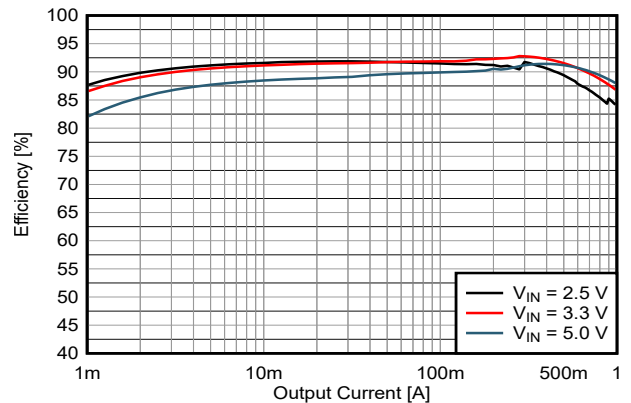
8-10. 1.8V Output Efficiency



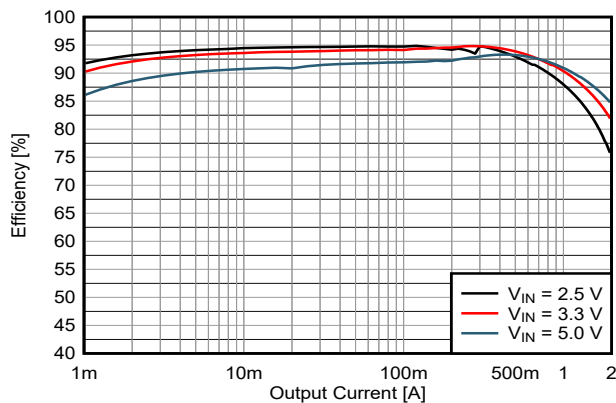
8-11. 1.8V Output Efficiency



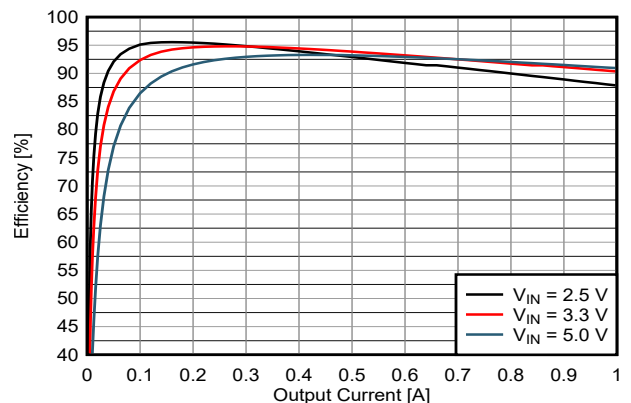
8-12. 0.6V Output Efficiency



8-13. 1.2V Output Efficiency



8-14. 1.8V Output Efficiency



8-15. 1.8V Output Efficiency

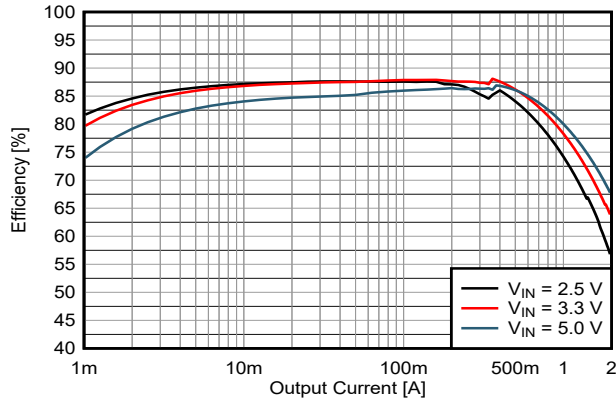


図 8-16. 0.6V Output Efficiency

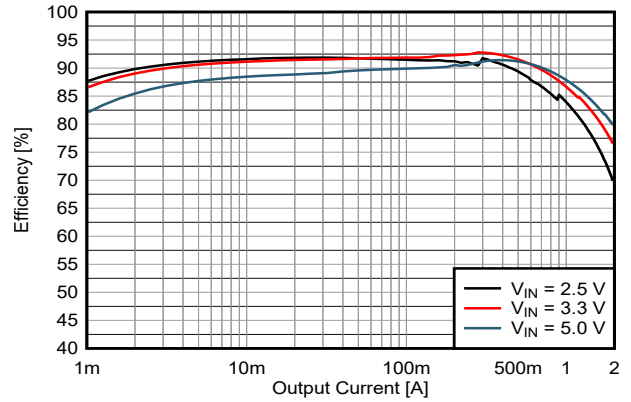


図 8-17. 1.2V Output Efficiency

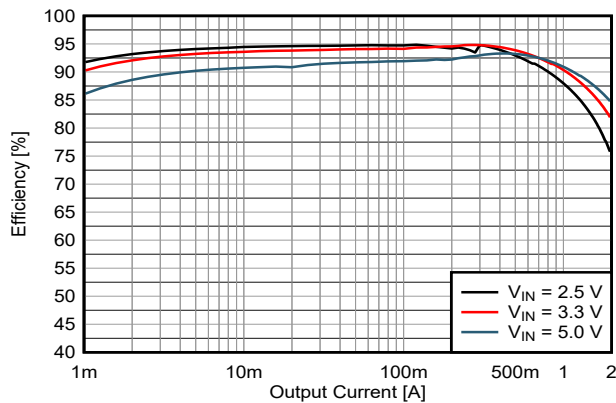


図 8-18. 1.8V Output Efficiency

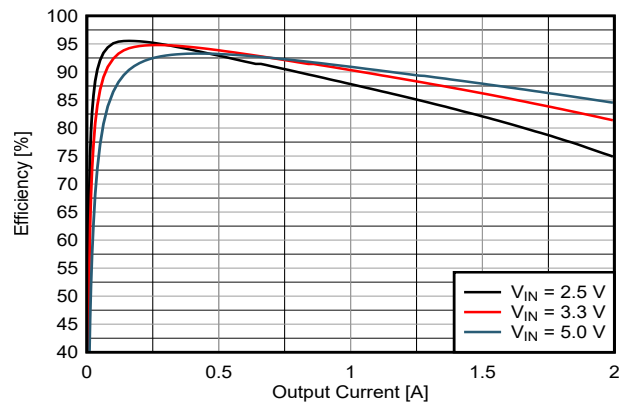


図 8-19. 1.8V Output Efficiency

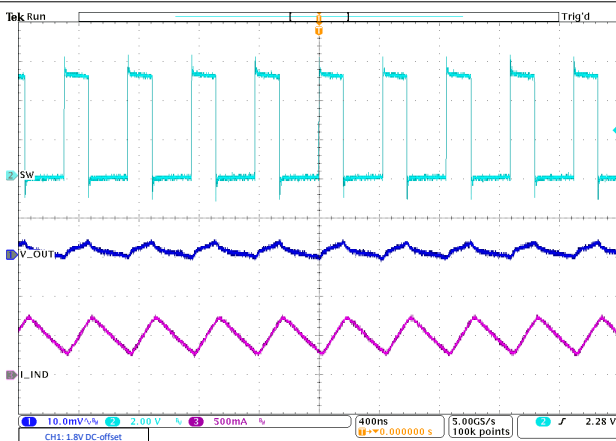


図 8-20. PWM Operation

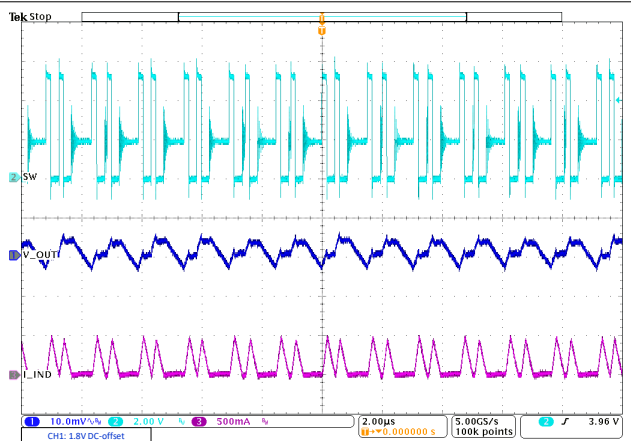
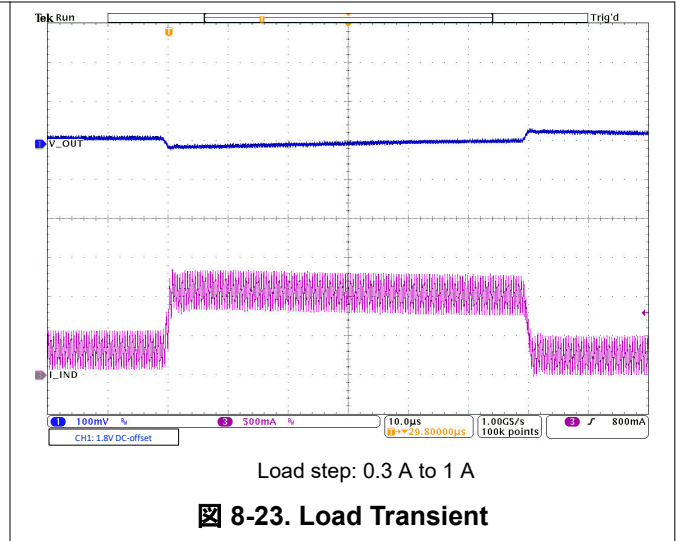
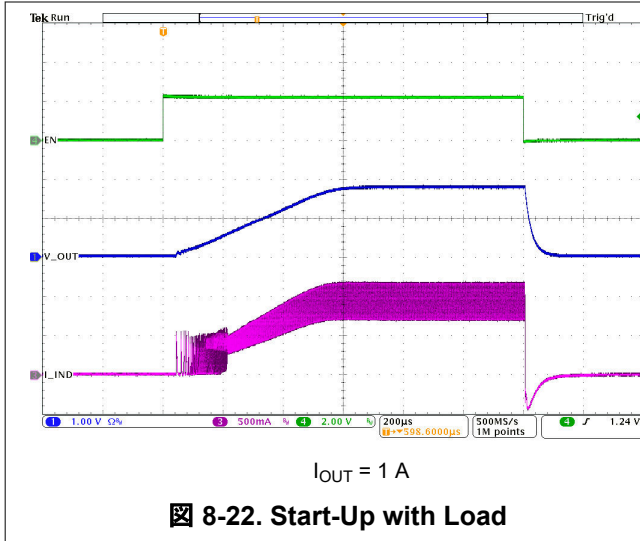


図 8-21. Power Save Mode Operation



### 8.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 2.5V to 5.5V. Make sure that the input power supply has a sufficient current rating for the application.

### 8.4 Layout

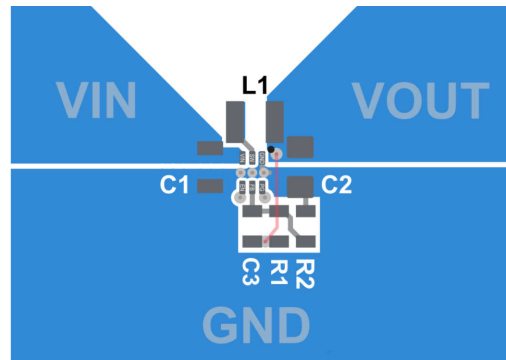
#### 8.4.1 Layout Guidelines

The printed-circuit-board (PCB) layout is an important step to maintain the high performance of the TPS62A01x and TPS62A02x devices.

- Place the input and output capacitors and the inductor as close as possible to the IC. This action keeps the power traces short. Routing these power traces direct and wide results in low trace resistance and low parasitic inductance.
- Connect the low side of the input and output capacitors properly to the GND pin to avoid a ground potential shift.
- The sense traces connected to FB is a signal trace. Take special care to avoid noise being induced. Keep these traces away from SW nodes.
- Use a common ground. GND layers can be used for shielding.

See 8-24 and 8-25 for the recommended PCB layout.

#### 8.4.2 Layout Example



**8-24. TPS62A0x (SOT563) PCB Layout Recommendation**

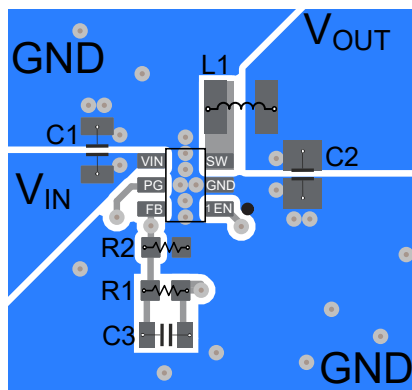


図 8-25. TPS62A0x (SOT23-6) PCB Layout Recommendation

## 9 Device and Documentation Support

### 9.1 Device Support

#### 9.1.1 サード・パーティ製品に関する免責事項

サード・パーティ製品またはサービスに関するテキサス・インスツルメンツの出版物は、単独またはテキサス・インスツルメンツの製品、サービスと一緒に提供される場合に関係なく、サード・パーティ製品またはサービスの適合性に関する是認、サード・パーティ製品またはサービスの是認の表明を意味するものではありません。

### 9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[www.tij.co.jp](http://www.tij.co.jp) のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

### 9.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの [使用条件](#) を参照してください。

### 9.4 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.  
すべての商標は、それぞれの所有者に帰属します。

### 9.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 9.6 用語集

#### テキサス・インスツルメンツ用語集

この用語集には、用語や略語の一覧および定義が記載されています。

## 10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

### Changes from Revision D (April 2024) to Revision E (June 2024) Page

- Changed device status of TPS62A02Nx versions and devices in DDC package from preview to production throughout the data sheet.....3

### Changes from Revision C (December 2023) to Revision D (April 2024) Page

- データシート全体にわたって接尾辞「N」のあるデバイスを追加..... 1
- Changed absolute maximum voltage of VIN, EN and PG from 6V to 6.5V.....4
- Updated block diagram to include devices with 'N' suffix (OUT instead of PG)..... 8

### Changes from Revision B (July 2022) to Revision C (December 2023) Page

- Added DDC package option throughout the data sheet..... 3
- Changed ESD Ratings CDM row from showing testing was per JESD22-C101 to show that testing was per JS-002..... 4
- Changed block diagram PG circuit by swapping  $V_{PG}$  and  $V_{FB}$  .....8

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## 重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、[テキサス・インスツルメンツの販売条件](#)、または [ti.com](https://www.ti.com) やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2024, Texas Instruments Incorporated

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TPS62A01ADRLR</a>	Active	Production	SOT-5X3 (DRL)   6	4000   LARGE T&R	Yes	Call TI   Sn	Level-1-260C-UNLIM	-40 to 125	1J8
TPS62A01ADRLR.A	Active	Production	SOT-5X3 (DRL)   6	4000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1J8
<a href="#">TPS62A01APDDCR</a>	Active	Production	SOT-23- THIN (DDC)   6	3000   LARGE T&R	Yes	Call TI   Sn	Level-1-260C-UNLIM	-40 to 125	A01AP
TPS62A01APDDCR.A	Active	Production	SOT-23- THIN (DDC)   6	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	A01AP
<a href="#">TPS62A01DRLR</a>	Active	Production	SOT-5X3 (DRL)   6	4000   LARGE T&R	Yes	Call TI   Sn	Level-1-260C-UNLIM	-40 to 125	1J7
TPS62A01DRLR.A	Active	Production	SOT-5X3 (DRL)   6	4000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1J7
<a href="#">TPS62A01PDDCR</a>	Active	Production	SOT-23- THIN (DDC)   6	3000   LARGE T&R	Yes	Call TI   Sn	Level-1-260C-UNLIM	-40 to 125	A01P
TPS62A01PDDCR.A	Active	Production	SOT-23- THIN (DDC)   6	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	A01P
<a href="#">TPS62A02ADRLR</a>	Active	Production	SOT-5X3 (DRL)   6	4000   LARGE T&R	Yes	Call TI   Sn	Level-1-260C-UNLIM	-40 to 125	1JM
TPS62A02ADRLR.A	Active	Production	SOT-5X3 (DRL)   6	4000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1JM
<a href="#">TPS62A02APDDCR</a>	Active	Production	SOT-23- THIN (DDC)   6	3000   LARGE T&R	Yes	Call TI   Sn	Level-1-260C-UNLIM	-40 to 125	A02AP
TPS62A02APDDCR.A	Active	Production	SOT-23- THIN (DDC)   6	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	A02AP
<a href="#">TPS62A02DRLR</a>	Active	Production	SOT-5X3 (DRL)   6	4000   LARGE T&R	Yes	Call TI   Sn	Level-1-260C-UNLIM	-40 to 125	1JL
TPS62A02DRLR.A	Active	Production	SOT-5X3 (DRL)   6	4000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1JL
<a href="#">TPS62A02NADRLR</a>	Active	Production	SOT-5X3 (DRL)   6	4000   LARGE T&R	Yes	Call TI   Sn	Level-1-260C-UNLIM	-40 to 125	1SC
TPS62A02NADRLR.A	Active	Production	SOT-5X3 (DRL)   6	4000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1SC
<a href="#">TPS62A02NDRLR</a>	Active	Production	SOT-5X3 (DRL)   6	4000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1SB
TPS62A02NDRLR.A	Active	Production	SOT-5X3 (DRL)   6	4000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1SB
<a href="#">TPS62A02PDDCR</a>	Active	Production	SOT-23- THIN (DDC)   6	3000   LARGE T&R	Yes	Call TI   Sn	Level-1-260C-UNLIM	-40 to 125	A02P
TPS62A02PDDCR.A	Active	Production	SOT-23- THIN (DDC)   6	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	A02P

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TPS62A01, TPS62A01A, TPS62A02, TPS62A02A :**

- Automotive : [TPS62A01-Q1](#), [TPS62A01A-Q1](#), [TPS62A02-Q1](#), [TPS62A02A-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

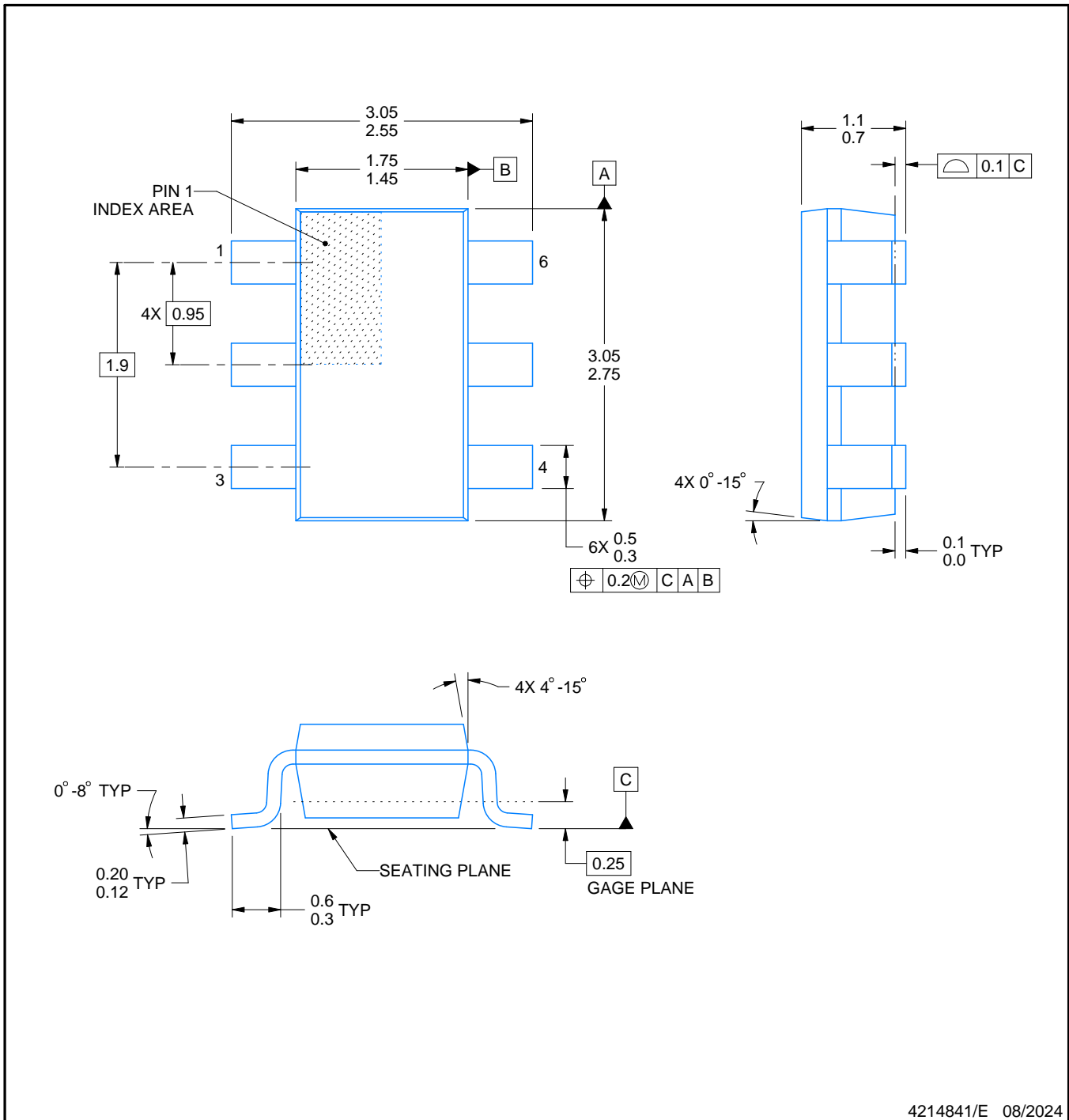

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62A01ADRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TPS62A01APDDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS62A01DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TPS62A01PDDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS62A02ADRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TPS62A02APDDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS62A02DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	1.8	1.8	0.75	4.0	8.0	Q3
TPS62A02DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	1.8	1.8	0.75	4.0	8.0	Q3
TPS62A02DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TPS62A02NADRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TPS62A02NDRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TPS62A02PDDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62A01ADRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
TPS62A01APDDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
TPS62A01DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
TPS62A01PDDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
TPS62A02ADRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
TPS62A02APDDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
TPS62A02DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
TPS62A02DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
TPS62A02DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
TPS62A02NADRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
TPS62A02NDRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
TPS62A02PDDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0



4214841/E 08/2024

NOTES:

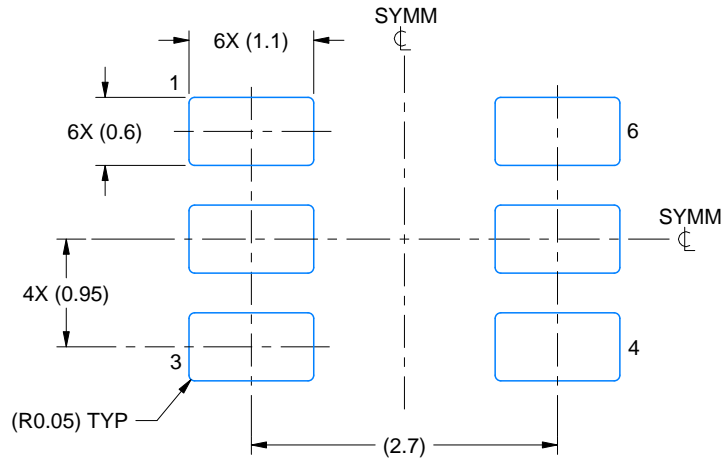
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.

# EXAMPLE BOARD LAYOUT

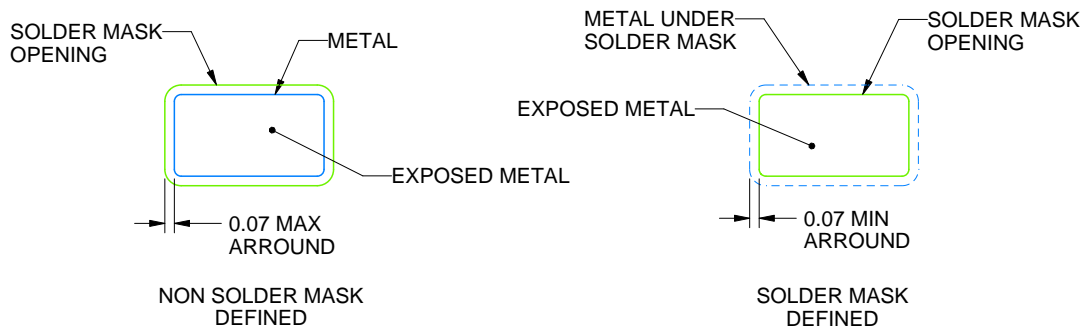
DDC0006A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPLODED METAL SHOWN  
SCALE:15X



SOLDEMASK DETAILS

4214841/E 08/2024

NOTES: (continued)

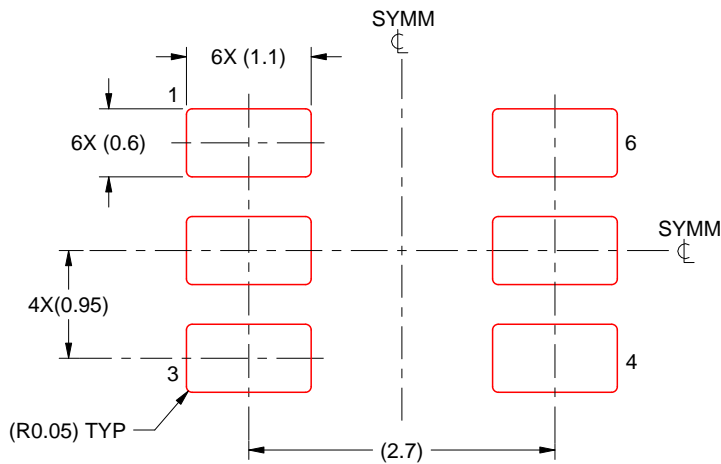
- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DDC0006A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:15X

4214841/E 08/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

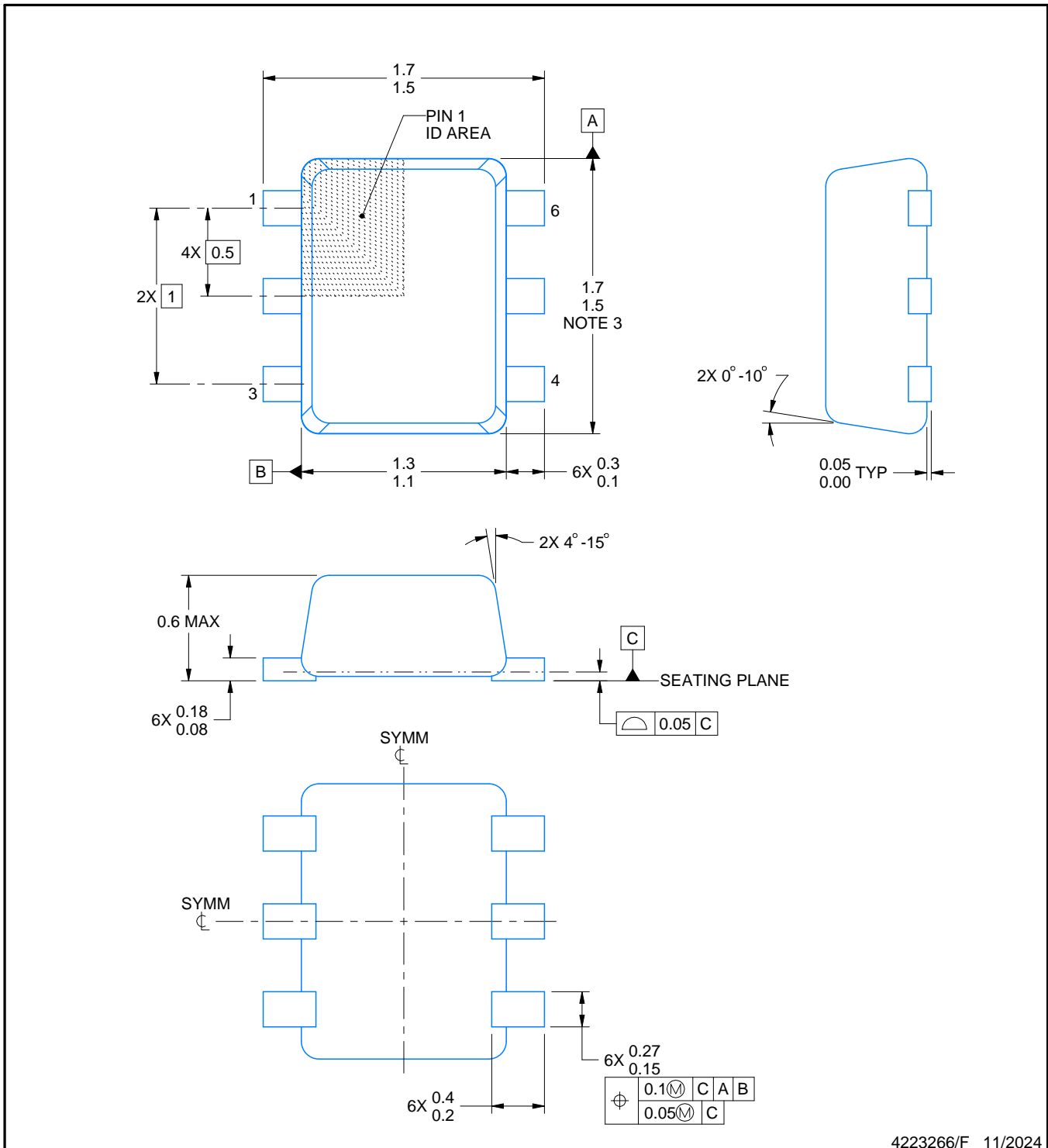
# DRL0006A



# PACKAGE OUTLINE

## SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



4223266/F 11/2024

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

# EXAMPLE BOARD LAYOUT

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
SCALE:30X



SOLDERMASK DETAILS

4223266/F 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

# EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:30X

4223266/F 11/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## 重要なお知らせと免責事項

TI は、技術データと信頼性データ(データシートを含みます)、設計リソース(リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、[TI の総合的な品質ガイドライン](#)、[ti.com](#) または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2026, Texas Instruments Incorporated

最終更新日 : 2025 年 10 月