

# TPS65023-Q1 3つのDC/DC、3つのLDO、I<sup>2</sup>Cインターフェイス およびDVSを搭載した電力管理IC (PMIC)

## 1 特長

- 車載アプリケーション用に認定済み
- 下記内容でAEC-Q100認定済み:
  - デバイス温度グレード 1: 動作時周囲温度範囲 –40°C~125°C
  - デバイスHBM ESD分類レベル2
  - デバイスCDM ESD分類レベルC4A (RHAパッケージ)またはC5 (RSBパッケージ)
- プロセッサ・コア用の1.5A、90%効率の降圧コンバータ (VDCDC1)
- システム電圧用の1.2A、最高95%効率の降圧コンバータ (VDCDC2)
- メモリ電圧用の1A、92%効率の降圧コンバータ (VDCDC3)
- リアルタイム・クロック用の30mA LDO/スイッチ (VRTC)
- 2x200mAの汎用低ドロップアウト (LDO)
- プロセッサ・コア用の動的電圧管理
- 2つのデジタル入力ピンを使用してLDO電圧を事前選択可能
- リセットの遅延時間を外部で変更可能
- バッテリー・バックアップ機能
- 誘導性コンバータ用の別のイネーブル・ピン
- I<sup>2</sup>C互換のシリアル・インターフェイス
- 85μAの静止電流
- 低リップルのパルス周波数変調 (PFM) モード
- サーマル・シャットダウン保護機能

## 2 アプリケーション

- 車載用クラスタ
- 車載インフォテインメント・システム
- デジタル・ラジオ
- Supply DaVinci™ デジタル信号プロセッサ (DSP) ファミリのソリューション

## 3 概要

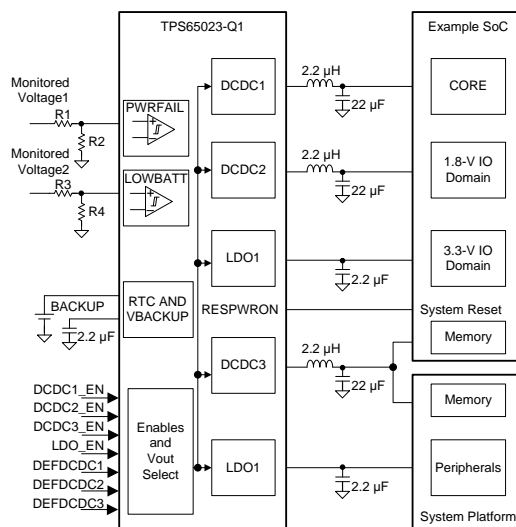
TPS65023-Q1 デバイスは統合された電力管理集積回路 (IC) で、1つのリチウムイオンまたはリチウムポリマー・セルで駆動され、複数の電源レールを必要とするアプリケーション向けです。TPS65023-Q1 デバイスには、プロセッサ・ベースのシステムにおいてコア電圧、ペリフェラル、入出力 (I/O)、およびメモリ・レールを提供するため、3つの高効率な降圧コンバータが搭載されています。コア用コンバータは、シリアル・インターフェイスにより即座に電圧を変更できるため、動的な節電機能をシステムに実装できます。3つの降圧コンバータはすべて、軽負荷時には低消費電力モードへ移行し、可能な限り広い負荷電流の範囲にわたって最大の効率を維持します。

### 製品情報<sup>(1)</sup>

型番	パッケージ	本体サイズ (公称)
TPS65023-Q1	VQFN (40)	6.00mmx6.00mm
	WQFN (40)	5.00mmx5.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

### 概略回路図



## 目次

<b>1</b>	特長 .....	1	8.5	Programming.....	22
<b>2</b>	アプリケーション .....	1	8.6	Register Maps .....	24
<b>3</b>	概要 .....	1	<b>9</b>	<b>Application and Implementation .....</b>	<b>31</b>
<b>4</b>	改訂履歴.....	2	9.1	Application Information.....	31
<b>5</b>	概要 (続き) .....	3	9.2	Typical Application .....	33
<b>6</b>	<b>Pin Configuration and Functions .....</b>	<b>3</b>	<b>10</b>	<b>Power Supply Recommendations .....</b>	<b>37</b>
<b>7</b>	<b>Specifications.....</b>	<b>5</b>	<b>11</b>	<b>Layout.....</b>	<b>38</b>
7.1	Absolute Maximum Ratings .....	5	11.1	Layout Guidelines .....	38
7.2	ESD Ratings.....	5	11.2	Layout Example .....	38
7.3	Recommended Operating Conditions.....	6	<b>12</b>	<b>デバイスおよびドキュメントのサポート .....</b>	<b>39</b>
7.4	Thermal Information .....	6	12.1	デバイス・サポート .....	39
7.5	Electrical Characteristics.....	7	12.2	ドキュメントのサポート .....	39
7.6	Timing Requirements .....	10	12.3	ドキュメントの更新通知を受け取る方法.....	39
7.7	Typical Characteristics .....	11	12.4	コミュニティ・リソース .....	39
<b>8</b>	<b>Detailed Description .....</b>	<b>16</b>	12.5	Trademarks .....	39
8.1	Overview .....	16	12.6	Electrostatic Discharge Caution.....	39
8.2	Functional Block Diagram .....	16	12.7	Glossary .....	39
8.3	Feature Description.....	17	<b>13</b>	<b>メカニカル、パッケージ、および注文情報 .....</b>	<b>39</b>
8.4	Device Functional Modes.....	18			

## 4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision E (March 2016) to Revision F	Page
• データ・シートのタイトル Changed .....	1
• Changed all references of PowerPAD to thermal pad.....	4
• Changed the units of the current and peak current parameters from V to mA in the <i>Absolute Maximum Ratings</i> table .....	5
• Added 「ドキュメントの更新通知を受け取る方法」セクション .....	39

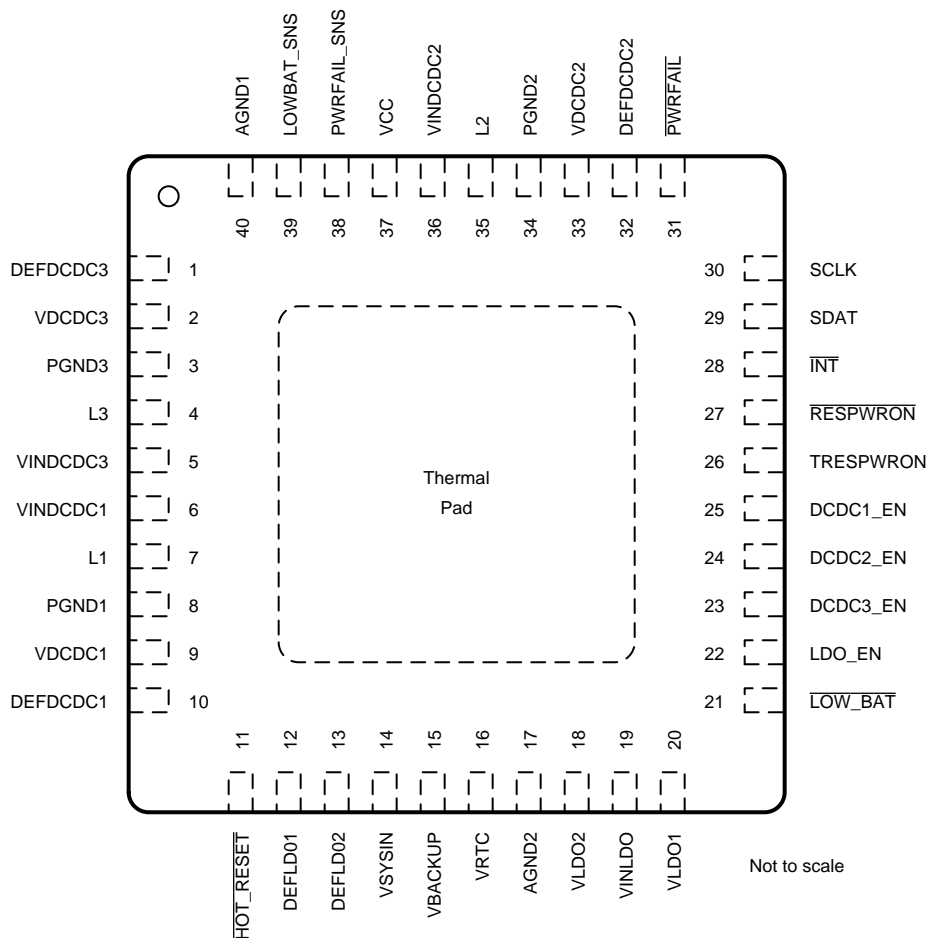
Revision D (September 2011) to Revision E	Page
• 「製品情報」表、「目次」、「改訂履歴」セクション、「ピン構成および機能」セクション、「仕様」セクション、「ESD定格」表、「詳細説明」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクション Added .....	1

## 5 概要 (続き)

また、TPS65023-Q1デバイスには2つの汎用200mA LDO電圧レギュレータも統合されており、外部入力ピンによりイネーブルします。各LDOは1.5V~6.5Vの入力電圧範囲で動作し、降圧コンバータの1つから、またはバッテリーから直接給電可能です。LDOのデフォルト出力電圧は、DEFLDO1およびDEFLDO2ピンを使用して、4種類の電圧の組み合わせにデジタルで設定可能です。シリアル・インターフェイスは動的な電圧スケーリング、割り込みのマスク、またはLDO出力電圧のディセーブル、イネーブル、および設定に使用可能です。このインターフェイスはファースト・モードおよび標準モードのI<sup>2</sup>C仕様と互換性があり、最高400kHzでの転送が可能です。TPS65023-Q1デバイスは、-40°C~125°Cのフリーエア温度範囲で動作します。

## 6 Pin Configuration and Functions

RHA and RSB Packages  
40-Pin VQFN and WQFN  
Top View



**Pin Functions**

PIN		I/O	DESCRIPTION
NAME	NO.		
<b>SWITCHING REGULATOR</b>			
AGND1	40	—	Analog ground. All analog ground pins are connected internally on the chip
AGND2	17	—	Analog ground. All analog ground pins are connected internally on the chip
DCDC1_EN	25	I	VDCDC1 enable pin. A logic high enables the regulator, a logic low disables the regulator
DCDC2_EN	24	I	VDCDC2 enable pin. A logic high enables the regulator, a logic low disables the regulator
DCDC3_EN	23	I	VDCDC3 enable pin. A logic high enables the regulator, a logic low disables the regulator
DEFDCDC1	10	I	Input for signal indicating default VDCDC1 voltage, 0 = 1.2 V, 1 = 1.6 V. DEFDCDC1 can also be connected to a resistor divider between VDCDC1 and GND, if the output voltage of the DCDC1 converter is set in a range from 0.6 V to VINDCDC1 V.
DEFDCDC2	32	I	Input for signal indicating default VDCDC2 voltage, 0 = 1.8 V, 1 = 3.3 V. DEFDCDC2 can also be connected to a resistor divider between VDCDC2 and GND, if the output voltage of the DCDC2 converter is set in a range from 0.6 V to VINDCDC2 V.
DEFDCDC3	1	I	Input for signal indicating default VDCDC3 voltage, 0 = 1.8 V, 1 = 3.3 V. DEFDCDC3 can also be connected to a resistor divider between VDCDC3 and GND, if the output voltage of the DCDC3 converter is set in a range from 0.6 V to VINDCDC3 V.
L1	7	—	Switch pin of VDCDC1 converter. The VDCDC1 inductor is connected here.
L2	35	—	Switch pin of VDCDC2 converter. The VDCDC2 inductor is connected here
L3	4	—	Switch pin of VDCDC3 converter. The VDCDC3 inductor is connected here
PGND1	8	—	Power ground for VDCDC1 converter
PGND2	34	—	Power ground for VDCDC2 converter
PGND3	3	—	Power ground for VDCDC3 converter
VCC	37	I	Power supply for digital and analog circuitry of VDCDC1, VDCDC2, and VDCDC3 DC-DC converters. VCC must be connected to the same voltage supply as VINDCDC3, VINDCDC1, and VINDCDC2. VCC also supplies serial interface block.
VDCDC1	9	I	VDCDC1 feedback voltage sense input. Connect directly to VDCDC1
VDCDC2	33	I	VDCDC2 feedback voltage sense input. Connect directly to VDCDC2
VDCDC3	2	I	VDCDC3 feedback voltage sense input. Connect directly to VDCDC3
VINDCDC1	6	I	Input for VDCDC1 step-down converter. VINDCDC1 must be connected to the same voltage supply as VINDCDC2, VINDCDC3, and VCC
VINDCDC2	36	I	Input for VDCDC2 step-down converter. VINDCDC2 must be connected to the same voltage supply as VINDCDC1, VINDCDC3, and VCC
VINDCDC3	5	I	Input for VDCDC3 step-down converter. VINDCDC3 must be connected to the same voltage supply as VINDCDC1, VINDCDC2, and VCC
Thermal pad	—	—	Connect the thermal pad to analog ground
<b>LDO REGULATOR</b>			
DEFLD01	12	I	Digital input. DEFLD01 sets the default output voltage of LDO1 and LDO2
DEFLD02	13	I	Digital input. DEFLD02 sets the default output voltage of LDO1 and LDO2
LDO_EN	22	I	Enable input for LDO1 and LDO2. A logic high enables the LDOs, a logic low disables the LDOs
VBACKUP	15	I	Connect the backup battery to this input pin
VINLDO	19	I	Input for LDO1 and LDO2
VLDO1	20	O	Output of LDO1
VLDO2	18	O	Output of LDO2
VRTC	16	O	Output of the LDO/switch for the real time clock
VSYSIN	14	I	Input of system voltage for VRTC switch
<b>CONTROL AND I<sup>2</sup>C</b>			
HOT_RESET	11	I	Push-button input that reboots or wakes up the processor through RESPWRON output pin
INT	28	O	Open drain output
LOW_BAT	21	O	Open-drain output of LOW_BAT comparator
LOWBAT_SNS	39	I	Input for the comparator driving the LOW_BAT output
PWRFAIL	31	O	Open-drain output. Active low when PWRFAIL comparator indicates low VBAT condition

### Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
PWRFAIL_SNS	38	I	Input for the comparator driving the $\overline{\text{PWRFAIL}}$ output
$\overline{\text{RESPWRON}}$	27	O	Open-drain system reset output
SCLK	30	I	Serial interface clock line
SDAT	29	I/O	Serial interface data/address
TRESPWRON	26	I	Connect the timing capacitor to TRESPWRON to set the reset delay time: 1 nF → 100 ms.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Input voltage <sup>(2)</sup>	All pins except AGND and PGND	-0.3	7	V
Current	L1, L2, L3, PGND1, PGND2, PGND3, VINDCDC1, VINDCDC2, VINDCDC3		2000	mA
Peak current	All pins except L1, L2, L3, PGND1, PGND2, PGND3, VINDCDC1, VINDCDC2, VINDCDC3		1000	mA
Operating free-air temperature		-40	125	°C
Maximum junction temperature, $T_{J(\text{MAX})}$			150	°C
Storage temperature, $T_{\text{stg}}$		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Voltages are in respect to AGND.

### 7.2 ESD Ratings

		VALUE	UNIT
<b>TPS65023-Q1 IN RHA PACKAGE</b>			
$V_{(\text{ESD})}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per AEC Q100-011	±750
		Machine model (MM)	±50
<b>TPS65023-Q1 IN RSB PACKAGE</b>			
$V_{(\text{ESD})}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per AEC Q100-011	±1000
		Machine model (MM)	±100

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Input voltage range step-down converters	V <sub>CC</sub> , VINDCDC1, VINDCDC2, VINDCDC3	2.5		6	V
V <sub>O</sub>	Output voltage range for VDCDC1 step-down converter <sup>(1)</sup>		0.6		V <sub>CC</sub>	V
	Output voltage range for VDCDC2 step-down converter <sup>(1)</sup>		0.6		V <sub>CC</sub>	
	Output voltage range for VDCDC3 step-down converter <sup>(1)</sup>		0.6		V <sub>CC</sub>	
V <sub>INLDO</sub>	Input voltage range for LDOs	VINLDO1, VINLDO2	1.5		6.5	V
V <sub>O</sub>	Output voltage range for LDOs	VLDO1, VLDO2	1		V <sub>CC</sub>	V
I <sub>O(DCDC1)</sub>	Output current L1				1500	mA
	Inductor at L1 <sup>(2)</sup>		1.5	2.2		
C <sub>I(DCDC1)</sub>	Input capacitor at VINDCDC1 <sup>(2)</sup>		10			μF
C <sub>O(DCDC1)</sub>	Output capacitor at VDCDC1 <sup>(2)</sup>		10	22		μF
I <sub>O(DCDC2)</sub>	Output current at L2				1200	mA
	Inductor at L2 <sup>(2)</sup>		1.5	2.2		
C <sub>I(DCDC2)</sub>	Input capacitor at VINDCDC2 <sup>(2)</sup>		10			μF
C <sub>O(DCDC2)</sub>	Output capacitor at VDCDC2 <sup>(2)</sup>		10	22		μF
I <sub>O(DCDC3)</sub>	Output current at L3				1000	mA
	Inductor at L3 <sup>(2)</sup>		1.5	2.2		
C <sub>I(DCDC3)</sub>	Input capacitor at VINDCDC3 <sup>(2)</sup>		10			μF
C <sub>O(DCDC3)</sub>	Output capacitor at VDCDC3 <sup>(2)</sup>		10	22		μF
C <sub>I(VCC)</sub>	Input capacitor at VCC <sup>(2)</sup>		1			μF
C <sub>I(VINLDO)</sub>	Input capacitor at VINLDO <sup>(2)</sup>		1			μF
C <sub>O(VLDO1-2)</sub>	Output capacitor at VLDO1, VLDO2 <sup>(2)</sup>		2.2			μF
I <sub>O(VLDO1-2)</sub>	Output current at VLDO1, VLDO2				200	mA
C <sub>O(VRTC)</sub>	Output capacitor at VRTC <sup>(2)</sup>		4.7			
T <sub>A</sub>	Operating ambient temperature		−40		125	°C
T <sub>J</sub>	Operating junction temperature		−40		125	°C
	Resistor from VINDCDC3, VINDCDC2, and VINDCDC1 to VCC used for filtering <sup>(3)</sup>			1	10	Ω

(1) When using an external resistor divider at DEFDCDC3, DEFDCDC2, DEFDCDC1

 (2) See [Detailed Design Procedure](#) for more information.

(3) Up to 3 mA can flow into VCC when all three converters are running in PWM. This resistor causes the UVLO threshold to be shifted accordingly.

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	TPS65023-Q1		UNIT
	RHA (VQFN)	RSB (WQFN)	
	40 PINS	40 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance		°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance		°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance		°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter		°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter		°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance		°C/W

 (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

## 7.5 Electrical Characteristics

VINDCDC1 = VINDCDC2 = VINDCDC3 =  $V_{CC}$  =  $V_{INLDO}$  = 3.6 V,  $V_{BACKUP}$  = 3 V,  $T_A$  =  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ , typical values are at  $T_A$  =  $25^{\circ}\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>CONTROL SIGNALS: SCLK, SDAT (INPUT), DCDC1_EN, DCDC2_EN, DCDC3_EN, LDO_EN, DEF LDO1, DEF LDO2</b>						
$V_{IH}$	High-level input voltage	Resistor pullup at SCLK and SDAT = 4.7 k $\Omega$ , pulled to VRTC	1.3		$V_{CC}$	V
$V_{IH}$	High-level input voltage, SDAT	Resistor pullup at SCLK and SDAT = 4.7 k $\Omega$ , pulled to VRTC	1.45		$V_{CC}$	V
$V_{IL}$	Low-level input voltage	Resistor pullup at SCLK and SDAT = 4.7 k $\Omega$ , pulled to VRTC	0		0.4	V
$I_H$	Input bias current			0.01	0.1	$\mu\text{A}$
<b>CONTROL SIGNALS: HOT_RESET</b>						
$V_{IH}$	High-level input voltage		1.3		$V_{CC}$	V
$V_{IL}$	Low-level input voltage		0		0.4	V
$I_{IB}$	Input bias current			0.01	0.1	$\mu\text{A}$
$t_{glitch}$	Deglitch time at HOT_RESET		25	30	35	ms
<b>CONTROL SIGNALS: LOWBAT, PWRFAIL, RESPWRON, INT, SDAT (OUTPUT)</b>						
$V_{OH}$	High-level output voltage				6	V
$V_{OL}$	Low-level output voltage	$I_{IL}$ = 5 mA	0		0.3	V
	Duration of low pulse at RESPWRON	External capacitor 1 nF		100		ms
	Reset power-on threshold	VRTC falling	-3%	2.4	3%	V
		VRTC rising	-3%	2.52	3%	V
<b>SUPPLY PINS: VCC, VINDCDC1, VINDCDC2, VINDCDC3</b>						
$I_{(q)}$	Operating quiescent current, PFM	All three DC-DC converters enabled, zero load, no switching, and LDOs enabled	$V_{CC}$ = 3.6 V, $V_{BACKUP}$ = 3 V, $V_{SYSIN}$ = 0 V	85	100	$\mu\text{A}$
		All three DC-DC converters enabled, zero load, no switching, and LDOs off	$V_{CC}$ = 3.6 V, $V_{BACKUP}$ = 3 V, $V_{SYSIN}$ = 0 V	78	90	
		DCDC1 and DCDC2 converters enabled, zero load, no switching, and LDOs off	$V_{CC}$ = 3.6 V, $V_{BACKUP}$ = 3 V, $V_{SYSIN}$ = 0 V	57	70	
		DCDC1 converter enabled, zero load, no switching, and LDOs off	$V_{CC}$ = 3.6 V, $V_{BACKUP}$ = 3 V, $V_{SYSIN}$ = 0 V	43	55	
$I_I$	Current into VCC, PWM	All three DC-DC converters enabled and running in PWM, LDOs off	$V_{CC}$ = 3.6 V, $V_{BACKUP}$ = 3 V, $V_{SYSIN}$ = 0 V	2	3	mA
		DCDC1 and DCDC2 converters enabled and running in PWM, LDOs off	$V_{CC}$ = 3.6 V, $V_{BACKUP}$ = 3 V, $V_{SYSIN}$ = 0 V	1.5	2.5	
		DCDC1 converter enabled and running in PWM, LDOs off	$V_{CC}$ = 3.6 V, $V_{BACKUP}$ = 3 V, $V_{SYSIN}$ = 0 V	0.85	2	
$I_{(q)}$	Quiescent current	All converters disabled, LDOs off	$V_{CC}$ = 3.6 V, $V_{BACKUP}$ = 3 V, $V_{SYSIN}$ = 0 V	23	33	$\mu\text{A}$
			$V_{CC}$ = 2.6 V, $V_{BACKUP}$ = 3 V, $V_{SYSIN}$ = 0 V	3.5	5	
			$V_{CC}$ = 3.6 V, $V_{BACKUP}$ = 0 V, $V_{SYSIN}$ = 0 V		43	
<b>SUPPLY PINS: VBACKUP, VSYSIN, VRTC</b>						
$I_{(q)}$	Operating quiescent current	$V_{BACKUP}$ = 3 V, $V_{SYSIN}$ = 0 V, $V_{CC}$ = 2.6 V, current into VBACKUP		20	33	$\mu\text{A}$
$I_{(SD)}$	Operating quiescent current	$V_{BACKUP}$ < $V_{\_VBACKUP}$ , current into VBACKUP		2	3	$\mu\text{A}$
	VRTC LDO output voltage	$V_{SYSIN}$ = $V_{BACKUP}$ = 0 V, $I_O$ = 0 mA		3		V
$I_O$	Output current for VRTC	$V_{SYSIN}$ < 2.57 V and $V_{BACKUP}$ < 2.57 V			30	mA
	VRTC short-circuit current limit	$V_{RTC}$ = GND, $V_{SYSIN}$ = $V_{BACKUP}$ = 0 V			100	mA
	Maximum output current at VRTC for RESPWRON = 1	$V_{RTC}$ > 2.6 V, $V_{CC}$ = 3 V, $V_{SYSIN}$ = $V_{BACKUP}$ = 0 V		30		mA
$V_O$	Output voltage accuracy for VRTC	$V_{SYSIN}$ = $V_{BACKUP}$ = 0 V, $I_O$ = 0 mA	-1%		1%	

**Electrical Characteristics (continued)**

VINDCDC1 = VINDCDC2 = VINDCDC3 =  $V_{CC} = V_{INLDO} = 3.6\text{ V}$ ,  $V_{BACKUP} = 3\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ , typical values are at  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Line regulation for VRTC		$V_{CC} = V_{RTC} + 0.5\text{ V}$ to $6.5\text{ V}$ , $I_O = 5\text{ mA}$	-1%		1%	
Load regulation VRTC		$I_O = 1\text{ mA}$ to $30\text{ mA}$ , $V_{SYSIN} = V_{BACKUP} = 0\text{ V}$	-3%		1%	
Regulation time for VRTC		Load change from 10% to 90%		10		$\mu\text{s}$
$I_{lkg}$	Input leakage current at VSYSIN	$V_{SYSIN} < V_{-VSYSIN}$			2	$\mu\text{A}$
	$r_{DS(on)}$ of VSYSIN switch				12.5	$\Omega$
	$r_{DS(on)}$ of VBACKUP switch				12.5	$\Omega$
Input voltage range at VBACKUP <sup>(1)</sup>			2.73		3.75	V
Input voltage range at VSYSIN <sup>(1)</sup>			2.73		3.75	V
	VSYSIN threshold	VSYSIN falling	-3%	2.55	3%	V
	VSYSIN threshold	VSYSIN rising	-3%	2.65	3%	V
	VBACKUP threshold	VBACKUP falling	-3%	2.55	3%	V
	VBACKUP threshold	VBACKUP falling	-3%	2.65	3%	V
<b>SUPPLY PIN: VINLDO</b>						
$I_{(q)}$	Operating quiescent current	Current per LDO into VINLDO		16	30	$\mu\text{A}$
$I_{(SD)}$	Shutdown current	Total current for both LDOs into VINLDO, $V_{INLDO} = 0\text{ V}$		0.1	1	$\mu\text{A}$
<b>VDCDC1 STEP-DOWN CONVERTER</b>						
$I_O$	Maximum output current		1500			mA
$I_{(SD)}$	Shutdown supply current in VINDCDC1	DCDC1_EN = GND		0.1	1	$\mu\text{A}$
	$r_{DS(on)}$ P-channel MOSFET on-resistance	$V_{CC} = V_{(GS)} = 3.6\text{ V}$		125	261	m $\Omega$
	$I_{lkg}$ P-channel leakage current	$V_{CC} = 6\text{ V}$			2	$\mu\text{A}$
	$r_{DS(on)}$ N-channel MOSFET on-resistance	$V_{CC} = V_{(GS)} = 3.6\text{ V}$		130	260	m $\Omega$
	$I_{lkg}$ N-channel leakage current	$V_{(DS)} = 6\text{ V}$		7	10	$\mu\text{A}$
	Forward current limit (P-channel and N-channel)	$2.5\text{ V} < V_{I(MAIN)} < 6\text{ V}$	1.9	2.19	2.6	A
$f_S$	Oscillator frequency		1.95	2.25	2.55	MHz
	Fixed output voltage FPWMDCDC1 = 0	All VDCDC1	$V_{CC} = 2.5\text{ V}$ to $6\text{ V}$ , $0\text{ mA} \leq I_O \leq 1.5\text{ A}$		-2%	2%
			$V_{CC} = 2.5\text{ V}$ to $6\text{ V}$ , $0\text{ mA} \leq I_O \leq 1.5\text{ A}$		-1%	1%
	Adjustable output voltage with resistor divider at DEFDCDC1, FPWMDCDC1 = 0	$V_{CC} = \text{VDCDC1} + 0.3\text{ V}$ (minimum 2.5 V) to $6\text{ V}$ , $0\text{ mA} \leq I_O \leq 1.2\text{ A}$	-2%		2%	
	Adjustable output voltage with resistor divider at DEFDCDC1, FPWMDCDC1 = 1	$V_{CC} = \text{VDCDC1} + 0.3\text{ V}$ (minimum 2.5 V) to $6\text{ V}$ , $0\text{ mA} \leq I_O \leq 1.2\text{ A}$	-1%		1%	
	Line regulation	$V_{CC} = \text{VDCDC1} + 0.3\text{ V}$ (minimum 2.5 V) to $6\text{ V}$ , $I_O = 10\text{ mA}$		0		%/V
	Load regulation	$I_O = 10\text{ mA}$ to $1200\text{ mA}$		0.25		%/A
	Soft-start ramp time	VDCDC1 ramping from 5% to 95% of target value		750		$\mu\text{s}$
	Internal resistance from L1 to GND			1		M $\Omega$
	VDCDC1 discharge resistance	DCDC1 discharge = 1		300		$\Omega$
<b>VDCDC2 STEP-DOWN CONVERTER</b>						
$I_O$	Maximum output current	DEFDCDC2 = GND $V_{CC} = 3.6\text{ V}$ , $3.3\text{ V} - 1\% \leq \text{VDCDC2} \leq 3.3\text{ V} + 1\%$	1200 1000			mA
$I_{(SD)}$	Shutdown supply current in VINDCDC2	DCDC2_EN = GND		0.1	1	$\mu\text{A}$
	$r_{DS(on)}$ P-channel MOSFET on-resistance	$V_{CC} = V_{(GS)} = 3.6\text{ V}$		140	300	m $\Omega$
	$I_{lkg}$ P-channel leakage current	$V_{CC} = 6\text{ V}$			2	$\mu\text{A}$
	$r_{DS(on)}$ N-channel MOSFET on-resistance	$V_{CC} = V_{(GS)} = 3.6\text{ V}$		150	297	m $\Omega$
	$I_{lkg}$ N-channel leakage current	$V_{(DS)} = 6\text{ V}$		7	10	$\mu\text{A}$
	Forward current limit (P-channel and N-channel)	$2.5\text{ V} < V_{CC} < 6\text{ V}$	1.7	1.94	2.2	A
$f_S$	Oscillator frequency		1.95	2.25	2.55	MHz
	Fixed output voltage FPWMDCDC2=0	VDCDC2 = 1.8 V	$V_{CC} = 2.5\text{ V}$ to $6\text{ V}$ , $0\text{ mA} \leq I_O \leq 1.2\text{ A}$		-2%	2%
		VDCDC2 = 3.3 V	$V_{CC} = 3.7\text{ V}$ to $6\text{ V}$ , $0\text{ mA} \leq I_O \leq 1.2\text{ A}$		-1%	1%

(1) Based on the requirements for the Intel PXA270 processor.

**Electrical Characteristics (continued)**

VINDCDC1 = VINDCDC2 = VINDCDC3 =  $V_{CC} = V_{INLDO} = 3.6\text{ V}$ ,  $V_{BACKUP} = 3\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ , typical values are at  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Fixed output voltage FPWMDCDC2=1	VDCDC2 = 1.8 V	$V_{CC} = 2.5\text{ V}$ to $6\text{ V}$ , $0\text{ mA} \leq I_O \leq 1.2\text{ A}$	-2%		2%	
	VDCDC2 = 3.3 V	$V_{CC} = 3.7\text{ V}$ to $6\text{ V}$ , $0\text{ mA} \leq I_O \leq 1.2\text{ A}$	-1%		1%	
Adjustable output voltage with resistor divider at DEFDCDC2 FPWMDCDC2 = 0		$V_{CC} = \text{VDCDC2} + 0.3\text{ V}$ (minimum 2.5 V) to $6\text{ V}$ , $0\text{ mA} \leq I_O \leq 1\text{ A}$	-2%		2%	
Adjustable output voltage with resistor divider at DEFDCDC2, FPWMDCDC2 = 1		$V_{CC} = \text{VDCDC2} + 0.3\text{ V}$ (minimum 2.5 V) to $6\text{ V}$ , $0\text{ mA} \leq I_O \leq 1\text{ A}$	-1%		1%	
Line regulation		$V_{CC} = \text{VDCDC2} + 0.3\text{ V}$ (minimum. 2.5 V) to $6\text{ V}$ , $I_O = 10\text{ mA}$		0		%/V
Load regulation		$I_O = 10\text{ mA}$ to $1000\text{ mA}$		0.25		%/A
Soft-start ramp time		VDCDC2 ramping from 5% to 95% of target value		750		$\mu\text{s}$
Internal resistance from L2 to GND				1		M $\Omega$
VDCDC2 discharge resistance		DCDC2 discharge = 1		300		$\Omega$
<b>VDCDC3 STEP-DOWN CONVERTER</b>						
$I_O$	Maximum output current	DEFDCDC3 = GND		1000		mA
		$V_{CC} = 3.6\text{ V}$ , $3.3\text{ V} - 1\% \leq \text{VDCDC3} \leq 3.3\text{ V} + 1\%$		525		
$I_{(SD)}$	Shutdown supply current in VINDCDC3	DCDC3_EN = GND		0.1	1	$\mu\text{A}$
$r_{DS(on)}$	P-channel MOSFET on-resistance	$V_{CC} = V_{(GS)} = 3.6\text{ V}$		310	698	m $\Omega$
$I_{lk}$	P-channel leakage current	$V_{CC} = 6\text{ V}$		0.1	2	$\mu\text{A}$
$r_{DS(on)}$	N-channel MOSFET on-resistance	$V_{CC} = V_{(GS)} = 3.6\text{ V}$		220	503	m $\Omega$
$I_{lk}$	N-channel leakage current	$V_{(DS)} = 6\text{ V}$		7	10	$\mu\text{A}$
Forward current limit (P-channel and N-channel)		$2.5\text{ V} < V_{CC} < 6\text{ V}$	1.28	1.49	1.69	A
$f_S$	Oscillator frequency		1.95	2.25	2.55	MHz
Fixed output voltage FPWMDCDC3=0	VDCDC3 = 1.8 V	$V_{CC} = 2.5\text{ V}$ to $6\text{ V}$ , $0\text{ mA} \leq I_O \leq 1\text{ A}$	-2%		2%	
	VDCDC3 = 3.3 V	$V_{CC} = 3.6\text{ V}$ to $6\text{ V}$ , $0\text{ mA} \leq I_O \leq 1\text{ A}$	-1%		1%	
Fixed output voltage FPWMDCDC3=1	VDCDC3 = 1.8 V	$V_{CC} = 2.5\text{ V}$ to $6\text{ V}$ , $0\text{ mA} \leq I_O \leq 1\text{ A}$	-2%		2%	
	VDCDC3 = 3.3 V	$V_{CC} = 3.6\text{ V}$ to $6\text{ V}$ , $0\text{ mA} \leq I_O \leq 1\text{ A}$	-1%		1%	
Adjustable output voltage with resistor divider at DEFDCDC3 FPWMDCDC3 = 0		$V_{CC} = \text{VDCDC3} + 0.5\text{ V}$ (minimum 2.5 V) to $6\text{ V}$ , $0\text{ mA} \leq I_O \leq 800\text{ mA}$	-2%		2%	
Adjustable output voltage with resistor divider at DEFDCDC3, FPWMDCDC3 = 1		$V_{CC} = \text{VDCDC3} + 0.5\text{ V}$ (minimum 2.5 V) to $6\text{ V}$ , $0\text{ mA} \leq I_O \leq 800\text{ mA}$	-1%		1%	
Line regulation		$V_{CC} = \text{VDCDC3} + 0.3\text{ V}$ (minimum. 2.5 V) to $6\text{ V}$ , $I_O = 10\text{ mA}$		0		%/V
Load regulation		$I_O = 10\text{ mA}$ to $1000\text{ mA}$		0.25		%/A
Soft-start ramp time		VDCDC3 ramping from 5% to 95% of target value		750		$\mu\text{s}$
Internal resistance from L3 to GND				1		M $\Omega$
VDCDC3 discharge resistance		DCDC3 discharge = 1		300		$\Omega$
<b>VLDO1 AND VLDO2 LOW DROPOUT REGULATORS</b>						
$V_I$	Input voltage range for LDO1, 2		1.5		6.5	V
$V_{O(LD01)}$	LDO1 output voltage range		1		3.15	V
$V_{O(LD02)}$	LDO2 output voltage range		1		3.3	V
$I_O$	Maximum output current for LDO1, LDO2	$V_{CC} = 1.8\text{ V}$ , $V_O = 1.3\text{ V}$		200		mA
		$V_{CC} = 1.5\text{ V}$ , $V_O = 1.3\text{ V}$		120		
$I_{(SC)}$	LDO1 and LDO2 short circuit current limit	$V_{(LD01)} = \text{GND}$ , $V_{(LD02)} = \text{GND}$			400	mA
	Minimum voltage drop at LDO1, LDO2	$I_O = 50\text{ mA}$ , $V_{INLDO} = 1.8\text{ V}$			120	mV
		$I_O = 50\text{ mA}$ , $V_{INLDO} = 1.5\text{ V}$		65	150	
		$I_O = 200\text{ mA}$ , $V_{INLDO} = 1.8\text{ V}$			300	
Output voltage accuracy for LDO1, LDO2		$I_O = 10\text{ mA}$	-2%		1%	
Line regulation for LDO1, LDO2		$V_{INLDO} = \text{VLDO1,2} + 0.5\text{ V}$ (minimum 2.5 V) to $6.5\text{ V}$ , $I_O = 10\text{ mA}$	-1%		1%	
Load regulation for LDO1, LDO2		$I_O = 0\text{ mA}$ to $50\text{ mA}$	-1%		1%	
Regulation time for LDO1, LDO2		Load change from 10% to 90%		10		$\mu\text{s}$

### Electrical Characteristics (continued)

VINDCDC1 = VINDCDC2 = VINDCDC3 = V<sub>CC</sub> = V<sub>INLDO</sub> = 3.6 V, V<sub>BACKUP</sub> = 3 V, T<sub>A</sub> = -40°C to 125°C, typical values are at T<sub>A</sub> = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>ANALOG SIGNALS DEFDCDC1, DEFDCDC2, DEFDCDC3</b>						
V <sub>IH</sub>	High-level input voltage <sup>(2)</sup>		1.3		V <sub>CC</sub>	V
V <sub>IL</sub>	Low-level input voltage		0		0.1	V
	Input bias current			0.001	0.05	μA
<b>THERMAL SHUTDOWN</b>						
T <sub>(SD)</sub>	Thermal shutdown	Increasing junction temperature		160		°C
	Thermal shutdown hysteresis	Decreasing junction temperature		20		°C
<b>INTERNAL UNDERVOLTAGE LOCK OUT</b>						
UVLO	Internal UVLO	VCC falling	-2%	2.35	2%	V
V <sub>UVLO_HYST</sub>	Internal UVLO comparator hysteresis			120		mV
<b>VOLTAGE DETECTOR COMPARATORS</b>						
	Comparator threshold (PWRFAIL_SNS, LOWBAT_SNS)	Falling threshold	-2%	1	2%	V
	Hysteresis		40	50	60	mV
	Propagation delay	25-mV overdrive			10	μs
<b>POWER GOOD</b>						
V <sub>PGOODF</sub>		VDCDC1, VDCDC2, VDCDC3, VLDO1, VLDO2, decreasing	-12%	-10%	-8%	
V <sub>PGOODR</sub>		VDCDC1, VDCDC2, VDCDC3, VLDO1, VLDO2, increasing	-7%	-5%	-3%	

(2) The input voltage can go as high as 6 V. If the input voltage exceeds V<sub>CC</sub>, an input current of (V<sub>(PB\_IN)</sub> - 0.7 V - V<sub>CC</sub>) / 10 kΩ flows.

### 7.6 Timing Requirements

		MIN	MAX	UNIT
f <sub>MAX</sub>	Clock frequency		400	kHz
t <sub>wH(HIGH)</sub>	Clock high time	600		ns
t <sub>wL(LOW)</sub>	Clock low time	1300		ns
t <sub>r</sub>	DATA and CLK rise time		300	ns
t <sub>f</sub>	DATA and CLK fall time		300	ns
t <sub>h(STA)</sub>	Hold time (repeated) START condition (after this period the first clock pulse is generated)	600		ns
t <sub>h(DATA)</sub>	Setup time for repeated START condition	600		ns
t <sub>h(DATA)</sub>	Data input hold time	300		ns
t <sub>su(DATA)</sub>	Data input setup time	300		ns
t <sub>su(STO)</sub>	STOP condition setup time	600		ns
t <sub>(BUF)</sub>	Bus free time	1300		ns

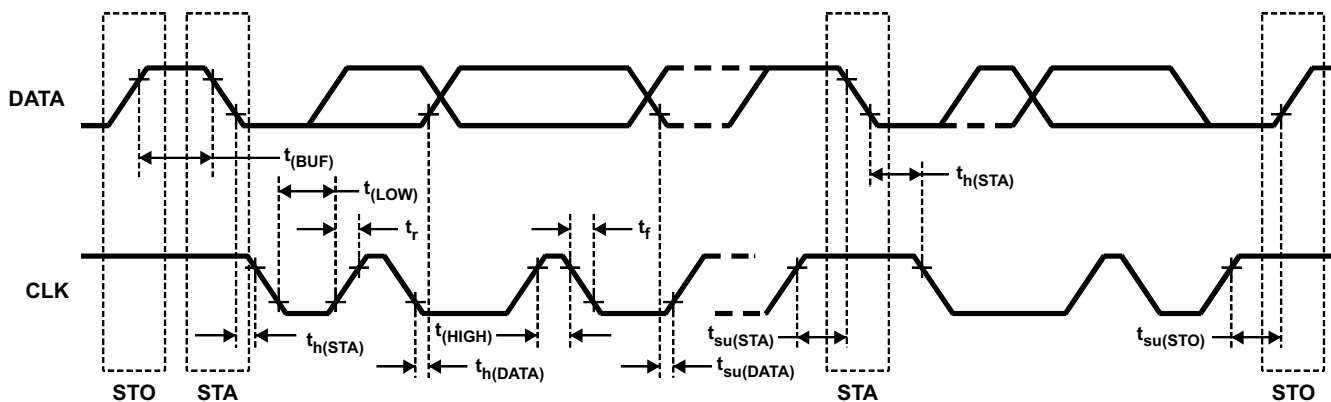


Figure 1. Serial Interface Timing Diagram

## 7.7 Typical Characteristics

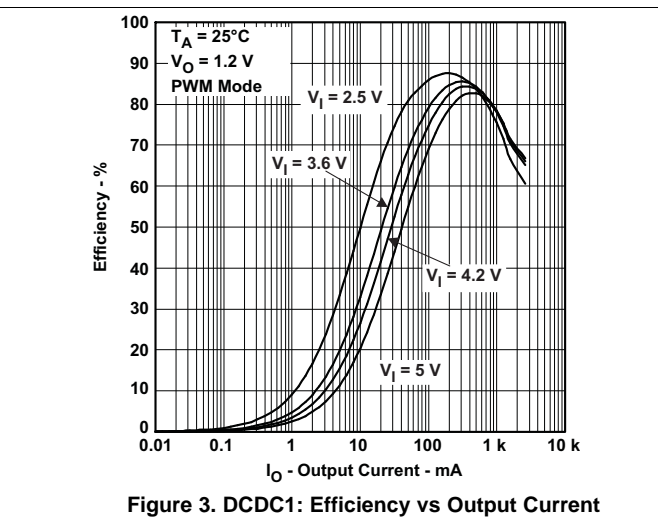
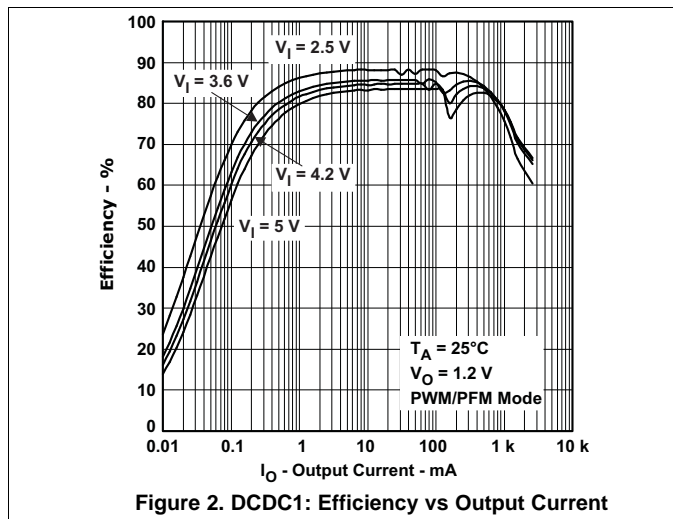
**Table 1. EVM Parameters for Typical Characteristics Measurement<sup>(1)</sup>**

CONVERTER	INDUCTOR	OUTPUT CAPACITOR	OUTPUT CAPACITOR VALUE
VDCDC1	VLCF4020-2R2	C2012X5R0J106M	2 × 10 μF
VDCDC2	VLCF4020-2R2	C2012X5R0J106M	2 × 10 μF
VDCDC3	VLF4012AT-2R2M1R5	C2012X5R0J106M	2 × 10 μF

(1) Graphs were taken using the evaluation module (EVM), TPS65023EVM-205, with the inductor and output capacitor combinations in Table 1. See [TPS65023EVM, User's Guide](#) for more information.

**Table 2. Table Of Graphs**

		FIGURE
Efficiency	vs Output current	Figure 2, Figure 3, Figure 4, Figure 5, Figure 6, Figure 7
Output voltage	vs Output current at 85°C	Figure 8, Figure 9
Line transient response		Figure 10, Figure 11, Figure 12
Load transient response		Figure 13, Figure 14, Figure 15
VDCDC2 PFM operation		Figure 16
VDCDC2 low ripple PFM operation		Figure 17
VDCDC2 PWM operation		Figure 18
Startup VDCDC1, VDCDC2 and VDCDC3		Figure 19
Startup LDO1 and LDO2		Figure 20
Line transient response		Figure 21, Figure 22, Figure 23
Load transient response		Figure 24, Figure 25, Figure 26



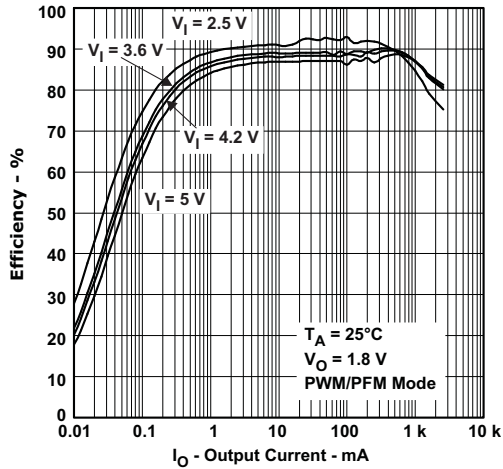


Figure 4. DCDC2: Efficiency vs Output Current

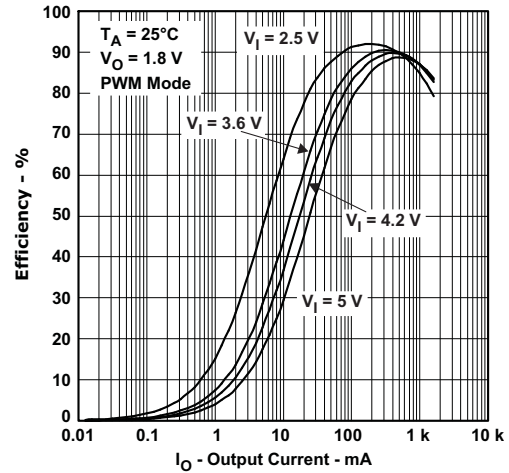


Figure 5. DCDC2: Efficiency vs Output Current

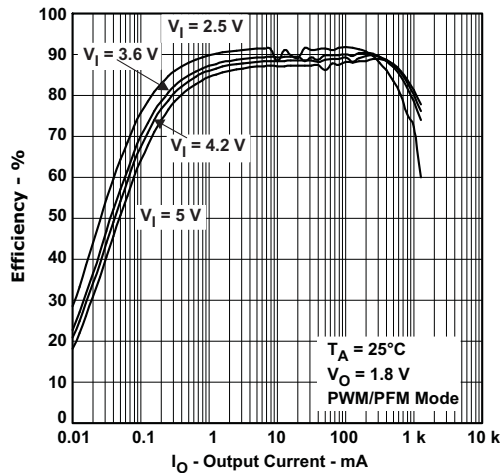


Figure 6. DCDC3: Efficiency vs Output Current

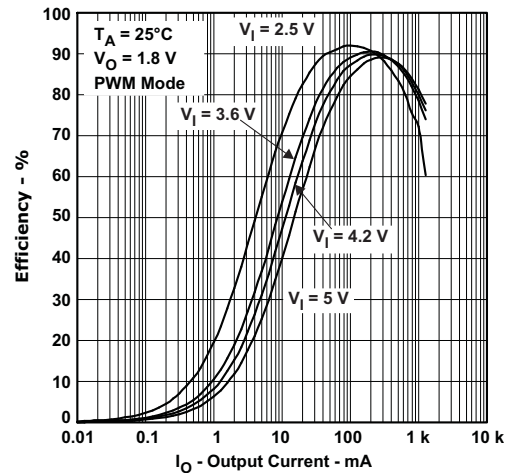


Figure 7. DCDC3: Efficiency vs Output Current

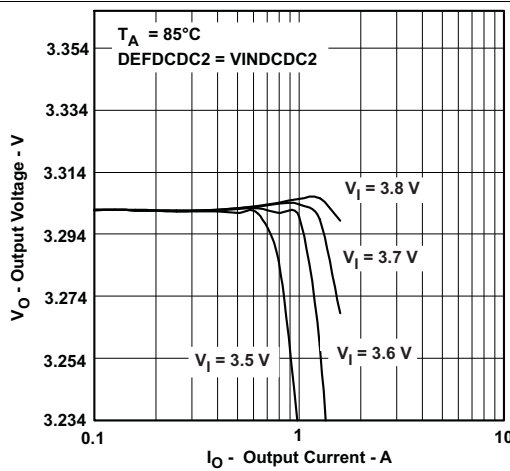


Figure 8. DCDC2: Output Voltage vs Output Current At 85°C

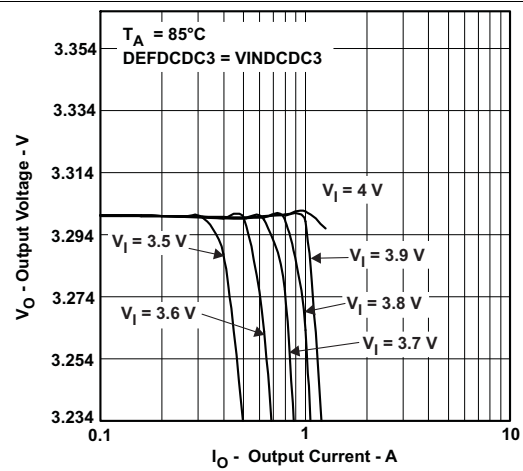


Figure 9. DCDC3: Output Voltage vs Output Current At 85°C

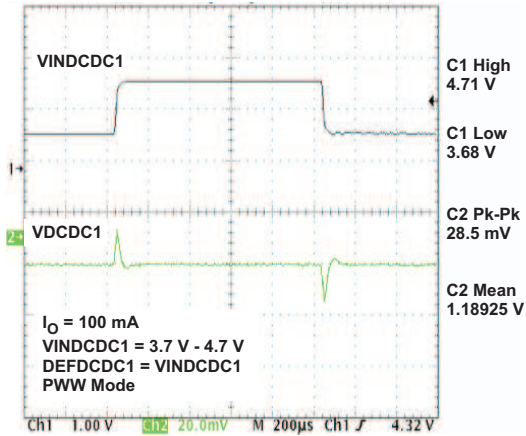


Figure 10. VDCDC1 Line Transient Response

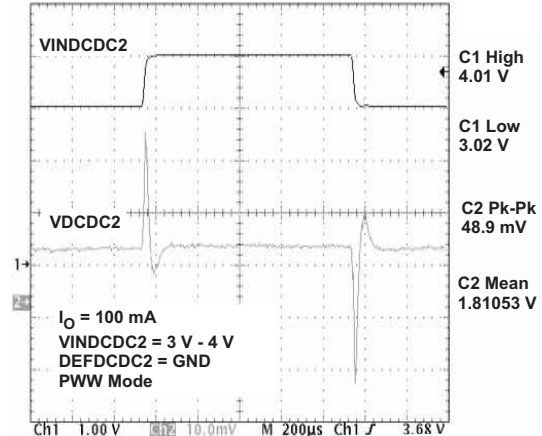


Figure 11. VDCDC2 Line Transient Response

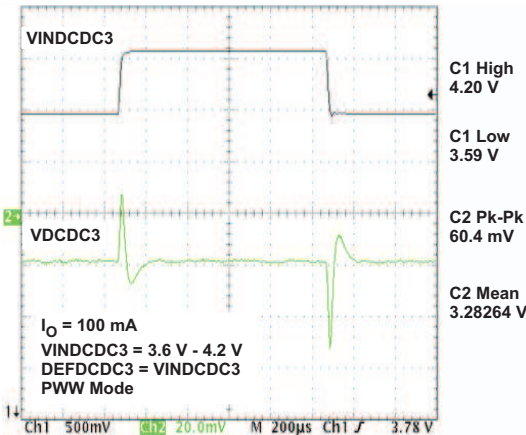


Figure 12. VDCDC3 Line Transient Response

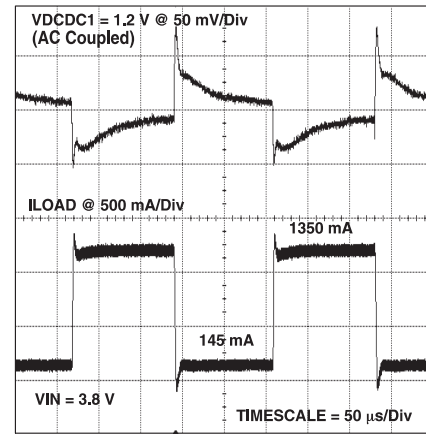


Figure 13. VDCDC1 Load Transient Response

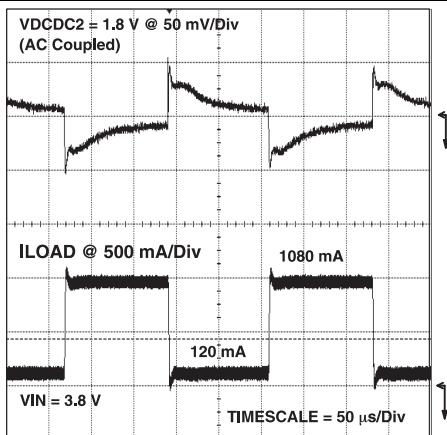


Figure 14. VDCDC2 Load Transient Response

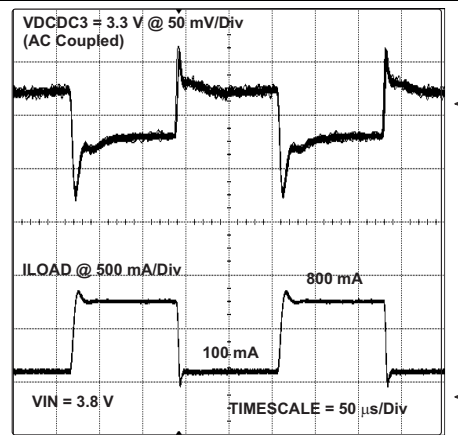


Figure 15. VDCDC3 Load Transient Response

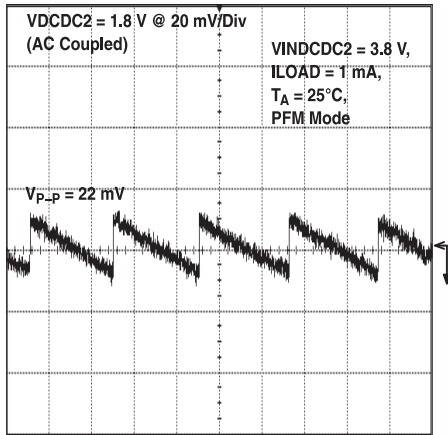


Figure 16. VDCDC2 Output Voltage Ripple

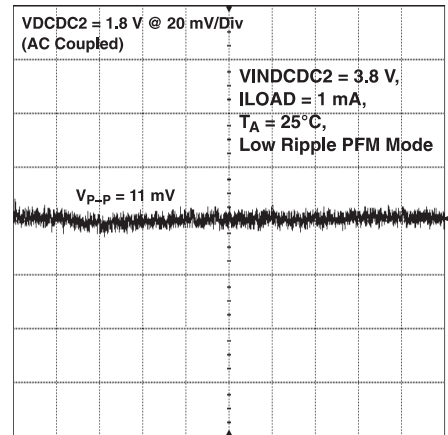


Figure 17. VDCDC2 Output Voltage Ripple

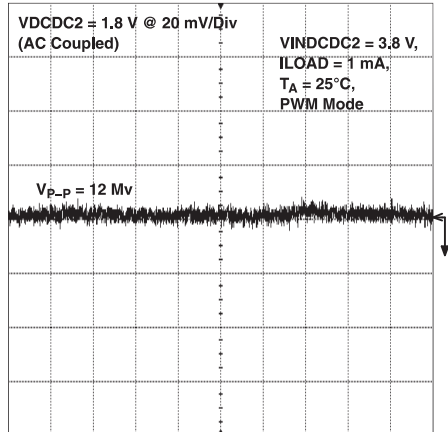


Figure 18. VDCDC2 Output Voltage Ripple

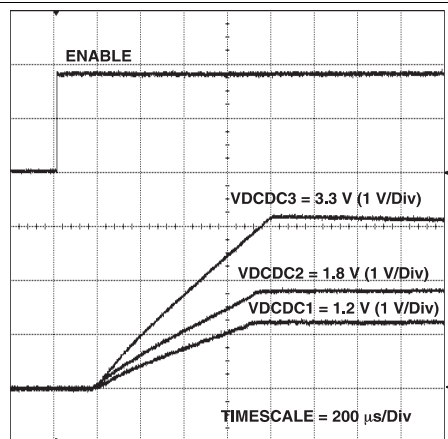


Figure 19. Startup VDCDC1, VDCDC2, and VDCDC3

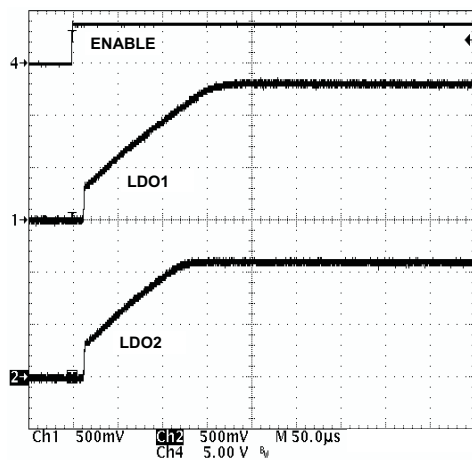


Figure 20. Startup LDO1 and LDO2

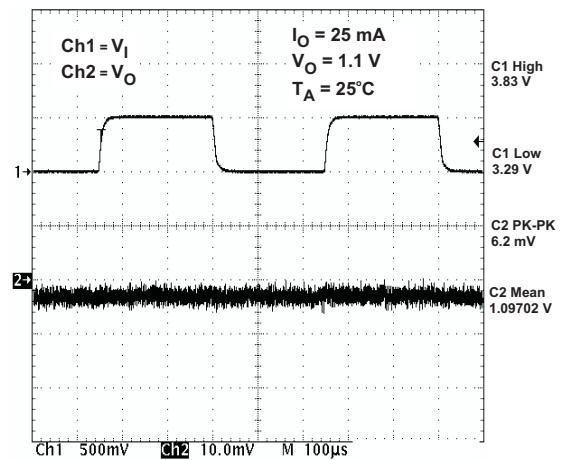


Figure 21. LDO1 Line Transient Response

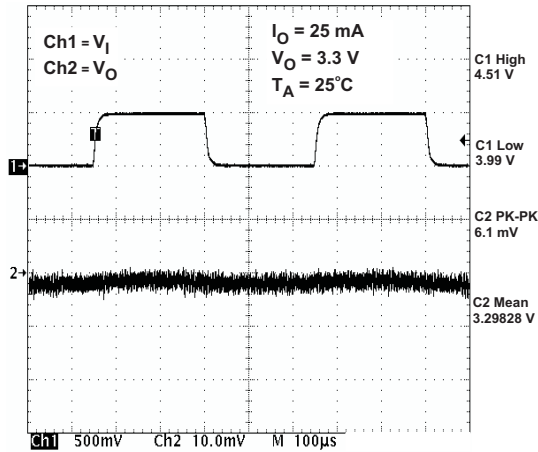


Figure 22. LDO2 Line Transient Response

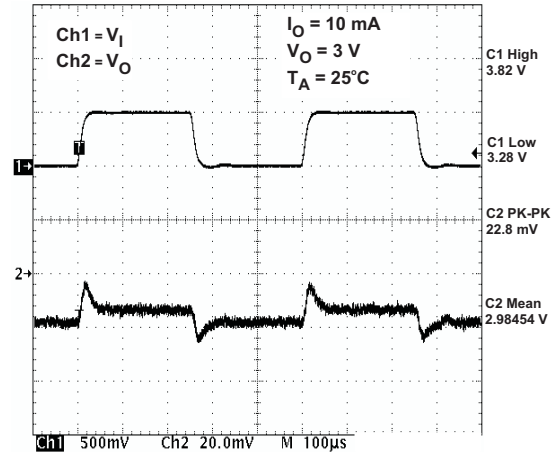


Figure 23. VRTC Line Transient Response

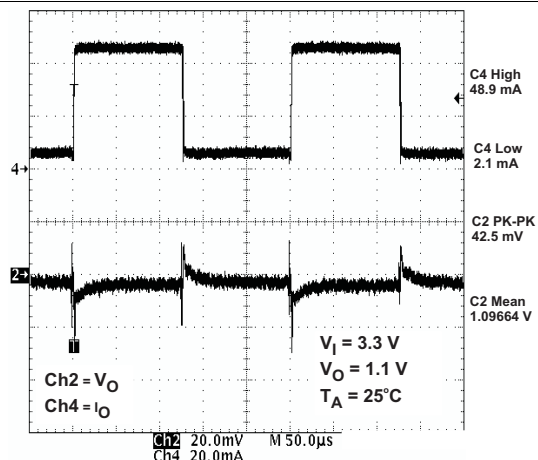


Figure 24. LDO1 Load Transient Response

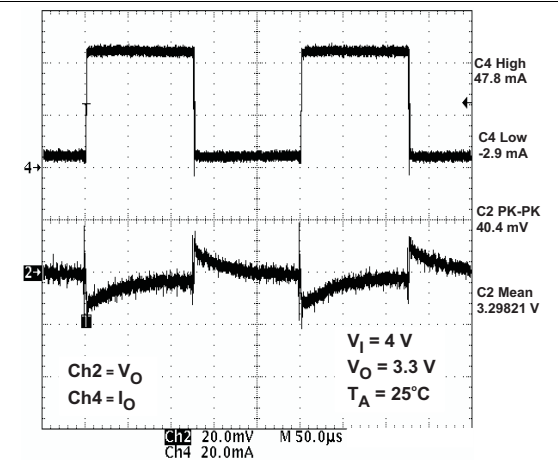


Figure 25. LDO2 Load Transient Response

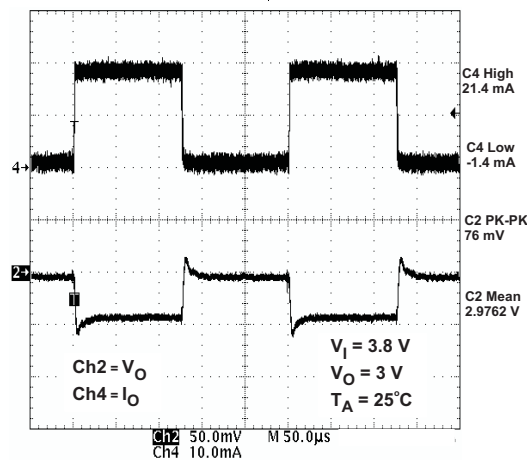


Figure 26. VRTC Load Transient Response

## 8 Detailed Description

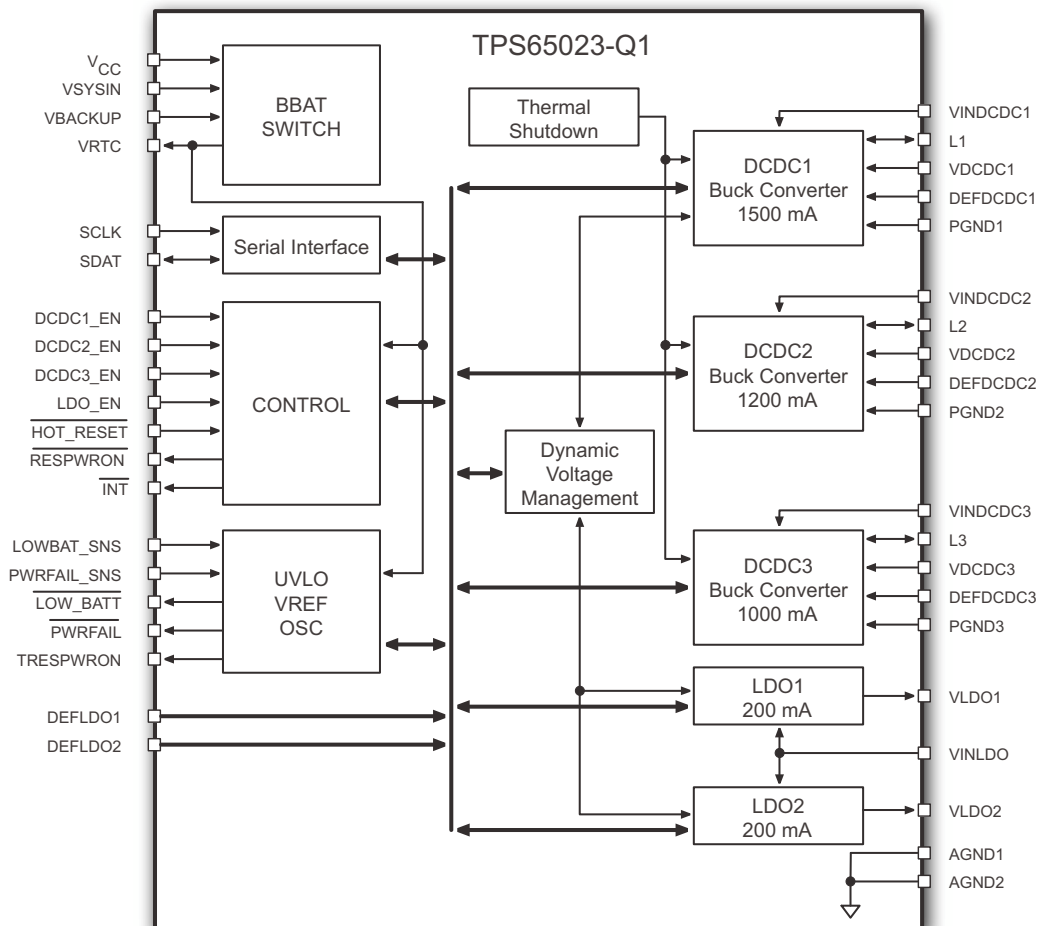
### 8.1 Overview

The TPS65023-Q1 device has 5 regulator channels, 3 DCDCs, and 2 LDOs. DCDC3 has dynamic voltage scaling feature (DVS) that allows for power reduction to CORE supplies during idle operation or overvoltage during heavy-duty operation. With DVS and 2 more DCDCs plus 2 LDOs, the TPS65023-Q1 is ideal for CORE, Memory, IO, and peripheral power for the entire system of a wide range of suitable applications.

The device incorporates enables for the DCDCs and LDOs, I<sup>2</sup>C for device control, push button, and a reset interface that complete the system and allow the TPS65023-Q1 to be adapted for different kinds of processors or FPGAs.

For noise-sensitive circuits, the DCDCs can be synchronized out of phase from one another, reducing the peak noise at the switching frequency. Each converter can be forced to operate in PWM mode to ensure constant switching frequency across the entire load range. However, for low load efficiency performance the DCDCs automatically enter PSM mode which reduces the switching frequency when the load current is low, saving power at idle operation.

### 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Step-Down Converters, VDCDC1, VDCDC2, and VDCDC3

The TPS65023-Q1 incorporates three synchronous step-down converters operating typically at 2.25 MHz fixed-frequency pulse-width modulation (PWM) at moderate to heavy load currents. At light load currents, the converters automatically enter the power-save mode (PSM), and operate with pulse-frequency modulation (PFM). The VDCDC1 converter is capable of delivering 1.5-A output current, the VDCDC2 converter is capable of delivering 1.2 A, and the VDCDC3 converter is capable of delivering up to 1 A.

The converter output voltages can be programmed through the DEFDCDC1, DEFDCDC2, and DEFDCDC3 pins. The pins can either be connected to GND, VCC, or to a resistor divider between the output voltage and GND. The VDCDC1 converter defaults to 1.2 V or 1.6 V, depending on the DEFDCDC1 configuration pin. If DEFDCDC1 is tied to ground, the default is 1.2 V. If it is tied to VCC, the default is 1.6 V. When the DEFDCDC1 pin is connected to a resistor divider, the output voltage can be set in the range of 0.6 V to  $V_{CC}$ . See [Application and Implementation](#) for more details. The core voltage can be reprogrammed through the serial interface in the range of 0.8 V to 1.6 V with a programmable slew rate. The converter is forced into PWM operation while any programmed voltage change is underway, whether the voltage is being increased or decreased. The DEFDCDC1 and DEFDCDC2 registers are used to program the output voltage and slew rate during voltage transitions.

The VDCDC2 converter defaults to 1.8 V or 3.3 V, depending on the DEFDCDC2 configuration pin. If DEFDCDC2 is tied to ground, the default is 1.8 V. If it is tied to VCC, the default is 3.3 V. When the DEFDCDC2 pin is connected to a resistor divider, the output voltage can be set in the range of 0.6 V to  $V_{CC}$ .

The VDCDC3 converter defaults to 1.8 V or 3.3 V, depending on the DEFDCDC3 configuration pin. If DEFDCDC3 is tied to ground, the default is 1.8 V. If it is tied to VCC, the default is 3.3 V. When the DEFDCDC3 pin is connected to a resistor divider, the output voltage can be set in the range of 0.6 V to  $V_{CC}$ .

The step-down converter outputs (when enabled) are monitored by power good (PG) comparators, the outputs of which are available through the serial interface. The outputs of the DC-DC converters can be optionally discharged through on-chip 300- $\Omega$  resistors when the DC-DC converters are disabled.

During PWM operation, the converters use a unique fast-response voltage-mode controller scheme with input-voltage feed-forward to achieve good line and load regulation, allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the P-channel MOSFET switch is turned on. The inductor current ramps up until the comparator trips and the control logic turns off the switch. The current-limit comparator also turns off the switch if the current limit of the P-channel switch is exceeded. After the adaptive dead time used to prevent shoot-through current, the N-channel MOSFET rectifier is turned on, and the inductor current ramps down. The next cycle is initiated by the clock signal, again turning off the N-channel rectifier and turning on the P-channel switch.

The three DC-DC converters operate synchronized to each other with the VDCDC1 converter as the master. A 180° phase shift between the VDCDC1 switch turnon and the VDCDC2 and a further 90° shift to the VDCDC3 switch turnon decreases the input rms current, and smaller input capacitors can be used. This is optimized for a typical application where the VDCDC1 converter regulates a Li-Ion battery voltage of 3.7 V to 1.2 V, the VDCDC2 converter from 3.7 V to 1.8 V, and the VDCDC3 converter from 3.7 V to 3.3 V. The phase of the three converters can be changed using the CON\_CTRL register.

### 8.3.2 Soft Start

Each of the three converters has an internal soft-start circuit that limits the inrush current during start-up. The soft start is realized by using a low initial current to charge the internal compensation capacitor. The soft-start time is typically 750  $\mu$ s if the output voltage ramps from 5% to 95% of the final target value. If the output is already precharged to some voltage when the converter is enabled, then this time is reduced proportionally. There is a short delay of typically 170  $\mu$ s between the converter being enabled and switching activity actually starting. This allows the converter to bias itself properly, to recognize if the output is precharged, and if so to prevent discharging of the output while the internal soft-start ramp catches up with the output voltage.

## Feature Description (continued)

### 8.3.3 Active Discharge When Disabled

When the VDCDC1, VDCDC2, and VDCDC3 converters are disabled, due to an UVLO, DCDC\_EN or OVERTEMP condition, it is possible to pull down the outputs actively. This feature is disabled per default and is individually enabled through the CON\_CTRL2 register in the serial interface. When this feature is enabled, the VDCDC1, VDCDC2, and VDCDC3 outputs are discharged by a 300- $\Omega$  (typical) load which is active as long as the converters are disabled.

### 8.3.4 Power-Good Monitoring

All three step-down converters and both the LDO1 and LDO2 linear regulators have power-good comparators. Each comparator indicates when the relevant output voltage has dropped 10% below its target value with 5% hysteresis. The outputs of these comparators are available in the PGOODZ register through the serial interface. An interrupt is generated when any voltage rail drops below the 10% threshold. The comparators are disabled when the converters are disabled and the relevant PGOODZ register bits indicate that power is good.

### 8.3.5 Low-Dropout Voltage Regulators

The low-dropout voltage regulators are designed to operate well with low-value ceramic input and output capacitors. They operate with input voltages down to 1.5 V. The LDOs offer a maximum dropout voltage of 300 mV at rated output current. Each LDO supports a current-limit feature. Both LDOs are enabled by the LDO\_EN pin, and both LDOs can be disabled or programmed through the serial interface using the REG\_CTRL and LDO\_CTRL registers. The LDOs also have reverse-conduction prevention. This allows the possibility to connect external regulators in parallel in systems with a backup battery. The TPS65023-Q1 step-down and LDO voltage regulators automatically power down when the  $V_{CC}$  voltage drops below the UVLO threshold or when the junction temperature rises above 160°C.

### 8.3.6 Undervoltage Lockout

The undervoltage-lockout circuit for the five regulators on the TPS65023-Q1 prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery. It disables the converters and LDOs. The UVLO circuit monitors the VCC pin, the threshold is set internally to 2.35 V with 5% (120 mV) hysteresis. Note that when any of the DC-DC converters are running, there is an input current at the VCC pin, which is up to 3 mA when all three converters are running in PWM mode. This current must be considered if an external RC filter is used at the VCC pin to remove switching noise from the TPS65023-Q1 internal analog circuitry supply.

## 8.4 Device Functional Modes

### 8.4.1 VRTC Output and Operation With or Without Backup Battery

The VRTC pin is an always-on output, intended to supply up to 30 mA to a permanently required rail (that is, for a real-time clock). The TPS65023-Q1 asserts the  $\overline{\text{RESPWRON}}$  signal if VRTC drops below 2.4 V. VRTC is selected from a priority scheme based on the VSYSIN and VBACKUP inputs.

When the voltage at the VSYSIN pin exceeds 2.65 V, VRTC connects to the VSYSIN input through a PMOS switch and all other paths to VRTC are disabled. The PMOS switch drops a maximum of 375 mV at 30 mA, which should be considered when using VRTC. VSYSIN can be connected to any voltage source with the appropriate input voltage, including VCC or, if set to 3.3-V output, DCDC2 or DCDC3. When VSYSIN falls below 2.65 V or shorts to ground, the PMOS switch connecting VRTC and VSYSIN opens and VRTC then connects to either VBACKUP or the output of a dedicated 3-V, 30-mA LDO. TI recommends connecting VSYSIN to VCC or ground—VCC if a non-replaceable primary cell is connected to VBACKUP and ground if the VRTC output floats.

If the PMOS switch between VSYSIN and VRTC is open and VBACKUP exceeds 2.65 V, VRTC connects to VBACKUP through a PMOS switch. The PMOS switch drops a maximum of 375 mV at 30 mA, which should be considered if using VRTC. A typical application may connect VBACKUP to a primary Li button cell, but any battery that provides a voltage between 2.65 V and 6 V (that is, a single Li-Ion cell or a single boosted NiMH battery) is acceptable, to supply the VRTC output. *In systems with no backup battery, the VBACKUP pin should be connected to GND.*

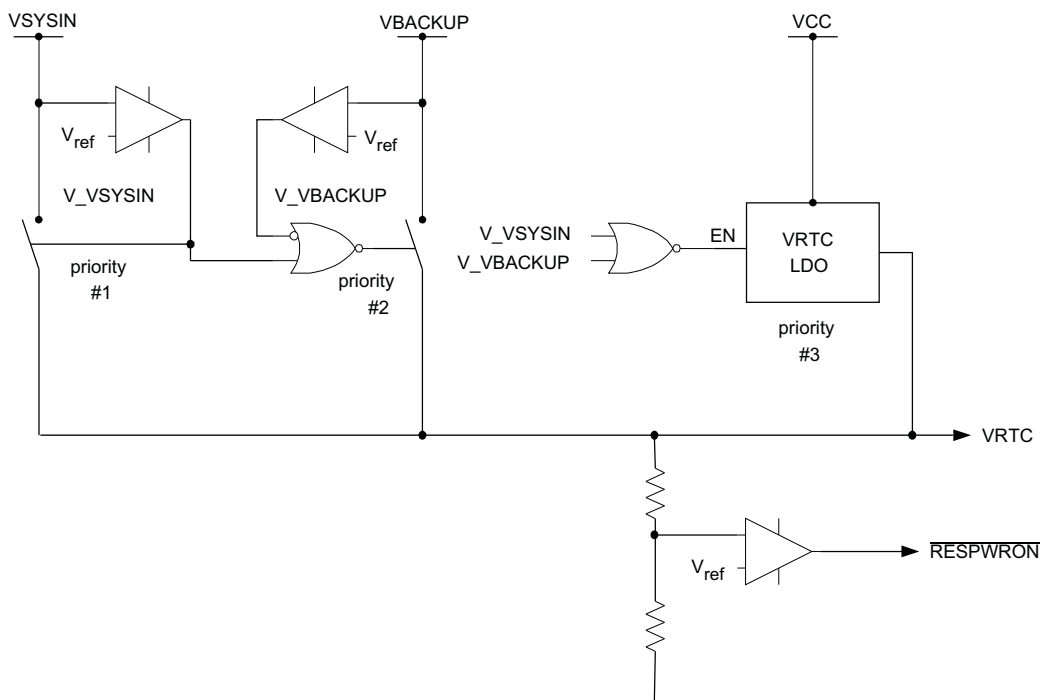
If the switches between VRTC and VSYSIN or VBACKUP are open, the dedicated 3-V, 30-mA LDO, driven from VCC, connects to VRTC. This LDO is disabled if the voltage at the VSYSIN input exceeds 2.65 V.

### Device Functional Modes (continued)

Inside TPS65023-Q1 there is a switch ( $V_{MAX}$  switch) which selects the higher voltage between  $V_{CC}$  and  $V_{BACKUP}$ . This is used as the supply voltage for some basic functions. The functions powered from the output of the  $V_{MAX}$  switch are:

- $\overline{INT}$  output
- $\overline{RESPWRON}$  output
- $\overline{HOT\_RESET}$  input
- $\overline{LOW\_BAT}$  output
- $\overline{PWRFAIL}$  output
- Enable pins for DC-DC converters, LDO1 and LDO2
- Undervoltage lockout comparator (UVLO)
- Reference system with low-frequency timing oscillators
- $\overline{LOW\_BAT}$  and  $\overline{PWRFAIL}$  comparators

The main 2.25-MHz oscillator, and the I<sup>2</sup>C interface are only powered from VCC.



- A.  $V_{VSYSIN}$ ,  $V_{VBACKUP}$  thresholds: falling = 2.55 V, rising = 2.65 V  $\pm 3\%$   
 B.  $\overline{RESPWRON}$  thresholds: falling = 2.4 V, rising = 2.52 V  $\pm 3\%$

**Figure 27. Power Switches Block Diagram**

## Device Functional Modes (continued)

### 8.4.2 Power-Save Mode Operation (PSM)

As the load current decreases, the converters enter the power-save mode of operation. During PSM, the converters operate in a burst mode (PFM mode) with a frequency between 750 kHz and 2.25 MHz, nominal, for one burst cycle. However, the frequency between different burst cycles depends on the actual load current and is typically far less than the switching frequency, with a minimum quiescent current to maintain high efficiency.

To optimize the converter efficiency at light load, the average current is monitored, and if in PWM mode the inductor current remains below a certain threshold, then PSM is entered. The typical threshold to enter PSM is calculated as follows:

$$\begin{aligned}
 I_{\text{PFMDCDC1 enter}} &= \frac{V_{\text{INDCDC1}}}{24 \, \Omega} \\
 I_{\text{PFMDCDC2 enter}} &= \frac{V_{\text{INDCDC2}}}{26 \, \Omega} \\
 I_{\text{PFMDCDC3 enter}} &= \frac{V_{\text{INDCDC3}}}{39 \, \Omega}
 \end{aligned} \tag{1}$$

During PSM, the output voltage is monitored with a comparator, and by maximum skip burst duration. As the output voltage falls below the threshold, set to the nominal  $V_O$ , the P-channel switch turns on, and the converter effectively delivers a constant current defined as follows.

$$\begin{aligned}
 I_{\text{PFMDCDC1 leave}} &= \frac{V_{\text{INDCDC1}}}{18 \, \Omega} \\
 I_{\text{PFMDCDC2 leave}} &= \frac{V_{\text{INDCDC2}}}{20 \, \Omega} \\
 I_{\text{PFMDCDC3 leave}} &= \frac{V_{\text{INDCDC3}}}{29 \, \Omega}
 \end{aligned} \tag{2}$$

If the load is below the delivered current, then the output voltage rises until the same threshold is crossed in the other direction. All switching activity ceases, reducing the quiescent current to a minimum until the output voltage has again dropped below the threshold. The power-save mode is exited, and the converter returns to PWM mode if either of the following conditions is met:

- the output voltage drops 2% below the nominal  $V_O$  due to increasing load current
- the PFM burst time exceeds  $16 \times 1 / f_S$  (7.11  $\mu\text{s}$  typical).

These control methods reduce the quiescent current to typically 14  $\mu\text{A}$  per converter, and the switching activity to a minimum, thus achieving the highest converter efficiency. Setting the comparator thresholds at the nominal output voltage at light load current results in a low output-voltage ripple. The ripple depends on the comparator delay and the size of the output capacitor. Increasing capacitor values makes the output ripple tend to zero. The PSM is disabled through the I<sup>2</sup>C interface to force the individual converters to stay in fixed-frequency PWM mode.

### 8.4.3 Low-Ripple Mode

Setting bit 3 in register CON-CTRL to 1 enables the low-ripple mode for all of the DC-DC converters if operated in PFM mode. For an output current less than approximately 10 mA, the output-voltage ripple in PFM mode is reduced, depending on the actual load current. The lower the actual output current on the converter, the lower the output ripple voltage. For an output current above 10 mA, there is only a minor difference in output-voltage ripple between PFM mode and low-ripple PFM mode. As this feature also increases switching frequency, it is used to keep the switching frequency above the audible range in PFM mode down to a low output current.

## Device Functional Modes (continued)

### 8.4.4 100% Duty-Cycle Low-Dropout Operation

The TPS65023-Q1 converters offer a low input-to-output voltage difference while still maintaining operation with the use of the 100% duty-cycle mode. In this mode, the P-channel switch is constantly turned on. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage required to maintain DC regulation depends on the load current and output voltage. Use Equation 3 to calculate the minimum input voltage.

$$V_{IN(min)} = V_{OUT(min)} + I_{OUT(max)} \times (r_{DS(ON)max} + R_L)$$

where

- $I_{OUT(max)}$  = maximum load current (Note: ripple current in the inductor is zero under these conditions)
  - $r_{DS(ON)max}$  = maximum P-channel switch  $r_{DS(on)}$
  - $R_L$  = DC resistance of the inductor
  - $V_{OUT(min)}$  = nominal output voltage minus 2% tolerance limit
- (3)

### 8.4.5 System Reset and Control Signals

The  $\overline{RESPWRON}$  signal can be used as a global reset for the application. It is an open-drain output. The  $\overline{RESPWRON}$  signal is generated according to the power-good comparator of VRTC, and remains low for  $t_{nrespwron}$  seconds after VRTC has risen above 2.52 V (falling threshold is 2.4 V, 5% hysteresis).  $t_{nrespwron}$  is set by an external capacitor at the TRESPWRON pin. 1 nF gives typically 100 ms.  $\overline{RESPWRON}$  is also triggered by the  $\overline{HOT\_RESET}$  input. This input is internally debounced, with a filter time of typically 30 ms.

The  $\overline{PWRFAIL}$  and  $\overline{LOW\_BAT}$  signals are generated by two voltage detectors using the PWRFAIL\_SNS and LOWBAT\_SNS input signals. Each input signal is compared to a 1-V threshold (falling edge) with 5% (50 mV) hysteresis.

The DCDC1 converter is reset to its default output voltage defined by the DEFDCDC1 input, when  $\overline{HOT\_RESET}$  is asserted. Other I<sup>2</sup>C registers are not affected. Generally, the DCDC1 converter is set to its default voltage with one of these conditions:  $\overline{HOT\_RESET}$  active, VRTC lower than its threshold voltage, undervoltage lockout (UVLO) condition, or  $\overline{RESPWRON}$  active.

#### 8.4.5.1 DEFLD01 and DEFLD02

These two pins are used to set the default output voltage of the two 200-mA LDOs. The digital value applied to the pins is latched during power up and determines the initial output voltage according to Table 3. The voltage of both LDOs can be changed during operation with the I<sup>2</sup>C interface as described in the interface description.

**Table 3. VLDO1 and VLDO2 Voltage Options**

DEFLD02	DEFLD01	VLDO1	VLDO2
0	0	1.3 V	3.3 V
0	1	2.8 V	3.3 V
1	0	1.3 V	1.8 V
1	1	1.8 V	3.3 V

#### 8.4.5.2 Interrupt Management and the $\overline{INT}$ Pin

The  $\overline{INT}$  pin combines the outputs of the PGOOD comparators from each DC-DC converter and the LDOs. The  $\overline{INT}$  pin is used as a POWER\_OK pin to indicate when all enabled supplies are in regulation. The  $\overline{INT}$  pin remains active (low state) during power up as long as all enabled power rails are below their regulation limit. Once the last enabled power rail is within regulation, the  $\overline{INT}$  pin transitions to a high state.

During operation, if one of the enabled supplies goes out of regulation,  $\overline{INT}$  transitions to a low state, and the corresponding bit in the PGOODZ register goes high. If the supply goes back to its regulation limits,  $\overline{INT}$  transitions back to a high state.

While  $\overline{\text{INT}}$  is in an active low state, reading the PGOODZ register through the I<sup>2</sup>C bus forces  $\overline{\text{INT}}$  into a high-Z state. Because this pin requires an external pullup resistor, the  $\overline{\text{INT}}$  pin transitions to a logic-high state even though the supply in question is still out of regulation. The corresponding bit in the PGOODZ register still indicates that the power rail is out of regulation.

Interrupts can be masked using the MASK register. The default operation is not to mask any DCDC or LDO interrupts, because these provide the POWER\_OK function.

## 8.5 Programming

### 8.5.1 Power-Up Sequencing

The TPS65023-Q1 power-up sequencing is designed to be entirely flexible and customer driven. This is achieved by providing separate enable pins for each switch-mode converter and a common enable signal for the LDOs. The relevant control pins are described in [Table 4](#).

**Table 4. Control Pins and Status Outputs For DC-DC Converters**

PIN NAME	I/O	FUNCTION
DEFDCDC3	I	Defines the default voltage of the VDCDC3 switching converter. DEFDCDC3 = 0 defaults VDCDC3 to 1.8 V, DEFDCDC3 = VCC defaults VDCDC3 to 3.3 V.
DEFDCDC2	I	Defines the default voltage of the VDCDC2 switching converter. DEFDCDC2 = 0 defaults VDCDC2 to 1.8 V, DEFDCDC2 = VCC defaults VDCDC2 to 3.3 V.
DEFDCDC1	I	Defines the default voltage of the VDCDC1 switching converter. DEFDCDC1 = 0 defaults VDCDC1 to 1.2 V, DEFDCDC1 = VCC defaults VDCDC1 to 1.6 V.
DCDC3_EN	I	Set DCDC3_EN = 0 to disable and DCDC3_EN = 1 to enable the VDCDC3 converter
DCDC2_EN	I	Set DCDC2_EN = 0 to disable and DCDC2_EN = 1 to enable the VDCDC2 converter
DCDC1_EN	I	Set DCDC1_EN = 0 to disable and DCDC1_EN = 1 to enable the VDCDC1 converter
$\overline{\text{HOT\_RESET}}$	I	The $\overline{\text{HOT\_RESET}}$ pin generates a reset ( $\overline{\text{RESPWRON}}$ ) for the processor. $\overline{\text{HOT\_RESET}}$ does not alter any TPS65023-Q1 settings except the output voltage of VDCDC1. Activating $\overline{\text{HOT\_RESET}}$ sets the voltage of VDCDC1 to its default value defined with the DEFDCDC1 pin. $\overline{\text{HOT\_RESET}}$ is internally de-bounced by the TPS65023-Q1.
$\overline{\text{RESPWRON}}$	O	$\overline{\text{RESPWRON}}$ is held low when power is initially applied to the TPS65023-Q1. The VRTC voltage is monitored: $\overline{\text{RESPWRON}}$ is low when $\text{VRTC} < 2.4 \text{ V}$ and remains low for a time defined by the external capacitor at the $\overline{\text{RESPWRON}}$ pin. $\overline{\text{RESPWRON}}$ can also be forced low by activation of the $\overline{\text{HOT\_RESET}}$ pin.
TRESPWRON	I	Connect a capacitor here to define the RESET time at the $\overline{\text{RESPWRON}}$ pin (1 nF typically gives 100 ms).

### 8.5.2 Serial Interface

The serial interface is compatible with the standard- and fast-mode I<sup>2</sup>C specifications, allowing transfers at up to 400 kHz. The interface adds flexibility to the power-supply solution, enabling most functions to be programmed to new values, depending on the instantaneous application requirements and charger status to be monitored. Register contents remain intact as long as  $V_{\text{CC}}$  remains above 2 V. The TPS65023-Q1 has a 7-bit address: 1001000; other addresses are available on contact with the factory. Attempting to read data from the register addresses not listed in this section results in FFh being read out.

For normal data transfer, DATA is allowed to change only when CLK is low. Changes when CLK is high are reserved for indicating the start and stop conditions. During data transfer, the data line must remain stable whenever the clock line is high. There is one clock pulse per bit of data. Each data transfer is initiated with a start condition and terminated with a stop condition. When addressed, the TPS65023-Q1 device generates an acknowledge bit after the reception of each byte. The master device (microprocessor) must generate an extra clock pulse that is associated with the acknowledge bit. The TPS65023-Q1 device must pull down the DATA line during the acknowledge clock pulse so that the DATA line is a stable low during the high period of the acknowledge clock pulse. The DATA line is a stable low during the high period of the acknowledge-related clock pulse. Setup and hold times must be taken into account. During read operations, a master must signal the end of data to the slave by not generating an acknowledge bit on the last byte that was clocked out of the slave. In this case, the slave TPS65023-Q1 device must leave the data line high to enable the master to generate the stop condition.

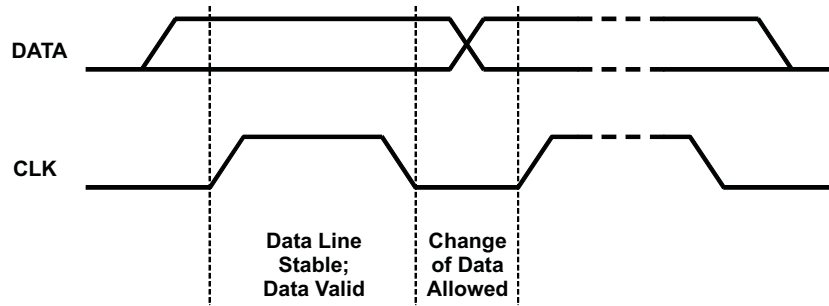


Figure 28. Bit Transfer on the Serial Interface

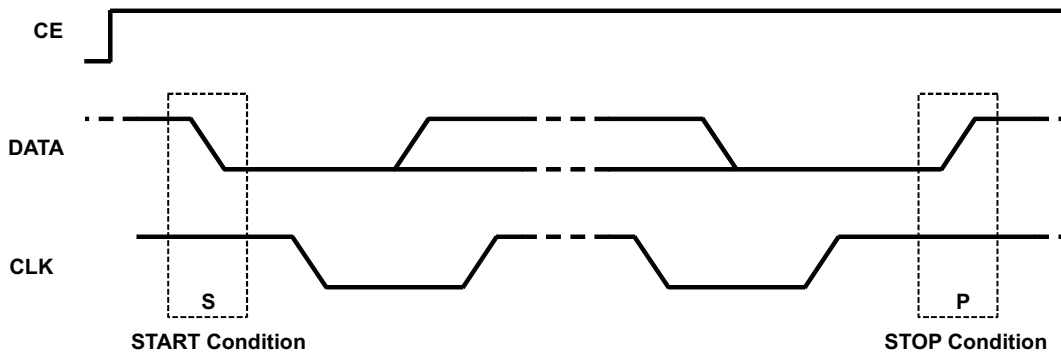
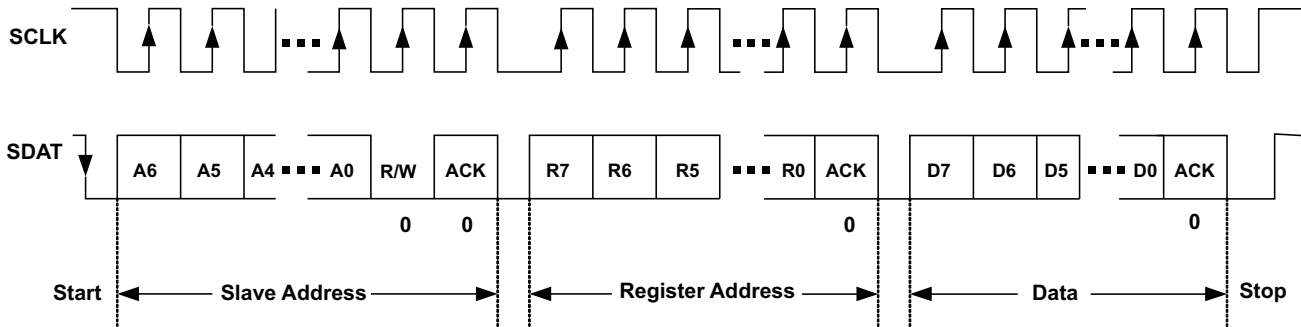
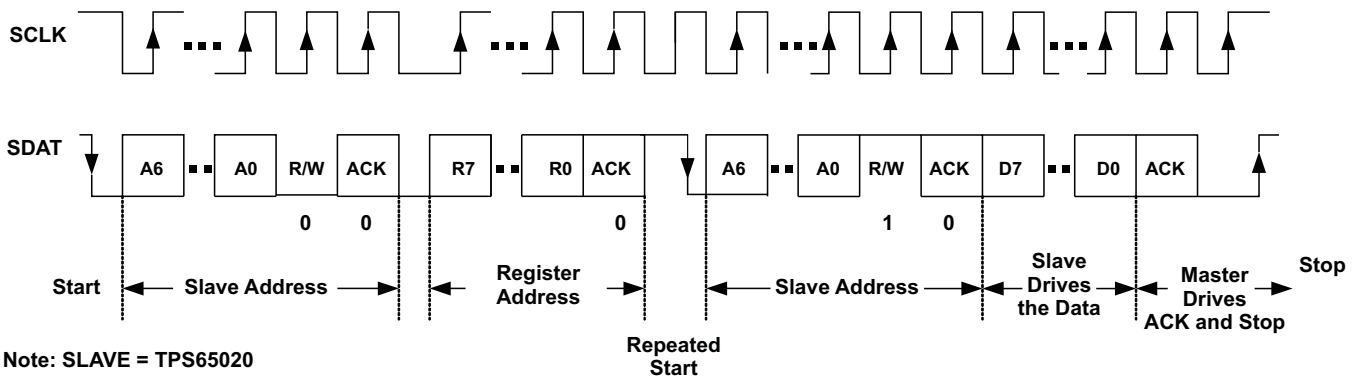


Figure 29. Start and Stop Conditions



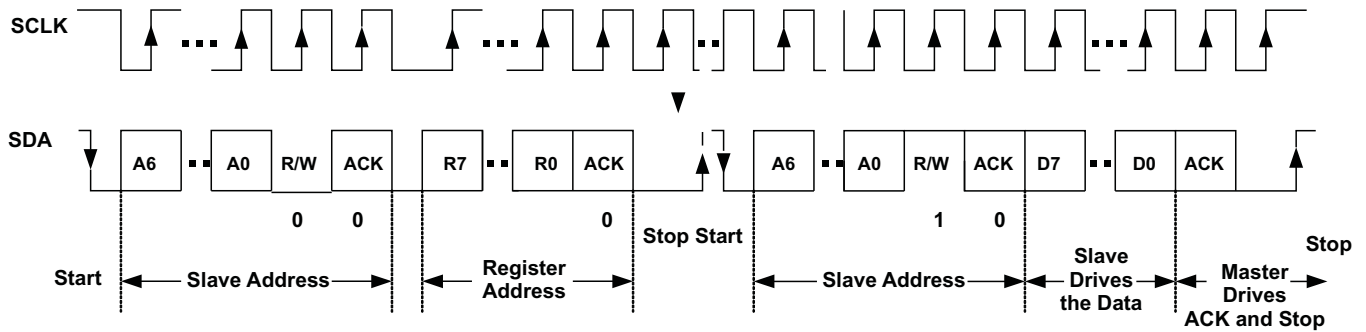
Note: SLAVE = TPS65020

Figure 30. Serial Interface Write to TPS65023-Q1 Device



Note: SLAVE = TPS65020

Figure 31. Serial Interface Read from TPS65023-Q1: Protocol A



Note: SLAVE = TPS65020

**Figure 32. Serial Interface Read from TPS65023-Q1: Protocol B**

## 8.6 Register Maps

### 8.6.1 VERSION Register (address: 00h) Read-Only

**Figure 33. VERSION Register Fields**

7	6	5	4	3	2	1	0
VERSION							
R-0	R-0	R-1	R-0	R-0	R-0	R-1	R-1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**8.6.2 PGOODZ Register (address: 01h) Read-Only**
**Figure 34. PGOODZ Register Fields**

7	6	5	4	3	2	1	0
PWRFAILZ	LOWBATTZ	PGOODZ VDCDC1	PGOODZ VDCDC2	PGOODZ VDCDC3	PGOODZ LDO2	PGOODZ LDO1	
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 5. PGOODZ Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	PWRFAILZ	R	0	Set by signal: PWRFAIL 0 = indicates that the PWRFAIL_SNS input voltage is above the 1-V threshold. 1 = indicates that the PWRFAIL_SNS input voltage is below the 1-V threshold.
6	LOWBATTZ	R	0	Set by signal: LOWBATT 0 = indicates that the LOWBATT_SNS input voltage is above the 1-V threshold. 1 = indicates that the LOWBATT_SNS input voltage is below the 1-V threshold.
5	PGOODZ VDCDC1	R	0	Set by signal: PGOODZ_VDCDC1 0 = indicates that the VDCDC1 converter output voltage is within its nominal range. This bit is zero if the VDCDC1 converter is disabled. 1 = indicates that the VDCDC1 converter output voltage is below its target regulation voltage.
4	PGOODZ VDCDC2	R	0	Set by signal: PGOODZ_VDCDC2 0 = indicates that the VDCDC2 converter output voltage is within its nominal range. This bit is zero if the VDCDC2 converter is disabled. 1 = indicates that the VDCDC2 converter output voltage is below its target regulation voltage.
3	PGOODZ VDCDC3	R	0	Set by signal: PGOODZ_VDCDC3 0 = indicates that the VDCDC3 converter output voltage is within its nominal range. This bit is zero if the VDCDC3 converter is disabled and during a DVM-controlled output-voltage transition. 1 = indicates that the VDCDC3 converter output voltage is below its target regulation voltage.
2	PGOODZ LDO2	R	0	Set by signal: PGOODZ_LDO2 0 = indicates that the LDO2 output voltage is within its nominal range. This bit is zero if LDO2 is disabled. 1 = indicates that LDO2 output voltage is below its target regulation voltage.
1	PGOODZ LDO1	R	0	Set by signal: PGOODZ_LDO1 0 = indicates that the LDO1 output voltage is within its nominal range. This bit is zero if LDO1 is disabled. 1 = indicates that the LDO1 output voltage is below its target regulation voltage.

**8.6.3 MASK Register (address: 02h)**
**Figure 35. MASK Register Fields**

7	6	5	4	3	2	1	0
MASK PWRFAILZ	MASK LOWBATTZ	MASK VDCDC1	MASK VDCDC2	MASK VDCDC3	MASK LDO2	MASK LDO1	
R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

The MASK register can be used to mask particular fault conditions from appearing at the  $\overline{\text{INT}}$  pin. MASK<n> = 1 masks PGOODZ<n>.

**8.6.4 REG\_CTRL Register (address: 03h)**

The REG\_CTRL register is used to disable or enable the power supplies through the serial interface. The contents of the register are logically ANDed with the enable pins to determine the state of the supplies. A UVLO condition resets the REG\_CTRL to 0xFF, so the state of the supplies defaults to the state of the enable pin. The REG\_CTRL bits are automatically reset to default when the corresponding enable pin is low.

**Figure 36. REG\_CTRL Register Fields**

7	6	5	4	3	2	1	0
		VDCDC1 ENABLE	VDCDC2 ENABLE	VDCDC3 ENABLE	LDO2 ENABLE	LDO1 ENABLE	
R-1	R-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R-1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 6. REG\_CTRL Register Field Descriptions**

Bit	Field	Type	Reset	Description
5	VDCDC1 ENABLE	R/W	1	Set by signal: DCDC1_ENZ DCDC1 enable. This bit is logically ANDed with the state of the DCDC1_EN pin to turn on the DCDC1 converter. Reset to 1 by a UVLO condition, the bit can be written to 0 or 1 through the serial interface. The bit is reset to 1 when the DCDC1_EN pin is pulled to GND, allowing DCDC1 to turn on when DCDC1_EN returns high.
4	VDCDC2 ENABLE	R/W	1	Set by signal: DCDC2_ENZ DCDC2 enable. This bit is logically ANDed with the state of the DCDC2_EN pin to turn on the DCDC2 converter. Reset to 1 by a UVLO condition, the bit can be written to 0 or 1 through the serial interface. The bit is reset to 1 when the DCDC2_EN pin is pulled to GND, allowing DCDC2 to turn on when DCDC2_EN returns high.
3	VDCDC3 ENABLE	R/W	1	Set by signal: DCDC3_ENZ DCDC3 enable. This bit is logically ANDed with the state of the DCDC3_EN pin to turn on the DCDC3 converter. Reset to 1 by a UVLO condition, the bit can be written to 0 or 1 through the serial interface. The bit is reset to 1 when the DCDC3_EN pin is pulled to GND, allowing DCDC3 to turn on when DCDC3_EN returns high.
2	LDO2 ENABLE	R/W	1	Set by signal: LDO_ENZ LDO2 enable. This bit is logically ANDed with the state of the LDO2_EN pin to turn on LDO2. Reset to 1 by a UVLO condition, the bit can be written to 0 or 1 through the serial interface. The bit is reset to 1 when the LDO_EN pin is pulled to GND, allowing LDO2 to turn on when LDO_EN returns high.
1	LDO1 ENABLE	R/W	1	Set by signal: LDO_ENZ LDO1 enable. This bit is logically ANDed with the state of the LDO1_EN pin to turn on LDO1. Reset to 1 by a UVLO condition, the bit can be written to 0 or 1 through the serial interface. The bit is reset to 1 when the LDO_EN pin is pulled to GND, allowing LDO1 to turn on when LDO_EN returns high.

### 8.6.5 CON\_CTRL Register (address: 04h)

**Figure 37. CON\_CTRL Register Fields**

7	6	5	4	3	2	1	0
DCDC2 PHASE1	DCDC2 PHASE0	DCDC3 PHASE1	DCDC3 PHASE0	LOW RIPPLE	FPWM DCDC2	FPW DCDC1	FPWM DCDC3
R/W-1	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

The CON\_CTRL register is used to force any or all of the converters into forced PWM operation when low output-voltage ripple is vital. It is also used to control the phase shift between the three converters to minimize the input rms current, hence reduce the required input blocking capacitance. The DCDC1 converter is taken as the reference and consequently has a fixed-zero phase shift.

**Table 7. CON\_CTRL Register Field Descriptions**

Bit	Field	Type	Reset	Description
7–6	DCDC2 PHASE1, PHASE0	R/W	10	DCDC2 Converter delay is set by these bits. 00 = Zero 01 = 1/4 cycle 10 = 1/2 cycle 11 = 3/4 cycle
5–4	DCDC3 PHASE1, PHASE0	R/W	11	DCDC3 Converter delay is set by these bits. 00 = Zero 01 = 1/4 cycle 10 = 1/2 cycle 11 = 3/4 cycle
3	LOW RIPPLE:	R/W	0	0 = PFM mode operation optimized for high efficiency for all converters 1 = PFM mode operation optimized for low output-voltage ripple for all converters
2	FPWM DCDC2:	R/W	0	0 = DCDC2 converter operates in PWM or PFM mode 1 = DCDC2 converter is forced into fixed-frequency PWM mode.
1	FPWM DCDC1:	R/W	0	0 = DCDC1 converter operates in PWM or PFM mode 1 = DCDC1 converter is forced into fixed-frequency PWM mode.
0	FPWM DCDC3:	R/W	0	0 = DCDC3 converter operates in PWM or PFM mode 1 = DCDC3 converter is forced into fixed-frequency PWM mode.

**8.6.6 CON\_CTRL2 Register (address: 05h)**
**Figure 38. CON\_CTRL2 Register Fields**

7	6	5	4	3	2	1	0
GO	Core adj allowed				DCDC2 discharge	DCDC1 discharge	DCDC3 discharge
R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

The CON\_CTRL2 register can be used to take control the inductive converters.

RESET(1): CON\_CTRL2[6] is reset to its default value by one of these events:

- Undervoltage lockout (UVLO)
- $\overline{\text{HOT\_RESET}}$  pulled low
- $\overline{\text{RESPWRON}}$  active
- VRTC below threshold

**Table 8. CON\_CTRL2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	GO	R/W	0	0 = no change in the output voltage for the DCDC1 converter 1 = the output voltage of the DCDC1 converter is changed to the value defined in DEFDCORE with the slew rate defined in DEFSLEW. This bit is automatically cleared when the DVM transition is complete. The transition is considered complete in this case when the desired output voltage code has been reached, not when the VDCDC3 output voltage is actually in regulation at the desired voltage.
6	CORE ADJ allowed	R/W	1	0 = the output voltage is set with the I <sup>2</sup> C register 1 = DEFDCDC1 is either connected to GND or VCC or an external voltage divider. When connected to GND or VCC, VDCDC1 defaults to 1.2 V or 1.6 V, respectively, at start-up.
2–0	DCDC2, DCDC1, DCDC3 discharge	R/W	000	0 = the output capacitor of the associated converter is not actively discharged when the converter is disabled. 1 = the output capacitor of the associated converter is actively discharged when the converter is disabled. This decreases the fall time of the output voltage at light load.



**8.6.8 DEFSLEW Register (address: 07h)**
**Figure 40. DEFSLEW Register Fields**

7	6	5	4	3	2	1	0
					SLEW2	SLEW1	SLEW0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 10. DEFSLEW Register Field Descriptions**

Bit	Field	Type	Reset	Description
2–0	SLEW2, SLEW1, SLEW0	R/W	110	These bits set the VDCDC1 SLEW RATE 000 = 0.225 mV/μs 001 = 0.45 mV/μs 010 = 0.9 mV/μs 011 = 1.8 mV/μs 100 = 3.6 mV/μs 101 = 7.2 mV/μs 110 = 14.4 mV/μs 111 = Immediate

**8.6.9 LDO\_CTRL Register (address: 08h)**
**Figure 41. LDO\_CTRL Register Fields**

7	6	5	4	3	2	1	0
Reserved	LDO2_2	LDO2_1	LDO2_0	Reserved	LDO1_2	LDO1_1	LDO1_0
R/W-0	R/W-DEFLDOx	R/W-DEFLDOx	R/W-DEFLDOx	R/W-0	R/W-DEFLDOx	R/W-DEFLDOx	R/W-DEFLDOx

The default value for this register is set with DEFLDO1 and DEFLDO2.

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

The LDO\_CTRL registers can be used to set the output voltage of LDO1 and LDO2. LDO\_CTRL[7] and LDO\_CTRL[3] are reserved and should always be written to 0.

The default voltage is set with DEFLDO1 and DEFLDO2 pins as described in [Table 11](#).

**Table 11. LDO\_CTRL Register Field Descriptions**

Bit	Field	Type	Reset	Description
6–4	LDO2_2, LDO2_1, LDO2_0	R/W	See (1)	000 = 1.05 V 001 = 1.2 V 010 = 1.3 V 011 = 1.8 V 100 = 2.5 V 101 = 2.8 V 110 = 3 V 111 = 3.3 V
2–0	LDO1_2, LDO1_1, LDO1_0	R/W	See (1)	000 = 1 V 001 = 1.1 V 010 = 1.3 V 011 = 1.8 V 100 = 2.2 V 101 = 2.6 V 110 = 2.8 V 111 = 3.15 V

(1) [Table 3](#) describes the default voltage options based on DEFLDO1 and DEFLDO2 pins.

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

#### 9.1.1 Reset Condition of DCDC1

If DEFDCDC1 is connected to ground and DCDC1\_EN is pulled high after VINDCDC1 is applied, the output voltage of DCDC1 defaults to 1.225 V instead of 1.2 V (high by 2%). [Figure 42](#) illustrates the problem.

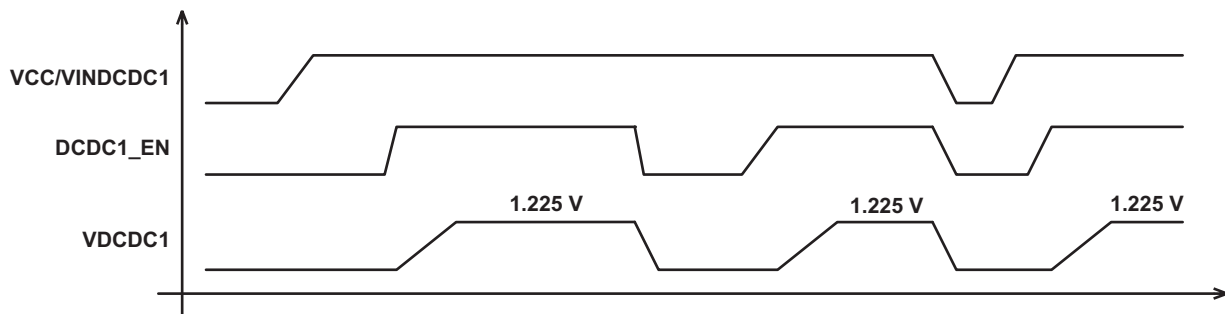


Figure 42. Default DCDC1

Workaround 1: Tie DCDC1\_EN to VINDCDC1 ([Figure 43](#))

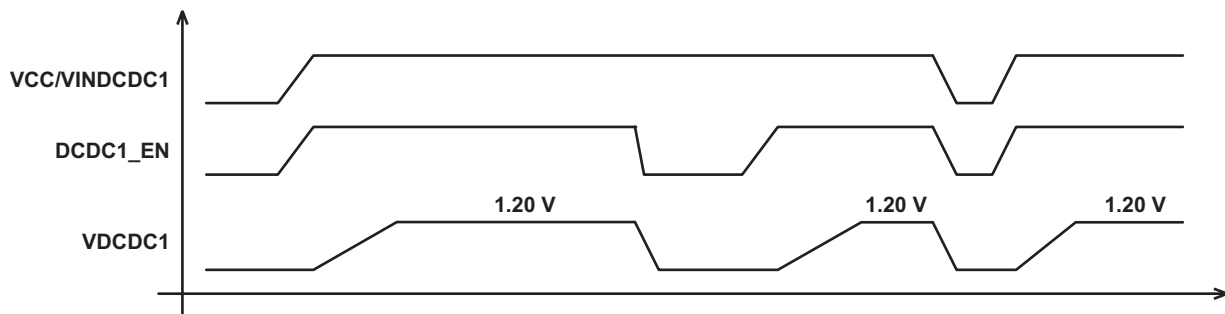
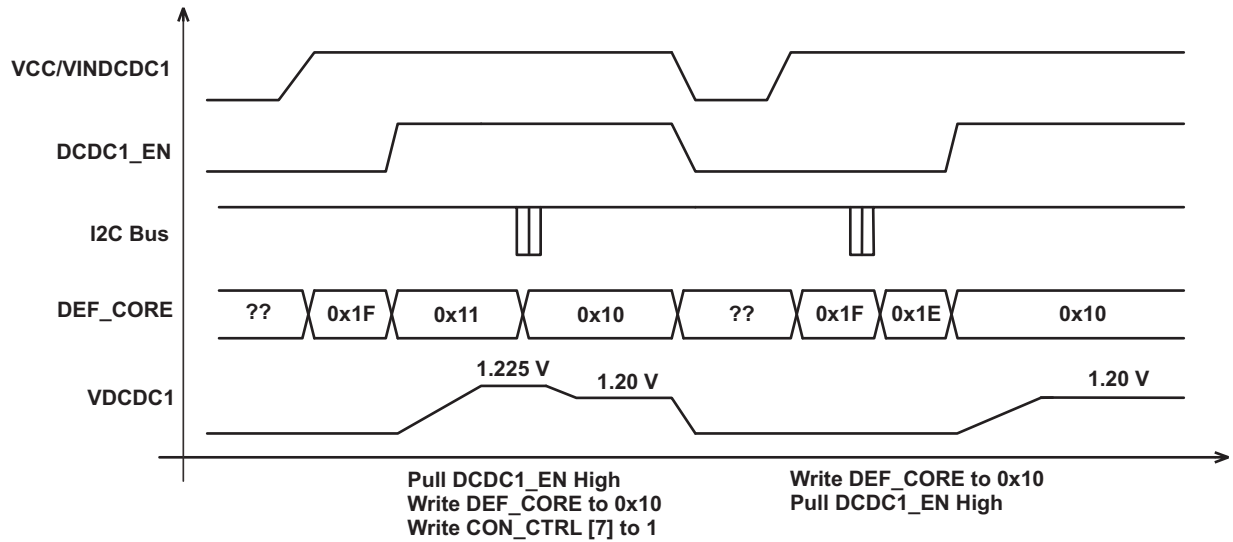


Figure 43. Workaround 1

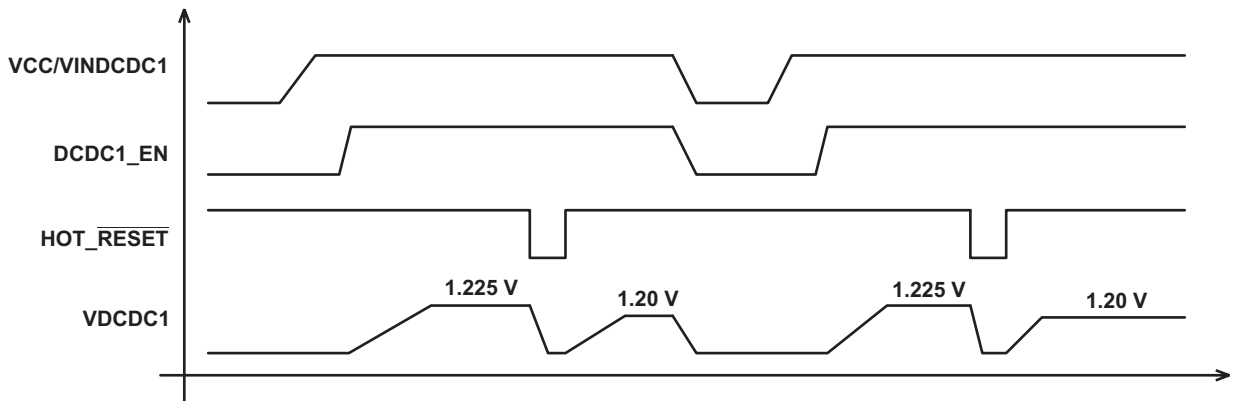
**Application Information (continued)**

Workaround 2: Write the correct voltage to the DEF\_CORE register through I<sup>2</sup>C. This can be done before or after the converter is enabled. If written before the enable, the only bit changed is DEF\_CORE[0]. The voltage is 1.2 V, however, when the enable is pulled high (Figure 44).



**Figure 44. Workaround 2**

Workaround 3: Generate a  $\overline{\text{HOT\_RESET}}$  after enabling DCDC1 (Figure 45)



**Figure 45. Workaround 3**



## Typical Application (continued)

### 9.2.2 Detailed Design Procedure

#### 9.2.2.1 Inductor Selection for the DC-DC Converters

Each of the converters in the TPS65023-Q1 typically uses a 2.2- $\mu$ H output inductor. Larger or smaller inductor values are used to optimize the performance of the device for specific operation conditions. The selected inductor must be rated for its DC resistance and saturation current. The DC resistance of the inductance influences directly the efficiency of the converter. Therefore, an inductor with lowest DC resistance should be selected for highest efficiency.

For a fast transient response, TI recommends a 2.2- $\mu$ H inductor in combination with a 22- $\mu$ F output capacitor.

[Equation 4](#) calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with [Equation 4](#). This is needed because during a heavy load transient the inductor current rises above the value calculated under [Equation 4](#).

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \quad (4)$$

$$I_{L(max)} = I_{OUT(max)} + \frac{\Delta I_L}{2}$$

where

- f = Switching frequency (2.25 MHz typical)
- L = Inductor value
- $\Delta I_L$  = Peak-to-peak inductor ripple current
- $I_{LMAX}$  = Maximum inductor current
- 

(5)

The highest inductor current occurs at maximum  $V_{IN}$ .

Open-core inductors have a soft saturation characteristic, and they can usually handle higher inductor currents versus a comparable shielded inductor.

A more-conservative approach is to select the inductor current rating just for the maximum switch current of the TPS65023-Q1 (2 A for the VDCDC1 and VDCDC2 converters, and 1.5 A for the VDCDC3 converter). The core material from inductor to inductor differs and has an impact on the efficiency, especially at high switching frequencies.

See [Table 12](#) and the typical applications for possible inductors.

**Table 12. Tested Inductors**

DEVICE	INDUCTOR VALUE	TYPE	COMPONENT SUPPLIER
All converters	2.2 $\mu$ H	LPS4012-222LMB	Coilcraft
	2.2 $\mu$ H	VLFC4020T-2R2N1R7	TDK

#### 9.2.2.2 Output Capacitor Selection

The advanced fast-response voltage-mode control scheme of the inductive converters implemented in the TPS65023-Q1 allow the use of small ceramic capacitors with a typical value of 10  $\mu$ F for each converter without having large output-voltage under- and overshoots during heavy load transients. Ceramic capacitors having low ESR values have the lowest output-voltage ripple and are recommended. See [Table 13](#) for recommended components.

If ceramic output capacitors are used, the capacitor rms ripple-current rating always meets the application requirements. Just for completeness, the rms ripple current is calculated as:

$$I_{RMSCOU} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (6)$$

At nominal load current, the inductive converters operate in PWM mode. The overall output-voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta V_{OUT} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \left( \frac{1}{8 \times C_{OUT} \times f} + ESR \right)$$

where

- the highest output-voltage ripple occurs at the highest input-voltage  $V_{IN}$  (7)

At light load currents, the converters operate in PSM and the output-voltage ripple is dependent on the output-capacitor value. The output-voltage ripple is set by the internal comparator delay and the external capacitor. The typical output-voltage ripple is less than 1% of the nominal output voltage.

### 9.2.2.3 Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low-ESR input capacitor is required for best input-voltage filtering and minimizing the interference with other circuits caused by high input-voltage spikes. Each DC-DC converter requires a 10- $\mu$ F ceramic input capacitor on its input pin VINDCDCx. The input capacitor is increased without any limit for better input-voltage filtering. The VCC pin is separated from the input for the DC-DC converters. A filter resistor of up to 10R and a 1- $\mu$ F capacitor are used for decoupling the VCC pin from switching noise. Note that the filter resistor may affect the UVLO threshold, because up to 3 mA can flow through this resistor into the VCC pin when all converters are running in PWM mode.

**Table 13. Possible Capacitors**

CAPACITOR VALUE	CASE SIZE	COMPONENT SUPPLIER	COMMENTS
22 $\mu$ F	1206	TDK C3216X5R0J226M	Ceramic
22 $\mu$ F	1206	Taiyo Yuden JMK316BJ226ML	Ceramic
22 $\mu$ F	0805	TDK C2012X5R0J226MT	Ceramic
22 $\mu$ F	0805	Taiyo Yuden JMK212BJ226MG	Ceramic
10 $\mu$ F	0805	Taiyo Yuden JMK212BJ106M	Ceramic
10 $\mu$ F	0805	TDK C2012X5R0J106M	Ceramic

### 9.2.2.4 Output Voltage Selection

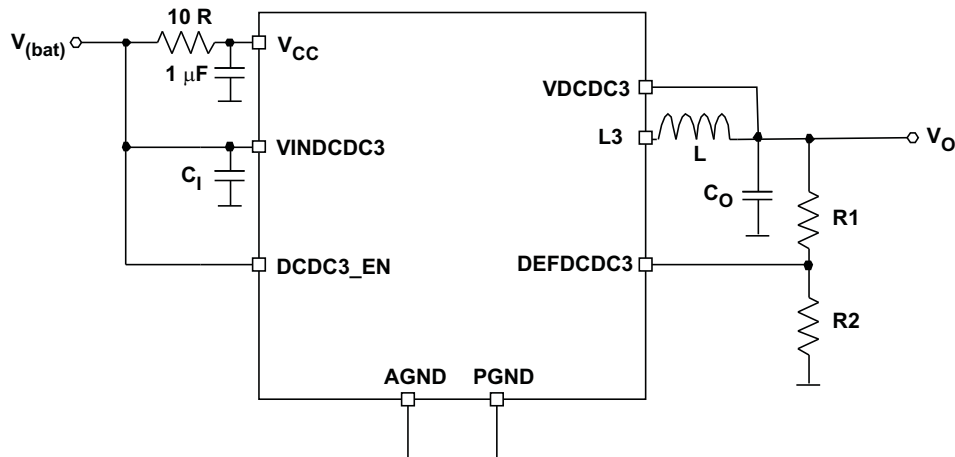
The DEFDCDC1, DEFDCDC2, and DEFDCDC3 pins are used to set the output voltage for each step-down converter. See [Table 14](#) for the default voltages if the pins are pulled to GND or to VCC. If a different voltage is needed, an external resistor divider can be added to the DEFDCDCx pin as shown in [Figure 47](#).

The output voltage of VDCDC1 is set with the I<sup>2</sup>C interface. If the voltage is changed from the default, using the DEFDCDC register, the output voltage only depends on the register value. Any resistor divider at DEFDCDC1 does not change the voltage set with the register.

**Table 14. DCDC1, DCDC2, and DCDC3 Default Voltage Levels**

PIN	LEVEL	DEFAULT OUTPUT VOLTAGE
DEFDCDC1	VCC	1.6 V
	GND	1.2 V
DEFDCDC2	VCC	3.3 V
	GND	1.8 V
DEFDCDC3	VCC	3.3 V
	GND	1.8 V

Using an external resistor divider at DEFDCDCx:



**Figure 47. External Resistor Divider**

When a resistor divider is connected to DEFDCDCx, the output voltage can be set from 0.6 V up to the input voltage  $V_{(bat)}$ . The total resistance ( $R1 + R2$ ) of the voltage divider should be kept in the 1-MR range to maintain a high efficiency at light load.

$$V_{(DEFDCDCx)} = 0.6 \text{ V}$$

$$V_{OUT} = V_{DEFDCDCx} \times \frac{R1+R2}{R2} \quad R1 = R2 \times \left( \frac{V_{OUT}}{V_{DEFDCDCx}} \right) - R2 \quad (8)$$

### 9.2.2.5 VRTC Output

TI recommends adding a 4.7- $\mu\text{F}$  (minimum) capacitor to the VRTC pin.

### 9.2.2.6 LDO1 and LDO2

The LDOs in the TPS65023-Q1 are general-purpose LDOs which are stable using ceramic capacitors. The minimum output capacitor required is 2.2  $\mu\text{F}$ . The LDO output voltages can be changed to different values between 1 V and 3.3 V using the I<sup>2</sup>C interface. Therefore, they can also be used as general-purpose LDOs in applications powering processors different from DaVinci processors. The supply voltage for the LDOs must be connected to the VINLDO pin, giving the flexibility to connect the lowest voltage available in the system and providing the highest efficiency.

### 9.2.2.7 TRESPWRON

This is the input to a capacitor that defines the reset delay time after the voltage at VRTC rises above 2.52 V. The timing is generated by charging and discharging the capacitor with a current of 2  $\mu\text{A}$  between a threshold of 0.25 V and 1 V for 128 cycles. A 1-nF capacitor gives a delay time of 100 ms.

$$t_{(reset)} = 2 \times 128 \times \left( \frac{(1 \text{ V} - 0.25 \text{ V}) \times C_{(reset)}}{2 \mu\text{A}} \right)$$

where

- $t_{(reset)}$  is the reset delay time
  - $C_{(reset)}$  is the capacitor connected to the TRESPWRON pin
- (9)

### 9.2.2.8 $V_{CC}$ Filter

An RC filter connected at the VCC input is used to keep noise from the internal supply for the band-gap and other analog circuitry. A typical value of 1  $\Omega$  and 1  $\mu\text{F}$  is used to filter the switching spikes generated by the DC-DC converters. A larger resistor than 10  $\Omega$  should not be used, because the current into VCC of up to 3 mA causes a voltage drop at the resistor causing the undervoltage lockout circuitry connected at VCC internally to switch off too early.

### 9.2.3 Application Curves

Graphs were taken using the EVM with the inductor and output capacitor combinations found in [Table 1](#).

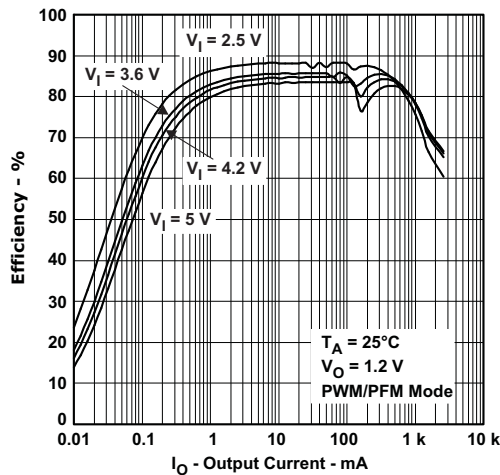


Figure 48. DCDC1 Efficiency

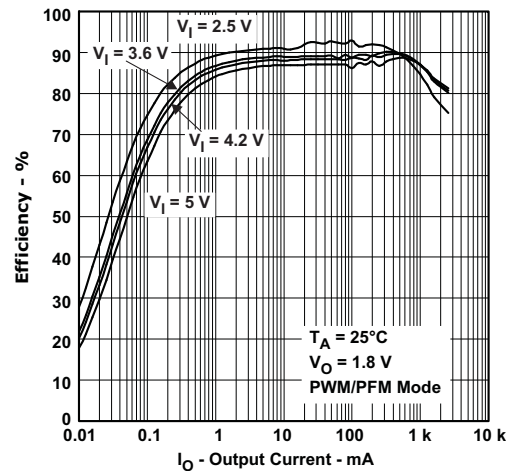


Figure 49. DCDC2 Efficiency

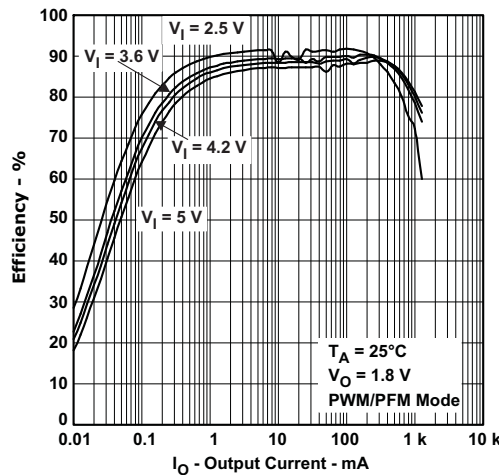


Figure 50. DCDC3 Efficiency

## 10 Power Supply Recommendations

For a supply voltage on pins VCC, VINDCDC1, VINDCDC2, and VINDCDC3 below 3 V, TI recommends enabling the DCDC1, DCDC2, and DCDC3 converters in sequence. If all 3 step-down converters are enabled at the same time while the supply voltage is close to the internal reset detection threshold, a reset may be generated during power up. Therefore TI recommends enabling the DC-DC converters in sequence. This can be done by driving one or two of the enable pins with a RC delay or by driving the enable pin by the output voltage of one of the other step-down converters. If a voltage above 3 V is applied on pin VBACKUP while  $V_{CC}$  and VINDCDCx is below 3 V, there is no restriction in the power-up sequencing as VBACKUP is used to power the internal circuitry.

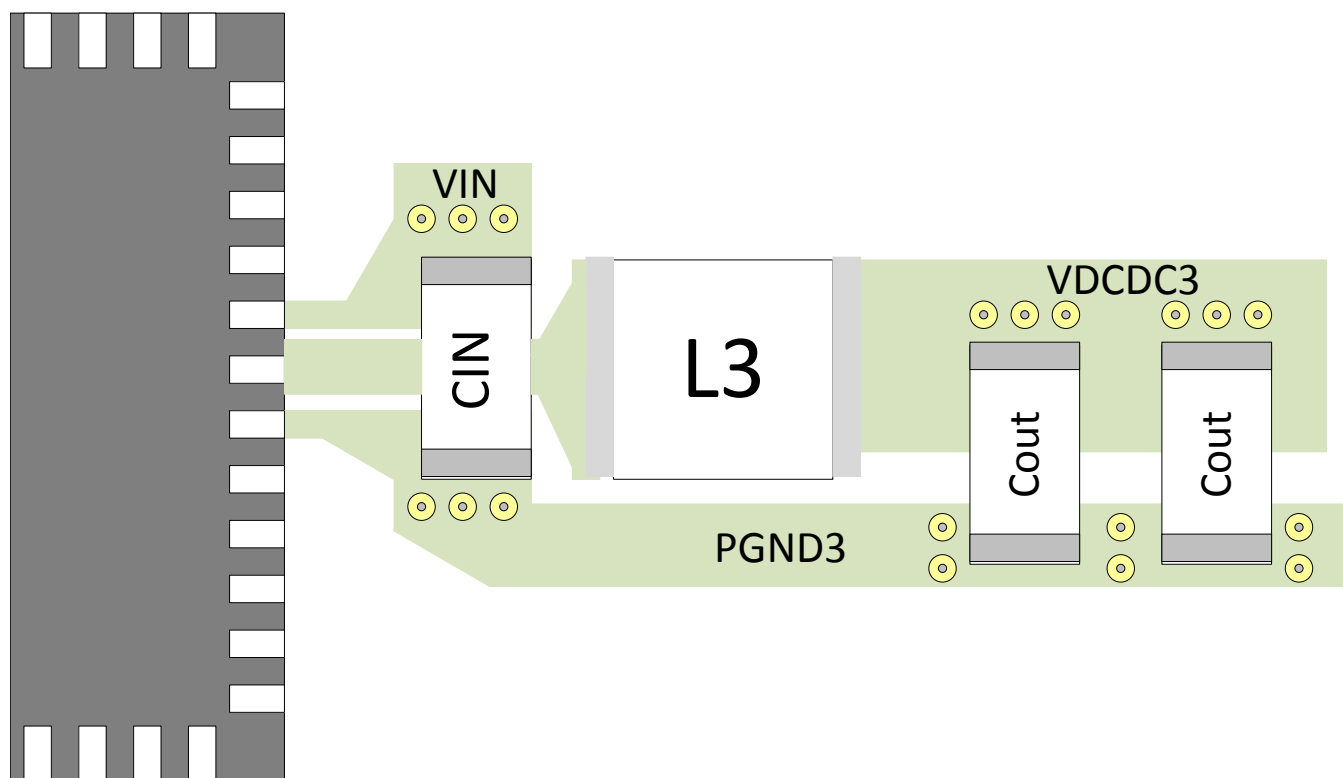
## 11 Layout

### 11.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design. Proper function of the device demands careful attention to PCB layout. Take care in board layout to get the specified performance. If the layout is not carefully done, the regulators may show poor line, load regulation, or both, along with stability issues and EMI problems. It is critical to provide a low impedance ground path. Therefore, use wide and short traces for the main current paths. The input capacitors must be placed as close as possible to the IC pins as well as the inductor and output capacitor.

For the TPS65023-Q1 device, connect the PGND pins of the device to the thermal pad land of the PCB and connect the analog ground connections (AGND) to the PGND at the thermal pad. It is essential to provide a good thermal and electrical connection of all GND pins using multiple vias to the GND-plane. Keep the common path to the AGND pins, which returns the small signal components, and the high current of the output capacitors as short as possible to avoid ground noise. The VDCDCx line must be connected right to the output capacitor and routed away from noisy components and traces (for example, the L1, L2, and L3 traces).

### 11.2 Layout Example



**Figure 51. Layout Example of a DC-DC Converter**

## 12 デバイスおよびドキュメントのサポート

### 12.1 デバイス・サポート

#### 12.1.1 デベロッパー・ネットワークの製品に関する免責事項

デベロッパー・ネットワークの製品またはサービスに関するTIの出版物は、単独またはTIの製品、サービスと一緒に提供される場合に関係なく、デベロッパー・ネットワークの製品またはサービスの適合性に関する是認、デベロッパー・ネットワークの製品またはサービスの是認の表明を意味するものではありません。

### 12.2 ドキュメントのサポート

#### 12.2.1 関連資料

関連資料については、以下を参照してください。

- テキサス・インスツルメンツ、『オープン・ドレイン出力に適切なプルアップ/プルダウン抵抗の選択』アプリケーション・レポート
- テキサス・インスツルメンツ、『TPS65023を使用するNXP i.MX 7用電源の設計』アプリケーション・レポート
- テキサス・インスツルメンツ、『TPS65023を使用するNXP i.MX 6用電源の設計』アプリケーション・レポート
- テキサス・インスツルメンツ、『TPS65023EVMユーザー・ガイド』

#### 12.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](http://ti.com)のデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

#### 12.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™オンライン・コミュニティ** TIのE2E ( *Engineer-to-Engineer* ) コミュニティ。エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイデアを検討して、問題解決に役立てることができます。

**設計サポート** TIの設計サポート役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

#### 12.5 Trademarks

DaVinci, E2E are trademarks of Texas Instruments.

All other trademarks are the property of their respective owners.

#### 12.6 Electrostatic Discharge Caution



これらのデバイスは、限定的なESD (静電破壊) 保護機能を内蔵しています。保存時または取り扱い時は、MOSゲートに対する静電破壊を防止するために、リード線同士をショートさせておくか、デバイスを導電フォームに入れる必要があります。

#### 12.7 Glossary

**SLYZ022** — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

## 13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TPS65023QRHARQ1</a>	Active	Production	VQFN (RHA)   40	3000   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-	65023Q RHA
TPS65023QRHARQ1.B	Active	Production	VQFN (RHA)   40	3000   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	65023Q RHA
<a href="#">TPS65023QRSBRQ1</a>	Active	Production	WQFN (RSB)   40	3000   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS 65023Q
TPS65023QRSBRQ1.B	Active	Production	WQFN (RSB)   40	3000   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS 65023Q

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TPS65023-Q1 :**

- Catalog : [TPS65023](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65023QRHARQ1	VQFN	RHA	40	3000	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65023QRSBRQ1	WQFN	RSB	40	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65023QRHARQ1	VQFN	RHA	40	3000	353.0	353.0	32.0
TPS65023QRSBRQ1	WQFN	RSB	40	3000	353.0	353.0	32.0

## GENERIC PACKAGE VIEW

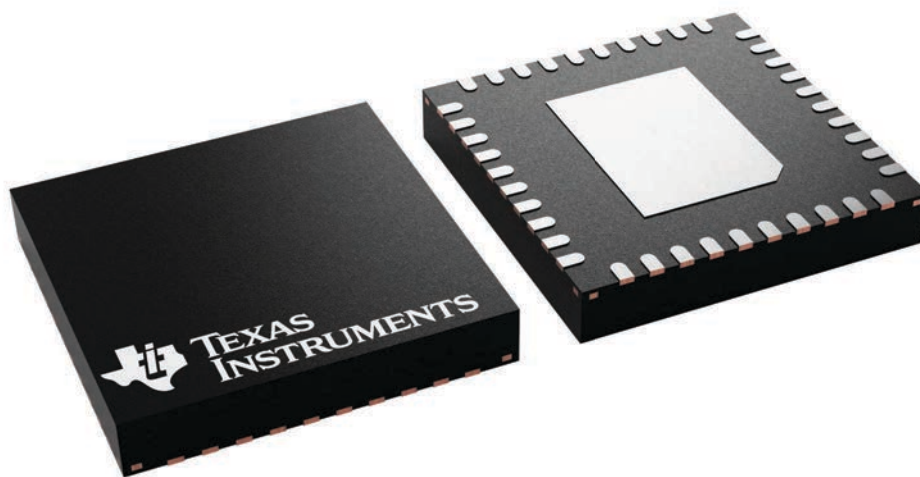
**RHA 40**

**VQFN - 1 mm max height**

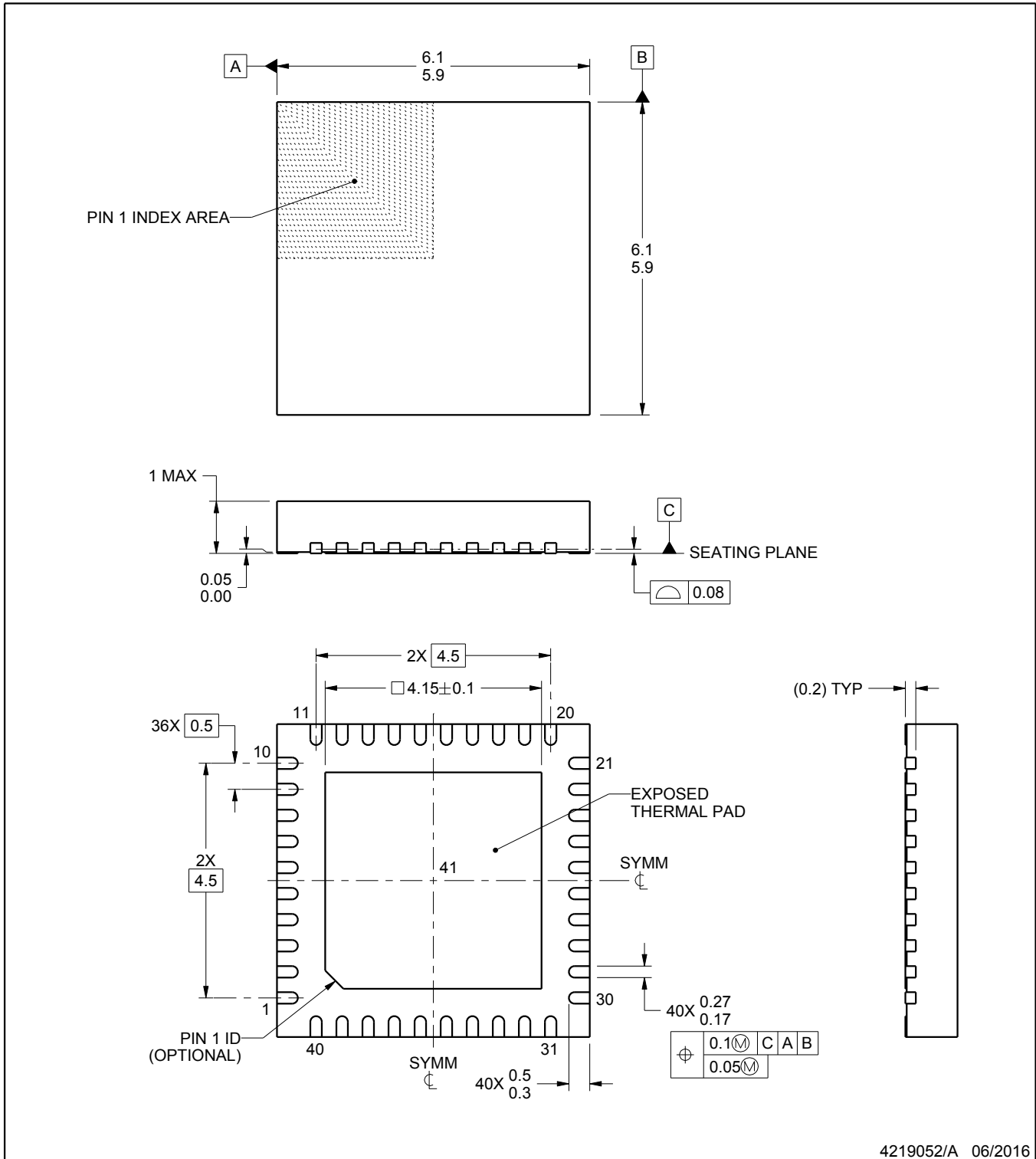
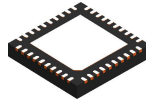
6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4225870/A



4219052/A 06/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

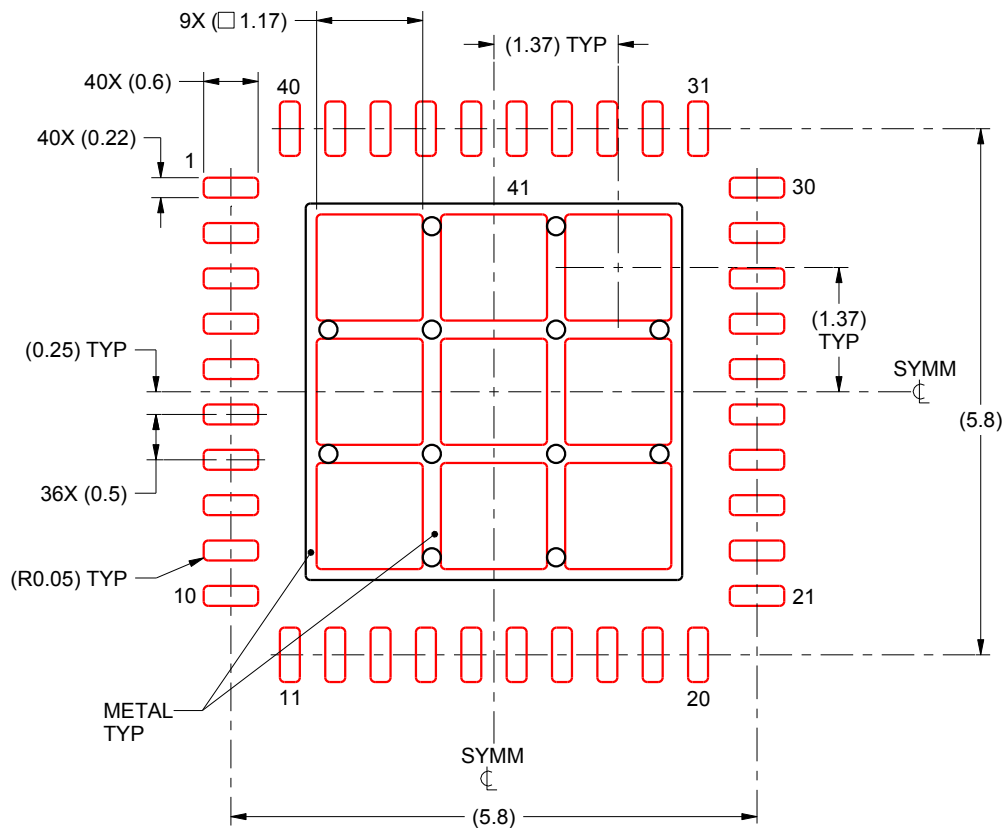


# EXAMPLE STENCIL DESIGN

RHA0040B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:  
72% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:12X

4219052/A 06/2016

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

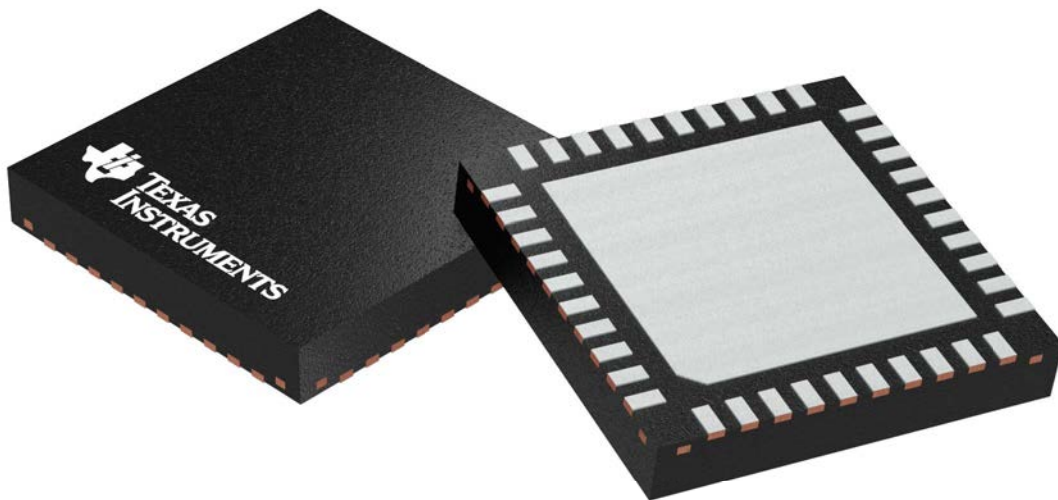
## GENERIC PACKAGE VIEW

**RSB 40**

**WQFN - 0.8 mm max height**

5 x 5 mm, 0.4 mm pitch

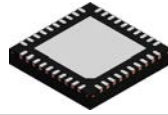
PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4207182/D

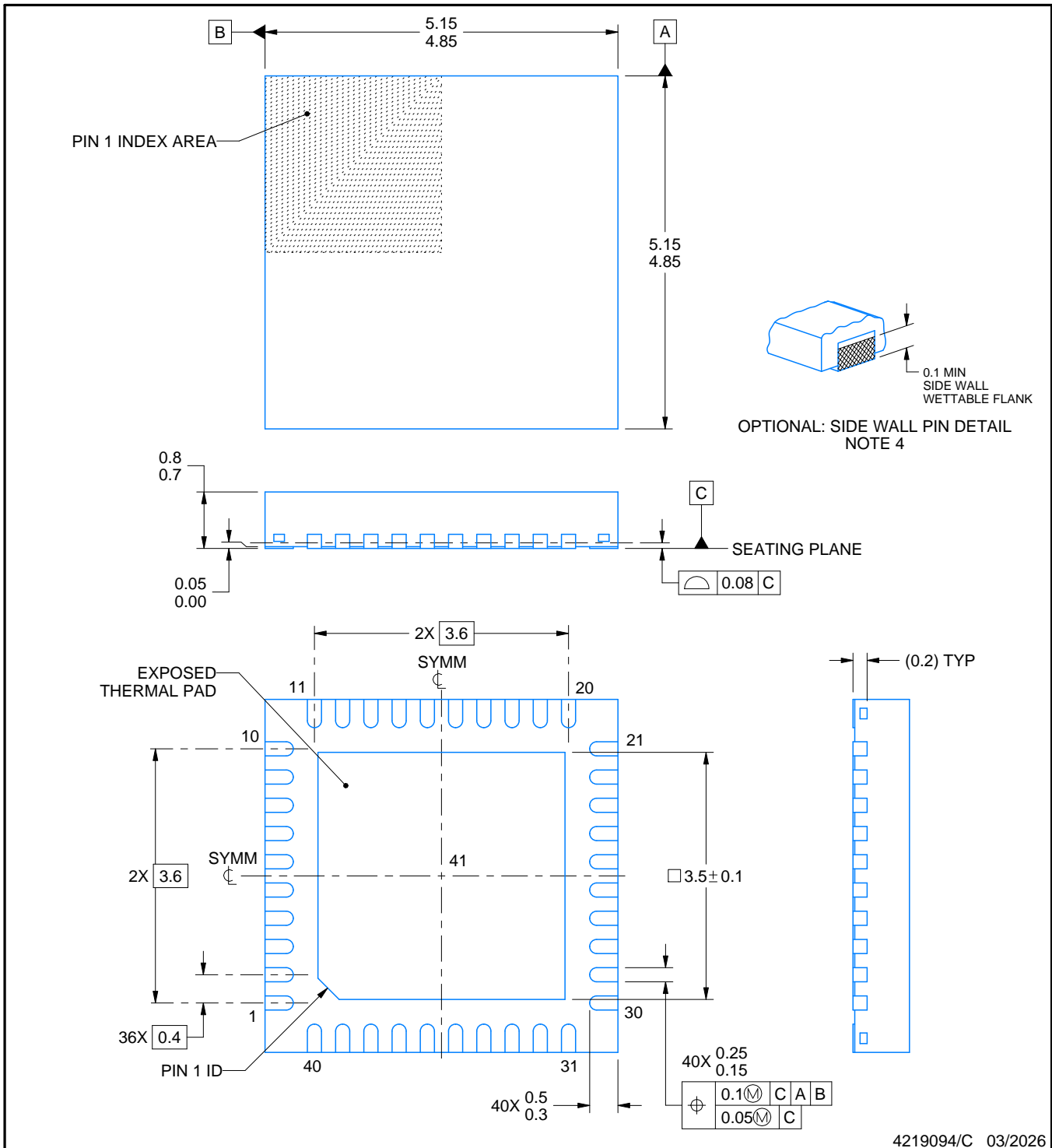
# RSB0040B



# PACKAGE OUTLINE

## WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**NOTES:**

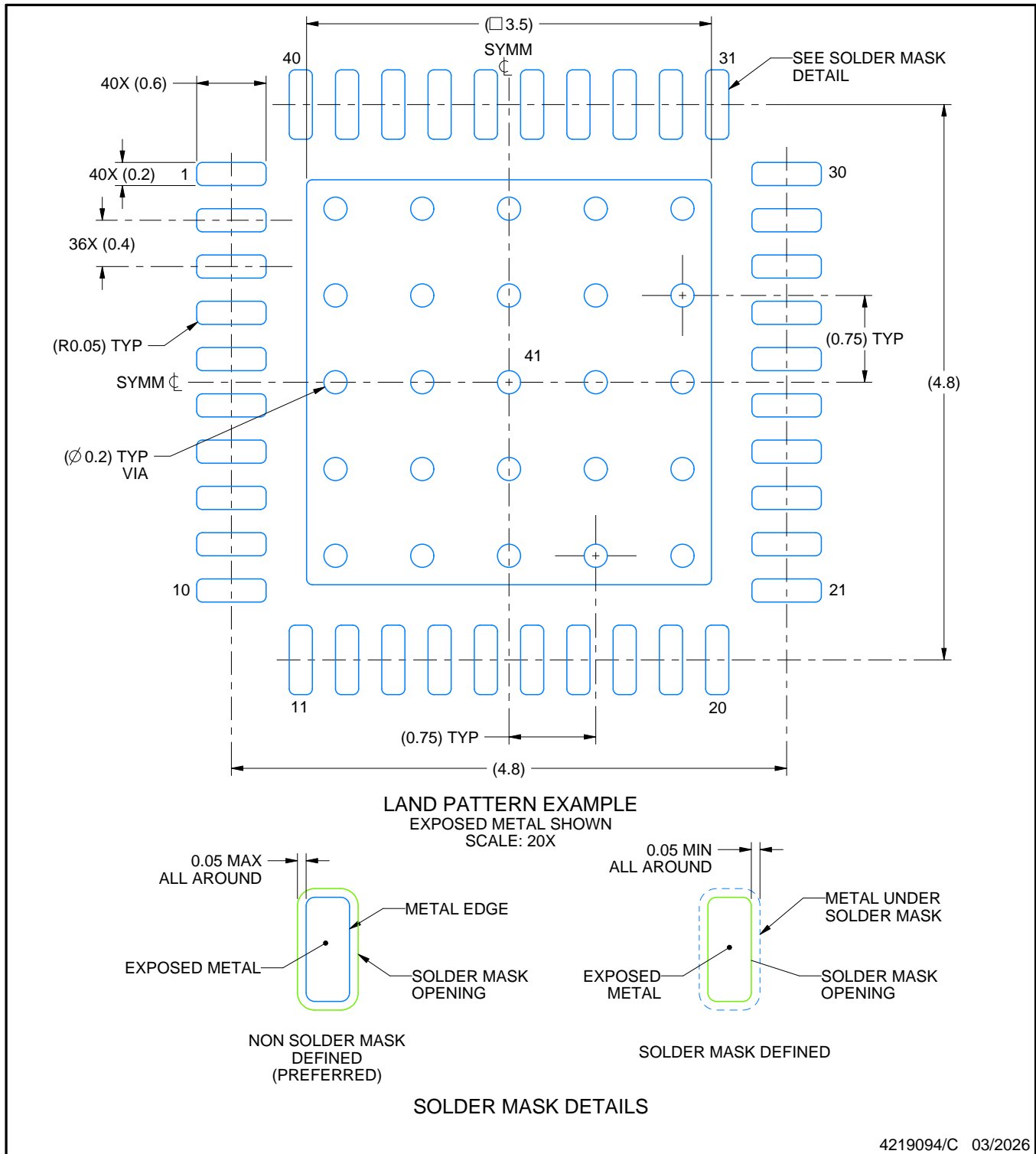
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.

# EXAMPLE BOARD LAYOUT

**RSB0040B**

**WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



4219094/C 03/2026

NOTES: (continued)

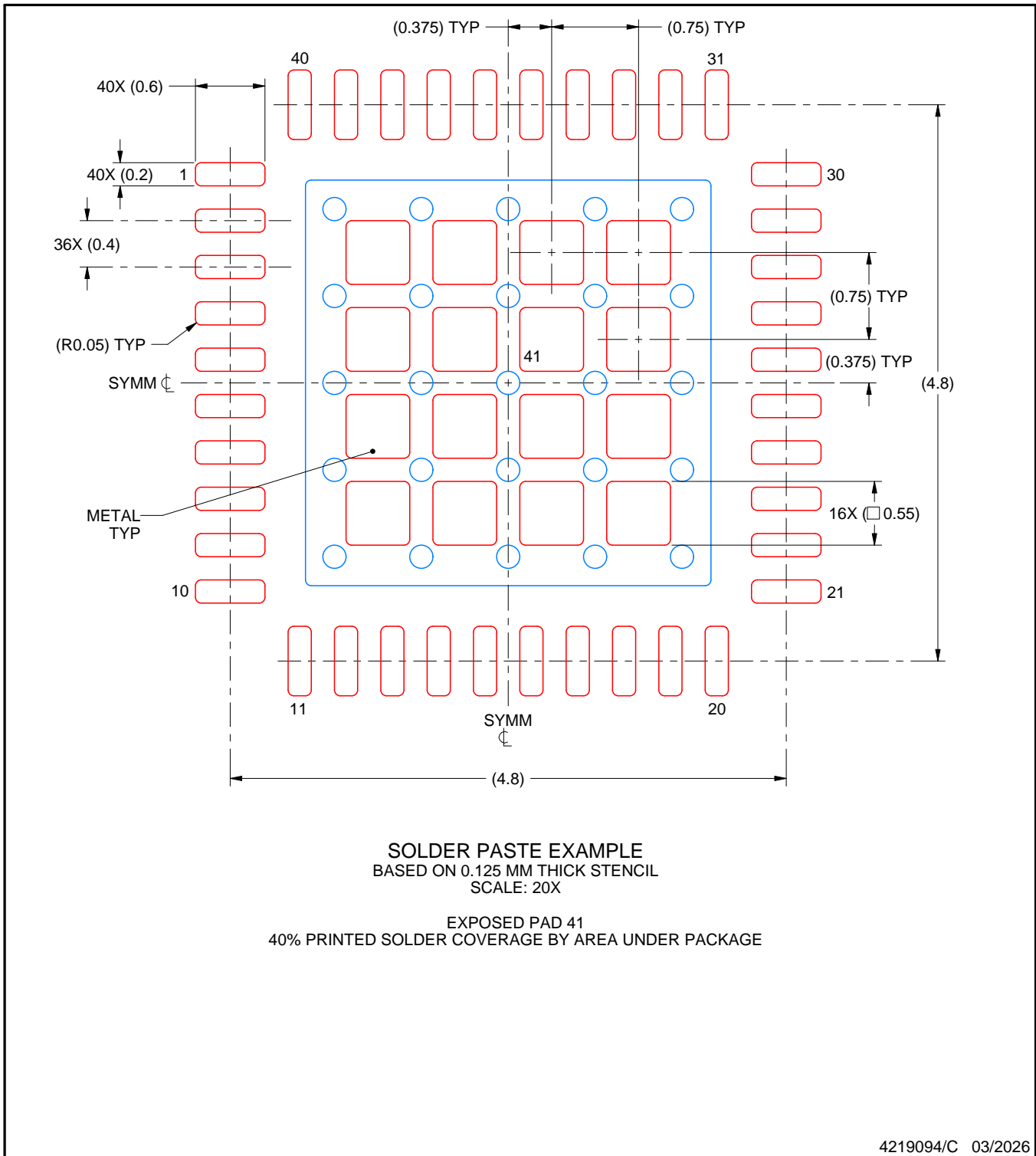
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RSB0040B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## 重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、[TI の総合的な品質ガイドライン](#)、[ti.com](#) または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2026, Texas Instruments Incorporated

最終更新日 : 2025 年 10 月