I²C インターフェイス搭載の TPS652353 LNB 電圧レギュレータ

1 特長

- LNB および I²C インターフェイス用の完全な統合ソリューション
- DiSEqC 2.x および DiSEqC 1.x 互換
- 5V、12V、15V の電源レールに対応
- 外付け抵抗により 1000mA までの高精度出力電流制限を設定可能
- 昇圧スイッチ・ピーク電流制限は LDO 電流制限に比例
- 140mΩ の低 $R_{ds(on)}$ 内部電力スイッチ付き昇圧コンバータ
- 昇圧スイッチング周波数は 1MHz または 500kHz を選択可能
- 強制 PWM モードにより可聴周波数のノイズを回避
- I²C 以外のアプリケーション用の専用イネーブル・ピン
- VLNB 出力用のプッシュプル出力段付き低ドロップアウト (LDO) レギュレータ
- 高精度の 22kHz トーン・ジェネレータ内蔵、外部トーン入力もサポート
- 外部の 44kHz および 22kHz トーン入力をサポート
- ソフトスタートおよび 13V から 18V への電圧遷移時間を調整可能
- 650mV～750mV の 22kHz トーン振幅選択
- 選択可能な過電流時間 (29ms/58ms)
- EN Low 時に I²C レジスタへアクセス可能
- 動的な短絡保護
- 出力電圧レベル、DiSEqC トーン入力および出力、電流レベル、ケーブル接続の診断
- 過熱保護機能を搭載
- 20 ピン WQFN 3mm x 3mm (RUK) パッケージ

2 アプリケーション

- セットトップ・ボックスの衛星放送受信機
- テレビの衛星放送受信機
- PC カードの衛星放送受信機
- 衛星放送テレビ

3 概要

TPS652353 は、I²C インターフェイスを搭載したモノリシックな電圧レギュレータで、アナログおよびデジタルの衛星放送受信機用に設計されており、13V～18V の電源と 22kHz のトーン信号を、皿型アンテナの LNB ダウン・コンバータ、またはマルチスイッチ・ボックスへ供給します。このデバイスは、最小の部品数、低消費電力、単純な設計で、I²C 標準インターフェイスを備えた、包括的なソリューションを提供します。

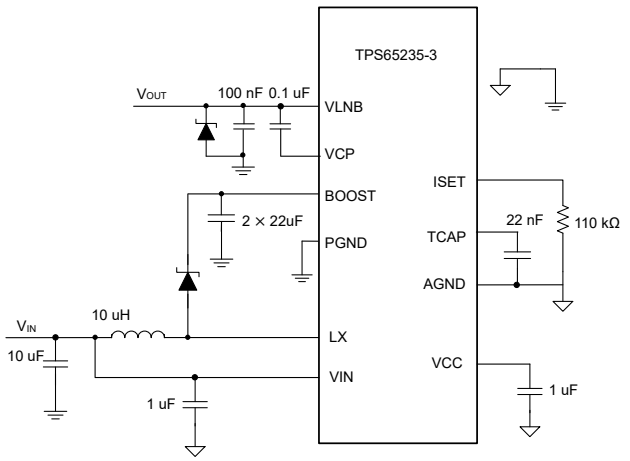
TPS652353 は、電力効率が高いことが特長です。昇圧コンバータには 140mΩ のパワー MOSFET が内蔵されており、スイッチング周波数として 1MHz または 500kHz を選択できます。リニア・レギュレータでのドロップアウト電圧は 0.8V で、電力損失を最小化できます。TPS652353 では、複数の方法で 22kHz 信号を生成できます。プッシュプル出力段を備えた内蔵のリニア・レギュレータは、22kHz トーン信号を生成し、負荷がゼロのときでも出力に重畳されます。リニア・レギュレータの電流制限は、外付け抵抗により ±10% の精度でプログラム可能です。I²C で読み取られる幅広い診断情報をシステム監視に使用可能です。

TPS652353 は、特に VIN が VLNB 出力に近いか超えている場合に可聴周波数のノイズを回避するため、PWM モードで特殊な設計が使用されています。

TPS652353 は、22kHz のトーン検出回路と出力インターフェイスにより、先進の DiSEqC 2.x 規格をサポートしています。

パッケージ情報

部品番号	パッケージ	本体サイズ (公称)
TPS652353	RUK (WQFN、20)	3.00mm x 3.00mm



簡略回路図

Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (January 2023) to Revision D (May 2023)	Page
• Updated the ADDR pin voltage range for I^2C address 0x11 in 表 7-4	18

Changes from Revision B (May 2021) to Revision C (January 2023)	Page
• Update the ESD table to be in accordance with standards	4
• Changed all instances of legacy terminology to controller and target where I^2C is mentioned	18
• Added description of Control Register 2 Bit 6 in 表 7-6	20

Changes from Revision A (December 2019) to Revision B (May 2021)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新	1
• Changed $V_{(drop)}$ min and max values	5
• Changed $I_{(rev\_dis)}$ min and max values	5

Changes from Revision * (December 2019) to Revision A (December 2019)	Page
• マーケティング・ステータスを「事前情報」から「量産データ」に変更。	1

5 Pin Configuration and Functions

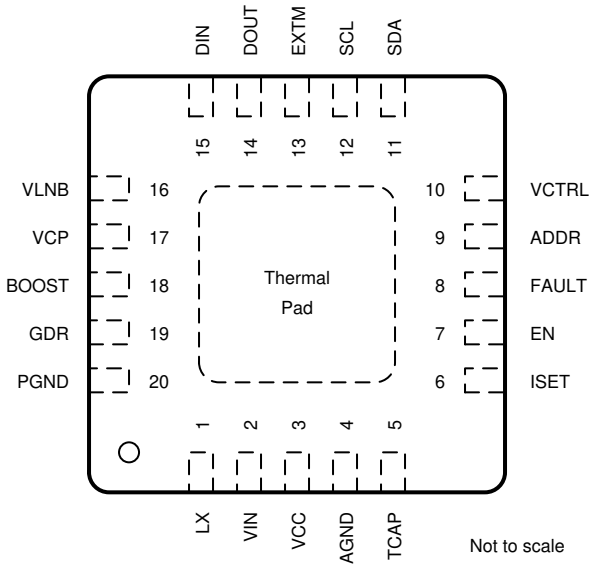


図 5-1. RUK Package. 20-Pin WQFN With Exposed Thermal Pad. Top View.

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	LX	I	Switching node of the boost converter
2	VIN	S	Input of internal linear regulator
3	VCC	O	Internal 6.3-V power supply. Connect a 1-µF ceramic capacitor from this pin to ground. When V_{IN} is 5 V, connect the VCC pin to the VIN pin.
4	AGND	S	Analog ground. Connect all ground pins and power pad together.
5	TCAP	O	Connect a capacitor to this pin to set the rise time of the LNB output.
6	ISET	O	Connect a resistor to this pin to set the LNB output current limit.
7	EN	I	Enable this pin to enable the VLNB output. pull this pin to ground to disable the output. The output is then pulled to ground, and, when the EN pin is low, the I^2C interface can be accessed.
8	FAULT	O	Open drain output pin, it goes low if any fault flag is set.
9	ADDR	I	Connect a different resistor to this pin to set different I^2C addresses (see the *I^2C Address Selection* 表 7-4 table).
10	VCTRL	I	Voltage level at this pin to set the output voltage (see the *Logic table* 表 7-3).
11	SDA	I/O	I^2C compatible bidirectional data
12	SCL	I	I^2C compatible clock input
13	EXTM	I	External modulation logic input pin that activates the 22-kHz tone output. The feeding signal can be 22-kHz tone or logic high or low.
14	DOUT	O	Tone detection output
15	DIN	I	Tone detection input
16	VLNB	O	Output of the power supply connected to satellite receiver or switch
17	VCP	O	Gate drive supply voltage and output of charge pump. Connect a capacitor between this pin and the VLNB pin.
18	BOOST	O	Output of the boost regulator and Input voltage of the internal linear regulator
19	GDR	O	Control the gate of the external MOSFET for DiSEqc 2.x support
20	PGND	S	Power ground for the boost converter
—	Thermal Pad	—	The thermal pad must be soldered to the printed circuit board (PCB) for optimal thermal performance. Use thermal vias on the PCB to enhance power dissipation.

(1) I = input, O = output, I/O = input and output, S = power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	VIN, LX, BOOST, VLNB	–1	30	V
	VCP, GDR (referenced to VLNB pin)	–0.3	7	
	VCC, EN, ADDR, FAULT, SCL, SDA, VCTRL, EXTM, DOUT, DIN, TCAP	–0.3	7	
	ISET	–0.3	3.6	
	PGND	–0.3	0.3	
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–55	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input operating voltage	4.5		20	V
T_A	Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS652353 RUK (WQFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	44.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	16.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

–40°C ≤ T_J ≤ 125°C, V_{IN} = 12 V, f_{SW} = 1 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{IN}	Input voltage range		4.5	12	20	V
$I_{DD(SDN)}$	Shutdown supply current	EN = 0b	90	120	150	µA
$I_{LDO(Q)}$	LDO quiescent current	EN = 1b, I_O = 0 A, V_{VLNB} = 18.2 V	1.5	5	8.5	mA
UVLO	V_{IN} undervoltage lockout	V_{IN} rising	4.15	4.3	4.45	V
		Hysteresis	280	480	550	mV
OUTPUT VOLTAGE						
V_{OUT}	Regulated output voltage	$V_{(ctrl)}$ = 1, I_O = 500 mA	18	18.2	18.4	V
		$V_{(ctrl)}$ = 0, I_O = 500 mA	13.25	13.4	13.55	V
		SCL = 1b, $V_{(ctrl)}$ = 1, I_O = 500 mA (Non I^2C)	19.18	19.4	19.62	V
		SCL = 1b, $V_{(ctrl)}$ = 0, I_O = 500 mA (Non I^2C)	14.44	14.6	14.76	V
$I_{(OCP)}$	Output short circuit current limit	$R_{(SET)}$ = 200 kΩ, Full temperature	580	650	720	mA
		T_J = 25°C	629	650	688	mA
f_{SW}	Boost switching frequency	f = 1 MHz	977	1060	1134	kHz
$I_{(limitsw)}$ (1)	Switching current limit	V_{IN} = 12 V, V_{OUT} = 18.2 V, $R_{(SET)}$ = 200 kΩ		3		A
$R_{ds(on)\_LS}$	On resistance of low side FET	V_{IN} = 12 V	90	140	210	mΩ
$V_{(drop)}$	Linear regulator voltage dropout	I_O = 500 mA, TONEAMP = 0b	0.44	0.8	1.15	V
		I_O = 500 mA, TONEAMP = 1b	0.55	0.9	1.2	V
$I_{(cable)}$	Cable good detection current threshold	V_{IN} = 12 V, V_{OUT} = 13.4 V or 18.2 V	0.9	5	8.8	mA
$I_{(rev)}$	Reverse bias current	EN = 1b, V_{VLNB} = 21 V	49	58	65	mA
$I_{(rev\_dis)}$	Disabled reverse bias current	EN = 0b, V_{VLNB} = 21 V	2.9	4.6	6.3	mA
LOGIC SIGNALS						
	Enable threshold ($V_{(EN)}$), high		1.6			V
	Enable threshold ($V_{(EN)}$), low				0.8	V
$I_{(EN)}$	Enable internal pullup current	$V_{(EN)}$ = 1.5 V	5	6	7	µA
		$V_{(EN)}$ = 1 V	2	3	4	µA
$V_{(VCTRL\_H)}$	VCTRL logic threshold level for high-level input voltage		2			V
$V_{(VCTRL\_L)}$	VCTRL logic threshold level for low-level input voltage				0.8	V
$V_{(EXTM\_H)}$	EXTM logic threshold level for high-level input voltage		2			V
$V_{(EXTM\_L)}$	EXTM logic threshold level for low-level input voltage				0.8	V
$V_{OL(FAULT)}$	FAULT output low voltage	FAULT open drain, I_{OL} = 1 mA			0.4	V
TONE						
$f_{(tone)}$	Tone frequency	22-kHz tone output	20	22	24	kHz
$A_{(tone)}$	Tone amplitude	0 mA ≤ I_O ≤ 500 mA, C_O = 100 nF, TONEAMP = 0b	617	650	696	mV
		0 mA ≤ I_O ≤ 500 mA, C_O = 100 nF, TONEAMP = 1b	703	750	803	mV
$D_{(tone)}$	Tone duty cycle		45%	50%	55%	
$f_{(EXTM)}$	External tone input frequency range	22-kHz tone output	17.6	22	26.4	kHz
		44-kHz tone output	35.2	44	52.8	kHz
TONE DETECTION						
$f_{(DIN)}$	Tone detector frequency capture range	0.4-V_{PP} sine wave	17.6	22	26.4	kHz
$V_{(DIN)}$	Tone detector input amplitude	Sine wave, 22 kHz	0.3		1.5	V

6.5 Electrical Characteristics (continued)

–40°C ≤ T_J ≤ 125°C, V_{IN} = 12 V, f_{SW} = 1 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(DOUT)}$	DOUT output voltage	Tone present, I_{load} = 2 mA			0.4	V
GDR	Bypass FET gate voltage, LNB	TONE_TRANS = 1b, $V_{(LNB)}$ = 18.2 V	23.11	23.5	24.33	V
		TONE_TRANS = 0b, $V_{(LNB)}$ = 18.2 V	18.17	18.2	18.23	V
THERMAL SHUT-DOWN (JUNCTION TEMPERATURE)						
$T_{(TRIP)}$	Thermal protection trip point	Temperature rising		160		°C
$T_{(HYST)}$	Thermal protection hysteresis			20		°C
I²C READ BACK FAULT STATUS						
$V_{(PGOOD)}$	PGOOD trip levels	Feedback voltage UVP low	94%	96%	97.1%	
		Feedback voltage UVP high	93%	94.5%	95.5%	
		Feedback voltage OVP high	104%	106.6%	108%	
		Feedback voltage OVP low	102%	104.6%	106%	
$T_{(warn)}$	Temperature warning threshold			125		°C
I²C INTERFACE						
V_{IH}	SDA,SCL input high voltage		2			V
V_{IL}	SDA,SCL input low voltage				0.8	V
I_I	Input current	SDA, SCL, 0.4 V ≤ V_I ≤ 4.5 V	–10		10	µA
V_{OL}	SDA output low voltage	SDA open drain, I_{OL} = 2 mA			0.4	V
$f_{(SCL)}$	Maximum SCL clock frequency		400			kHz

(1) Specified by design

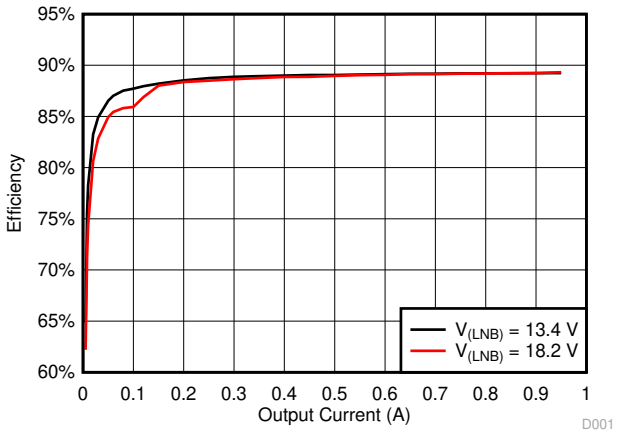
6.6 Timing Requirements

			MIN	NOM	MAX	UNIT
OUTPUT VOLTAGE						
t_r, t_f	13-V to 18-V transition rising falling time	$C_{(TCAP)}$ = 22 nF		2		ms
$t_{ON(min)}$	Minimum on time for the Low side FET		75	102	130	ns
TONE						
$t_{r(tone)}$	Tone rise time	0 mA ≤ I_O ≤ 500 mA, C_O = 100 nF, Control Reg1[0] = 0b		11		µs
		0 mA ≤ I_O ≤ 500 mA, C_O = 100 nF, Control Reg1[0] = 1b, and EXTM has 44-kHz input		5.5		µs
$t_{f(tone)}$	Tone fall time	0 mA ≤ I_O ≤ 500 mA, C_O = 100 nF, Control Reg1[0] = 0b		10.8		µs
		0 mA ≤ I_O ≤ 500 mA, C_O = 100 nF, Control Reg1[0] = 1b, and EXTM has 44 kHz input		5.4		µs
OVERCURRENT PROTECTION						
t_{ON}	Overcurrent protection ON time	TIMER = 0b	25	29	33	ms
t_{OFF}	Overcurrent protection OFF time	TIMER = 0b	208	233	260	ms
I²C INTERFACE						
t_{BUF}	Bus free time between a STOP and START condition		1.3			µs
t_{HD_STA}	Hold time (repeated) START condition		0.6			µs
t_{SU_STO}	Setup time for STOP condition		0.6			µs
t_{LOW}	LOW period of the SCL clock		1			µs
t_{HIGH}	HIGH period of the SCL clock		0.6			µs
t_{SU_STA}	Setup time for a repeated START condition		0.6			µs
t_{SU_DAT}	Data setup time		0.1			µs
t_{HD_DAT}	Data hold time		0		0.9	µs
t_{RCL}	Rise time of SCL signal	Capacitance of one bus line (pF)	20 + 0.1 C_B		300	ns

			MIN	NOM	MAX	UNIT
t_{RCL1}	Rise time of SCL Signal after a Repeated START condition and after an acknowledge BIT	Capacitance of one bus line (pF)	20 + 0.1 C_B		300	ns
t_{FCL}	Fall time of SCL signal	Capacitance of one bus line (pF)	20 + 0.1 C_B		300	ns
t_{RDA}	Rise time of SDA signal	Capacitance of one bus line (pF)	20 + 0.1 C_B		300	ns
t_{FDA}	Fall time of SDA signal	Capacitance of one bus line (pF)	20 + 0.1 C_B		300	ns
C_B	Capacitance of one bus line(SCL and SDA)				400	pF

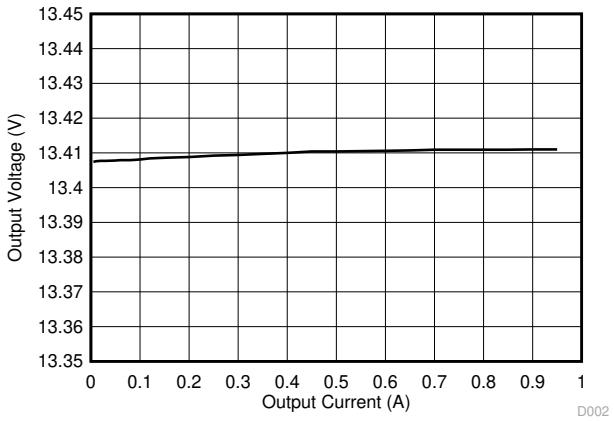
6.7 Typical Characteristics

T_J = 25°C, V_{IN} = 12 V, f_{SW} = 1 MHz, C_{Boost} = (2 × 22 µF / 35 V) (unless otherwise noted)



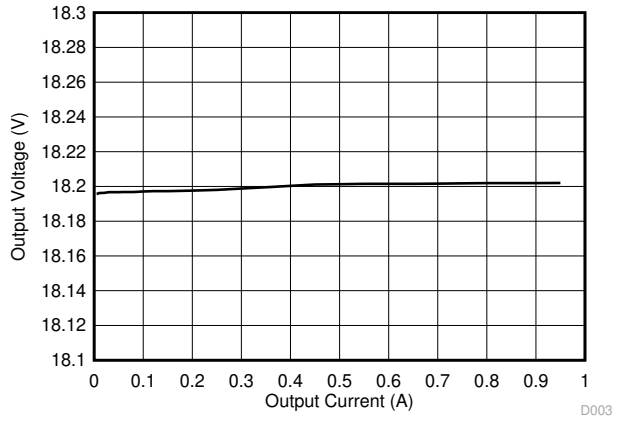
L = 4.7 µH

図 6-1. Power Efficiency



V_{VLNB} = 13.4 V

図 6-2. Load Regulation



V_{VLNB} =18.2 V

図 6-3. Load Regulation

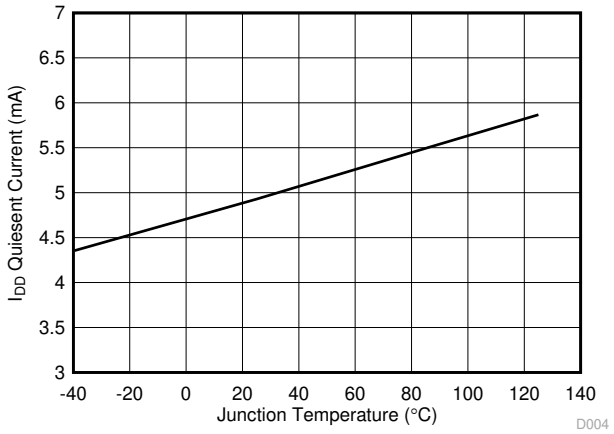


図 6-4. Input Supply Quiescent Current vs Junction Temperature

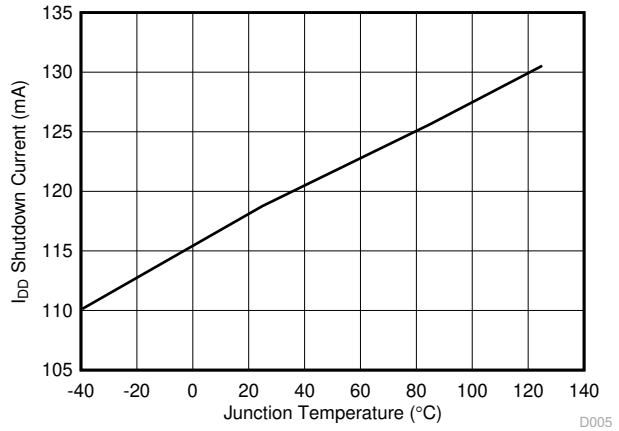
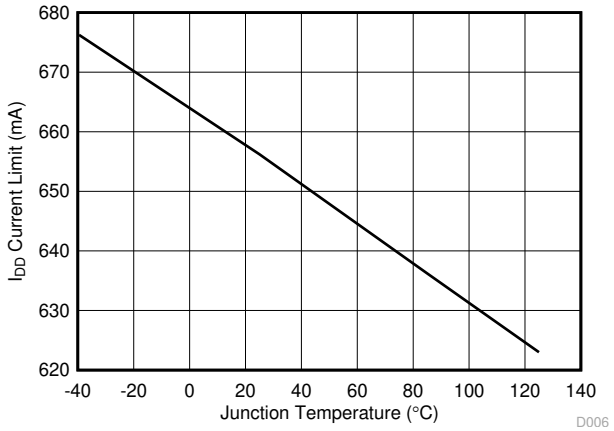


図 6-5. Shutdown Current vs Junction Temperature



I_{LOAD} = 650 mA

図 6-6. LNB Current Limit vs Junction Temperature

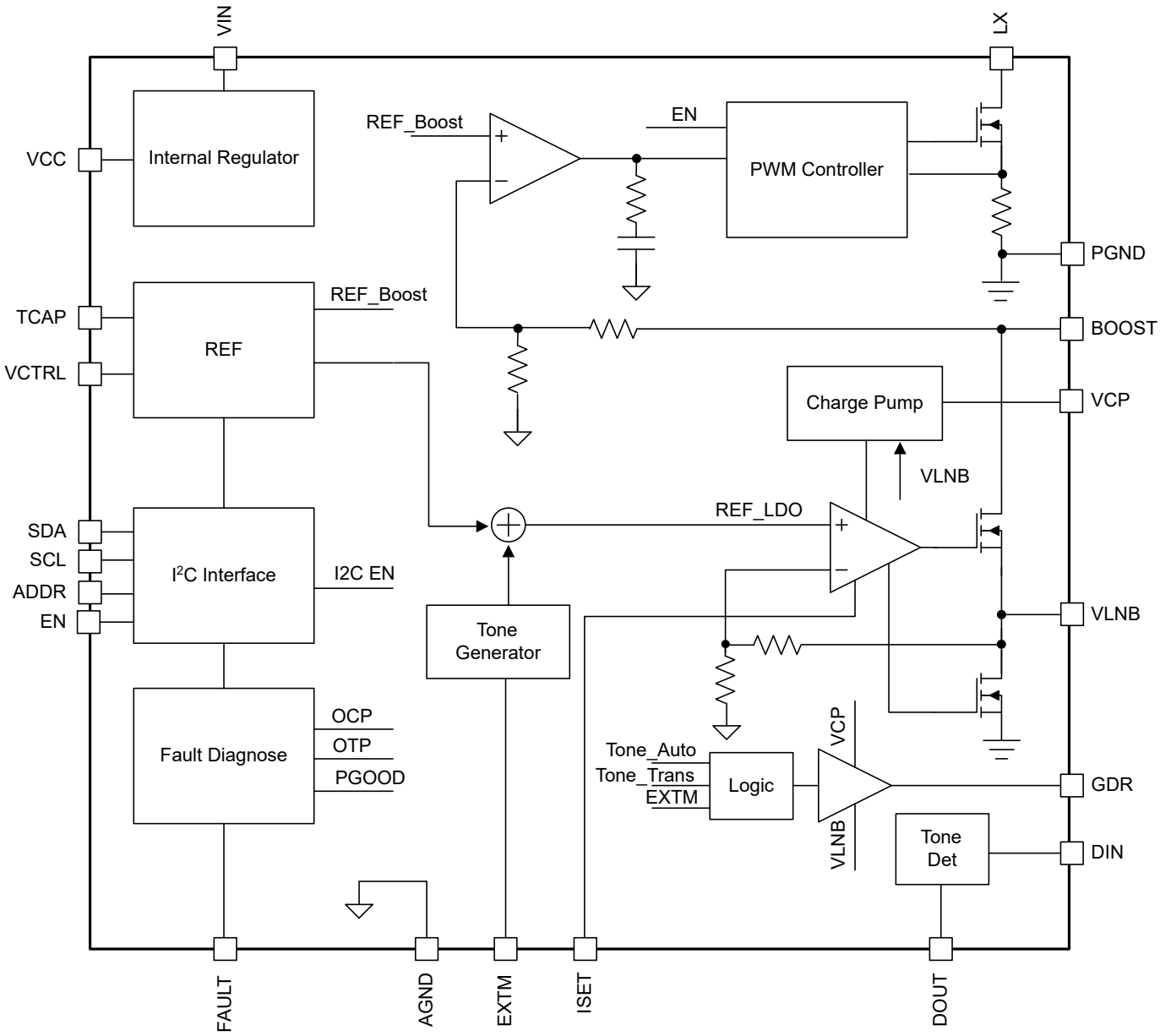
7 Detailed Description

7.1 Overview

The TPS652353 device is the power management IC (PMIC) that integrates a boost converter, an LDO regulator, and a 22-kHz tone generator to serve as a LNB power supply. This solution compiles the DiSEqC 2.x standard with or without I^{2}C interface. An external resistor allows for precise programming of the output current limit. The 22-kHz tone signal can be generated in one of two ways, either with or without I^{2}C. The integrated boost features low $R_{ds(on)}$ MOSFET and internal compensation. A selectable switching frequency of 1 MHz or 500 kHz is designed to reduce the size of passive components and be flexible for design.

The TPS652353 device can support the 44-kHz tone output. When the EXTM pin has a 44-kHz tone input, and the EXTM TONE bit in the *Control Register 1* is set to 1b, the LNB tone output is 44 kHz. By default, the TPS652353 device has a typical 22-kHz tone output.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Boost Converter

The TPS652353 device has an internal compensated boost converter and low-dropout (LDO) linear regulator. The boost converter tracks the LNB output voltage within 800 mV even at loading 1000 mA, which minimizes power loss.

The boost converter operates at 1 MHz by default. The TPS652353 device has internal cycle-by-cycle peak current limit in the boost converter and DC current limit in the LNB output to help protect the device from short circuits and over loading. When the LNB output is shorted to ground, the LNB output current is clamped at the LDO current limit. The LDO current limit is set by the external resistor at the ISET pin. The current limit of the boost switch is proportional to the LDO current limit. If an overcurrent condition occurs for more than 29 ms, the boost converter enters hiccup mode and retries startup in 233 ms. This hiccup mode ON time and OFF time are selectable through the I^2C control register (address 0x01) to be either 29 ms and 233 ms or 58 ms and 466 ms, respectively. At extremely light loads, the boost converter automatically operates in a pulse-skipping mode.

The boost converter is stable with either ceramic capacitor or electrolytic capacitor.

If two or more set-top box LNB outputs are connected together, one output voltage can be set higher than others. The output with the lower set voltage is then effectively turned off. When the voltage drops to the set level, the LNB output with the lower set output voltage returns to normal conditions.

7.3.2 Linear Regulator and Current Limit

The linear regulator is used to generate the 22-kHz tone signal by changing the LDO reference voltage. The linear regulator features low-dropout voltage to minimize power loss while maintaining enough head room for the 22-kHz tone with 650-mV amplitude. The linear regulator also implements a tight current limit for overcurrent protection. The current limit is set by an external resistor connected to ISET pin. Linear Regulator Current Limit Vs Resistor shows the relationship between the current limit threshold and the resistor value.

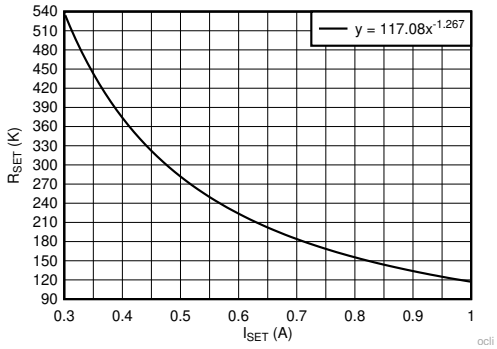


図 7-1. Linear Regulator Current Limit Vs Resistor

$$R_{SET}\,(k\Omega) = 117.08 \times I_{SET}{}^{-1.267}\,(A) \quad (1)$$

A 200-kΩ resistor sets the current to 0.65 A, and 110-kΩ resistor sets the current to approximately 1 A.

7.3.3 Boost Converter Current Limit

The boost converter has the cycle-by-cycle peak current limit on the internal Power MOSFET switch to serve as the secondary protection when LNB output is hard short. With ISW bit default setting 0b on I^2C control register 0x01, the switch current limit I_{SW} is proportional as LDO current limit $I_{(OCP)}$ set by ISET pin resistor, and the relationship can be expressed as:

$$I_{SW} = 3 \times I_{(OCP)} + 0.8\,A \quad (2)$$

For the 5 V V_{IN}, if LNB current load is up to 1 A, the ISW bit should be written as 1b, the switch current limit I_{SW} for the internal Power MOSFET is:

$$I_{SW} = 5 \times I_{(OCP)} + 0.8\,A \quad (3)$$

While due to the high power loss at 5 V, V_{IN}, it has a chance to trigger the thermal shutdown before the loading is up to 1 A, especially the VLNB output is high.

7.3.4 Charge Pump

The charge pump circuitry generates a voltage to drive the NMOS of the linear regulator. The voltage across the charge pump capacitor between VLNB and VCP is about 5.4 V, so the absolute value of the VCP voltage will be VLNB + 5.4 V.

7.3.5 Slew Rate Control

When LNB output voltage transits from 13.4 V to 18.2 V or 18.2 V to 13.4 V , the cap at pin TCAP controls the transition time. This transition time makes sure the boost converter output to follow LNB output change. Usually boost converter has low bandwidth and can't response fast. The voltage at TCAP acts as the reference voltage of the linear regulator. The boost converter's reference is also based on TCAP with additional fixed voltage to generate a 0.8 V above the LNB output.

The charging and discharging current is 10 µA, thus the transition time can be estimated as:

$$t_{TCAP}\,(ms) = 0.8 \times \frac{C_{SS}\,(nF)}{I_{SS}\,(\mu A)} \quad (4)$$

A 22-nF capacitor generates about 2 ms transition time.

In light load conditions, when LNB output voltage is set from 18.2 V to 13.4 V, the voltage drops very slow, which causes wrong VOUT_GOOD (Bit 0 at status register 0x02) logic for LNB output voltage detection. TPS652353 has integrated a pull down circuit to pull down the output during the transition. This ensures the voltage change can follow the voltage at TCAP. When the 22-kHz tone signal is superimposing on the LNB output voltage, the pull down current can also provide square wave instead of a distorted waveforms.

7.3.6 Short Circuit Protection, Hiccup and Overtemperature Protection

The LNB output current limit can be set by an external resistor. When short circuit conditions occur or current limit is triggered, the output current is clamped at the current limit for 29 ms or 58 ms with LDO on. If the condition retains, the converter will shut down for 233 ms or 466 ms and then restart. This hiccup behavior prevents IC from being overheat. The hiccup ON/OFF time can be set by I^2C register. Refer to *Control Register 1* for detail.

The low side MOSFET of the boost converter has a peak current limit threshold which serves as the secondary protection. If boost converter's peak current limit is triggered, the peak current will be clamped as high as 3.8 A when setting I_{SW} default and LNB current limit up to 1 A. If loading current continues to increase, output voltage starts to drop and output power drops.

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the junction temperature exceeds 160°C, the output shuts down. When the die temperature drops below its lower threshold typically 140°C, the output is enabled.

When the chip is in overcurrent protection or thermal shutdown, the I^2C interface and logic are still active. The FAULT pin is pulled down to signal the processor. The FAULT pin signal remains low unless the following action is taken:

1. If I^2C interface is not used to control, EN pin must be recycled to pull the FAULT pin back to high.
2. If I^2C interface is used, the I^2C controller need to read the status *Control Register 2*, then the FAULT pin will be back to high.

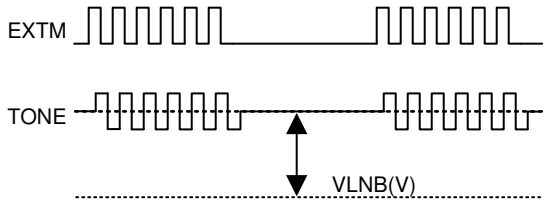
7.3.7 Tone Generation

A 22-kHz tone signal is implemented at the LNB output voltage as a carrier for DiSEqC command. This tone signal can be generated by feeding an external 22-kHz clock at the EXTM pin, and it can also be generated with its internal tone generator controlled by EXTM pin. If EXTM pin is toggled to high, the internal tone signal will be

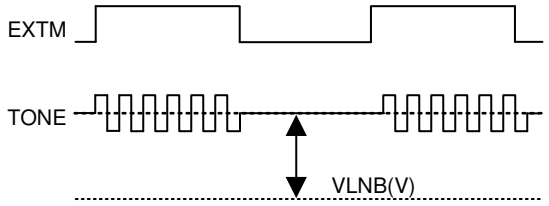
superimposed at the LNB output, if EXTM pin is low, there will be no tone superimposed at the output stage of the regulator facilitates a push-pull circuit, so even at zero loading; the 22-kHz tone at the output is still clean without distortion.

There are two ways to generate the 22-kHz tone signal at the output.

For option1, if the EXTM has 44-kHz tone input, and the bit EXTM TONE of the *Control Register 1* is set to 1b, the LNB tone output is 44 kHz.



Option 1. Use external tone, gated by EXTM logic pulse



Option 2. Use internal tone, gated by EXTM logic envelop

図 7-2. Two Ways to Generate 22-kHz tone

7.3.8 Tone Detection

A 22-kHz tone detector is implemented in the TPS652353 solution. The detector extracts the AC-coupled tone signal from the DIN input and provides it as an open-drain signal on the DOUT pin. When the DOUTMODE bit in the *Control Register 2* is set to the default setting, if a tone is present, the DOUT output is logic low. If a tone is not present, the internal output FET is off. If a pullup resistor is connected to the DOUT pin, the output is logic high. The maximum tone out delay with respect to the input is one and a half of the tone cycle.

The DOUTMODE bit in the *Control Register 2* is reserved and should not be used.

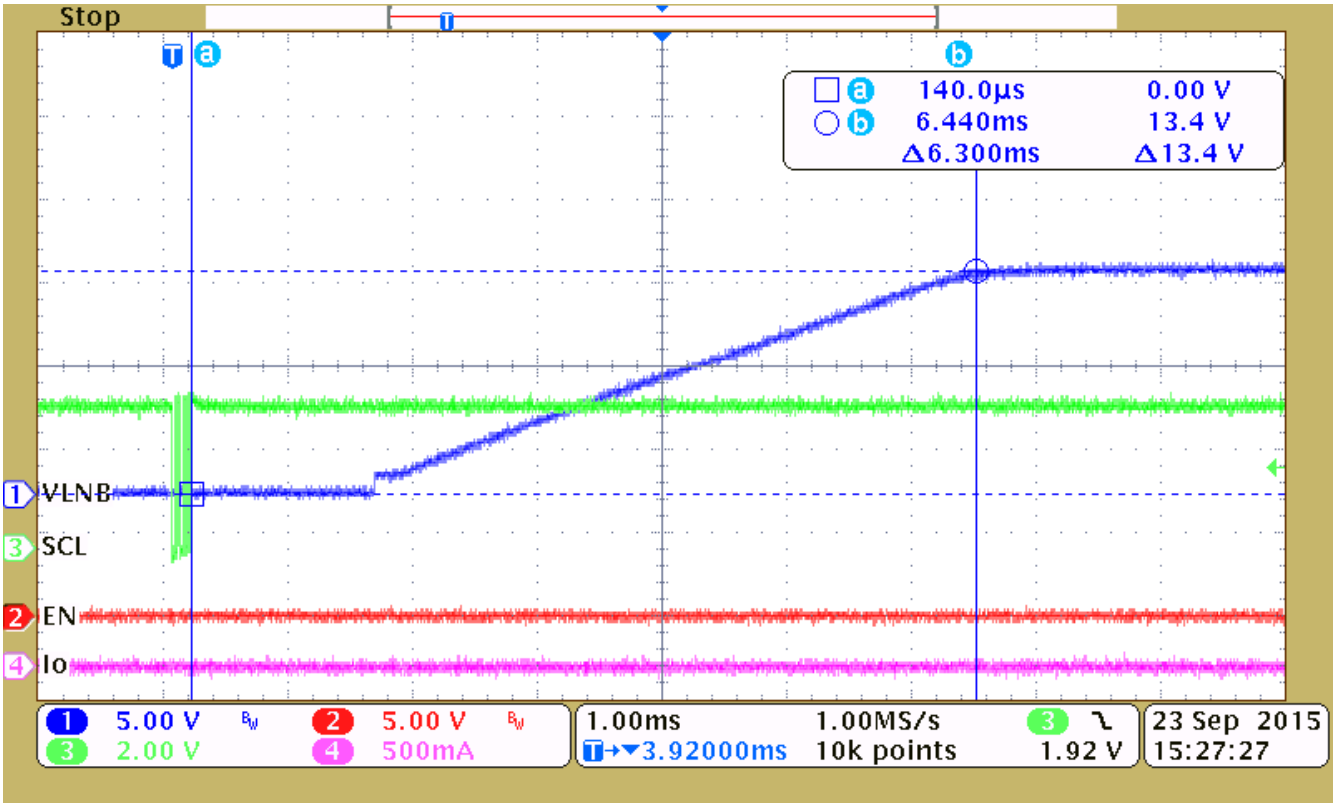
7.3.9 Audio Noise Rejection

When the TPS652353 operates in PSM mode, locating the switching frequency at the range of audio frequency is possible. Which causes audible noise, especially when the VLNB voltage is lower or closer to the VIN voltage, and the current load is light.

When audible noise occurs, setting the TPS652353 device to operate in Forced PWM mode is recommended. In Forced PWM mode, a special design is implemented to avoid the audible noise.

7.3.10 Disable and Enable

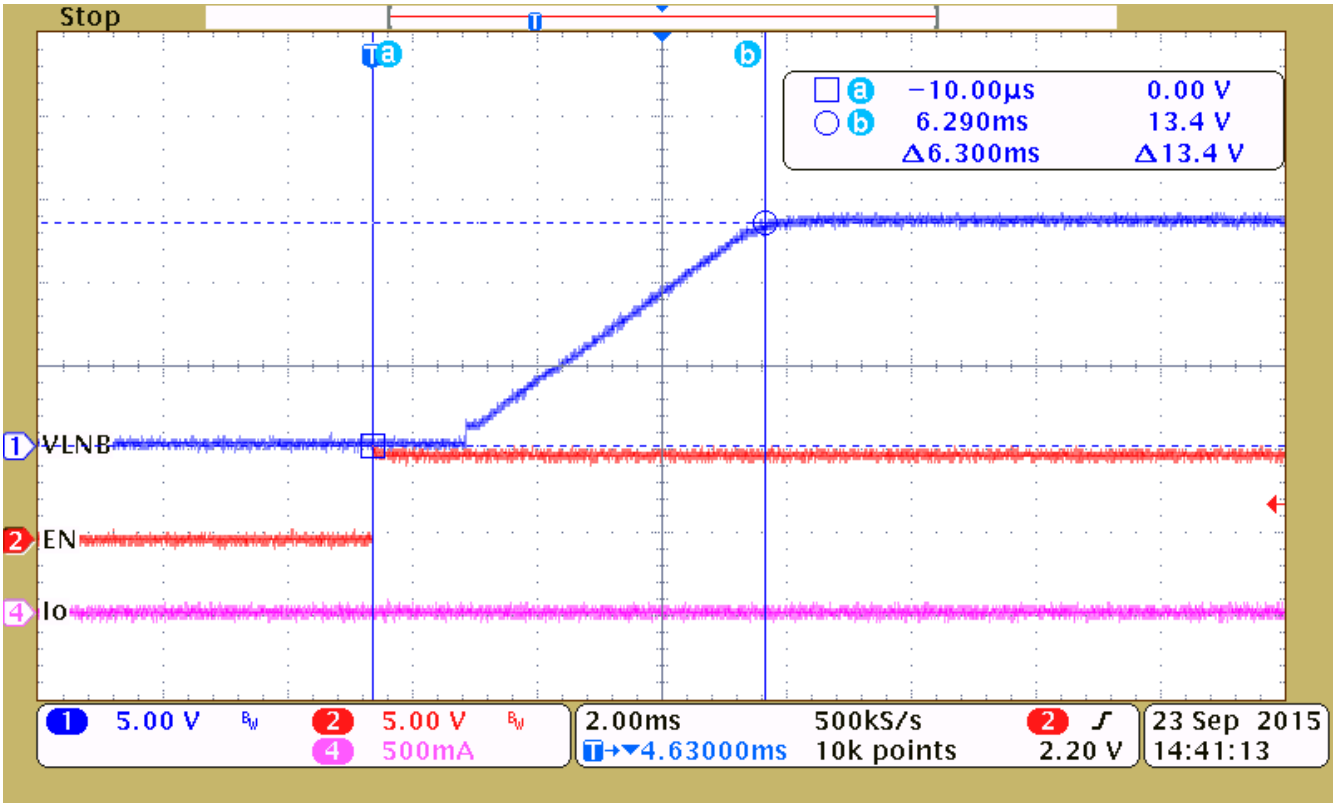
The TPS652353 device has a dedicated EN pin to disable and enable the LNB output. In a non-I^2C application, when the EN pin is pulled high, the LNB output is enabled. When the EN pin is pulled low, the LNB output is disabled. In an I^2C application, when the EN pin is either low or high, the I^2C registers can be accessed, which allows users to change the default LNB output at system power-up. When the I2C_CON bit in the *Control Register 1* is set to 1b, the LNB output enable or disable is controlled by the EN bit in the *Control Register 2*. By default, the I2C_CON bit of the control register is set to 0b, which makes the LNB output is controlled by the EN pin. 図 7-3 and 図 7-4 shows the detailed control behavior.



注

$V_{(EN)}$ = 0 V　　I2C_CON = 1b

図 7-3. VLNB Output Controlled by bit EN of Control Register 2



注

I2C_CON = 0b

図 7-4. VLNB Output Controlled by EN Pin

7.3.11 Component Selection

7.3.11.1 Boost Inductor

The TPS652353 device is recommended to operate with a boost inductor value of 4.7 µH or 10 µH. The boost inductor must be able to support the peak current requirement to maintain the maximum LNB output current without saturation. Use 式 5 to estimate the peak current of the boost inductor (I_{peak}).

$$I_{peak} = \frac{I_{OUT}}{1 - D} + \frac{1}{2} \times \frac{V_{IN} \times D}{L \times f_S} \quad (5)$$

where

$$D = 1 - \frac{V_{IN}}{VLNB + 0.8} \quad (6)$$

With a different inductance, the system has different gain and phase margins. 図 7-5 shows a Bode plot of boost loop with 2 × 10 µF / 35 V of boost capacitor and 4.7 µH, 5.6 µH, 6.8 µH, 8.2 µH, and 10 µH of boost inductance. As the boost inductance increases, the 0-dB crossover frequency keeps relatively constant while reducing the phase and gain margins. With a 4.7-µH boost inductance, the phase margin is 66.96° and with a 10-µH inductance, the phase margin is 39.63°.

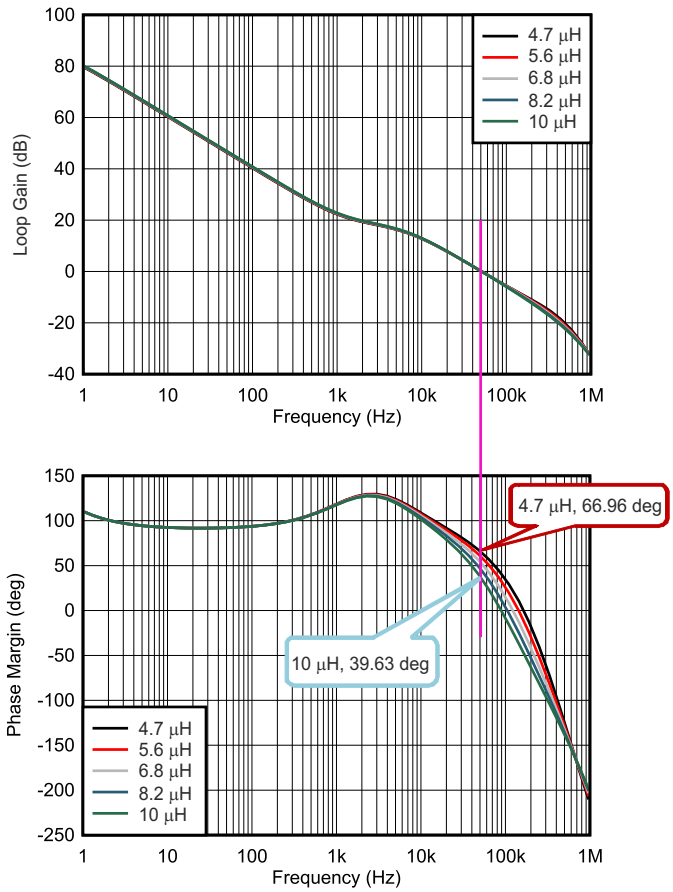


図 7-5. Gain and Phase Margin of the Boost Loop with Different Inductance (V_{IN} = 12 V, V_{OUT} = 18.2 V, I_{LOAD} = 1 A, f_{SW} = 1 MHz, 5 µF, Typical Bode Plot)

7.3.11.2 Capacitor Selection

The TPS652353 device has a 1-MHz nonsynchronous boost converter integrated and the boost converter features the internal compensation network. The TPS652353 device works well with both ceramic capacitor and electrolytic capacitor.

The recommended ceramic capacitors for the TPS652353 application are, at the minimum, rated as X7R/X5R, with a 35-V rating, and a 1206 size for the achieving lower LNB output ripple. 表 7-1 lists the recommended ceramic capacitors list for both 4.7-µH and 10-µH boost inductors.

If more cost-effictive design is needed, use a 100-µF electrolytic (low ESR) and a 10-µF or 35-V ceramic capacitor.

表 7-1. Boost Inductor and Capacitor Selections

BOOST INDUCTOR	CAPACITORS	TOLERANCE (%)	RATING (V)	SIZE
10 µH	2 × 22 µF	±10	35	1206
	2 × 10 µF	±10	35	1206
4.7 µH	2 × 22 µF	±10	35	1206
	2 × 10 µF	±10	35	1206
	22 µF	±10	35	1206

図 7-6 and 図 7-7 show a bode plot of boost loop with 4.7-µH and 10-µH inductance and 4 µF, 5 µF, 7.5 µF, 10 µF, 15 µF, and 20 µF of boost capacitance after degrading. As the boost capacitance increases, the phase margin increases.

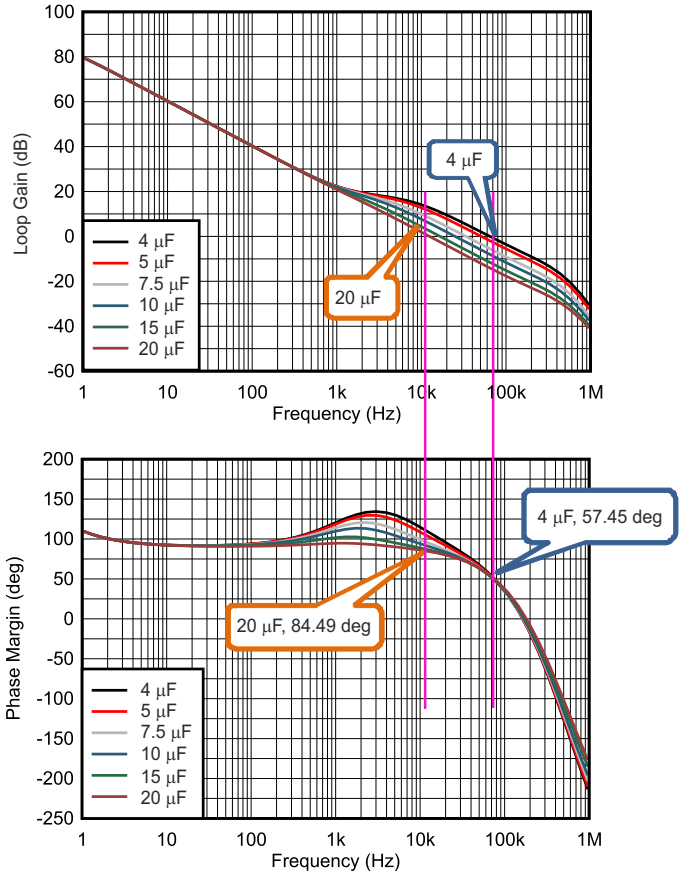


図 7-6. Gain and Phase Margin of the Boost Loop With Different Boost Capacitance (V_{IN} = 12 V, V_{OUT} = 18.2 V, I_{LOAD} = 1 A, f_{SW} = 1 MHz, 4.7 µH, Typical Bode Plot)

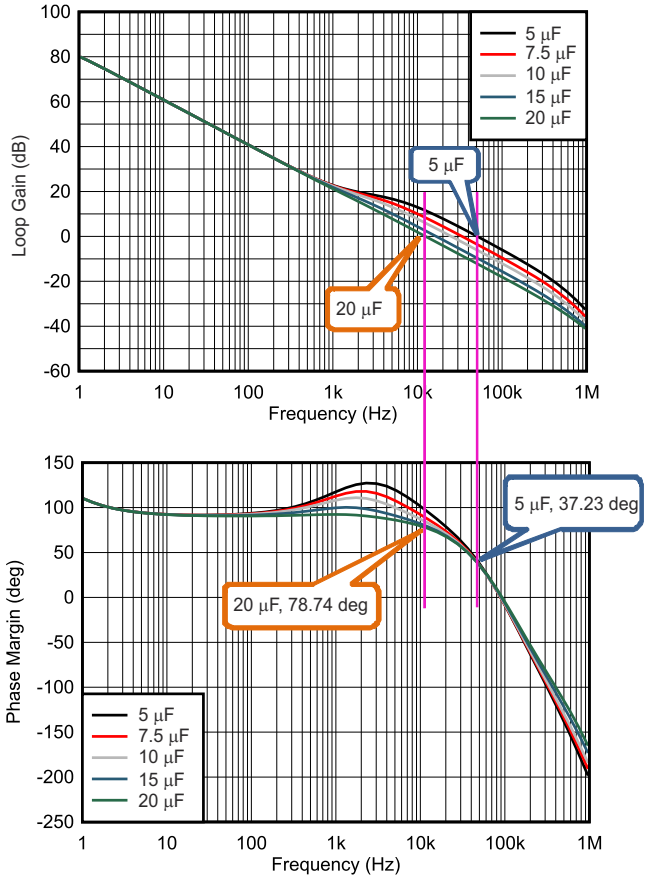


図 7-7. Gain and Phase Margin of the Boost Loop With Different Boost Capacitance (V_{IN} = 12 V, V_{OUT} =18.2 V, I_{LOAD} = 1 A, f_{SW} = 1 MHz, 10 µH, Typical Bode Plot)

7.3.11.3 Surge Components

If a surge test is required for the application, the D0 and D2 diodes should be added as the external protection components. If no surge test is required, remove the D0 and D2 diodes. 表 7-2 lists the recommended surge components.

表 7-2. Surge Components

DESIGNATOR	DESCRIPTION	PART NUMBER	MANUFACTURER (1)
D0	Diode, TVS, Uni, 28 V, 1500 W, SMC	SMCJ28A	Fairchild Semiconductor
D2	Diode, Schottky, 40 V, 2 A, SMA	B240A-13-F	Diodes Inc.

(1) See *Third-party Products Disclaimer*

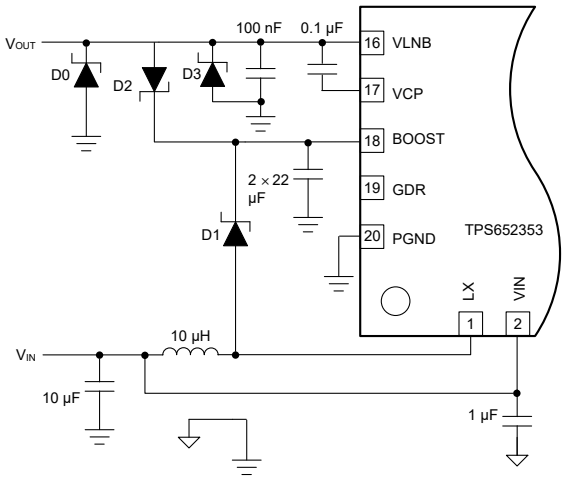


図 7-8. Surge Components Selection

7.3.11.4 Consideration for Boost Filtering and LNB Noise

Smaller capacitance on the BOOST pin reduces the cost of the system. However, when the inductor in system is the same, the smaller capacitance on the boost and the larger ripple on the LNB output.

7.4 Device Functional Modes

表 7-3 is the logic table for the device.

表 7-3. Logic table

EN	I2C_CON(1) (2) (3)	SCL	VCTRL	VLNB(4)
H	0	H	H	19.4 V
H	0	H	L	14.6 V
H	0	L	H	18.2 V
H	0	L	L	13.4 V
X	1	X	X	Controlled by VSET[3:0] bits at 0x01 register(5)
L	0	X	X	0 V

(1) I2C_CON is the bit7 of the I²C control register 0x01, which is used to set the VLNB output controlled by the I²C register or not.
(2) When I²C interface is used in design, all the I²C registers are accessible even if the I2C_CON bit is 0b.
(3) When I2C_CON is 1b, the VLNB output is controlled by the I²C control register even if the EN pin is low.
(4) When I²C interface is used in design, it is recommended to set the I2C_CON with 1b, if not, the LNB output will be variable because the SCL is toggled by the I²C register access as the clock signal.
(5) Bit EN of the control register2 is used to disable or enable the LNB output, by default , the bit EN is 1b which enable the LNB output.

7.5 Programming

7.5.1 Serial Interface Description

I²C is a 2-wire serial interface developed by Philips Semiconductor (see I²C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is idle, both SDA and SCL lines are pulled high external. All the I²C compatible devices connect to the I²C bus through open drain I/O pins, SDA and SCL. A controller device, usually a microcontroller (MCU) or a digital signal processor (DSP), controls the bus. The controller device is responsible for generating the SCL signal and device addresses. The controller device also generates specific conditions that indicate the START and STOP of data transfer. A target device receives, transmits data, or both on the bus under control of the controller device.

The TPS652353 device works as a target and supports the following data transfer modes, as defined in the I²CBus Specification: standard mode (100 kbps), and fast mode (400 kbps). The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the

instantaneous application requirements. Register contents remain intact as long as supply voltage remains above 4.5 V (typical).

The data transfer protocol for standard and fast modes is exactly the same; therefore, they are referred to as F/S-mode in this document. The TPS652353 device supports 7-bit addressing; 10-bit addressing and general call address are not supported.

The TPS652353 device has a 7-bit address set by ADDR pin. 表 7-4 shows how to set the I²C address.

表 7-4. I²C Address Selection

ADDR PIN	I²C ADDRESS	ADDRESS FORMAT (A6 ≥ A0)
Connect to VCC	0x08	000 1000b
Floating	0x09	000 1001b
Connected to GND	0x10	001 0000b
Resistor divider to make ADDR pin voltage in 3.7 V - 5.9 V	0x11	001 0001b

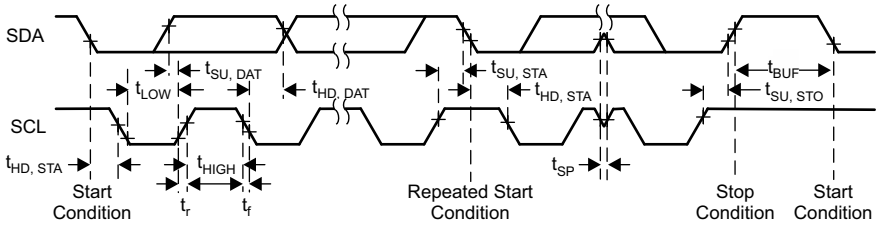


図 7-9. I²C Interface Timing Diagram

7.5.2 TPS652353 I²C Update Sequence

The TPS652353 requires a start condition, a valid I²C address, a register address byte, and a data byte for a single update. After the receipt of each byte, TPS652353device acknowledges by pulling the SDA line low during the high period of a single clock pulse. TPS652353 performs an update on the falling edge of the LSB byte.

When the TPS652353 is disabled (EN pin tied to ground) the device cannot be updated via the I²C interface.

図 7-10. I²C Write Data Format

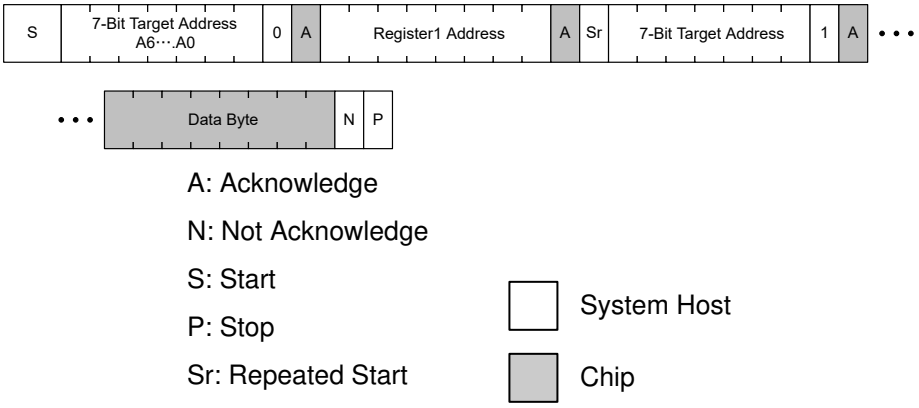


図 7-11. I²C Read Data Format

7.6 Register Maps

Control Register 1 (address = 0x00) [reset = 0x08]

図 7-12. Control Register 1

7	6	5	4	3	2	1	0
I2C_CON	PWM/PSM	RESERVED	VSET[3:0]				EXTM TONE
R/W-0b	R/W-0b	R/W-0b	R/W-0100b				R/W-0b

表 7-5. Control Register 1

Bit	Field	Type	Reset	Description
7	I2C_CON	R/W	0b	0b = I^2C control disabled 1b = I^2C control enabled
6	PWM/PSM	R/W	0b	0b = PSM at light load 1b = Forced PWM
5	RESERVED	R/W	0b	Reserved
4-1	VSET[3:0]	R/W	0100b	LNB output voltage selection 0000b = 11 V 0001b = 11.6 V 0010b = 12.2 V 0011b = 12.8 V 0100b = 13.4 V 0101b = 14 V 0110b = 14.6 V 0111b = 15.2 V 1000b = 15.8 V 1001b = 16.4 V 1010b = 17 V 1011b = 17.6 V 1100b = 18.2 V 1101b = 18.8 V 1110b = 19.4 V 1111b = 21 V
0	EXTM TONE	R/W	0b	0b = EXTM 44-kHz tone input not support, with only 22-kHz tone output at VLNB 1b = EXTM 44-kHz tone input support, with 44-kHz tone output at VLNB

Control Register 2 (address = 0x01) [reset = 0x09]

図 7-13. Control Register 2

7	6	5	4	3	2	1	0
TONEAMP	TIMER	I_{SW}	FSET	EN	DOUTMODE	TONE_AUTO	TONE_TRANS
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-1b	R/W-0b	R/W-0b	R/W-1b

表 7-6. Control Register 2

Bit	Field	Type	Reset	Description
7	TONEAMP	R/W	0b	0b = 22-kHz tone amplitude is 650 mV (typ) 1b = 22-kHz tone amplitude is 750 mV (typ)

表 7-6. Control Register 2 (continued)

Bit	Field	Type	Reset	Description
6	TIMER	R/W	0b	0b = Hiccup ON time set to 29 ms and OFF time set to 233 ms 1b = Hiccup ON time set to 58 ms and OFF time set to 466 ms (If I_{SW} is set as 1A, recommend to set TIMER as 0b.)
5	I_{SW}	R/W	0b	0b = Boost switch peak current limit set to 3 × I_{OCP} + 0.8 A 1b = Boost switch peak current limit set to 5 × I_{OCP} + 0.8 A
4	FSET	R/W	0b	0b = 1-MHz switching frequency 1b = 500-kHz switching frequency
3	EN	R/W	1b	0b = LNB output disabled 1b = LNB output voltage Enabled
2	DOUTMODE	R/W	0b	0b = DOUT is kept to low when DIN has the tone input 1b = Reserved, cannot set to 1b
1	TONE_AUTO	R/W	0b	0b = GDR (External bypass FET control) is controlled by TONE_TRANS 1b = GDR (External bypass FET control) is automatically controlled by 22-kHz tones transmit
0	TONE_TRANS	R/W	1b	0b = GDR output with VLNB voltage for tone receive. Bypass FET is OFF for tone receiving from satellite 1b = GDR output with VCP voltage. Bypass FET is ON for tone transmit from TPS652353

表 7-7. 22-kHz Tone Receive Mode Selection

TONE_AUTO	TONE_TRANS	BYPASS FET
0b	0b	OFF
0b	1b	ON
1b	x	Auto Detect

The TPS652353 has full range of diagnostic flags for operation and debug. Processor can read the status register to check the error conditions. Once the error happens, the flags are changed, once the errors are gone, the flags are set back without I^2C access.

If the TSD and OCP flags are triggered, FAULT pin will be pulled low, so FAULT pin can be the interrupt signal to processor. Once TSD and OCP are set to 1b, the FAULT pin logic is latched to low, processor need to read this status register to release the fault conditions.

Status Register (address = 0x02) [reset = 0x29]

図 7-14. Status Register

7	6	5	4	3	2	1	0
Reserved	0	LDO_ON	T125	TSD	OCP	CABLE_GOOD	VOUT_GOOD
R-0b	R-0b	R-0b	R-0b	R-1b	R-0b	R-0b	R-1b

表 7-8. Status Register

Bit	Field	Type	Reset	Description
7	Reserved	R	0b	Reserved
6	TDETGOOD	R	0b	0b = 22-kHz tone detected on DIN pin is out of range 1b = 22-kHz tone detected on DIN pin is in range
5	LDO_ON	R	1b	0b = Internal LDO is turned off but boost converter is on 1b = Internal LDO is turned on and boost converter is on

表 7-8. Status Register (continued)

Bit	Field	Type	Reset	Description
4	T125	R	0b	0b = Die temperature < 125°C 1b = Die temperature > 125°C
3	TSD	R	1b	0b = No thermal shutdown triggered 1b = Thermal shutdown triggered. The FAULT pin logic is latched to low, processor need to read this register to release the fault conditions
2	OCP	R	0b	0b = Overcurrent protection conditions released 1b = Overcurrent protection triggered. The FAULT pin logic is latched to low, processor need to read this register to release the fault conditions
1	CABLE_GOOD	R	0b	0b = Cable not connected 1b = Cable connection good
0	VOUT_GOOD	R	1b	0b = LNB output voltage out of range 1b = LNB output voltage in range

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS652353 supports both DisEqc1.x and DisEqc2.x application. When the input voltage VIN is greater than the expected output voltage VLNB, the linear regulator drops the voltage difference between VIN and VLNB, which causes the lower efficiency and the higher power loss on the internal linear regulator if the current loading is high. For care must be taken to ensure that the safe operating temperature range of the TPS652353 is not exceeded. TI recommends operating the device in Forced PWM mode when V_{IN} > V_{OUT} to reduce output ripple.

8.2 Typical Application

8.2.1 DiSEqc1.x Support

TPS652353 can operate in I²C and non-I²C interface mode. 図 8-1 shows the application with the device in I²C interface mode to support DiSEqC 1.x application. In non-I²C mode, the SCL, SDA, and ADDR pins can be floating.

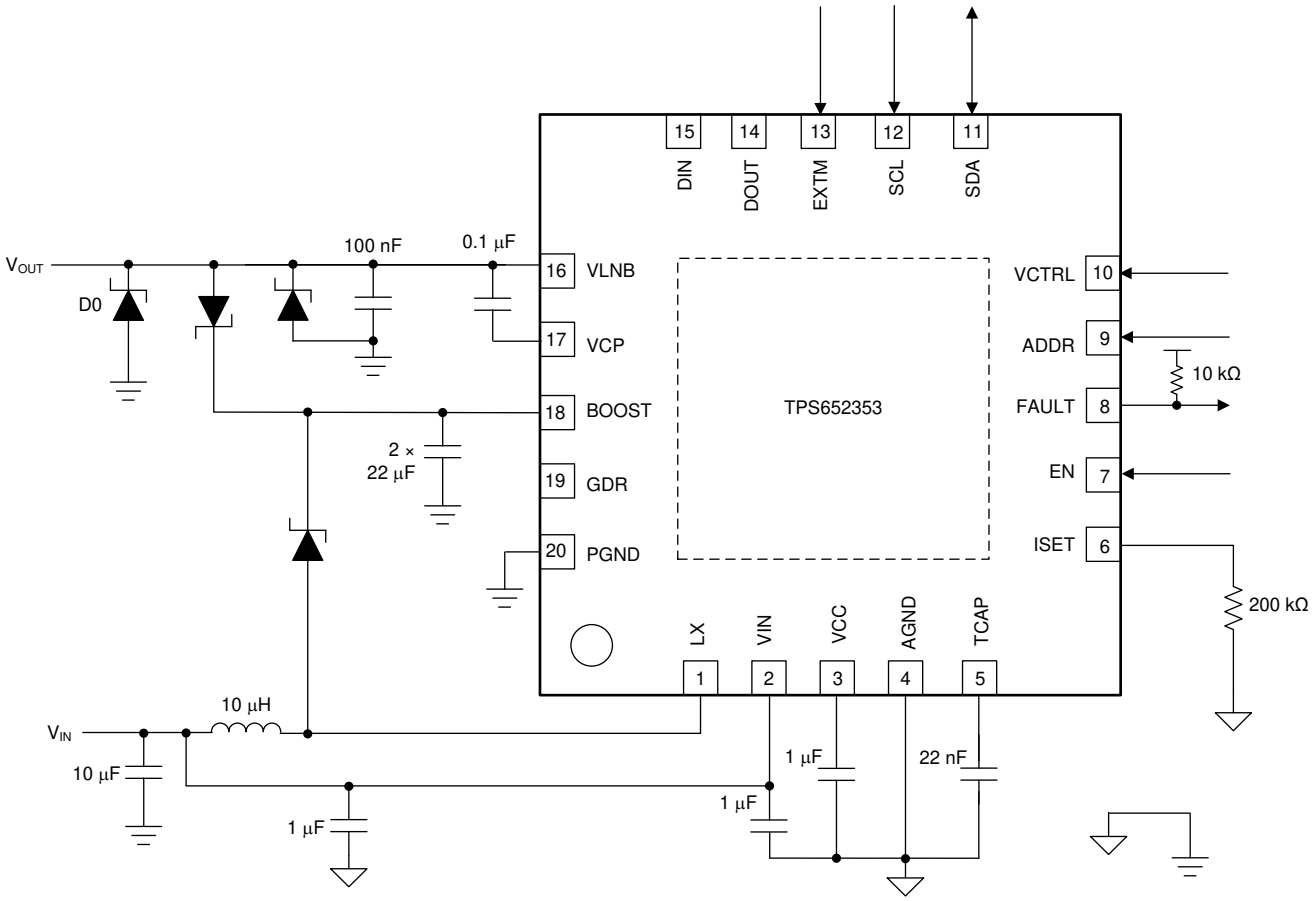


図 8-1. Application for DiSEqc1.x Support

8.2.1.1 Design Requirements

For this design example, use the parameters in 表 8-1.

表 8-1. Design Parameters

PARAMETER	VALUE
Input voltage range, V_{IN}	4.5 V to 20 V
Output voltage range V_{LNB}	11 V to 21 V
Output current range	0 A to 1 A

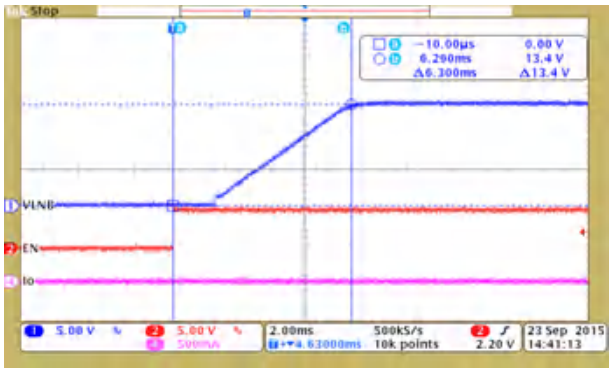
8.2.1.2 Detailed Design Procedure

To begin the design process, the following component values must be selected:

- Inductor
  - Choose the appropriate value of the inductor based on application cost requirements, ripple requirements, and セクション 7.3.11.
- BOOST capacitor
  - Choose the appropriate BOOST capacitor value based on application cost requirements, ripple requirements, and セクション 7.3.11.
- Diodes
  - The D0 and D2 diodes are used to help meet the surge-protection requirement of the application. If the application does not require surge protection, remove these diodes. For diode component selection, refer to セクション 7.3.11.3.
  - The D1 diode is used for the boost loop. A Schottky diode is recommended for D1. The application requirements, which include input power range, output power range, and the current requirement, determine the current and voltage capability of the D1 diode.
  - The D3 diode is to help with the output protection for the VLNB voltage. A Schottky diode is recommended for D3. The application requirements determine the current and voltage capability of the D3 diode.

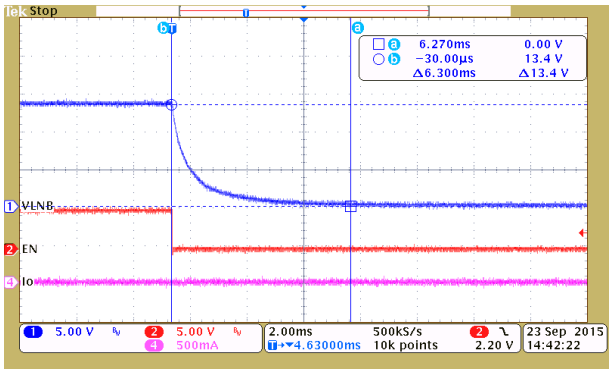
8.2.1.3 Application Curves

T_J = 25°C, V_{IN} = 12 V, f_{SW} = 1 MHz, C_{Boost} = (2 × 22 µF / 35 V) (unless otherwise noted)



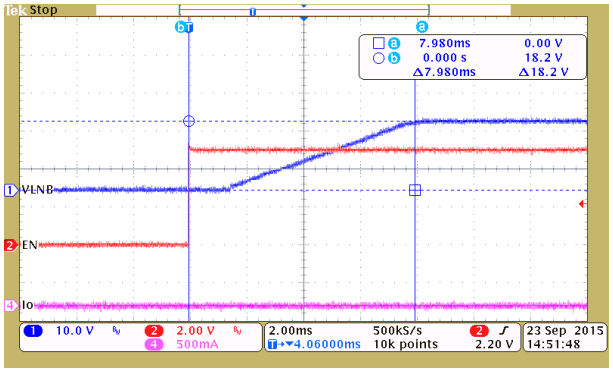
V_{VLNB} = 13.4 V

図 8-2. Soft Start, Delay from EN High to LNB Output High



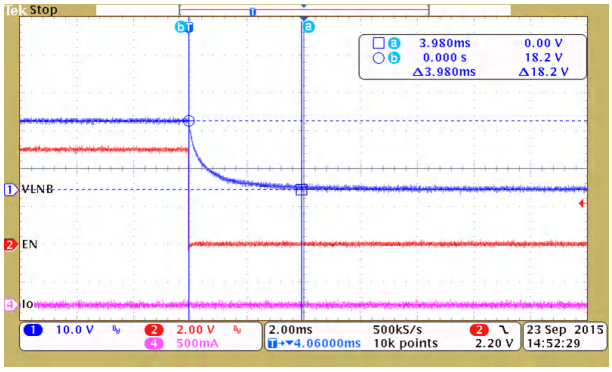
V_{VLNB} = 13.4 V

図 8-3. Disabled, Delay from EN Low to LNB Output Low



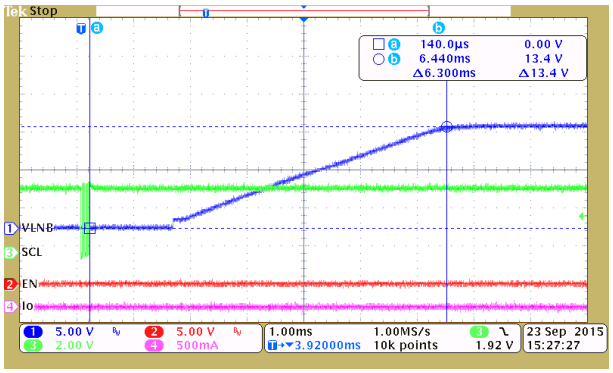
V_{VLNB} = 18.2 V

図 8-4. Soft-Start, Delay from EN High to LNB Output High



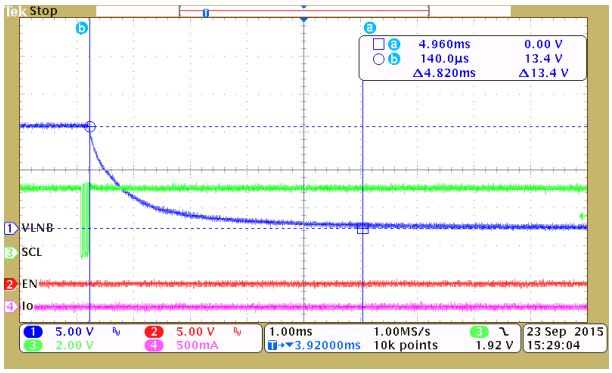
V_{VLNB} = 18.2 V

図 8-5. Disabled, Delay From EN Low to LNB Output Low



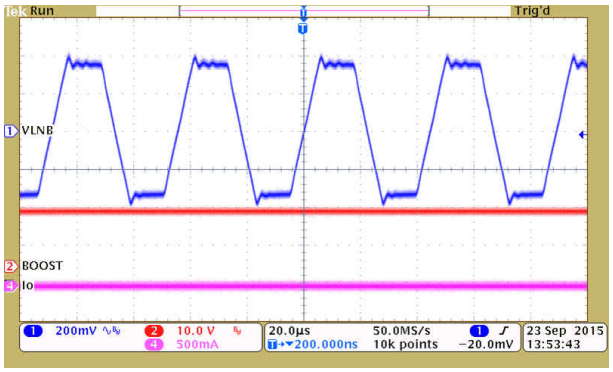
EN = 0b V_{VLNB} = 13.4 V

図 8-6. Soft Start, Delay From I²C Enable (I2C_CON = 1b) to LNB Output High



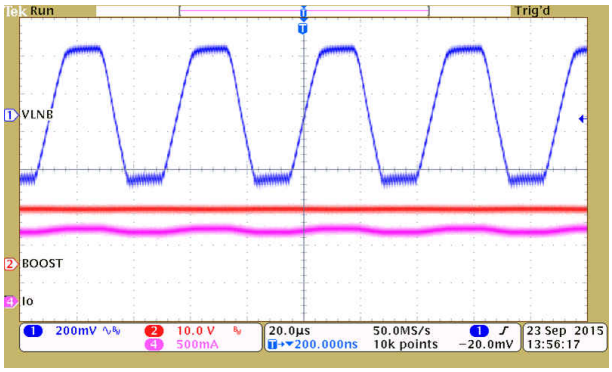
EN = 0b V_{VLNB} = 13.4 V

図 8-7. Delay From I²C Disable (I2C_CON = 0b) to LNB Output Low



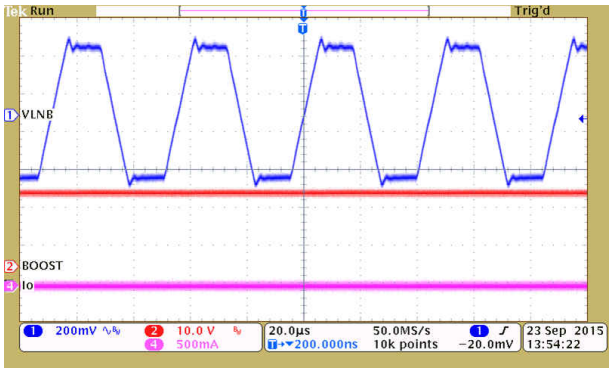
V_{VLNB} = 13.4 V

図 8-8. No Load, 22-kHz Tone Output



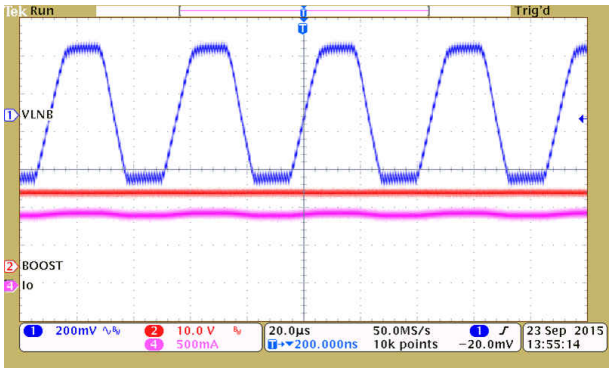
V_{VLNB} = 13.4 V

図 8-9. 950-mA Load, 22-kHz Tone Output



V_{VLNB} = 18.2 V

図 8-10. No Load, 22-kHz Tone Output



V_{VLNB} = 18.2 V

図 8-11. 950-mA Load, 22-kHz Tone Output

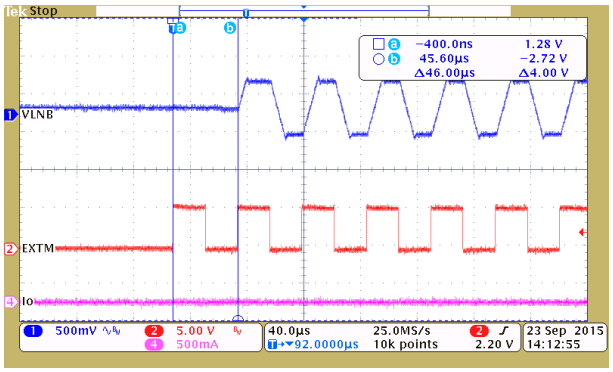


図 8-12. No load, 22-kHz Tone Delay from EXTM 22-kHz Input Turns High to Output Tone On

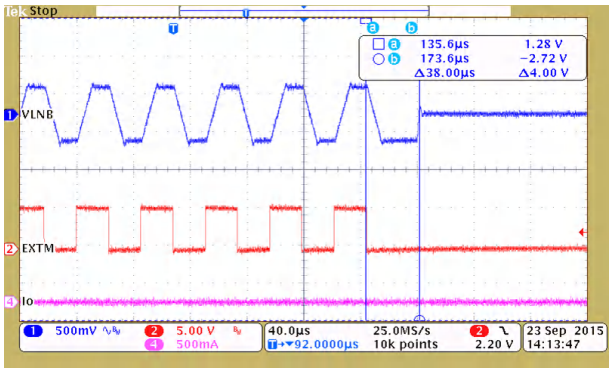


図 8-13. No load, 22-kHz Tone Delay from EXTM 22-kHz Input Turns Low to Output Tone Off

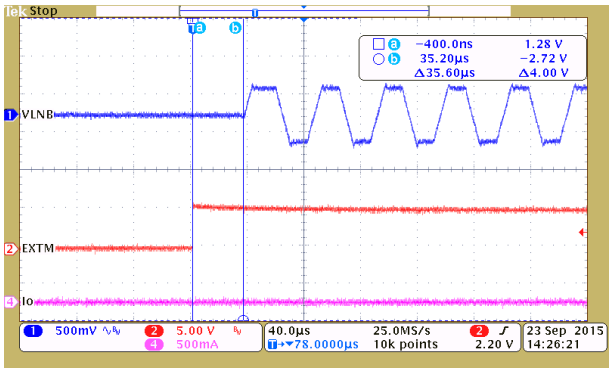


図 8-14. No Load, 22-kHz Tone Delay from EXTM Tone Envelop Input Turns High to Output Tone On

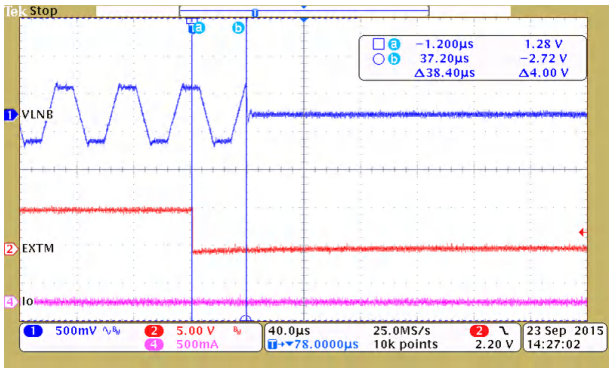


図 8-15. No Load, 22-kHz Tone Delay from EXTM Tone Envelop Input Turns Low to Output Tone Off

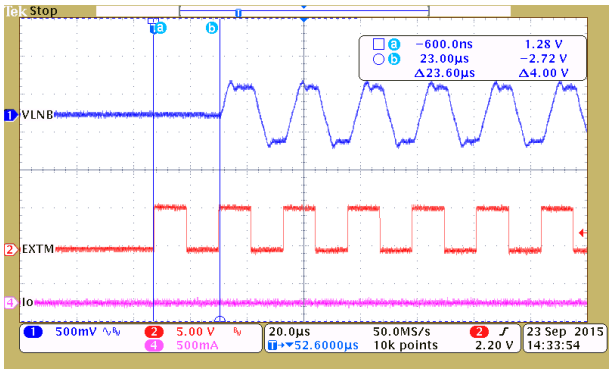


図 8-16. No Load, 44-kHz Tone Delay from EXTM 22-kHz Input Turns High to Output Tone On

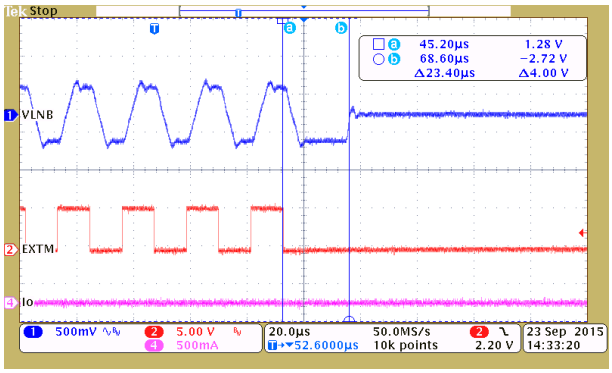


図 8-17. No Load, 44-kHz Tone Delay from EXTM 22-kHz Input Turns Low to Output Tone Off

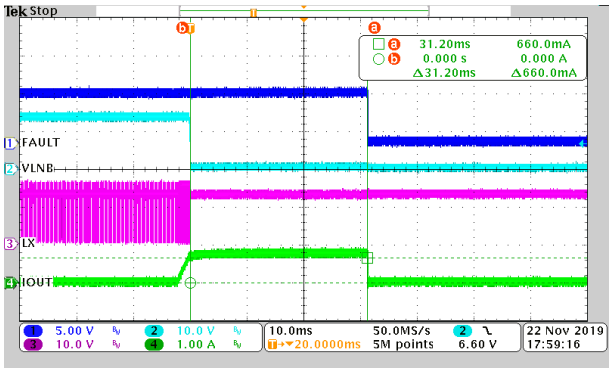


図 8-18. Current Limit Operation at R_{SET} = 200 kΩ

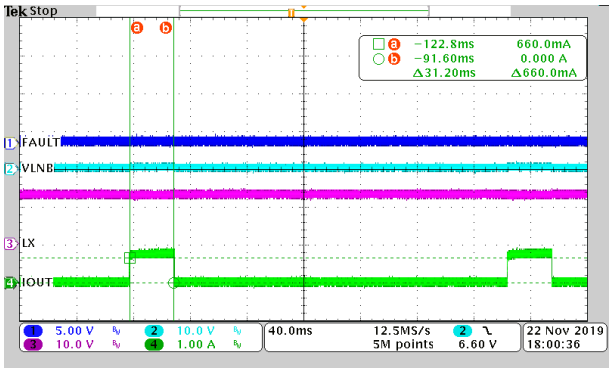


図 8-19. Hiccup Operation at R_{SET} = 200 kΩ

8.2.2 DiSEqc2.x Support

The TPS652353 can support both DiSEqC 1.x application and DiSEqC 2.x application. 図 8-20 shows the application for supporting DiSEqC 2.x application.

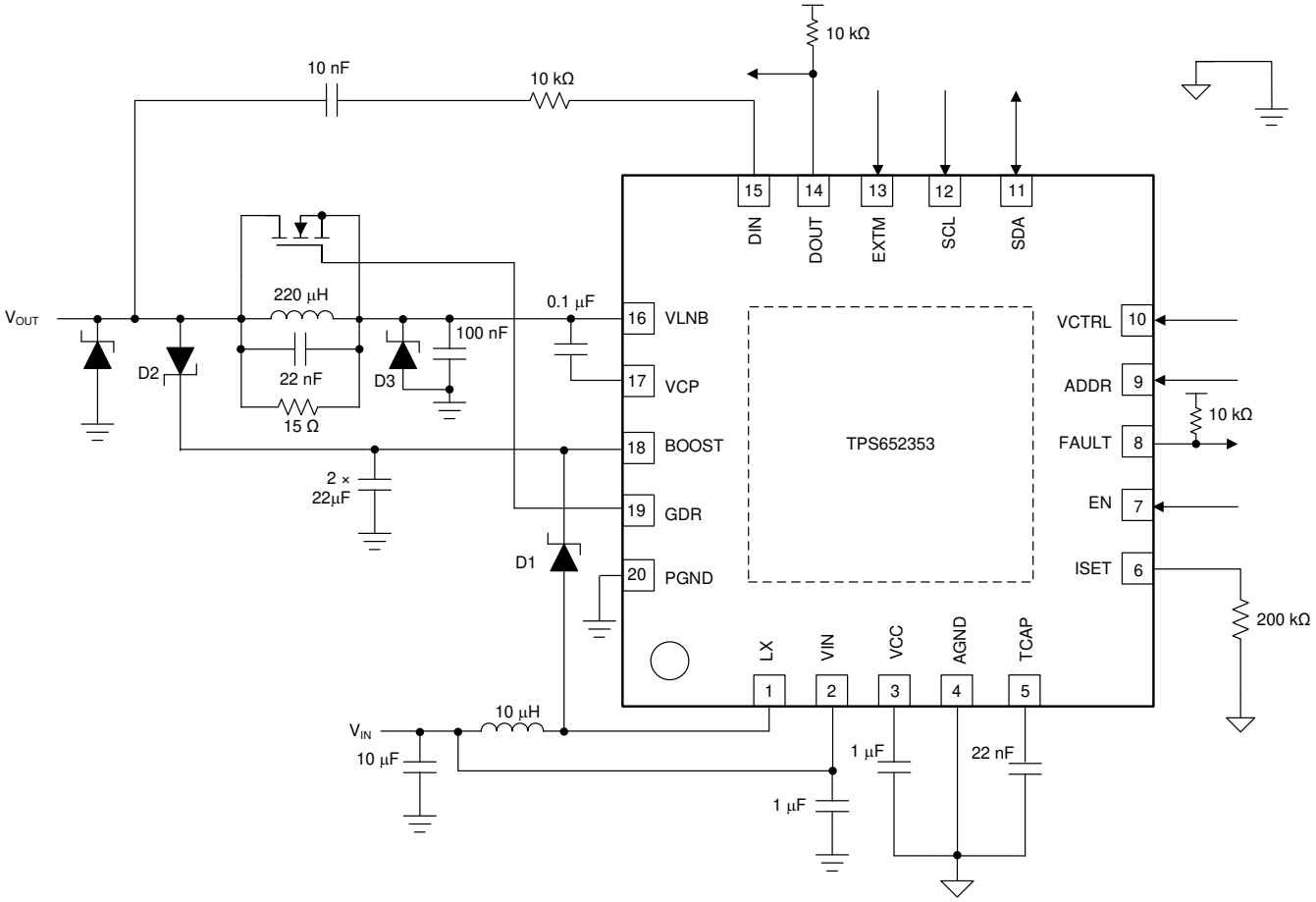


図 8-20. Application Schematic for DiSEqc2.x Support

8.2.2.1 Design Requirements

Refer to the *DiSEqc1.x Support* section for design requirements.

8.2.2.2 Detailed Design Procedure

Refer to the *DiSEqc1.x Support* section for detailed design procedures.

8.2.2.3 Application Curve

Refer to the *DiSEqc1.x Support* section for typical application curves. 図 8-21 is the unique tone-detection curve for the DiSEqC 2.x application.

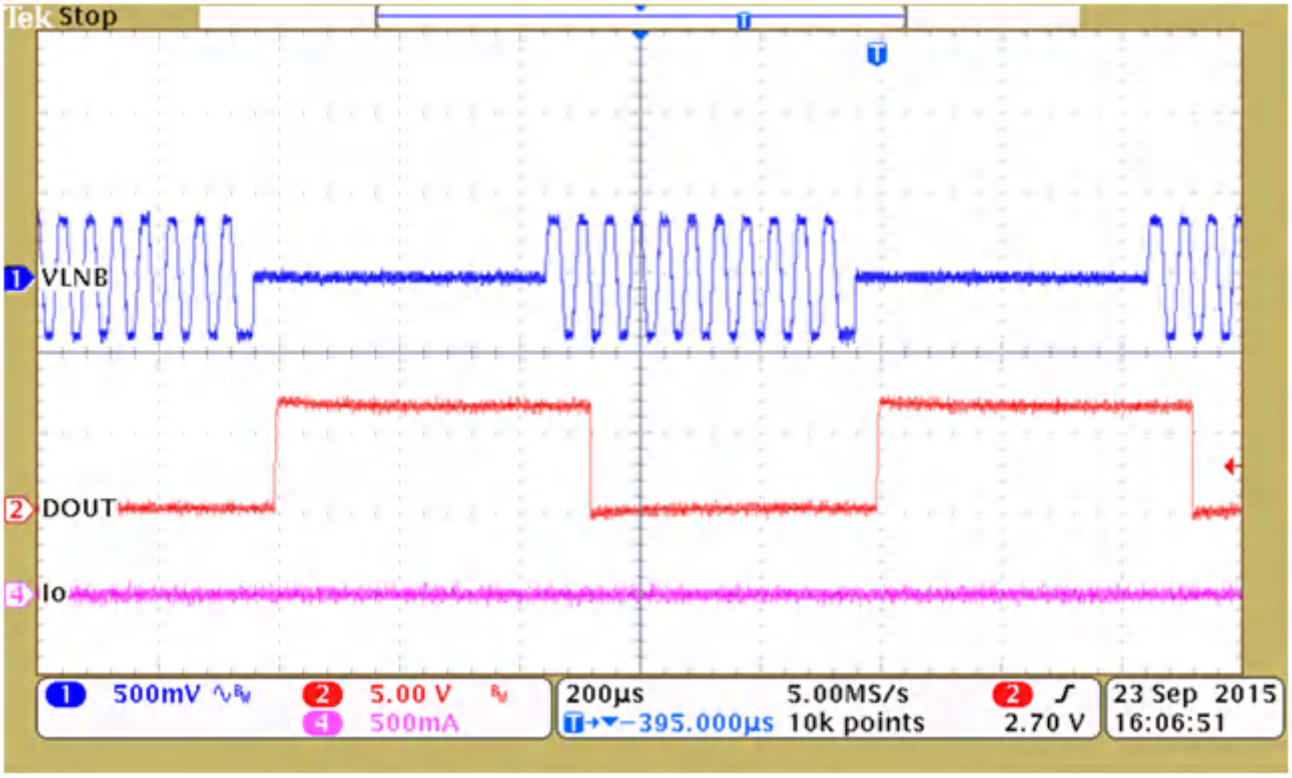


図 8-21. DOUT Tone Detection Output

8.3 Power Supply Recommendations

The device is designed to operate from an input supply ranging from 4.5 V to 20 V. The input supply should be well regulated. If the input supply is located more than a few inches from the converter, an additional bulk capacitance, typically with a value 100 µF, may be required in addition to the ceramic bypass capacitors.

8.4 Layout

8.4.1 Layout Guidelines

The TPS652353 is designed to layout in 2-layer PCB. To ensure reliability of the device, following common printed-circuit board layout guidelines is recommended.

- It is critical to make sure the ground of input capacitor, output capacitor, and the boost converter are connected at one point at same layer.
- The PGND and AGND pins are located in different regions. Connect these grounds to the thermal pad. Other components are connected the AGND pin.
- Put the BOOST capacitors as close as possible.
- The loop from the VIN inductor to the LX pin should be as short as possible.
- The loop from the VIN inductor to D1 Schottky diode to the BOOST should be as short as possible.
- The loop for boost capacitors to the PGND pin should be within the loop from the LX pin to D1 Schottky diode to the BOOST pin.

8.4.2 Layout Example

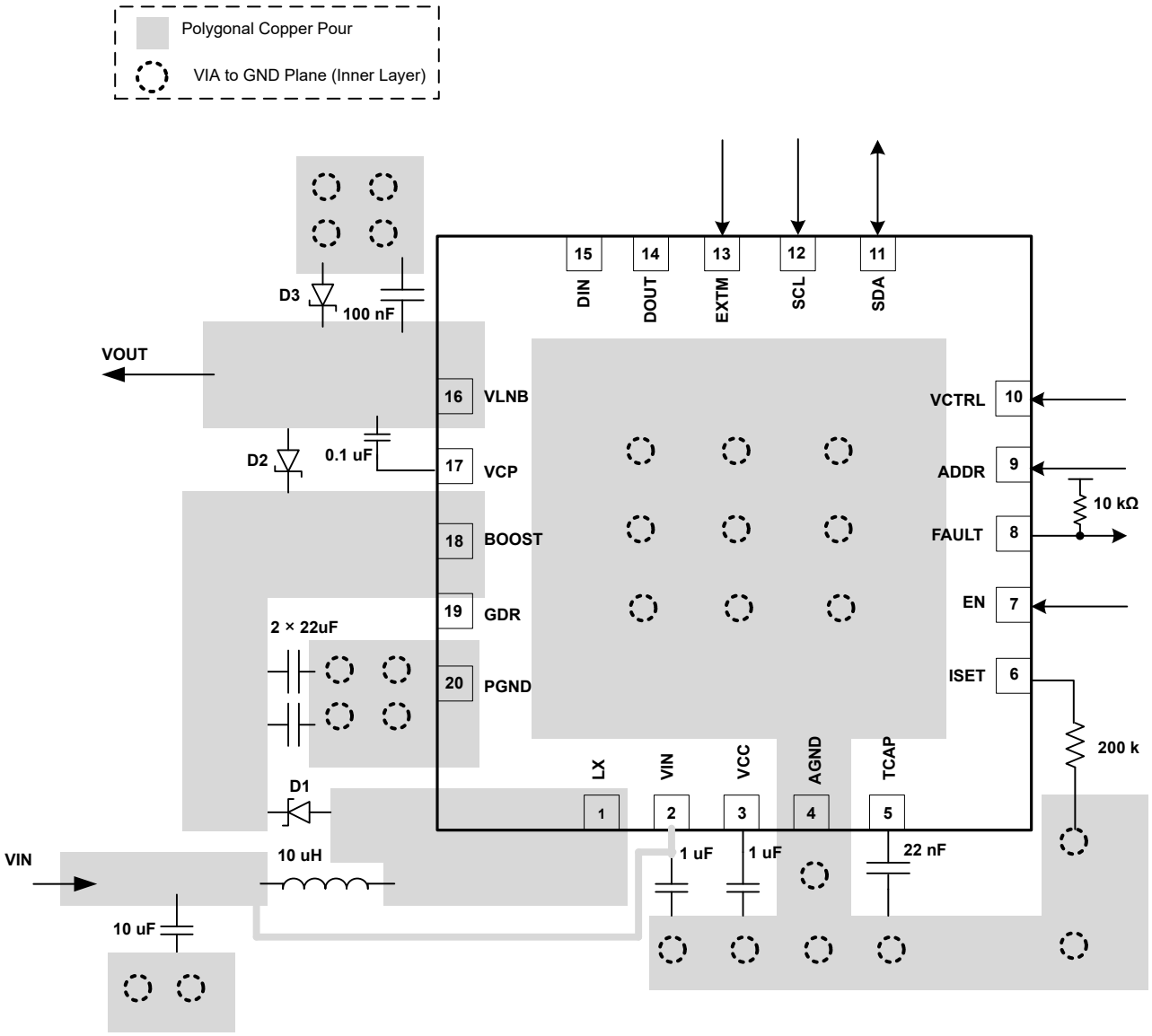


図 8-22. Layout

9 Device and Documentation Support

9.1 Device Support

9.1.1 サード・パーティ製品に関する免責事項

サード・パーティ製品またはサービスに関するテキサス・インスツルメンツの出版物は、単独またはテキサス・インスツルメンツの製品、サービスと一緒に提供される場合に関係なく、サード・パーティ製品またはサービスの適合性に関する是認、サード・パーティ製品またはサービスの是認の表明を意味するものではありません。

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Evaluation Module for the TPS652353 LNB Voltage Regulator With I²C Interface for DiSEqC2.x Application* user's guide
- Texas Instruments, *Evaluation Module for the TPS652353 LNB Voltage Regulator With I²C Interface for DiSEqC1.x Application* user's guide

9.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

9.4 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

9.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

9.6 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS65235-3RUKR	Active	Production	WQFN (RUK) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	652353
TPS65235-3RUKR.A	Active	Production	WQFN (RUK) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	652353

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

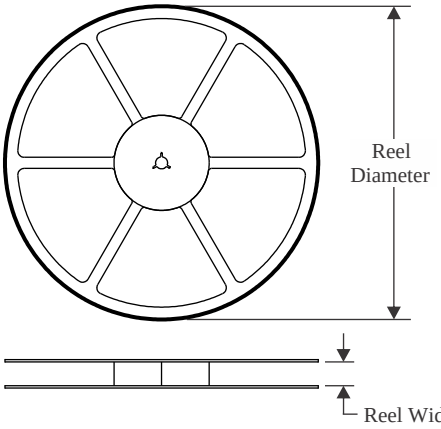
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

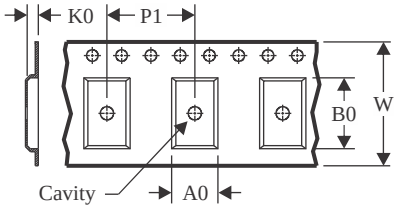
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

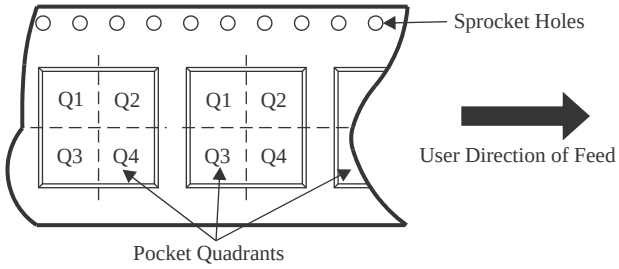


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

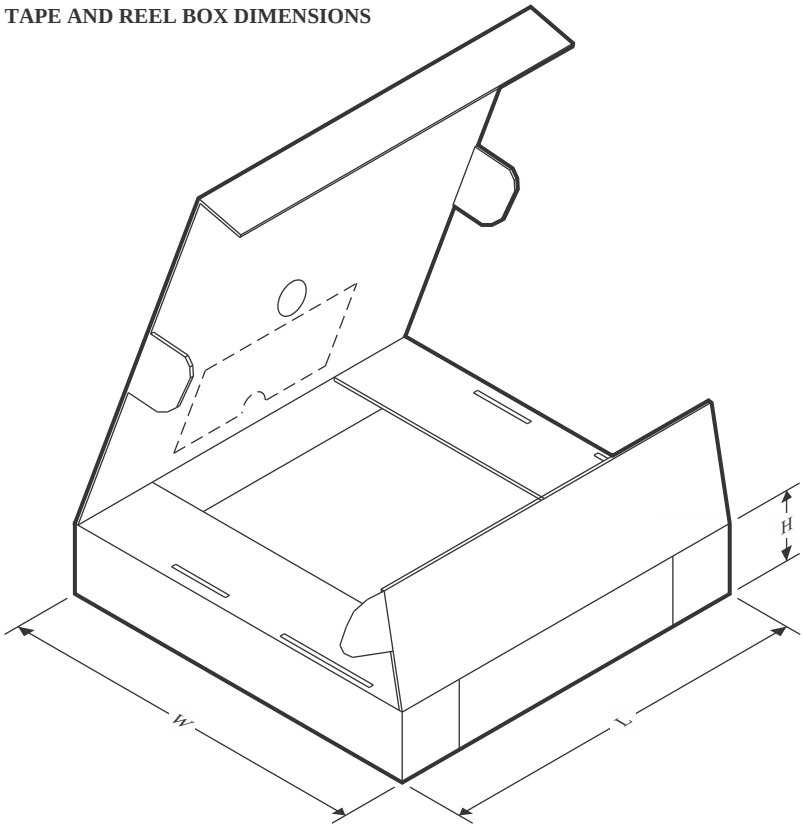
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65235-3RUKR	WQFN	RUK	20	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS65235-3RUKR	WQFN	RUK	20	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65235-3RUKR	WQFN	RUK	20	3000	367.0	367.0	35.0
TPS65235-3RUKR	WQFN	RUK	20	3000	356.0	356.0	36.0

GENERIC PACKAGE VIEW

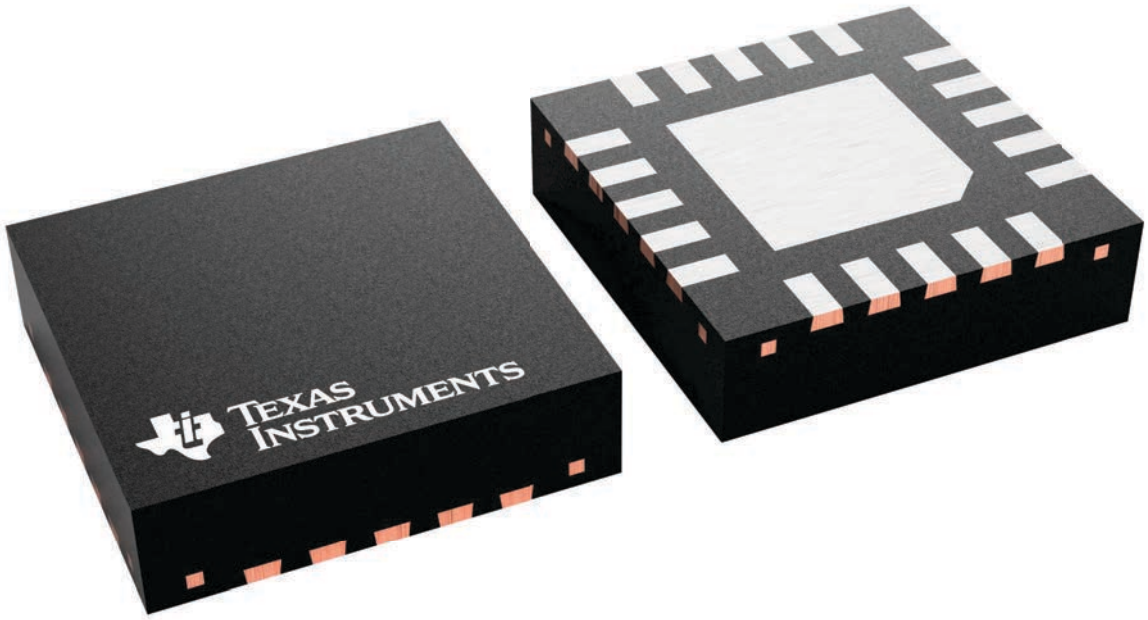
RUK 20

WQFN - 0.8 mm max height

3 x 3, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



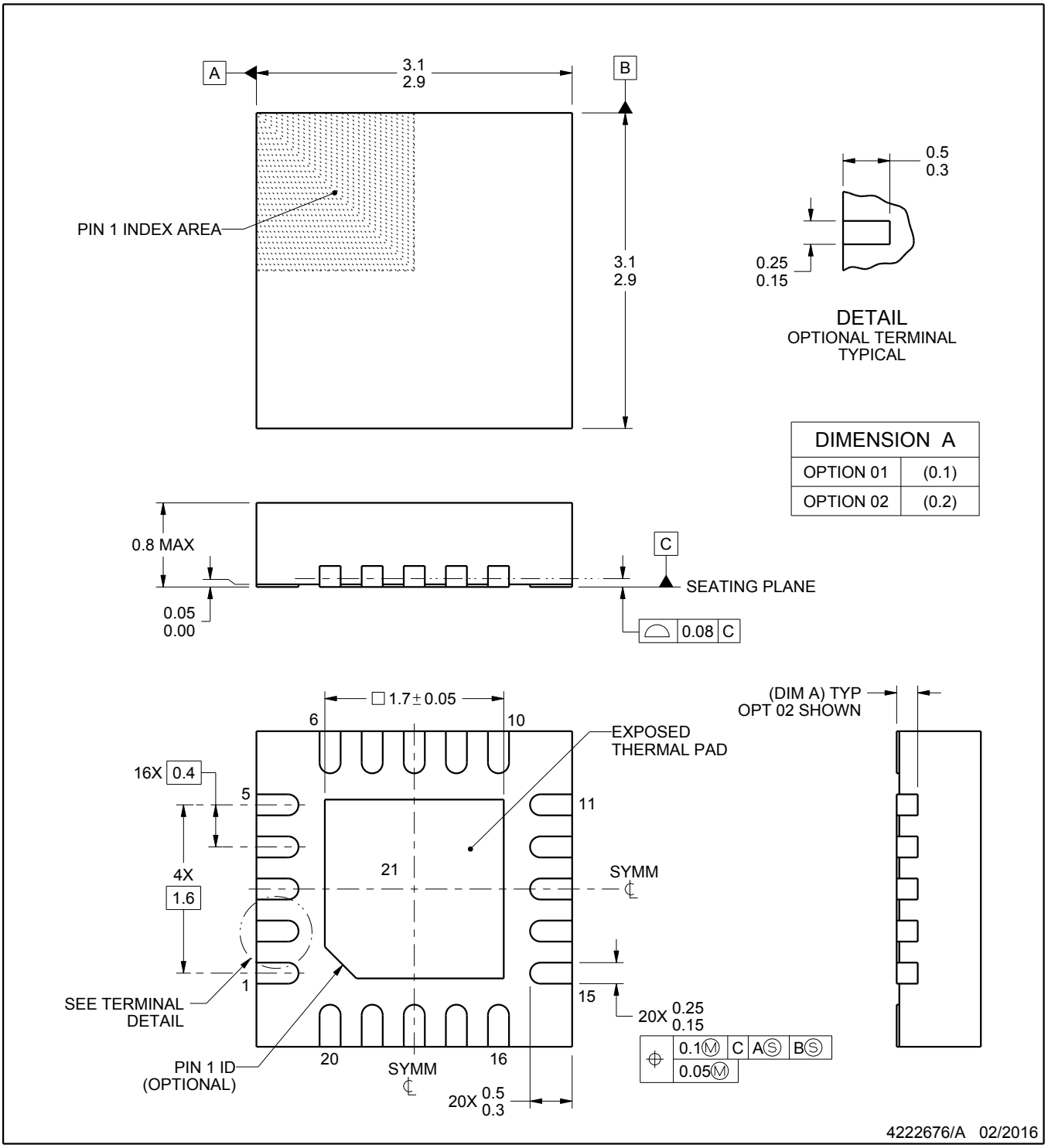
4229651/A

PACKAGE OUTLINE

RUK0020B

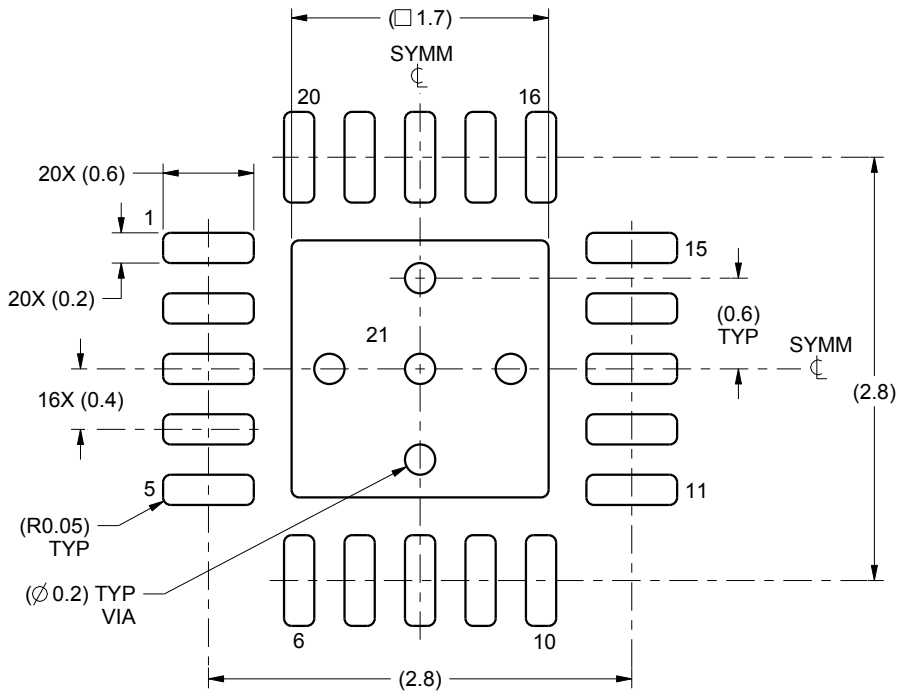
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

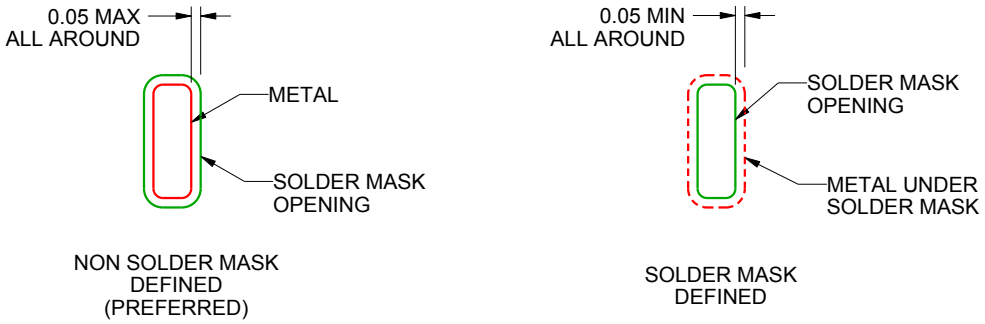


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

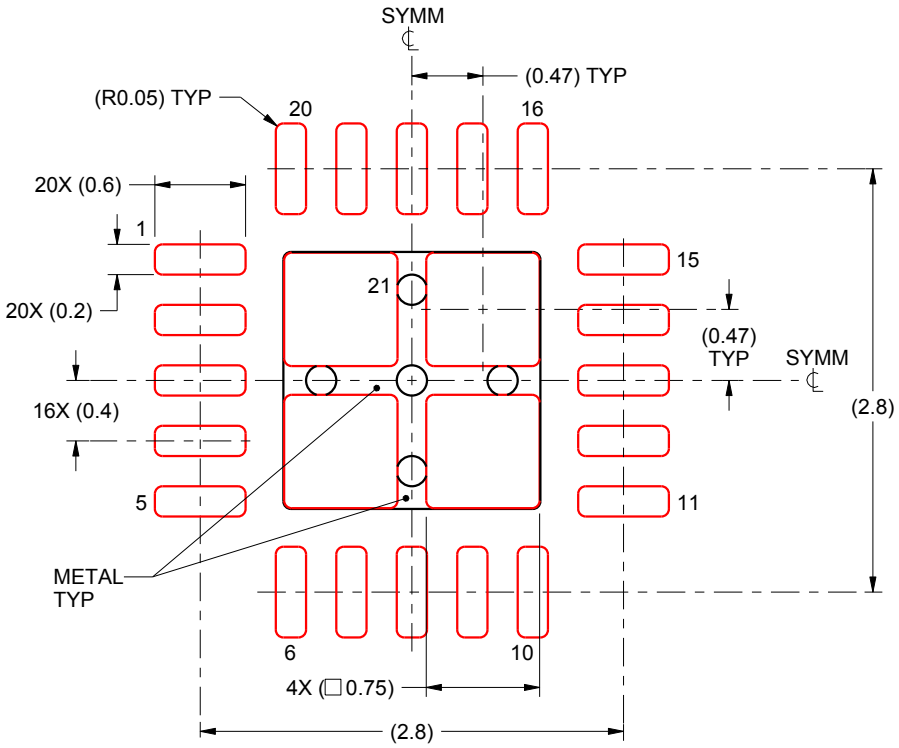


SOLDER MASK DETAILS

4222676/A 02/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 21:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4222676/A 02/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、 TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

最終更新日：2025 年 10 月