TEXAS INSTRUMENTS
TPS65982DMC
JAJSJU6 – SEPTEMBER 2020

TPS65982DMC ドック管理コントローラ

1 特長

- ファームウェアのセキュア・アップデート
  - TPS65982DMC とその他の TI PD コントローラを USB Low Speed を介してセキュアに更新
  - SHA-256 および RSA-3072
  - TI PD コントローラの I2C ブート - 1 つのフラッシュですべてのデバイスに対応
  - セキュリティ対策が施されていないファームウェア更新をサポート
- バレル・ジャック入力制御
  - 過電圧検出機能を備えた NFET ゲート駆動回路を内蔵
  - ソフト・スタート
- スマート電源ポリシー・マネージャ
  - ドックのすべての電源を管理 – USB Type-C、USB Type-A、システム電源
  - 構成可能なスマート電源ポリシー・マネージャ
- USB4 接続マネージャ
  - UFP ホスト接続に基づいて DFP ポートを更新
  - PD コントローラを再構成し、適切な接続変更を発行
  - システム用の構成可能な GPIO
- NFBGA パッケージ
  - 0.5mm ピッチ
  - すべてのピンについて、スルーホール・ビア互換

2 アプリケーション

- Thunderbolt 4 デバイス
- USB4 デバイス
- ドッキング・ステーション
- モニタ

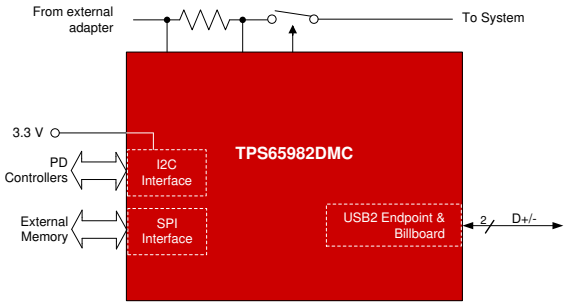
3 概要

TPS65982DMC は、TI の PD コントローラを実装するドック、ハブ、モニタのためのドック管理コントローラです。TPS65982DMC は、システムの PD コントローラのためのファームウェア更新を受け付けることができる USB Low Speed エンドポイントを内蔵しています。このファームウェア更新は、SHA-256 および RSA-3072 認証を使用してセキュアに実行されます。また、このエンドポイントは USB ビルボード機能を備えています。TPS65982DMC は、外部アダプタからシステム電源を制御するために、逆直列接続された NFET のためのドライバを内蔵しています。本 DMC は、アダプタの入力経路とシステムのその他の場所を流れる電流を監視し、管理対象の PD コントローラの電力アドバタイズメントを調整することで、外部アダプタの過負荷を防止します。USB4 システムに組込まれた TPS65982DMC は、上流側ポートの接続状態を監視し下流側ポートの接続状態を更新することで、システム全体のデータの挙動の一貫性を確保します。

製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
TPS65982DMC	NFBGA (96)	6.00mm × 6.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



簡略ブロック図

Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
September 2020	*	Initial Release

5 Pin Configuration and Functions

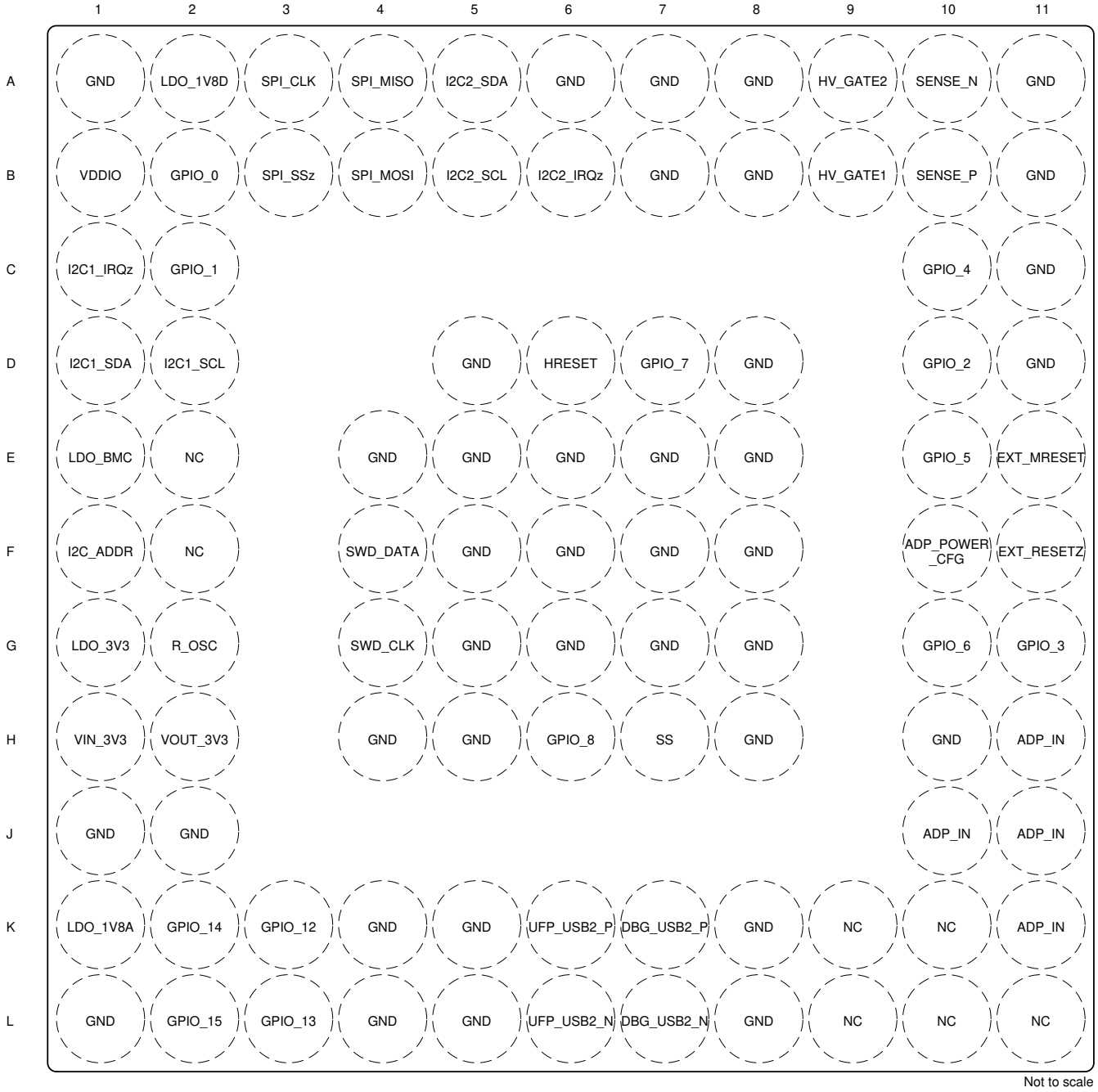


図 5-1. ZBH Package 96-Pin NFBGA Top View

Pin Functions

BALL NAME	BALL NUMBER	TYPE	POR STATE	DESCRIPTION
ADP_IN	H11, J10, J11, K11	Power	N/A	Adapter Input to Internal LDO.
ADP_POWER_CFG	F10	Analog Input	Input (Hi-Z)	Sampled by ADC at boot to determine adapter switch behavior.
DBG_USB2_N	L7	Analog I/O	Hi-Z	USB D- Connection for USB Debug.
DBG_USB2_P	K7	Analog I/O	Hi-Z	USB D+ Connection for USB Debug.
EXT_MRESET	E11	Digital I/O	Hi-Z	Forces RESETZ to assert. This pin asserts RESETZ when pulled high. Ground pin with a 1-MΩ resistor when unused in the application.

BALL NAME	BALL NUMBER	TYPE	POR STATE	DESCRIPTION
EXT_RESETZ	F11	Digital I/O	Push-Pull Output (Low)	Active low reset output when VOUT_3V3 is low (driven low on start-up). Float pin when unused.
GND	A1, A11, A6, A7, A8, B11, B7, B8, C11, D11, D5, D8, E4, E5, E6, E7, E8, F5, F6, F7, F8, G5, G6, G7, G8, H10, H4, H5, H8, J1, J2, K4, K5, K8, L1, L4, L5, L8	Ground	N/A	Ground. Connect all balls to ground plane.
GPIO_0(1)	B2	Digital I/O	Hi-Z	General Purpose Digital I/O 0. Float pin if it is configured as a push-pull output in the application. Ground pin with a 1-MΩ resistor when unused in the application.
GPIO_1(1)	C2	Digital I/O	Hi-Z	General Purpose Digital I/O 1. Float pin if it is configured as a push-pull output in the application. Ground pin with a 1-MΩ resistor when unused in the application.
GPIO_2(1)	D10	Digital I/O	Hi-Z	General Purpose Digital I/O 2. Float pin if it is configured as a push-pull output in the application. Ground pin with a 1-MΩ resistor when unused in the application.
GPIO_3(1)	G11	Digital I/O	Hi-Z	General Purpose Digital I/O 3. Float pin if it is configured as a push-pull output in the application. Ground pin with a 1-MΩ resistor when unused in the application.
GPIO_4(1)	C10	Digital I/O	Hi-Z	General Purpose Digital I/O 4. Float pin if it is configured as a push-pull output in the application. Ground pin with a 1-MΩ resistor when unused in the application.
GPIO_5(1)	E10	Digital I/O	Hi-Z	General Purpose Digital I/O 5. Float pin if it is configured as a push-pull output in the application. Ground pin with a 1-MΩ resistor when unused in the application.
GPIO_6(1)	G10	Digital I/O	Hi-Z	General Purpose Digital I/O 6. Float pin if it is configured as a push-pull output in the application. Ground pin with a 1-MΩ resistor when unused in the application.
GPIO_7(1)	D7	Digital I/O	Hi-Z	General Purpose Digital I/O 7. Float pin if it is configured as a push-pull output in the application. Ground pin with a 1-MΩ resistor when unused in the application.
GPIO_8(1)	H6	Digital I/O	Hi-Z	General Purpose Digital I/O 8. Float pin if it is configured as a push-pull output in the application. Ground pin with a 1-MΩ resistor when unused in the application.
GPIO_12(1)	K3	Digital I/O	Hi-Z	General Purpose Digital I/O 12. Float pin if it is configured as a push-pull output in the application. Ground pin with a 1-MΩ resistor when unused in the application.
GPIO_13(1)	L3	Digital I/O	Hi-Z	General Purpose Digital I/O 13. Float pin if it is configured as a push-pull output in the application. Ground pin with a 1-MΩ resistor when unused in the application.
GPIO_14(1)	K2	Digital I/O	Hi-Z	General Purpose Digital I/O 14. Float pin if it is configured as a push-pull output in the application. Ground pin with a 1-MΩ resistor when unused in the application.
GPIO_15(1)	L2	Digital I/O	Hi-Z	General Purpose Digital I/O 15. Float pin if it is configured as a push-pull output in the application. Ground pin with a 1-MΩ resistor when unused in the application.
HRESET	D6	Digital Input	Hi-Z	Active high hardware reset input. Will re-load settings from external flash memory. Ground pin when HRESET functionality will not be used.
HV_GATE1	B9	Analog Output	Short to Sense_P	External NFET gate control for high voltage power path. Float pin when unused
HV_GATE2	A9	Analog Output	Short to ADP_IN	External NFET gate control for high voltage power path. Float pin when unused
I2C1_IRQz	C1	Digital Output	Hi-Z	I2C port 1 interrupt. Active low. Implement externally as an open drain with a pullup resistance. Float pin when unused.
I2C1_SCL	D2	Digital I/O	Digital Input	I2C port 1 serial clock. Open-drain output. Tie pin to LDO_3V3 or VDDIO (depending on configuration) through a 10-kΩ resistance when used or unused.
I2C1_SDA	D1	Digital I/O	Digital Input	I2C port 1 serial data. Open-drain output. Tie pin to LDO_3V3 or VDDIO (depending on configuration) through a 10-kΩ resistance when used or unused.
I2C2_IRQz	B6	Digital Output	Hi-Z	I2C port 2 interrupt. Active low. Implement externally as an open drain with a pullup resistance. Float pin when unused.
I2C2_SCL	B5	Digital I/O	Digital Input	I2C port 2 serial clock. Open-drain output. Tie pin to LDO_3V3 or VDDIO (depending on configuration) through a 10-kΩ resistance when used or unused.
I2C2_SDA	A5	Digital I/O	Digital Input	I2C port 2 serial data. Open-drain output. Tie pin to LDO_3V3 or VDDIO (depending on configuration) through a 10-kΩ resistance when used or unused.
I2C_ADDR	F1	Analog I/O	Analog Input	Sets the I2C address for both I2C ports as well as determine the master and slave devices for memory code sharing.
LDO_1V8A	K1	Power	N/A	Output of the 3.3 V or 1.8 V LDO for Core Analog Circuits. Bypass with capacitance CLDO_1V8A to GND.
LDO_1V8D	A2	Power	N/A	Output of the 3.3 V or 1.8 V LDO for Core Digital Circuits. Bypass with capacitance CLDO_1V8D to GND.
LDO_3V3	G1	Power	N/A	Output of the ADP_IN to 3.3 V LDO or connected to VIN_3V3 by a switch. Main internal supply rail. Used to power external flash memory. Bypass with capacitance CLDO_3V3 to GND
LDO_BMC	E1	Power	N/A	Output of the 1.1V output level LDO. Bypass with capacitance CLDO_BMC to GND.
NC	E2, F2, K10, K9, L10, L11, L9	Blank	N/A	Populated Ball that must remain unconnected.
R_OSC	G2	Analog I/O	Hi-Z	External resistance setting for oscillator accuracy. Connect R_OSC to GND through resistance RR_OSC.
SENSE_N	A10	Analog Input	Analog Input	Negative sense for external high voltage power path current sense resistance. Short pin to ADP_IN when unused.

BALL NAME	BALL NUMBER	TYPE	POR STATE	DESCRIPTION
SENSE_P	B10	Analog Input	Analog Input	Positive sense for external high voltage power path current sense resistance. Short pin to ADP_IN when unused.
SPI_CLK	A3	Digital Output	Digital Input	SPI serial clock. Ground pin when unused.
SPI_MISO	A4	Digital Input	Digital Input	SPI serial master input from slave. This pin is used during boot sequence to determine if the flash memory is valid. Ground pin when unused.
SPI_MOSI	B4	Digital Output	Digital Input	SPI serial master output to slave. Ground pin when unused.
SPI_SSz	B3	Digital Output	Digital Input	SPI slave select. Ground pin when unused.
SS	H7	Analog Output	Driven Low	Soft Start. Tie pin to capacitance CSS to ground.
SWD_CLK	G4	Digital Input	Resistive Pull High	SWD serial clock. Float pin when unused.
SWD_DATA	F4	Digital I/O	Resistive Pull High	SWD serial data. Float pin when unused.
UFP_USB2_N	L6	Analog I/O	Hi-Z	USB D- Connection for USB Endpoint.
UFP_USB2_P	K6	Analog I/O	Hi-Z	USB D+ Connection for USB Endpoint.
VDDIO	B1	Power	N/A	VDD for I/O. Some I/Os are reconfigurable to be powered from VDDIO instead of LDO_3V3. When VDDIO is not used, tie pin to LDO_3V3. When not tied to LDO_3V3 and used as a supply input, bypass with capacitance CVDDIO to GND.
VIN_3V3	H1	Power	N/A	Supply for core circuitry and I/O. Bypass with capacitance CVIN_3V3 to GND.
VOUT_3V3	H2	Power	N/A	Output of supply switched from VIN_3V3. Bypass with capacitance COUT_3V3 to GND. Float pin when unused.

(1) GPIO Function is determined by device firmware. Consult device TRM for available GPIO behaviors.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_I	Input voltage(2)	VIN_3V3	–0.3	3.6	V
		SENSEP, SENSEN(3)	–0.3	24	
		VDDIO	–0.3	LDO_3V3 + 0.3	
V_{IO}	Output voltage (2)	LDO_1V8A, LDO_1V8D, LDO_BMC, SS	–0.3	2	V
		LDO_3V3	–0.3	3.45	
		VOUT_3V3, RESETZ, I2C _IRQ1Z, I2C_IRQ2Z, SPI_MOSI, SPI_CLK, SPI_SSZ, SWD_CLK	–0.3	LDO_3V3 + 0.3	
		HV_GATE1, HV_GATE2	–0.3	30	
		HV_GATE1 (relative to SENSEP)	–0.3	6	
		HV_GATE2 (relative to ADP_IN)	–0.3	6	
V_{IO}	I/O voltage (2)	ADP_IN	–0.3	24	V
		I2C_SDA1, I2C_SCL1, SWD_DATA, SPI_MISO, I2C_SDA2, I2C_SCL2, GPIOn, MRESET, ADP_POWER_CFG	–0.3	LDO_3V3 + 0.3	
		R_OSC, I2C_ADDR	–0.3	2	
		HRESET	–0.3	LDO_1V8D + 0.3	
		UFP_USB2_N, UFP_USB2_P, DBG_USB2_N, DBG_USB2_P (Switches Open)	–2	6	
		UFP_USB2_N, UFP_USB2_P, DBG_USB2_N, DBG_USB2_P (Switches Closed)	–0.3	6	
T_J	Operating junction temperature		–10	125	°C
T_{stg}	Storage temperature		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under セクション 6.3. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network GND. All GND pins must be connected directly to the GND plane of the board.
(3) The 24 V maximum is based on keeping HV_GATE1/2 at or below 30 V. Fast voltage transitions (<100 ns) may occur up to 30 V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_I	Input voltage range[1]	VIN_3V3	2.85	3.45	V
		VDDIO	1.7	3.45	
V_{IO}	I/O voltage range[1]	ADP_IN	4	22	V
		UFP_USB2_N, UFP_USB2_P, DBG_USB2_N, DBG_USB2_P	–2	5.5	
T_A	Ambient operating temperature range		–10	85	°C
T_B	Operating board temperature range		–10	100	°C
T_J	Operating junction temperature range		–10	125	°C

(1) All voltage values are with respect to network GND. All GND pins must be connected directly to the GND plane of the board.

6.4 Thermal Information

THERMAL METRIC[1]		TPS65982DMC ZBH (NFBGA) 96 BALLS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	42.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	12.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	13	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Power Supply Requirements and Characteristics

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EXTERNAL						
VIN_3V3	Input 3.3-V supply		2.85	3.3	3.45	V
ADP_IN	Input DC bus voltage. Input to the TPS65982DMC.		4	5	22	V
VDDIO(1)	Optional supply for I/O cells.		1.7		3.45	V
INTERNAL						
VLDO_3V3	DC 3.3V generated internally by either a switch from VIN_3V3, an LDO from PP_CABLE, or an LDO from ADP_IN		2.7	3.3	3.45	V
VDO_LDO3V3	Drop Out Voltage of LDO_3V3 from PP_CABLE	I_{LOAD} = 50 mA			250	mV
	Drop Out Voltage of LDO_3V3 from ADP_IN		250	500	750	mV
VLDO_1V8D	DC 1.8V generated for internal digital circuitry.		1.7	1.8	1.9	V
VLDO_1V8A	DC 1.8V generated for internal analog circuitry.		1.7	1.8	1.9	V
VLDO_BMC	DC voltage generated on LDO_BMC. Setting for USB-PD.		1.05	1.125	1.2	V
ILDO_3V3	DC current supplied by the 3.3V LDOs. This includes internal core power and external load on LDO_3V3.				70	mA
ILDO_3V3EX	External DC current supplied by LDO_3V3				30	mA
IOUT_3V3	External DC current supplied by VOUT_3V3				100	mA
ILDO_1V8D	DC current supplied by LDO_1V8D. This is intended for internal loads only but small external loads may be added.				50	mA
ILDO_1V8DEX	External DC current supplied by LDO_1V8D.				5	mA
ILDO_1V8A	DC current supplied by LDO_1V8A. This is intended for internal loads only but small external loads may be added.				20	mA
ILDO_1V8AEX	External DC current supplied by LDO_1V8A.				5	mA
ILDO_BMC	DC current supplied by LDO_BMC. This is intended for internal loads only.				5	mA
ILDO_BMCEX	External DC current supplied by LDO_BMC.				0	mA
VFWD_DROP	Forward voltage drop across VIN_3V3 to LDO_3V3 switch	I_{LOAD} = 50 mA	25	60	90	mV
RIN_3V3	Input switch resistance from VIN_3V3 to LDO_3V3	$V_{VIN\_3V3} – V_{LDO\_3V3}$ > 50 mV	0.5	1.1	1.75	Ω
ROUT_3V3	Output switch resistance from VIN_3V3 to VOUT_3V3			0.35	0.7	Ω
TR_OUT3V3	10-90% rise time on VOUT_3V3 from switch enable.	C_{VOUT_3V3} = 1 µF	35		120	µs

(1) I/O buffers are not fail-safe to LDO_3V3. Therefore, VDDIO may power-up before LDO_3V3. When VDDIO powers up before LDO_3V3, the I/Os shall not be driven high. When VDDIO is low and LDO_3V3 is high, the I/Os may be driven high.

6.6 Power Supervisor Characteristics

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
UV_LDO3V3	Under-voltage threshold for LDO_3V3. Locks out 1.8-V LDOs	LDO_3V3 rising	2.2	2.325	2.45	V
UVH_LDO3V3	Under-voltage hysteresis for LDO_3V3	LDO_3V3 falling	20	80	150	mV
UV_ADP_IN_LDO	Under-voltage threshold for ADP_IN to enable LDO	ADP_IN rising	3.35	3.75	3.95	V
UVH_ADP_IN_LDO	Under-voltage hysteresis for ADP_IN to enable LDO	ADP_IN falling	20	80	150	mV

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OV_ADP_IN	Over-voltage threshold for ADP_IN. This value is a 6-bit programmable threshold	ADP_IN rising	5		24	V
OVLSB_ADP_IN	Over-voltage threshold step for ADP_IN. This value is the LSB of the programmable threshold	ADP_IN rising		328		mV
OVH_ADP_IN	Over-voltage hysteresis for ADP_IN	ADP_IN falling, % of OV_ADP_IN	0.9%	1.3%	1.7%	
UV_ADP_IN	Under-voltage threshold for ADP_IN. This value is a 6-bit programmable threshold	ADP_IN falling	2.5		18.21	V
UVLSB_ADP_IN	Under-voltage threshold step for ADP_IN. This value is the LSB of the programmable threshold	ADP_IN falling		249		mV
UVH_ADP_IN	Under-voltage hysteresis for ADP_IN	ADP_IN rising, % of UV_ADP_IN	0.9%	1.3%	1.7%	
UVR_OUT3V3	Configurable under-voltage threshold for VOUT_3V3 rising. De-asserts RESETZ	Setting 0	2.019	2.125	2.231	V
		Setting 1	2.138	2.25	2.363	
		Setting 2	2.256	2.375	2.494	
		Setting 3	2.375	2.5	2.625	
		Setting 4	2.494	2.625	2.756	
		Setting 5	2.613	2.75	2.888	
		Setting 6	2.731	2.875	3.019	
		Setting 7	2.85	3	3.15	
UVRH_OUT3V3	Under-voltage hysteresis for VOUT_3V3 falling.	OUT_3V3 falling		30	50	mV
TUVRASSERT	Delay from falling VOUT_3V3 or MRESET assertion to RESETZ asserting low				75	µs
TUVRDELAY	Configurable delay from VOUT_3V3 to RESETZ de-assertion.		0		161.3	ms

6.7 Adapter Power Switch Characteristics

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS(2)	MIN	TYP	MAX	UNIT
IHVEXTACT	Active quiescent current from SENSEP pin, EN_HV = 1	Configured as source			1	mA
	Active quiescent current from ADP_IN pin, EN_HV = 1	Configured as sink			3.5	mA
IHVEXTSD	Shutdown quiescent current from SENSEP pin, EN_HV = 0				40	µA
IHVEXT_ACC	PP_EXT current sense accuracy (excluding RSENSE accuracy)	I = 100 mA , RSENSE = 10 mΩ Reverse current blocking disabled	3.5	5	6.5	A/V
		I = 200 mA, RSENSE = 10 mΩ	4	5	6	A/V
		I = 500 mA, RSENSE = 10 mΩ	4.4	5	5.6	A/V
		I ≥ 1 A, RSENSE = 10 mΩ	4.5	5	5.5	A/V
IGATEEXT(1)	External Gate Drive Current on HV_GATE1 and HV_GATE2		4	5	6	µA
VGSEXT	VGS voltage driving external FETs		4.5		7.5	V
ISS	Soft start charging current		5.5	7	8.5	µA
RSS_DIS	Soft start discharge resistance		0.6	1	1.4	kΩ
VTHSS	Soft start complete threshold		1.35	1.5	1.65	V
TSSDONE	Soft start complete time	CSS = 470 nF	68.3	99	129.7	ms
VREVPEXT	Reverse Current Blocking voltage Threshold for PP_EXT external switches		2	6	10	mV

(1) Limit the resistance from the HV_GATE1/2 pins to the external FET gate pins to < 1 Ω to provide adequate response time to short circuit events.
(2) Maximum capacitance on ADP_IN when configured as a source must not exceed 12 µF.

6.8 USB Endpoint Requirements and Characteristics

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TRANSMITTER(1)						
T_RISE_EP	Rising transition time	Low-speed (1.5 Mbps) data rate only	75		300	ns
T_FALL_EP	Falling transition time	Low-speed (1.5 Mbps) data rate only	75		300	ns

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_RRM_EP	Rise and fall time matching	Low-speed (1.5 Mbps) data rate only	–20%		25%	
V_XOVER_EP	Output crossover voltage		1.3		2	V
RS_EP	Source resistance of driver including 2nd Stage Port Data Multiplexer			34		Ω
DIFFERENTIAL RECEIVER (1)						
VOS_DIFF_EP	Input offset		–100		100	mV
VIN_CM_EP	Common Mode Range		0.8		2.5	V
RPU_EP	D– Bias Resistance	Receiving	1.425		1.575	kΩ
SINGLE ENDED RECEIVER(1)						
VTH_SE_EP	Single ended threshold	Signal rising/falling	0.8		2	V
VHYS_SE_EP	Single ended threshold hysteresis	Signal falling		200		mV

(1) The USB Endpoint PHY is functional across the entire VIN_3V3 operating range, but parameter values are only verified by design for VIN_3V3 ≥ 3.135 V

6.9 Analog-to-Digital Converter (ADC) Characteristics

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RES_ADC	ADC resolution			10		bits
F_ADC	ADC clock frequency		1.477	1.5	1.523	MHz
T_ENA	ADC enable time		42.14	43	43.86	µs
T_SAMPLEA	ADC input sample time		10.5	10.67	10.9	µs
T_CONVERTA	ADC conversion time		7.88	8	8.12	µs
T_INTA	ADC interrupt time		1.31	1.33	1.35	µs
LSB	Least significant bit		1.152	1.17	1.188	mV
DNL	Differential non-linearity		–0.65		0.65	LSB
INL	Integral non-linearity		–1.2		1.2	LSB
GAIN_ERR	Gain error (divider)		–1.5%		1.5%	
	Gain error (no divider)		–1		1	
VOS_ERR	Buffer offset error		–10		10	mV
THERM_ACC	Thermal sense accuracy		–8		8	°C
THERM_GAIN	Thermal slope			3.095		mV/°C
THERM_V0	Zero degree voltage			0.823		V

6.10 Input/Output (I/O) Requirements and Characteristics

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SPI						
SPI_VIH	High-level input voltage	LDO_3V3 = 3.3 V	2			V
SPI_VIL	Low-level input voltage	LDO_3V3 = 3.3 V			0.8	V
SPI_HYS	Input hysteresis voltage	LDO_3V3 = 3.3 V	0.2			V
SPI_ILKG	Leakage current	Output is Hi-Z, V_{IN} = 0 to LDO_3V3	–1		1	µA
SPI_VOH	SPI output high voltage	I_O = –8 mA, LDO_3V3 = 3.3 V	2.9			V
		I_O = –15 mA, LDO_3V3 = 3.3 V	2.5			
SPI_VOL	SPI output low voltage	I_O = 10 mA			0.4	V
		I_O = 20 mA			0.8	

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SWDIO						
SWDIO_VIH	High-level input voltage	LDO_3V3 = 3.3 V	2			V
SWDIO_VIL	Low-level input voltage	LDO_3V3 = 3.3 V			0.8	V
SWDIO_HYS	Input Hysteresis Voltage	LDO_3V3 = 3.3 V	0.2			V
SWDIO_ILKG	Leakage current	Output is Hi-Z, V_{IN} = 0 to LDO_3V3	–1		1	µA
SWDIO_VOH	Output high voltage	I_O = –8 mA, LDO_3V3 = 3.3 V	2.9			V
		I_O = –15 mA, LDO_3V3 = 3.3 V	2.5			
SWDIO_VOL	Output low voltage	I_O = 10 mA			0.4	V
		I_O = 20 mA			0.8	
SWDIO_RPU	Pullup resistance		2.8	4	5.2	kΩ
SWDIO_TOS	SWDIO output skew to falling edge SWDCLK		–5		5	ns
SWDIO_TIS	Input setup time required between SWDIO and rising edge of SWCLK		6			ns
SWDIO_TIH	Input hold time required between SWDIO and rising edge of SWCLK		1			ns
SWDCLK						
SWDCL_VIH	High-level input voltage	LDO_3V3 = 3.3 V	2			V
SWDCL_VIL	Low-level input voltage	LDO_3V3 = 3.3 V			0.8	V
SWDCL_THI	SWDIOCLK HIGH period		0.05		500	µs
SWDCL_TLO	SWDIOCLK LOW period		0.05		500	µs
SWDCL_HYS	Input hysteresis voltage	LDO_3V3 = 3.3 V	0.2			V
SWDCL_RPU	Pullup resistance		2.8	4	5.2	kΩ
GPIO, MRESET, RESETZ, ADP_POWER_CFG						
GPIO_VIH	High-level input voltage	LDO_3V3 = 3.3 V	2			V
		VDDIO = 1.8 V	1.25			
GPIO_VIL	Low-level input voltage	LDO_3V3 = 3.3 V			0.8	V
		VDDIO = 1.8 V			0.63	
GPIO_HYS	Input hysteresis Voltage	LDO_3V3 = 3.3 V	0.2			V
		VDDIO = 1.8 V	0.09			
GPIO_ILKG	I/O leakage current	INPUT = 0 V to VDD	–1		1	µA
GPIO_RPU	Pullup resistance	Pullup enabled	50	100	150	kΩ
GPIO_RPD	Pulldown resistance	Pulldown enabled	50	100	150	kΩ
GPIO_DG	Digital input path deglitch			20		ns
GPIO_VOH	GPIO output high voltage	I_O = –2 mA, LDO_3V3 = 3.3 V	2.9			V
		I_O = –2 mA, VDDIO = 1.8 V	1.35			
GPIO_VOL	GPIO output low voltage	I_O = 2 mA, LDO_3V3 = 3.3 V			0.4	V
		I_O = 2 mA, VDDIO = 1.8 V			0.45	
HRESET						
HRESET_VIH	High-level input voltage		1.25			V
HRESET_VIL	Low-level input voltage				0.63	V
HRESET_HYS	Input hysteresis Voltage		.09			V
HRESET_ILKG	I/O leakage current	INPUT = 0 V to LDO_1V8D	–1		1	µA
HRESET_THIGH	HRESET minimum high time to assert a reset condition.		2.0			ms
HRESET_TLOW	HRESET minimum low time to deassert a reset condition.		2.0			

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I2C_IRQ1Z, I2C_IRQ2Z						
OD_VOL	Low level output voltage	I_{OL} = 2 mA			0.4	V
OD_LKG	Leakage current	Output is Hi-Z, V_{IN} = 0 to LDO_3V3	–1		1	µA

6.11 I²C Slave Requirements and Characteristics

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SDA and SCL COMMON CHARACTERISTICS						
ILEAK	Input leakage current	Voltage on Pin = LDO_3V3	-3		3	µA
VOL	SDA output low voltage	IOL = 3mA, LDO_3V3 = 3.3 V			0.4	V
		IOL = 3mA, VDDIO = 1.8 V			0.36	
IOL	SDA max output low current	VOL = 0.4 V	3			mA
		VOL = 0.6 V	6			
VIL	Input low signal	LDO_3V3 = 3.3 V			0.99	V
		VDDIO = 1.8 V			0.54	
VIH	Input high signal	LDO_3V3 = 3.3 V	2.31			V
		VDDIO = 1.8 V	1.26			
VHYS	Input Hysteresis	LDO_3V3 = 3.3 V	0.17			V
		VDDIO = 1.8 V	0.09			
TSP	I²C pulse width suppressed				50	ns
CI	Pin Capacitance				10	pF
SDA and SCL STANDARD MODE CHARACTERISTICS						
FSCL	I²C clock frequency		0		100	kHz
THIGH	I²C clock high time		4			µs
TLOW	I²C clock low time		4.7			µs
TSUDAT	I²C serial data setup time		250			ns
THDDAT	I²C serial data hold time		0			ns
TVDDAT	I²C Valid data time	SCL low to SDA output valid			3.4	µs
TVDACK	I²C Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low			3.4	µs
TOCF	I²C output fall time	10-pF to 400-pF bus			250	ns
TBUF	I²C bus free time between stop and start		4.7			µs
TSTS	I²C start or repeated Start condition setup time		4.7			µs
TSTH	I²C Start or repeated Start condition hold time		4			µs
TSPS	I²C Stop condition setup time		4			µs

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SDA and SCL FAST MODE CHARACTERISTICS						
FSCL	I²C clock frequency		0		400	kHz
THIGH	I²C clock high time		0.6			µs
TLOW	I²C clock low time		1.3			µs
TSUDAT	I²C serial data setup time		100			ns
THDDAT	I²C serial data hold time		0			ns
TVDDAT	I²C Valid data time	SCL low to SDA output valid			0.9	µs
TVDACK	I²C Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low			0.9	µs
TOCF	I²C output fall time	10-pF to 400-pF bus, VDD = 3.3 V	12		250	ns
		10-pF to 400-pF bus, VDD = 1.8 V	6.5		250	
TBUF	I²C bus free time between stop and start		1.3			µs
TSTS	I²Cstart or repeated Start condition setup time		0.6			µs
TSTH	I²C Start or repeated Start condition hold time		0.6			µs
TSPS	I²C Stop condition setup time		0.6			µs

6.12 SPI Master Characteristics

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FSPI	Frequency of SPI_CLK		11.82	12	12.18	MHz
TPER	Period of SPI_CLK (1/F_SPI)		82.1	83.33	84.6	ns
TWHI	SPI_CLK High Width		30			ns
TWLO	SPI_CLK Low Width		30			ns
TDACT	SPI_SZZ falling to SPI_CLK rising delay time		30		50	ns
TDINACT	SPI_CLK falling to SPI_SSZ rising delay time		160		180	ns
TDMOSI	SPI_CLK falling to SPI_MOSI Valid delay time		–5		5	ns
TSUMISO	SPI_MISO valid to SPI_CLK falling setup time		21			ns
THDMSIO	SPI_CLK falling to SPI_MISO invalid hold time		0			ns
TRSPI	SPI_SSZ/CLK/MOSI rise time	10% to 90%, C_L = 5 pF to 50 pF, LDO_3V3 = 3.3 V	0.1		8	ns
TFSPI	SPI_SSZ/CLK/MOSI fall time	90% to 10%, C_L = 5 pF to 50 pF, LDO_3V3 = 3.3 V	0.1		8	ns

6.13 Single-Wire Debugger (SWD) Timing Requirements

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FSWD	Frequency of SWD_CLK				10	MHz
TPER	Period of SWD_CLK (1/FSWD)		100			ns
TWHI	SWD_CLK High Width		35			ns
TWLO	SWD_CLK Low Width		35			ns
TDOUT	SWD_CLK rising to SWD_DATA valid delay time		2		25	ns
TSUIN	SWD_DATA valid to SWD_CLK rising setup time		9			ns
THDIN	SWD_DATA hold time from SWD_CLK rising		3			ns
TRSWD	SWD Output rise time	10% to 90%, C_L = 5 pF to 50 pF, LDO_3V3 = 3.3 V	0.1		8	ns
TFSWD	SWD Output fall time	90% to 10%, C_L = 5 pF to 50 pF, LDO_3V3 = 3.3 V	0.1		8	ns

6.14 ADP_POWER_CFG Configuration Requirements

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VADP_EXT	ADP_POWER_CFG Voltage for receiving ADP_IN Power through the PP_EXT path				0.8	V
VADP_DIS	ADP_POWER_CFG Voltage for disabling system power from ADP_IN		2.4			V

6.15 Thermal Shutdown Characteristics

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TSD_MAIN	Thermal shutdown temperature of the main thermal shutdown	Temperature rising	145	160	175	°C
TSDH_MAIN	Thermal shutdown hysteresis of the main thermal shutdown	Temperature falling		20		°C
TSD_PWR	Thermal shutdown temperature of the power path block	Temperature rising	135	150	165	°C
TSDH_PWR	Thermal shutdown hysteresis of the power path block	Temperature falling		37		°C
TSD_DG	Programmable thermal shutdown detection deglitch time				0.1	ms

6.16 Oscillator Requirements and Characteristics

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FOSC_48M	48-MHz oscillator		47.28	48	48.72	MHz
FOSC_100K	100-kHz oscillator		95	100	105	kHz
RR_OSC	External oscillator set resistance (0.2%)		14.985	15	15.015	kΩ

7 Parameter Measurement Information

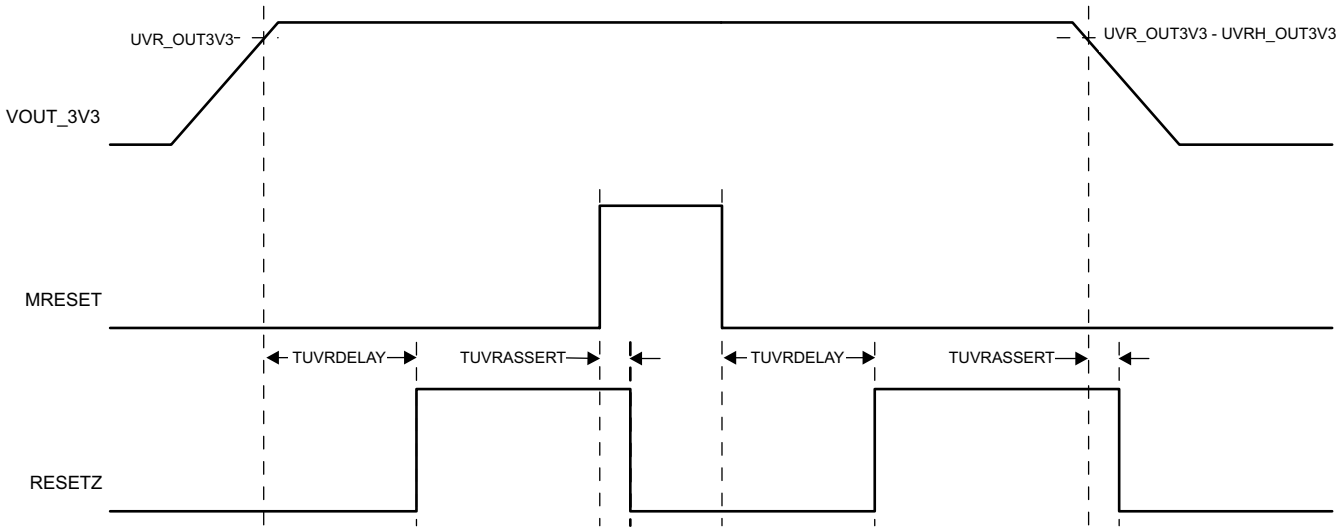


図 7-1. RESETZ Assertion Timing

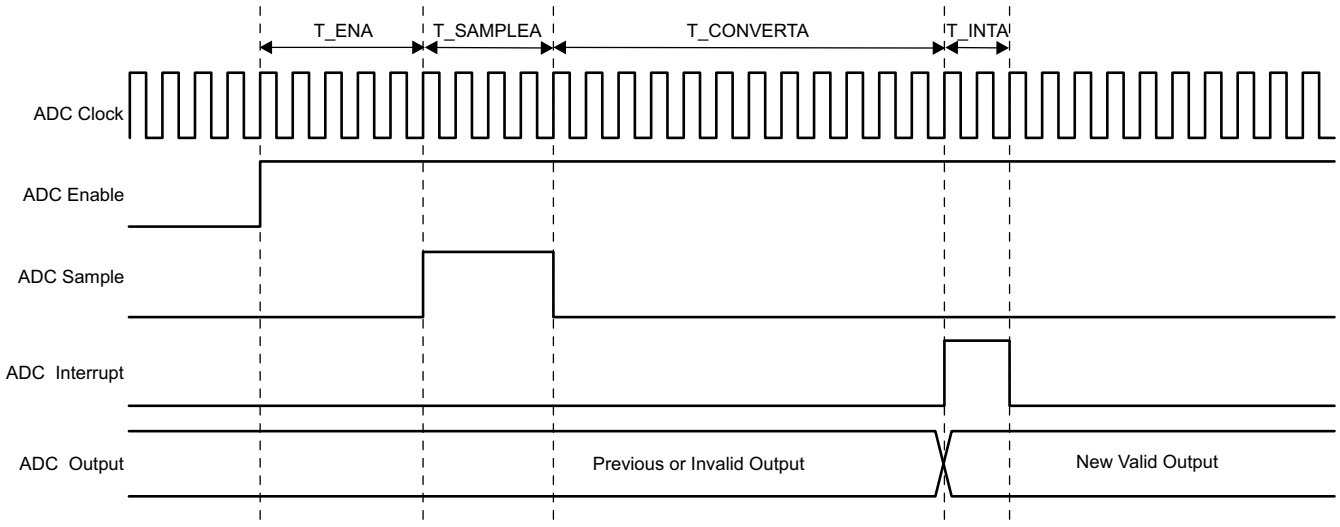


図 7-2. ADC Enable and Conversion Timing

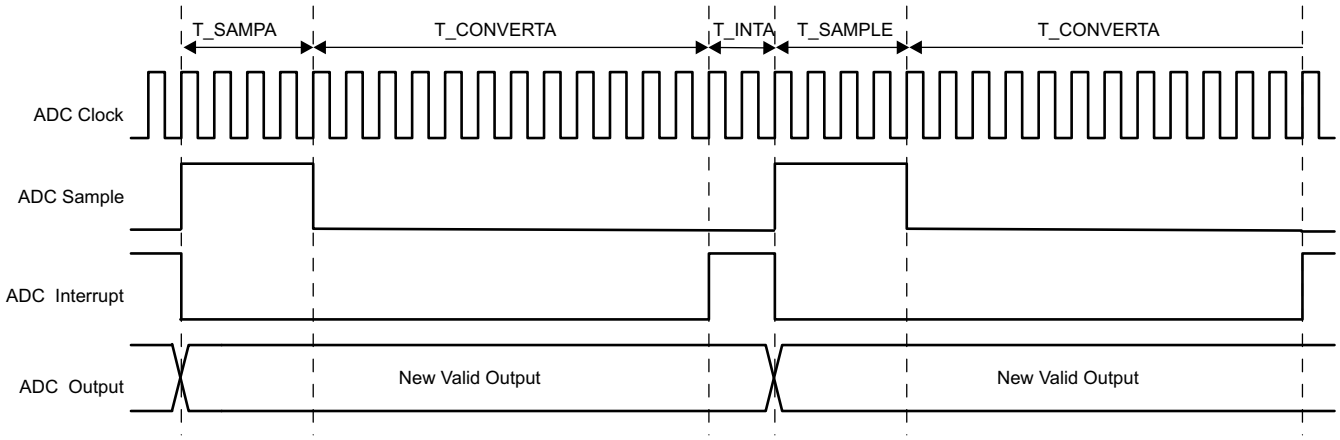


図 7-3. ADC Repeated Conversion Timing

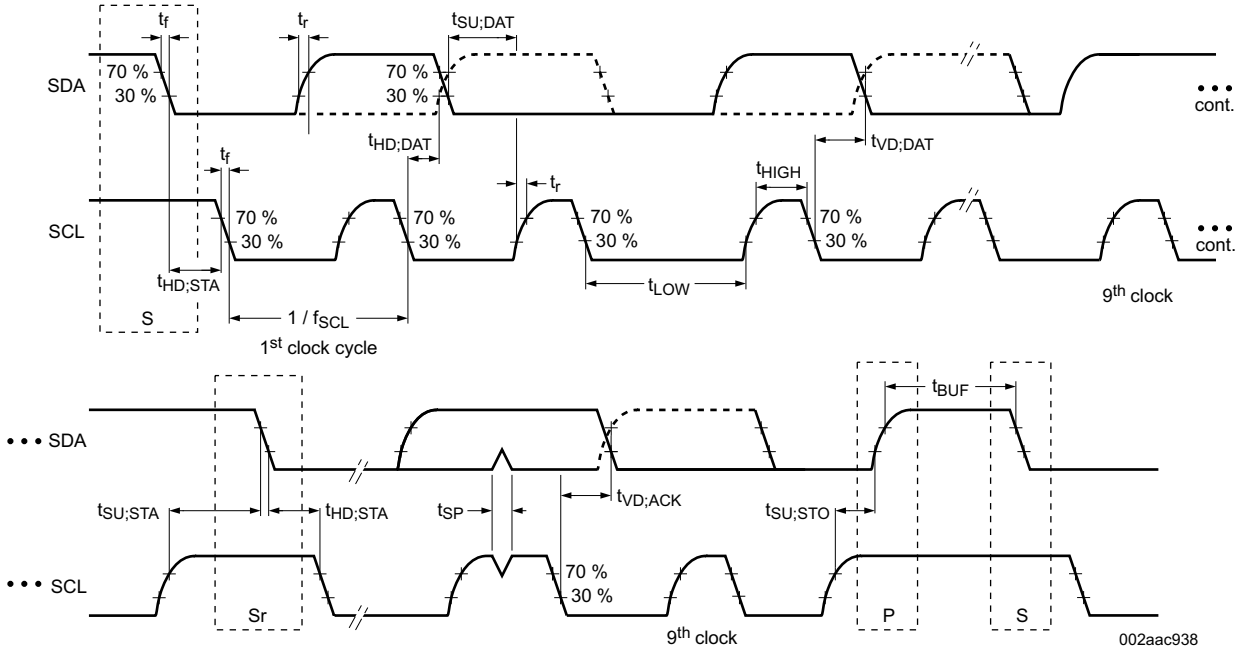


図 7-4. I²C Slave Interface Timing

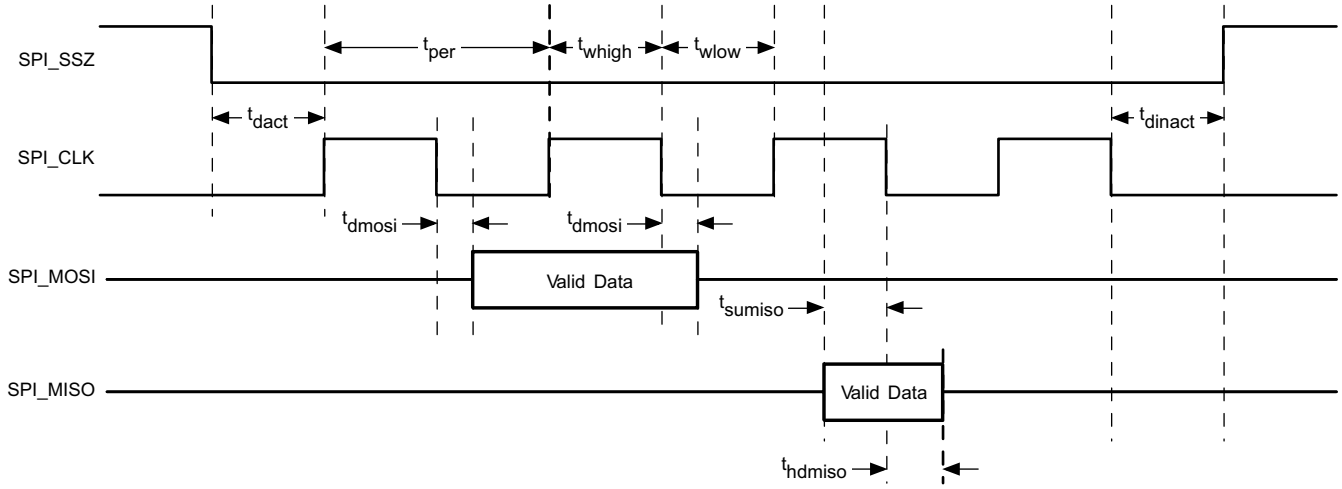


図 7-5. SPI Master Timing

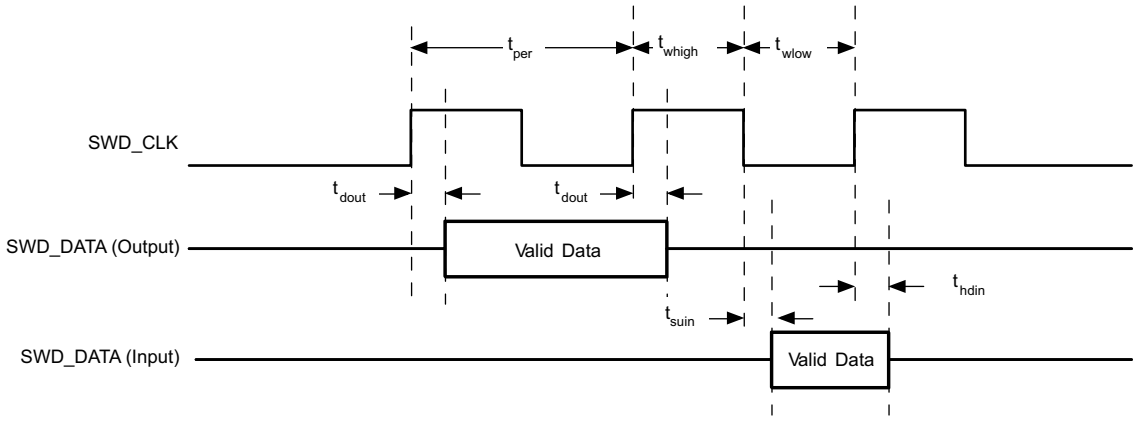


図 7-6. SWD Timing

8 Detailed Description

8.1 Overview

The TPS65982DMC is a simple dock management controller (DMC) for USB4 devices. The TPS65982 is capable of managing system power and alternate mode policy for system PD controllers such as the TPS65988DK. The integrated USB low-speed endpoint allows the TPS6598SDMC to provide in-field firmware update functionality for system PD controllers as well as billboard support. The TPS65982DMC may also control an input power adapter switch to soft-start system power and provide input power monitoring.

The TPS65982DMC is divided into four main sections: the adapter power switch, the port-data multiplexer, the power-management circuitry, and the digital core.

The adapter power switch provides power to the system through external switchec controlled by the integrated nFET gate drivers. For a high-level block diagram of the adapter power switch, a description of features, and more detailed circuitry, refer to the *Adapter Power Switch* section.

The port-data multiplexer connects the internal USB low speed controller to the UFP_USB and DBG_USB pins. For a high-level block diagram of the port-data multiplexer, a description of features, and more detailed circuitry, refer to the *USB Type-C Port Data Multiplexer* section.

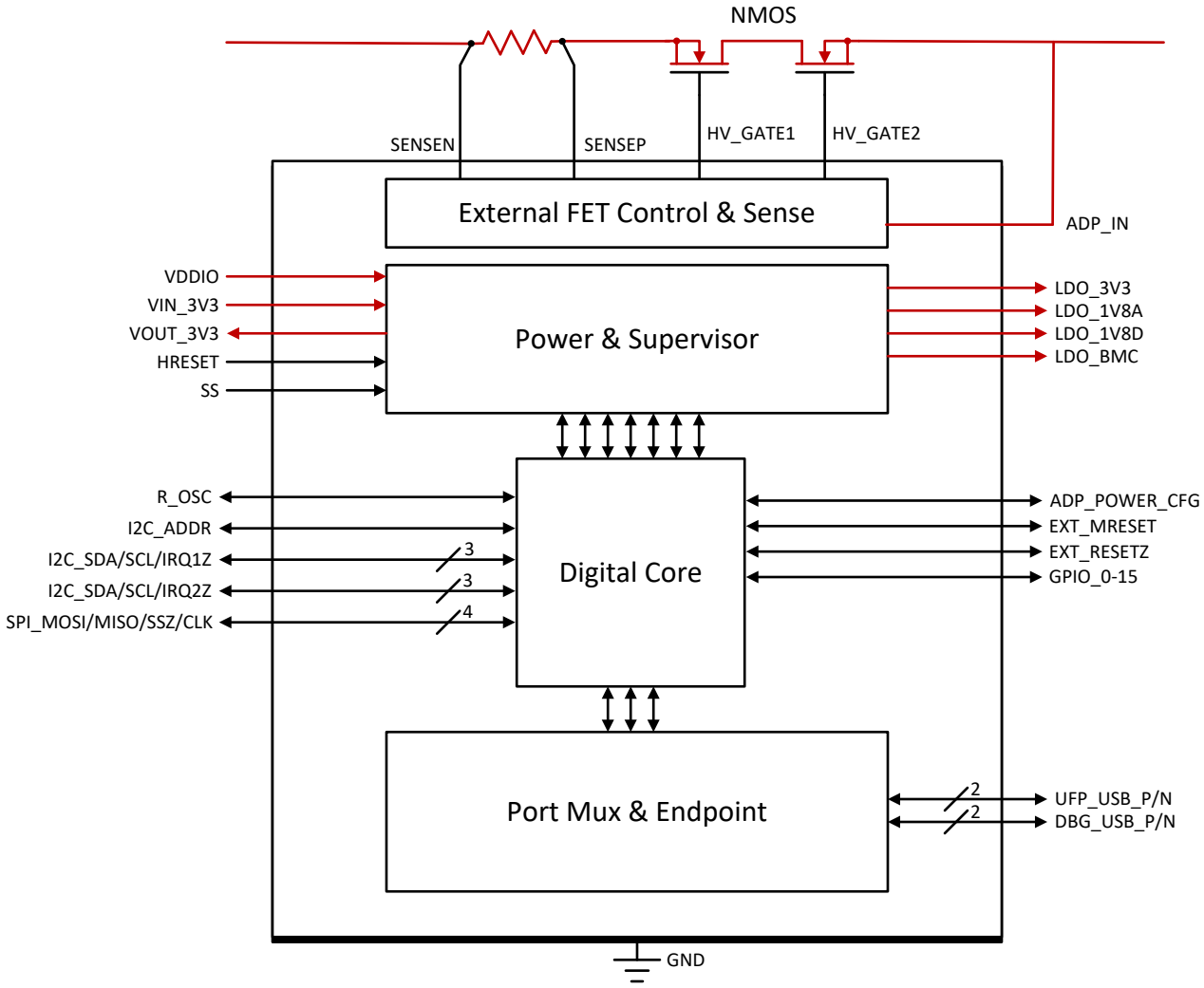
The power-management circuitry receives and provides power to the TPS65982DMC internal circuitry and to the VOUT_3V3 and LDO_3V3 outputs. For a high-level block diagram of the power-management circuitry, a description of features and, more detailed circuitry, refer to the *Power Management* section.

The digital core provides the engine for managing system policy, processing firmware updates, as well as handling control of all other TPS65982DMC functionality. A small portion of the digital core contains non-volatile memory, called boot code, which is capable of initializing the TPS65982DMC and loading a larger, configurable portion of application code into volatile memory in the digital core. For a high-level block diagram of the digital core, a description of features and, more detailed circuitry, refer to the *Digital Core* section.

The digital core of the TPS65982DMC also interprets and uses information provided by the analog-to-digital converter ADC (see the *ADC* section), is configurable to read the status of general purpose inputs and trigger events accordingly, and controls general outputs which are configurable as push-pull or open-drain types with integrated pullup or pulldown resistors and can operate tied to a 1.8 V or 3.3-V rail. The TPS65982DMC is an I^2C master to control system PD controllers (see the *I^2C Slave Interface* section), a SPI master to write to and read from an external flash memory (see the *SPI Master Interface* section), and is programmed by a single-wire debugger (SWD) connection (see the *Single-Wire Debugger Interface* section).

The TPS65982DMC also integrates a thermal shutdown mechanism (see *Thermal Shutdown* section) and runs off of accurate clocks provided by the integrated oscillators (see the *Oscillators* section).

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Adapter Power Switch

The TPS65982DMC is capable of controlling an external high-voltage, common-drain back-to-back NMOS FET switch path to sink up to 20 V at 10 A of current. The TPS65982DMC provides external control and sense to external NMOS power switches for currents greater than 3 A. The external NMOS switches are back-to-back to protect the system from large voltage differential across the FETs as well as blocking reverse current flow. Each NFET has a separate gate control. HV_GATE2 is always connected to the ADP_IN side and HV_GATE1 is always connected to the opposite side, referred to as PP_EXT. Two sense pins, SENSEP and SENSEN, are used to implement reverse current blocking, over-current protection, and current sensing.

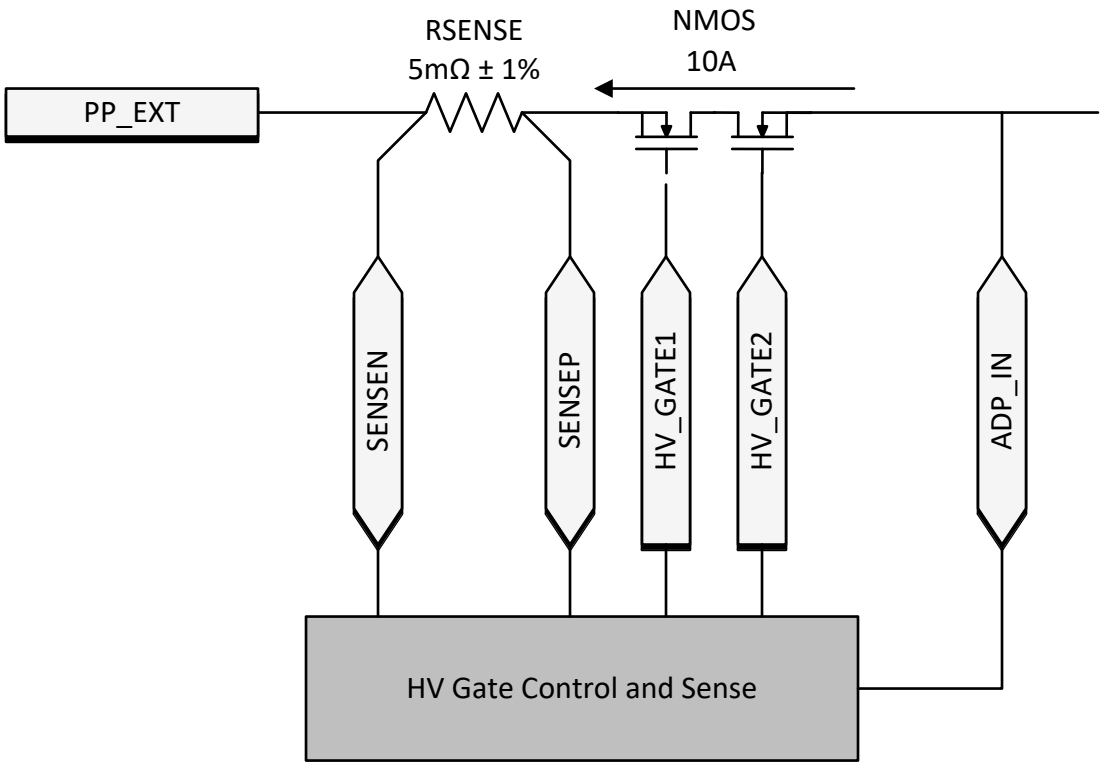


図 8-1. Adapter Power Switch

8.3.1.1 Adapter Switch with RSENSE

図 8-1 shows the configuration when the TPS65982DMC is acting as a sink for the external switch path. The external FETs must be connected in a common-drain configuration and will not work in a common source configuration. In this mode, current is sourced from ADP_IN. RSENSE provides an accurate current measurement and is used to initiate the current limiting feature of the external power path. The voltage between SENSEP (PP_EXT) and SENSEN (ADP_IN) is sensed to block reverse current flow. This measurement is also digitally readable via the ADC.

8.3.1.2 Adapter Switch without RSENSE

図 8-2 shows the configuration when the TPS65982DMC is acting as a sink for the external switch path without an RSENSE resistor. In this mode, current is sunk from ADP_IN to an internal system power node, referred to as PP_EXT. To block reverse current, the ADP_IN and SENSEP pins monitor the voltage across the NFETs. To ensure that SENSEN does not float, tie SENSEP to SENSEN in this configuration. When configured in this mode, the digital readout from current from the ADC will be approximately zero.

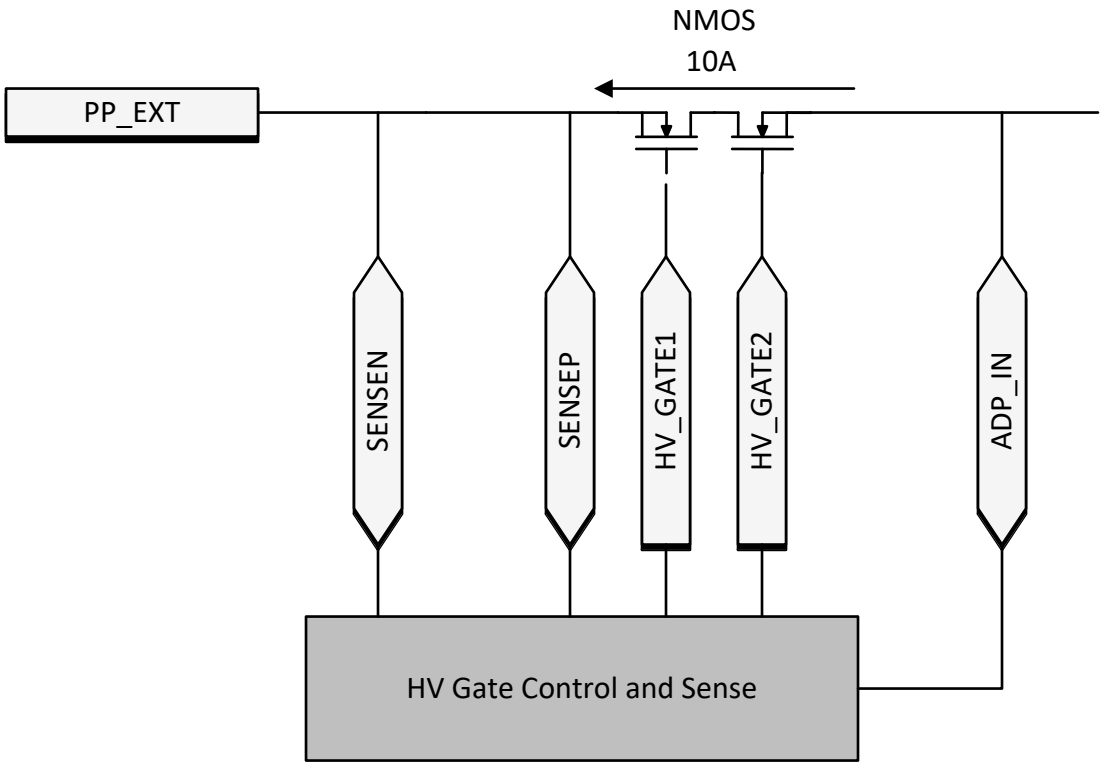


図 8-2. Adapter Switch without RSENSE

8.3.1.3 External Current Sense

The current through the external NFETs to ADP_IN is sensed through the RSENSE resistor and is available to be read digitally through the ADC. When controlling the adapter input, the readout from the ADC will only accurately reflect the current through the external NFETs when the connection of SENSEP and SENSEN adheres to セクション 8.3.1.

8.3.1.4 External Current Limit

The current through the external NFETs to ADP_IN is current limited when enabled. The current is sensed across the external RSENSE resistance. The current limit is set by a combination of the RSENSE magnitude and configuration settings for the voltage across the resistance. When the voltage across the RSENSE resistance exceeds the automatically set voltage limit, the current-limit circuit is activated.

8.3.1.5 Soft Start

When configured as a sink, the SS pin provides a soft start function for each of the high-voltage power path supplies (P_HV and external PP_EXT path) up to 5.5 V. The SS circuitry is shared for each path and only one path will turn on as a sink at a time. The soft start is enabled by application code or via the host processor. The SS pin is initially discharged through a resistance RSS_DIS. When the switch is turned on, a current ISS is sourced from the pin to a capacitance CSS. This current into the capacitance generates a slow ramping voltage. This voltage is sensed and the power path FETs turn on and the voltage follows this ramp. When the voltage reaches the threshold VTHSS, the power path FET will be near being fully turned on, the output voltage will be fully charged. At time TSSDONE, a signal to the digital core indicates that the soft start function has completed. The ramp rate of the supply is given by 式 1:

$$\text{Ramp Rate} = 17 \times \frac{\text{ISS}}{\text{CSS}} \tag{1}$$

8.3.1.6 ADP_POWER_CFG

At power-up, when VIN_3V3 is not present and ADP_IN is present, The TPS65982DMC will power itself from the ADP_IN rail (see *Power Management*) and execute boot code (see *Boot Code*). The boot code will observe the ADP_POWER_CFG voltage, which will fall into one of two voltage ranges: VBPZ_DIS, and VBPZ_EXT (defined in *ADP_POWER_CFG Configuration Requirements*).

When the voltage on ADP_POWER_CFG is in the VBPZ_DIS range (when ADP_POWER_CFG is tied to LDO_3V3 as in 図 8-3), this indicates that the TPS65982DMC will not close the adapter power switch and route ADP_IN to the entire system. In this case, the TPS65982DMC will load SPI-connected flash memory and execute this application code.

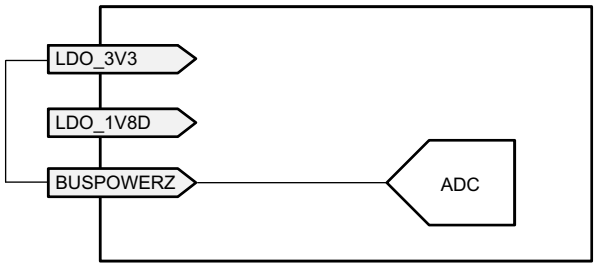


図 8-3. ADP_POWER_CFG Configured to Disable Power from ADP_IN

The ADP_POWER_CFG pin can also alternately configure the TPS65982DMC to power the entire system through the adapter power switch when the voltage on ADP_POWER_CFG is in the VBPZ_EXT range (when ADP_POWER_CFG is tied to GND as in 図 8-4).

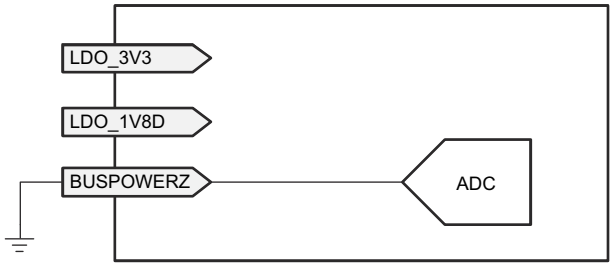


図 8-4. ADP_POWER_CFG Configured with PP_EXT as Input Power Path

8.3.2 USB Type-C Port Data Multiplexer

The Port Data Multiplexor routes the internal USB Low Speed endpoint between the endpoint port (UFP_USB_P and UFP_USB_N) and the debug port (DBG_USB_P and DBG_USB_N). The TPS65982DMC digital core selects the appropriate connection based on UFP PD state and application firmware configuration.

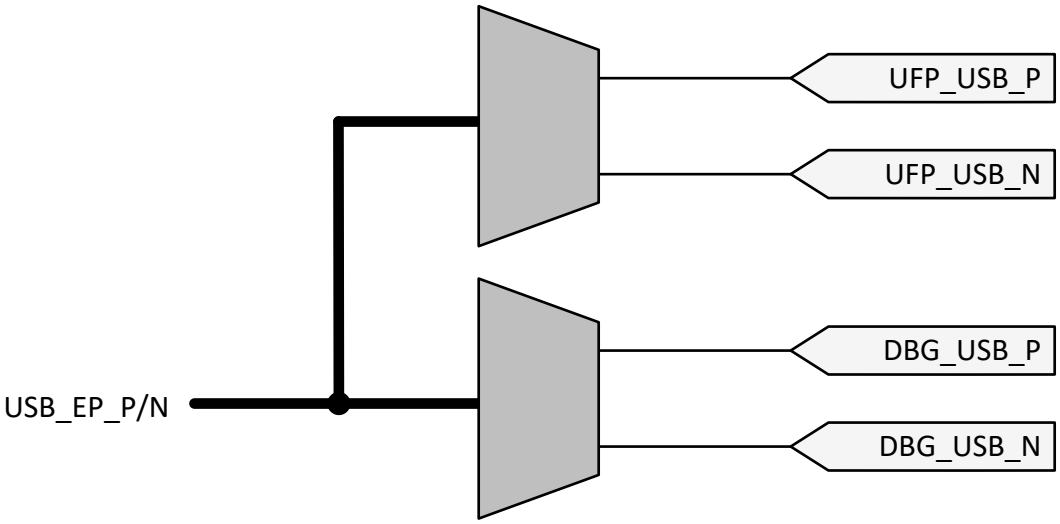


図 8-5. Port Data Multiplexers

8.3.2.1 USB2.0 Low-Speed Endpoint

The USB low-speed Endpoint is a USB 2.0 low-speed (1.5 Mbps) interface used to support HID class based accesses. The TPS65982DMC supports control of endpoint EP0. This endpoint enumerates to a USB 2.0 bus to provide USB-Billboard information to a host system as defined in the USB Type-C standard. EP0 is used for advertising the Billboard Class. When a host is connected to a device that provides Alternate Modes which cannot be supported by the host, the Billboard class allows a means for the host to report back to the user without any silent failures.

図 8-6 shows the USB Endpoint physical layer. The physical layer consists of the analog transceiver, the Serial Interface Engine, and the Endpoint FIFOs and supports low speed operation.

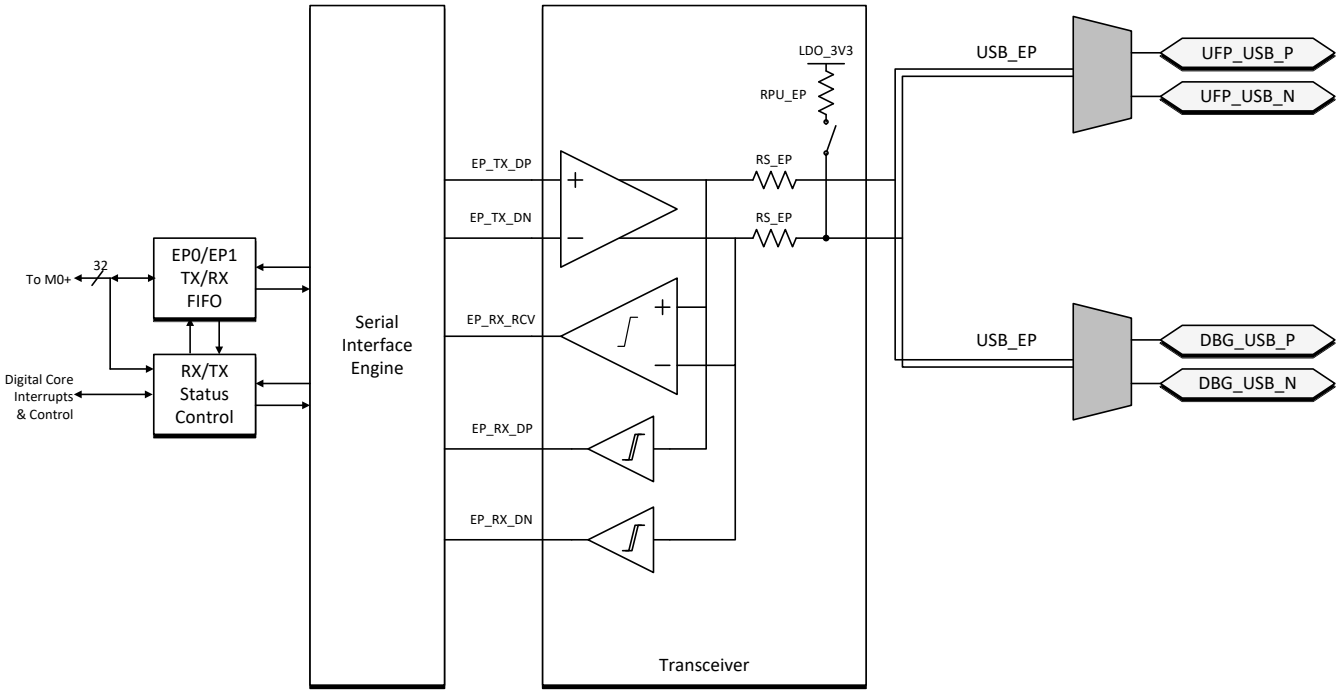


図 8-6. USB Endpoint Phy

The transceiver is made up of a fully differential output driver, a differential to single-ended receive buffer and two single-ended receive buffers on the D+/D– independently. The output driver drives the D+/D– of the selected output of the Port Multiplexer. The signals pass through the 2nd Stage Port Data Multiplexer to the port pins. When driving, the signal is driven through a source resistance RS_EP. RS_EP is shown as a single resistor in USB Endpoint Phy but this resistance also includes the resistance of the 2nd Stage Port Data Multiplexer defined in Port Data Multiplexer Requirements and Characteristics. RPU_EP is disconnected during transmit mode of the transceiver.

When the endpoint is in receive mode, the resistance RPU_EP is connected to the D– pin of the top or bottom port (UFP_USB_N or DBG_USB_N) depending on the operating condition. The RPU_EP resistance advertises low speed mode only.

8.3.3 Power Management

The TPS65982DMC Power Management block receives power and generates voltages to provide power to the TPS65982DMC internal circuitry. These generated power rails are LDO_3V3, LDO_1V8A, and LDO_1V8D. LDO_3V3 is also a low power output to load flash memory. VOUT_3V3 is a low power output that does not power internal circuitry that is controlled by application code and can be used to power other ICs in some applications. The power supply path is shown in 図 8-7.

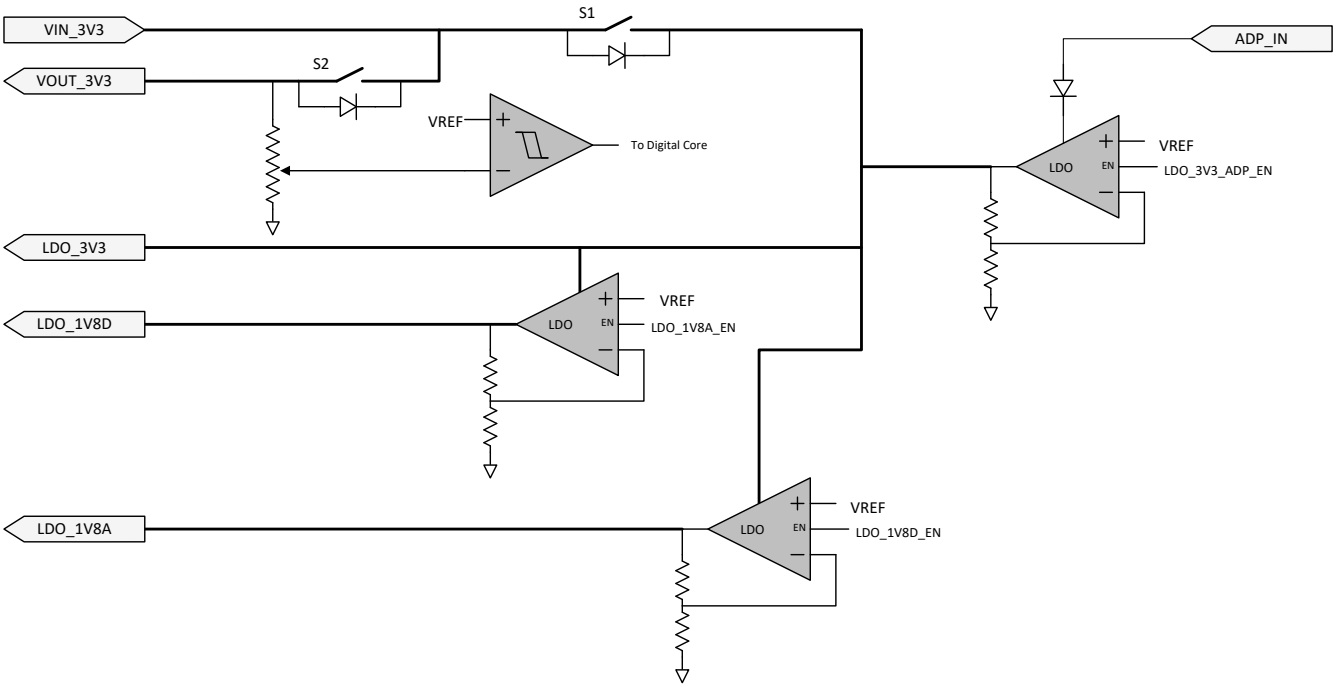


図 8-7. Power Supply Path

The TPS65982DMC is powered from either VIN_3V3 or ADP_IN. The normal power supply input is VIN_3V3. In this mode, current flows from VIN_3V3 to LDO_3V3 to power the core 3.3-V circuitry and the 3.3-V I/Os. A second LDO steps the voltage down from LDO_3V3 to LDO_1V8D and LDO_1V8A to power the 1.8-V core digital circuitry and 1.8-V analog circuits. When VIN_3V3 power is unavailable and power is available on ADP_IN, the TPS65982DMC will be powered from ADP_IN. In this mode, the voltage on ADP_IN is stepped down through an LDO to LDO_3V3. Switch S1 in 図 8-7 is unidirectional and no current will flow from LDO_3V3 to VIN_3V3 or VOUT_3V3.

8.3.3.1 Power-On and Supervisory Functions

A power-on-reset (POR) circuit monitors each supply. This POR allows active circuitry to turn on only when a good supply is present. In addition to the POR and supervisory circuits for the internal supplies, a separate programmable voltage supervisor monitors the VOUT_3V3 voltage.

8.3.3.2 Supply Switch-Over

VIN_3V3 takes precedence over ADP_IN, meaning that when both supply voltages are present the TPS65982DMC will power from VIN_3V3. Refer to The 図 8-7 for a diagram showing the power supply path block. There are two cases in with a power supply switch-over will occur. The first is when ADP_IN is present first and then VIN_3V3 becomes available. In this case, the supply will automatically switch-over to VIN_3V3 and brown-out prevention is verified by design. The other way a supply switch-over will occur is when both supplies are present and VIN_3V3 is removed and falls below 2.85 V. In this case, a hard reset of the TPS65982DMC occurs prompting a re-boot.

8.3.3.3 RESETZ and MRESET

The VIN_3V3 voltage is connected to the VOUT_3V3 output by a single FET switch (S2 in 図 8-7).

The enabling of the switch is controlled by the core digital circuitry and the conditions are programmable. A supervisor circuit monitors the voltage at VOUT_3V3 for an under-voltage condition and sets the external indicator RESETZ. The RESETZ pin is active low (low when an under-voltage condition occurs). The RESETZ output is also asserted when the MRESET input is asserted. The MRESET input is active-high by default, but is configurable to be active low. 図 7-1 shows the RESETZ timing with MRESET set to active high. When VOUT_3V3 is disabled, a resistance of RPDOUT_3V3 pulls down on the pin.

8.3.4 Digital Core

図 8-8 shows a simplified block diagram of the digital core. This diagram shows the interface between the digital and analog portions of the TPS65982DMC.

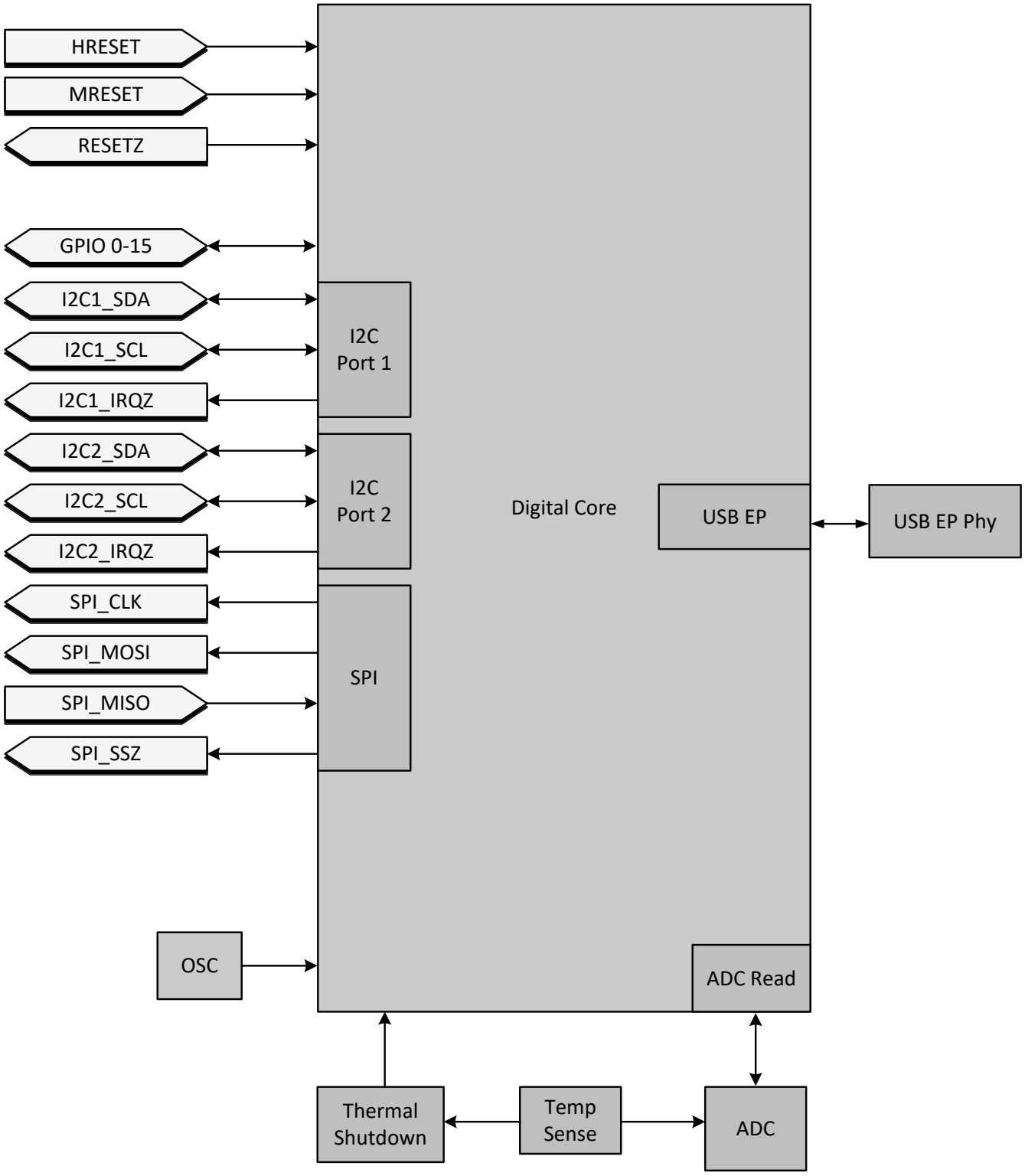


図 8-8. Digital Core Block Diagram

8.3.5 System Glue Logic

The system glue logic module performs various system interface functions such as control of the system interface for RESETZ, MRESET, and VOUT_3V3. This module supports various hardware timers for digital control of analog circuits.

8.3.6 Power Reset Congrol Module (PRCM)

The PRCM implements all clock management, reset control, and sleep mode control.

8.3.7 Interrupt Monitor

The Interrupt Control module handles all interrupt from the external GPIO as well as interrupts from internal analog circuits.

8.3.8 ADC Sense

The ADC Sense module is a digital interface to the SAR ADC. The ADC converts various voltages and currents from the analog circuits. The ADC converts up to 11 channels from analog levels to digital signals. The ADC can be programmed to convert a single sampled value.

8.3.9 I²C Slave

Two I²C interfaces provide interface to the digital core from the system. These interfaces are master/slave configurable and support low-speed and full-speed signaling. See the *I²C Slave Interface* section for more information.

8.3.10 SPI Master

The SPI master provides a serial interface to an external flash memory. The recommended memory is the W25Q80DV 8 Mbit Serial Flash Memory. A memory of at least 2 Mbit is required when the TPS65982DMC is using the memory in an unshared manner. A memory of at least 8 Mbit is required when the TPS65982DMC is using the memory in an shared manner. See the*SPI Master Interface* section for more information.

8.3.11 Single-Wire Debugger Interface

The SWD interface provides a mechanism to directly master the digital core.

8.3.12 ADC

図 8-9 shows the TPS65982DMC ADC. The ADC is a 10-bit successive approximation ADC. The input to the ADC is an analog input multiplexer that supports multiple inputs from various voltages and currents in the device. The output from the ADC is available to be read and used by application firmware. Each supply voltage into the TPS65982DMC is available to be converted including the port power path inputs and outputs.

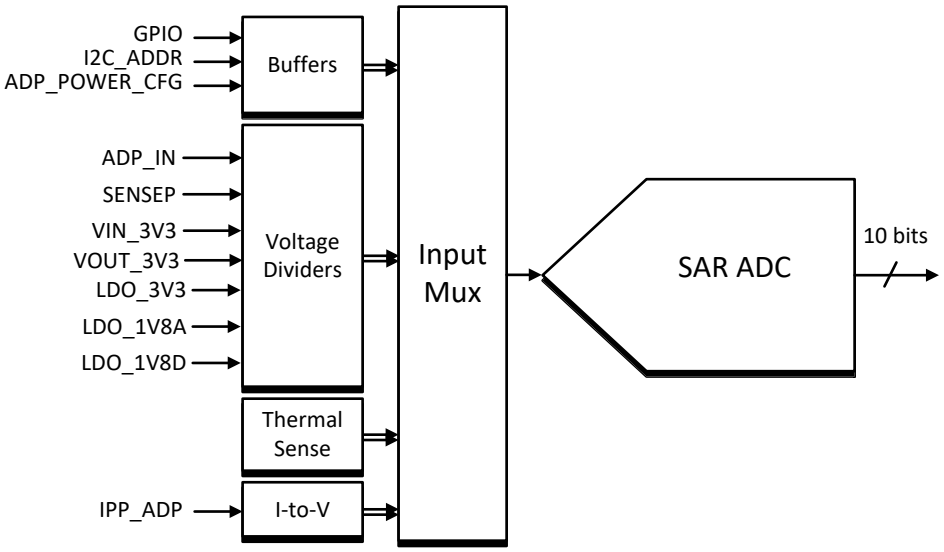


図 8-9. SAR ADC

8.3.12.1 ADC Divider Ratios

The ADC voltage inputs are each divided down to the full-scale input of 1.2 V. The ADC current sensing elements are not divided.

表 8-1 shows the divider ratios for each ADC input. The table also shows which inputs are auto-sequenced in the round robin automatic readout mode.

表 8-1. ADC Divider Ratios

CHANNEL #	SIGNAL	TYPE	AUTO-SEQUENCED	DIVIDER RATIO	BUFFERED
0	Thermal Sense	Temperature	Yes	N/A	No
1	ADP_IN	Voltage	Yes	25	No
2	SENSEP	Voltage	Yes	25	No
3	IPP_ADP	Current	Yes	N/A	No
4	Reserved	-	-	-	-
5	Reserved	-	-	-	-
6	Reserved	-	-	-	-
7	Reserved	-	-	-	-
8	Reserved	-	-	-	-
9	Reserved	-	-	-	-
10	Reserved	-	-	-	-
11	GPIO5	Voltage	No	1	No
12	Reserved	-	-	-	-
13	Reserved	-	-	-	-
14	Reserved	-	-	-	-
15	VIN_3V3	Voltage	No	3	No
16	VOUT_3V3	Voltage	No	3	No
17	Reserved	-	-	-	-
18	LDO_1V8A	Voltage	No	2	No
19	LDO_1V8D	Voltage	No	2	No
20	LDO_3V3	Voltage	No	3	No
21	I2C_ADDR	Voltage	No	3	Yes
22	GPIO0	Voltage	No	3	Yes
23	GPIO1	Voltage	No	3	Yes
24	GPIO2	Voltage	No	3	Yes
25	GPIO3	Voltage	No	3	Yes
26	GPIO4	Voltage	No	3	Yes
27	GPIO5	Voltage	No	3	Yes
28	GPIO6	Voltage	No	3	Yes
29	GPIO7	Voltage	No	3	Yes
30	GPIO8	Voltage	No	3	Yes
31	ADP_POWER_CFG	Voltage	No	3	Yes

8.3.12.2 ADC Operating Modes

The ADC is configured into one of three modes: single channel readout, round robin automatic readout and one time automatic readout.

8.3.12.3 Single Channel Readout

In Single Channel Readout mode, the ADC reads a single channel only. Once the channel is selected by firmware, a conversion takes place followed by an interrupt back to the digital core. 図 7-2 shows the timing diagram for a conversion starting with an ADC enable. When the ADC is disabled and then enabled, there is an enable time T_ADC_EN (programmable) before sampling occurs. Sampling of the input signal then occurs for

time T_SAMPLE (programmable) and the conversion process takes time T_CONVERT (12 clock cycles). After time T_CONVERT, the output data is available for read and an Interrupt is sent to the digital core for time T_INTA (2 clock cycles).

In Single Channel Readout mode, the ADC can be configured to continuously convert that channel. 図 7-3 shows the ADC repeated conversion process. In this case, once the interrupt time has passed after a conversion, a new sample and conversion occurs.

8.3.12.4 Round Robin Automatic Readout

When this mode is enabled, the ADC state machine will read from channel 0 to channel 11 and place the converted data into registers. The host interface can request to read from the registers at any time. During Round Robin Automatic Readout, the channel averaging must be set to 1 sample.

When the TPS65982DMC is running a Round Robin Readout, it will take approximately 696 µs (11 channels × 63.33 µs conversion) to fully convert all channels. Since the conversion is continuous, when a channel is converted, it will overwrite the previous result. Therefore, when all channels are read, any given value may be 649 µs out of sync with any other value.

8.3.12.5 One Time Automatic Readout

The One Time Automatic Readout mode is identical to the Round Robin Automatic Readout except the conversion process halts after the final channel is converted. Once all 11 channels are converted, an interrupt occurs to the digital core.

8.3.13 I/O Buffers

表 8-2 lists the I/O buffer types and descriptions. 表 8-3 lists the pin to I/O buffer mapping for cross-referencing a pin's particular I/O structure. The following sections show a simplified version of the architecture of each I/O buffer type.

表 8-2. I/O Buffer Type Description

BUFFER TYPE	DESCRIPTION
IOBUF_GPIOHSSWD	General Purpose High-Speed I/O
IOBUF_GPIOHSSPI	General Purpose High-Speed I/O
IOBUF_GPIOLS	General Purpose Low-Speed I/O
IOBUF_GPIOLSI2C	General Purpose Low-Speed I/O with I^2C deglitch time
IOBUF_I2C	I^2C Compliant Clock/Data Buffers
IOBUF_OD	Open-Drain Output
IOBUF_UTX	Push-Pull output buffer for UART
IOBUF_URX	Input buffer for UART
IOBUF_PORT	Input buffer between 1st/2nd stage Port Data Mux

表 8-3. Pin to I/O Buffer Mapping

I/O GROUP/PIN	BUFFER TYPE	SUPPLY CONNECTION (DEFAULT FIRST)
DEBUG1/2/3/4	IOBUF_GPIOLS	LDO_3V3, VDDIO
DEBUG_CTL1/2	IOBUF_GPIOLSI2C	LDO_3V3, VDDIO
ADP_POWER_CFG	IOBUF_GPIOLS	LDO_3V3, VDDIO
GPIO0-8	IOBUF_GPIOLS	LDO_3V3, VDDIO
I2C_IRQ1/2Z	IOBUF_OD	LDO_3V3, VDDIO
I2C_SDA1/2/SCL/1/2	IOBUF_I2C	LDO_3V3, VDDIO
LSX_P2R	IOBUF_UTX	LDO_3V3, VDDIO
LSX_R2P	IOBUF_URX	LDO_3V3, VDDIO
MRESET	IOBUF_GPIOLS	LDO_3V3, VDDIO
RESETZ	IOBUF_GPIOLS	LDO_3V3, VDDIO
UART_RX	IOBUF_URX	LDO_3V3, VDDIO

表 8-3. Pin to I/O Buffer Mapping (continued)

I/O GROUP/PIN	BUFFER TYPE	SUPPLY CONNECTION (DEFAULT FIRST)
UART_TX	IOBUF_UTX	LDO_3V3, VDDIO
PORT_INT	IOBUF_PORT	LDO_3V3
SPI_MOSI/MISO/CLK/SSZ	IOBUF_GPIOHSSPI	LDO_3V3
SWD_CLK/DATA	IOBUF_GPIOHSSWD	LDO_3V3

8.3.13.1 IOBUF_GPIOLS and IOBUF_GPIOLSI2C

図 8-10 shows the GPIO I/O buffer for all GPIOn pins listed GPIO0-GPIO17 in *Pin Functions*. GPIOn pins can be mapped to application-specific events to control other ICs, interrupt a host processor, or receive input from another IC. This buffer is configurable to be a push-pull output, a weak push-pull, or open drain output. When configured as an input, the signal can be a deglitched digital input or an analog input to the ADC. The push-pull output is a simple CMOS output with independent pulldown control allowing open-drain connections. The weak push-pull is also a CMOS output, but with GPIO_RPU resistance in series with the drain. The supply voltage to this buffer is configurable to be LDO_3V3 by default or VDDIO. For simplicity, the connection to VDDIO is not shown in 図 8-10, but the connection to VDDIO is fail-safe and a diode will not be present from GPIOn to VDDIO in this configuration. The pullup and pulldown output drivers are independently controlled from the input and are enabled or disabled via application code in the digital core.

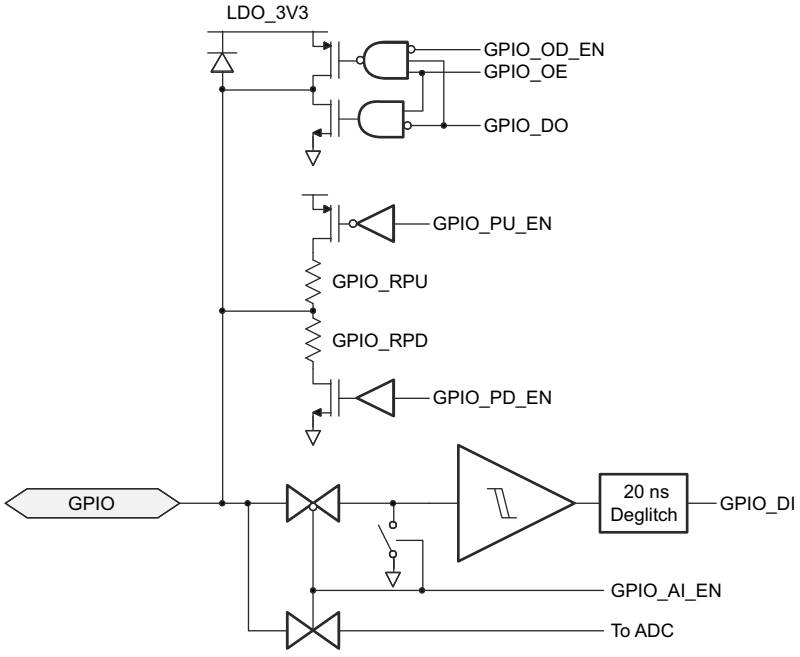


図 8-10. IOBUF_GPIOLS (General GPIO) I/O

図 8-11 shows the IOBUF_GPIOLSI2C that is identical to IOBUF_GPIOLS with an extended deglitch time.

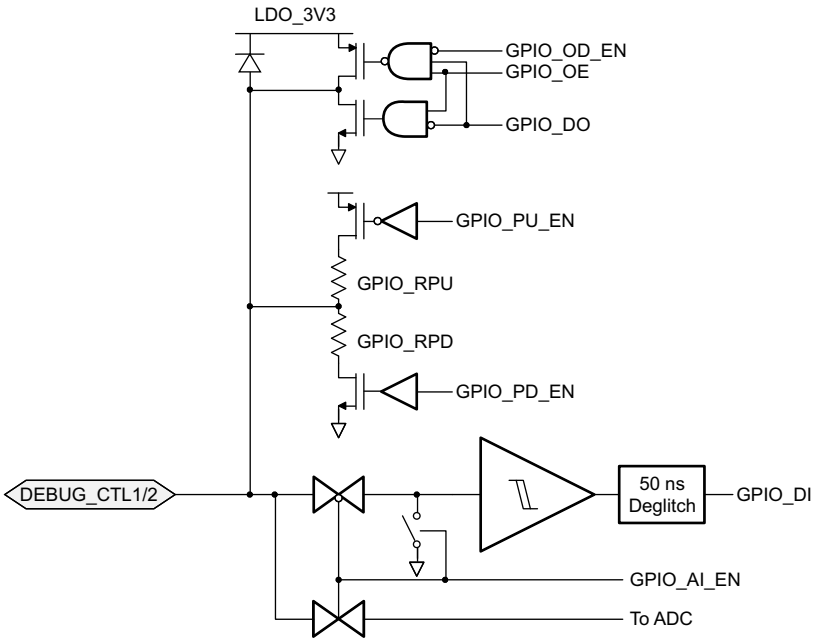


図 8-11. IOBUF_GPIOLSI2C (General GPIO) I/O with I²C Deglitch

8.3.13.2 IOBUF_OD

The open-drain output driver is shown in 図 8-12 and is the same push-pull CMOS output driver as the GPIO buffer. The output has independent pulldown control allowing open-drain connections.

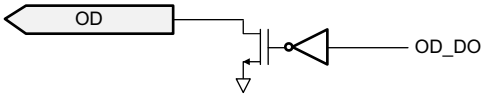


図 8-12. IOBUF_OD Output Buffer

8.3.13.3 IOBUF_I2C

The I²C I/O driver is shown in 図 8-13. This I/O consists of an open-drain output and an input comparator with deglitching. The supply voltage to this buffer is configurable to be LDO_3V3 by default or VDDIO. This is not shown in 図 8-13. Parameters for the I²C clock and data I/Os are found in *セクション 6.11*.

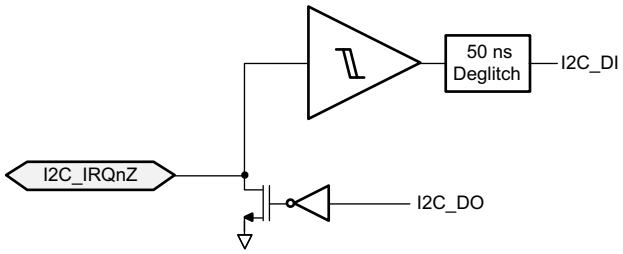


図 8-13. IOBUF_I2C I/O

8.3.13.4 IOBUF_GPIOHSPI

図 8-14 shows the I/O buffers for the SPI interface.

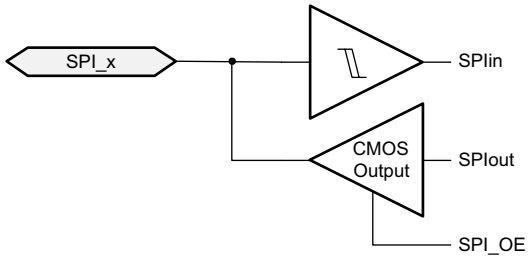


図 8-14. IOBUF_GPIOHSSPI

8.3.13.5 IOBUF_GPIOHSSWD

図 8-15 shows the I/O buffers for the SWD interface. The CLK input path is a comparator with a pullup SWD_RPU on the pin. The data I/O consists of an identical input structure as the CLK input but with a tri-state CMOS output driver.

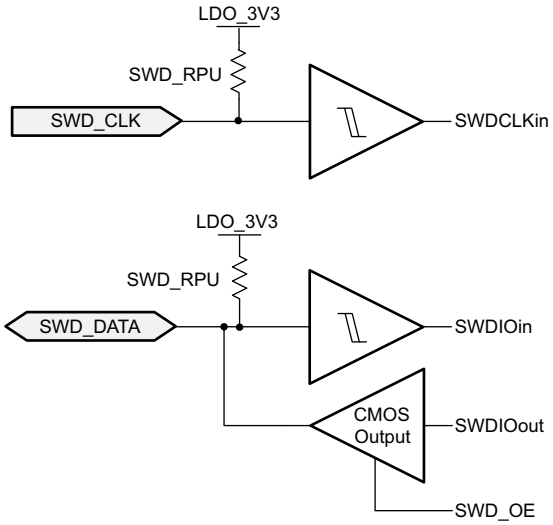


図 8-15. IOBUF_GPIOHSSWD

8.3.14 Thermal Shutdown

The TPS65982DMC has both a central thermal shutdown to the chip and a local thermal shutdown for the power path block. The central thermal shutdown monitors the temperature of the center of the die and disables all functions except for supervisory circuitry and halts digital core when die temperature goes above a rising temperature of TSD_MAIN. The temperature shutdown has a hysteresis of TSDH_MAIN and when the temperature falls back below this value, the device resumes normal operation. The power path block has its own local thermal shutdown circuit to detect an over temperature condition due to over current and quickly turn off the power switches. The power path thermal shutdown values are TSD_PWR and TSDH_PWR. The output of the thermal shutdown circuit is deglitched by TSD_DG before triggering. The thermal shutdown circuits interrupt to the digital core.

8.3.15 Oscillators

The TPS65982DMC has two independent oscillators for generating internal clock domains. A 48-MHz oscillator generates clocks for the core during normal operation and clocks for the USB 2.0 endpoint physical layer. An external resistance is placed on the R_OSC pin to set the oscillator accuracy. A 100-kHz oscillator generates clocks for various timers and clocking the core during low-power states.

8.4 Device Functional Modes

8.4.1 Boot Code

The TPS65982DMC has a Power-on-Reset (POR) circuit that monitors LDO_3V3 and issues an internal reset signal. The digital core, memory banks, and peripherals receive clock and RESET interrupt is issued to the digital core and the boot code starts executing. 図 8-16 provides the TPS65982DMC boot code sequence.

The TPS65982DMC boot code is loaded from OTP on POR, and begins initializing TPS65982DMC settings. This initialization includes enabling and resetting internal registers, loading trim values, waiting for the trim values to settle, and configuring the device I^2C addresses.

The unique I^2C address is based on the customer programmable OTP, DEBUG_CTLX pins, and resistor configuration on the I2C_ADDR pin.

Once initial device configuration is complete the boot code determines if the TPS65982DMC is booting under dead battery condition (VIN_3V3 invalid, ADP_IN valid). If the boot code determines the TPS65982DMC is booting under dead battery condition, the ADP_POWER_CFG pin is sampled to determine if the adapter power switch from ADP_IN should be enabled.

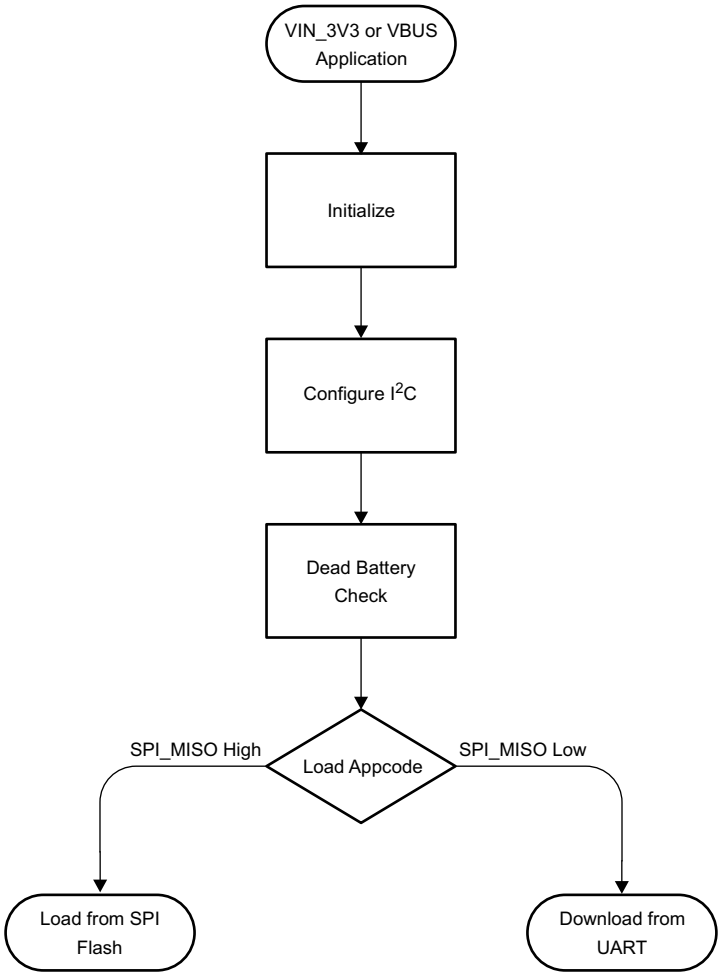


図 8-16. Flow Diagram for Boot Code Sequence

8.4.2 Initialization

During initialization the TPS65982DMC enables device internal hardware and loads default configurations. The 48-MHz clock is enabled and the TPS65982DMC persistence counters begin monitoring ADP_IN and VIN_3V3. These counters ensure the supply powering the TPS65982DMC is stable before continuing the initialization process. The initialization concludes by enabling the thermal monitoring blocks and thermal shutdown protection, along with the ADC, CRC, GPIO and NVIC blocks.

8.4.3 I²C Configuration

The TPS65982DMC features dual I²C busses with configurable addresses. The I²C addresses are determined according to the flow depicted in 図 8-17. The address is configured by reading device GPIO states at boot (refer to the *I²C Pin Address Setting* section for details). When the I²C addresses are established the TPS65982DMC enables a limited host interface to allow for communication with the device during the boot process.

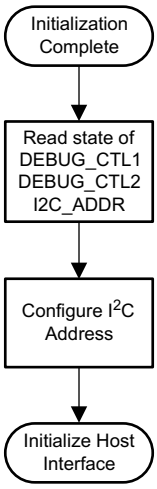


図 8-17. I²C Address Configuration

8.4.4 Application Code

The TPS65982DMC application code is stored in an external flash memory. The flash memory used for storing the TPS65982DMC application code may be shared with other devices in the system. The flash memory organization shown in 図 8-18 supports the sharing of the flash as well as the TPS65982DMC using the flash without sharing.

The flash is divided into two separate regions, the *Low Region* and the *High Region*. The size of this region is flexible and only depends on the size of the flash memory used. The two regions are used to allow updating the application code in the memory without over-writing the previous code. This ensures that the new updated code is valid before switching to the new code. For example, if a power loss occurred while writing new code, the original code is still in place and used at the next boot.

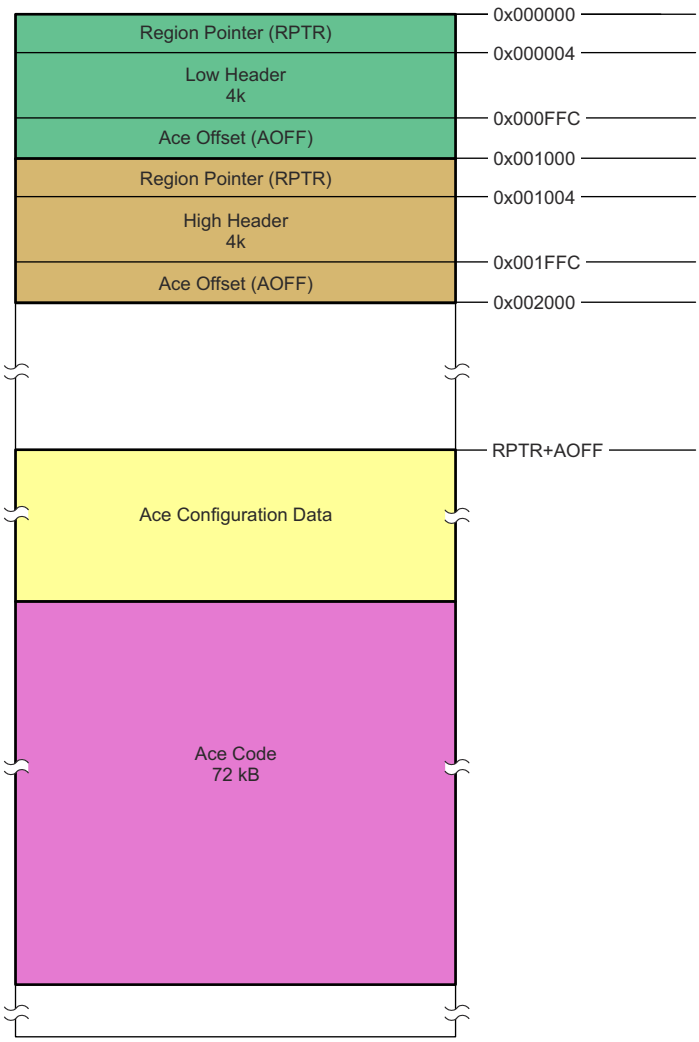


図 8-18. Flash Memory Organization

There are two 4-kB header blocks starting at address 0x000000h. The Low Header 4-kB block is at address 0x000000h and the High Header 4 kB block is at 0x001000h. Each header contains a Region Pointer (RPTR) that holds the address of the physical location in memory where the low region application code resides. Each also contains an Application Code Offset (AOFF) that contains the physical offset inside the region where the TPS65982DMC application code resides. The TPS65982DMC firmware physical location in memory is RPTR + AOFF. The first sections of the TPS65982DMC application code contain device configuration settings. This configuration determines the devices default behavior after power-up and can be customized using the TPS65982DMC Configuration Tool. These pointers may be valid or invalid. The Flash Read flow handles reading and determining whether a region is valid and contains good application code.

8.4.5 Flash Memory Read

The TPS65982DMC first attempts to load application code from the low region of the attached flash memory. If any part of the read process yields invalid data, the TPS65982DMC will abort the low region read and attempt to read from the high region. If both regions contain invalid data the device carries out the Invalid Memory flow. 図 8-19 shows the flash memory read flow.

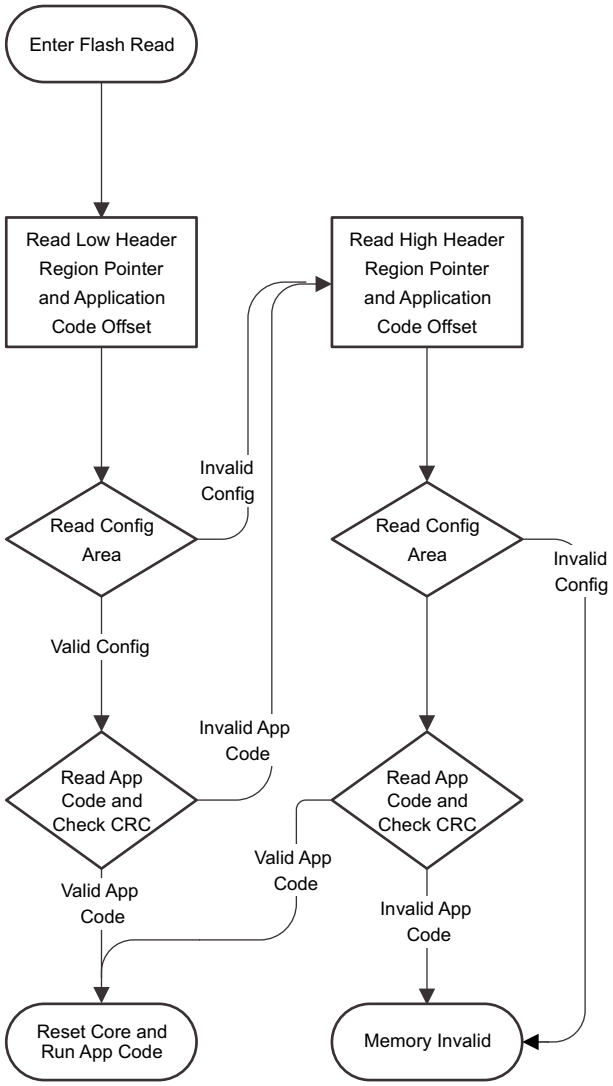


図 8-19. Flash Read Flow

8.4.6 Invalid Flash Memory

If the flash memory read fails because of invalid data, the TPS65982DMC carries out the memory invalid flow and presents the SWD interface on the USB Type-C SBU pins.

図 8-20 shows the invalid memory process.

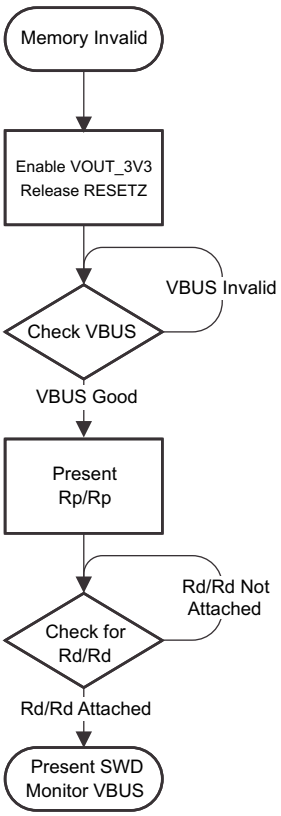


図 8-20. Memory Invalid Flow

8.5 Programming

8.5.1 SPI Master Interface

The TPS65982DMC loads flash memory during the *Boot Code* sequence. The SPI master electrical characteristics are defined in *SPI Master Characteristics* and timing characteristics are defined in 図 7-5. The TPS65982DMC is designed to power the flash from LDO_3V3 in order to support dead-battery or no-battery conditions, and therefore pullup resistors used for the flash memory must be tied to LDO_3V3. The flash memory IC must support 12 MHz SPI clock frequency. The size of the flash must be at least 1 Mbyte (equivalent to 8 Mbit) to hold the standard application code outlined in *Application Code*. The SPI master of the TPS65982DMC supports SPI Mode 0. For Mode 0, data delay is defined such that data is output on the same cycle as chip select (SPI_SSZ pin) becomes active. The chip select polarity is active-low. The clock phase is defined such that data (on the SPI_MISO and SPI_MOSI pins) is shifted out on the falling edge of the clock (SPI_CLK pin) and data is sampled on the rising edge of the clock. The clock polarity for chip select is defined such that when data is not being transferred the SPI_CLK pin is held (or idling) low. The minimum erasable sector size of the flash must be 4 kB. The W25Q80 flash memory IC is recommended. Refer to TPS65982DMC I^2C Host Interface Specification for instructions for interacting with the attached flash memory over SPI using the host interface of the TPS65982DMC.

8.5.2 I^2C Slave Interface

The TPS65982DMC has two I^2C interface ports. I^2C Port 1 is comprised of the I2C_SDA1, I2C_SCL1, and I2C_IRQ1Z pins. I^2C Port 2 is comprised of the I2C_SDA2, I2C_SCL2, and I2C_IRQ2Z pins. These interfaces

provide general status information about the TPS65982DMC, the ability to control the TPS65982DMC behavior, as well as providing control of system PD controllers.

The two ports can be a master or a slave, but the default behavior is to be a slave. Port 1 and Port 2 are interchangeable. Each port operates the same way and has the same access in and out of the core. An interrupt mask is set for each that determines what events are interrupted on that given port.

8.5.2.1 I²C Interface Description

The TPS65982DMC support Standard and Fast mode I²C interface. The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a supply through a pullup resistor. Data transfer may be initiated only when the bus is not busy.

A master sending a Start condition, a high-to-low transition on the SDA input/output, while the SCL input is high initiates I²C communication. After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/W).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period as changes in the data line at this time are interpreted as control commands (Start or Stop). The master sends a Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high.

Any number of data bytes can be transferred from the transmitter to receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period. When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation

A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. The master receiver holding the SDA line high does this. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.

図 8-21 shows the start and stop conditions of the transfer. 図 8-22 shows the SDA and SCL signals for transferring a bit. 図 8-23 shows a data transfer sequence with the ACK or NACK at the last clock pulse.

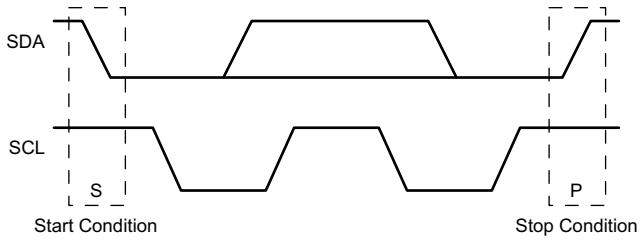


図 8-21. I²C Definition of Start and Stop Conditions

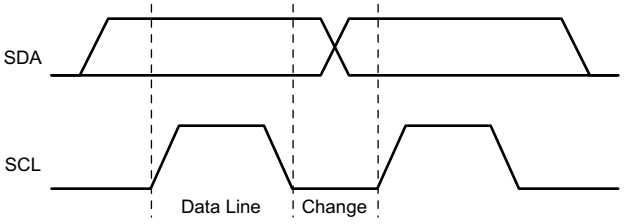


図 8-22. I²C Bit Transfer

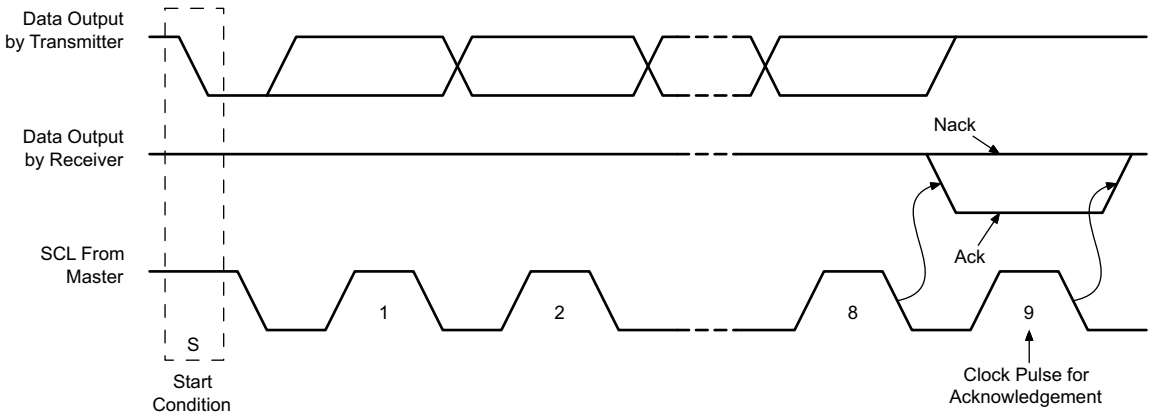


図 8-23. I²C Acknowledgment

8.5.2.2 I²C Clock Stretching

The TPS65982DMC features clock stretching for the I²C protocol. The TPS65982DMC slave I²C port may hold the clock line (SCL) low after receiving (or sending) a byte, indicating that it is not yet ready to process more data. The master communicating with the slave must not finish the transmission of the current bit and must wait until the clock line actually goes high. When the slave is clock stretching, the clock line will remain low.

The master must wait until it observes the clock line transitioning high plus an additional minimum time (4 µs for standard 100-kbps I²C) before pulling the clock low again.

Any clock pulse may be stretched but typically it is the interval before or after the acknowledgment bit.

8.5.2.3 I²C Address Setting

The boot code sets the hardware configurable unique I²C address of the TPS65982DMC before the port is enabled to respond to I²C transactions. The unique I²C address is determined by the analog level set by the analog I2C_ADDR strap pin (three bits) as shown in 表 8-4.

表 8-4. I²C Default Unique Address

Default I²C Unique Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	0	0	I2C_ADDR_DECODE[2:0]			R/W
Note 1: Any bit is maskable for each port independently providing firmware override of the I²C address.							

8.5.2.4 Unique Address Interface

The Unique Address Interface allows for complex interaction between an I²C master and a single TPS65982DMC. The I²C Slave sub-address is used to receive or respond to Host Interface protocol commands. 図 8-24 and 図 8-25 show the write and read protocol for the I²C slave interface, and a key is included in 図 8-26 to explain the terminology used. The key to the protocol diagrams is in the SMBus Specification and is repeated here in part.

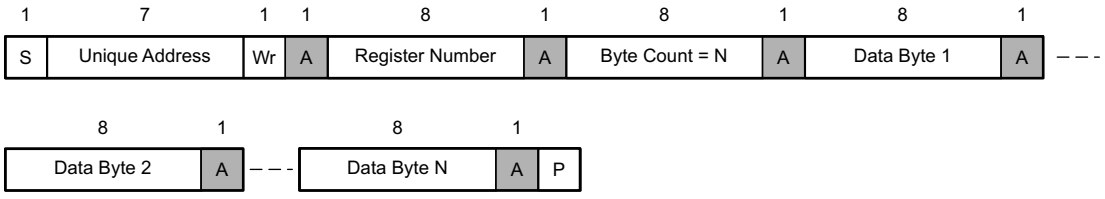


図 8-24. I²C Unique Address Write Register Protocol

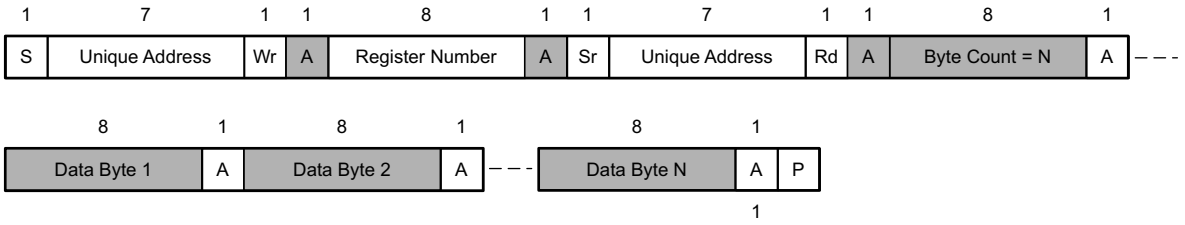


図 8-25. I²C Unique Address Read Register Protocol

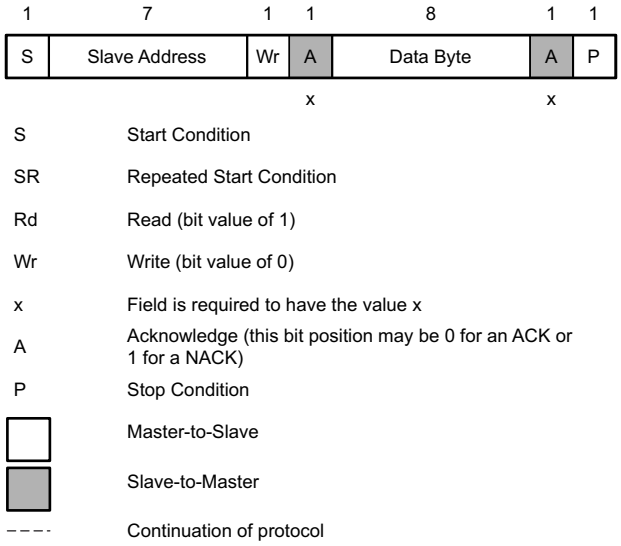


図 8-26. I²C Read/Write Protocol Key

8.5.2.5 I²C Pin Address Setting

To enable the setting of multiple I²C addresses using a single TPS65982DMC pin, a resistance is placed externally on the I2C_ADDR pin. The internal ADC then decodes the address from this resistance value. 図 8-27 shows the decoding. DEBUG_CTL1/2 are checked at the same time for the DC condition on this pin (high or low) for setting other bits of the address described previously. Note, DEBUG_CTL1/2 are GPIO and the address decoding is done by firmware in the digital core.

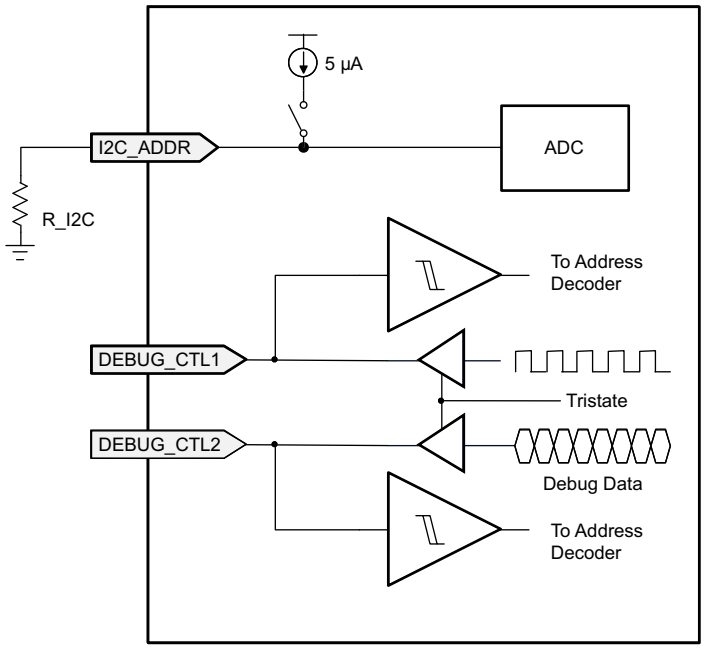


図 8-27. I²C Address Decode

表 8-5 lists the external resistance needed to set bits [3:1] of the I²C Unique Address. For the master TPS65982DMC, the pin is grounded.

表 8-5. I²C Address Resistance

TPS65982DMC DEVICE	EXTERNAL RESISTANCE (1%)	I²C UNIQUE ADDRESS [3:1]
Master 0	0	0x00
Slave 7	38.3 k	0x01
Slave 6	84.5 k	0x02
Slave 5	140 k	0x03
Slave 4	205 k	0x04
Slave 3	280 k	0x05
Slave 2	374 k	0x06
Slave 1	Open	0x0F

9 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The typical applications of the TPS65982DMC is as a system policy manager for USB4 docks and hubs with a single upstream facing port (UFP) capable of sourcing high voltage, and multiple downstream facing ports (DFP).

9.2 Typical Application

9.2.1 USB4 Device Application with Host Charging

The figure below shows a USB4 Device application, where there are a total of four Type-C PD Ports. One port is the main connection to a USB4 Host that is a UFP in terms of data and a source of power. The other three ports are DFPs in terms of data and source power. Generally the main UFP source Type-C PD port provides the highest power (up to 100 W) to charge a USB4 Host. The key four devices in the system are the PD Controller (2), Dock Management Controller, USB4 Hub Controller, and UFP Variable Power Supply.

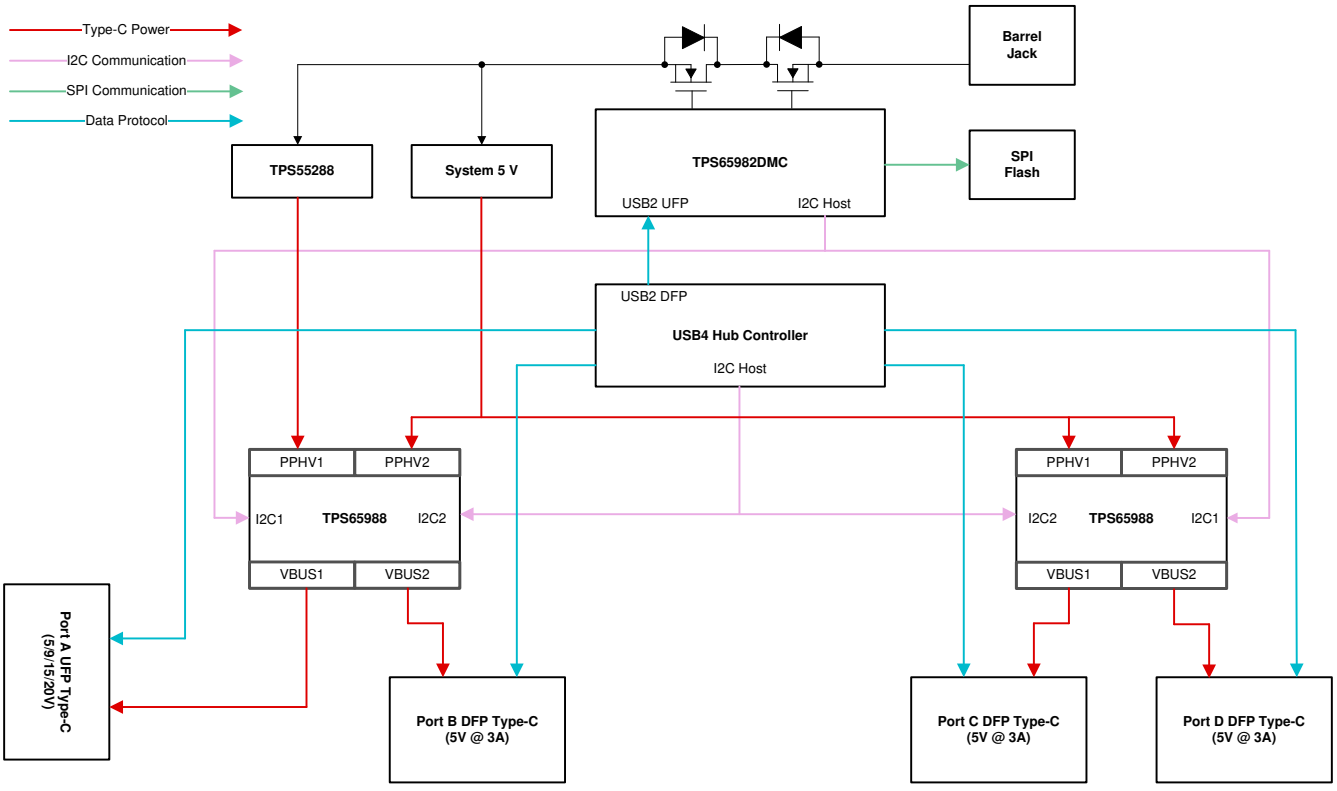


図 9-1. USB4 Device Block Diagram

In this application, two dual port TPS65988DK PD controllers are used to determine the connection and provide power on the Type-C ports. The primary TPS65988DK manages Port A (UFP Source) and Port B (DFP Source). The secondary TPS65988DK manages the other two, Port C (DFP Source) and Port D (DFP Source). For systems that do not need all four ports a combination of TPS65988DK and TPS65987DDK may be used to scale for specific design requirements. The PD controllers have two I2C clients that are controlled by the Dock

Management Controller and the USB4 Hub Controller. The PD controllers have an optional I2C Host that may be used to control a variable power supply.

The Dock Management Controller (DMC), TPS65982DMC, main functions are the Connection Manager, Power Manager, Input Power Control, Secure Firmware Update & booting of the PD controllers. The Connection Manager determines the capabilities of the UFP connection and sets the DFP capabilities accordingly. The Power Manager keeps the power allocated to each of the Type-C ports within a specific power budget and also monitors the entire system power to keep from over loading the Barrel Jack adapter supply. The DMC also controls the input power to the system and soft starts the power path to prevent large inrush currents when the Barrel Jack supply is connected. The Secure Firmware Update is accomplished over USB2, the DMC is connected to one of the USB2 DFP ports on the USB4 Hub Controller or USB2 Hub in the system. The DMC provides the Secure Firmware Update for itself and the PD controllers. The DMC will boot the PD controllers over the I2C connection. The I2C connection between the DMC and PD controllers also serves as communication channel for the Connection and Power Manager.

The USB4 Hub Controller manages the data paths for all of the Type-C ports and determines the required data protocol by reading the PD controller status over I2C connection. The UFP port is the main connection to the USB4 Hub Controller from a USB4 host. The other DFP ports act as expansion ports to connect other USB Type-C & PD devices.

The UFP Variable Power Supply provides 5 V/9 V/15 V/20 V up to 100 W to charge the connected USB4 host. The TPS55288 is used in this application since it is capable of tightly regulating the output voltage and current. The TPS55288 is best connected to the I2C Host on the Primary PD controller, to set the output voltage and current regulation. The other DFP ports generally support 5 V @ 3 A to connect to Type-C & PD devices.

9.2.1.1 Design Requirements

9.2.1.1.1 Power Supply Design Requirements

表 9-1 shows the Power Design parameters for the USB4 Device application.

表 9-1. Power Supply Design Requirements

Power Design Parameters	Value	Current Path
UFP Source Port A	5 V/9 V/15 V/20 V @ 5 A	Host Charging VBUS
DFP Source Port B/C/D	5 V @ 9 A (3 A per Port)	DFP VBUS
PP_CABLE Port A/B/C/D	5 V @ 2 A (500 mA per Port)	VCONN Source
DMC External Input Path	20 V @ 10 A (Imax Sensed)	USB4 Device Input Power
VIN_3V3 PD Controller & DMC	3.3 V @ 150 mA (50 mA per device)	PD Controller& DMC Power

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 USB Power Delivery Source Capabilities

表 9-2 summarizes the source PDOs for all of the ports for the USB4 Device.

表 9-2. Source Capabilities

Port	PDO Types	Voltage	Current
Port A	Fixed	5 V/9 V/15 V/20 V	3 A/3 A/3 A/5 A
Port B	Fixed	5 V	3 A
Port C	Fixed	5 V	3 A
Port D	Fixed	5 V	3 A

9.2.1.2.2 USB Power Delivery Sink Capabilities

The UFP Source port is the only DRP port that may connect as a DFP or UFP which means that it should have at least one sink capability when connected as a UFP. The DFP ports can only connect as a DFP, where they do not have any sink capabilities.

表 9-3. Sink Capabilities

Port	PDO Types	Voltage	Current
Port A	Fixed	5 V	0 A

9.2.1.2.3 Supported Data Modes

USB4 Hub Controllers may vary on the data supported on the UFP and DFP ports. In this specific example the USB4 Hub Controllers support USB3, DisplayPort, Thunderbolt, and USB4 on the UFP Port. The DFP Ports will also support these modes when connected to other Type-C & PD devices.

表 9-4. Data Modes

Mode of Operation	Data	Data Role
USB Data	USB3.1 Gen2	UFP: Device, DFP: Host
DisplayPort	DP Video	UFP: UFP_D, DFP: DFP_D
Thunderbolt	PCIe/DP Video	UFP: Host/Device, DFP: Host
USB4	Tunneled USB3/PCIe/DP	UFP: Device, DFP Host

9.2.1.2.4 USB4 Hub Controller & PD Controller I2C Communication

The I2C connection from the PD controllers and the USB4 Hub Controller communicates the connection present at the Type-C Ports. Each port on the USB4 controller may have its I2C interrupt pin to notify the USB4 Hub Controller which port has a new connection. The PD controllers have an option to use the shared interrupt for both ports or to have a separate interrupt for each port that is mapped to a GPIO in its configuration. In the shared interrupt case, the USB4 Hub Controller will query both port addresses and will determine which port has a data connection. For the dedicated interrupt the USB4 hub controller will only query the specific port address and determine the connection present.

図 9-2 shows the dedicated GPIO interrupt connection.

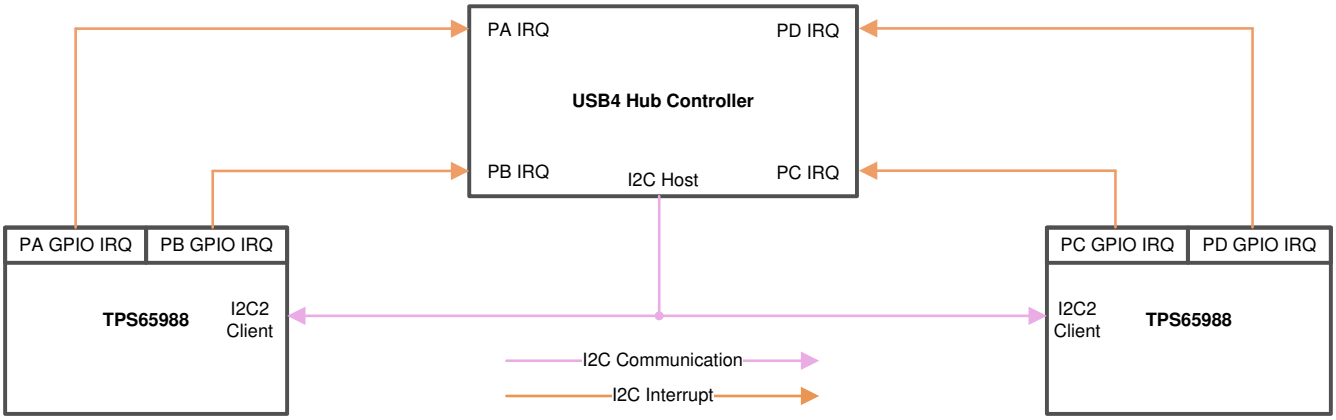


図 9-2. Dedicated Interrupts for USB4 Hub

図 9-3 shows the shared interrupt connection on I2C2_IRQ.

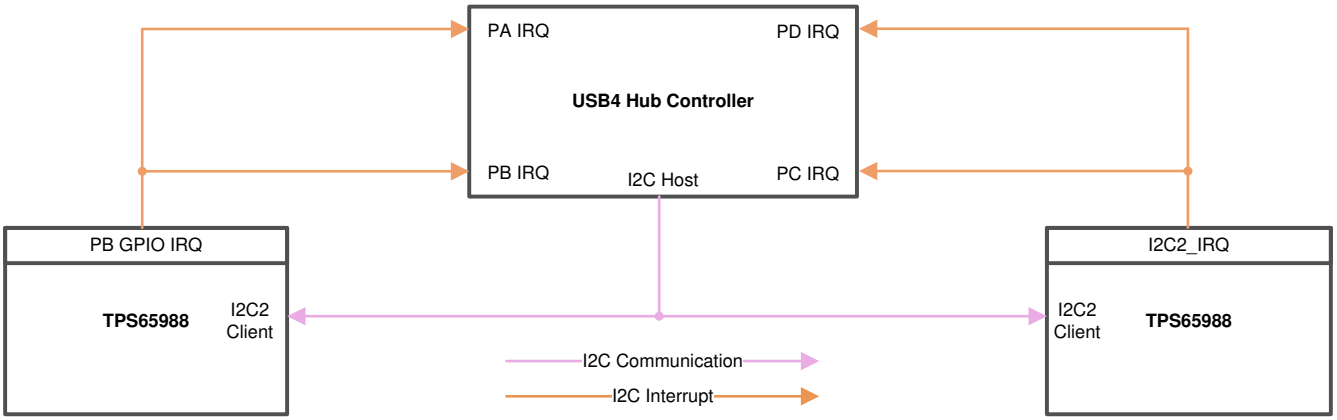


図 9-3. Shared Interrupts for USB4 Hub

表 9-5 shows an example of the port I2C addresses for each of the PD controller ports.

表 9-5. Recommended I2C Addresses - Hub Controller

Port	I2C Address
Port A	0x38
Port B	0x3F
Port C	0x48
Port D	0x4F

9.2.1.2.5 Dock Management Controller & PD Controller I2C Communication

The I2C connection from the PD controllers and the Dock Management Controller communicates to boot up the PD controllers and enable the Connection & Power Manager functions. The DMC has two GPIO dedicated for Port A/B and Port C/D interrupts. The shared interrupt connection to the Dock Management Controller will query both port addresses and will determine which port has been updated.

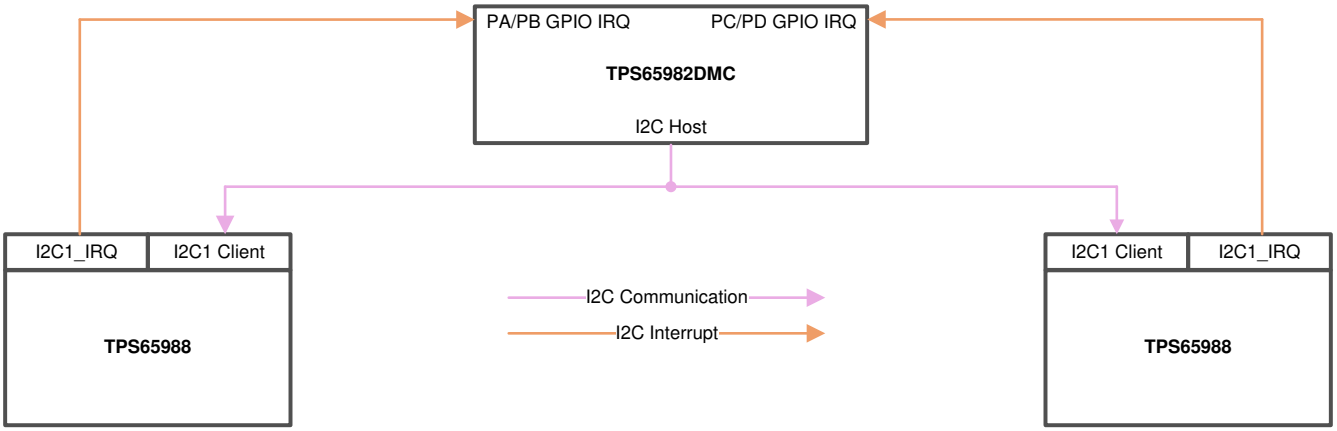


図 9-4. Interupt Configuration for DMC

表 9-6 shows and example of the port I2C address for each of the PD controller ports.

表 9-6. Recommended I2C Addresses - DMC

Port	I2C Address
Port A	0x20
Port B	0x24

表 9-6. Recommended I2C Addresses - DMC (continued)

Port	I2C Address
Port C	0x21
Port D	0x25

9.2.1.2.6 SPI Flash Options

The TPS65982DMC is connected to the SPI Flash which contains the firmware for the DMC and the PD controllers connected. 表 9-7 shows the supported SPI flash options.

表 9-7. SPI Flash Options

Manufacturer	Part Number	Size
Winbond	W25Q80JVNIQ	8 Mb
Spansion	S25FL208K	8 Mb
AMIC	A25L080	8 Mb
Macronix	MX25L8006EM1I	8 Mb
Micron	M25PE80-VMN6TP	8 Mb
Micron	M25PX80-VMN6TP	8 Mb

10 Power Supply Recommendations

10.1 3.3 V Power

10.1.1 1VIN_3V3 Input Switch

The VIN_3V3 input is the main supply to the TPS65982DMC. The VIN_3V3 switch (S1 in 図 8-7) is a unidirectional switch from VIN_3V3 to LDO_3V3, not allowing current to flow backwards from LDO_3V3 to VIN_3V3. This switch is on when 3.3 V is available. See 表 10-1 for the recommended external capacitance on the VIN_3V3 pin.

10.1.2 VOUT_3V3 Output Switch

The VOUT_3V3 output switch (S2 in 図 8-7) enables a low-current auxiliary supply to an external element. This switch is controlled by and is off by default. The VOUT_3V3 output has a supervisory circuit that drives the RESETZ output as a POR signal to external elements. RESETZ is also asserted by the MRESET pin or a host controller. See the *RESETZ and MRESET* section for more details on RESETZ. See 表 10-1 for the recommended external capacitance on the VOUT_3V3 pin.

10.1.3 ADP_IN 3.3 V LDO

The 3.3 V LDO from ADP_IN steps down voltage from ADP_IN to LDO_3V3. This allows the TPS65982DMC to be powered from ADP_IN when VIN_3V3 is not available. This LDO steps down any recommended voltage on the ADP_IN pin. When ADP_IN is 20 V, the internal circuitry of the TPS65982DMC will operate without triggering thermal shutdown; however, a significant external load on the LDO_3V3 pin can increase temperature enough to trigger thermal shutdown. The ADP_IN 3.3 V LDO blocks reverse current from LDO_3V3 back to ADP_IN allowing ADP_IN to be unpowered when LDO_3V3 is driven from another source. See 表 10-1 for the recommended external capacitance on the ADP_IN and LDO_3V3 pins.

10.2 1.8 V Core Power

Internal circuitry is powered from 1.8 V. There are two LDOs that step the voltage down from LDO_3V3 to 1.8 V. One LDO powers the internal digital circuits. The other LDO powers internal low voltage analog circuits.

10.2.1 1.8 V Digital LDO

The 1.8 V Digital LDO provides power to all internal low voltage digital circuits. This includes the digital core, memory, and other digital circuits. See 表 10-1 for the recommended external capacitance on the LDO_1V8D pin.

10.2.2 1.8 V Analog LDO

The 1.8 V Analog LDO provides power to all internal low voltage analog circuits. See 表 10-1 for the recommended external capacitance on the LDO_1V8A pin.

10.3 VDDIO

The VDDIO pin provides a secondary input allowing some I/Os to be powered by a source other than LDO_3V3. The default state is power from LDO_3V3. The memory stored in the flash will configure the I/O's to use LDO_3V3 or VDDIO as a source and application code will automatically scale the input and output voltage thresholds of the I/O buffer accordingly. See *I/O Buffers* for more information on the I/O buffer circuitry. See 表 10-1 for the recommended external capacitance on the VDDIO pin.

10.3.1 Recommended Supply Load Capacitance

表 10-1 lists the recommended board capacitances for the various supplies. The typical capacitance is the nominally rated capacitance that must be placed on the board as close to the pin as possible. The maximum capacitance must not be exceeded on pins for which it is specified. The minimum capacitance is minimum capacitance allowing for tolerances and voltage de-rating ensuring proper operation.

表 10-1. Recommended Supply Load Capacitance

PARAMETER	DESCRIPTION	VOLTAGE RATING	CAPACITANCE		
			MIN (ABS MIN)	TYP (TYP PLACED)	MAX (ABS MAX)
CVIN_3V3	Capacitance on VIN_3V3	6.3 V	5 µF	10 µF	
CLDO_3V3	Capacitance on LDO_3V3	6.3 V	5 µF	10 µF	25 µF
CVOUT_3V3	Capacitance on VOUT_3V3	6.3 V	0.1 µF	1 µF	2.5 µF
CLDO_1V8D	Capacitance on LDO_1V8D	4 V	500 nF	2.2 µF	12 µF
CLDO_1V8A	Capacitance on LDO_1V8A	4 V	500 nF	2.2 µF	12 µF
CLDO_BMC	Capacitance on LDO_BMC	4 V	1 µF	2.2 µF	4 µF
CVDDIO	Capacitance on VDDIO. When shorted to LDO_3V3, the CLDO_3V3 capacitance may be shared.	6.3 V	0.1 µF	1 µF	
CADP_IN	Capacitance on ADP_IN	25 V	0.5 µF	1 µF	12 µF
CPP_HVEXT	Capacitance on external high voltage sink from ADP_IN	25 V		47 µF	120 µF
CSS	Capacitance on soft start pin	6.3 V		470 nF	

11 Layout

11.1 Layout Guidelines

Proper placement and routing will maintain signal integrity for the high speed signals and power integrity for the external power path. The following guidelines show the recommended methodology to properly route all required signals. Board manufacturing capabilities must be taken into account with any layout to guarantee manufacturability.

11.2 Layout Example

The layout example is based on the schematic shown in 図 11-1. Some system components are not shown as they have their own layout recommendations.

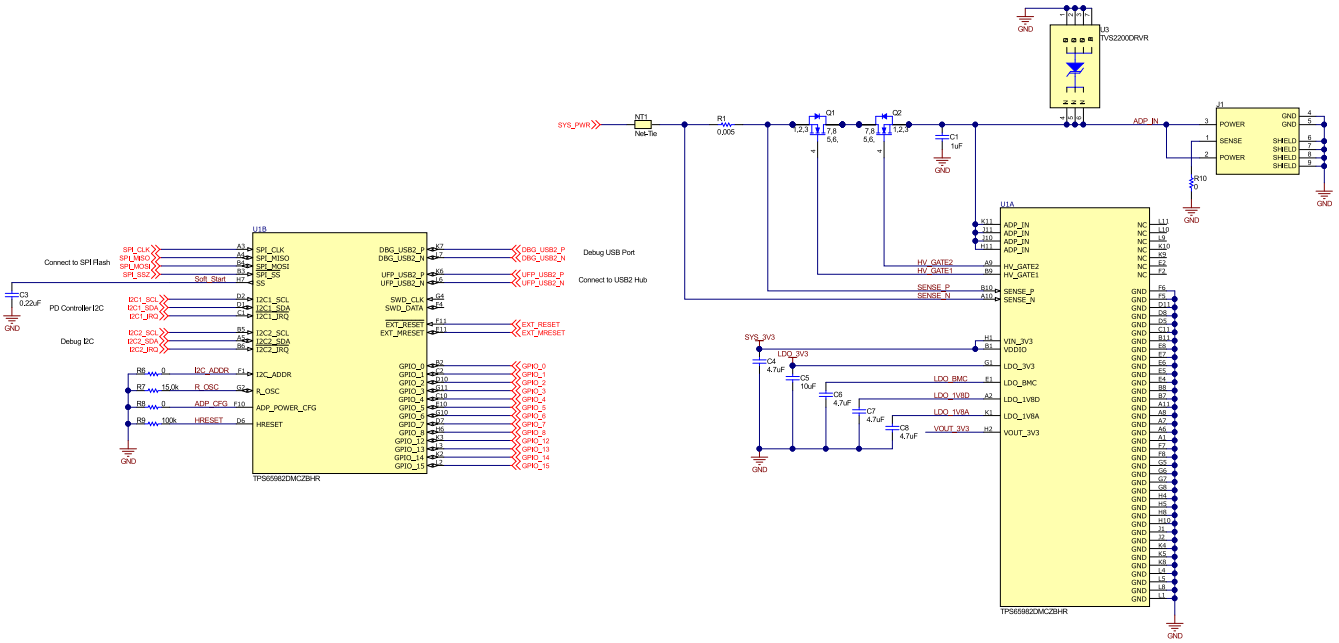


図 11-1. Example Schematic

11.2.1 Component Placement

The recommended placement is to have the TPS65982DMC on the Top Layer and have all of the passive components on the opposite layer of the PCB. This will significantly reduce solution size and allows for more clearance for the high speed and interface signals. 図 11-2 and 図 11-3 show the top and bottom placement.

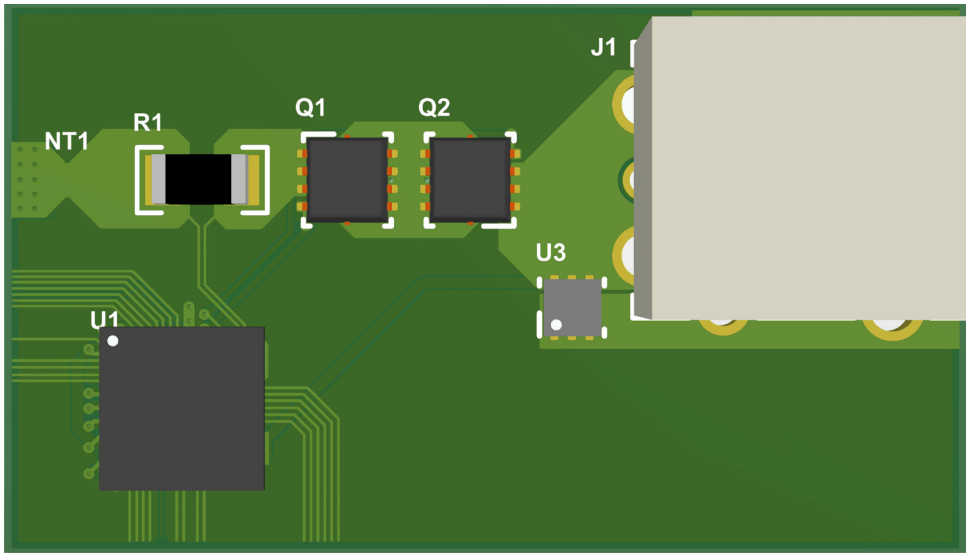


図 11-2. Top Layer Component Placement

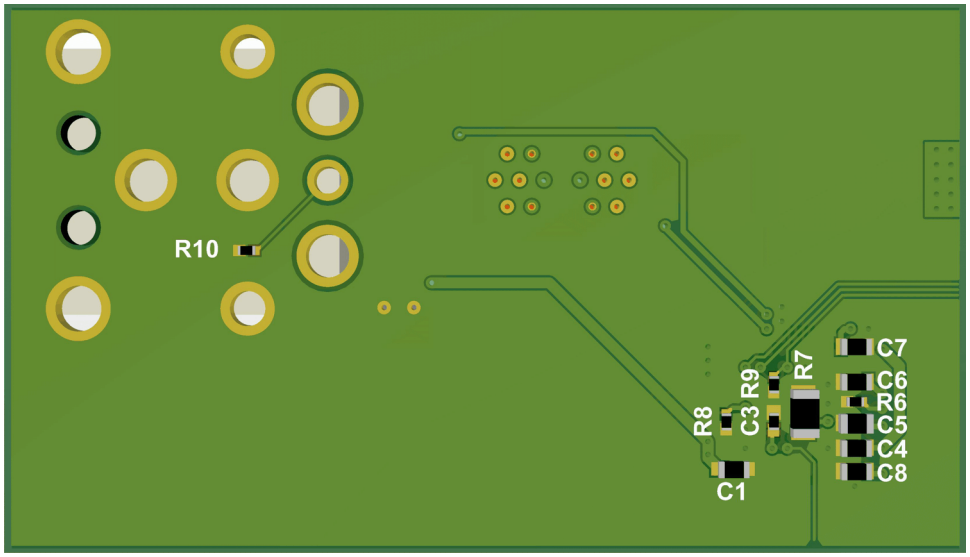


図 11-3. Bottom Layer Component Placement

11.2.2 Recommended Via Size and Trace Widths

For all LDO voltages, GPIO, Interface (I2C/SPI) and VIN_3V3 a single via connection to the pads on the TPS65982DMC is sufficient. For ADP_IN the current flowing into the device is less than 50mA but it is important to reduce the inductance in the trace. The ADP_IN capacitor is best placed close to the TPS65982DMC. The recommended via is a 16mil diameter / 8mil hole that is filled (epoxy fill or Cu fill) and tented on both sides of the PCB. The tenting will help reduce solder from wicking and lifting the BGA package. 図 11-4 shows the recommended via size.

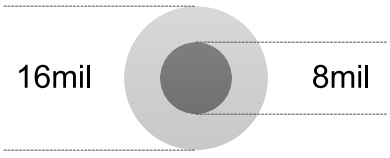


図 11-4. Recommended Via Sizing

表 11-1 shows the minimum trace widths. It is recommended to take into account any losses that may be present such as resistance from system supplies to input supply pins (VIN_3V3).

表 11-1. Trace Minimum Widths

Signal	Minimum Width (mil)
LDO_3V3, LDO_1V8A, LDO_1V8D, LDO_BMC, VIN_3V3, VOUT_3V3, VDDIO, HV_GATE1, HV_GATE2	6
GPIO, I2C, SPI	4
Component GND	6

11.2.3 Adapter Input Power Routing

The TPS65982DMC Adapter Input Power is the main power input to the system. When placing/routing the external power path it is important to consider the current handling. It is recommended placing a TVS such as the TVS2200 close to the Adapter Input Power Jack, to absorb any inductive ringing from a hot plug. The TPS65982DMC external power path should be placed in the same area as the Adapter Input Power Jack. The HV_GATE1/2 pins are high voltage nets, so it is recommended to space them from sensitive signals. The HV_GATE1/2 nets can be route through vias if needed. The SENSE_P/N current sense measures the current flowing into the system and the routing should be as direct, minimal layer changes, and kept from switching nets/signals.

11.2.4 USB2 Routing

It is important to reduce the number of vias use when routing USB2 signals for UFP_USB2_P/N and DBG_USB2_P/N. Routing on the top and bottom layers only will reduce the amount of antenna created when using a through hole via to connect an outer layer to an inner layer. When fanning out the BGA it is recommended to use 4mil traces to get enough clearance to route the width and gap requirements for impedance matching. Follow the USB2 specification and USB Hub requirements for complete routing rules

11.2.5 Oval Pad for BGA Fan Out

The footprint shown in 図 11-5 uses an oval footprint for the outer pads of the BGA. This allows for routing the inner pads through the outer pads. 図 11-6 shows the pad size for the out oval pads.

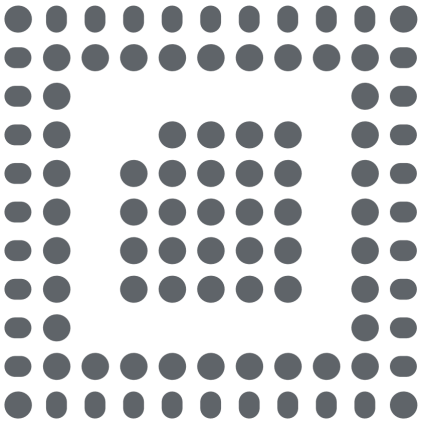


図 11-5. Example Footprint with Oval Pads

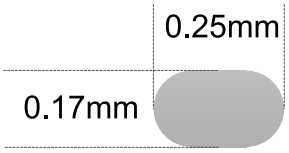


図 11-6. Oval Pad Sizing

11.2.6 Top and Bottom Layer Complete Routing

図 11-7 and 図 11-8 incorporate the guidelines to route all of the required TPS65982DMC signals on the top and bottom layer only. For GND and the external power path, they are connected all with planes/pours. Follow the amount of vias used and placement to ensure proper grounding and heat dissipation. All vias must be connected to a GND plane.

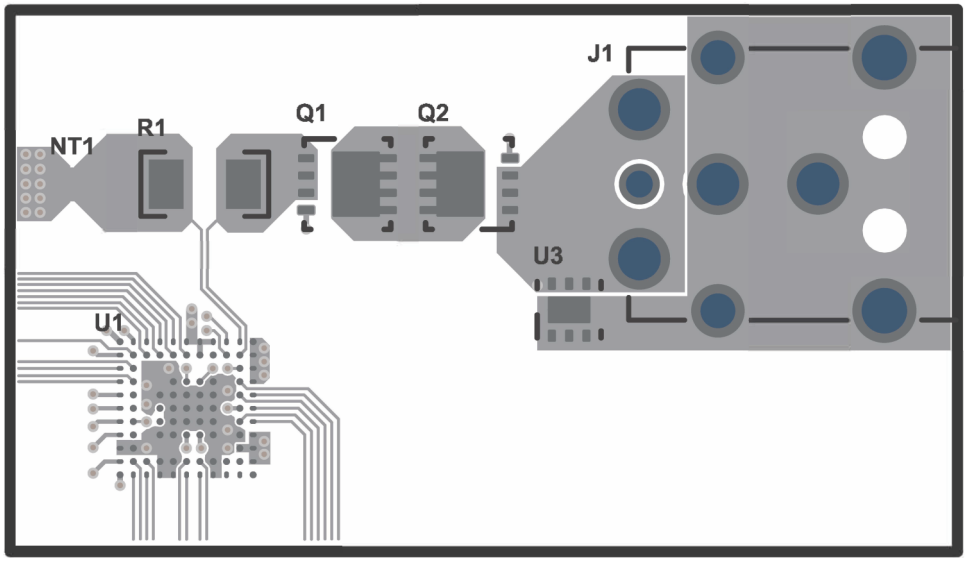


図 11-7. Top Layer Routing

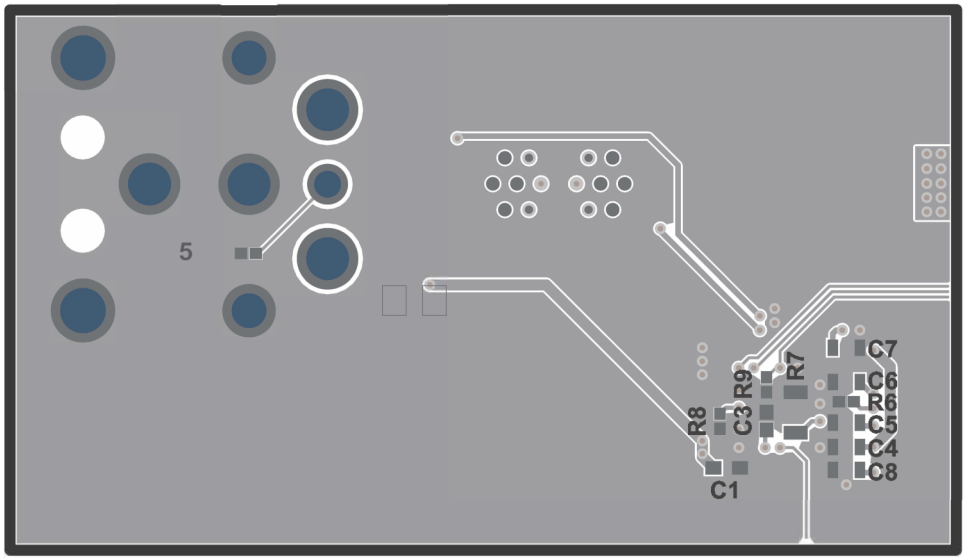


図 11-8. Bottom Layer Routing

12 Device and Documentation Support

12.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。*「更新の通知を受け取る」をクリック*して登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

12.5 用語集

TI 用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS65982DMCZBHR	Active	Production	NFBGA (ZBH) | 96	2500 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-10 to 85	T65982DMC
TPS65982DMCZBHR.A	Active	Production	NFBGA (ZBH) | 96	2500 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-10 to 85	T65982DMC

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

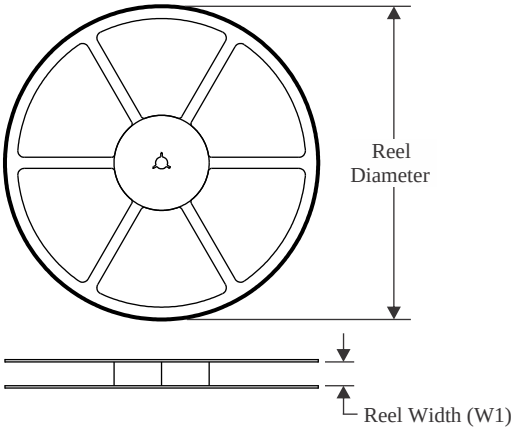
(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

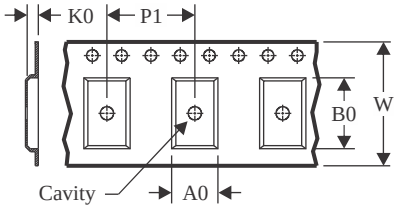
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

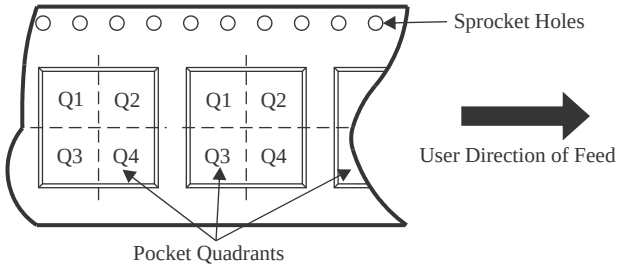


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

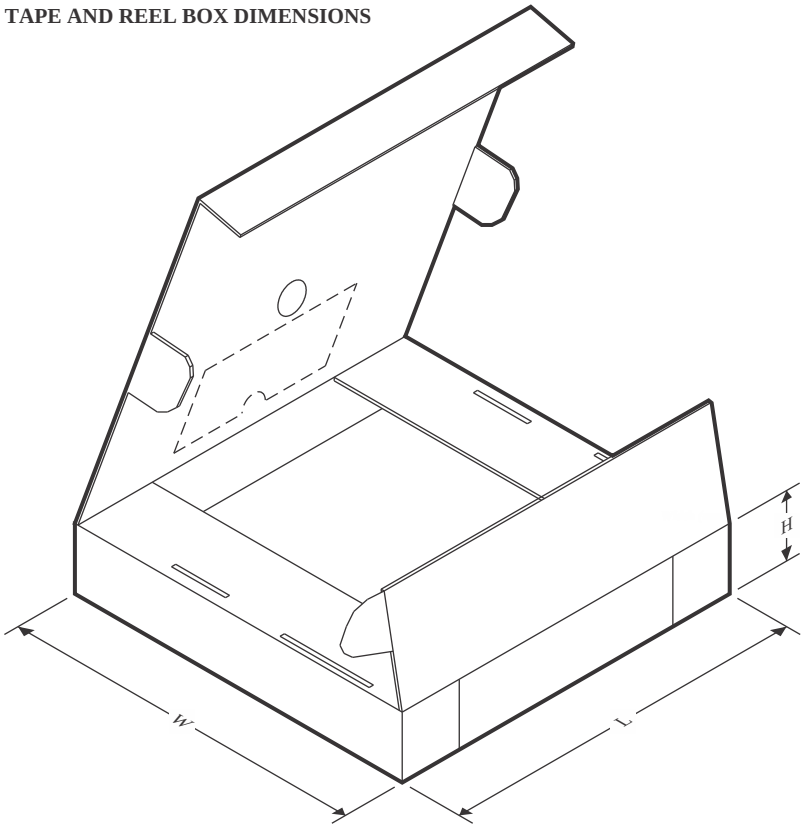
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65982DMCZBHR	NFBGA	ZBH	96	2500	330.0	16.4	6.3	6.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

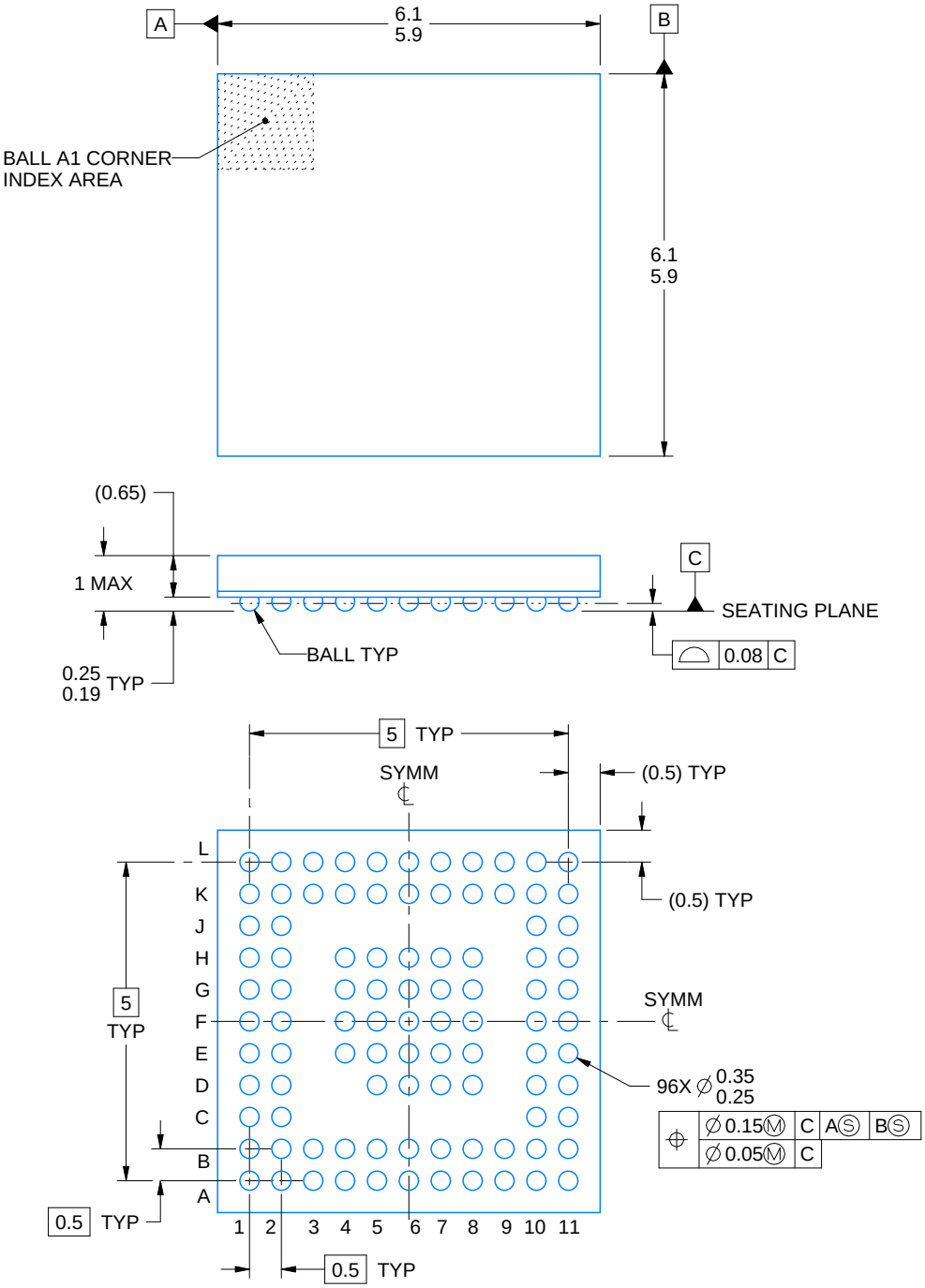
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65982DMCZBHR	NFBGA	ZBH	96	2500	336.6	336.6	31.8

PACKAGE OUTLINE

ZBH0096A

NFBGA - 1 mm max height

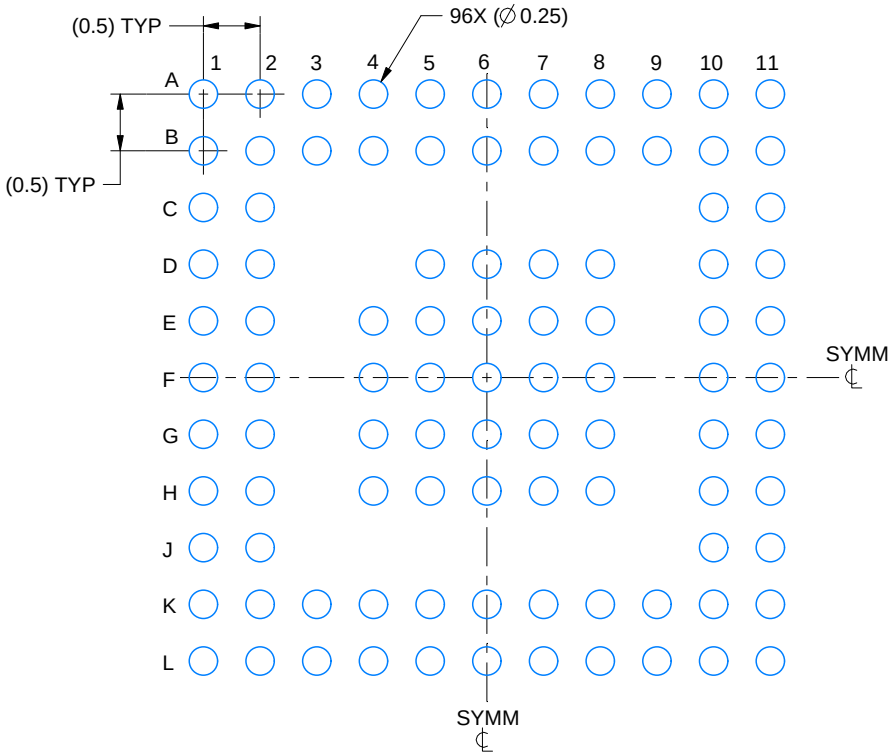
PLASTIC BALL GRID ARRAY



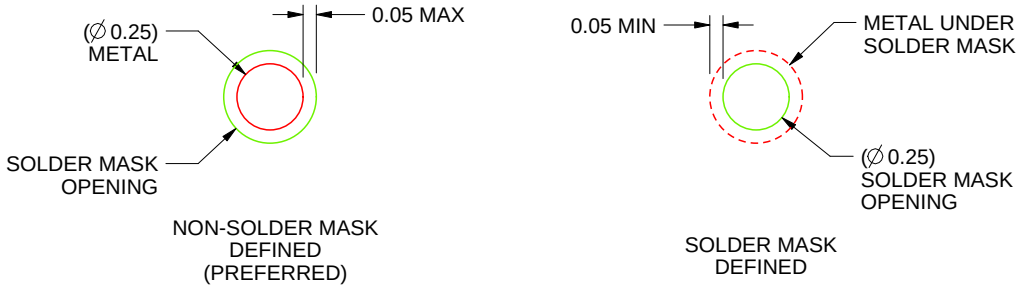
4221754/B 09/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS
NOT TO SCALE

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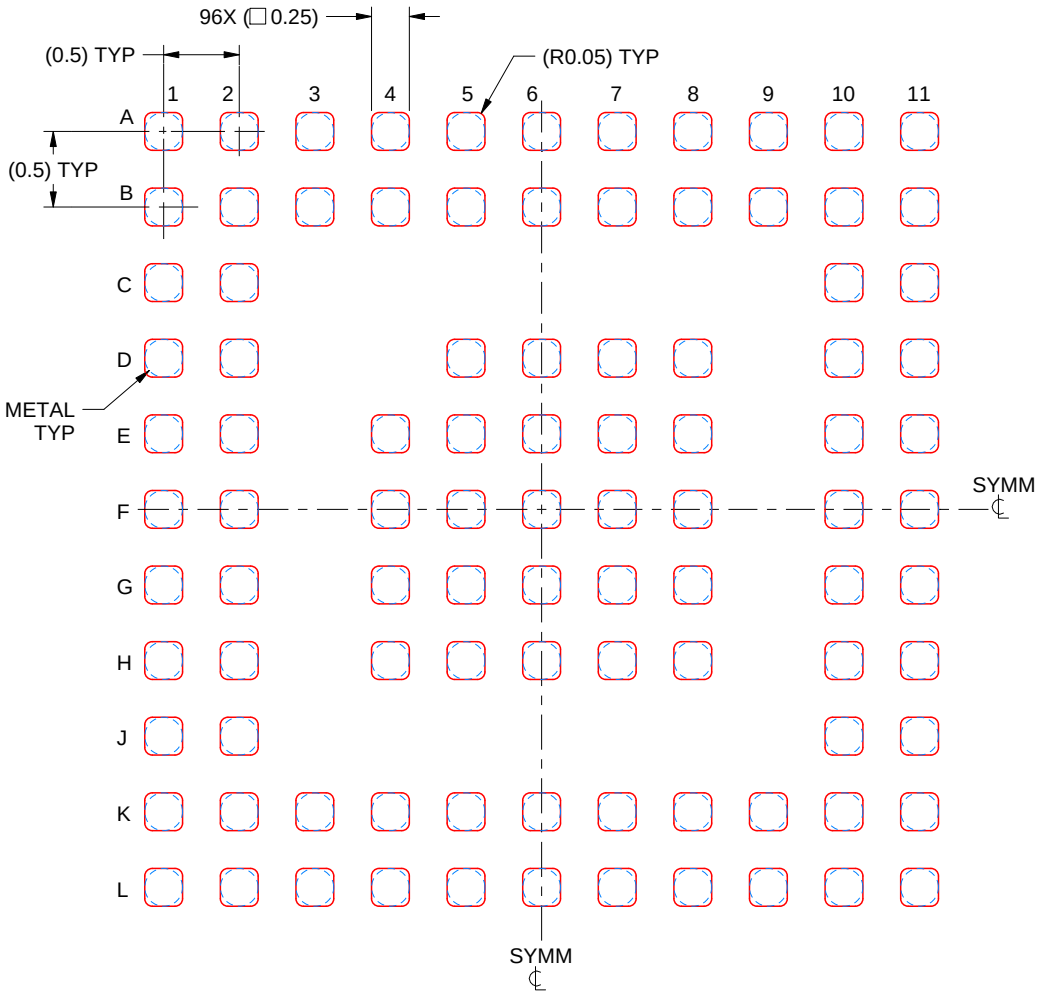
NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:20X

4221754/B 09/2018

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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最終更新日：2025 年 10 月