

# TPS6602x VBUS LDO レギュレータ搭載、統合型ソース / シンク・パワー・マルチプレクサ

## 1 特長

- 内蔵の  $30m\Omega$  (標準値)、32V 耐圧の NFET 5V ソース・バス、最大 3A
- 内蔵の  $22m\Omega$  (標準値)、32V 耐圧の NFET 4V~22V シンク・バス、最大 5A
- 5V ソース・バスの電流制限を選択可能
- 内蔵ソフトスタートによる突入電流の制限
- 高電圧 VBUS LDO レギュレータを内蔵 (デバイス・タイプに応じて 3.3V または 5.0V)
- ピンで設定可能な VBUS 過電圧保護
- システム電源および VBUS 低電圧保護
- 5V システム電源過電圧保護
- 過熱保護
- 逆電流保護
- フォルト・ピンによるグリッチ除去されたフォルト通知
- 高速ロール交換をサポート
- IEC/UL 認定番号US-34369-UL
  - 標準: IEC 62368-1 Ed. 2, UL 2367 Ed. 1
- 占有面積の小さい WCPW パッケージ、HDI 不要

## 2 アプリケーション

- デスクトップ PC / マザーボード
- 標準ノート PC
- Chromebook と WOA (Windows on Arm)
- ドッキング・ステーション
- ポート / ケーブル・アダプタとドングル

## 3 概要

TPS6602x は、5V ソース電力バスと 4V~22V シンク電力バスを内蔵したフル機能のパワー・スイッチ・マルチプレクサです。5V ソース・バスは、選択された電流制限のスレッショルドを出力負荷が上回ったときに定電流モードで動作することで出力電流を安全なレベルに制限します。各電力バスは、過熱および逆電流保護機能をサポートしています。VBUS は、オプションの外付け抵抗分圧器でレベルを設定できる過電圧保護機能を備えています。過電圧保護が不要の場合、OVP 端子を接地することで無効になります。TPS6602x シリーズは、過電流および過熱状態を示すフォルト・ピンをサポートしています。

また、TPS6602x シリーズは、デッド・バッテリ条件で動作する際にデバイスや他のシステム・コンポーネントに電力を供給するのに便利な高電圧 VBUS LDO レギュレータ (デバイスの種類により 3.3V または 5V) もサポートしています。TPS66020 は 3.3V、TPS66021 は 5V にレギュレートします。

### 製品情報<sup>(1)</sup>

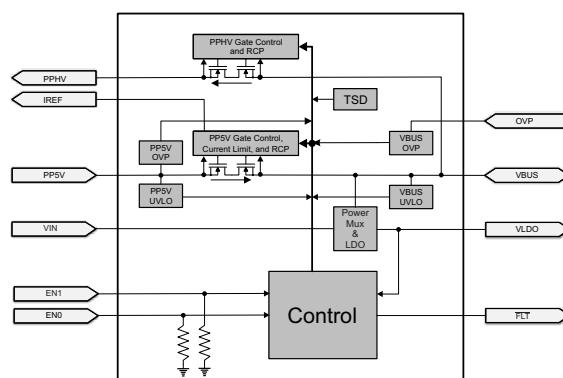
型番	パッケージ	本体サイズ(公称)
TPS66020	WCSP (28)	1.606mm × 2.806mm
TPS66021		

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

### 機能表

EN1	EN0	デバイスの状態
0	0	ソースおよびシンク・バスが無効
0	1	シンク・バスが有効
1	0	ソース・バスが有効、1.5A
1	1	ソース・バスが有効、3.0A

### TPS6602x ブロック図



英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、[www.ti.com](http://www.ti.com)で閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

English Data Sheet: [SLVSEW8](#)

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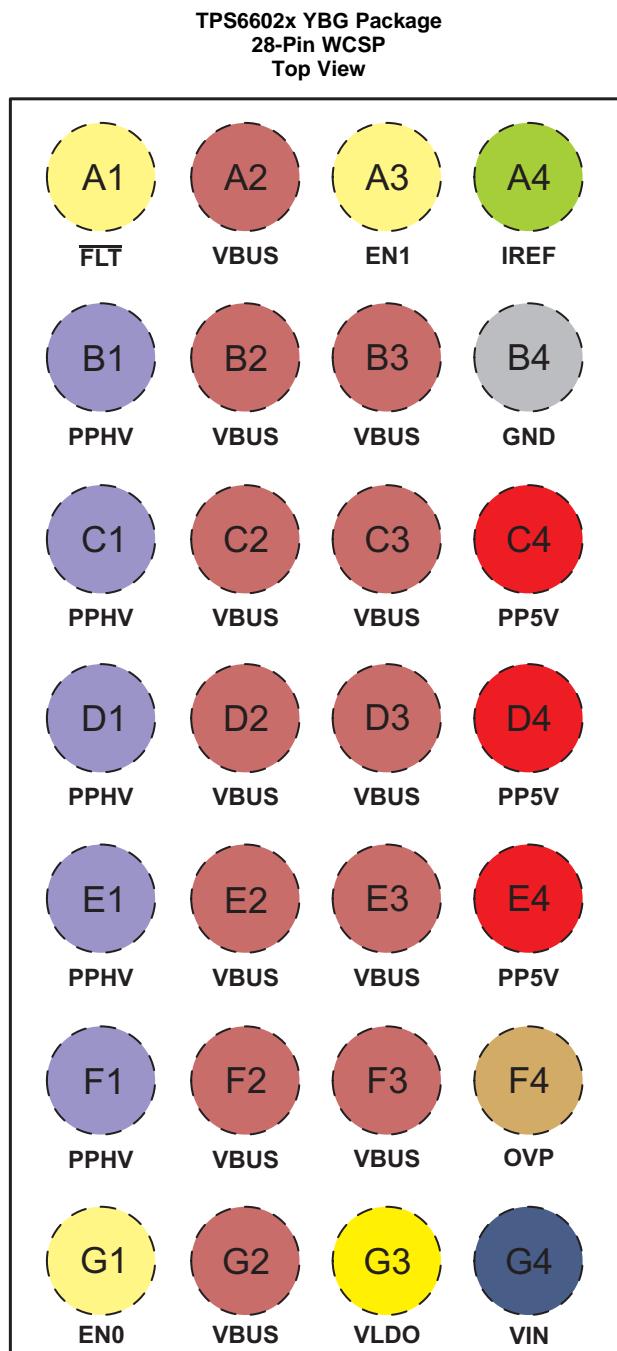
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## 4 改訂履歴

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## 5 Pin Configuration and Functions



### Pin Functions

Pin		I/O	Reset State	Description
Name	No.			
PP5V	C4, D4, E4	Power	Off	5-V System Supply to VBUS. Bypass with capacitance CPP5V to GND.
PPHV	B1, C1, D1, E1, F1	Power	Off	HV System Supply from VBUS. Bypass with capacitance CPPHV to GND.

**Pin Functions (continued)**

Pin		I/O	Reset State	Description
Name	No.			
VBUS	A2, B2, B3, C2, C3, D2, D3, E2, E3, F2, F3, G2	Power	-	5-V to 20-V nominal input supply to PPHV or 5-V output supply from PP5V. Bypass with capacitance CVBUS to GND.
VIN	G4	Power	-	Device input supply. Bypass with capacitance CVIN to GND.
VLDO	G3	Power	-	VIN supply or VBUS LDO regulated supply output from power multiplexer. Bypass with capacitance CVLDO to GND.
GND	B4	Ground	-	Ground. Connect all pins to ground plane.
OVP	F4	Analog	-	Selects VBUS OVP. Tie pin to VBUS resistor divider output to set desired VBUS OVP level. Tie pin to GND to remove VBUS OVP function.
EN1	A3	Digital Input	Pull-down	Enable control signal for PPHV Sink and PP5V Source paths. Internal pull-down.
EN0	G1	Digital Input	Pull-down	Enable control signal for PPHV Sink and PP5V Source paths. Internal pull-down.
IREF	A4	Analog		Used to set the PP5V source path current limit bias using an external resistor tied to GND.
FLT	A1	Digital Output	Hi-Z	Fault Output Indicator. Active low. This pin is a true open-drain (no PMOS). Float pin when unused.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

PARAMETER		MIN	MAX	UNIT
Terminal voltage range <sup>(2)</sup>	PP5V, EN0 <sup>(3)</sup> , EN1 <sup>(3)</sup> , $\overline{\text{FLT}}$ , VIN, VLDO	-0.3	6.2	V
Terminal voltage range <sup>(2)</sup>	OVP	-0.3	VBUS	V
Terminal voltage range <sup>(2)</sup>	VBUS, power path disabled (stand off voltage)	-0.5	32	V
Terminal voltage range <sup>(2)</sup>	VBUS, power path enabled <sup>(4)</sup>	-0.5	26	V
Terminal voltage range <sup>(2)</sup>	PPHV	-0.3	26	V
Terminal voltage range <sup>(2)</sup>	IREF	-0.3	4.5	V
Terminal positive source current	IREF	Internally limited		mA
Terminal positive source current	VLDO sourced from VBUS VLDO	Internally limited		mA
	VLDO sourced from VIN	50		mA
Storage temperature		-55	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network GND. All GND pins must be connected directly to the GND plane of the board.
- (3) EN0 and EN1 each have an internal voltage clamp and may be driven above the absolute maximum voltage rating up to EN\_CLAMP maximum specification if current is limited to less than 100 $\mu$ A.
- (4) For VBUS, a TVS protection with a break down voltage falling between the Recommended and Absolute maximum ratings is recommended, such as the TVS2200.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	$\pm 1000$	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	$\pm 500$	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>VIN</sub>	Input voltage range <sup>(1)</sup>	VIN, TPS66020 only.	2.85	3.6	V
		VIN, TPS66021 only.	4.5	5.5	V
V <sub>PP5V</sub>	Input voltage range <sup>(1)</sup>	PP5V	4.9	5.5	V
V <sub>PPHV</sub>	Output voltage range <sup>(1)</sup>	PPHV	0	22	V
V <sub>VBUS</sub>	Output voltage range <sup>(1)</sup>	VBUS when sourcing	0	5.5	V
V <sub>VBUS</sub>	Input voltage range <sup>(1)</sup>	VBUS when sinking	4	22	V
V <sub>EN</sub>	Input voltage range <sup>(1)</sup>	EN0, EN1	0	5.5	V
V <sub>FLT</sub>	Output voltage range <sup>(1)</sup>	FLT	0	5.5	V
I <sub>O_PP5V</sub>	Continuous current from PP5V to VBUS	T <sub>J</sub> = 105°C		3	A
I <sub>O_PPHV</sub>	Continuous current from VBUS to PPHV	T <sub>J</sub> = 105°C		4	A
		T <sub>J</sub> = 100°C		5	A
I <sub>O_VLDO</sub>	Output current from VBUS LDO			30	mA
R <sub>IREF</sub>	External resistor current limit reference	75kΩ ±1% overall tolerance	74.25	75.75	kΩ
T <sub>J</sub>	Operating junction temperature		-10	125	°C
RR_PP5V	Maximum ramp rate on PP5V input supply		-2	2	V/μs
RR_PPHV	Maximum ramp rate on PPHV input supply		-2	2	V/μs
RR_VBUS	Maximum ramp rate on VBUS input supply		-2	2	V/μs
RR_VIN	Maximum ramp rate on VIN input supply			30	mV/μs

(1) All voltage values are with respect to network GND. GND pin must be connected directly to the ground plane of the board.

## 6.4 Recommended Supply Load Capacitance

over operating free-air temperature range (unless otherwise noted)

PARAMETER <sup>(1)</sup>		MIN	TYP	MAX	UNIT
CVIN	Capacitance on VIN	1			μF
CVLDO	Capacitance on VLDO	2.5	4.7	10	μF
CVBUS	Capacitance on VBUS	1		10	μF
CPP5V	Capacitance on PP5V	2.5	4.7		μF
CPPHV	Capacitance present on PPHV <sup>(2)</sup>	1	47	100	μF

(1) Capacitance values do not include any derating factors. For example, if 5.0 μF is required and the external capacitor value reduces by 50% at the required operating voltage, then the required external capacitor value would be 10 μF.  
(2) This capacitance represents the system side load capacitance that may be seen by the device e.g. from a typical battery charging system. Discrete capacitance is not required for proper operation.

## 6.5 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS6602x	UNIT
		YBG (WCSP)	
		28 PINS	
R <sub>0JA,EFF</sub>	Effective Junction-to-ambient thermal resistance <sup>(2)</sup>	44.3	°C/W
R <sub>0JA</sub>	Junction-to-ambient thermal resistance	62.7	°C/W
R <sub>0JC(top)</sub>	Junction-to-case (top) thermal resistance	0.4	°C/W
R <sub>0JB</sub>	Junction-to-board thermal resistance	13.8	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.2	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	13.7	°C/W
Ψ <sub>JB,EFF</sub>	Effective Junction-to-board characterization parameter <sup>(2)</sup>	14.5	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.  
(2) Models based on typical application layout.

## 6.6 PP5V Power Switch Characteristics

Operating under these conditions unless otherwise noted:  $-10^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ ,  $2.85\text{V} \leq V_{\text{VIN}} \leq 5.5\text{V}$ ,  $R_{\text{REF}} = 75\text{ k}\Omega \pm 1\%$  overall tolerance,  $4.9\text{V} \leq V_{\text{PP5V}} \leq 5.5\text{V}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\text{PP5V}}$	Resistance from PP5V to VBUS	$I_{\text{LOAD}} = 1\text{ A}$ , $PP5V = 5.0\text{V}$ , $T_J = 25^{\circ}\text{C}$ , SRC 1P5A or SRC 3P0A state.		30	35	$\text{m}\Omega$
		$I_{\text{LOAD}} = 1\text{ A}$ , $PP5V = 5.0\text{V}$ , $-10^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ , SRC 1P5A or SRC 3P0A state.		30	50	$\text{m}\Omega$
$I_{\text{SC\_IREF}}$	Short circuit current from VBUS with IREF terminal shorted.	$V_{\text{IREF}} = 0\text{V}$ , SRC 1P5A or SRC 3P0A state.			8	A
$V_{\text{IREF}}$	Output voltage	SRC 1.5A state		0.56		V
		SRC 3.0A state		1.13		V
$I_{\text{LIM\_PP5V\_1P5}}$	Current limit for 1.5A setting	SRC 1.5A state	1.60	1.74	1.87	A
$I_{\text{LIM\_PP5V\_3P0}}$	Current limit for 3.0A setting	SRC 3.0A state	3.2	3.45	3.7	A
$I_{\text{LIMPP5VF}}$	Difference between current limit and current limit fault flag assertion, $I_{\text{LIM5VF}} \leq I_{\text{LIM5V}}$ .	SRC 1P5A or SRC 3P0A state. PP5V = 5V. Sweep load current and monitor $\overline{\text{FLT}}$ transition from 1 to 0 (50% point). $C_{\text{FLT}} = 20\text{pF}$ , $R_{\text{PU}} = 10\text{k}\Omega$ to VLDO.		12		$\text{mA}$
$t_{\text{ILIMIT\_FLT}}$	Time from PP5V current limit detected until $\overline{\text{FLT}}$ asserted low.	SRC 1P5A or SRC 3P0A state. PP5V = 5V. Sweep load current and monitor $\overline{\text{FLT}}$ transition from 1 to 0 (50% point). $C_{\text{FLT}} = 20\text{pF}$ , $R_{\text{PU}} = 10\text{k}\Omega$ to VLDO.	4	10	16	ms
$V_{\text{PP5V\_RCP}}$	Maximum voltage due to reverse current. Source path disables due to RCP comparator.	SRC 1P5A or SRC 3P0A state. $V_{\text{PP5V}} = 5.5\text{V}$ , ramp $V_{\text{VBUS}}$ from 5.5V to 21V at 75 V/ms, $C_{\text{PP5V}} = 47\mu\text{F}$ , measure $V_{\text{PP5V}}$			5.8	V
$V_{\text{PP5V\_RCP\_OVP}}$	Maximum voltage due to reverse current. Source path disables due to OVP protection on PP5V.	SRC 1P5A or SRC 3P0A state. $V_{\text{PP5V}} = 5.5\text{V}$ , ramp $V_{\text{VBUS}}$ from 5.5V to 21V at 5 V/ms, $C_{\text{PP5V}} = 4.7\mu\text{F}$ , measure $V_{\text{PP5V}}$			6.25	V
$V_{\text{RCP\_THRES\_PP5V}}$	Reverse current blocking voltage threshold for PP5V switch		25	35	45	$\text{mV}$
$t_{\text{OS\_PP5V}}$	Response time to VBUS short circuit	VBUS to GND through $10\text{m}\Omega$		2.0		$\mu\text{s}$
$t_{\text{ON\_PP5V}}$	PP5V enable time.	$R_L = 100\Omega$ , $V_{\text{PP5V}} = 5\text{V}$ , $C_L = 0$ , Transition from DISABLED state to SRC 1.5A state, $V_{\text{VBUS}}$ reaches 90% of final value.	2.6	4.5	5.3	ms
$t_{\text{OFF\_PP5V}}$	PP5V disable time.	$R_L = 100\Omega$ , $V_{\text{PP5V}} = 5\text{V}$ , $C_L = 0$ , Transition from SRC 1.5A or SRC 3.0A state to DISABLED state, $V_{\text{VBUS}}$ at 10% of final value.	0.5	0.7	1.2	ms
$t_{\text{RISE\_PP5V}}$	VBUS from 10% to 90% of final value	$R_L = 100\Omega$ , $V_{\text{PP5V}} = 5\text{V}$ , $C_L = 0$ , Transition from DISABLED state to SRC 1.5A state	0.5	0.9	1.5	ms
$t_{\text{FALL\_PP5V}}$	VBUS from 90% to 10% of initial value	$R_L = 100\Omega$ , $V_{\text{PP5V}} = 5\text{V}$ , $C_L = 0$ , Transition from SRC 1.5A or SRC 3.0A state to DISABLED state	0.1	0.16	0.25	ms

## 6.7 PPHV Power Switch Characteristics

Operating under these conditions unless otherwise noted:  $-10^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ ,  $2.85\text{V} \leq V_{\text{VIN}} \leq 5.5\text{V}$ ,  $R_{\text{REF}} = 75\text{ k}\Omega \pm 1\%$  overall tolerance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\text{PPHV}}$	Resistance from PPHV to VBUS	$I_{\text{LOAD}} = 1\text{ A}$ , $T_J = 25^{\circ}\text{C}$ , SNK state.		22	26	$\text{m}\Omega$
		$I_{\text{LOAD}} = 1\text{ A}$ , $-10^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ , SNK state.		22	45	$\text{m}\Omega$
$V_{\text{PPHV\_RCP}}$	Maximum voltage due to reverse current during RCP response.	SNK state, $V_{\text{VBUS}} = 5.5\text{V}$ , ramp $V_{\text{PPHV}}$ from $5.5\text{V}$ to $21\text{V}$ at $100\text{ V/ms}$ , $C_{\text{VBUS}} = 10\mu\text{F}$ , measure $V_{\text{VBUS}}$		5.8		V
$V_{\text{PPHV\_OVP}}$	Maximum voltage rise due to reverse current during VBUS OVP response.	SNK state, $V_{\text{VBUS}} = 5.5\text{V}$ , set $V_{\text{OVP}} = 6\text{V}$ , ramp $V_{\text{VBUS}}$ from $5.5\text{V}$ to $21\text{V}$ at $100\text{ V/ms}$ , $C_{\text{PPHV}} = 4.7\mu\text{F}$ , measure $V_{\text{PPHV}}$		6.2		V
$V_{\text{RCP\_THRES\_PPHV}}$	Reverse current blocking voltage threshold for PPHV switch		2	6	10	$\text{mV}$
SS	Soft-start slew rate	Transition from DISABLED state to SNK state, $V_{\text{VBUS}} = 5\text{V}$ , $C_{\text{PPHV}} = 100\mu\text{F}$ . Measure slew rate on PPHV.	0.2		0.6	$\text{V/ms}$
$t_{\text{ON\_PPHV}}$	PPHV enable time including Soft-start.	$R_{\text{PPHV}} = 100\Omega$ , $V_{\text{VBUS}} = 5\text{V}$ , $C_{\text{PPHV}} = 100\mu\text{F}$ . Transition from DISABLED state to SNK state, $V_{\text{PPHV}}$ at 90% of final value.	9	15	29	ms
$t_{\text{OFF\_PPHV}}$	PPHV disable time.	$R_{\text{PPHV}} = 100\Omega$ , $V_{\text{VBUS}} = 5\text{V}$ , $C_{\text{PPHV}} = 4.7\mu\text{F}$ . Transition from SNK state to DISABLED state, $V_{\text{PPHV}}$ falls to $4.5\text{V}$ .	0.9	2.2	4.3	ms

## 6.8 Power Path Supervisory

Operating under these conditions unless otherwise noted:  $-10^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ ,  $2.85\text{V} \leq V_{\text{VIN}} \leq 5.5\text{V}$ ,  $R_{\text{REF}} = 75\text{ k}\Omega \pm 1\%$  overall tolerance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
UV_VIN_R	Undervoltage threshold for VIN. VBUS LDO disables when threshold reached.	VIN rising, TPS66020 only.	2.45		2.75	V
		VIN rising, TPS66021 only.	3.89		4.40	V
UV_VIN_F	Undervoltage threshold for VIN. Device resets.	VIN falling, TPS66020 only.	2.35		2.65	V
		VIN falling, TPS66021 only.	3.79		4.30	V
UVH_VIN	Undervoltage hysteresis for VIN.			100		$\text{mV}$
UV_VBUS_R	Undervoltage threshold for VBUS. PPHV switch disabled until threshold reached.	VBUS rising	3.35		3.75	V
UV_VBUS_F	Undervoltage threshold for VBUS. PPHV switch disables when threshold reached.	VBUS falling	3.15		3.55	V
UVH_VBUS	Undervoltage hysteresis for VBUS			200		$\text{mV}$
OVP_REF	OVP reference voltage.		0.93	1	1.07	V
UV_PP5V_R	Undervoltage threshold for PP5V. PP5V switch disabled until threshold reached.	PP5V rising	3.9		4.5	V
UVH_PP5V	Undervoltage hysteresis for PP5V			100		$\text{mV}$
UV_PP5V_F	Undervoltage threshold for PP5V. PP5V switch disables when threshold reached.	PP5V falling	3.8		4.4	V
OV_PP5V_R	Ovvoltage threshold for PP5V. PP5V switch disabled if threshold reached.	PP5V rising	5.60	5.9	6.2	V
OV_PP5V_F	Ovvoltage threshold for PP5V. PP5V switch enabled if threshold reached.	PP5V falling	5.50	5.8	6.1	V
OVH_PP5V	Ovvoltage hysteresis for PP5V			100		$\text{mV}$
VFWD_DROP_VIN	Forward voltage drop across VIN to VLDO switch	$I_{\text{VLDO}} = 35\text{ mA}$			90	$\text{mV}$

## Power Path Supervisory (continued)

Operating under these conditions unless otherwise noted:  $-10^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ ,  $2.85\text{V} \leq V_{\text{VIN}} \leq 5.5\text{V}$ ,  $R_{\text{REF}} = 75\text{ k}\Omega \pm 1\%$  overall tolerance

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{\text{VIN\_STABLE}}$	When $V_{\text{IN}}$ is above $UV_{\text{VIN\_R}}$ for this duration, $V_{\text{IN}}$ is considered valid. If device is being powered by VBUS LDO, it will then switch to $V_{\text{IN}}$ supply and VBUS LDO will be disabled.		5	15	ms

## 6.9 VBUS LDO Characteristics

Operating under these conditions unless otherwise noted:  $-10^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ ,  $2.85\text{V} \leq V_{\text{VIN}} \leq 5.5\text{V}$ ,  $R_{\text{REF}} = 75\text{ k}\Omega \pm 1\%$  overall tolerance

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$V_{\text{VBUS\_LDO\_3V}}$	Output voltage of VBUS LDO	For TPS66020: $V_{\text{IN}} = 0\text{V}$ , $V_{\text{BUS}} \geq 3.8\text{V}$ , $0 \leq I_{\text{VBUS\_LDO}} \leq 30\text{mA}$	3.07	3.3	3.53	V
$V_{\text{VBUS\_LDO\_5V}}$	Output voltage of VBUS LDO	For TPS66021: $V_{\text{IN}} = 0\text{V}$ , $V_{\text{BUS}} \geq 5.5\text{V}$ , $0 \leq I_{\text{VBUS\_LDO}} \leq 30\text{mA}$	4.65	5.0	5.35	V
$V_{\text{D}\text{O\_VBUS\_LDO\_3V}}$	Drop out voltage of VDD LDO	For TPS66020: $V_{\text{IN}} = 0\text{V}$ , $V_{\text{BUS}} = 3.135\text{V}$ , $I_{\text{VBUS\_LDO}} = 30\text{ mA}$		0.5	V	
$V_{\text{D}\text{O\_VBUS\_LDO\_5V}}$	Drop out voltage of VDD LDO	For TPS66021: $V_{\text{IN}} = 0\text{V}$ , $V_{\text{BUS}} = 4.75\text{V}$ , $I_{\text{VBUS\_LDO}} = 30\text{ mA}$		0.5	V	
$I_{\text{LIMIT\_VBUS\_LDO}}$	Current limit VBUS LDO.	$V_{\text{BUS}} = 5.5\text{V}$ , $V_{\text{IN}} = 0\text{V}$ , $V_{\text{LDO}} = 0\text{V}$	50	100	mA	
$t_{\text{EN\_VBUS\_LDO}}$	Turn-on time of VBUS LDO.	For TPS66020: $I_{\text{VBUS\_LDO}} = 30\text{mA}$ , $C_{\text{VLDO}} = 4.7\text{ }\mu\text{F}$ , $V_{\text{IN}} = 0\text{V}$ . Ramp $V_{\text{VBUS}}$ from 0 to 5V at $\geq 50\text{V/ms}$ . Measure from $V_{\text{BUS}} = 4.5\text{V}$ to $V_{\text{LDO}} = 3\text{V}$ .		1.2	ms	
		For TPS66021: $I_{\text{VBUS\_LDO}} = 30\text{mA}$ , $C_{\text{VLDO}} = 4.7\text{ }\mu\text{F}$ , $V_{\text{IN}} = 0\text{V}$ . Ramp $V_{\text{VBUS}}$ from 0 to 7.5V at $\geq 50\text{V/ms}$ . Measure from $V_{\text{BUS}} = 7\text{V}$ to $V_{\text{LDO}} = 4.5\text{V}$ .		1.2	ms	

## 6.10 Thermal Shutdown Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$T_{\text{SD\_PP5V\_R}}$	Thermal Shutdown Temperature of the PP5V power path.	Temperature rising	128	150	172	°C
$T_{\text{SD\_PP5V\_F}}$	Thermal Shutdown Temperature of the PP5V power path.	Temperature falling	115	140	165	°C
$T_{\text{SDH\_PP5V}}$	Thermal Shutdown hysteresis of the PP5V power path.			10	°C	
$T_{\text{SD\_PPHV\_R}}$	Thermal Shutdown Temperature of the PPHV power path.	Temperature rising	128	150	172	°C
$T_{\text{SD\_PPHV\_F}}$	Thermal Shutdown Temperature of the PPHV power path.	Temperature falling	115	140	165	°C
$T_{\text{SDH\_PPHV}}$	Thermal Shutdown hysteresis of the PPHV power path.			10	°C	
$T_{\text{SD\_MAIN\_R}}$	Thermal Shutdown Temperature of the entire device.	Temperature rising	140	160	178	°C
$T_{\text{SD\_MAIN\_F}}$	Thermal Shutdown Temperature of the entire device.	Temperature falling	120	140	160	°C
$T_{\text{SDH\_MAIN}}$	Thermal Shutdown hysteresis of the entire device.			20	°C	

## 6.11 Input-output (I/O) Characteristics

Operating under these conditions unless otherwise noted:  $-10^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ ,  $2.85\text{ V} \leq V_{\text{VIN}} \leq 5.5\text{V}$ ,  $R_{\text{REF}} = 75\text{ k}\Omega \pm 1\%$  overall tolerance

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
EN_Vt+	Positive going input-threshold voltage, % of VLDO	VLDO = 2.85 - 5.5V	40	70	%	
EN_Vt-	Negative going input-threshold voltage, % of VLDO	VLDO = 2.85 - 5.5V	30	60	%	
EN_HYS	Input hysteresis voltage, % of VLDO	VLDO = 2.85 - 5.5V	10		%	
EN_RPD	Pull-down resistance EN pin.	Measured with pin voltage $V_{\text{EN}} = 3.3\text{V}$	500	650	800	$\text{k}\Omega$
EN_CLAMP	Voltage clamp on EN pin.	$I_{\text{EN}} = 100\text{ }\mu\text{A}$	6	7.1	V	
FLT_VOL	Output Low Voltage, $\overline{\text{FLT}}$ pin	$I_{\text{OL}} = 2\text{mA}$ , $\overline{\text{FLT}}$ driven low.		0.4	V	
FLT_ILKG	Leakage Current, $\overline{\text{FLT}}$ pin	$\overline{\text{FLT}}$ not driven low.	-1	1	$\mu\text{A}$	
$t_{\text{H\_FLT}}$	Time $\overline{\text{FLT}}$ pin remains asserted low.		4	10	16	ms
$t_{\text{DG\_EN}}$	Enable deglitch filter. Pulses on EN0 or EN1 $< t_{\text{DG\_EN(MIN)}}$ are not propagated to the control logic. Pulses on EN0 or EN1 $> t_{\text{DG\_EN(MAX)}}$ are propagated to the control logic. Pulses on EN0 or EN1 $\geq t_{\text{DG\_EN(MIN)}}$ and $\leq t_{\text{DG\_EN(MAX)}}$ may or may not propagate to the control logic. The filter is not applied to EN1 transition to the FRS state.		78	242	$\mu\text{s}$	

## 6.12 Power Consumption Characteristics

Operating under these conditions unless otherwise noted:  $-10^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$ ,  $2.85\text{V} \leq V_{\text{VIN}} \leq 5.5\text{V}$ ,  $R_{\text{REF}} = 75\text{ k}\Omega \pm 1\%$  overall tolerance

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$I_{\text{VIN\_DISABLE}}$	VIN = 3.3V, VBUS = 0V, PP5V = 0V, PPHV = 0V, DISABLED state. Measure $I_{\text{VIN}}$ . TPS66020 only.			19	27	$\mu\text{A}$
	VIN = 5V, VBUS = 0V, PP5V = 0V, PPHV = 0V, DISABLED state. Measure $I_{\text{VIN}}$ . TPS66021 only.			25	36	$\mu\text{A}$
$I_{\text{VIN\_SRC}}$	VIN = 3.3V, PP5V = 5.5V, PPHV = 0V, SRC 1.5A or SRC 3.0A state. Measure $I_{\text{VIN}}$ . TPS66020 only.			136		$\mu\text{A}$
	VIN = 5V, PP5V = 5.5V, PPHV = 0V, SRC 1.5A or SRC 3.0A state. Measure $I_{\text{VIN}}$ . TPS66021 only.			214		$\mu\text{A}$
$I_{\text{VIN\_SNK}}$	VIN = 3.3V, PP5V = 0V, SNK state. Measure $I_{\text{VIN}}$ . TPS66020 only.	VBUS = 5.5V/22V		130		$\mu\text{A}$
	VIN = 5V, PP5V = 0V, SNK state. Measure $I_{\text{VIN}}$ . TPS66021 only.	VBUS = 5.5V/22V		215		$\mu\text{A}$

(1) Measured with EN0 and/or EN1 set to GND or VLDO levels as required for the respective state.

## Power Consumption Characteristics (continued)

Operating under these conditions unless otherwise noted:  $-10^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$ ,  $2.85\text{V} \leq V_{\text{VIN}} \leq 5.5\text{V}$ ,  $R_{\text{REF}} = 75\text{ k}\Omega \pm 1\%$  overall tolerance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{\text{SD\_PP5V}}$	Current consumed by PP5V <sup>(1)</sup>	VIN = 3.3V, PP5V = 5.5V, PPHV = 0V, VBUS = 0V, DISABLED state. Measure $I_{\text{PP5V}}$ . TPS66020 only.		2		$\mu\text{A}$
		VIN = 5V, PP5V = 5.5V, PPHV = 0V, VBUS = 0V, DISABLED state. Measure $I_{\text{PP5V}}$ . TPS66021 only.		2		$\mu\text{A}$
$I_{\text{ACT\_PP5V}}$	Current consumed by PP5V <sup>(1)</sup>	VIN = 3.3V, PP5V = 5.5V, PPHV = 0V, SRC 1.5A or SRC 3.0A state. Measure $I_{\text{PP5V}}$ . TPS66020 only.		109		$\mu\text{A}$
		VIN = 5V, PP5V = 5.5V, PPHV = 0V, SRC 1.5A or SRC 3.0A state. Measure $I_{\text{PP5V}}$ . TPS66021 only.		109		$\mu\text{A}$
$I_{\text{SD\_VBUS}}$	Current consumed by VBUS <sup>(1)</sup>	VIN = 3.3V, PP5V = 0V, PPHV = 0V, DISABLED state. Measure $I_{\text{VBUS}}$ . TPS66020 only.	VBUS = 5.5V	12	26	$\mu\text{A}$
			VBUS = 22V	34		$\mu\text{A}$
		VIN = 5V, PP5V = 0V, PPHV = 0V, DISABLED state. Measure $I_{\text{VBUS}}$ . TPS66021 only.	VBUS = 5.5V	8		$\mu\text{A}$
			VBUS = 22V	30		$\mu\text{A}$
$I_{\text{SD\_VBUS\_LDO}}$	Current consumed by VBUS <sup>(1)</sup>	VIN = 0V, PP5V = 0V, PPHV = 0V, DISABLED state. Measure $I_{\text{VBUS}}$ .	VBUS = 5.5V	45		$\mu\text{A}$
			VBUS = 22V	69		$\mu\text{A}$
$I_{\text{ACT\_VBUS}}$	Current consumed by VBUS <sup>(1)</sup>	VIN = 3.3V, PP5V = 0V, SNK state. Measure $I_{\text{VBUS}}$ . TPS66020 only.	VBUS = 5.5V	325		$\mu\text{A}$
			VBUS = 22V	360		$\mu\text{A}$
		VIN = 5V, PP5V = 0V, SNK state. Measure $I_{\text{VBUS}}$ . TPS66021 only.	VBUS = 5.5V	342		$\mu\text{A}$
			VBUS = 22V	377		$\mu\text{A}$
$V_{\text{OC\_VBUS}}$	Open circuit voltage, VBUS	PP5V = 5.5V, PPHV = 22V, DISABLED state, no DC loading on VBUS. Measure $V_{\text{VBUS}}$ under steady state conditions.			0.8	V
$V_{\text{OC\_PP5V}}$	Open circuit voltage, PP5V	VBUS = 22V, PPHV = 0V, DISABLED state, no DC loading on PP5V. Measure $V_{\text{PP5V}}$ under steady state conditions.			0.8	V
$V_{\text{OC\_PPHV}}$	Open circuit voltage, PPHV	VBUS = 22V, PP5V = 0V, DISABLED state, no DC loading on PPHV. Measure $V_{\text{PPHV}}$ under steady state conditions.			0.8	V

## 6.13 Typical Characteristics

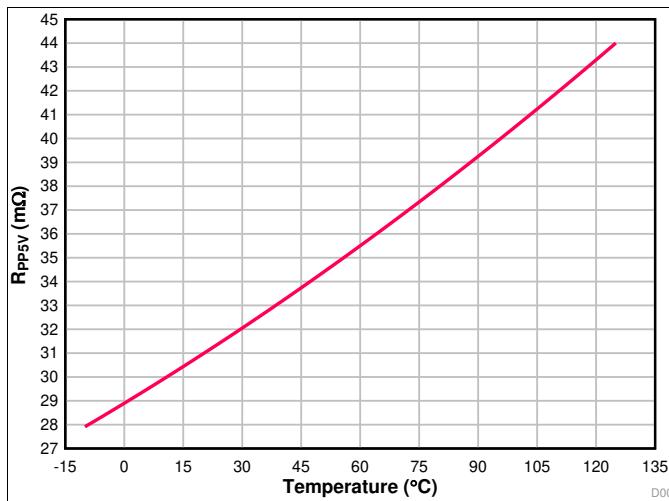


図 1.  $R_{PP5V}$  versus Temperature

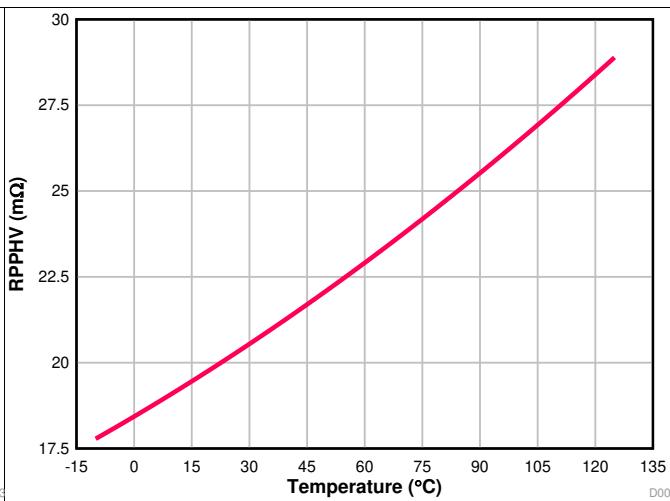


図 2.  $R_{PPHV}$  versus Temperature

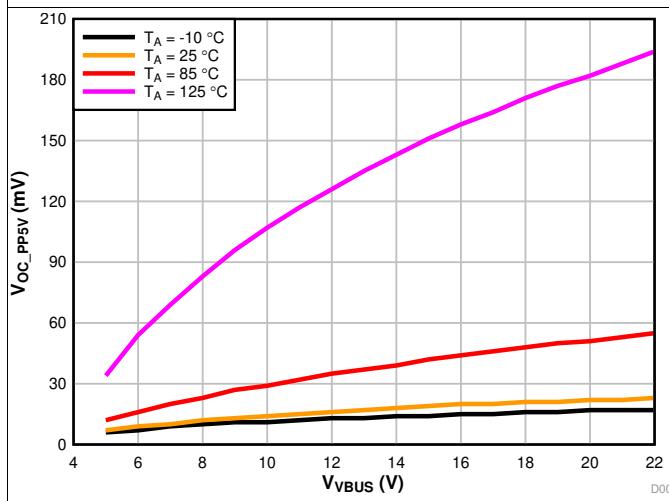


図 3.  $V_{OC\_PP5V}$ , PP5V Open Circuit Voltage versus VBUS

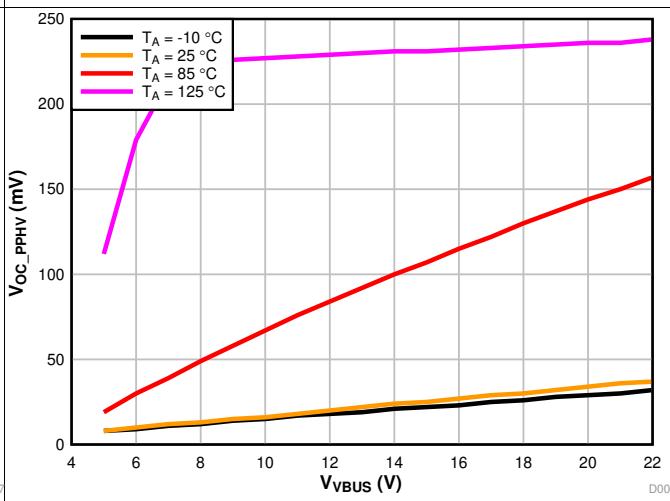


図 4.  $V_{OC\_PPHV}$ , PPHV Open Circuit Voltage versus VBUS

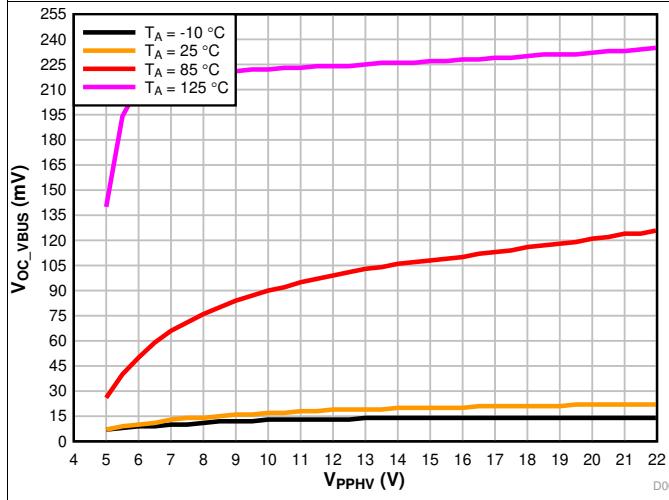


図 5.  $V_{OC\_VBUS}$ , VBUS Open Circuit Voltage versus PPHV

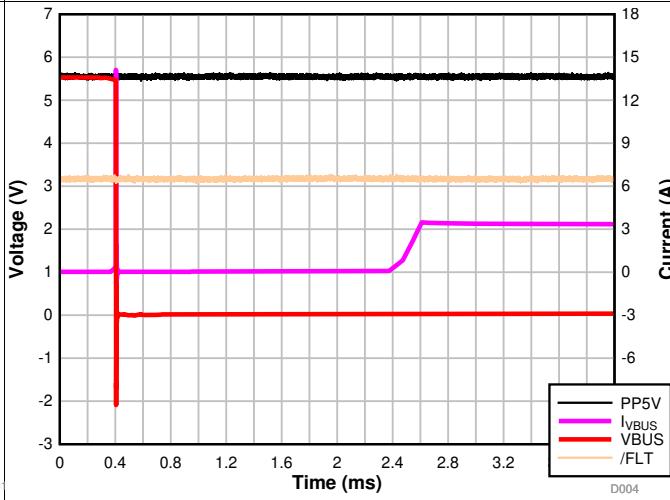
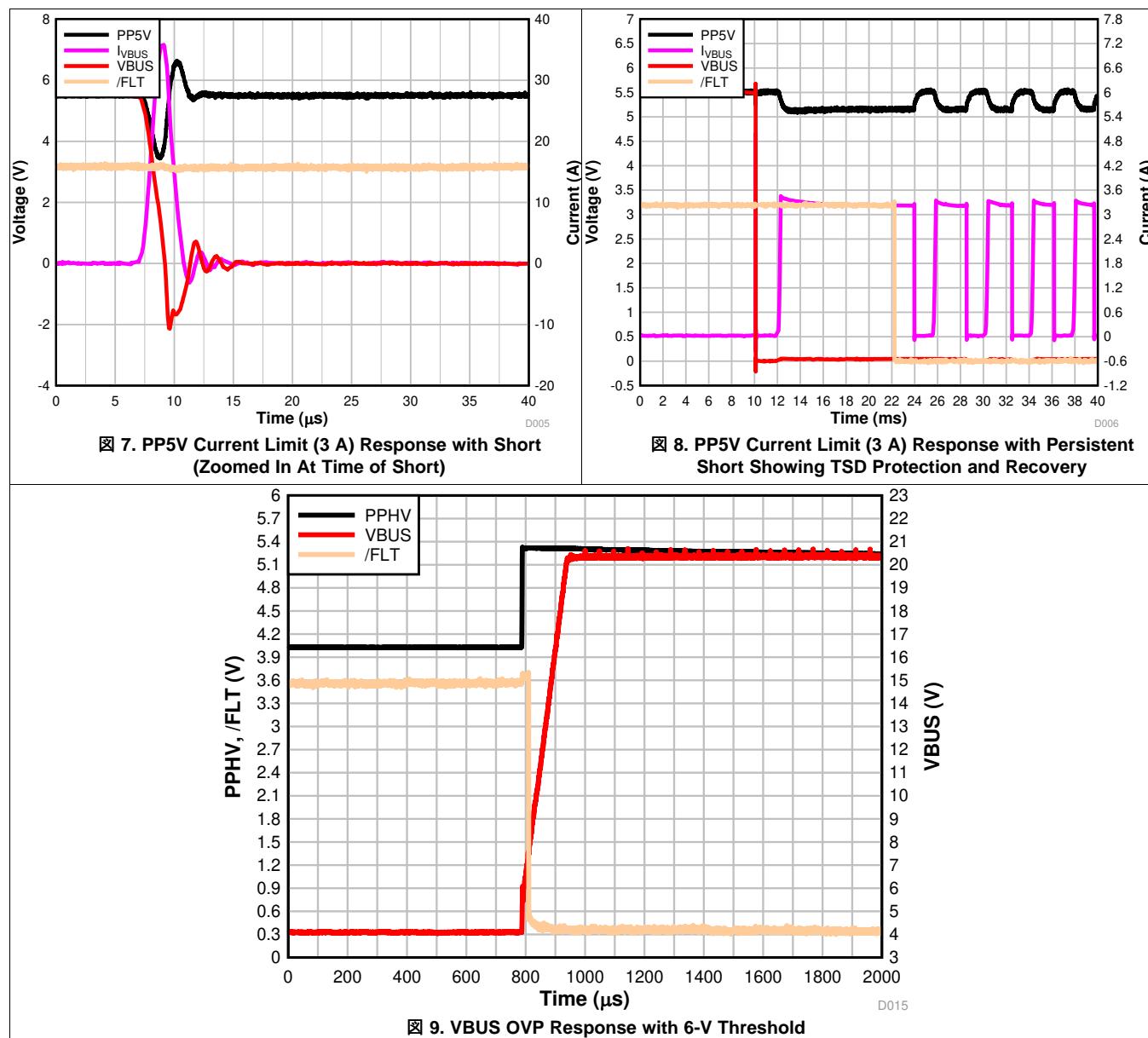


図 6. PP5V Current Limit (3 A) Response with Short (Zoomed Out)

## Typical Characteristics (continued)



## 7 Parameter Measurement Information

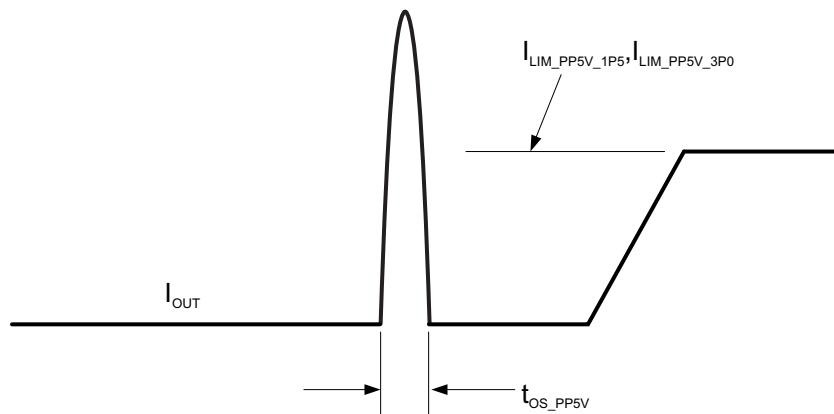


図 10. PP5V to VBUS Short Circuit Parameter Diagram

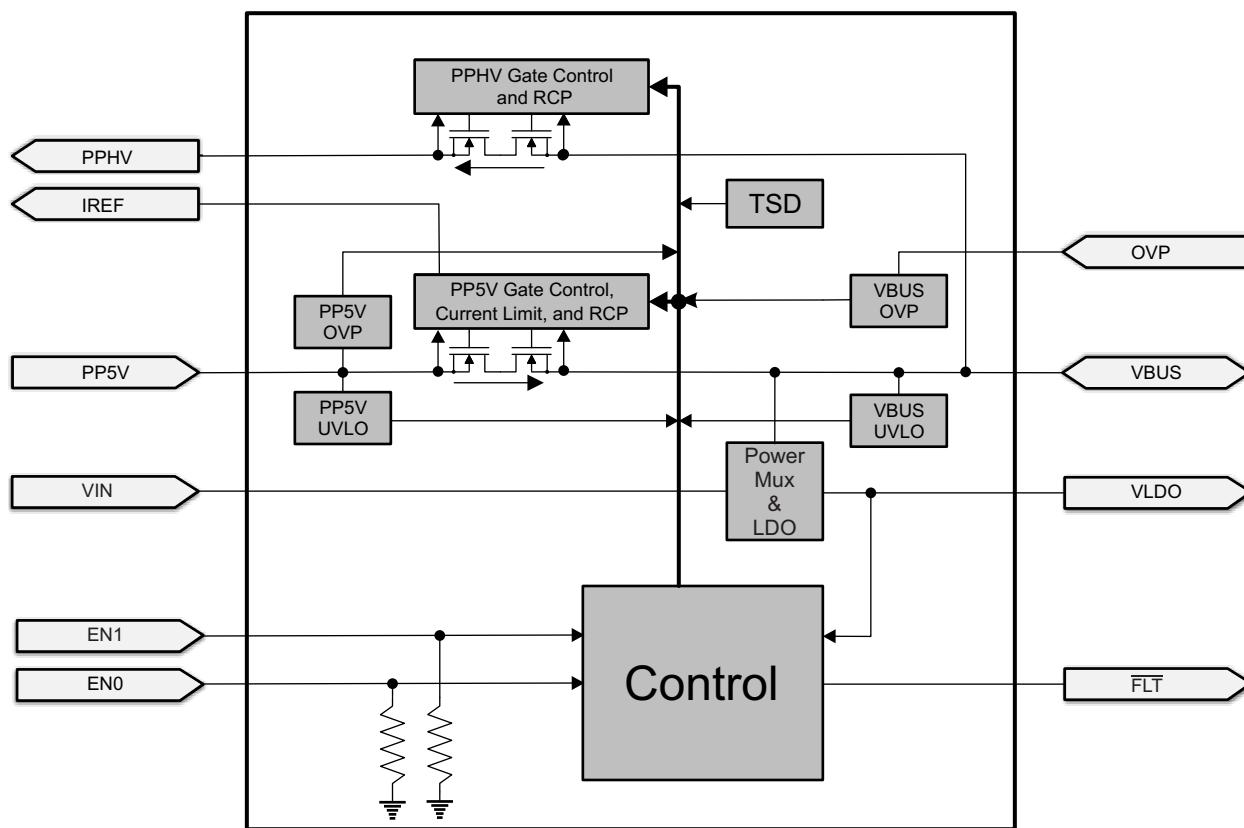
## 8 Detailed Description

### 8.1 Overview

The TPS6602x is a fully featured power multiplexer with an integrated Source power path, a Sink power path, and a high voltage VBUS LDO voltage regulator. The Source power path can supply 5-V nominal power, and supports two current limit settings (1.5 A or 3 A) controlled by general-purpose I/O. The Source power path includes current limit protection, overtemperature protection, reverse-current protection, undervoltage protection, and overvoltage protection. See the [5-V Source \(PP5V Power Path\)](#) section. The Sink power path can support up to 5 A at 20 V controlled by general-purpose I/O. The Sink power path includes soft-start to minimize in-rush currents, overtemperature protection, reverse-current protection, undervoltage protection, and an optional overvoltage protection configured in the application. See the [20-V Sink \(PPHV Power Path\)](#) section. The TPS6602x fully supports Fast Role Swap operation as specified in the Power Delivery specification. See the [Fast Role Swap \(FRS\)](#) section.

The VBUS low dropout voltage regulator may be used in systems that require power during dead battery conditions and can provide up to 30 mA to the system via the VLDO pin. Once VIN power is available, VLDO pin power is switched from the VBUS LDO regulator to the VIN pin. The TPS66020 devices VBUS LDO regulator nominally supplies 3.3 V where the TPS66021 device VBUS LDO nominally supplies 5 V. See the [Power Management and Supervisory](#) section.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 5-V Source (PP5V Power Path)

The PP5V power path uses two back-to-back N-channel MOSFETs, and blocks current in both directions when the power path is disabled. The PP5V power path is a Source only path and when enabled provides power from the PP5V terminal to the VBUS terminal. The PP5V path provides up to 3-A current delivery to VBUS.

## Feature Description (continued)

### 8.3.1.1 PP5V Current Limit

The current through PP5V to VBUS current limit may be dynamically selected to support 1.5-A or 3-A operation via EN0 and EN1. An external resistance to GND on IREF terminal is required to set the bias current for accurate current limit operation.

Under overload conditions, the internal current-limit regulator limits the output current to the selected current limit setting,  $I_{LIM\_PP5V}$ , where  $I_{LIM\_PP5V}$  is  $I_{LIM\_PP5V\_1P5}$  or  $I_{LIM\_PP5V\_3P0}$ , as shown in the [PP5V Power Switch Characteristics](#) table. When an overload condition is present, the device maintains a constant output current, with the output voltage determined by  $(I_{LIM\_PP5V} \times R_{LOAD})$ . Two possible overload conditions can occur. The first overload condition occurs when either: 1) PP5V input voltage is first applied, PP5V source path is enabled (EN1\_EN0 = 10b or EN1\_EN0 = 11b), and a short circuit is presented (load which draws  $I_{OUT} > I_{LIM\_PP5V}$ ), or 2) PP5V input voltage is present and the PP5V source path is enabled into a short circuit. The output voltage is held near zero potential with respect to ground and the TPS6602x ramps the output current to  $I_{LIM\_PP5V}$ . The TPS6602x limits the current to  $I_{LIM\_PP5V}$  until the overload condition is removed or the device begins to thermal cycle. This is demonstrated in [Figure 31](#) where the device was enabled into a short, and subsequently cycles current off and on as the thermal protection engages.

The second condition is when an overload occurs while the PP5V source path is enabled and fully turned on. The device responds to the overload condition within time  $t_{OS\_PP5V}$  (see [Figure 10](#)) when the specified overload (per Electrical Characteristics) is applied. The response speed and shape vary with the overload level, input circuit and rate of application. The current-limit response varies between simply settling to  $I_{LIM\_PP5V}$  or turning off and a controlled return to  $I_{LIM\_PP5V}$ . Similar to the previous case, the TPS6602x limits the current to  $I_{LIM\_PP5V}$  until the overload condition is removed or the device begins to thermal cycle. The TPS6602x thermal cycles if an overload condition is present long enough to activate thermal limiting in any of the above cases. This is due to the relatively large power dissipation  $[(V_{PP5V} - V_{VBUS}) \times I_{LIM\_PP5V}]$  elevating the junction temperature. The PP5V source path turns off when its temperature reaches its thermal shutdown temperature of  $TSD\_PP5V\_R$  while in current limit. The PP5V source path remains off until its temperature cools to  $TSD\_PP5V\_F$  and then re-enables automatically.

### 8.3.1.2 PP5V Reverse Current Protection (RCP)

When the PP5V power path is enabled, the RCP circuitry monitors the voltage across the path. If the RCP monitor detects  $V_{VBUS} - V_{PP5V} \geq V_{RCP\_THRES\_PP5V}$ , the PP5V path will be disabled preventing additional current flow from VBUS to PP5V. The power path will be completely disabled and remain disabled as long as the RCP condition persists. After the RCP event, the PP5V path will automatically re-enable.  $\overline{FLT}$  is asserted when a reverse current protection event occurs on the PP5V path.

### 8.3.2 20-V Sink (PPHV Power Path)

The PPHV path is a Sink only path, providing power from the VBUS terminal to the PPHV terminal when enabled. The PPHV power path uses two back-to-back N-channel MOSFETs, and blocks current in both directions when the power path is disabled.

#### 8.3.2.1 PPHV Soft Start

The TPS6602x PPHV power path has soft start circuitry to control in-rush current when the PPHV power path is enabled. DC loading should be minimized during soft start since the PPHV path may experience high power dissipation especially at higher VBUS voltages. This may lead to a PPHV overtemperature protection event.

#### 8.3.2.2 PPHV Reverse Current Protection (RCP)

When the PPHV power path is enabled, the RCP circuitry monitors the voltage across the path. If the RCP monitor detects  $V_{PPHV} - V_{VBUS} \geq V_{RCP\_THRES\_PPHV}$ , the PPHV path will be disabled preventing additional current flow from PPHV to VBUS. The power path will be completely disabled and remain disabled as long as the RCP condition persists. After the RCP event, the PPHV path will automatically re-enable.  $\overline{FLT}$  is not asserted when a reverse current protection event occurs on the PPHV path.

## Feature Description (continued)

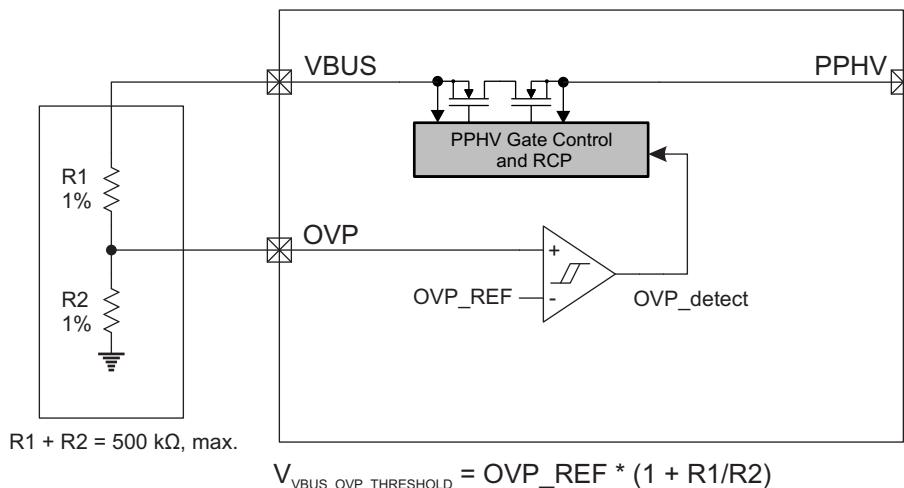
### 8.3.3 Overtemperature Protection

The PP5V and PPHV power paths each have an integrated temperature sensor to protect these paths from excessive heating. When the sensor in each respective path detects an overtemperature condition, the path will be automatically disabled (if enabled) and cannot be enabled until the overtemperature condition has been removed. **FLT** is asserted when an overtemperature event occurs.

In addition, the device has an integrated main temperature sensor. When the sensor detects an overtemperature condition, the PP5V and PPHV power paths and the VBUS LDO of the device are completely disabled until the overtemperature condition has been removed.

### 8.3.4 VBUS Overvoltage Protection (OVP)

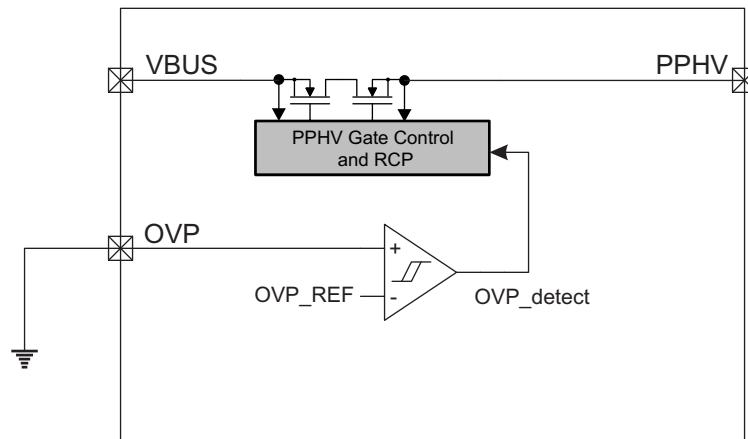
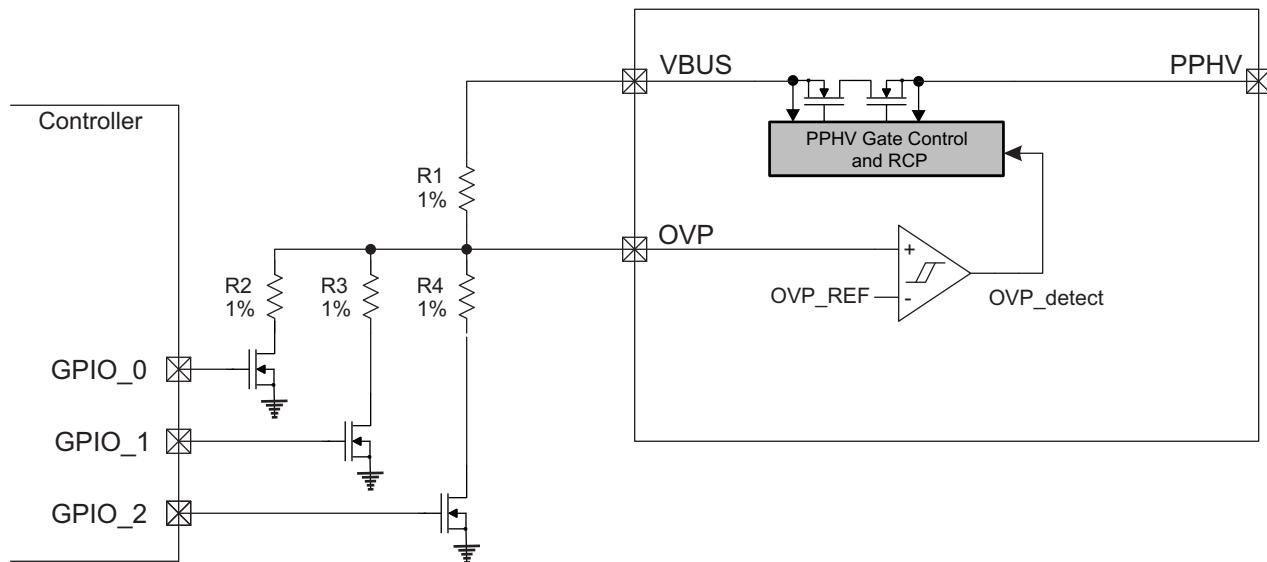
TPS6602x supports overvoltage protection on the VBUS terminal. When the voltage detected on OVP exceeds a set level, the PPHV power path will automatically be disabled (if enabled), and will remain disabled until the OVP event is removed. **FLT** is asserted when an overvoltage event occurs. The VBUS OVP threshold may be set using a resistor divider from VBUS to GND, whose divider output is connected to the OVP terminal as shown in [図 11](#). [表 1](#) shows resistor divider settings for common USB Power Delivery fixed voltage supply contracts along with the resulting nominal OVP thresholds. These thresholds may be adjusted based on desired margins for a given application. If VBUS OVP is not required or needs to be disabled, the OVP terminal may be tied or driven to GND as shown in [図 12](#). Lastly, as one example implementation, the OVP threshold may be controlled dynamically using outputs from a PD controller or microcontroller as shown in [図 13](#). By selecting each output, different VBUS OVP threshold settings are possible.



**図 11. VBUS OVP Threshold Set by External Resistor Divider**

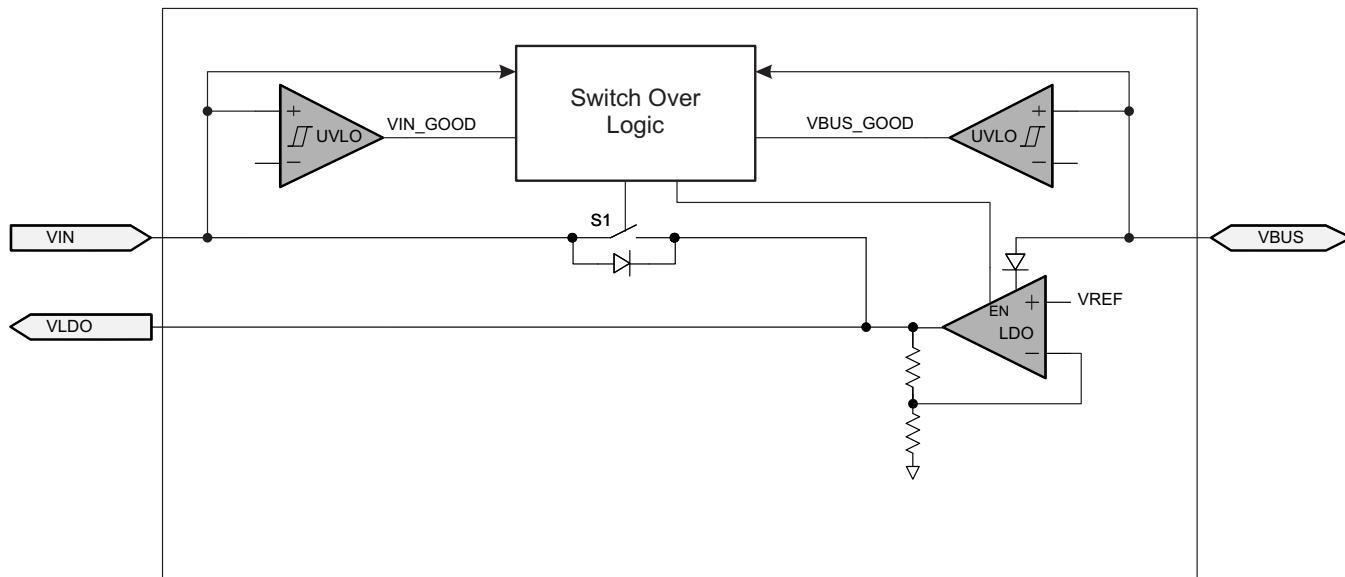
**表 1. Typical External Resistor Divider Settings**

PD Fixed Contract	R1, kΩ	R2, kΩ	Nominal VBUS OVP Threshold, V
5 V	102	20	6.1
9 V	182	20	10.1
15 V	309	20	16.5
20 V	432	20	22.6


**図 12. VBUS OVP Disabled**

**図 13. Selectable VBUS OVP Thresholds**

### 8.3.5 Power Management and Supervisory

The TPS6602x Power Management block receives power from VIN or VBUS and generates voltages to provide power to the TPS6602x internal circuitry, as well as, provides power to VLDO. The power supply management and supervisory block is shown in [図 14](#).



**図 14. Power Management and Supervisory**

The VLDO terminal may be powered from either VIN or VBUS. The normal power supply input is VIN. When VIN is present, S1 is closed and current flows from VIN to VLDO and the VBUS LDO is disabled. When VIN power is unavailable, as in a dead battery condition, the VBUS LDO will be automatically enabled when VBUS is present, and the VLDO terminal is powered by the VBUS LDO. The Switch Over Logic provides the decision making capability to choose VIN or VBUS power, depending on the state of these voltages (based on their respective UVLO comparators) and their relative levels to each other.

#### 8.3.5.1 Supply Connections

図 15 shows the TPS66020 VIN being supplied from a 3.3-V supply. The VLDO output may or may not be used to supply other circuitry in the application, for example a PD Controller. During a dead battery condition, the internal 3.3-V VBUS LDO provides power to the TPS66020 and the VLDO output. Once VIN input supply becomes available, the VBUS LDO is disabled and VIN provides power to the VLDO output.

The TPS66021 is well suited for 5 V only systems. VIN of the TPS66021 may be powered from an independent supply, but in most applications it will be connected to the PP5V supply. 図 16 shows where the VIN supply is shared with PP5V. The VLDO output may be used optionally to supply power to external circuitry. During a dead battery condition, the internal 5-V VBUS LDO provides power to the TPS66021 and the VLDO output. Once the VIN input supply, in this case PP5V, becomes available, the VBUS LDO is disabled and PP5V provides power to the VLDO output.

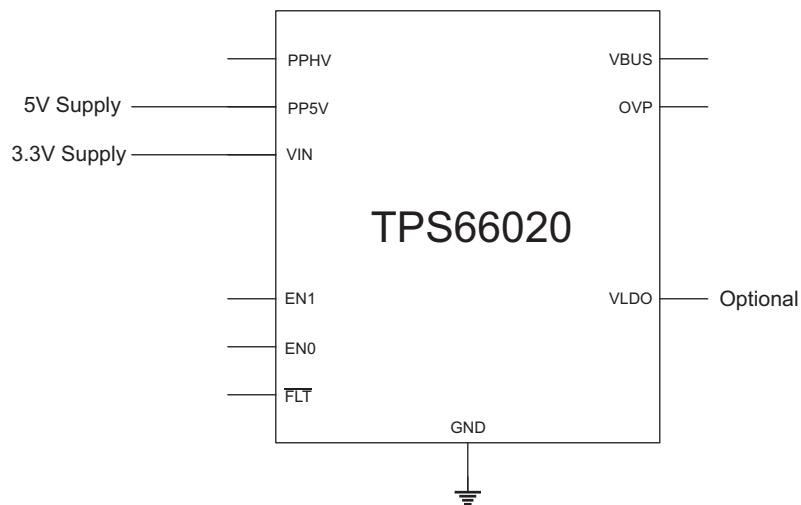


図 15. TPS66020 VIN 3.3-V Supply

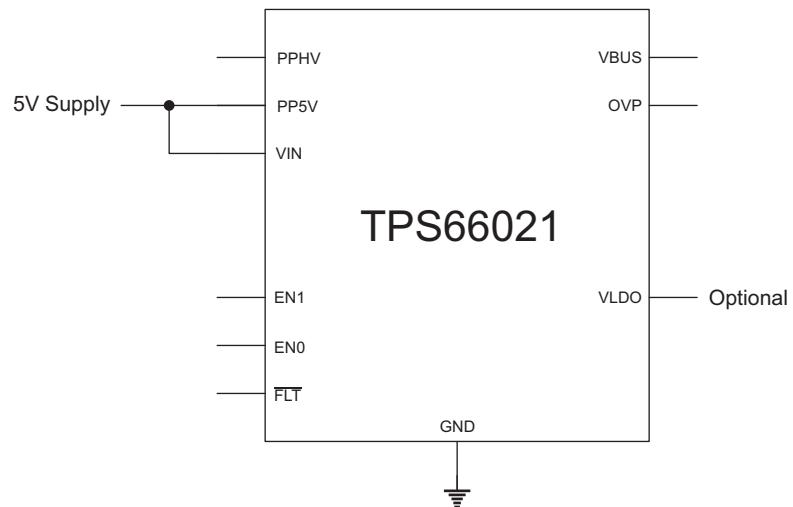
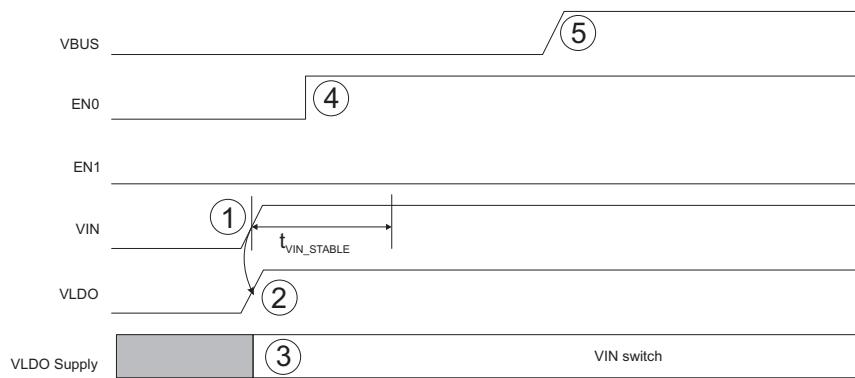


図 16. TPS66021 VIN 5-V Shared Supply

### 8.3.5.2 Power Up Sequences

#### 8.3.5.2.1 Normal Power Up

図 17 shows a typical power up sequence. During normal power up, VIN supplies power to the TPS6602x. In this case, VBUS remains powered down. It is assumed a PD Controller is controlling the TPS6602x, and Sink operation is being requested.



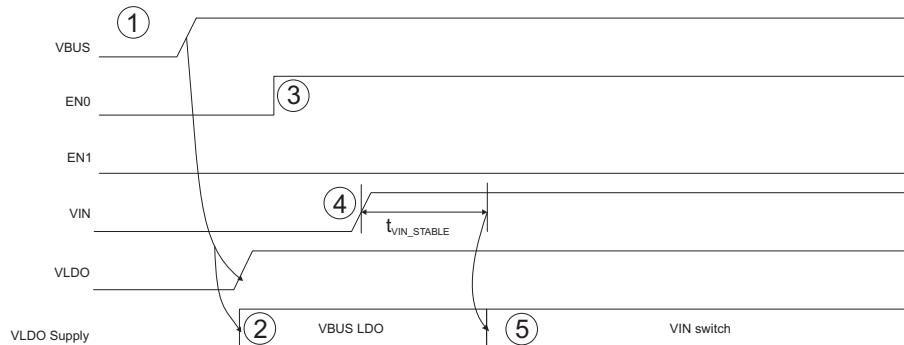
**图 17. Normal Power Up Sequence**

#### 8.3.5.2.2 Dead Battery Operation

图 18 shows the typical power up sequence during a dead battery condition. During a dead battery condition, the TPS6602x is internally powered by the VBUS LDO. The VBUS LDO may be used to supply a limited amount of current for use in the system during dead battery, such as supplying power to a PD controller. In this case, it is assumed the VLDO terminal is providing power to a PD controller that is controlling the TPS6602x. Once VIN is stable, the VLDO terminal switches from being supplied by the VBUS LDO to being supplied by the VIN terminal, and the VBUS LDO is automatically disabled. The switch over process is completely seamless.

**注**

Switching from VBUS LDO operation to VIN operation is seamless and no device reset will occur. When switching from VIN power to VBUS LDO operation, the switch over circuitry will attempt to switch over to the VBUS LDO, however it is not assured that the VLDO level will be maintained above the VLDO UVLO threshold. In this case, a device reset may or may not occur.



1. Device is in dead battery condition. PD controller advertises as a Sink. Upon connection to a Source, VBUS begins to rise.

2. VBUS LDO is selected by the power management logic and VLDO begins to rise.

3. PD Controller negotiates a contract (may be 5V or higher) and asserts EN0 to turn on the PPHV Sink path in order to charge the system.

4. System begins to charge and VIN begins to rise. VIN passes its UVLO threshold.

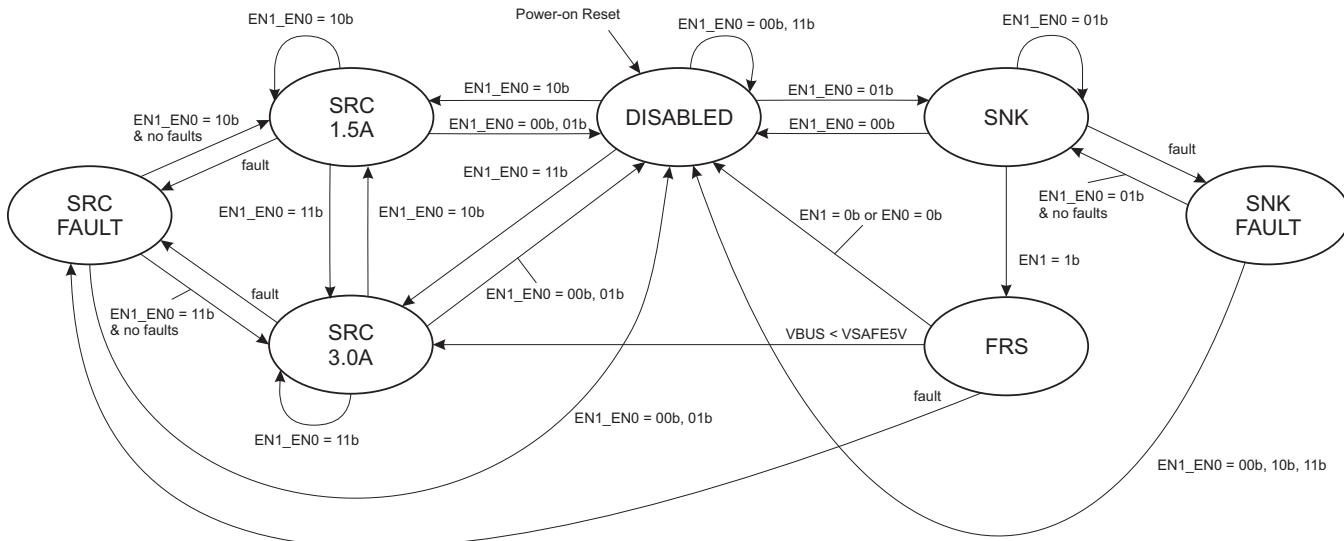
5. If VIN supply remains above its UVLO threshold for  $t_{VIN\_STABLE}$ , VBUS LDO is disabled and VLDO is switched over to be supplied by VIN via switch S1.

**图 18. Dead Battery Power Up Sequence**

## 8.4 Device Functional Modes

### 8.4.1 State Transitions

EN0 and EN1 are used by the application to control the state of the device. [图 19](#) shows the supported state transitions.



**图 19. TPS6602x Functional State Diagram**

#### 8.4.1.1 DISABLED State

In the DISABLED state, EN1 = 0, EN0 = 0. While in the DISABLED state:

- PP5V power path is disabled
- PP5V current limit, overvoltage, overtemperature, and reverse current protections are disabled
- PPHV power path is disabled
- PPHV overtemperature, reverse-current, and VBUS overvoltage protections are disabled
- VIN and VBUS undervoltage lockout are enabled

The following transitions are possible from the DISABLED state:

- SRC 1.5-A state if (EN1 = 1) and (EN0 = 0) and (PP5V UVLO event not detected) and (PPHV path is completely off)
- SRC 3.0-A state if (EN1 = 1) and (EN0 = 1) and (PP5V UVLO event not detected) and (PPHV path is completely off)
- SNK state if (EN1 = 0) and (EN0 = 1) and (VBUS UVLO event not detected) and (PP5V is completely off)

#### 8.4.1.2 SRC 1.5-A State

In the SRC 1.5-A state, EN1 = 1, EN0 = 0. While in the SRC 1.5-A state:

- PP5V power path is enabled with current limit set to  $I_{LIM\_PP5V\_1P5}$
- PP5V overvoltage, overtemperature and reverse current protections are enabled
- PPHV power path is disabled
- PPHV overtemperature, reverse-current and VBUS overvoltage protections are disabled
- VIN and PP5V undervoltage lockout are enabled

The following transitions are possible from the SRC 1.5-A state:

- SRC 3-A state if (EN1 = 1) and (EN0 = 1)
- DISABLED state if:
  - (EN1 = 0) and (EN0 = 0) -or-
  - (EN1 = 0) and (EN0 = 1)

## Device Functional Modes (continued)

- SRC FAULT state if:
  - PP5V UVLO, PP5V OVP, or PP5V RCP event detected -or-
  - PP5V current limit and PP5V TSD events detected

### 8.4.1.3 SRC 3-A State

In the SRC 3-A state, EN1 = 1, EN0 = 1. While in the SRC 3-A state:

- PP5V power path is enabled with current limit set to  $I_{LIM\_PP5V\_3P0}$
- PP5V overvoltage, overtemperature and reverse current protections are enabled
- PPHV power path is disabled
- PPHV overtemperature, reverse-current, and VBUS overvoltage protections are disabled
- VIN and PP5V undervoltage lockout are enabled

The following transitions are possible from the SRC 3-A state:

- SRC 1.5-A state if (EN1 = 1) and (EN0 = 0)
- DISABLED state if:
  - (EN1 = 0) and (EN0 = 0) -or-
  - (EN1 = 0) and (EN0 = 1)
- SRC FAULT state if:
  - PP5V UVLO, PP5V OVP, or PP5V RCP event detected -or-
  - PP5V current limit and PP5V TSD events detected

### 8.4.1.4 SNK State

In the SNK state, EN1 = 0, EN0 = 1. While in the SNK state:

- PP5V power path is disabled
- PP5V overvoltage, overtemperature and reverse current protections are disabled
- PPHV power path is enabled
- PPHV overtemperature, VBUS overvoltage (if OVP terminal not grounded) and reverse-current protections are enabled
- VIN and VBUS undervoltage lockout are enabled

The following transitions are possible from the SNK state:

- FRS (Fast Role Swap) state
- DISABLED state if:
  - (EN1 = 0) and (EN0 = 0)
- SNK FAULT state if:
  - VBUS OVP (if OVP terminal not grounded) event detected -or-
  - PPHV TSD event detected

### 8.4.1.5 FRS (Fast Role Swap) State

In the FRS state, EN1 = 1, EN0 = 1. The FRS state is a transitional state, that transitions automatically from the SNK state to the SRC 3-A state upon successful completion of the fast role swap sequence:

- PPHV power path is automatically disabled
- PPHV overtemperature, VBUS overvoltage (if OVP terminal not grounded) protections are disabled
- VIN and PP5V undervoltage lockout are enabled
- PP5V power path is automatically enabled along with its overvoltage, overtemperature and RCP protection circuits upon successfully completing the fast role swap sequence.

The following transitions are possible from the FRS state:

- SRC 3-A state. This transition is automatic upon successful completion of the fast role swap sequence.
- DISABLED state if:
  - (EN1 = 0) or (EN0 = 0). This may allow for exiting a FRS sequence depending on the current status of the

## Device Functional Modes (continued)

FRS sequence.

- SRC FAULT state if:
  - PP5V UVLO, PP5V OVP event detected -or-
  - PP5V current limit and PP5V TSD events detected

### 8.4.2 SRC FAULT State

The SRC FAULT state is entered when any PP5V fault event is detected. Upon entering the SRC FAULT state, the PP5V power path is disabled. The following transitions are possible from the SRC FAULT state:

- DISABLED state if:
  - (EN1 = 0) and (EN0 = 0) -or-
  - (EN1 = 0) and (EN0 = 1)
- SRC 1.5-A state if:
  - (EN1 = 1) and (EN0 = 0) -and-
  - PP5V TSD, PP5V OVP, PP5V RCP, PP5V UVLO, and PP5V current limit events are not detected.
- SRC 3-A state if:
  - (EN1 = 1) and (EN0 = 1) -and-
  - PP5V TSD, PP5V OVP, PP5V RCP, PP5V UVLO, and PP5V current limit events are not detected.

### 8.4.3 SNK FAULT State

The SNK FAULT state is entered when any PPHV fault event is detected. Upon entering the SNK FAULT state, the PPHV power path is disabled. The following transitions are possible from the SNK FAULT state:

- DISABLED state if:
  - (EN1 = 1) or (EN0 = 0)
- SNK state if:
  - (EN1 = 0) and (EN0 = 1) -and-
  - PPHV TSD, VBUS OVP (if OVP terminal not grounded) events are not detected

### 8.4.4 Device Functional Mode Summary

[表 2](#) summarizes the functional modes for the TPS6602x. As shown, the enabling and disabling of the respective Source or Sink is dependent upon the voltages present on PP5V and VBUS, as well as, the EN0 and EN1 control signals.

## Device Functional Modes (continued)

表 2. TPS6602x Device Functional Modes<sup>(1)</sup>

EN1	EN0	VIN	V <sub>VBUS</sub>	V <sub>PP5V</sub>	FLT	Device State	Source Path	Sink Path
0	0	≥ UV_VIN	X	X	Hi-Z	DISABLED	Disabled Safety engaged.	Disabled Safety engaged.
1	0	≥ UV_VIN	X	≥ UV_PP5V	Hi-Z	SRC 1.5 A	Enabled RCP, OVT, ILIM 1.5-A enabled.	Disabled Safety engaged.
					L	SRC FAULT	Disabled OVP, OVT, ILIMIT, or RCP event.	Disabled Safety engaged.
				< UV_PP5V	L	SRC FAULT	Disabled PP5V UVLO event.	Disabled Safety engaged.
1	1	≥ UV_VIN	X	≥ UV_PP5V	Hi-Z	SRC 3 A	Enabled RCP, OVT, ILIM 3-A enabled.	Disabled Safety engaged.
					L	SRC FAULT	Disabled OVP, OVT, ILIMIT, or RCP event.	Disabled Safety engaged.
				< UV_PP5V	L	SRC FAULT	Disabled PP5V UVLO event.	Disabled Safety engaged.
0	1	≥ UV_VIN	≥ UV_VBUS	X	Hi-Z	SNK	Disabled Safety engaged.	Enabled RCP, OVT enabled
				X	Hi-Z	SNK FAULT	Disabled Safety engaged.	Enabled with Blocking RCP event.
				X	L	SNK FAULT	Disabled Safety engaged.	Disabled OVP <sup>(2)</sup> or OVT event.
			< UV_VBUS	X	Hi-Z	SNK FAULT	Disabled Safety engaged.	Disabled VBUS UVLO event.
1	1	≥ UV_VIN	≥ vSafe5V	≥ UV_PP5V	Hi-Z	FRS	Disabled OVT, ILIM 3-A enabled	Disabled Safety engaged.
			< vSafe5V	≥ UV_PP5V	Hi-Z	SRC 3 A	Enabled RCP, OVT, ILIM 3-A enabled	Disabled Safety engaged.
				≥ UV_PP5V	L	SRC FAULT	Disabled OVP, OVT, ILIMIT, or RCP event.	Disabled Safety engaged.
				< UV_PP5V	L	SRC FAULT	Disabled PP5V UVLO event.	Disabled Safety engaged.
X	X	< UV_VIN	< UV_VBUS	X	Hi-Z	DISABLED	Disabled Safety engaged.	Disabled Safety engaged.
0	0	< UV_VIN	≥ UV_VBUS	X	Hi-Z	DISABLED	Disabled Safety engaged.	Disabled Safety engaged.
1	0	< UV_VIN	≥ UV_VBUS	≥ UV_PP5V	L	SRC FAULT	Disabled RCP, OVT, ILIM 1.5A enabled	Disabled Safety engaged.
1	1	< UV_VIN	≥ UV_VBUS	≥ UV_PP5V	L	SRC FAULT	Disabled RCP, OVT, ILIM 3A enabled	Disabled Safety engaged.

(1) X: do-not-care.

(2) When OVP function used and VBUS exceeds OVP threshold, V<sub>VBUS\_OVP\_THRESHOLD</sub>.

## Device Functional Modes (continued)

表 2. TPS6602x Device Functional Modes<sup>(1)</sup> (continued)

EN1	EN0	VIN	V <sub>VBUS</sub>	V <sub>PP5V</sub>	FLT	Device State	Source Path	Sink Path
0	1	< UV_VIN	UV_VBUS <sup>(3)</sup>	X	Hi-Z	SNK	Disabled Safety engaged.	Enabled RCP, OVT enabled
				X	Hi-Z	SNK FAULT	Disabled Safety engaged.	Enabled with Blocking RCP event.
				X	L	SNK FAULT	Disabled Safety engaged.	Disabled OVP <sup>(2)</sup> or OVT event.
			< UV_VBUS <sup>(3)</sup>	X	Hi-Z	SNK FAULT	Disabled Safety engaged.	Disabled VBUS UVLO event.

(3) In this case VLDO is supplying power to the device.

### 8.4.5 Enabling the PP5V Source Path

The timing diagram of enabling the PP5V Source path with a current limit set to 1.5 A is shown in [图 20](#). As shown, transitions from either the Source path to the Sink path or vice-versa always requires a transition first to the DISABLED state, EN1\_EN0 = 00b. [图 21](#) shows the timing diagram going from a Sink to a 3-A Source. [图 22](#) shows changing the current limit back to 1.5 A from its original 3-A setting.

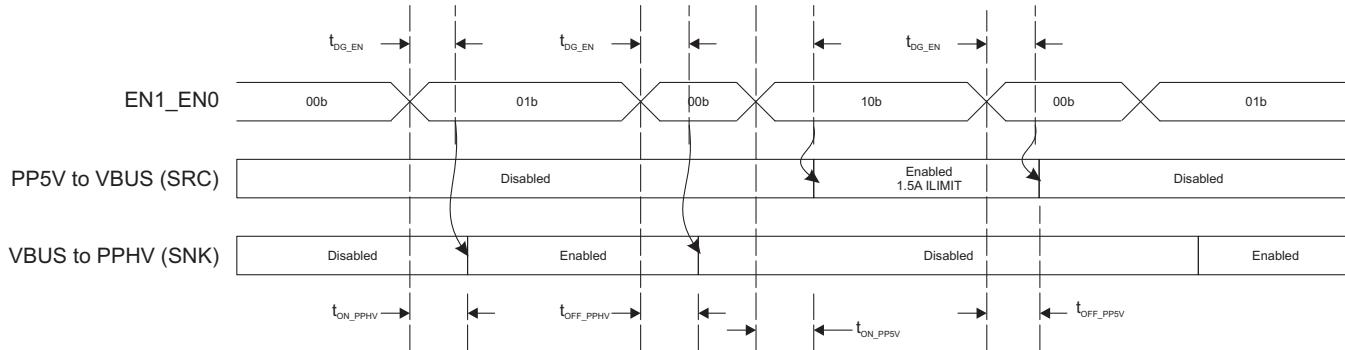


图 20. Enabling the PP5V Source Path to 1.5-A Current Limit

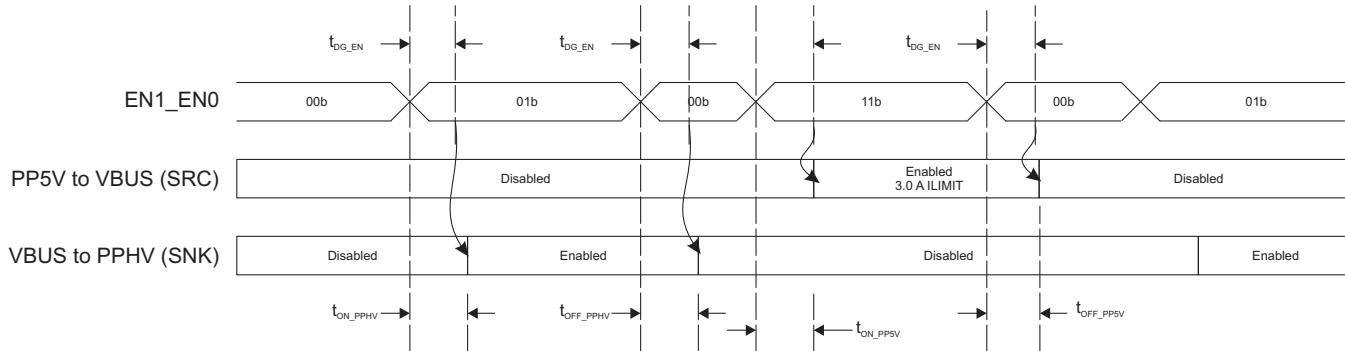


图 21. Enabling the PP5V Source Path to 3-A Current Limit

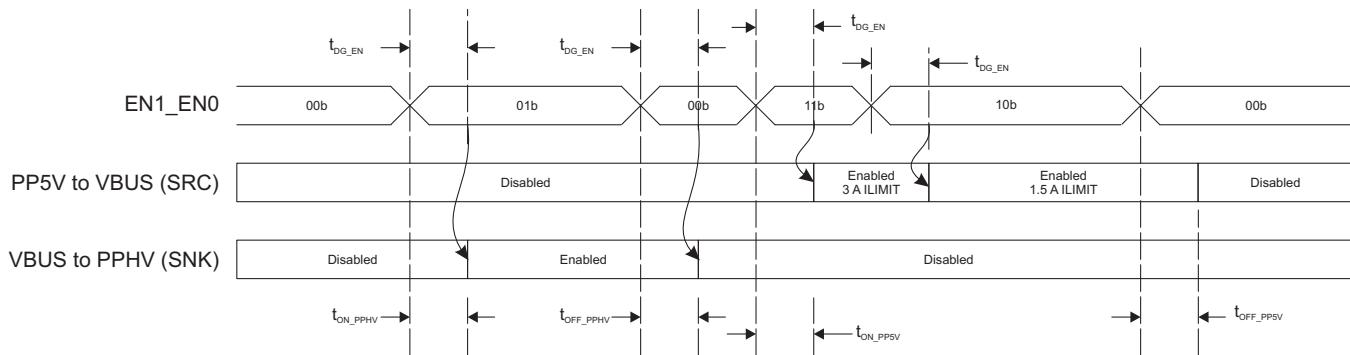


图 22. Changing the PP5V Source Path from 3-A to 1.5-A Current Limit

#### 8.4.6 Enabling the PPHV Sink Path

The timing diagram of enabling the PPHV Sink path is shown in 图 23. As stated earlier, transitions from either the Source path to the Sink path or vice-versa always requires a transition first to the DISABLED state, EN1\_EN0 = 00b.

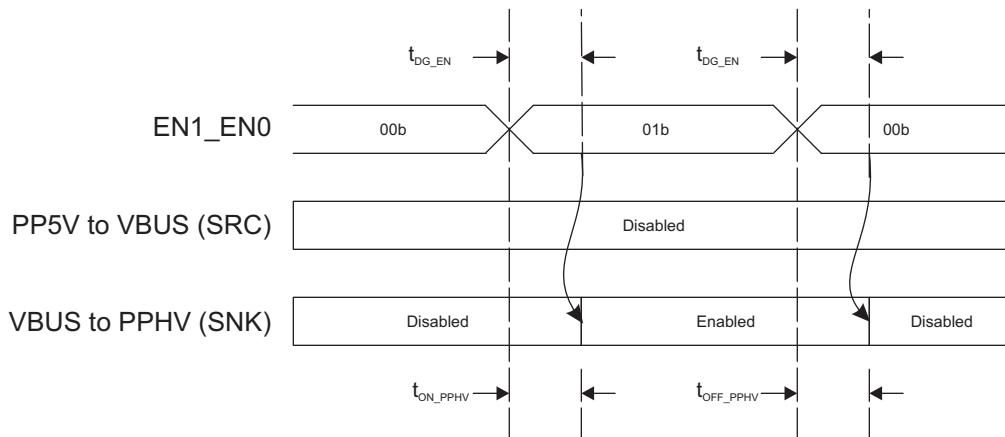


图 23. Enabling the PPHV Sink Path

#### 8.4.7 Fast Role Swap (FRS)

##### 8.4.7.1 Overview

For a hub application, the hub may be supplied by an external power source that is supplying power to a Host (via the Source path of the dual-role power (DRP) of the hub), as well as, a downstream Bus Powered Device (BPD) (DFP Source to the BPD). A communication path is formed from Host to the Bus Powered Device. Prior to FRS, power flows from the external power source to the Host and the Bus Powered Device. If the external power is removed, FRS operation will attempt to change the power role of the Host to a Source and the hub DRP port to a Sink allowing power to change direction from the Host to the BPD in an attempt to maintain the connection. It should be noted that after FRS, the contract is 5 V. Refer to the PD3.0 specification for further details on the Fast Role Swap function.

Two PD controllers are used in the FRS process. One PD controller resides on the Host side (USB PD Capable Host); the other resides on the hub side (USB PD Capable Hub). Both PD controllers are DRP since they must support power role swapping. Prior to FRS, the Hub DRP is a Source (known as the old Source) and may be supplying power to the DRP Host, which is acting as a Sink (known as the old Sink). After FRS, the Host DRP is a 5-V Source (known as the new Source, old Sink), and is supplying power to the Hub DRP configured as a Sink (known as the new Sink, old Source).

#### 8.4.7.2 Fast Role Swap Use Cases

When the TPS6602x is used on the Host side, prior to a FRS event, the PD Controller power role is the Sink (old Sink). Since the TPS6602x only supports Sink operation via PPHV, PPHV is configured as a Sink (old Sink) and is receiving power from VBUS. Upon fast role signaling from the Hub, the TPS6602x power role will change to a Source (new Source) via the PP5V path.

注

The TPS6602x does not support a fast turn-on of the PPHV path, so it cannot be used effectively as a new Sink in a fast role condition. Fast turn-on is only possible with the PP5V (Source only path) for fast role swap scenarios.

图 24 shows the supported TPS6602x usage case before and after a fast role swap. The TPS6602x is used in the Host DRP. Prior to a fast role swap, PPHV is configured as a Sink (old Sink) and the PP5V path is disabled. Once a Fast Role Swap signal is requested by the PD Controller, by the transition of EN1\_EN0 from 01b to 11b, the TPS6602x disables its PPHV path, waits until VBUS drops vSafe5V (maximum) and then quickly enables the PP5V path, which is now the new Source.

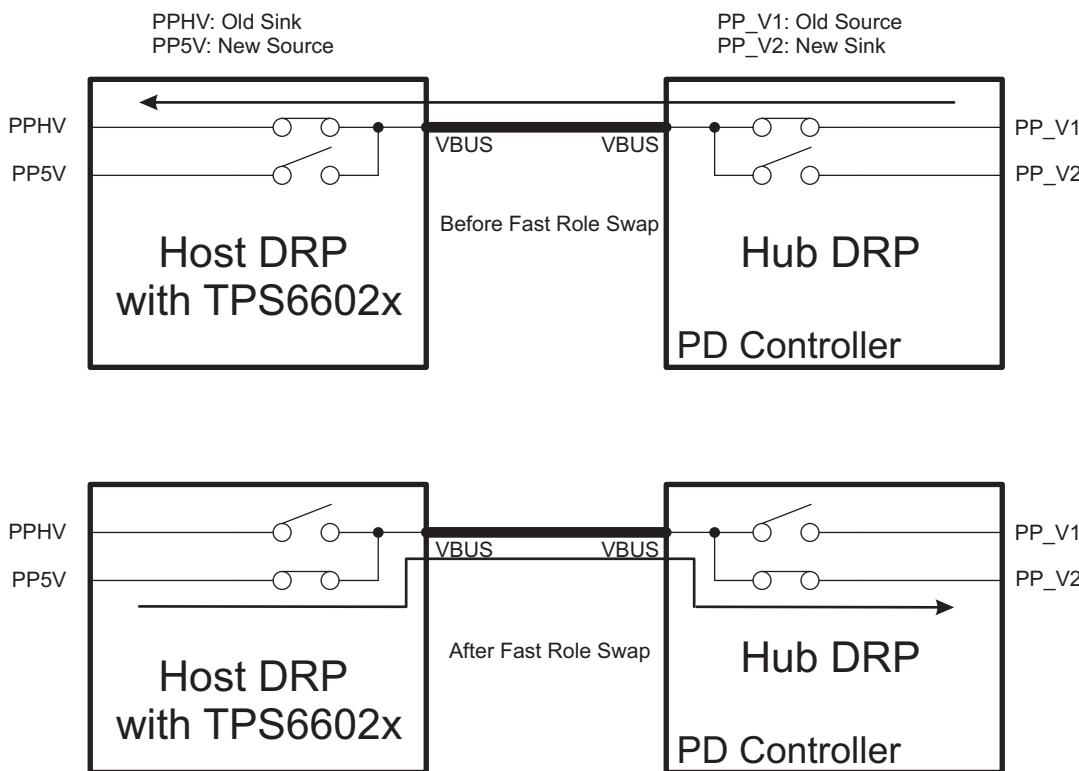


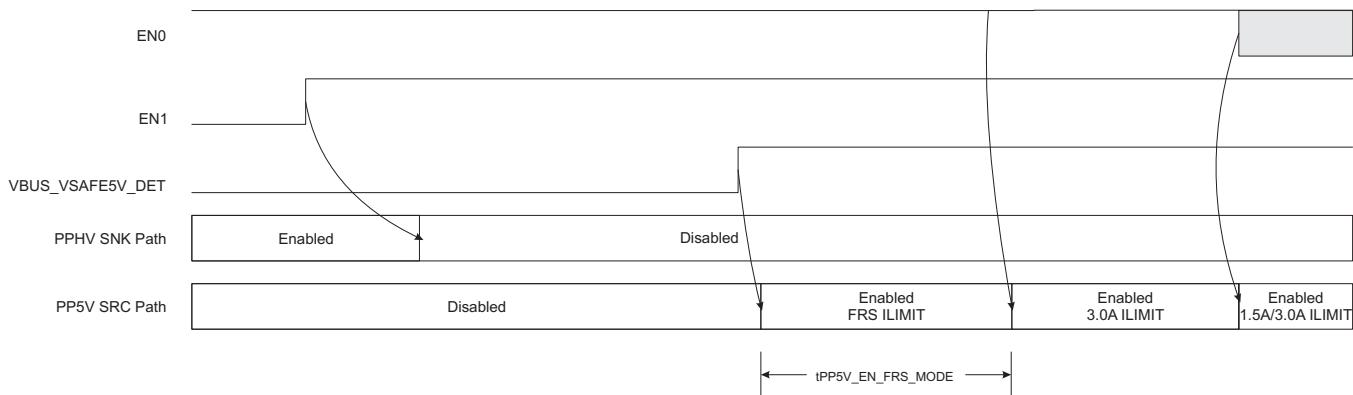
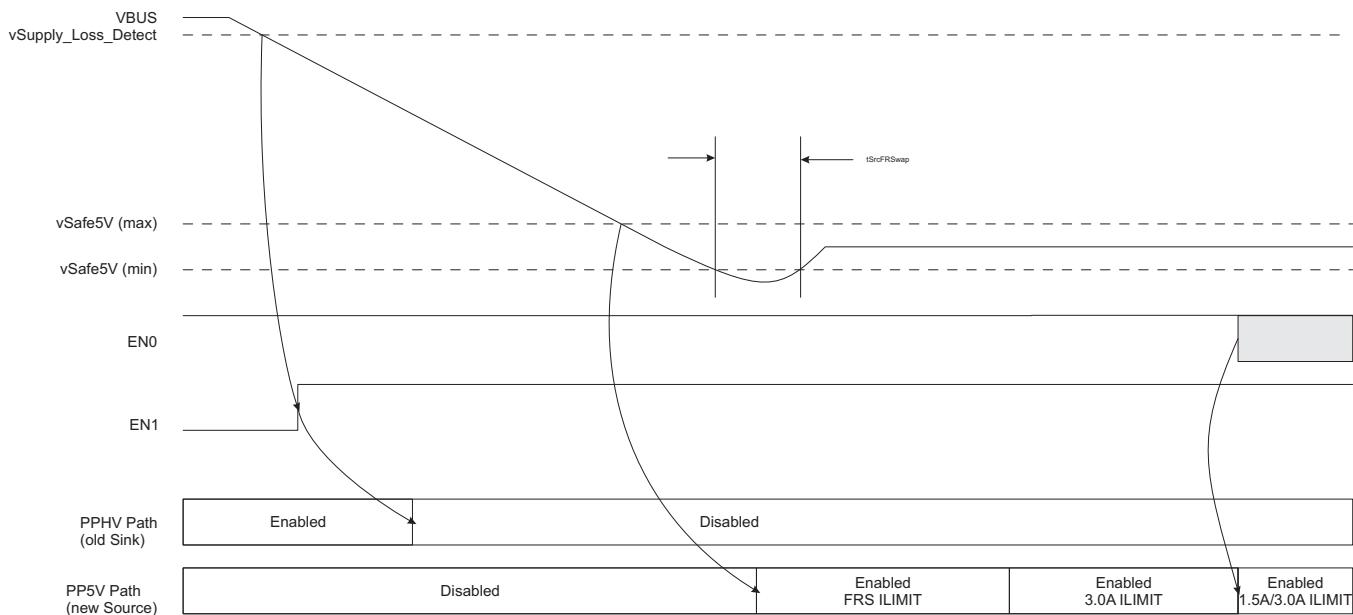
图 24. TPS6602x Fast Role Swap Usage Case

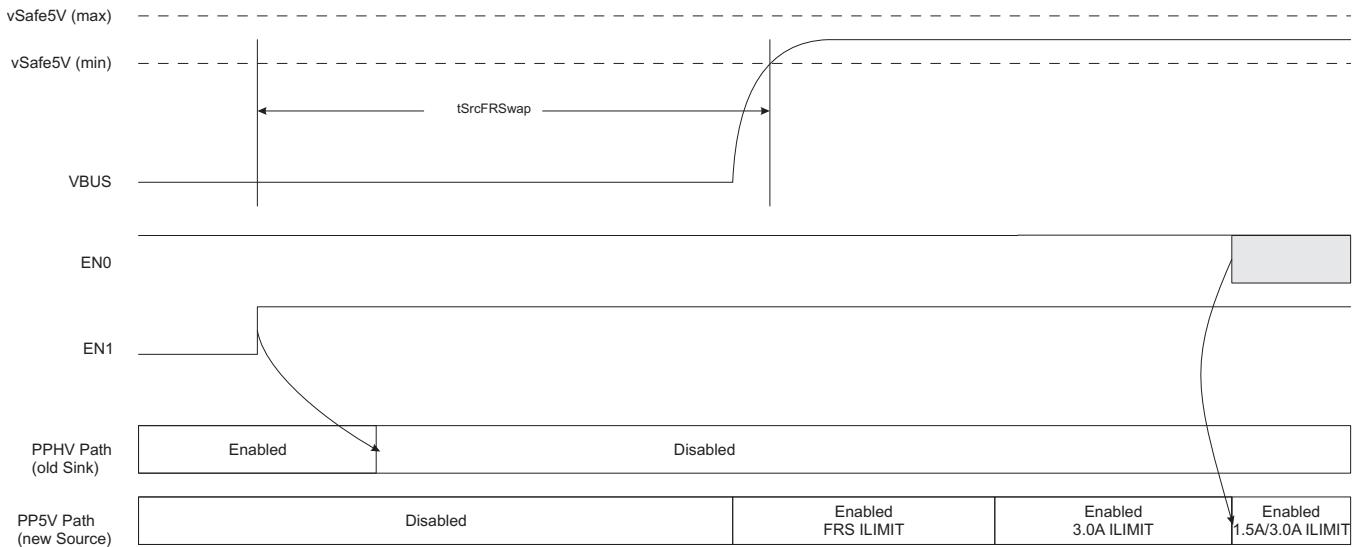
#### 8.4.7.3 Fast Role Swap Sequence

The TPS6602x supports specialized hardware to minimize unnecessary delays upon a Fast Role Swap event. 图 25 shows the fast role swap sequencing.

1. At some point, the Hub device connected to the Host detects a power loss condition and begins to transmit fast role swap signaling on its CC line to the Host PD Controller.
2. The Host PD Controller's CC detection circuitry detects fast role swap signaling applied by observing the CC line and is validated.
3. Upon validating the FRS signaling, the Host PD Controller shall assert EN1 = 1 of the TPS6602x as soon as possible to initiate the power role swap. It should be noted that since the transition of the FRS is initiated by the PD Controller, it is critical that the delay from detection of the FRS signaling to the assertion of EN1 be minimized.

4. Upon  $EN1 = 1$  assertion, the TPS6602x PPHV path is disabled automatically by the fast role swap hardware.
5. There are two cases to consider. In Case 1, as shown in **図 26**, VBUS begins to decay, while being continuously monitored by the vSafe5V comparator circuitry that indicates when VBUS has fallen below vSafe5V. Once this occurs, the comparator output is asserted indicating to the fast role swap hardware that it is safe to turn on the PP5V path, and the PP5V path is enabled automatically. In Case 2, as shown in **図 27**, VBUS may have fallen below vSafe5V, or even fully discharged to ground, so the comparator output may already be asserted low. If so, the PP5V path shall be immediately enabled. It should be noted in this scenario, since the VBUS capacitance has been fully discharged, a significant in-rush current will occur when the PP5V path is enabled. Application should ensure sufficient decoupling capacitance is applied on the PP5V supply or that the supply is designed to react to fast transient responses to avoid brown-out of the supply rail.
6. PP5V is initially enabled with a higher current limit to ensure fast turn-on. Once fast role swap is completed, it reverts back to the 3-A setting. The application may then choose to stay at the 3-A setting or switch to the 1.5-A setting.


**図 25. Fast Role Swap Timing**

**図 26. Fast Role Swap Events - Case 1**


**图 27. Fast Role Swap Events - Case 2**

#### 8.4.8 Faults

The TPS6602x includes a fault pin,  $\overline{\text{FLT}}$ . The  $\overline{\text{FLT}}$  pin is an open-drain output and requires an external pull-up resistor. If the  $\overline{\text{FLT}}$  pin is not required, it may be tied to GND or left floating. The  $\overline{\text{FLT}}$  pin will be asserted low only under certain conditions and not all fault conditions will assert the  $\overline{\text{FLT}}$  pin, see [表 3](#). If the  $\overline{\text{FLT}}$  pin is asserted, it will remain asserted for a minimum of  $t_{\text{HOLD\_FLT}}$  regardless if the fault condition is removed. After  $t_{\text{HOLD\_FLT}}$ , if all fault conditions have surpassed, the  $\overline{\text{FLT}}$  pin is released.

##### 8.4.8.1 Fault Types

[表 3](#) summarizes the various fault types available and when the  $\overline{\text{FLT}}$  shall be asserted.

**表 3. Fault Types**

Fault Name	Fault	$\overline{\text{FLT}}$	Description
PP5V_UVLO	PP5V undervoltage Lockout	Low	If PP5V input supply is below the PP5V UVLO threshold, the PP5V path is disabled automatically if enabled or remains disabled until the PP5V UVLO threshold is exceeded. If a SRC state is selected to be entered, the device will remain in the DISABLED state until the UVLO event is removed. The $\overline{\text{FLT}}$ pin will not be asserted. If a SRC state has been entered successfully and a UVLO event occurs, the device will enter the DISABLED state, and the $\overline{\text{FLT}}$ pin will be asserted.
PP5V_OVP	PP5V overvoltage Protection	Low	If a SRC state is selected to be entered or device currently is in a SRC state (SRC 1.5 A or SRC 3 A) and the PP5V input supply rises above the PP5V OVP threshold, the PP5V path is disabled automatically and the $\overline{\text{FLT}}$ pin will be asserted.
PP5V_ILIMIT	PP5V Current Limit Protection	Low	The PP5V power path has a closed-loop current limit protection. If the load current exceeds the selected current limit, the control loop will increase the voltage across the FET to compensate. Note: $\overline{\text{FLT}}$ will not be asserted unless the current limit event lasts longer than $t_{\text{ILIMIT\_FLT}}$ .
PP5V_OVT	PP5V overtemperature Protection	Low	If a SRC state is selected to be entered or device currently is in a SRC state (SRC 1.5 A or SRC 3 A) and the local temperature of PP5V power path exceeds $T_{\text{SD\_PP5V\_R}}$ while in current limit, the PP5V path is disabled automatically and the $\overline{\text{FLT}}$ pin will remain asserted. PP5V power path will remain disabled until temperature falls below $T_{\text{SD\_PP5V\_F}}$ .

**表 3. Fault Types (continued)**

Fault Name	Fault	$\overline{FLT}$	Description
PP5V_RCP	PP5V Reverse-Current Protection	Low	If a SRC state is selected to be entered or device currently is in a SRC state (SRC 1.5 A or SRC 3 A) and a reverse-current condition is detected, the PP5V path is disabled automatically and the $\overline{FLT}$ pin will be asserted. If the reverse-current condition is removed, the PP5V path will automatically re-enable.
VBUS_UVLO	VBUS undervoltage Lockout	Hi-Z	If VBUS supply is below the VBUS UVLO threshold, the PPHV path is disabled automatically if enabled or remains disabled. If the SNK state is selected to be entered, the device will remain in the DISABLED state until the UVLO event is removed. If the SNK state has been entered successfully and a UVLO event occurs, the PPHV path is disabled automatically.
VBUS_OVP <sup>(1)</sup>	VBUS overvoltage Protection	Low	If the SNK state is selected to be entered or device currently is in the SNK state and the VBUS supply rises above the VBUS OVP threshold, the PPHV path is disabled automatically and the $\overline{FLT}$ pin will be asserted.
VBUS_RCP	VBUS Reverse-Current Protection	Hi-Z	If the SNK state is selected to be entered or device currently is in the SNK state and a reverse-current condition is detected, the PPHV path is disabled automatically, but the $\overline{FLT}$ is not asserted.. If the reverse-current condition is removed, the PPHV path will automatically re-enable.
PPHV_OVT	PPHV overtemperature Protection	Low	If the SNK state is selected to be entered or device currently is in the SNK state and the local temperature of PPHV power path exceeds TSD_PPHV_R, the PPHV path is disabled automatically and the $\overline{FLT}$ pin will be asserted. PPHV power path will remain disabled until temperature falls below TSD_PPHV_F.

(1) OVP terminal is not connected to GND.

## 9 Application and Implementation

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The typical applications of the TPS6602x include chargers, notebooks, tablets, ultra-books, dongles and any other product supporting USB Type-C and/or USB-PD as a power source or power sink. The typical applications outlined in the following sections detail a Fully-Featured USB Type-C using a single 5-V supply and another using a separate 3.3-V supply.

### 9.2 Typical Application

图 28 shows a USB Type-C single port design using a Power Delivery (PD) controller that supports 5-V operation. For this system, a single 5-V supply is used to supply power to the PP5V and VIN supplies of the TPS66021, as well as, the connector power, VCONN. The TPS66021 supplies power to the 5-V supply of the PD controller via its VLDO output which is sourced either from the integrated 5-V VBUS LDO for dead battery operation or from VIN once the dead battery condition ends.

Similarly, 图 29 shows a USB Type-C single port design using a PD controller that only supports 3.3-V operation. In this case, a separate 3.3-V supply in the system is used to supply power to the TPS66020. The TPS66020 supplies power to the 3.3-V supply of the PD controller via its VLDO output which is sourced either from the integrated 3.3-V VBUS LDO for dead battery operation or from VIN once the dead battery condition ends.

The PP5V integrated power path is used to provide 5-V VBUS power when the device is enabled as Source. The PPHV integrated power path provides power to the system and battery charger from VBUS when the device is enabled as a Sink.

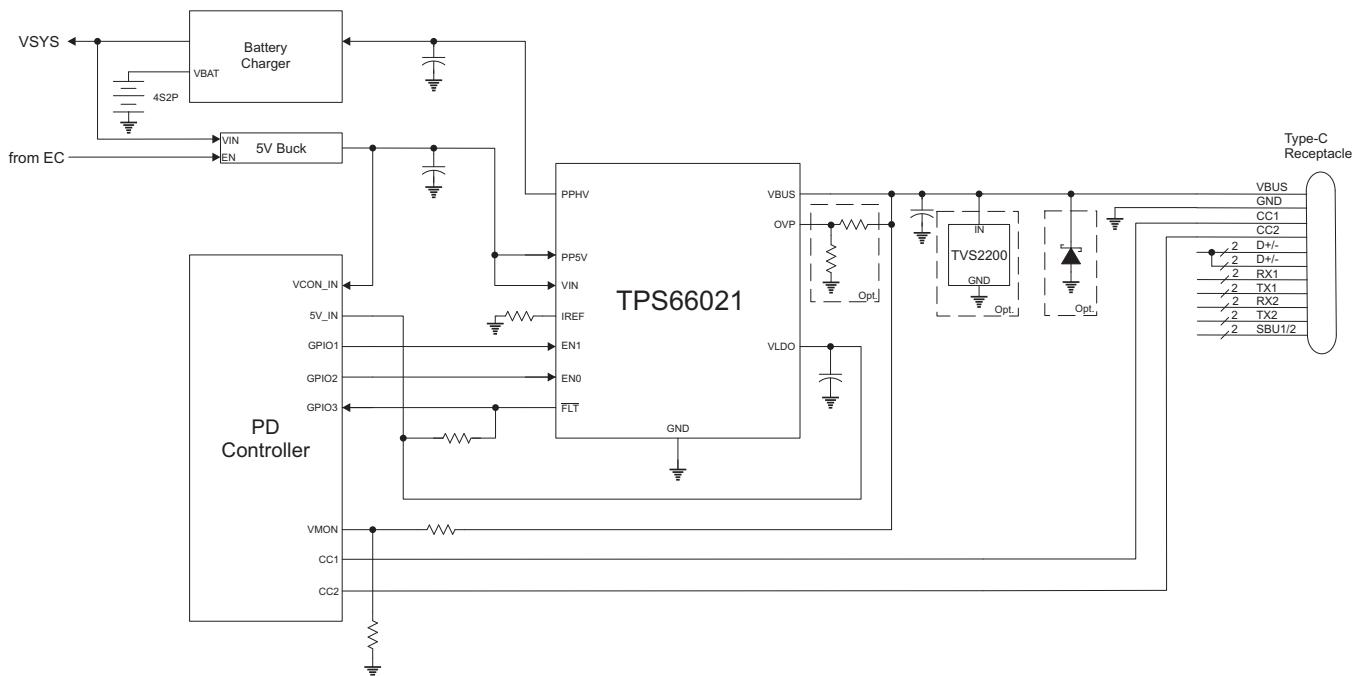


图 28. Single Port Type-C PD Port Using a Single 5-V Supply

## Typical Application (continued)

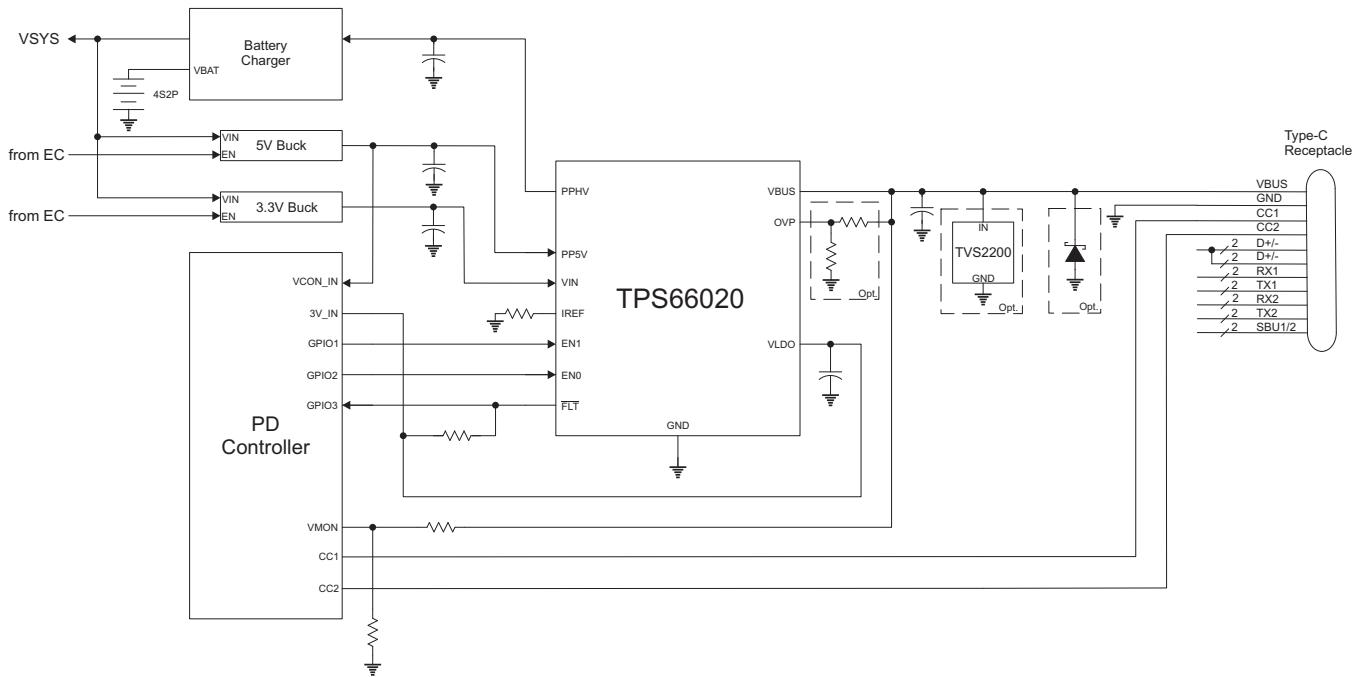


图 29. Single Port Type-C PD Port Using a 3.3-V Supply

### 9.2.1 Design Requirements

For a single port notebook application, 表 4 lists the input voltage requirements and expected current capabilities.

表 4. Single-Port Notebook Application Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE(S)	POWER PATH DIRECTION
PP5V Input Voltage and Current Capabilities	5V/3A	Source from PP5V to VBUS
VCONN_IN Input Voltage and Current Capabilities	5V/300mA (1.5W)	Source to VCONN
VBUS Input Voltage and Current Capabilities	5V/3A, 9V/3A, 15V/3A, 20V/3A	Sink from VBUS to PPHV
5V_IN Input Voltage and Current Capabilities	4.5-5.5V/30mA	5-V PD Controller Supply
3V_IN Input Voltage and Current Capabilities	3.0-3.6V/30mA	3.3-V PD Controller Supply

### 9.2.2 Detailed Design Procedure

#### 9.2.2.1 External Current Reference Resistor ( $R_{IREF}$ )

A 75-k $\Omega$  resistor is required from the TPS6602x IREF terminal to ground.  $R_{IREF}$  is used to set the proper reference current required to meet the min/max current limit specifications in the datasheet of the PP5V power path. An overall resistance tolerance of +/- 1% is required to meet the datasheet specifications which includes aging, temperature, and resistance variation. A +/- 0.5% resistor is recommended. Care should be taken to ensure the ground return of  $R_{IREF}$  is in close proximity to the GND terminal of the TPS6602x to minimize error in the current limit setting due to voltage drops that may occur across the ground supply.

### 9.2.2.2 External VLDO Capacitor (CVLDO)

For all capacitances, the DC operating voltage must be factored into the derating of ceramic capacitors. Generally, the effective capacitance is 35-50% of the nominal capacitance with voltage applied. Assuming VLDO = 5 V, and a minimum derated capacitance of 2.5 uF, a 10-V rated 4.7-uF capacitor is sufficient.

### 9.2.2.3 PP5V Power Path Capacitance

For most systems, the PP5V terminal is supplied by a DC-DC converter. Typically, the capacitance placed on the output of the DC-DC converter is significant in order to handle current load steps. This capacitance value will be dependent on the DC-DC converter selected. A ceramic 10 uF (X7R/X5R) 10-V rated capacitor coupled with a 0.1-uF high frequency capacitor placed, is placed as close as possible to the PP5V terminal of the TPS6602x. This is in addition to the DC-DC converter required capacitance should be sufficient, but may need to be adjusted based on the specific application.

It should be noted that in many Type-C/PD systems, the VCONN supply is shared with the PP5V path. Therefore, in these systems, the application must budget the power requirements of the DC-DC converter for the VCONN and PP5V paths combined. For this example, a minimum of 5 V at 3.3 A is required to meet the defined system specifications.

### 9.2.2.4 PPHV, VBUS Power Path Capacitance

The PPHV power path is a Sink. The capacitance on the PPHV shown in [Figure 29](#) represents capacitance of the charger sub-system. In a typical application, this capacitance can be in the range of 47 uF up to 100 uF, far exceeding the 1-uF minimum specification for the TPS6602x, so no external capacitance is required to meet this requirement in most cases. As per the PD Specification, the total capacitance on VBUS should be maximum 10 uF at connection.

The TPS6602x PPHV power path has soft start circuitry to control in-rush current when the PPHV power path is enabled. DC loading should be minimized during soft start since the PPHV path may experience high power dissipation especially at higher VBUS voltages. This in turn may lead to a PPHV overtemperature protection event.

### 9.2.2.5 VBUS TVS Protection (Optional)

It is recommended that each VBUS port in the system have TVS protection to protect the VBUS terminal. Inductive ringing during momentary disconnects and reconnects due to mechanical vibration or plug removal while sinking large current loads may cause large peak voltages to be present on the VBUS terminal that may exceed the absolute maximums of the TPS6602x. Under such events, the TVS2200 clamps the VBUS terminal and prevents VBUS from exceeding the maximum specification. The TVS trip point should be chosen to be safely above the normal operating ranges of the device. For this case, it is assumed VBUS voltage contracts are less than 22-V maximum which is below the minimum breakdown voltage of the TVS2200. The maximum clamping voltage of 28.3 V of the TVS2200 is sufficient to protect the VBUS terminal of the TPS6602x.

### 9.2.2.6 VBUS Schottky Diode Protection (Optional)

To prevent the possibility of large ground currents into the TPS6602x during sudden disconnects because of inductive effects in a cable, it is recommended that a Schottky diode be placed from VBUS to GND. The NSR20F30NXT5G or comparable device is recommended.

### 9.2.2.7 VBUS Overvoltage Protection (Optional)

VBUS Overvoltage Protection (OVP) is optional. If VBUS OVP is not required, then the OVP terminal should be tied to ground as shown in [Figure 12](#). VBUS OVP is used to detect voltages on VBUS that exceed a set threshold. Upon detection, the PPHV power path is disabled quickly to help protect components connected downstream of the PPHV terminal. It should be noted that VBUS OVP is not a replacement for VBUS TVS protection which is protecting the VBUS terminal itself.

The VBUS OVP threshold is set by a resistor divider from the VBUS terminal to ground as shown in [Figure 11](#). For this design, R1 and R2 are fixed values to provide VBUS OVP protection at the highest voltage contract level. Using R1 = 432-kΩ and R2 = 20-kΩ sets a nominal VBUS OVP threshold of 22.6 V. For some applications, it may be desirable to dynamically change the VBUS OVP level based on the negotiated power contract. One possible way is shown in [Figure 13](#). In this case, the PD controller via GPIO, selects the proper divider ratio to set the VBUS OVP threshold based on the negotiated voltage contract level.

### 9.2.2.8 Dead Battery Support

The TPS6602x integrates a high-voltage VBUS LDO that can be used to supply power to a PD Controller and other supporting circuitry when only VBUS power is available, such as in a dead battery condition. As shown in [图 29](#), the TPS66020 VLDO output supplies power to the PD Controller's 3V\_IN supply. Similarly, [图 28](#) shows the TPS66021 VLDO output supplies power to the PD Controller's 5V\_IN supply. During a dead battery condition, the PD Controller presents its Type-C RPD pull-downs on the CC1 and CC2 lines. Upon connection to a Type-C/PD Source, 5 V is provided to VBUS from the Source partner which powers the TPS6602x. The VBUS LDO is enabled and provides power to the PD Controller. Once powered, the PD Controller can decide to enable the TPS6602x PPHV Sink path by asserting EN0 high and use the 5-V VBUS to charge the battery or it may choose to negotiate a higher voltage contract first. Either way, once the contract is negotiated, the PD Controller will enable the PPHV Sink path and charge the system. Once the system is sufficiently charged, the VIN terminal will rise and will exceed the VIN UVLO threshold. If VIN remains above the UVLO threshold for  $t_{VIN\_STABLE}$ , VLDO will be supplied from VIN and the VBUS LDO will be disabled.

### 9.2.2.9 Fast Role Swap (FRS) (Optional)

The TPS6602x supports Fast Role Swap operation as in the new Source, old Sink scenario shown in [图 24](#). The PPHV power path represents the old Sink and the PP5V power path represents the new Source. During FRS, the PP5V power path of the TPS6602x has a much faster turn-on compared to normal operation, for example entering SRC 1P5A or SRC 3P0A states from the DISABLED state. This faster turn-on is required in order to meet the USB PD fast role swap timing requirements ( $t_{SrcFRSwap}$ ) for the new Source.

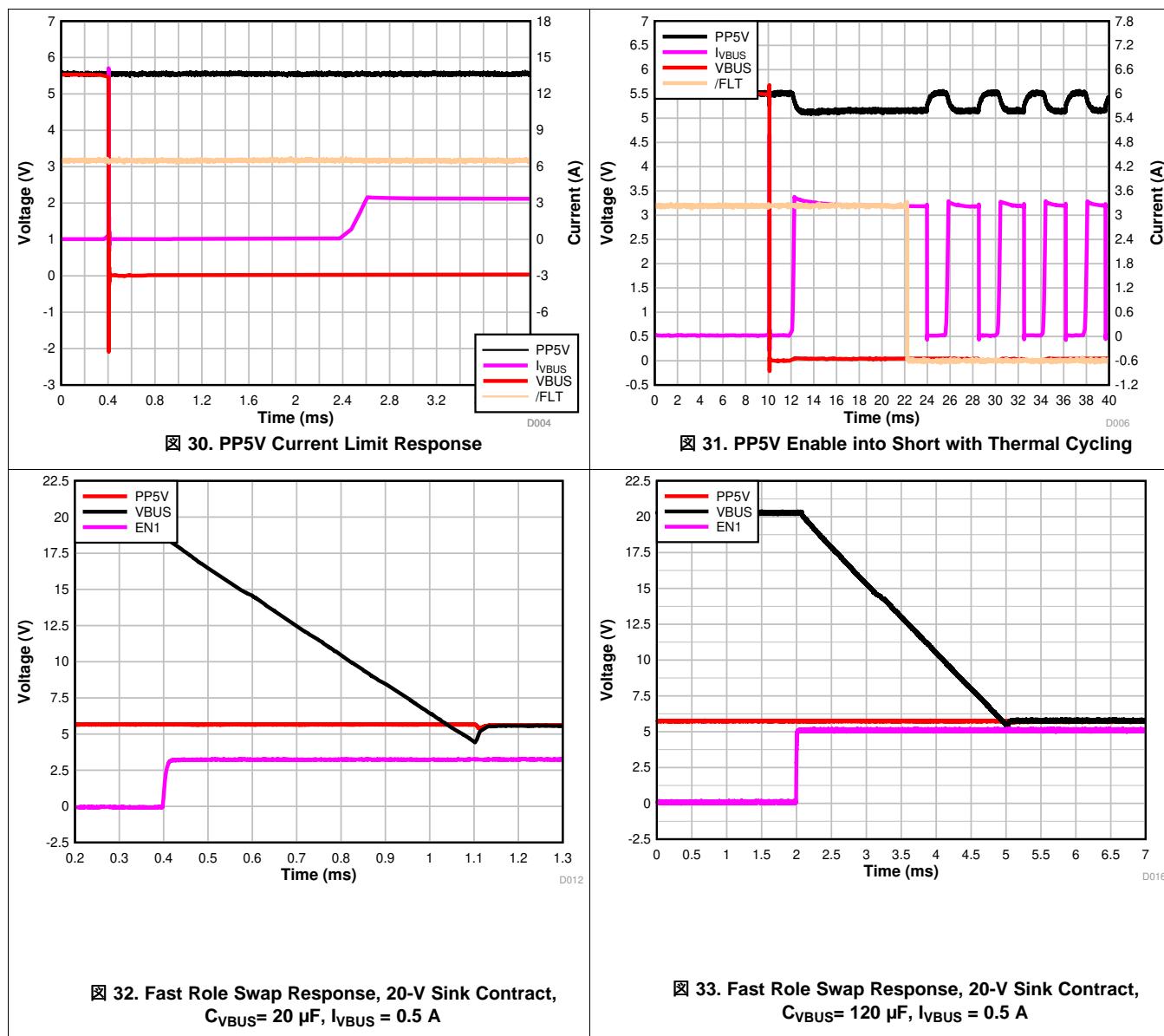
To enable FRS, the TPS6602x must first be operating as a Sink (SNK state). The TPS6602x must then transition to the FRS state by asserting EN1 high. EN1 is asserted high by the PD Controller as soon as possible once it has properly detected FRS signaling from its port partner on its CC line. The FRS signaling from the port partner to the PD Controller indicates that the port partner has lost its power and requires a fast role swap sequence to be performed.

It should be noted that the timing of when EN1 is asserted high relative to the port partner losing power is highly application, and implementation dependent. Some of these dependencies include:

- Loss of power detection accuracy, margin and propagation delay of the port partner.
- Timing from loss of power detection to FRS signaling transmitted on the CC line.
- Detection by the PD Controller of the FRS signaling received on its CC line.
- Assertion of a GPIO from the PD Controller after detection of the FRS signaling.

In systems that require good FRS performance, these should be optimized to minimize unnecessary delays from significantly impacting the turn-on of the new Source. Once the FRS state is entered, the TPS6602x will automatically handle the power role swap from Sink to Source as shown in [图 25](#). In most applications, there is significant charge being stored in reserve while power is being provided. Upon loss of power, this charge is then used to supply power to the application until the FRS completes. As this charge depletes, the voltage on VBUS will decay at some rate based on the current load and the amount of charge that has been stored. USB PD requires that the new Source only be enabled once VBUS is detected below vSafe5V (maximum). Therefore, the amount of voltage that VBUS drops below vSafe5V will depend heavily on the amount of remaining charge and what current load is on VBUS, along with how fast the PP5V power path can enable. It should be noted that the PD Specification allows VBUS to be discharged completely to ground and is shown in [图 32](#) typical response curve.

### 9.2.3 Application Curves



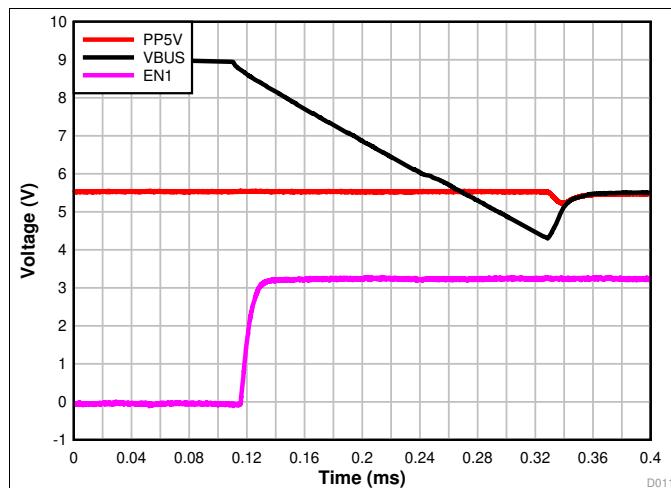


図 34. Fast Role Swap Response, 9-V Sink Contract,  
 $C_{VBUS} = 20 \mu\text{F}$ ,  $I_{VBUS} = 0.5 \text{ A}$

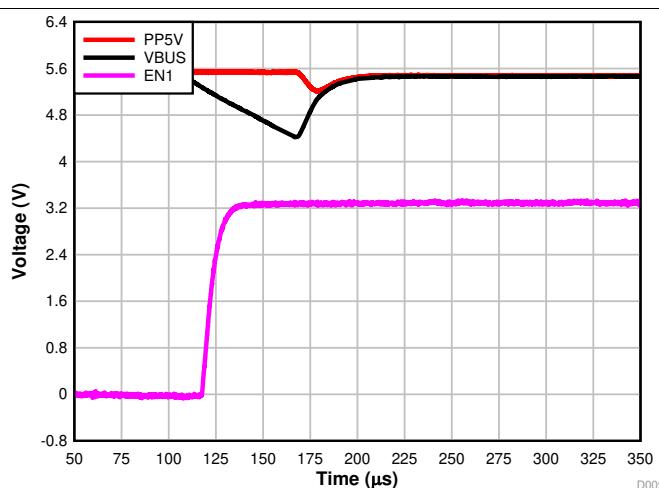


図 35. Fast Role Swap Response, 5-V Sink Contract,  
 $C_{VBUS} = 20 \mu\text{F}$ ,  $I_{VBUS} = 0.5 \text{ A}$

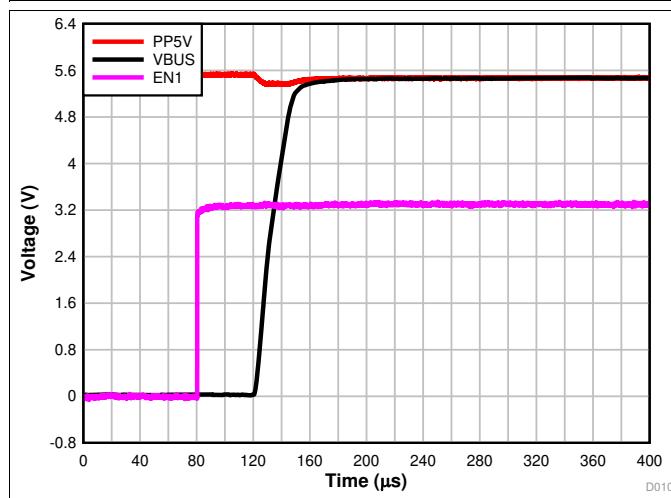


図 36. Fast Role Swap Response, 5-V Sink Contract, VBUS  
Fully Discharged,  $C_{VBUS} = 20 \mu\text{F}$ ,  $I_{VBUS} = 0.5 \text{ A}$

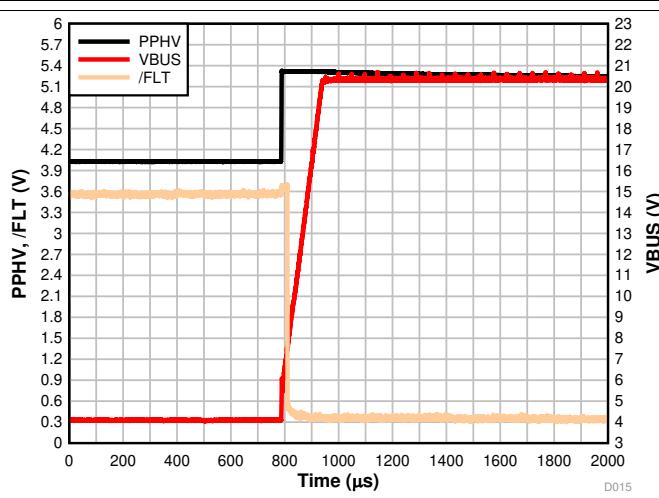


図 37. VBUS OVP Response with 6-V Threshold

## 10 Power Supply Recommendations

The device has a single input supply, VIN. VIN may be shared with PP5V when using the TPS66021 device. When shared with PP5V, the capacitance required on PP5V is sufficient for the VIN supply. When VIN is not shared, a 1- $\mu\text{F}$  or higher ceramic bypass capacitor between VIN and GND is recommended as close to the VIN as possible for local noise decoupling.

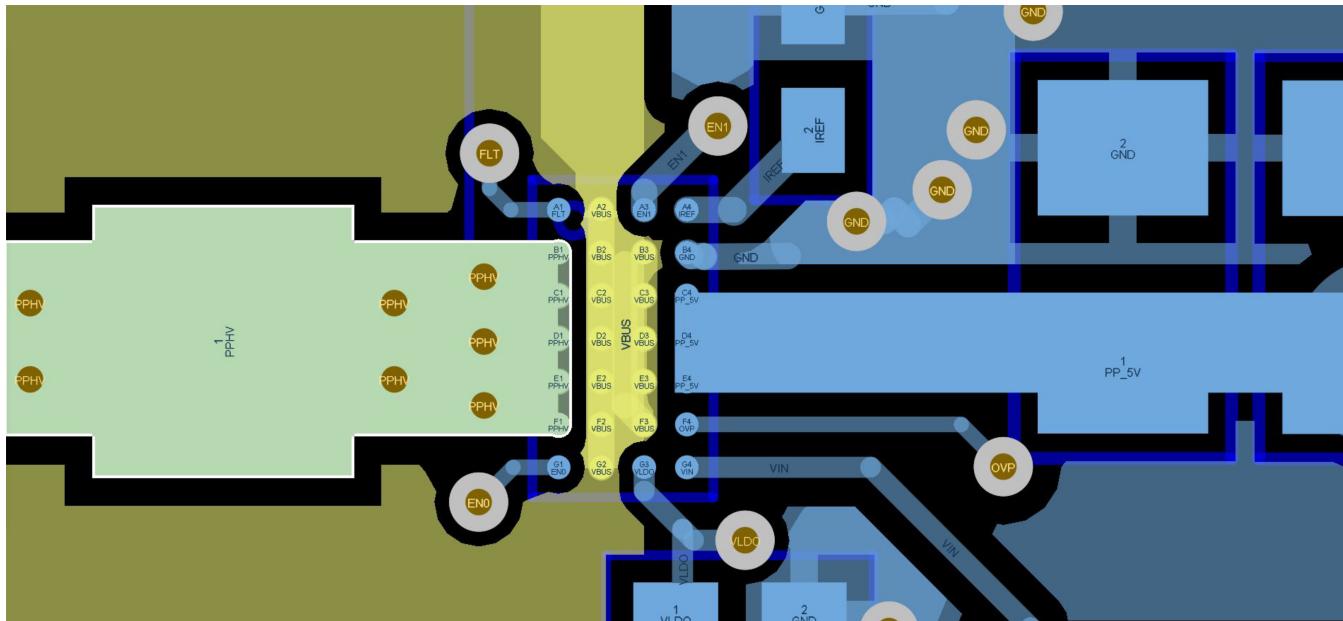
USB Specification Revisions 2.0 and 3.1 require VBUS voltage at the connector to be between 4.75 V to 5.5 V. Depending on layout and routing from supply to the connector the voltage droop on VBUS has to be tightly controlled. Locate the input supply close to the device. For all applications, a maximum 10- $\mu\text{F}$  ceramic bypass capacitor between VBUS and GND is recommended as close to the Type-C connector of the device as possible for local noise decoupling. The input power supply should be rated higher than the current limit set to avoid voltage drops during overcurrent and short-circuit conditions.

## 11 Layout

## 11.1 Layout Guidelines

1. PP5V, PPHV, and VBUS traces must be as short and wide as possible to accommodate for high currents.
2. A ceramic 10  $\mu$ F (X7R/X5R) 10-V rated capacitor coupled with a 0.1- $\mu$ F high frequency capacitor placed, is placed as close as possible to the PP5V terminal of the TPS6602x.
3. Care should be taken to ensure the ground return of  $R_{IREF}$  is in close proximity to the GND terminal of the TPS6602x to minimize error in the current limit setting due to voltage drops that may occur across the ground supply.
4. A ceramic 4.7  $\mu$ F (X7R/X5R) 10-V rated capacitor is placed as close as possible to the VLDO terminal of the TPS6602x.

## 11.2 Layout Example



## 图 38. Layout Example

## 12 デバイスおよびドキュメントのサポート

### 12.1 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびご注文へのクイック・アクセスが含まれます。

表 5. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
TPS66020	<a href="#">ここをクリック</a>				
TPS66021	<a href="#">ここをクリック</a>				

### 12.2 ドキュメントの更新通知を受け取る方法

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### 12.3 サポート・リソース

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### 12.6 Glossary

#### SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

## 13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあります。ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTPS66020A0YBGR.B	Active	Preproduction	DSBGA (YBG)   28	3000   LARGE T&R	-	Call TI	Call TI	-10 to 85	
PTPS66021A0YBGR.B	Active	Preproduction	DSBGA (YBG)   28	3000   LARGE T&R	-	Call TI	Call TI	-10 to 85	
<a href="#">TPS66020YBGR</a>	Active	Production	DSBGA (YBG)   28	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-10 to 85	TPS66020
TPS66020YBGR.A	Active	Production	DSBGA (YBG)   28	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-10 to 85	TPS66020
TPS66020YBGR.B	Active	Production	DSBGA (YBG)   28	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-10 to 85	TPS66020
<a href="#">TPS66021YBGR</a>	Active	Production	DSBGA (YBG)   28	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-10 to 85	TPS66021
TPS66021YBGR.A	Active	Production	DSBGA (YBG)   28	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-10 to 85	TPS66021
TPS66021YBGR.B	Active	Production	DSBGA (YBG)   28	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-10 to 85	TPS66021

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

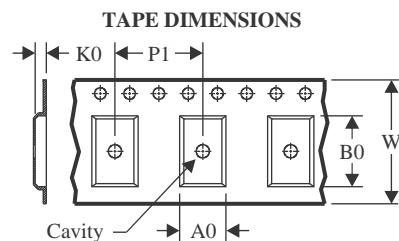
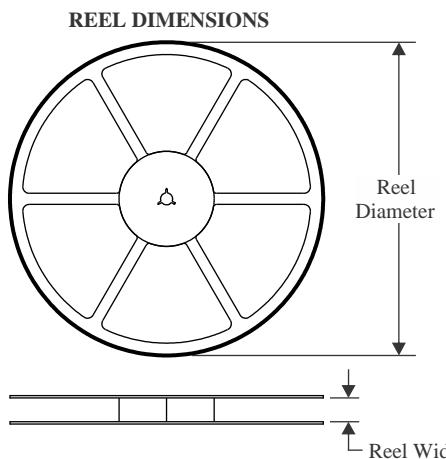
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

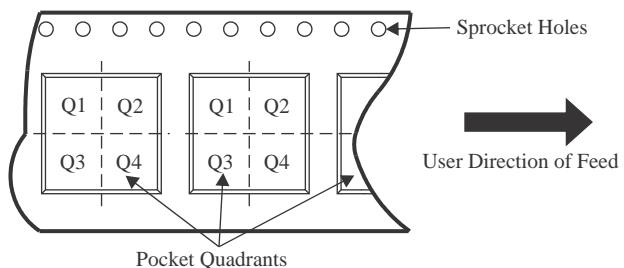
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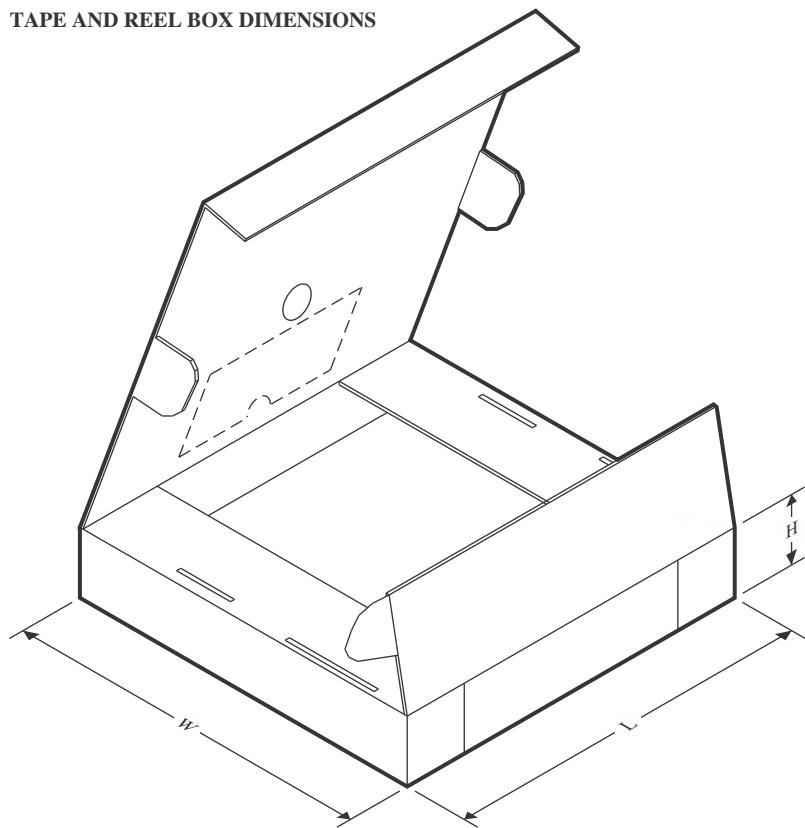
**TAPE AND REEL INFORMATION**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS66020YBGR	DSBGA	YBG	28	3000	330.0	12.4	1.78	2.98	0.7	4.0	12.0	Q1
TPS66020YBGR	DSBGA	YBG	28	3000	330.0	12.4	1.78	2.98	0.6	4.0	12.0	Q1
TPS66021YBGR	DSBGA	YBG	28	3000	330.0	12.4	1.78	2.98	0.6	4.0	12.0	Q1
TPS66021YBGR	DSBGA	YBG	28	3000	330.0	12.4	1.78	2.98	0.7	4.0	12.0	Q1

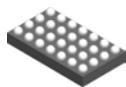
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS66020YBGR	DSBGA	YBG	28	3000	367.0	367.0	35.0
TPS66020YBGR	DSBGA	YBG	28	3000	335.0	335.0	25.0
TPS66021YBGR	DSBGA	YBG	28	3000	335.0	335.0	25.0
TPS66021YBGR	DSBGA	YBG	28	3000	367.0	367.0	35.0

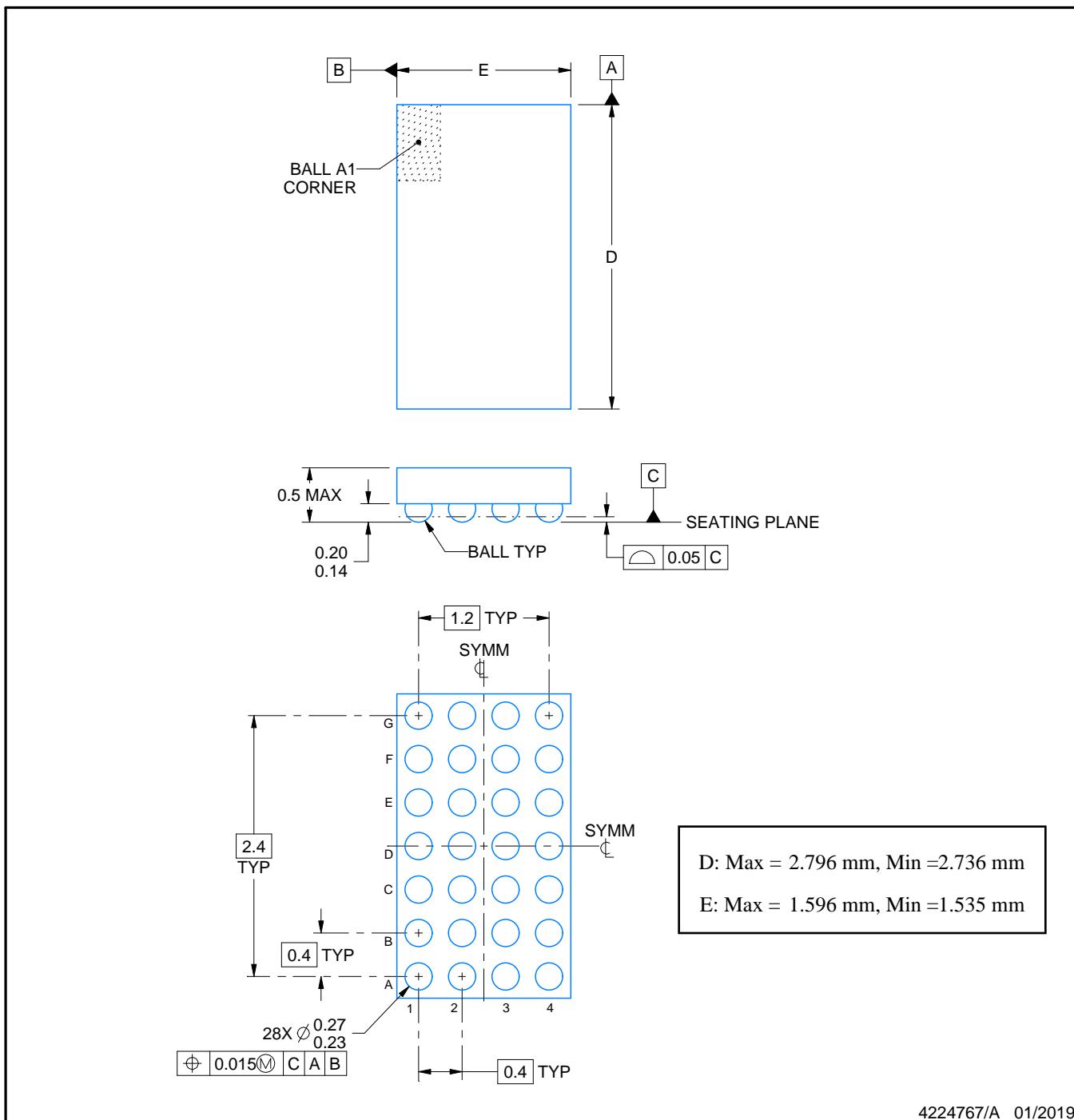
# PACKAGE OUTLINE

YBG0028



DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4224767/A 01/2019

## NOTES:

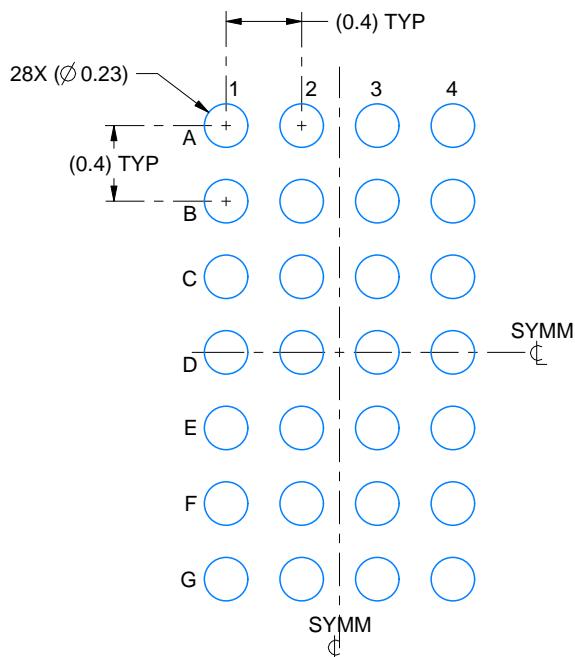
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

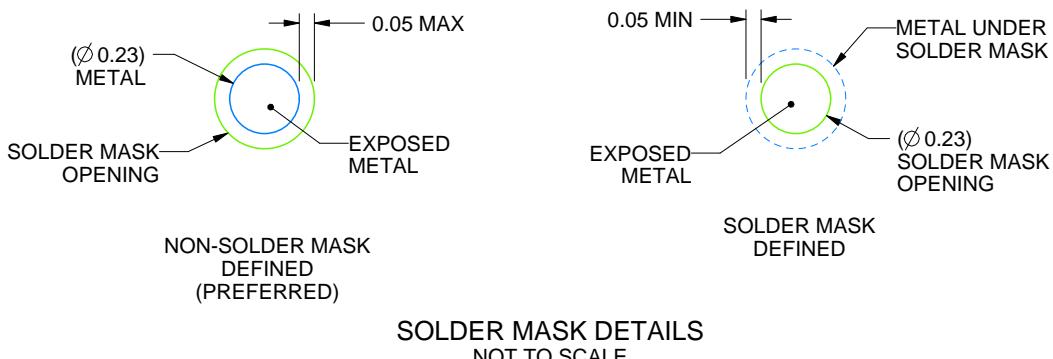
YBG0028

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 25X



4224767/A 01/2019

NOTES: (continued)

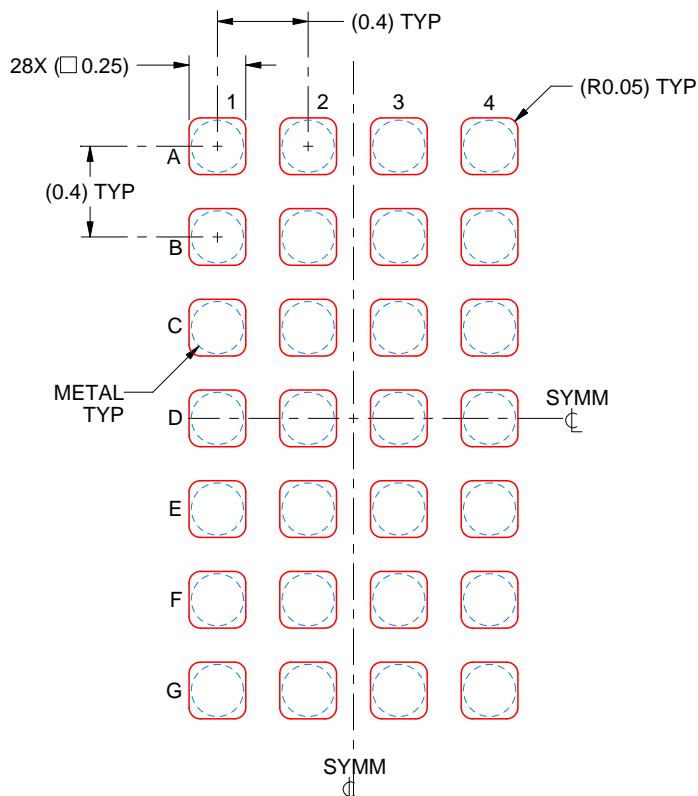
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.  
See Texas Instruments Literature No. SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

## EXAMPLE STENCIL DESIGN

YBG0028

## DSBGA - 0.5 mm max height

## DIE SIZE BALL GRID ARRAY



**SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE: 30X**

4224767/A 01/2019

#### NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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最終更新日：2025 年 10 月