



DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATORS

FEATURES

- Dual Output Voltages for Split-Supply Applications
- Output Current Range of 0mA to 1.0A per Regulator
- 3.3V/2.5V, 3.3V/1.8V, and 3.3V/Adjustable Output
- Fast-Transient Response
- 2% Tolerance Over Load and Temperature
- Dropout Voltage Typically 350mV at 1A
- Ultra-low 85 μ A Typical Quiescent Current
- 1 μ A Quiescent Current During Shutdown
- Dual Open-Drain Power-On Reset with 200ms Delay for Each Regulator
- 28-Pin PowerPAD™ TSSOP Package
- Thermal Shutdown Protection for Each Regulator

DESCRIPTION

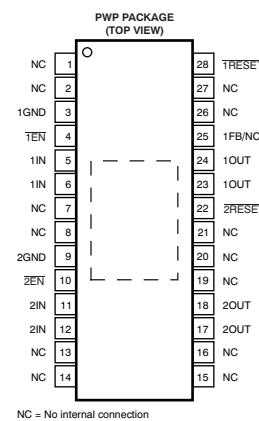
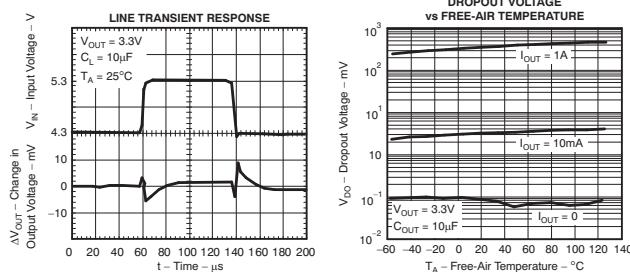
The TPS767D3xx family of dual voltage regulators offers fast transient response, low dropout voltages and dual outputs in a compact package and incorporating stability with 10 μ F low ESR output capacitors.

The TPS767D3xx family of dual voltage regulators is designed primarily for DSP applications. These devices can be used in any mixed-output voltage application, with each regulator supporting up to 1A. Dual active-low reset signals allow resetting of core-logic and I/O separately.

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (350mV typically at an output current of 1A for the TPS767D325) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (typically 85 μ A over the full range of output current, 0mA to 1A). These two key specifications yield a significant improvement in operating life for battery-powered systems. This LDO family also features a sleep mode; applying a TTL high signal to EN (enable) shuts down the regulator, reducing the quiescent current to 1 μ A at $T_J = +25^\circ\text{C}$.

The **RESET** output of the TPS767D3xx initiates a reset in microcomputer and microprocessor systems in the event of an undervoltage condition. An internal comparator in the TPS767D3xx monitors the output voltage of the regulator to detect an undervoltage condition on the regulated output voltage.

The TPS767D3xx is offered in 1.8V, 2.5V, and 3.3V fixed-voltage versions and in an adjustable version (programmable over the range of 1.5V to 5.5V). Output voltage tolerance is specified as a maximum of 2% over line, load, and temperature ranges. The TPS767D3xx family is available in a 28-pin PWP TSSOP package. They operate over a junction temperature range of -40°C to $+125^\circ\text{C}$.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

AVAILABLE OPTIONS⁽¹⁾

DEVICE	REGULATOR 1 V _{OUT} (V)	REGULATOR 2 V _{OUT} (V)
TPS767D301	Adjustable (1.5V – 5.5V)	3.3V
TPS767D318	1.8V	3.3V
TPS767D325	2.5V	3.3V

(1) For the most current specifications and package information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Over operating temperature range (unless otherwise noted).

	TPS767D3xx	UNIT
Input voltage range, V _{1IN} , V _{2IN} ⁽²⁾	–0.3 to +13.5	V
Enable voltage range, V _{1EN} , V _{2EN}	–0.3 to V _{IN} + 0.3	V
Output voltage range, V _{1OUT} , V _{2OUT}	–0.3 to +7.0	V
RESET voltage range, V _{1RESET} , V _{2RESET}	–0.3 to +16.5	V
Peak output current	Internally limited	
ESD rating, HBM	2	kV
Continuous total power dissipation	See Dissipation Ratings table	
Operating junction temperature range, T _J	–40 to +125	°C
Storage temperature range, T _{stg}	–65 to +150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network terminal ground.

POWER DISSIPATION RATINGS

PACKAGE	AIR FLOW (CFM)	T _A ≤ +25°C POWER RATING	DERATING FACTOR ABOVE t _a = +25°C	T _A = +70°C POWER RATING	T _A = +85°C POWER RATING
PWP ⁽¹⁾	0	3.58 W	35.8 mW/°C	1.97 W	1.43 W
	250	5.07 W	50.7 mW/°C	2.79 W	2.03 W

(1) This parameter is measured with the recommended copper heat sink pattern on a 4-layer PCB, 1oz. copper on 4-in × 4-in ground layer. For more information, refer to TI technical brief literature number [SLMA002](#).

ELECTRICAL CHARACTERISTICS

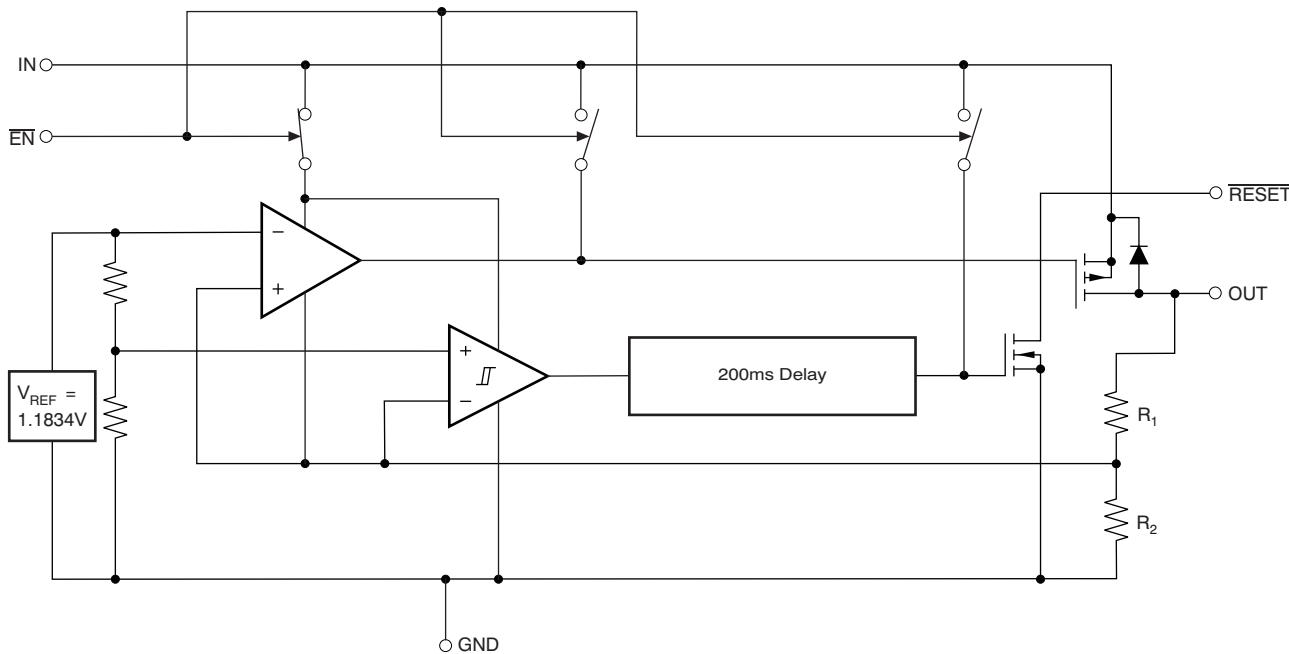
Over operating temperature range ($T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$), $V_{\text{IN}} = V_{\text{OUT}(\text{nom})} + 1\text{V}$, $I_{\text{OUT}} = 1\text{mA}$, $V_{\text{EN}} = 0\text{V}$, and $C_{\text{OUT}} = 10\mu\text{F}$, unless otherwise noted. Adjustable channels are set to $V_{\text{OUT}} = 3.3\text{V}$. Typical values are at $T_J = 25^\circ\text{C}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range, $V_{1\text{IN}}$, $V_{2\text{IN}}^{(1)}$		2.7	10		V
V_{OUT}	Adjustable V_{OUT} range, $V_{1\text{OUT}}$, $V_{2\text{OUT}}$		1.5	5.5		V
	Accuracy, adjustable V_{OUT} channels ⁽¹⁾	$V_{\text{OUT}} + 1\text{V} \leq V_{\text{IN}} \leq 5.5\text{V}$ $10\mu\text{A} \leq I_{\text{OUT}} \leq 1\text{A}$	-2.0	+2.0		%
	Accuracy, fixed V_{OUT} channels ⁽¹⁾	$V_{\text{OUT}} + 1\text{V} \leq V_{\text{IN}} \leq 10\text{V}$ $10\mu\text{A} \leq I_{\text{OUT}} \leq 1\text{A}$	-2.0	+2.0		%
$\Delta V_{\text{OUT}}\%/\Delta V_{\text{IN}}$	Line regulation ⁽¹⁾	$V_{\text{OUT}} + 1.0\text{V} \leq V_{\text{IN}} \leq 10\text{V}$		0.01		%/V
$\Delta V_{\text{OUT}}\%/\Delta I_{\text{OUT}}$	Load regulation	$10\mu\text{A} \leq I_{\text{OUT}} \leq 1\text{A}$		3		mV
V_{DO}	Dropout voltage ⁽²⁾ ($V_{\text{IN}} = V_{\text{OUT}} \text{ (nom)} - 0.1\text{V}$)	$V_{\text{OUT}} = 3.3\text{V}$, $I_{\text{OUT}} = 1\text{A}$	350	575		mV
I_{CL}	Output current limit, per LDO	$V_{\text{OUT}} = 0\text{V}$, $T_J = +25^\circ\text{C}$	1.7	2		A
I_{GND}	Ground pin current, per LDO	$10\mu\text{A} \leq I_{\text{OUT}} \leq 1\text{A}$	85	125		μA
I_{SHDN}	Standby current, per LDO	$2.7\text{V} \leq V_{\text{IN}} \leq 10\text{V}$, $V_{\text{EN}} = V_{\text{IN}}$	1	10		μA
I_{FB}	FB current input (Adjustable)	$V_{\text{FB}} = 1.5\text{V}$		2		nA
PSRR	Power-supply ripple rejection	$f = 1\text{kHz}$, $C_{\text{OUT}} = 10\mu\text{F}$		60		dB
V_{N}	Output noise voltage	$\text{BW} = 200\text{Hz}$ to 100kHz , $V_{\text{OUT}} = 1.8\text{V}$, $I_{\text{C}} = 1\text{A}$, $C_{\text{OUT}} = 10\mu\text{F}$		55		μV_{RMS}
$V_{\text{EN(HI)}}$	High-level enable input voltage	$T_J = +25^\circ\text{C}$		2.0		V
$V_{\text{EN(LO)}}$	Low-level enable input voltage	$T_J = +25^\circ\text{C}$		0.8		V
I_{EN}	Input current	$V_{\text{EN}} = 0\text{V}$, $T_J = +25^\circ\text{C}$	-1	0	1	μA
		$V_{\text{EN}} = V_{\text{IN}}$, $T_J = +25^\circ\text{C}$	-1		1	
Reset	Minimum input voltage for valid RESET	$I_{\text{OUT(RESET)}} = 300\mu\text{A}$		1.1		V
	Trip threshold voltage	V_{OUT} decreasing, $T_J = +25^\circ\text{C}$	92	98		$\%V_{\text{OUT}}$
	Hysteresis voltage	Measured at V_{OUT}		0.5		$\%V_{\text{OUT}}$
	Output low voltage	$V_1 = 2.7\text{V}$, $T_J = +25^\circ\text{C}$, $I_{\text{OUT(RESET)}} = 1\text{mA}$	0.15	0.4		V
	Leakage current	$V_{(\text{RESET})} = 7\text{V}$, $T_J = +25^\circ\text{C}$		1		μA
	RESET time-out delay	$T_J = +25^\circ\text{C}$	100	200	400	ms
T_{SD}	Thermal shutdown temperature			150		$^\circ\text{C}$
T_J	Operating junction temperature		-40	+125		$^\circ\text{C}$

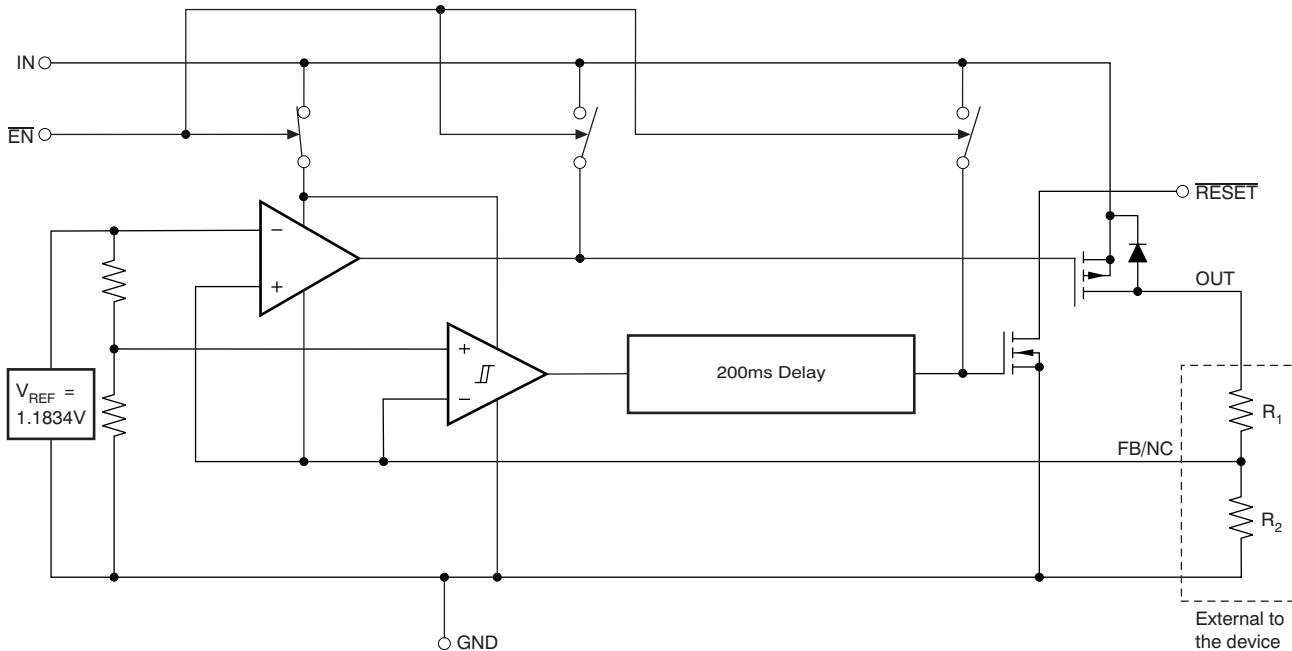
(1) Minimum $V_{\text{IN}} = V_{\text{OUT}} + V_{\text{DO}}$ or 2.7V , whichever is greater.

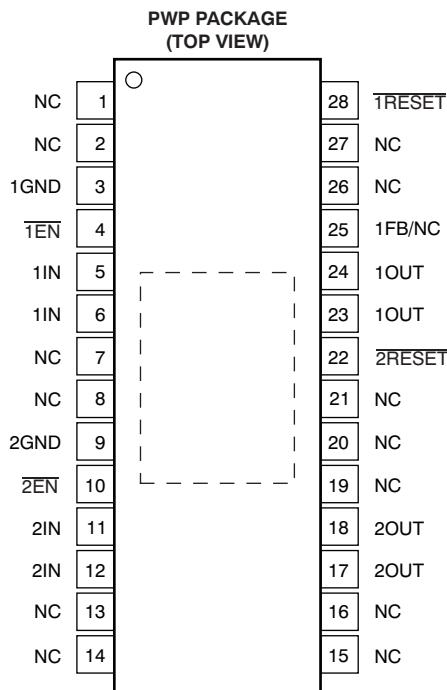
(2) Dropout voltage (V_{DO}) is not measured for channels with $V_{\text{OUT}(\text{nom})} < 2.8\text{V}$ since minimum $V_{\text{IN}} = 2.7\text{V}$.

FUNCTIONAL BLOCK DIAGRAM—Fixed Voltage Version (one regulator channel)



FUNCTIONAL BLOCK DIAGRAM—Adjustable Version (one regulator channel)





NC = No internal connection

TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
1GND	3	Regulator #1 ground
1EN	4	Regulator #1 enable
1IN	5, 6	Regulator #1 input supply voltage
2GND	9	Regulator #2 ground
2EN	10	Regulator #2 enable
2IN	11, 12	Regulator #2 input supply voltage
2OUT	17, 18	Regulator #2 output voltage
2RESET	22	Regulator #2 reset signal
1OUT	23, 24	Regulator #1 output voltage
1FB/NC	25	Regulator #1 output voltage feedback for adjustable output; no connection for fixed output
1RESET	28	Regulator #1 reset signal
NC	1, 2, 7, 8, 13–16, 19, 20, 21, 26, 27	No internal connection

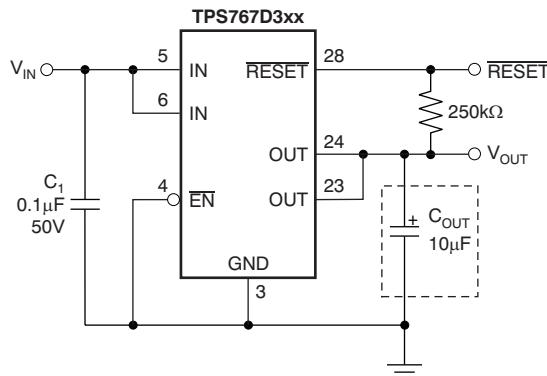
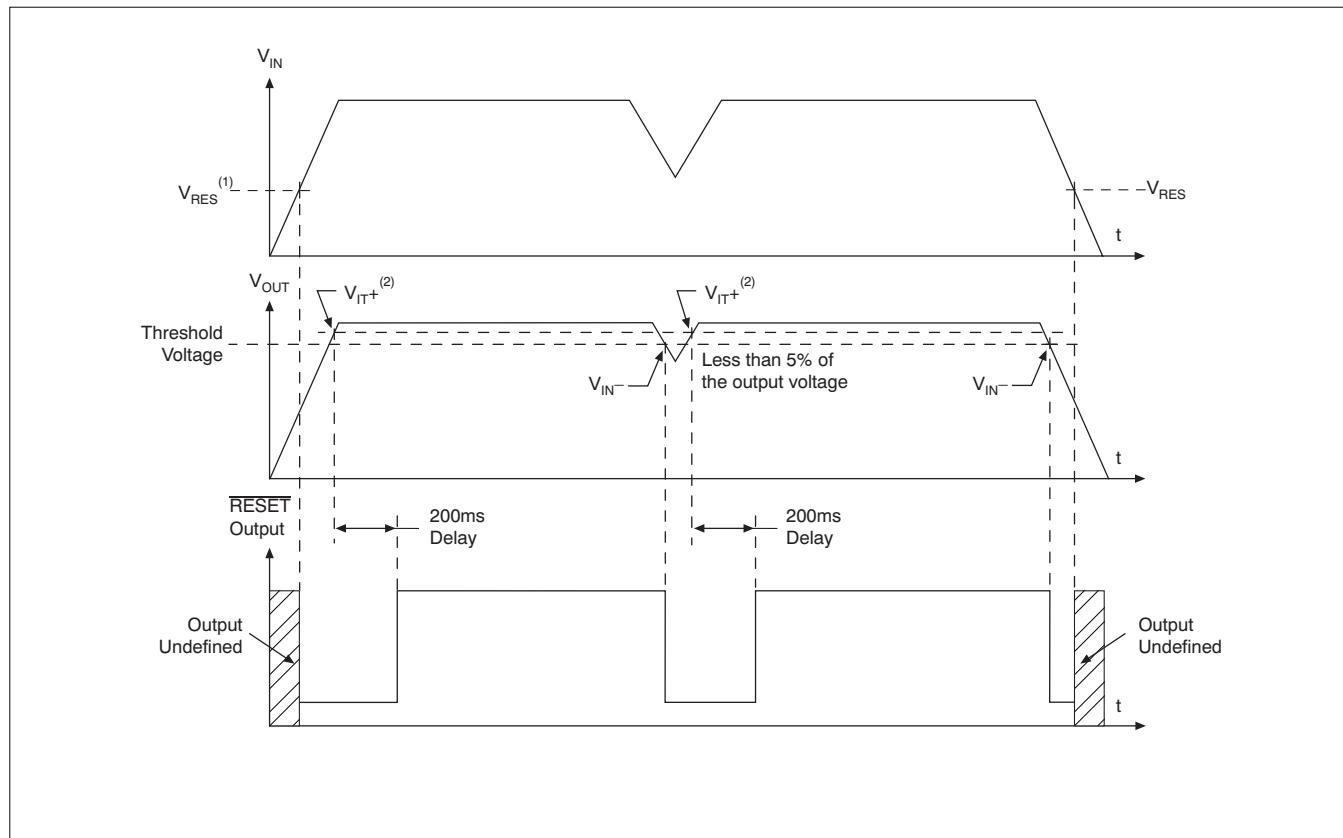


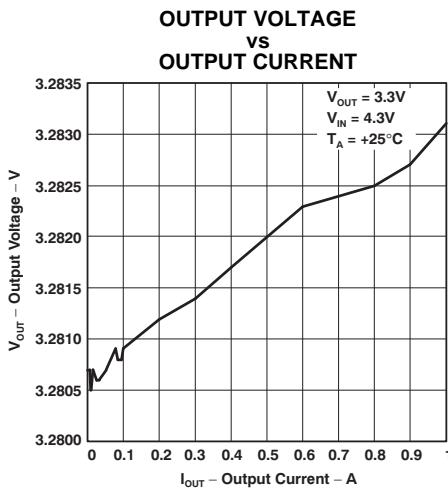
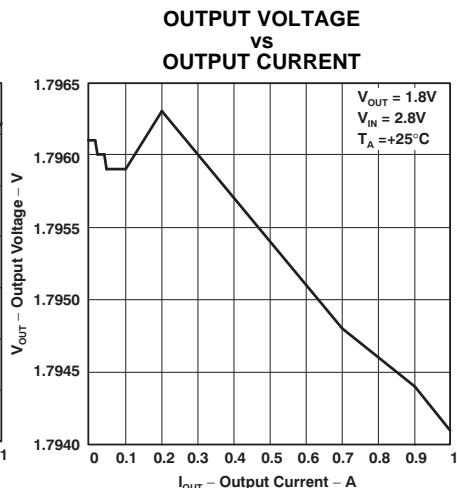
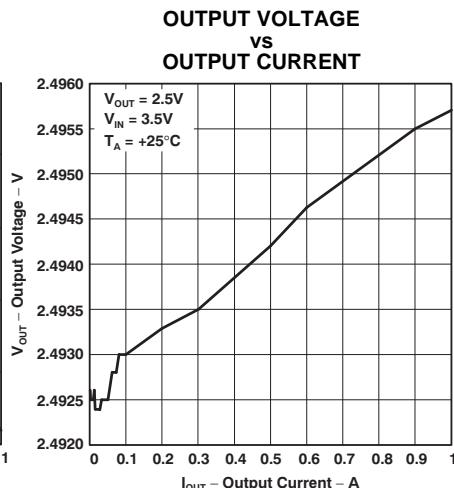
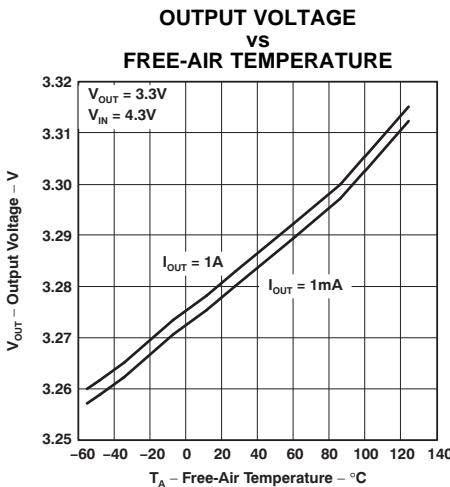
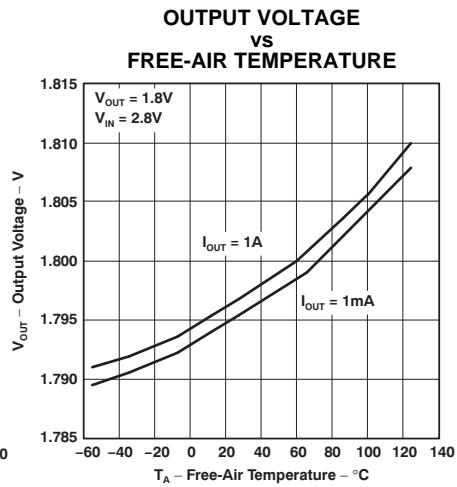
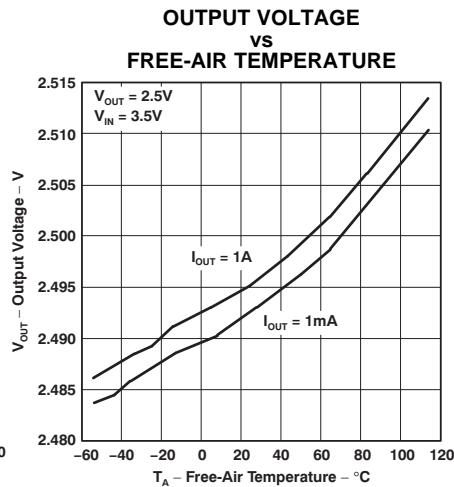
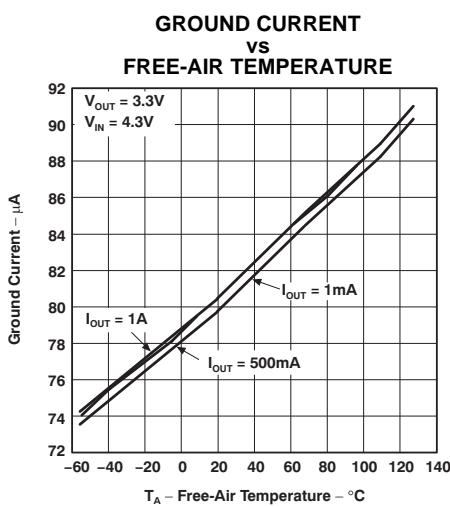
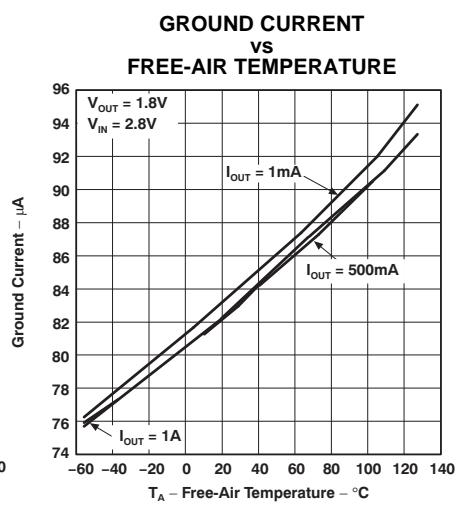
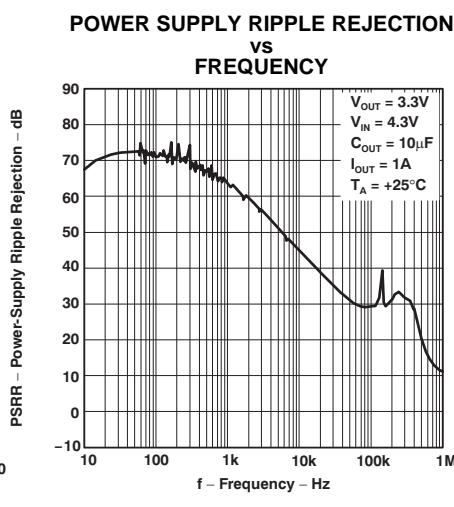
Figure 1. Typical Application Circuit (Fixed Versions) for Single Channel

TIMING DIAGRAM



(1) V_{RES} is the minimum input voltage for a valid \overline{RESET} .

(2) V_{IT+} —Trip voltage is typically 5% lower than the output voltage (95% V_{OUT}).

TYPICAL CHARACTERISTICS

Figure 2.

Figure 3.

Figure 4.

Figure 5.

Figure 6.

Figure 7.

Figure 8.

Figure 9.

Figure 10.

TYPICAL CHARACTERISTICS (continued)

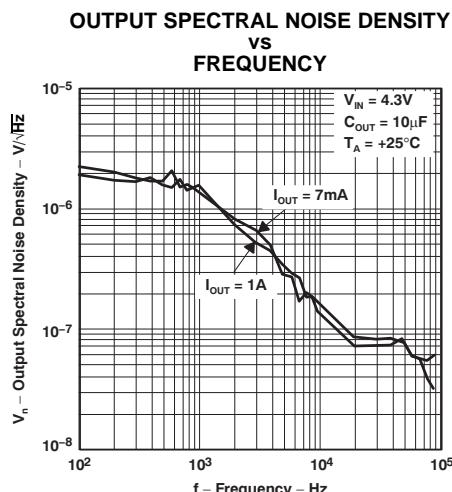


Figure 11.

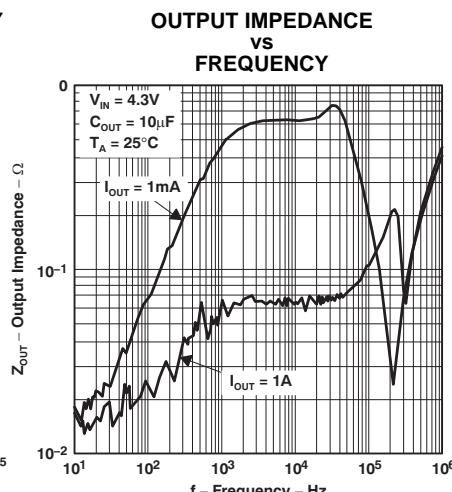


Figure 12.

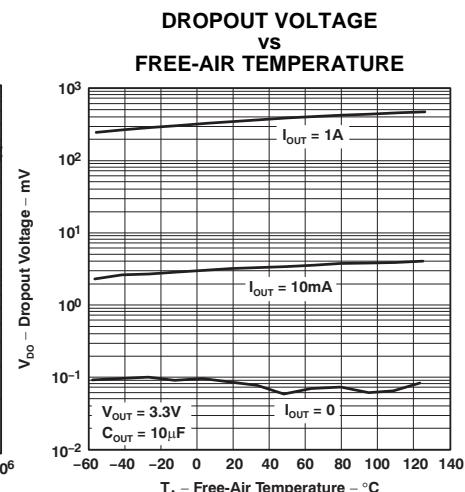


Figure 13.

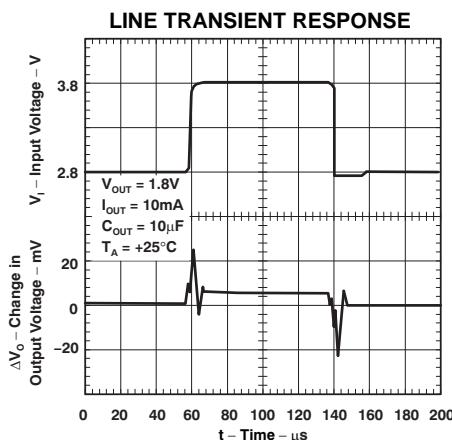


Figure 14.

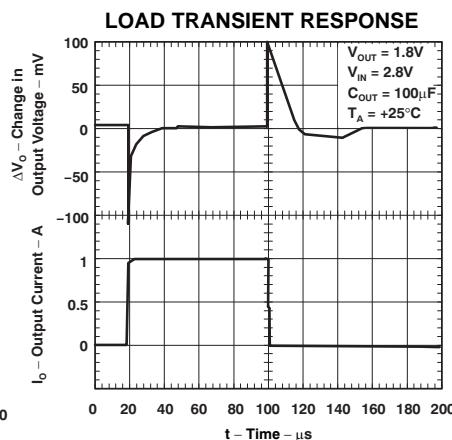


Figure 15.

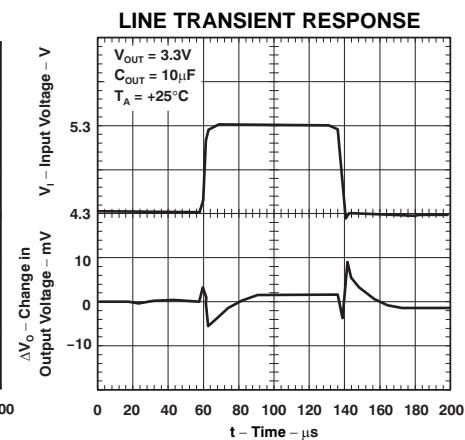


Figure 16.

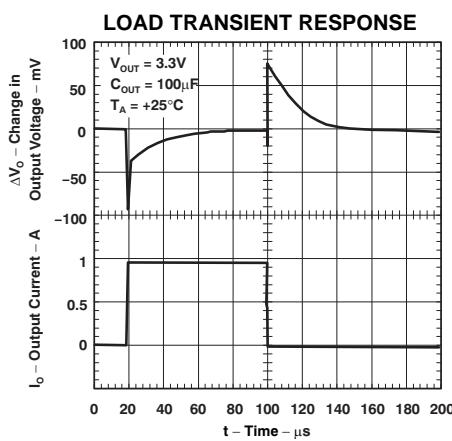


Figure 17.

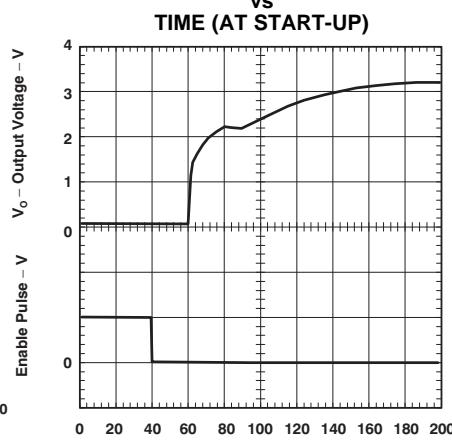


Figure 18.

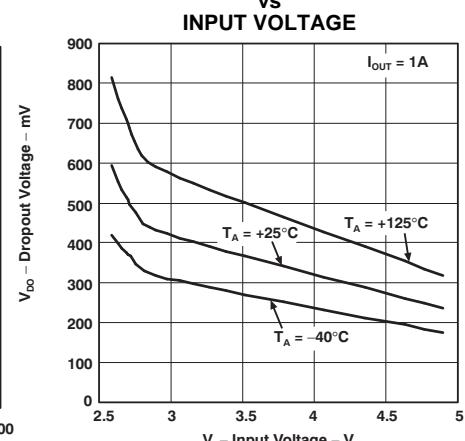
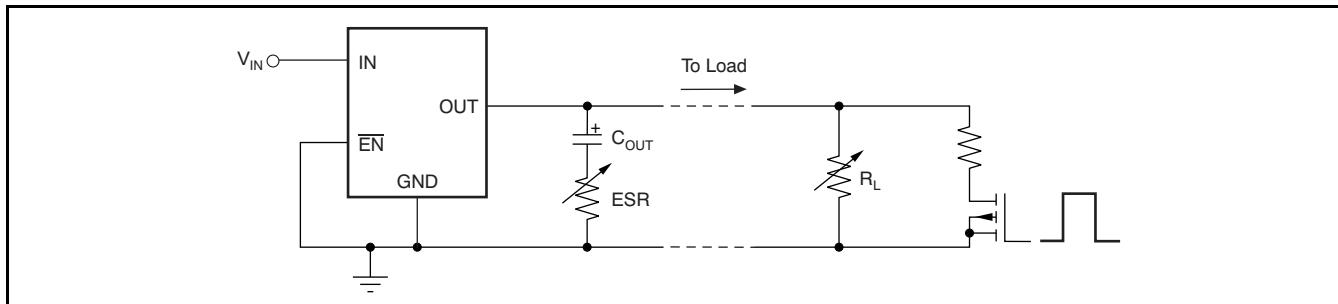


Figure 19.



**Figure 20. Test Circuit for Typical Regions of Stability (Figure 21 through Figure 24)
(Fixed Output Options)**

Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any resistance added externally, and PWB trace resistance to C_{OUT} .

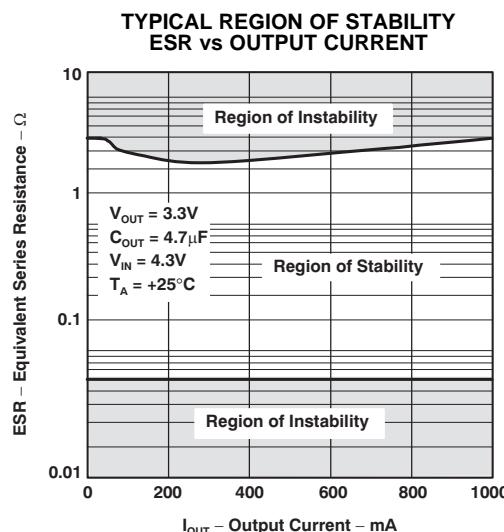


Figure 21.

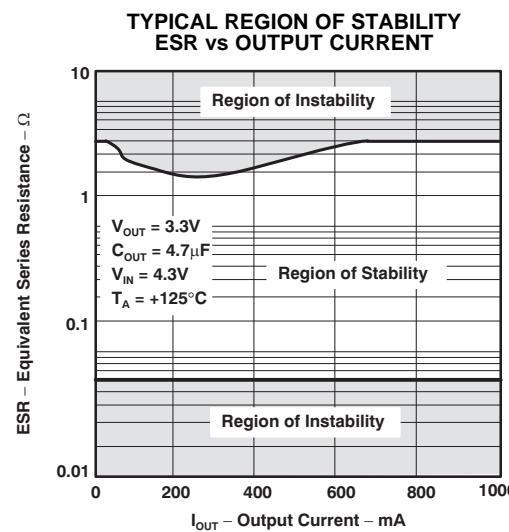


Figure 22.

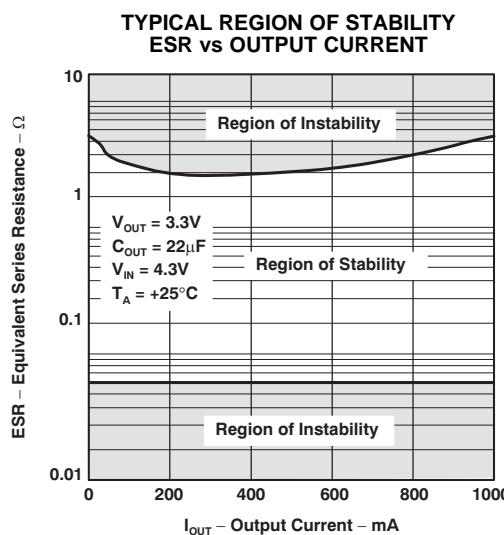


Figure 23.

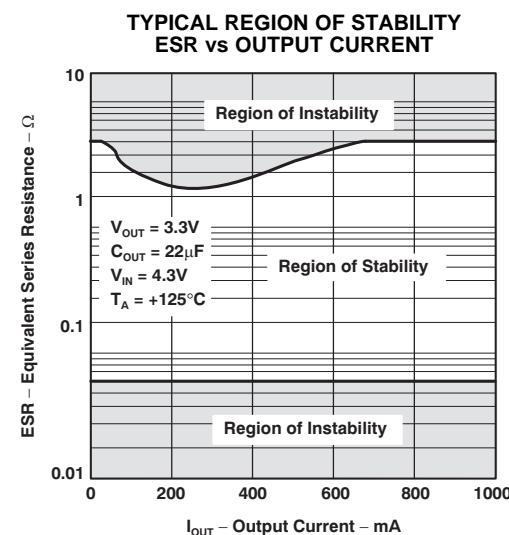


Figure 24.

APPLICATION INFORMATION

The features of the TPS7677D3xx family (low-dropout voltage, ultra low quiescent current, power-saving shutdown mode, and a supply-voltage supervisor) and the power-dissipation properties of the TSSOP PowerPAD package have enabled the integration of the dual LDO regulator with high output current for use in DSP and other multiple voltage applications. [Figure 25](#) shows a typical dual-voltage DSP application.

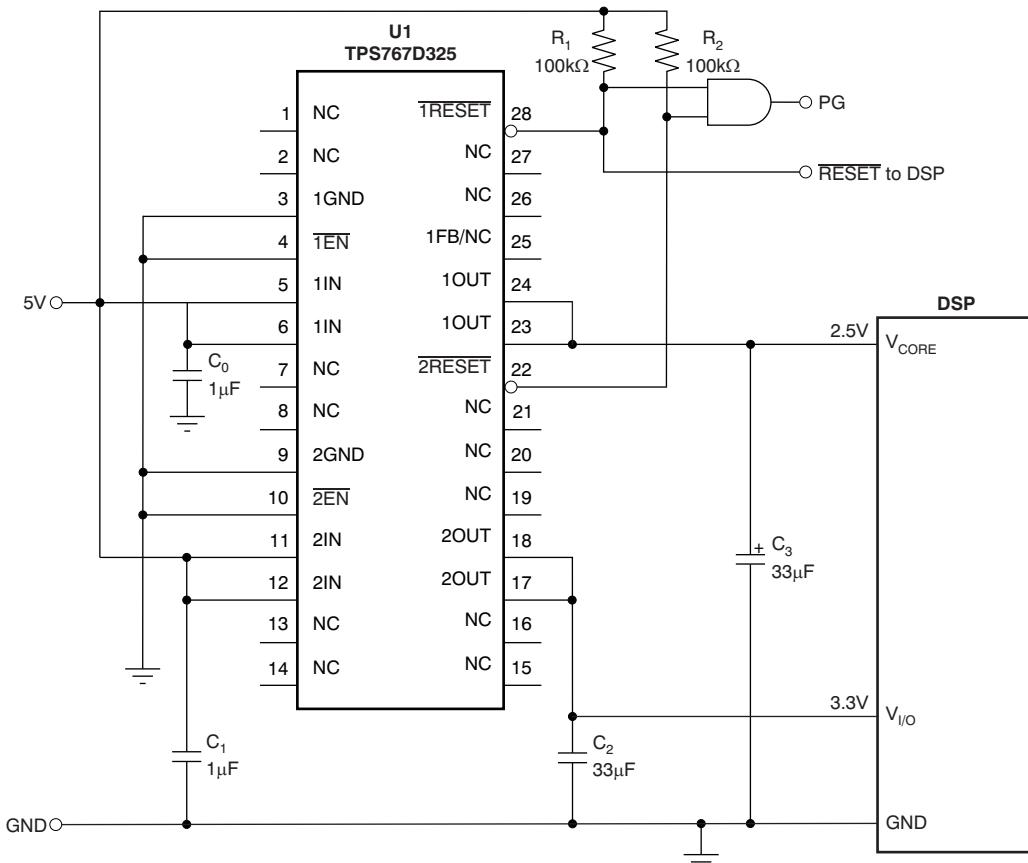


Figure 25. Dual-Voltage DSP Application

DSP power requirements include very high transient currents that must be considered in the initial design. This design uses higher-valued output capacitors to handle the large transient currents.

DEVICE OPERATION

The TPS767D3xx features very low quiescent current, which remain virtually constant even with varying loads. Conventional LDO regulators use a pnp pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). Close examination of the data sheets reveals that these devices are typically specified under near no-load conditions; actual operating currents are much higher as evidenced by typical quiescent current versus load current curves. The TPS767D3xx uses a PMOS transistor to pass current; because the gate of the PMOS is voltage driven, operating current is low and invariable over the full load range. The TPS767D3xx specifications reflect actual performance under load condition.

Another pitfall associated with the pnp pass element is its tendency to saturate when the device goes into dropout. The resulting drop in β forces an increase in I_B to maintain the load. During power-up, this translates to large start-up currents. Systems with limited supply current may fail to start up. In battery-powered systems, it means rapid battery discharge when the voltage decays below the minimum required for regulation. The TPS767D3xx quiescent current remains low even when the regulator drops out, eliminating both problems.

The TPS767D3xx family also features a shutdown mode that places the output in the high-impedance state (essentially equal to the feedback-divider resistance) and reduces quiescent current to under $2\mu\text{A}$. If the shutdown feature is not used, EN should be tied to ground. Response to an enable transition is quick; regulated output voltage is typically re-established in $120\mu\text{s}$.

MINIMUM LOAD REQUIREMENTS

The TPS767D3xx family is stable even at zero load; no minimum load is required for operation.

FB-PIN CONNECTION (ADJUSTABLE VERSION ONLY)

The FB pin is an input pin to sense the output voltage and close the loop for the adjustable option. The output voltage is sensed through a resistor divider network as is shown in [Figure 26](#) to close the loop. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit to improve performance at that point. Internally, FB connects to a high-impedance, wide-bandwidth amplifier and noise pickup feeds through to the regulator output. Routing the FB connection to minimize/avoid noise pickup is essential. In fixed output options, this pin is not connected.

EXTERNAL CAPACITOR REQUIREMENTS

An input capacitor is not required; however, a ceramic bypass capacitor (0.047pF to $0.1\mu\text{F}$) improves load transient response and noise rejection when the TPS767D3xx is located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of millamps) load transients with fast rise times are anticipated.

Like all low dropout regulators, the TPS767D3xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value is $10\mu\text{F}$ and the ESR (equivalent series resistance) must be between $60\text{m}\Omega$ and 1.5Ω . Capacitor values of $10\mu\text{F}$ or larger are acceptable, provided the ESR is less than 1.5Ω . Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described previously.

When necessary to achieve low height requirements along with high output current and/or high ceramic load capacitance, several higher ESR capacitors can be used in parallel to meet the previous guidelines.

PROGRAMMING THE TPS767D301 ADJUSTABLE LDO REGULATOR

The output voltage of the TPS767D301 adjustable regulator is programmed using an external resistor divider as shown in [Figure 26](#). The output voltage is calculated using:

$$V_{\text{OUT}} = V_{\text{REF}} \times \left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

Resistors R_1 and R_2 should be chosen for approximately $40\mu\text{A}$ divider current. Lower-value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error.

The recommended design procedure is to choose $R_2 = 30.1\text{ k}\Omega$ to set the divider current at $40\mu\text{A}$ and then calculate R_1 using:

$$R_1 = \left(\frac{V_{\text{OUT}}}{V_{\text{REF}}} - 1 \right) \times R_2 \quad (2)$$

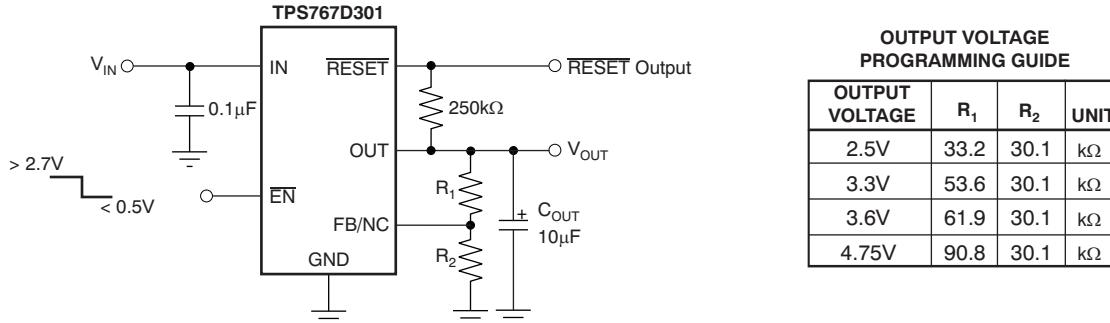


Figure 26. TPS767D301 Adjustable LDO Regulator Programming

RESET INDICATOR

The TPS767D3xx features a RESET output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to 95% (typical) of its regulated value, the RESET output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating. RESET can be used to drive power-on reset circuitry or as a low-battery indicator.

REGULATOR PROTECTION

The TPS767D3xx PMOS-pass transistor has a built-in back-gate diode that safely conducts reverse currents when the input voltage drops below the output voltage (for example, during power-down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS767D3xx also features internal current limiting and thermal protection. During normal operation, the TPS767D3xx limits output current to approximately 1.7A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds +150°C (typ), thermal-protection circuitry shuts it down. Once the device has cooled below +130°C (typ), regulator operation resumes.

POWER DISSIPATION AND JUNCTION TEMPERATURE

Specified regulator operation is assured to a junction temperature of +125°C; the maximum junction temperature should be restricted to +125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D\max}$, and the actual dissipation, P_D , which must be less than or equal to $P_{D\max}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D\max} = \frac{T_{J\max} - T_A}{R_{\theta JA}} \quad (3)$$

Where:

- $T_{J\max}$ is the maximum allowable junction temperature.
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, that is, 28°C/W for the 28-terminal PWP with no airflow.
- T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (4)$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation will trigger the thermal protection circuit.

Revision History

Changes from Revision F (February 2008) to Revision G	Page
• Changed Corrected symbol for FB current in <i>Electrical Characteristics</i>	3

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS767D301PWP	Active	Production	HTSSOP (PWP) 28	50 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS767D301
TPS767D301PWP.A	Active	Production	HTSSOP (PWP) 28	50 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS767D301
TPS767D301PWPG4	Active	Production	HTSSOP (PWP) 28	50 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS767D301
TPS767D301PWPR	Active	Production	HTSSOP (PWP) 28	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS767D301
TPS767D301PWPR.A	Active	Production	HTSSOP (PWP) 28	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS767D301
TPS767D301PWPRG4	Active	Production	HTSSOP (PWP) 28	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS767D301
TPS767D318PWP	Active	Production	HTSSOP (PWP) 28	50 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS767D318
TPS767D318PWP.A	Active	Production	HTSSOP (PWP) 28	50 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS767D318
TPS767D318PWPG4	Active	Production	HTSSOP (PWP) 28	50 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS767D318
TPS767D318PWPR	Active	Production	HTSSOP (PWP) 28	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS767D318
TPS767D318PWPR.A	Active	Production	HTSSOP (PWP) 28	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS767D318
TPS767D325PWP	Active	Production	HTSSOP (PWP) 28	50 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS767D325
TPS767D325PWP.A	Active	Production	HTSSOP (PWP) 28	50 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS767D325
TPS767D325PWPR	Active	Production	HTSSOP (PWP) 28	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS767D325
TPS767D325PWPR.A	Active	Production	HTSSOP (PWP) 28	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS767D325

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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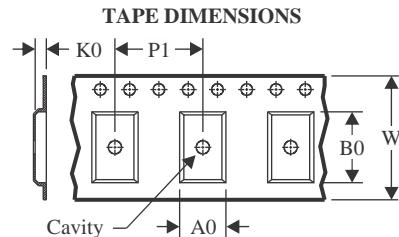
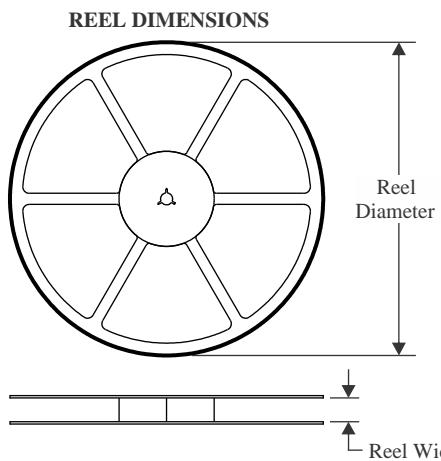
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS767D3 :

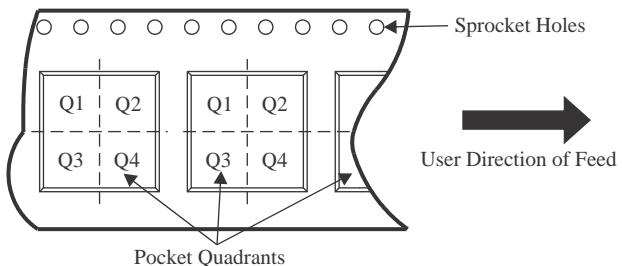
- Automotive : [TPS767D3-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


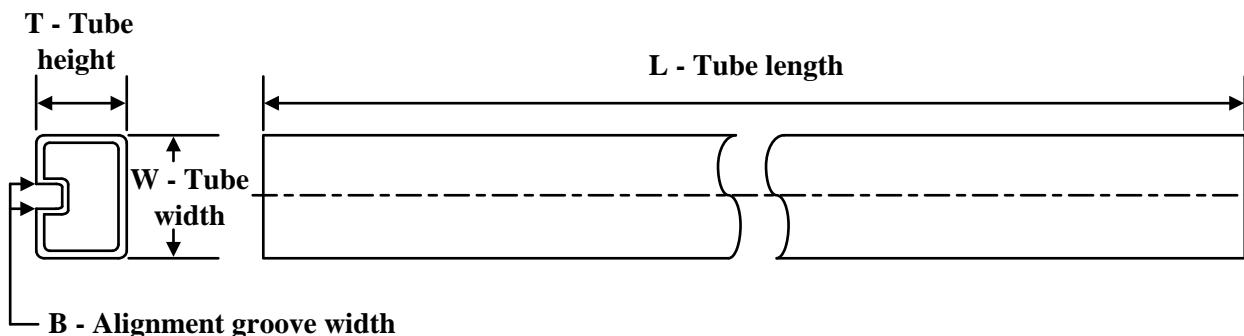
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS767D301PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
TPS767D318PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
TPS767D325PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS767D301PWPR	HTSSOP	PWP	28	2000	350.0	350.0	43.0
TPS767D318PWPR	HTSSOP	PWP	28	2000	350.0	350.0	43.0
TPS767D325PWPR	HTSSOP	PWP	28	2000	350.0	350.0	43.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μ m)	B (mm)
TPS767D301PWP	PWP	HTSSOP	28	50	530	10.2	3600	3.5
TPS767D301PWP.A	PWP	HTSSOP	28	50	530	10.2	3600	3.5
TPS767D301PWPG4	PWP	HTSSOP	28	50	530	10.2	3600	3.5
TPS767D318PWP	PWP	HTSSOP	28	50	530	10.2	3600	3.5
TPS767D318PWP.A	PWP	HTSSOP	28	50	530	10.2	3600	3.5
TPS767D318PWPG4	PWP	HTSSOP	28	50	530	10.2	3600	3.5
TPS767D325PWP	PWP	HTSSOP	28	50	530	10.2	3600	3.5
TPS767D325PWP.A	PWP	HTSSOP	28	50	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

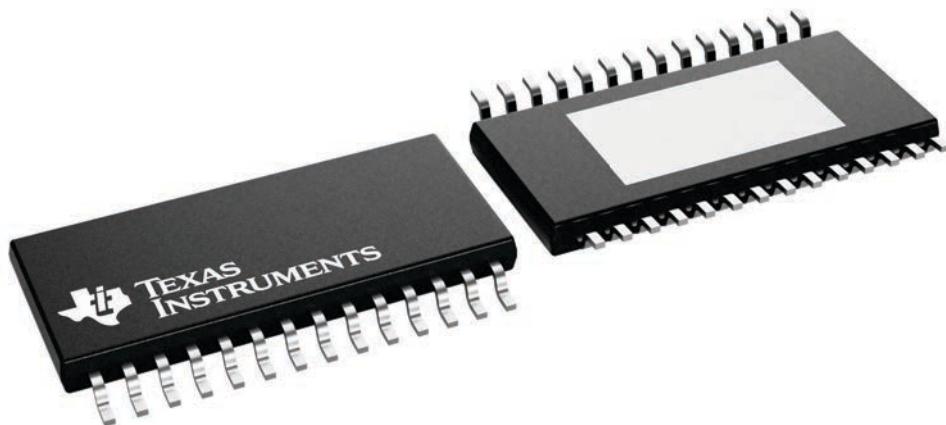
PWP 28

4.4 x 9.7, 0.65 mm pitch

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

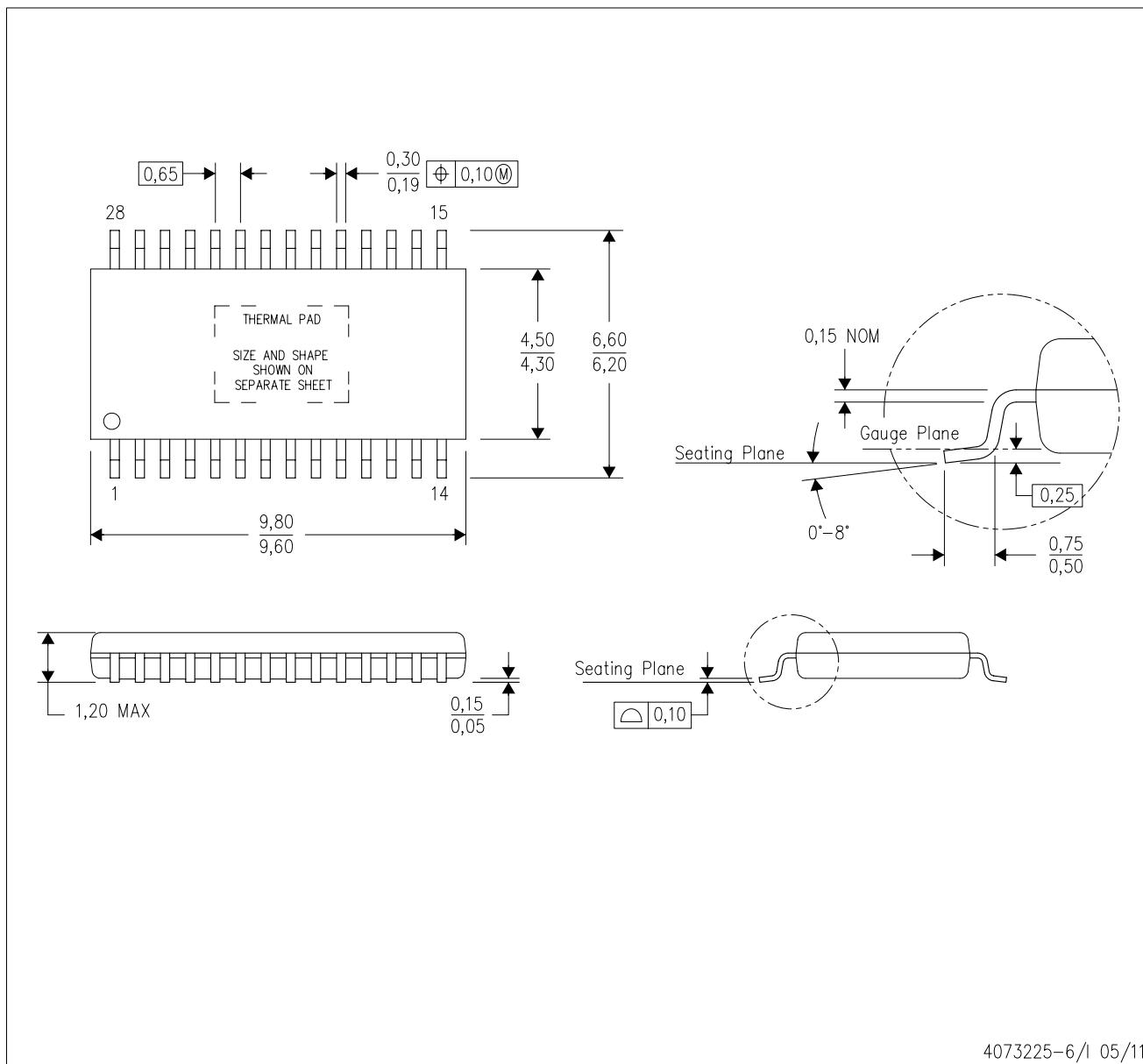
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224765/B

PWP (R-PDSO-G28)

PowerPAD™ PLASTIC SMALL OUTLINE



4073225-6/1 05/11

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
- This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
- See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

THERMAL PAD MECHANICAL DATA

PWP (R-PDSO-G28)

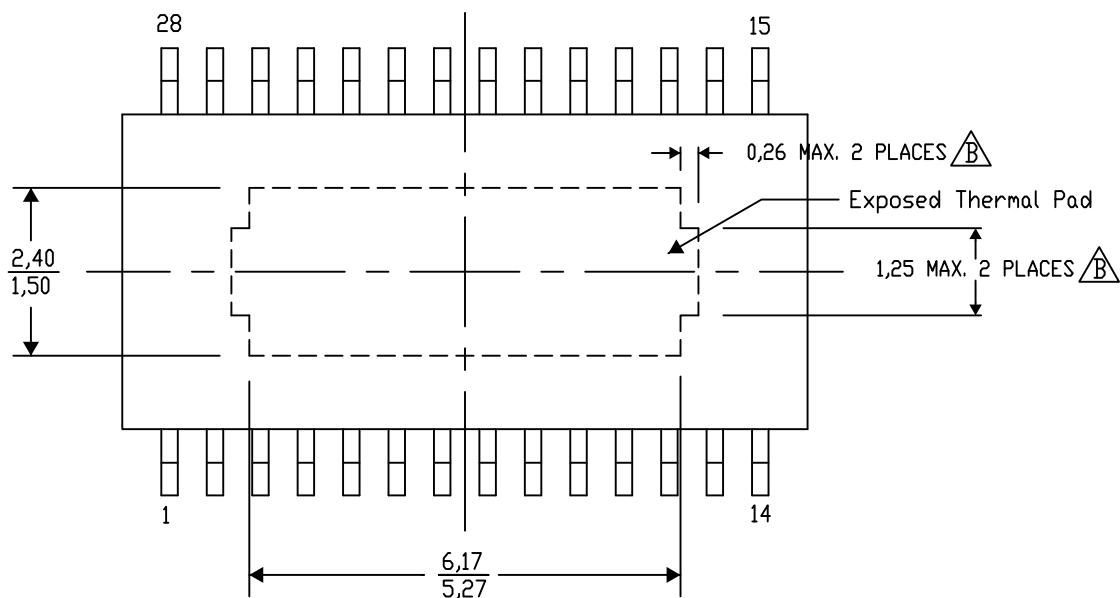
PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332-33/AO 01/16

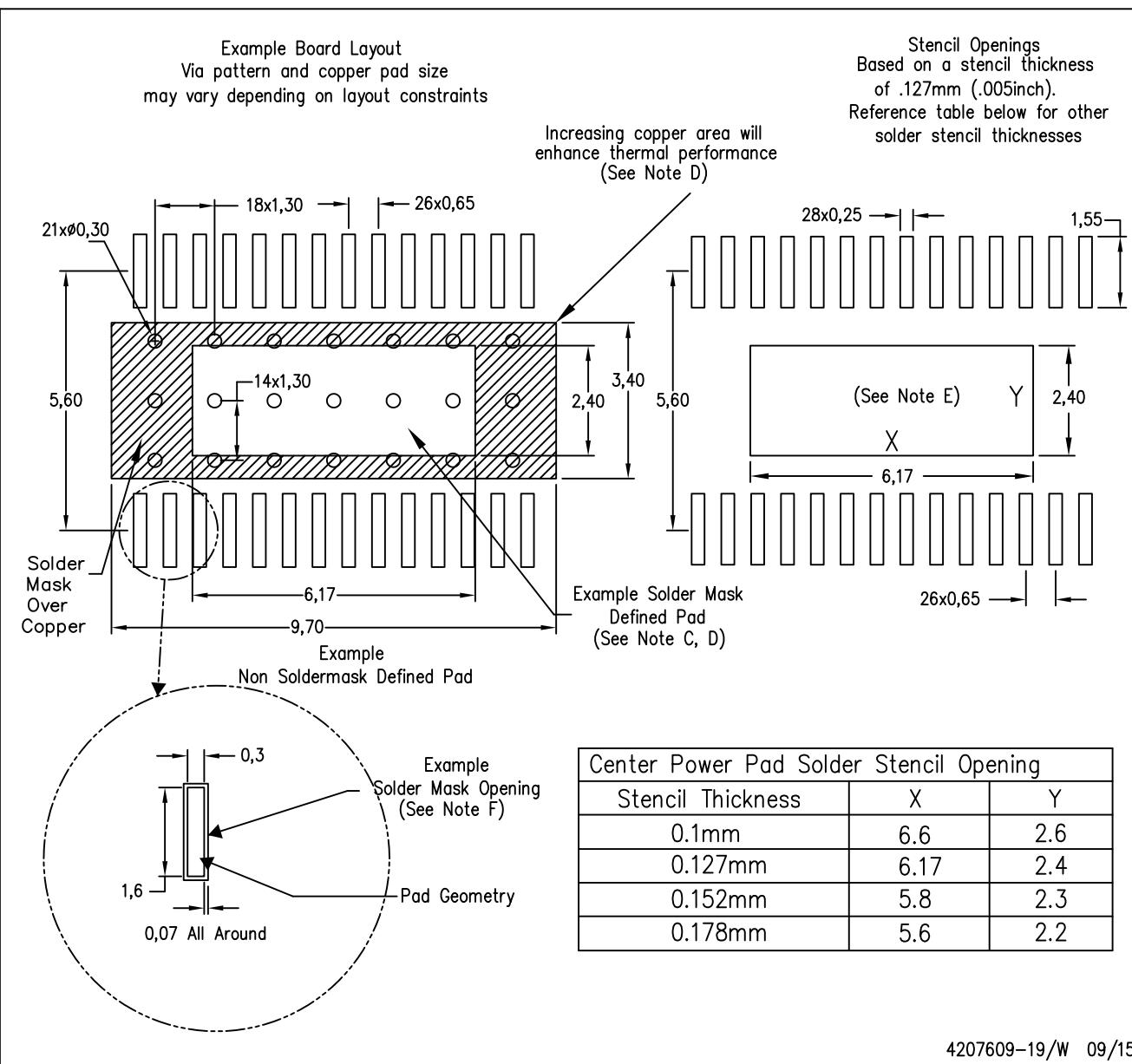
NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R-PDSO-G28)

PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets.
- For specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Last updated 10/2025