TPS793：低ノイズ、高 PSRR、RF 対応、200mA 出力の低ドロップアウト リニア レギュレータ、NanoStar™ ウェハー チップ スケールおよび SOT-23 パッケージ

1 特長

- イネーブル搭載、低ドロップアウト レギュレータ
- 固定電圧バージョンで利用可能:
  - 1.8V ～ 4.75V (レガシー チップ)
  - 1.8V ～ 3.3V (新チップ)
- 可変出力電圧範囲:1.22V～5.5V
- 低ノイズ:
  - 55μV_{RMS} (従来チップ)
  - 69μV_{RMS} (新チップ)
- 高速起動:
  - 50μs (従来チップ)
  - 500μs (新チップ)
- 非常に低いドロップアウト電圧:112mV (標準値)
- ポートフォリオの最新デバイスについては、TPS7A20 を参照してください

2 アプリケーション

- TV アプリケーション
- ビル オートメーション
- スマートフォンとタブレット
- ネットワーク接続の周辺機器とプリンタ
- ホーム シアターおよびエンターテインメント

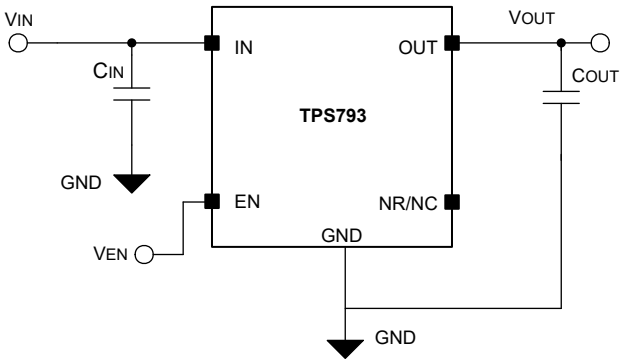
3 概要

TPS793 は、低ドロップアウト (LDO) 電圧レギュレータで、電源除去比 (PSRR) が高く、ラインおよび負荷の過渡応答が優れているのが特長です。このデバイスは、出力に小型の 2.2μF セラミック コンデンサを接続することで安定して動作します。TPS793 は、例えば 200mA で 112mV (代表値) といった低ドロップアウト電圧を提供します。出力ノイズが小さく PSRR が優れているため、このデバイスは電力の制約が厳しいアナログ負荷に適しています。TPS793 は、調整可能な機能により、ポスト レギュレーションに適したフレキシブルなオプションを提供します。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
TPS793	DBV (SOT-23、6)	2.9mm × 2.8mm
	DBV (SOT-23、5)	2.9mm × 2.8mm
	YZQ (DSBGA、5)(3)	1.35mm × 1mm

(1) 詳細については、*メカニカル、パッケージ、および注文情報*をご覧ください。
(2) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。
(3) レガシー チップ専用です。



代表的なアプリケーション回路

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4 Pin Configuration and Functions

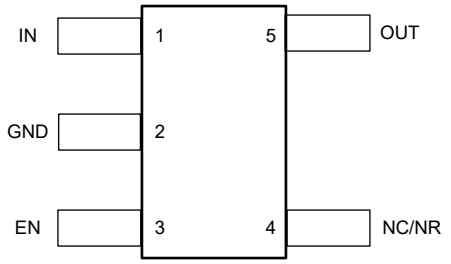


図 4-1. DBV Package, 5-Pin SOT-23 Fixed Voltage Version (Top View)

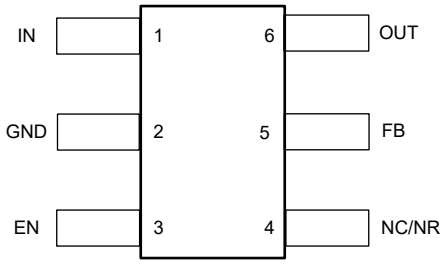


図 4-2. DBV Package, 6-Pin SOT-23 Adjustable Voltage Version (Top View)

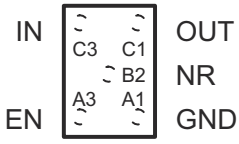


図 4-3. YZQ Package, 5-Pin DSBGA (Top View) (Legacy Chip Only)

表 4-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	DBV	YZQ		
EN	3	A3	I	Enable pin. Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. EN can be connected to IN if not used.
FB	5	—	I	Feedback pin. This terminal is the feedback input pin for the adjustable device. Fixed voltage versions in the DBV package do not have this pin.
GND	2	A1	—	Regulator ground.
IN	1	C3	I	Input to the device.
NR/NC	4	B2	—	Noise Reduction pin (legacy chip only). Connecting an external capacitor to this pin filters noise generated by the internal bandgap. This configuration improves power-supply rejection and reduces output noise for the legacy chip and YZQ package only. No Connect pin (new chip only). This pin is not internally connected. Connect to GND for improved thermal performance or leave floating. For lower noise performance on a fixed device, consider looking at the TPS7A20.
OUT	6	C1	O	Output of the regulator.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	V_{IN} , V_{EN}, V_{OUT} (Legacy Chip)	–0.3	6	V
	V_{IN} , V_{EN} (New Chip)	–0.3	6.5	V
	V_{OUT} (New Chip)	–0.3	V_{IN} + 0.3 (2)	
Current	Output, I_{OUT}	Internally limited		
Temperature	Operating junction, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The absolute maximum rating is V_{IN} + 0.3 V or 6.5 V, whichever is smaller.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, V all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.7		5.5	V
V_{EN}	Enable voltage	0		5.5	V
V_{OUT}	Output voltage	V_{FB}		5	V
I_{OUT}	Output current	0		200	mA
T_J	Operating junction temperature	–40		125	°C
C_{IN}	Input capacitor (Legacy Chip)	0.1	1		µF
	Input capacitor (New Chip)	1			
C_{OUT}	Output capacitor	2.2(1) (2)	10		µF
C_{NR}	Noise reduction capacitor(3)	0	10		nF
C_{FF}	Feed-forward capacitor (Legacy Chip)		15		pF
	Feed-forward capacitor (New Chip)(4)	0	10	100	nF
R_2	Lower feedback resistor (Legacy Chip)		30.1		kΩ
F_{EN}	Enable toggle frequency (New Chip)			10	kHz

(1) If C_{FF} is not used or V_{OUT}(nom) < 1.8V, the minimum recommended C_{OUT} = 4.7µF.
(2) The minimum effective capacitance is 0.47 µF for the new chip only.
(3) Legacy Chip only. The New Chip does not have a Noise Reduction pin. For more information please refer to Pin Functions table.
(4) Feed-forward capacitor is optional and not required for stability.

5.4 Thermal Information

THERMAL METRIC[1]		TPS793				UNIT
		DBV (SOT23-6)	YZQ (DSBGA)	DBV (SOT23-6)[2]	DBV (SOT23-5)[2]	
		6 PINS	5 PINS	6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	225.1	178.5	171.7	182.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78.4	1.4	110.8	114.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.7	62.1	85.4	79.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.3	0.9	54.4	56.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	53.8	62.1	85.2	78.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Packaging application note.
(2) New Chip.

5.5 Electrical Characteristics

over recommended operating temperature range, T_J = –40°C to +125°C $V_{EN} = V_{IN}$, $V_{IN} = V_{O(typ)}$ + 1V, I_{OUT} = 1 mA, C_{OUT} = 10 µF, C_{NR} = 0.01 µF (Legacy Chip) (unless otherwise noted). All typical values at T_J= 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range [1]			2.7		5.5	V
I_{OUT}	Continuous output current			0		200	mA
V_{OUT}	Output voltage range	TPS79301		V_{FB}		5.5 – $V_{DROPOUT}$	V
		TPS79318	0µA < I_{OUT} < 200mA, 2.8V < V_{IN} < 5.5V	1.764	1.8	1.836	
		TPS79325	0µA < I_{OUT} < 200mA, 3.5V < V_{IN} < 5.5V	2.45	2.5	2.55	
		TPS79328	0µA < I_{OUT} < 200mA, 3.8V < V_{IN} < 5.5V	2.744	2.8	2.856	
		TPS793285 (Legacy chip only)	0µA < I_{OUT} < 200mA, 3.85V < V_{IN} < 5.5V	2.793	2.85	2.907	
		TPS79330	0µA < I_{OUT} < 200mA, 4V < V_{IN} < 5.5V	2.94	3	3.06	
		TPS79333	0µA < I_{OUT} < 200mA, 4.3V < V_{IN} < 5.5V	3.234	3.3	3.366	
		TPS793475 (Legacy chip only)	0µA < I_{OUT} < 200mA, 5.25V < V_{IN} < 5.5V	4.655	4.75	4.845	
I_{GND}	Quiescent current (GND current)	0µA ≤ I_O ≤ 200mA (Legacy Chip)			170	220	µA
		0µA ≤ I_O ≤ 200mA(New Chip)			250	1000	
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	0µA ≤ I_{OUT} ≤ 200mA			5		mV
$\Delta V_{OUT}/\Delta VIN$	Line regulation	V_{OUT} + 1V ≤ V_{IN} ≤ 5.5V			0.05	0.12	%/V

5.5 Electrical Characteristics (続き)

over recommended operating temperature range, T_J = –40°C to +125°C V_{EN} = V_{IN}, V_{IN} = $V_{O(typ)}$ + 1V, I_{OUT} = 1 mA, C_{OUT} = 10 µF, C_{NR} = 0.01 µF (Legacy Chip) (unless otherwise noted). All typical values at T_J= 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Vn[2]	Output noise voltage TPS79328	BW = 100Hz to 100kHz, I_{OUT} = 200mA	C_{NR} = 0.001µF		55		μV_{RMS}
		BW = 100Hz to 100kHz, I_{OUT} = 200mA	C_{NR} = 0.0047µF		36		
		BW = 100Hz to 100kHz, I_{OUT} = 200mA	C_{NR} = 0.01µF		33		
		BW = 100Hz to 100kHz, I_{OUT} = 200mA	C_{NR} = 0.1µF		32		
		BW = 100Hz to 100kHz, I_{OUT} = 200mA	(New Chip)[4]		69		
t_{STR}	Time, start-up (TPS79328)	R_L = 14 Ω, C_{OUT} = 1µF	C_{NR} = 0.001µF		50		µs
	Time, start-up (TPS79328)		C_{NR} = 0.0047µF		50		
	Time, start-up (TPS79328)		C_{NR} = 0.01µF		50		
	Time, start-up (TPS79328)		(New Chip)		500		
I_{CL}	Output current limit	V_{OUT} = 0V(Legacy Chip)		285		600	mA
I_{CL}	Output current limit	V_{IN} = $V_{OUT(NOM)}$ + 1 V, V_{OUT} = 0.9 x $V_{OUT(NOM)}$ (New Chip only)		320		460	mA
I_{SC}	Short-circuit current limit	V_{OUT} = 0V (New Chip)			175		mA
I_{SHDN}	Shutdown current	V_{EN} = 0V, 2.7V < V_I < 5.5V(Legacy Chip)[3]			0.07	1	µA
		V_{EN} = 0V, 2.7V < V_I < 5.5V(New Chip)[3]			0.01	1	
$V_{EN(HI)}$	High-level enable input voltage	2.7V ≤ V_{IN} ≤ 5.5V		1.7		V_{IN}	V
$V_{EN(HI)}$	High-level enable input voltage	2.7V ≤ V_{IN} ≤ 5.5V (New Chip)		0.85		V_{IN}	V
$V_{EN(LOW)}$	Low-level enable input voltage	2.7V ≤ V_{IN} ≤ 5.5V		0		0.7	V
$V_{EN(LOW)}$	Low-level enable input voltage	2.7V ≤ V_{IN} ≤ 5.5V (New Chip)		0		0.425	V
I_{EN}	Enable pin current	V_{EN} = 0 V		–1		1	µA
I_{FB}	Feedback pin current (TPS79301)	V_{FB} = 1.8V (Legacy Chip)				1	µA
		V_{FB} = 1.8V (New Chip)				0.05	
V_{REF}	Internal reference (TPS79301)			1.201	1.225	1.25	V

5.5 Electrical Characteristics (続き)

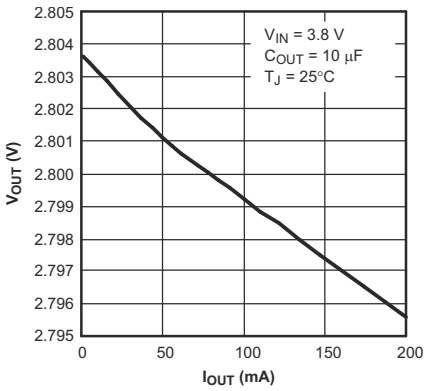
over recommended operating temperature range, T_J = –40°C to +125°C V_{EN} = V_{IN}, V_{IN} = $V_{O(typ)}$ + 1V, I_{OUT} = 1 mA, C_{OUT} = 10 µF, C_{NR} = 0.01 µF (Legacy Chip) (unless otherwise noted). All typical values at T_J= 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
PSRR	Power-supply rejection ratio (TPS79328)	f = 100Hz	I_{OUT} = 10mA (Legacy Chip)		70		dB
			I_{OUT} = 10mA (New Chip)		64		
			I_{OUT} = 200mA (Legacy Chip)		68		
			I_{OUT} = 200mA (New Chip)		65		
		f = 10kHz	I_{OUT} = 200mA (Legacy Chip)		70		
			I_{OUT} = 200mA (New Chip)		49		
		f = 100kHz	I_{OUT} = 200mA (Legacy Chip)		43		
			I_{OUT} = 200mA (New Chip)		39		
V_{DO} (4)	Dropout voltage (TPS79328)	V_{IN}= V_{OUT} - 0.1V, I_{OUT} = 200mA			120	200	mV
	Dropout voltage (TPS793285) (I egacy chip only)	V_{IN}= V_{OUT} - 0.1V, I_{OUT} = 200mA			120	200	
	Dropout voltage (TPS79330)	V_{IN}= V_{OUT} - 0.1V, I_{OUT} = 200mA			112	200	
	Dropout voltage (TPS79333)	V_{IN}= V_{OUT} - 0.1V, I_{OUT} = 200mA			112	180	
	Dropout voltage (TPS793475) (legacy chip only)	V_{IN}= V_{OUT} - 0.1V, I_{OUT} = 200mA			77	125	
V_{UVLO}	UVLO threshold	V_{IN} rising (Legacy Chip)		2.25		2.65	V
		VIN rising (New Chip)		1.32		1.6	
$V_{UVLO(HYST)}$	UVLO hysteresis	T_J = 25°C, V_{CC} rising (Legacy Chip)			100		mV
		T_J = 25°C, V_{CC} rising (New Chip)			130		

(1) Minimum VIN is 2.7 V or V_{OUT} + V_{DO}, whichever is greater.
(2) New Chip does not have a Noise Reduction pin.
(3) For adjustable versions, this parameters applies only after V_{IN} is applied; then V_{EN} transitions high to low.
(4) Dropout is not measured for the TPS79318 and TPS79325 because minimum V_{IN} = 2.7V.

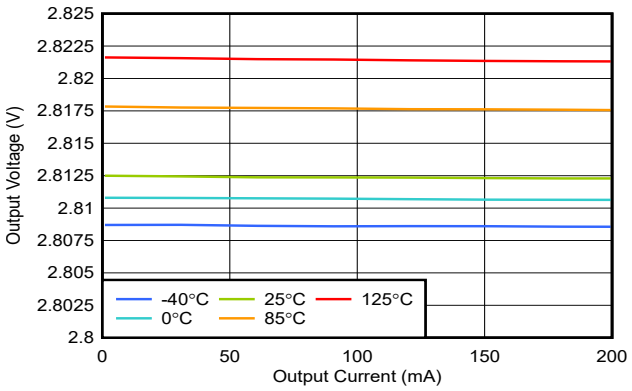
5.6 Typical Characteristics

over recommended operating temperature range, T_J = –40°C to +125°C $V_{EN} = V_{IN}$, $V_{IN} = V_{O(typ)}$ + 1V I_{OUT} = 1mA, C_{OUT} = 10µF, C_{NR} = 0.01µF (legacy chip) (unless otherwise noted); all typical values at T_J= 25°C



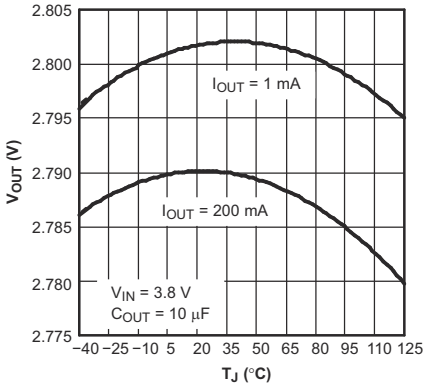
Legacy chip

図 5-1. TPS793 Output Voltage vs Output Current



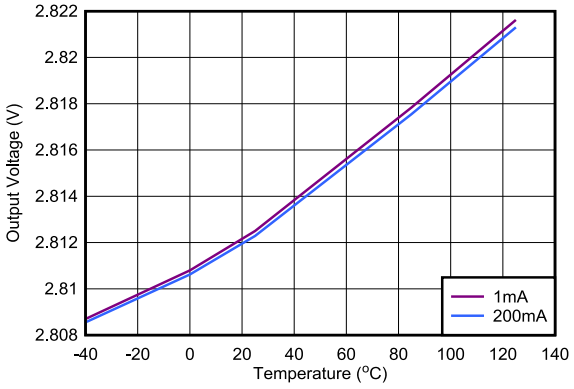
New chip

図 5-2. TPS793 Output Voltage vs Output Current



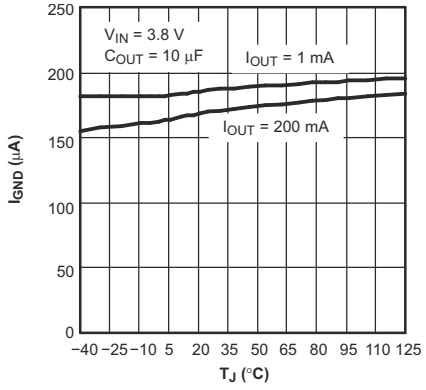
Legacy chip

図 5-3. TPS793 Output Voltage vs Junction Temperature



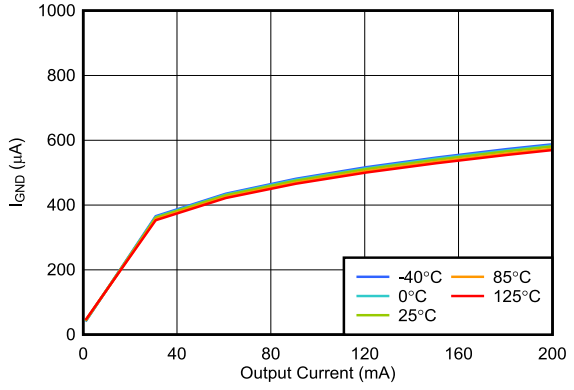
New chip

図 5-4. TPS793 Output Voltage vs Junction Temperature



Legacy chip

図 5-5. TPS793 Ground Current vs Junction Temperature

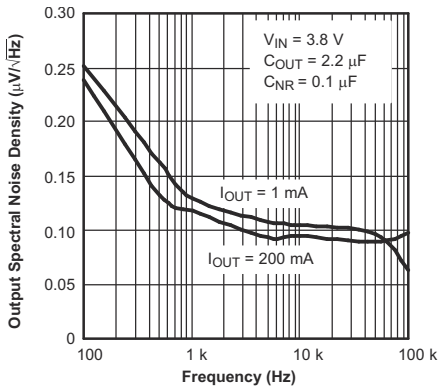


New chip

図 5-6. TPS793 Ground Current vs Junction Temperature

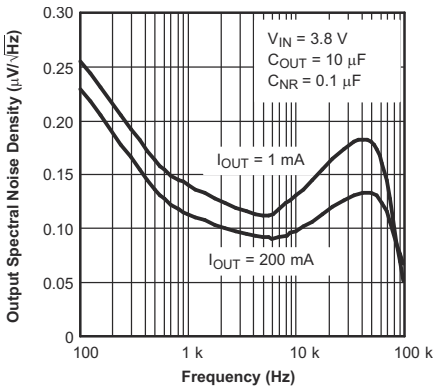
5.6 Typical Characteristics (continued)

over recommended operating temperature range, T_J = –40°C to +125°C V_{EN} = V_{IN}, V_{IN} = $V_{O(typ)}$ + 1V I_{OUT} = 1mA, C_{OUT} = 10µF, C_{NR} = 0.01µF (legacy chip) (unless otherwise noted); all typical values at T_J= 25°C



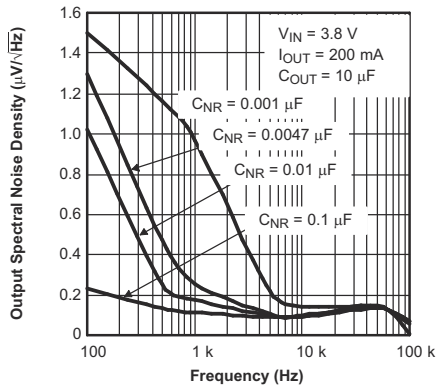
Legacy chip

図 5-7. TPS793 Output Spectral Noise Density vs Frequency



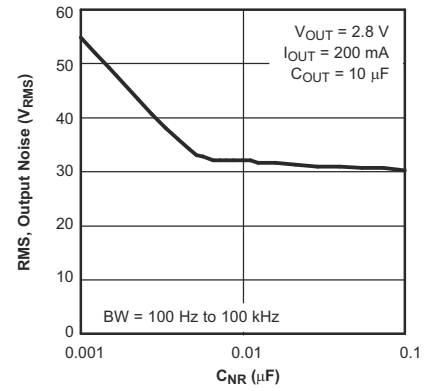
Legacy chip

図 5-8. TPS793 Output Spectral Noise Density vs Frequency



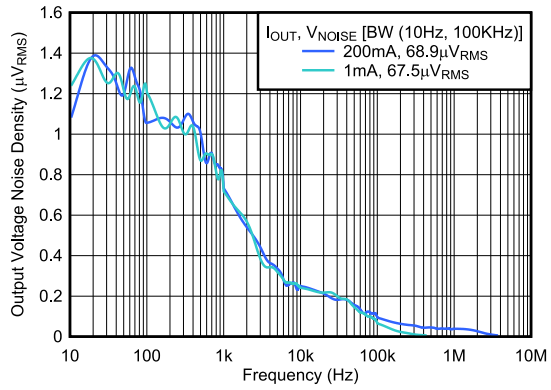
Legacy chip

図 5-9. TPS793 Output Spectral Noise Density vs Frequency



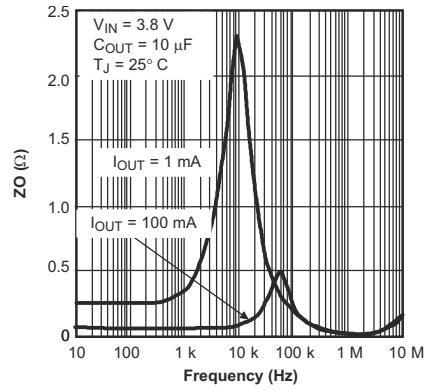
Legacy chip

図 5-10. Root Mean Square Output Noise vs C_{NR}



C_{OUT} = 10uF (new chip)

図 5-11. TPS793 Output Spectral Noise Density vs Frequency

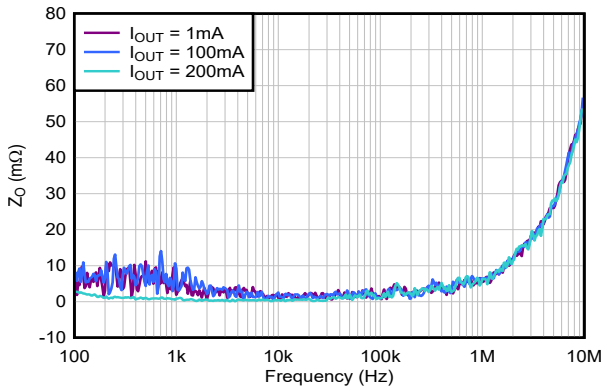


Legacy chip

図 5-12. Output Impedance vs Frequency

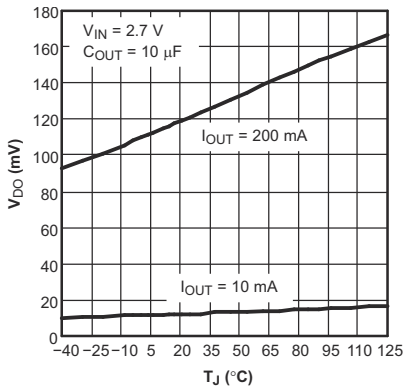
5.6 Typical Characteristics (continued)

over recommended operating temperature range, T_J = –40°C to +125°C V_{EN} = V_{IN}, V_{IN} = $V_{O(typ)}$ + 1V I_{OUT} = 1mA, C_{OUT} = 10µF, C_{NR} = 0.01µF (legacy chip) (unless otherwise noted); all typical values at T_J= 25°C



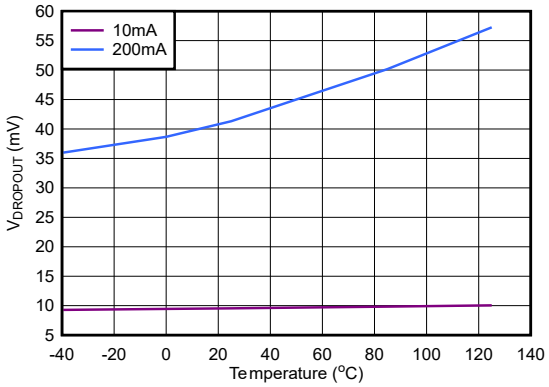
New chip

図 5-13. Output Impedance vs Frequency



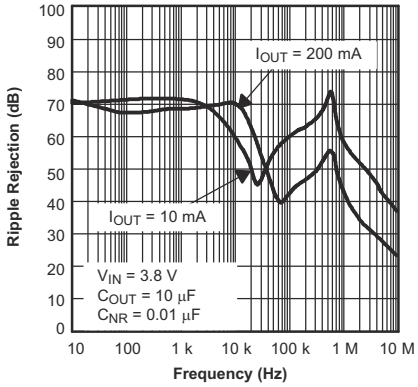
Legacy chip

図 5-14. TPS793 Dropout Voltage vs Junction Temperature



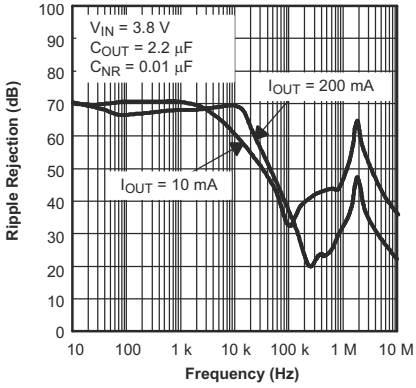
New chip

図 5-15. TPS793 Dropout Voltage vs Junction Temperature



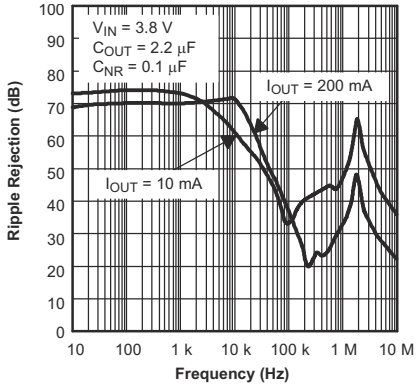
Legacy chip

図 5-16. TPS793 Ripple Rejection vs Frequency



Legacy chip

図 5-17. TPS793 Ripple Rejection vs Frequency

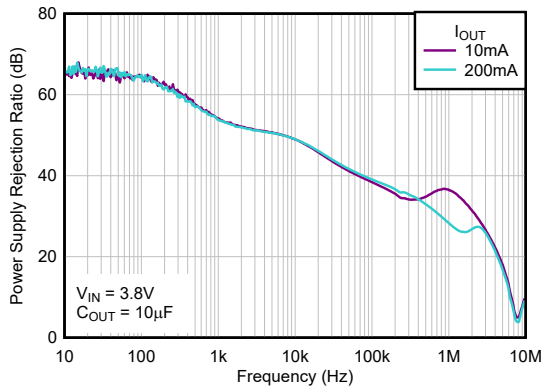


Legacy chip

図 5-18. TPS793 Ripple Rejection vs Frequency

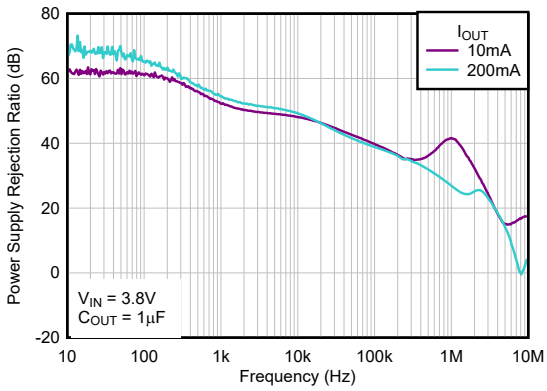
5.6 Typical Characteristics (continued)

over recommended operating temperature range, T_J = –40°C to +125°C $V_{EN} = V_{IN}$, $V_{IN} = V_{O(typ)}$ + 1V I_{OUT} = 1mA, C_{OUT} = 10µF, C_{NR} = 0.01µF (legacy chip) (unless otherwise noted); all typical values at T_J= 25°C



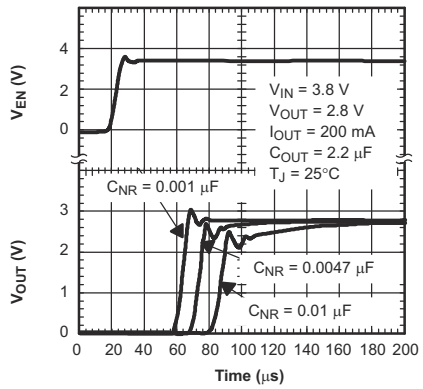
New chip

図 5-19. TPS793 Ripple Rejection vs Frequency



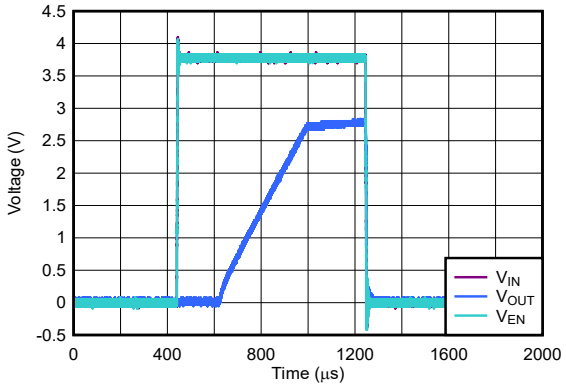
New chip

図 5-20. TPS793 Ripple Rejection vs Frequency



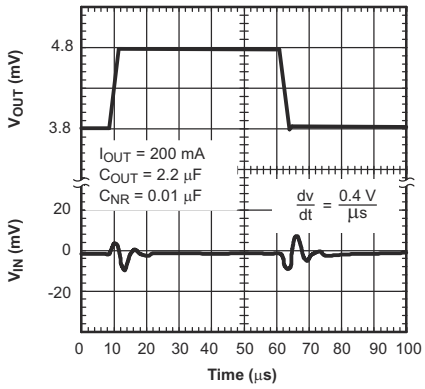
Legacy chip

図 5-21. TPS793 Output Voltage, Enable Voltage vs Time (Start-Up)



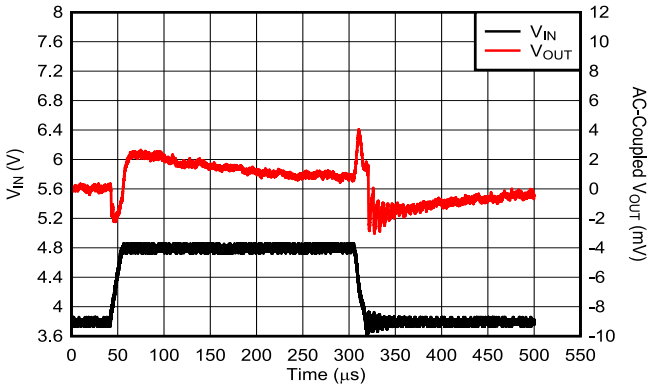
New chip

図 5-22. TPS793 Output Voltage, Enable Voltage vs Time (Start-Up)



Legacy chip

図 5-23. TPS793 Line Transient Response

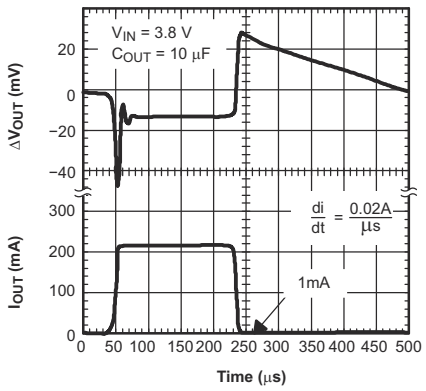


New chip

図 5-24. TPS793 Line Transient Response

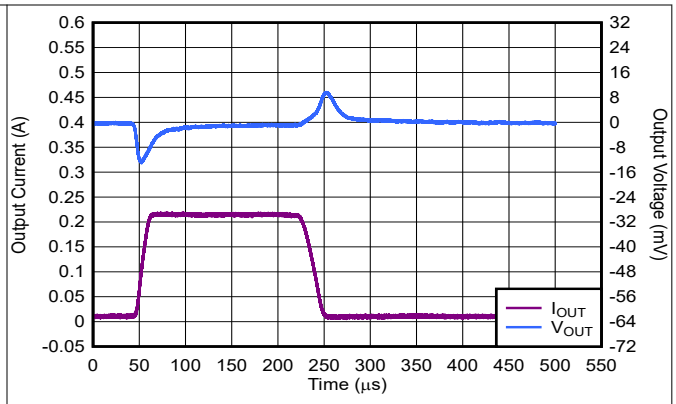
5.6 Typical Characteristics (continued)

over recommended operating temperature range, T_J = –40°C to +125°C V_{EN} = V_{IN}, V_{IN} = $V_{O(typ)}$ + 1V I_{OUT} = 1mA, C_{OUT} = 10µF, C_{NR} = 0.01µF (legacy chip) (unless otherwise noted); all typical values at T_J= 25°C



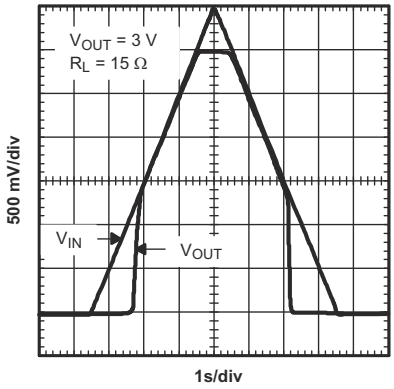
Legacy chip

図 5-25. TPS79328 Load Transient Response



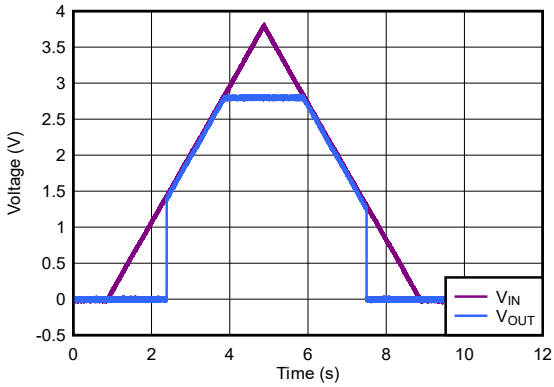
New chip

図 5-26. TPS79328 Load Transient Response



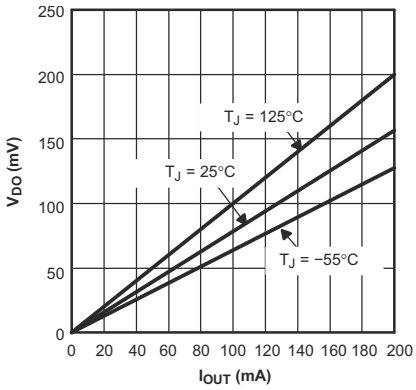
Legacy chip

図 5-27. Power-Up and Power-Down



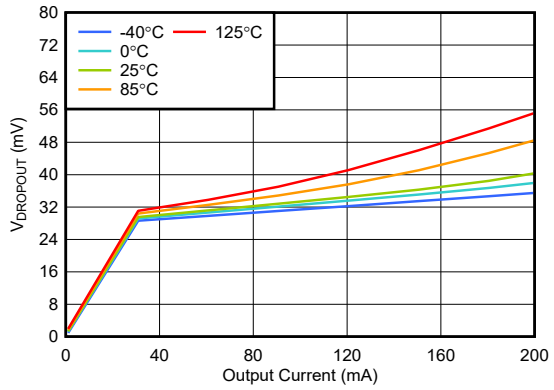
New chip

図 5-28. Power-Up and Power-Down



Legacy chip

図 5-29. Dropout Voltage vs Output Current

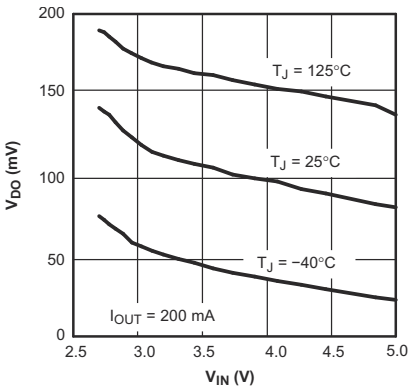


New chip

図 5-30. Dropout Voltage vs Output Current

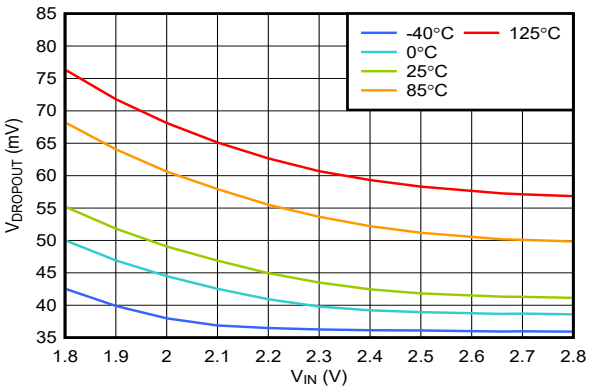
5.6 Typical Characteristics (continued)

over recommended operating temperature range, T_J = –40°C to +125°C V_{EN} = V_{IN}, V_{IN} = $V_{O(typ)}$ + 1V I_{OUT} = 1mA, C_{OUT} = 10µF, C_{NR} = 0.01µF (legacy chip) (unless otherwise noted); all typical values at T_J= 25°C



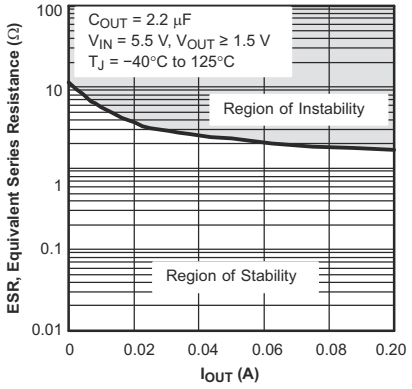
Legacy chip

図 5-31. TPS793 Dropout Voltage vs Input Voltage



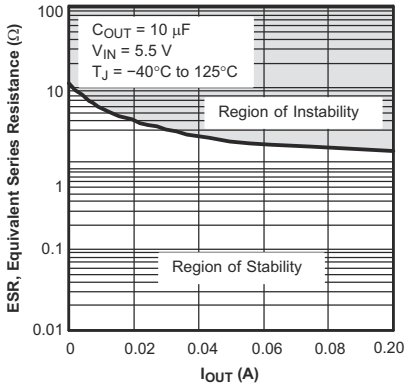
New chip

図 5-32. TPS793 Dropout Voltage vs Input Voltage



Legacy chip

図 5-33. Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current



Legacy chip

図 5-34. Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

6 Detailed Description

6.1 Overview

The TPS793 family of LDO regulators has been optimized for use in noise-sensitive battery-operated equipment. The device features extremely low dropout voltages, high PSRR, ultralow output noise, low quiescent current, and enable-input to reduce supply currents to less than 1µA when the regulator is turned off.

6.2 Functional Block Diagrams

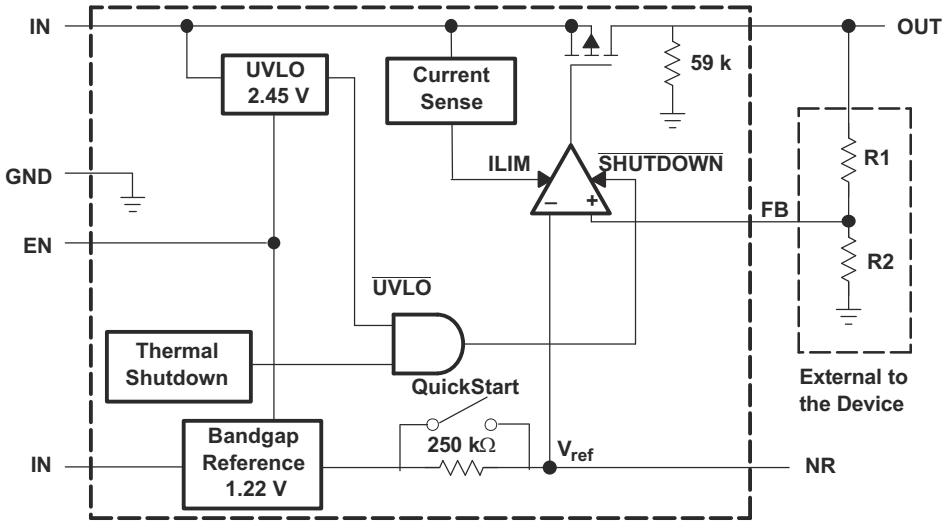


図 6-1. TPS79301 Block Diagram (Adjustable Version, Legacy Chip)

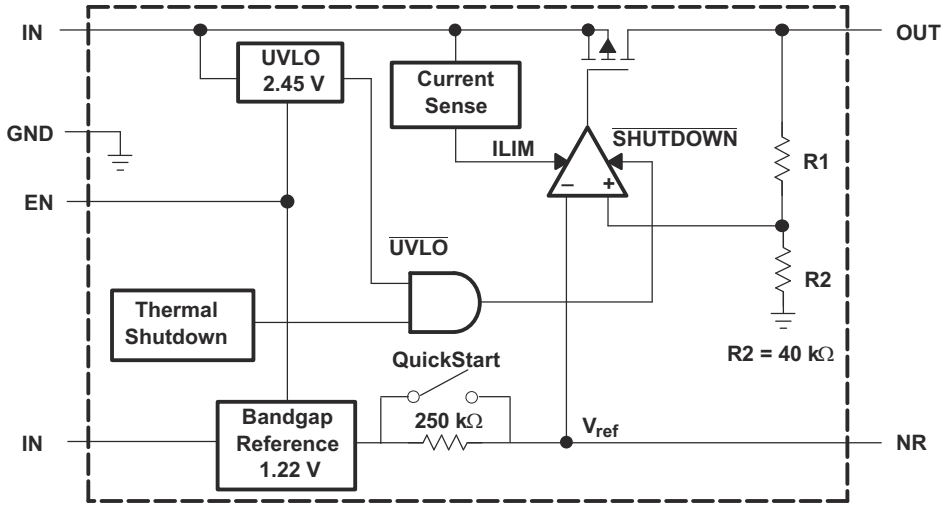


図 6-2. TPS793 Block Diagram (Fixed Version, Legacy Chip)

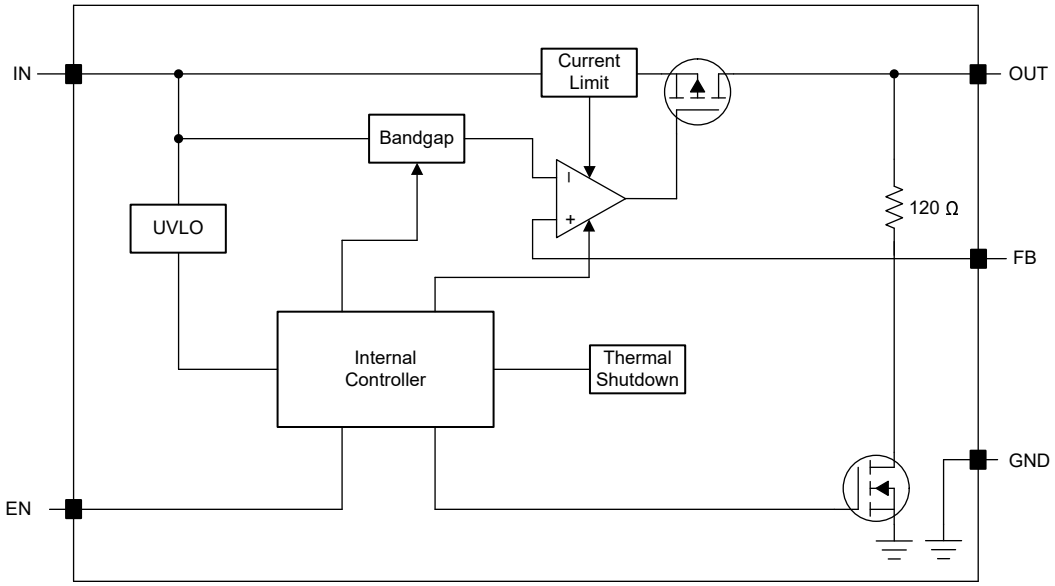


図 6-3. TPS79301 Block Diagram (Adjustable Version, Legacy Chip)

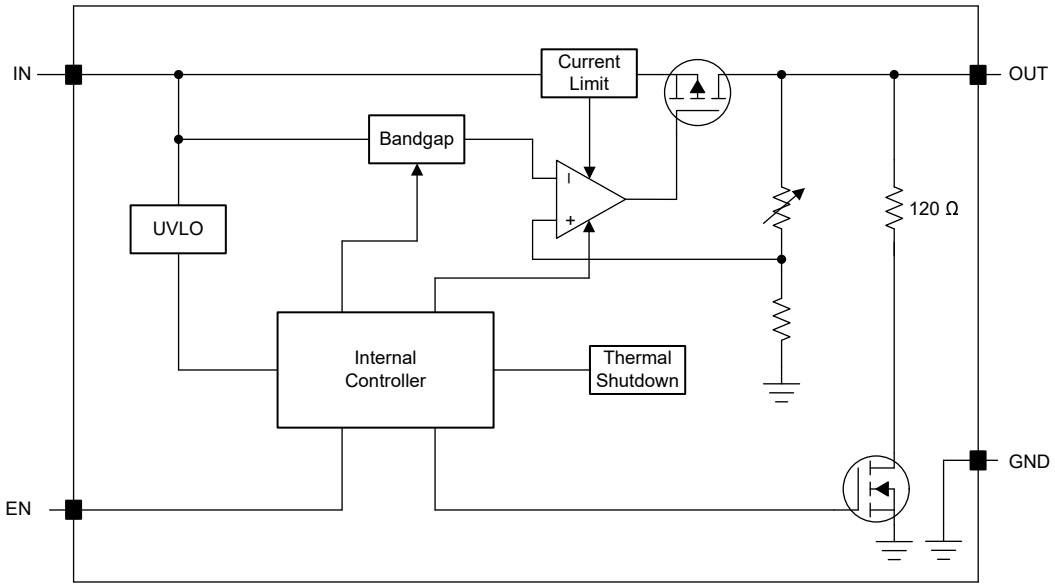


図 6-4. TPS793 Block Diagram (Fixed Version, New Chip)

6.3 Feature Description

6.3.1 Undervoltage Lockout (UVLO)

The TPS793 uses an undervoltage lockout (UVLO) circuit that disables the output until the input voltage is greater than the rising UVLO voltage. This circuit verifies that the device does not exhibit any unpredictable behavior when the supply voltage is lower than the operational range of the internal circuitry, $V_{IN(min)}$.

6.3.2 Shutdown

The enable pin (EN) is active high. Enable the device by forcing the EN pin to exceed $V_{EN(high)}$. Turn off the device by forcing the EN pin to drop below the maximum EN pin low-level input voltage (see *Electrical Characteristics* table). If shutdown capability is not required, connect EN to IN.

6.3.3 Active Discharge (new chip)

The device has an internal pulldown MOSFET that connects an $R_{PULLDOWN}$ resistor to ground when the device is disabled to actively discharge the output voltage. The active discharge circuit is activated by the enable pin.

Do not rely on the active discharge circuit to discharge the output voltage after the input supply has collapsed because reverse current can possibly flow from the output to the input. This reverse current flow can cause damage to the device especially when a large output capacitor is used. Limit reverse current to no more than 5% of the device rated current for a short period of time.

6.3.4 Foldback Current Limit

The legacy chip of TPS793 features internal current limiting and thermal protection. During normal operation, the TPS793 limits output current to approximately 400 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care must be taken not to exceed the power dissipation ratings of the package or the absolute maximum voltage ratings of the device.

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brickwall-foldback scheme. The current limit transitions from a brickwall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brickwall scheme limits the output current to the current limit (I_{CL}). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current as the output voltage approaches GND. When the output is shorted, the device supplies a typical current called the short-circuit current limit (I_{SC}). I_{CL} and I_{SC} are listed in the *Electrical Characteristics* table.

For this device, $V_{FOLDBACK} = 0.4 \times V_{OUT(NOM)}$.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brickwall current limit, the pass transistor dissipates power $[(V_{IN} – V_{OUT}) \times I_{CL}]$. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power $[(V_{IN} – V_{OUT}) \times I_{SC}]$. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application report.

図 6-5 shows a diagram of the foldback current limit.

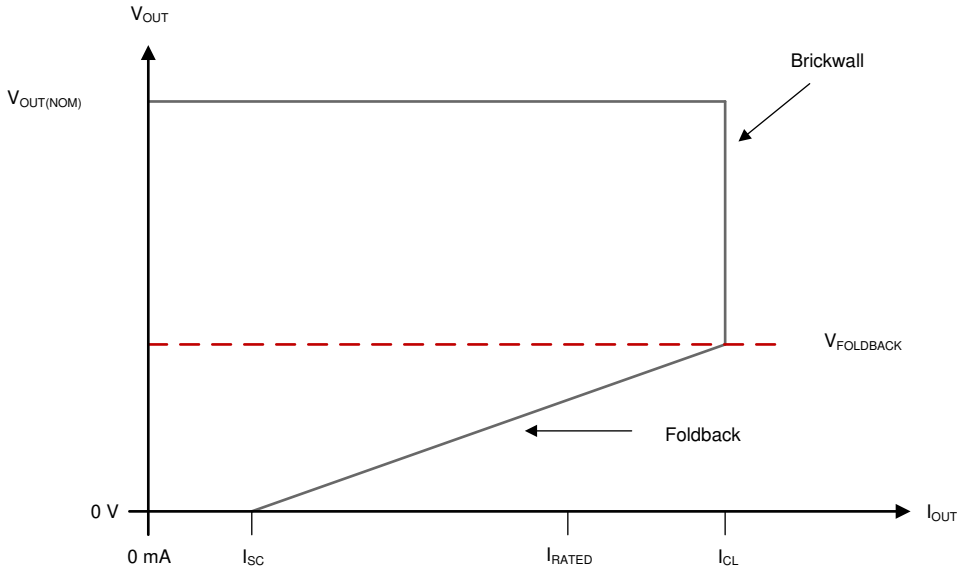


図 6-5. Foldback Current Limit

6.3.5 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 165°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle on and off. This cycling limits regulator dissipation, protecting the device from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature must be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The TPS793 internal protection circuitry is designed to protect against overload conditions. This circuitry is not intended to replace proper heatsinking. Continuously running the TPS793 into thermal shutdown degrades device reliability.

6.3.6 Reverse Current

The legacy chip of TPS793 PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (for example, during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting to 5% of the rated output current is recommended.

The new chip of TPS793, as with most modern LDOs, excessive reverse current can damage this device.

Reverse current flows through the body diode on the pass element instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device as a result of one of the following conditions:

- Degradation caused by electromigration
- Excessive heat dissipation
- Potential for a latch-up condition

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} > V_{IN} + 0.3$ V:

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, external protection must be used to protect the device. 図 6-6 shows one approach of protecting the device.

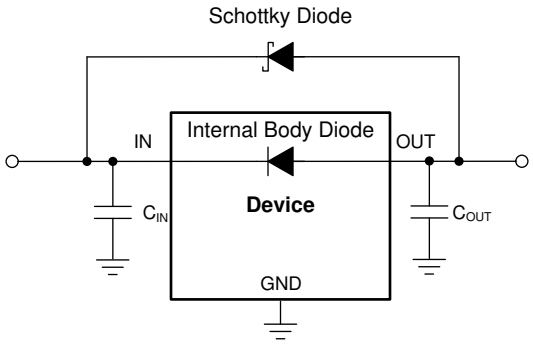


図 6-6. Example Circuit for Reverse Current Protection Using a Schottky Diode

6.4 Device Functional Modes

6.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is at least as high as $V_{IN(min)}$.
- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The enable voltage is greater than $V_{EN(min)}$.
- The output current is less than the current limit.
- The device junction temperature is less than the maximum specified junction temperature.

6.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode of operation, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in the linear region and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

6.4.3 Disabled

The device is disabled under the following conditions:

- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.
- The input voltage is less than $UVLO_{falling}$.

表 6-1 shows the conditions that lead to the different modes of operation.

表 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(high)}$	$I_{OUT} < I_{LIM}$	$T_J < 125°C$
Dropout mode	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(high)}$	—	$T_J < 125°C$
Disabled mode (any true condition disables the device)	$V_{IN} < UVLO_{falling}$	$V_{EN} < V_{EN(low)}$	—	$T_J > 165°C$(1)

(1) Approximate value for thermal shutdown.

7 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Application Information

The TPS793 family of LDO regulators has been optimized for use in noise-sensitive battery-operated equipment. The device features extremely low dropout voltages, high PSRR, low output noise, low quiescent current, and enable-input to reduce supply currents to less than 1µA when the regulator is turned off.

7.1.1 Adjustable Operation

The output voltage of the TPS79301 adjustable regulator is programmed using an external resistor divider as shown in 図 7-1. The output voltage is calculated using 式 1:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

where:

- V_{REF} = 1.2246 V typ (the internal reference voltage)

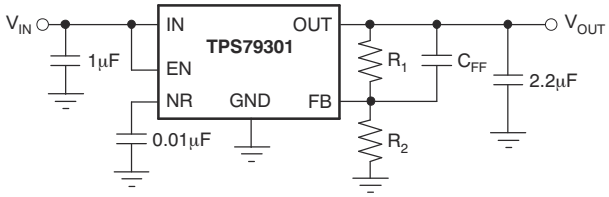
Resistors R_1 and R_2 must be selected for approximately 50-µA divider current. Lower value resistors can be used for improved noise performance, but the solution consumes more power. Higher resistors values can cause accuracy issues and other problems. The recommended design procedure is to choose R_2 = 30.1 kΩ to set the divider current at 50 µA, C_{FF} = 15 pF for stability, and then calculate R_1 using 式 2:

$$R_1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R_2 \quad (2)$$

To improve the stability of the adjustable version, place a small compensation capacitor between OUT and FB. For output voltages less than 1.8 V, the value of this capacitor must be 100 pF. For output voltages greater than 1.8 V, the approximate value of this capacitor can be calculated as shown in 式 3:

$$C_{FF} = \frac{(3 \times 10^{-7}) \times (R_1 + R_2)}{(R_1 \times R_2)} \quad (3)$$

The suggested value of this capacitor for several resistor ratios is shown in the table in 図 7-1. If this capacitor is not used (such as in a unity-gain configuration) or if an output voltage less than 1.8 V is chosen, then the minimum recommended output capacitor is 4.7 µF instead of 2.2 µF.



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R_1	R_2	C_{FF}
1.22V	short	open	0pF
2.5V	31.6kΩ	30.1kΩ	22pF
3.3V	51kΩ	30.1kΩ	15pF
3.6V	59kΩ	30.1kΩ	15pF

図 7-1. TPS79301 Adjustable LDO Regulator Programming

7.1.2 Exiting Dropout

Some applications have transients that place the LDO into dropout, such as slower ramps on V_{IN} during start-up. As with other LDOs, the output can overshoot on recovery from these conditions. A ramping input supply causes an LDO to overshoot on start-up, as shown in 図 7-2, when the slew rate and voltage levels are in the correct range. Use an enable signal to avoid this condition.

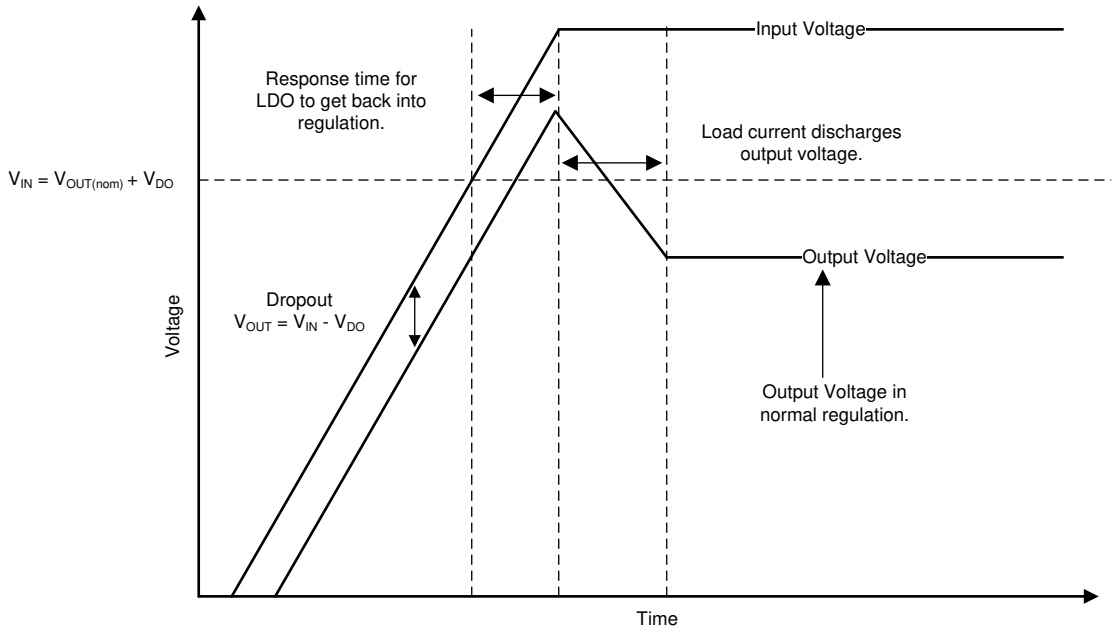


図 7-2. Start-Up Into Dropout

Line transients out of dropout can also cause overshoot on the output of the regulator. These overshoots are caused by the error amplifier having to drive the gate capacitance of the pass element and bring the gate back to the correct voltage for proper regulation. 図 7-3 illustrates what is happening internally with the gate voltage and how overshoot can be caused during operation. When the LDO is placed in dropout, the gate voltage (V_{GS}) is pulled all the way down to ground to give the pass device the lowest on-resistance as possible. However, if a line transient occurs when the device is in dropout, the loop is not in regulation and can cause the output to overshoot until the loop responds and the output current pulls the output voltage back down into regulation. If these transients are not acceptable, then continue to add input capacitance in the system until the transient is slow enough to reduce the overshoot.

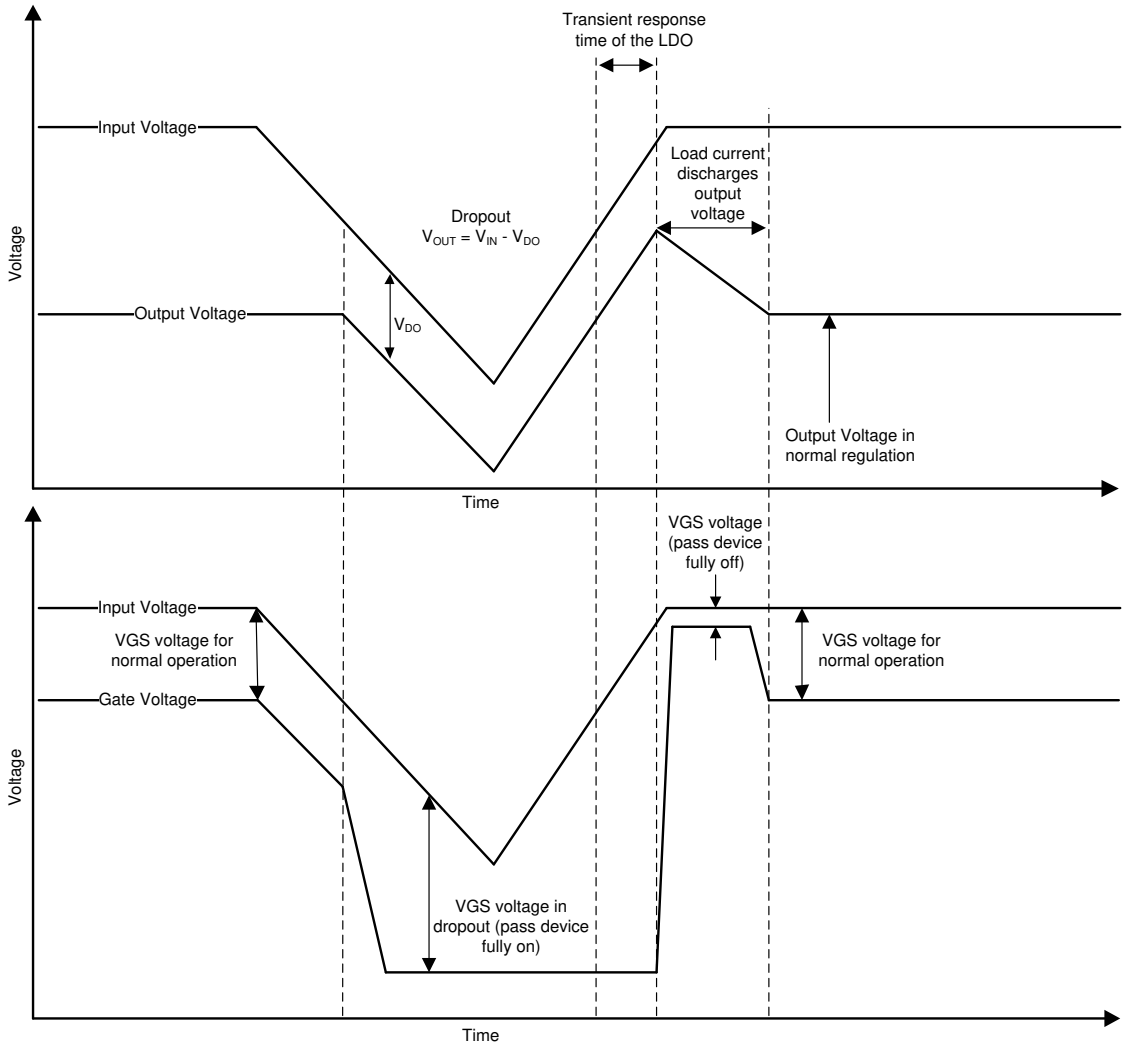


図 7-3. Line Transients From Dropout

7.2 Typical Application

A typical application circuit is shown in 図 7-4.

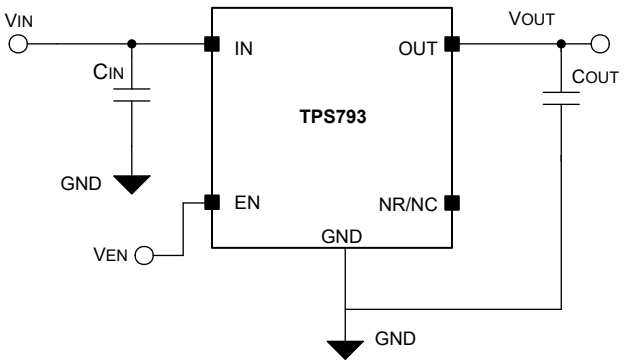


図 7-4. Typical Application Circuit

7.2.1 Design Requirements

表 7-1 lists the design requirements.

表 7-1. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	4.2V to 3V (lithium ion battery)
Output voltage	1.8V, ±1%
DC output current	10mA
Peak output current	75mA
Maximum ambient temperature	65°C

7.2.2 Detailed Design Procedure

Pick the desired output voltage option. An input capacitor of 1µF is used as the battery is connected to the input through a via and a short 10-mil (0.01-in) trace. An output capacitor of 10 µF is used to provide optimal response time for the load transient. Verify that the maximum junction temperature is not exceed by referring to 図 7-8.

7.2.2.1 Capacitor Recommendations

Low equivalent series resistance (ESR) capacitors must be used for the input, output, noise reduction, and bypass capacitors. Ceramic capacitors with X7R and X5R dielectrics are preferred. These dielectrics offer more stable characteristics. Ceramic X7R capacitors offer improved over-temperature performance, while ceramic X5R capacitors are more cost-effective and are available in higher values.

7.2.2.2 Input and Output Capacitor Requirements

A 0.1µF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the legacy chip of TPS793, is required for stability and improves transient response, noise rejection, and ripple rejection. A 1µF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the new chip of TPS793, is required for stability and improves transient response, noise rejection, and ripple rejection. A higher-value input capacitor can be necessary if large, fast-rise-time load transients are anticipated or the device is located several inches from the power source.

Like most low-dropout regulators, the TPS793 requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance is 2.2µF. Any 2.2µF or larger ceramic capacitor is suitable, provided the capacitance does not vary significantly over temperature. If load current is not expected to exceed 100 mA, a 1.0-µF ceramic capacitor can be used. If a feed-forward capacitor is not used (such as in a unity-gain configuration) or if an output voltage less than 1.8 V is chosen, then the

minimum recommended output capacitor is 4.7µF instead of 2.2µF. 表 7-2 lists the recommended output capacitor sizes for several common configurations.

表 7-2. Output Capacitor Sizing

Condition	C_{OUT} (µF)
V_{OUT} < 1.8 V or C_{FF} = 0 nF	4.7
V_{OUT} > 1.8 V, I_{OUT} > 100 mA	2.2
V_{OUT} > 1.8 V, I_{OUT} < 100 mA	1

7.2.2.3 Noise Reduction and Feed-Forward Capacitor Requirements

The internal voltage reference is a key source of noise in an LDO regulator. The legacy chip of TPS793 has an NR pin which is connected to the voltage reference through a 250-kΩ internal resistor. The 250-kΩ internal resistor, in conjunction with an external bypass capacitor connected to the NR pin, creates a low-pass filter to reduce the voltage reference noise and, therefore, the noise at the regulator output. In order for the regulator to operate properly, the current flow out of the NR pin must be at a minimum, because any leakage current creates an IR drop across the internal resistor, thus creating an output error. Therefore, the bypass capacitor must have minimal leakage current. The bypass capacitor must be no more than 0.1 µF to verify that the capacitor is fully charged during the quickstart time provided by the internal switch shown in the *Functional Block Diagrams*.

A feed-forward capacitor is recommended when using the adjustable version, to improve the stability of the device. If R_2 = 30.1 kΩ, set C_1 to 15 pF for optimal performance. For voltages less than 1.8 V, the value of this capacitor must be 100 pF. For voltages greater than 1.8 V, the approximate value of this capacitor can be calculated as shown in 式 3.

7.2.3 Application Curves

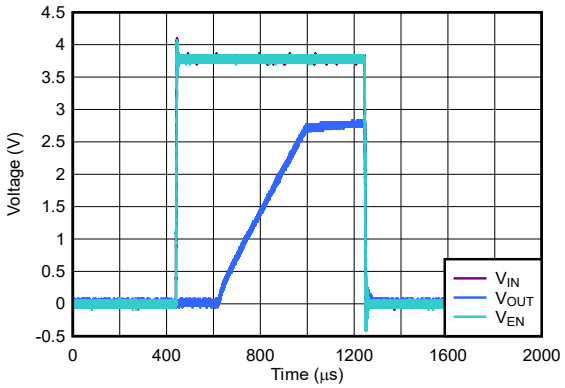


図 7-5. TPS79328 Output Voltage, Enable Voltage vs Time (Start-Up)

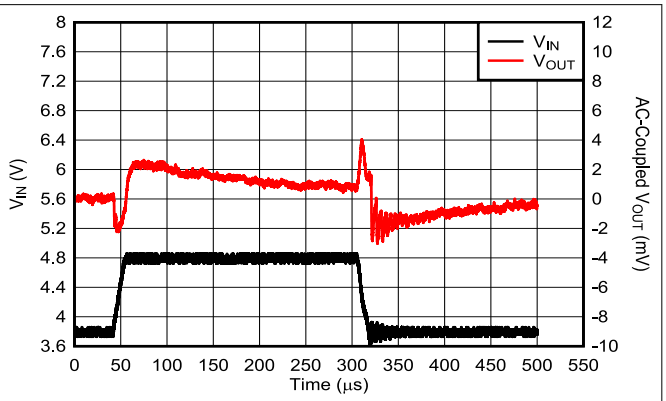


図 7-6. TPS79328 Line Transient Response

7.2.3 Application Curves (continued)

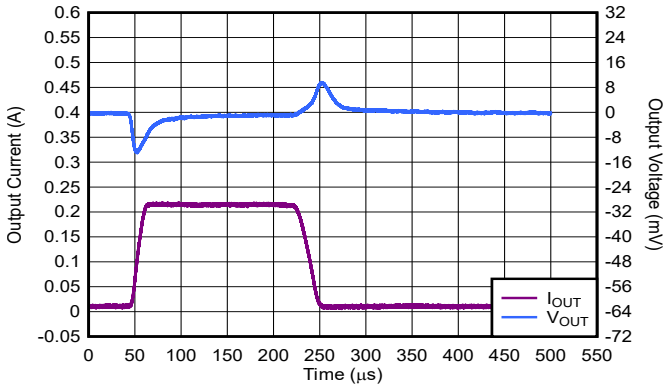


図 7-7. TPS79328 Load Transient Response

7.3 Best Design Practices

Do place at least one, low ESR, 2.2µF capacitor as close as possible between the OUT pin of the regulator and the GND pin.

Do place at least one, low ESR, 0.1µF capacitor as close as possible between the IN pin of the regulator and the GND pin.

Do provide adequate thermal paths away from the device.

Do not place the input or output capacitor more than 10mm away from the regulator.

Do not exceed the absolute maximum ratings.

Do not float the Enable (EN) pin.

Do not resistively or inductively load the NR pin.

Do not let the output voltage get more than 0.3V above the input voltage.

7.4 Power Supply Recommendations

These devices are designed to operate from an input voltage supply range from 2.7V to 5.5V. The input voltage range must provide adequate headroom for the device to have a regulated output. This input supply must be well-regulated and stable. A 0.1µF input capacitor is required for stability (legacy chip) or a 1µF (new chip); if the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

7.5 Layout

7.5.1 Layout Guidelines

Layout is a critical part of good power-supply design. There are several signal paths that conduct fast-changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power-supply performance. To help eliminate these problems, the IN pin must be bypassed to ground with a low ESR ceramic bypass capacitor with an X5R or X7R dielectric.

Equivalent series inductance (ESL) and equivalent series resistance (ESR) must be minimized to maximize performance and provide stability. Every capacitor (C_{IN}, C_{OUT}, $C_{NR/SS}$, C_{FF}) must be placed as close as possible to the device and on the same side of the PCB as the regulator.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because these circuits can impact system performance negatively, and even cause instability.

7.5.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve ac measurements like PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor must connect directly to the GND pin of the device.

7.5.1.2 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the *Thermal Information* table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) can be approximated by the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}), as shown in 式 4.

Where:

- $T_J$max is the maximum allowable junction temperature.
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package.
- T_A is the ambient temperature.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \tag{4}$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation triggers the thermal protection circuit.

図 7-8 shows the maximum ambient temperature versus the power dissipation of the TPS730. This figure assumes the device is soldered on a JEDEC standard, high-K layout with no airflow over the board. Actual board thermal impedances vary widely. If the application requires high power dissipation, having a thorough understanding of the board temperature and thermal impedances is helpful to verify the TPS730 does not operate above a junction temperature of 125°C.

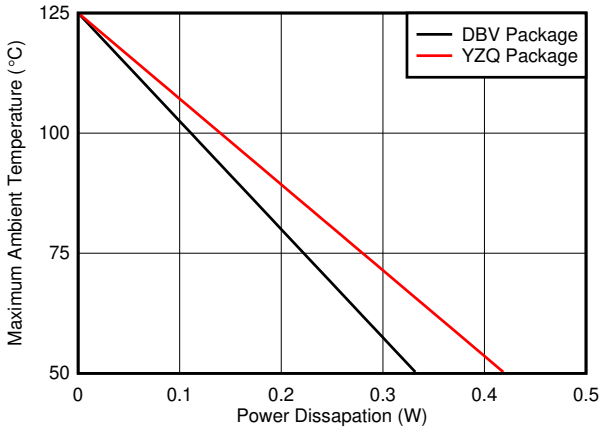


図 7-8. Maximum Ambient Temperature vs Power Dissipation

Estimating the junction temperature can be done by using the thermal metrics Ψ_{JT} and Ψ_{JB}, shown in the *Thermal Information* table. These metrics are a more accurate representation of the heat transfer characteristics of the die and the package than $R_{\theta JA}$. The junction temperature can be estimated with 式 5.

$$\Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \bullet P_D$$
$$\Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \bullet P_D \tag{5}$$

where

- P_D is the power dissipation shown by 式 4.
- T_T is the temperature at the center-top of the IC package.
- T_B is the PCB temperature measured 1 mm away from the IC package *on the PCB surface*.

注

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see the application note *Using New Thermal Metrics* (SBVA025), available for download at www.ti.com.

7.5.2 Layout Example

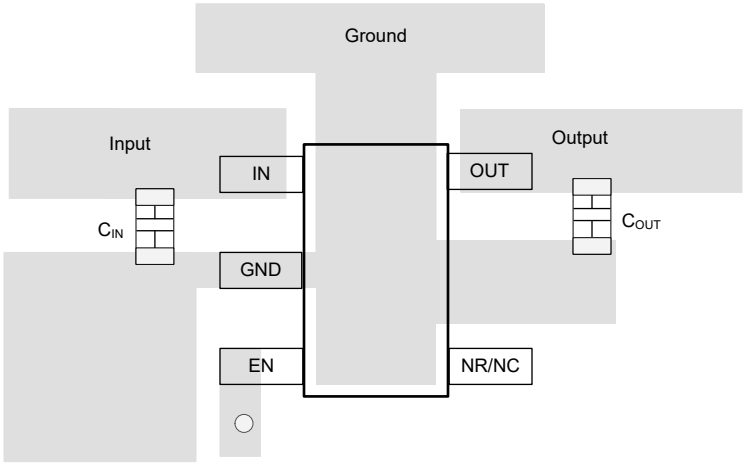


図 7-9. Layout Example (DBV Package, New Chip)

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 Evaluation Modules

Seven evaluation modules (EVMs) are available to assist in the initial circuit performance evaluation using the TPS793:

- TPS79301EVM
- TPS79318YEQEVM
- TPS79325YEQEVM
- TPS793285YEQEVM
- TPS79328EVM
- TPS79328YEQEVM
- TPS79330YEQEVM

These EVMs can be requested at the Texas Instruments website through the device product folders or purchased directly from the TI eStore.

8.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS793 is available through the product folders under *Tools & Software*.

8.1.2 Device Nomenclature

表 8-1. Ordering Information (1) (2)

PRODUCT	V_{OUT}
TPS793xx ***yyy*M3** *z*	**XX(X)** is the nominal output voltage (for example, 28 = 2.8 V; 285 = 2.85 V; 01 = adjustable version). **YYY** is the package designator. **M3** is a suffix designator for the devices that only use the latest manufacturing flow (CSO:RFB). Devices without this suffix can ship with the legacy chip (CSO:DLN) or the new chip (CSO:RFB). The reel packaging label provides CSO information to distinguish which chip is being used. **Z** is the package quantity. R is for reel (3000 pieces), T is for tape (250 pieces).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
(2) Output voltages from 1.2 V to 4.8 V in 50-mV increments are available. Contact the factory for details and availability.

8.2 Documentation Support

8.2.1 Related Documentation

- Application note, *Using New Thermal Metrics*, SBVA025.
- Application note, *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator*, SBVA042.
- *TPS793xxYEQEVM User's Guide*, SBVU001.
- *TPS79301EVM, TPS79328EVM LDO Linear Regulator Evaluation Module User's Guide*, SLVU060A.

8.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.4 サポート・リソース

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8.7 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision M (December 2024) to Revision N (January 2025)	Page
• Added *New Chip* to *Layout Example (DBV Package)* figure caption	27

Changes from Revision L (March 2015) to Revision M (December 2024)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新	1
• 現在のファミリのフォーマットに合わせてドキュメント全体を変更	1
• ドキュメントに M3 デバイスを追加	1
• Added NC/NR pin	3
• Updated Pin Description table to include new chip and legacy chip descriptions	3
• Added suggestion to look at TPS7A20 for lower noise performance	3
• Updated *Layout* section image	25

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS79301DBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGVI
TPS79301DBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGVI
TPS79301DBVRG4	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGVI
TPS79301DBVRG4.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGVI
TPS79301DBVRM3	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PGVI
TPS79301DBVT	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGVI
TPS79301DBVT.A	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGVI
TPS79318DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PHHI
TPS79318DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PHHI
TPS79318DBVRG4	NRND	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHHI
TPS79318DBVRG4.A	NRND	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHHI
TPS79318DBVRM3	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PHHI
TPS79318DBVT	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 125	PHHI
TPS79325DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PGWI
TPS79325DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PGWI
TPS79325DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGWI
TPS79325DBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGWI
TPS79325DBVRM3	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PGWI
TPS793285DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHII
TPS793285DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHII
TPS79328DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PGXI
TPS79328DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PGXI
TPS79328DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGXI
TPS79328DBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGXI
TPS79328DBVRM3	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PGXI
TPS79330DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PGYI
TPS79330DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PGYI
TPS79330DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGYI
TPS79330DBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGYI

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS79330DBVRM3	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PGYI
TPS79330DBVRM3.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PGYI
TPS79333DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PHUI
TPS79333DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PHUI
TPS79333DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHUI
TPS79333DBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHUI
TPS79333DBVRM3	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PHUI
TPS79333DBVRM3.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PHUI
TPS793475DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHJI
TPS793475DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHJI

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS793 :

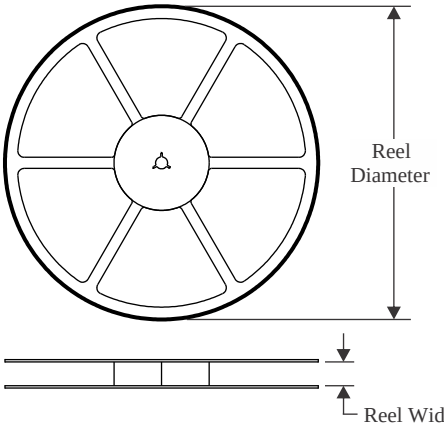
- Automotive : TPS793-Q1

NOTE: Qualified Version Definitions:

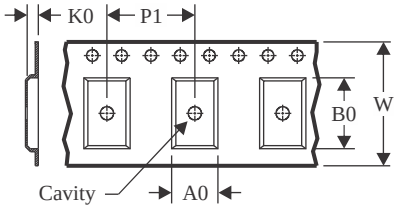
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

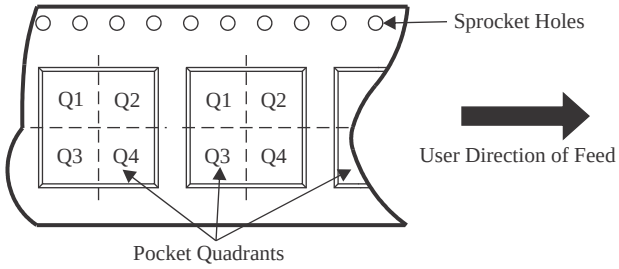


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

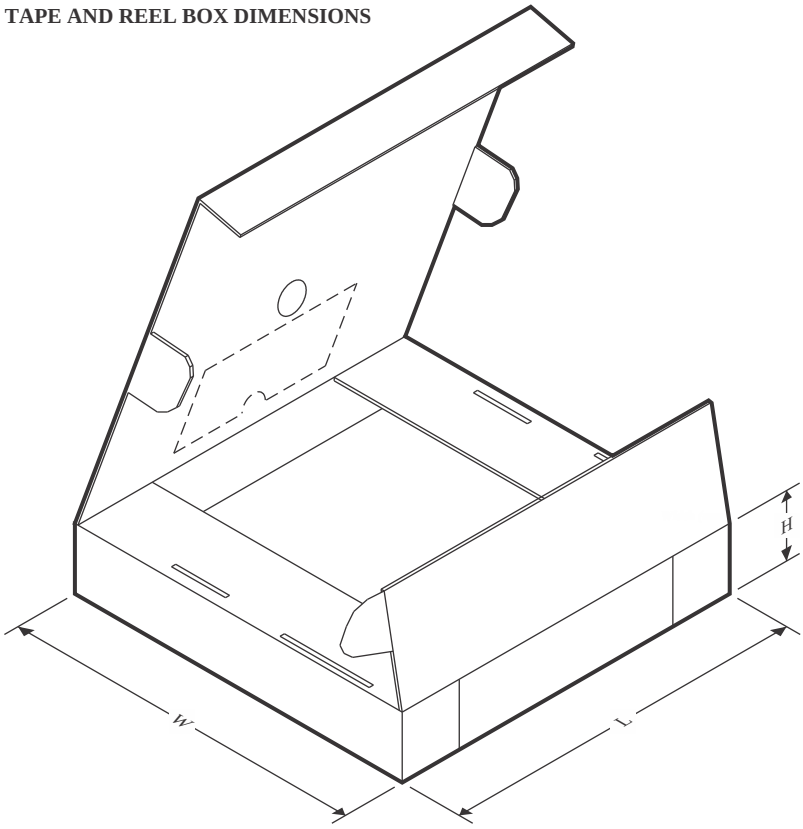


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS79301DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS79301DBVRG4	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS79301DBVRM3	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79301DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS79318DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS79318DBVRM3	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79325DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79325DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS79325DBVRM3	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS793285DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS79328DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79328DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS79328DBVRM3	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79330DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79330DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS79330DBVRM3	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS79333DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79333DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS79333DBVRG4	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79333DBVRG4	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79333DBVRM3	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS793475DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS79301DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS79301DBVRG4	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS79301DBVRM3	SOT-23	DBV	6	3000	210.0	185.0	35.0
TPS79301DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
TPS79318DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS79318DBVRM3	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS79325DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS79325DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS79325DBVRM3	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS793285DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS79328DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS79328DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS79328DBVRM3	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS79330DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS79330DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS79330DBVRM3	SOT-23	DBV	5	3000	208.0	191.0	35.0
TPS79333DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS79333DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0

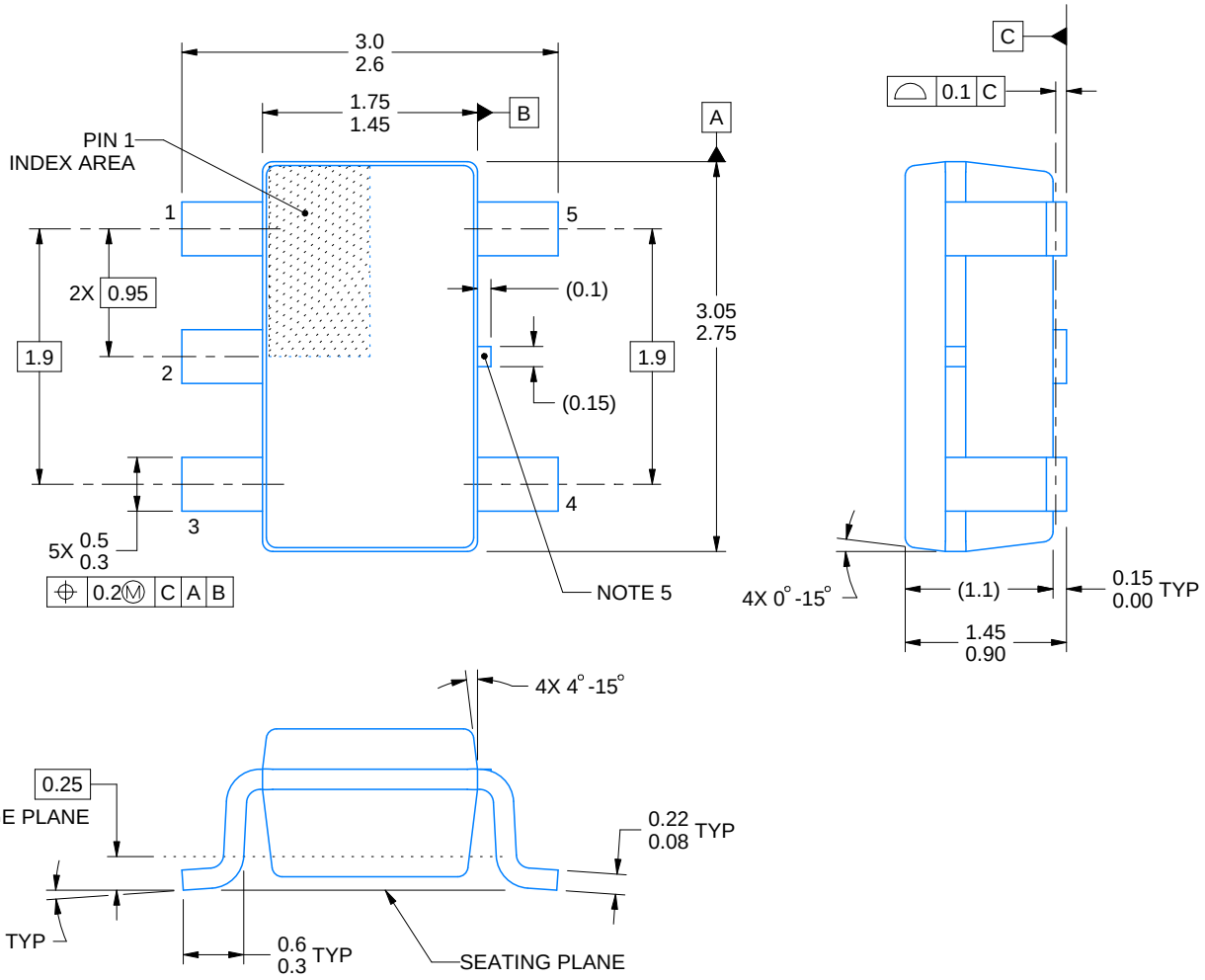
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS79333DBVRG4	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS79333DBVRG4	SOT-23	DBV	5	3000	203.0	203.0	35.0
TPS79333DBVRM3	SOT-23	DBV	5	3000	208.0	191.0	35.0
TPS793475DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

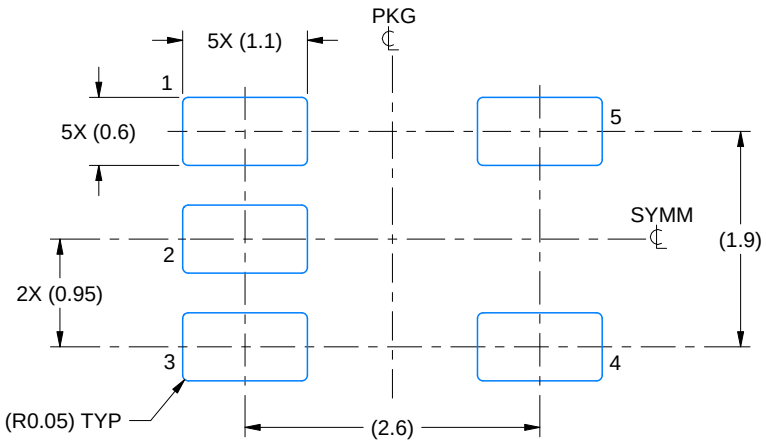
SMALL OUTLINE TRANSISTOR



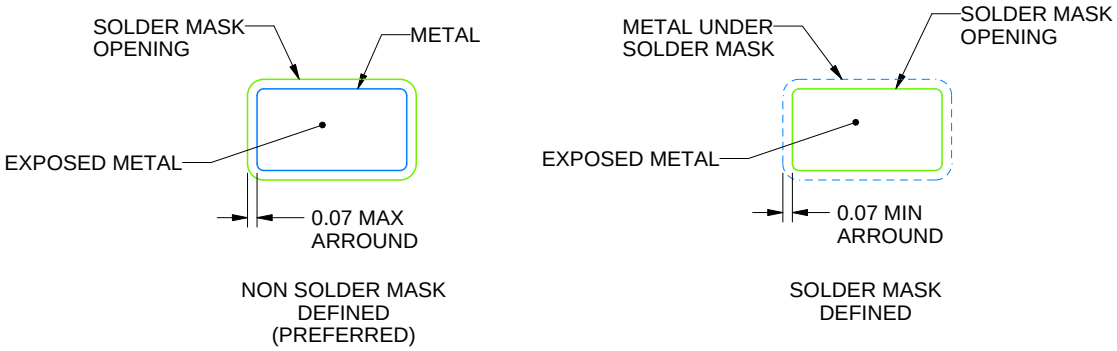
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

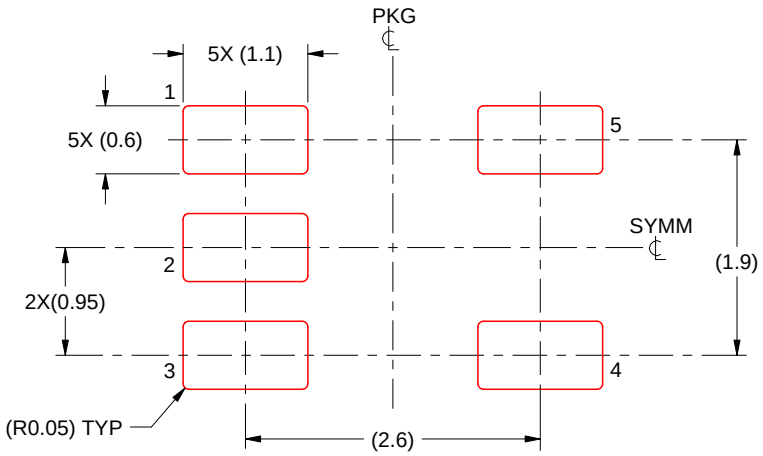


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

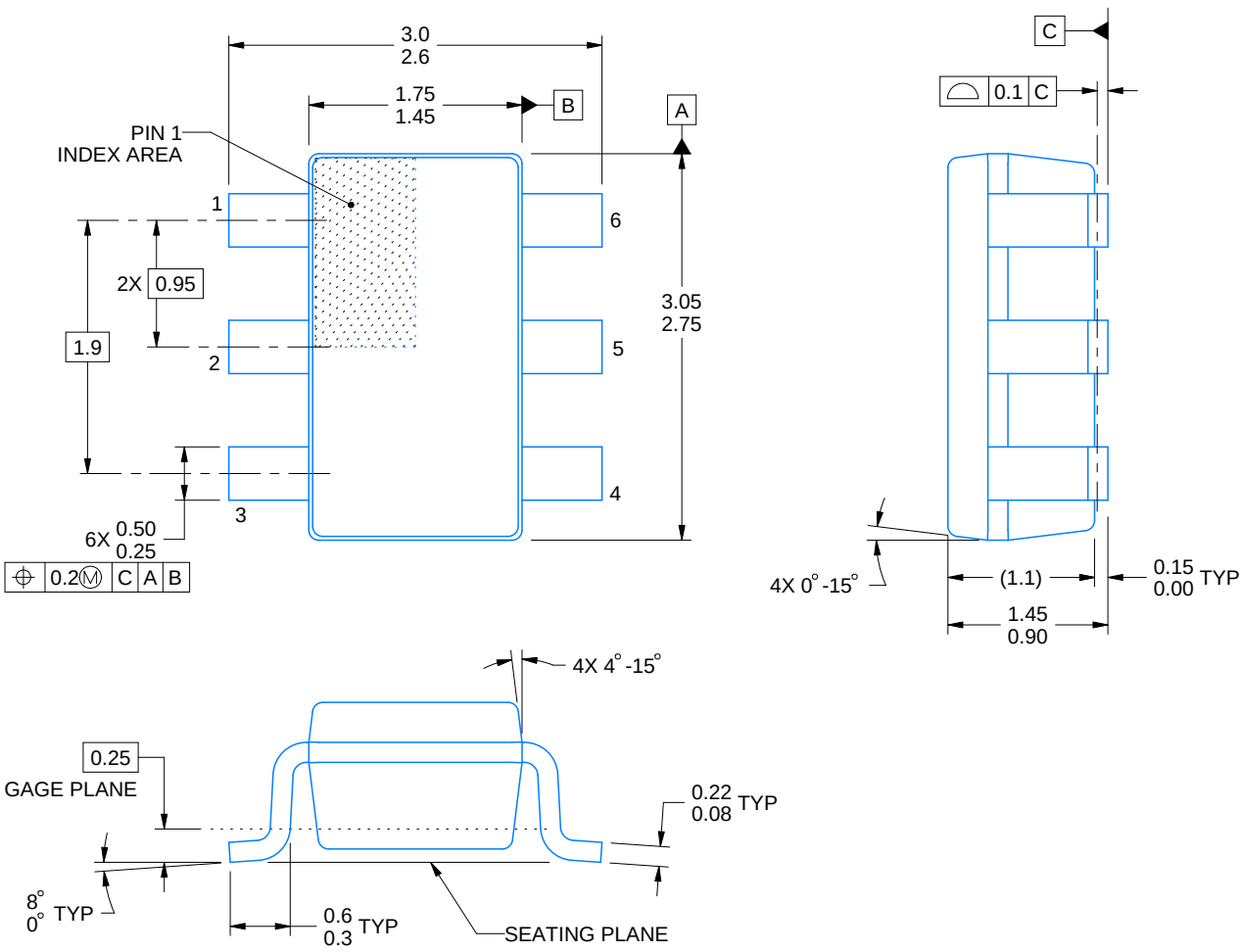
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

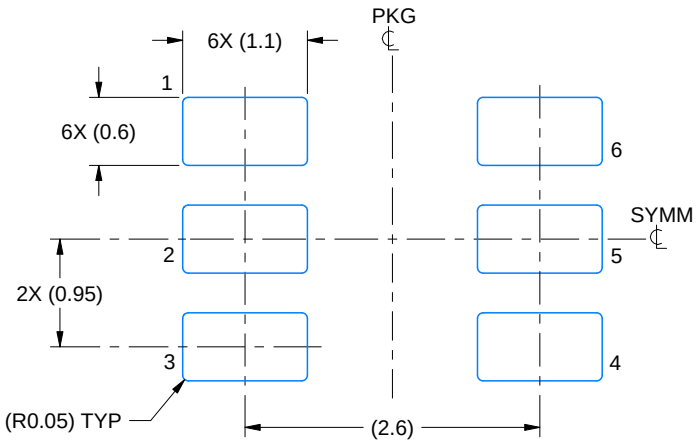
SMALL OUTLINE TRANSISTOR



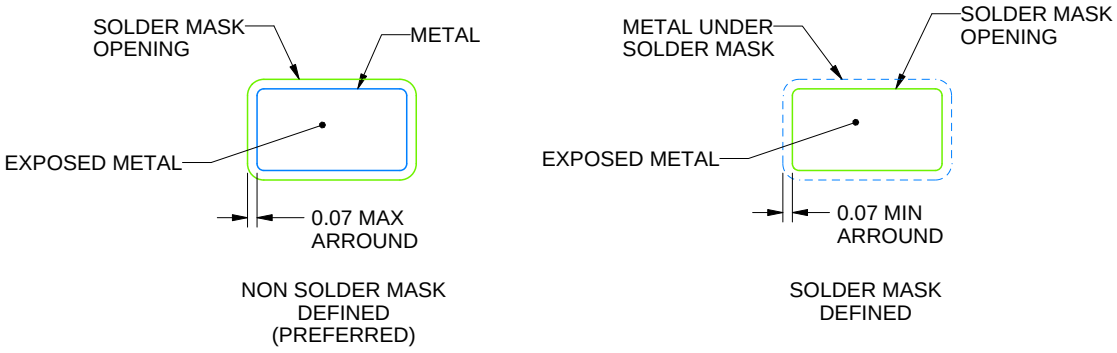
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

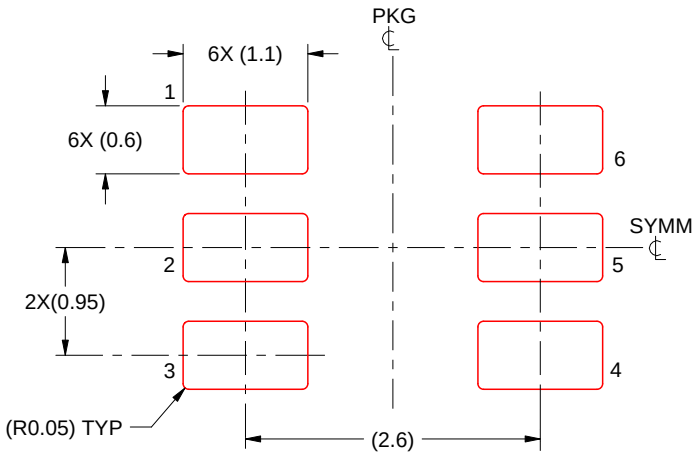


SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月