TPS7A25 パワー・グッド搭載、300mA、18V、超低静止電流 (I_Q)、低ドロップアウト・リニア電圧レギュレータ

1 特長

- きわめて小さい I_Q:2µA
- 入力電圧:2.4V～18V
- 出力電圧オプションを選択可能:
  - 固定:1.25V～5.0V
  - 可変:1.24V～17.66V
- 温度範囲全体で 1% の精度
- 低ドロップアウト:300mA のとき 340mV (最大値)
- オープン・ドレインのパワー・グッド出力
- サーマル・シャットダウン機能と過電流保護機能
- アクティブなオーバーシュート・プルダウン
- 動作時接合部温度:-40℃～+125℃
- 1µF の出力コンデンサで安定動作
- パッケージ:6 ピン WSON

2 アプリケーション

- ホーム / ビルディング・オートメーション
- マルチセルのパワー・バンク
- スマート・グリッドおよび計量
- 携帯用電動工具
- モーター・ドライブ
- 白物家電
- 携帯型家電機器

3 概要

TPS7A25 低ドロップアウト (LDO) リニア電圧レギュレータは、2.4V～18V の入力電圧と、非常に低い静止電流 (I_Q) が特長です。これらの特長は、現代の家電製品がますます厳しくなるエネルギー要件を満たすために役立つほか、携帯電源ソリューションでのバッテリ駆動時間も延長できます。

TPS7A25 には、固定電圧バージョンと可変電圧バージョンがあります。出力電圧をより柔軟にしたい場合や、高い出力電圧が必要な場合は、可変電圧バージョンで帰還抵抗を使って、出力電圧を 1.24V～17.64V の範囲に設定できます。どちらのバージョンも 1% の出力レギュレーション精度を備え、ほとんどのマイクロコントローラ (MCU) のリファレンス電圧に使用できる高精度のレギュレーションを行えます。

TPS7A25 LDO は、300mA の電流で最大ドロップアウト電圧が 340mV 未満なので、標準のリニア・レギュレータよりも効率的に動作します。この最大ドロップアウト電圧により、5.4V の入力電圧 (V_{IN}) から 5.0V の出力電圧 (V_{OUT}) で 92.5% の効率を実現できます。

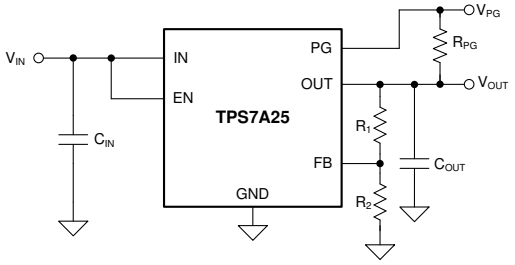
パワー・グッド (PG) インジケータを使用して、電源が正常になるまで MCU をリセット状態に保持したり、シーケンシングを実行したりできます。PG ピンはオープン・ドレイン出力なので、このピンは V_{OUT} 以外のレールによる監視のため、簡単にレベル・シフトが可能です。電流制限およびサーマル・シャットダウン機能が組み込まれているため、負荷の短絡やフォルト時にもレギュレータが保護されます。

より大きい出力電流を必要とする場合は、TPS7A26 を検討してください。

パッケージ情報 (1)

部品番号	パッケージ	本体サイズ (公称)
TPS7A25	DRV (WSON、6)	2.00mm × 2.00mm

(1) 利用可能なパッケージについては、データシートの末尾にあるパッケージ・オプションについての付録を参照してください。



代表的なアプリケーション回路

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (August 2019) to Revision C (December 2022) — **Page**

- 「*出力電圧オプション*」の項目の最大値を変更：固定電圧バージョンを 5.5V から 5.0V に変更 ... 1
- Added Vout abs max ratings for fixed version ... 4

Changes from Revision A (March 2019) to Revision B (August 2019) — **Page**

- 「*出力電圧オプション*」の項目の最大値を変更：固定電圧バージョンを 5V から 5.5V に変更、可変電圧バージョンを 17.64V から 17.66V に変更 ... 1
- 「概要」セクションを変更：第 2 段落から固定電圧バージョンの文を削除、360mV を 340mV に変更、最後の段落を追加 ... 1
- Added fixed version to *Pin Configuration and Functions* section ... 3
- Added accuracy for fixed output options ... 6
- Added *Fixed Version* image to *Functional Block Diagrams* section ... 13
- Added *Active* to *Active Overshoot Pulldown Circuitry* section title ... 16
- Added *Fixed Version Layout Example* figure ... 24

5 Pin Configuration and Functions

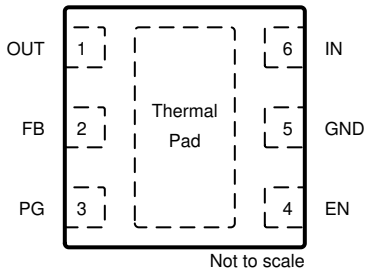


図 5-1. TPS7A25: DRV Package (Adjustable), 6-Pin WSON (Top View)

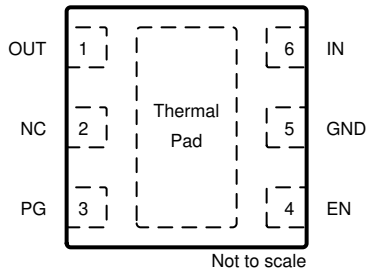


図 5-2. TPS7A25: DRV Package (Fixed), 6-Pin WSON (Top View)

表 5-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	DRV (Adjustable)	DRV (Fixed)		
EN	4	4	Input	Enable pin. Drive EN greater than $V_{EN(HI)}$ to enable the regulator. Drive EN less than $V_{EN(LOW)}$ to put the regulator into low-current shutdown. Do not float this pin. If not used, connect EN to IN.
FB	2	—	Input	Feedback pin. Input to the control-loop error amplifier. This pin is used to set the output voltage of the device with the use of external resistors. For adjustable-voltage version devices only.
GND	5	5	—	Ground pin.
IN	6	6	Input	Input pin. For best transient response and to minimize input impedance, use the recommended value or larger capacitor from IN to ground as listed in the *Recommended Operating Conditions* table. Place the input capacitor as close to the IN and GND pins of the device as possible.
NC	—	2	—	No internal connection. For fixed-voltage version devices only. This pin can be floated but the device will have better thermal performance with this pin tied to GND.
OUT	1	1	Output	Output pin. A capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger capacitor from OUT to ground. Follow the recommended capacitor value as listed in the *Recommended Operating Conditions* table. Place the output capacitor as close to the OUT and GND pins of the device as possible.
PG	3	3	Output	Power-good pin; open-collector output. Pullup externally to the OUT pin or another voltage rail. The PG pin goes high when $V_{OUT} > V_{IT(PG,RISING)}$ in the *Electrical Characteristics* table. The PG pin is driven low when $V_{OUT} < V_{IT(PG,FALLING)}$ in the *Electrical Characteristics* table. If not used this pin can be floated but the device will have better thermal performance with this pin tied to GND.
Thermal pad	Pad	Pad	—	Exposed pad of the package. Connect this pad to ground or leave floating. Connect the thermal pad to a large-area ground plane for best thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	V_{IN}	–0.3	20	V
	V_{OUT} (adjustable version)	–0.3	V_{IN} + 0.3(3)	
	V_{OUT} (fixed version)	–0.3	5.5	
	V_{FB}	–0.3	5.5	
	V_{EN}	–0.3	20	
	V_{PG}	–0.3	20	
Current	Maximum output	Internally limited		A
Temperature	Operating junction, T_J	–50	150	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages with respect to GND.
(3) V_{IN} + 0.3 V or 20 V (whichever is smaller).

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 2-kV HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 500-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.4		18	V
V_{OUT}	Output voltage (adjustable version)	1.24		18 - V_{DO}	V
V_{OUT}	Output voltage (fixed version)	1.25		5.0	V
I_{OUT}	Output current	0		300	mA
V_{EN}	Enable voltage	0		18	V
V_{PG} (1)	Power-good voltage	0		18	V
C_{IN} (2)	Input capacitor		1		µF
C_{OUT} (2)	Output capacitor	1	2.2	100	µF
T_J	Operating junction temperature	–40		125	°C

(1) Select pullup resistor to limit PG pin sink current when PG output is driven low. See the *Power Good* section for details.
(2) All capacitor values are assumed to derate to 50% of the nominal capacitor value.

6.4 Thermal Information

THERMAL METRIC(1)		TPS7A25 DRV (WSON) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	90.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	38.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	38.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	14.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

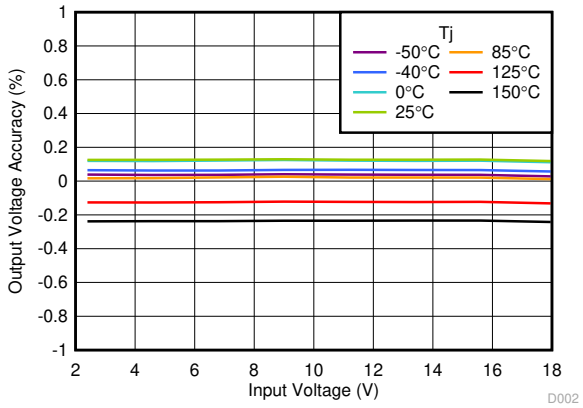
specified at T_J = –40°C to + 125°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V or V_{IN} = 2.4 V (whichever is greater), FB tied to OUT, I_{OUT} = 1 mA, V_{EN} = 2 V, and C_{IN} = 1 µF, C_{OUT} = 2.2 µF ceramic (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{UVLO(RISING)}$	UVLO threshold rising	V_{IN} rising	1.95	2.15	2.35	V
$V_{UVLO(HYS)}$	UVLO hysteresis			70		mV
$V_{UVLO(FALLING)}$	UVLO threshold falling	V_{IN} falling	1.85	2.09	2.25	V
V_{FB}	Feedback voltage	Adjustable version only		1.24		V
V_{OUT}	Output voltage accuracy	Adjustable version, V_{OUT} = V_{FB}	1.228	1.24	1.252	V
V_{OUT}	Output voltage accuracy	Fixed output versions	–1		1	%
$\Delta V_{OUT(\Delta VIN)}$	Line regulation(1)	($V_{OUT(nom)}$ + 0.5 V or 2.4 V) ≤ V_{IN} ≤ 18 V	–0.1		0.1	%
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	1 mA ≤ I_{OUT} ≤ 300 mA	–0.5		0.5	%
V_{DO}	Dropout voltage(2)	I_{OUT} = 50 mA		64	105	mV
		I_{OUT} = 150 mA		120	180	
		I_{OUT} = 300 mA		210	340	
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(nom)}$	325	510	720	mA
I_{GND}	Ground pin current	I_{OUT} = 0 mA		2	4.5	µA
		I_{OUT} = 1 mA		15		
$I_{SHUTDOWN}$	Shutdown current	V_{EN} ≤ 0.4 V, V_{IN} = 2.4 V, I_{out} = 0 mA		325	600	nA
I_{FB}	FB pin current			10		nA
I_{EN}	EN pin current	V_{EN} = 18 V		10		nA
$V_{EN(HI)}$	Enable pin high-level input voltage	Device enabled	0.9			V
$V_{EN(LOW)}$	Enable pin low-level input voltage	Device disabled			0.4	V
$V_{IT(PG,RISING)}$	PG pin threshold rising	R_{PULLUP} = 10 kΩ, V_{OUT} rising, V_{IN} ≥ $V_{UVLO(RISING)}$		93	96.5	%V_{OUT}
$V_{HYS(PG)}$	PG pin hysteresis	R_{PULLUP} = 10 kΩ, V_{OUT} falling, V_{IN} ≥ $V_{UVLO(RISING)}$		3		%V_{OUT}
$V_{IT(PG,FALLING)}$	PG pin threshold falling	R_{PULLUP} = 10 kΩ, V_{OUT} falling, V_{IN} ≥ $V_{UVLO(RISING)}$	84	90		%V_{OUT}
$V_{OL(PG)}$	PG pin low level output voltage	V_{OUT} < $V_{IT(PG,FALLING)}$, $I_{PG-SINK}$ = 500 µA			0.4	V
$I_{LKG(PG)}$	PG pin leakage current	V_{OUT} > $V_{IT(PG,RISING)}$, V_{PG} = 18 V		5	300	nA
PSRR	Power-supply rejection ratio	f = 10 Hz		75		dB
		f = 100 Hz		62		
		f = 1 kHz		52		
V_n	Output noise voltage	BW = 10 Hz to 100 kHz, V_{OUT} = 1.2 V		300		µV_{RMS}
$T_{SD(shutdown)}$	Thermal shutdown temperature	Shutdown, temperature increasing		165		°C
$T_{SD(reset)}$	Thermal shutdown reset temperature	Reset, temperature decreasing		145		°C

(1) $V_{out(nom)}$ + 0.5 V or 2.4 V (whichever is greater).
(2) V_{DO} is measured with V_{IN} = 0.97 × $V_{OUT(nom)}$ for fixed output voltage versions. V_{DO} is not measured for fixed output voltage versions when V_{OUT} ≤ 2.5 V. For the adjustable output device, V_{DO} is measured with V_{FB} = 0.97 × $V_{FB(nom)}$.

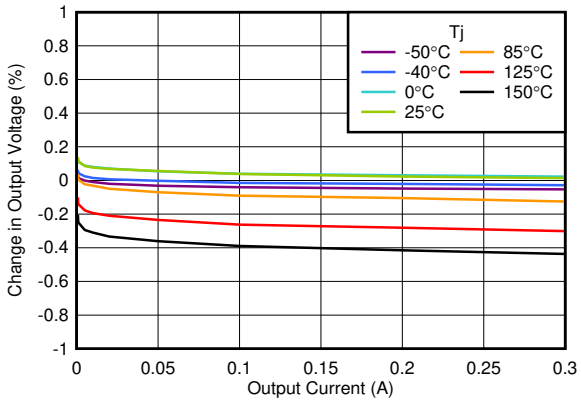
7 Typical Characteristics

at operating temperature T_J = 25°C, I_{OUT} = 1 mA, V_{EN} = 0.9 V, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, and V_{IN} = $V_{OUT(typ)}$ + 0.5 V or 2.4 V (whichever is greater), unless otherwise noted; typical values are at T_J = 25°C



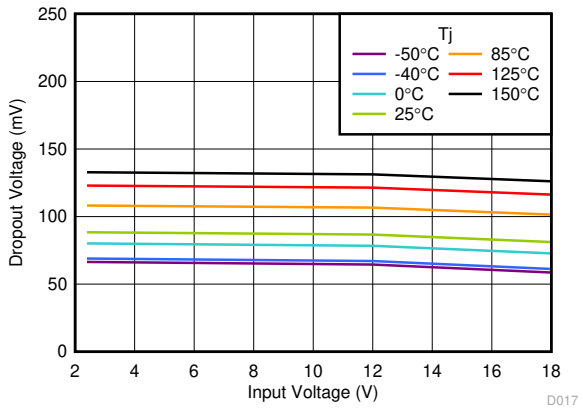
I_{OUT} = 1 mA

図 7-1. Line Regulation vs V_{IN}



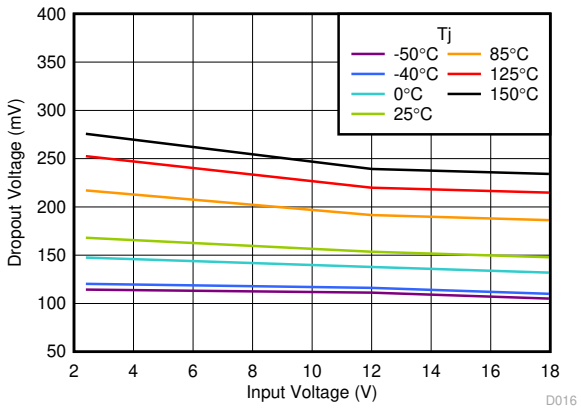
V_{OUT} = 1.24 V

図 7-2. Load Regulation vs I_{OUT}



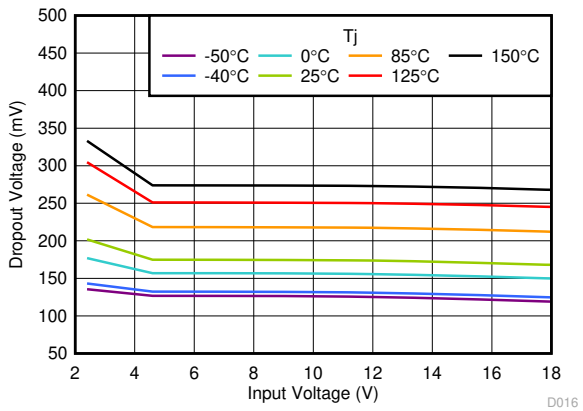
I_{OUT} = 100 mA

図 7-3. Dropout Voltage vs V_{IN}



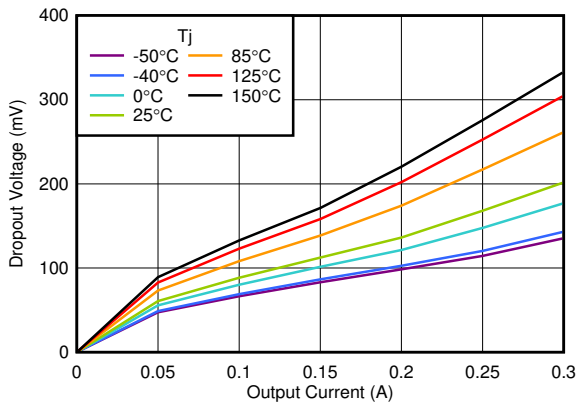
I_{OUT} = 250 mA

図 7-4. Dropout Voltage vs V_{IN}



I_{OUT} = 300 mA

図 7-5. Dropout Voltage vs V_{IN}

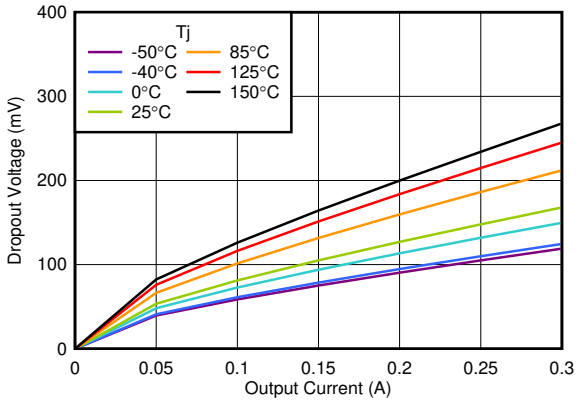


V_{IN} = 2.4 V

図 7-6. Dropout Voltage vs I_{IN}

7 Typical Characteristics (continued)

at operating temperature T_J = 25°C, I_{OUT} = 1 mA, V_{EN} = 0.9 V, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, and V_{IN} = $V_{OUT(typ)}$ + 0.5 V or 2.4 V (whichever is greater), unless otherwise noted; typical values are at T_J = 25°C



V_{IN} = 18 V

図 7-7. Dropout Voltage vs I_{OUT}

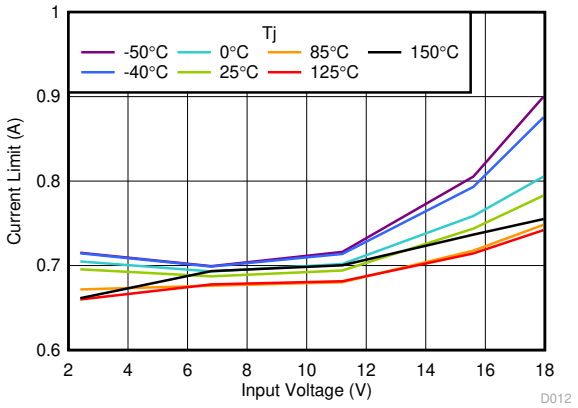
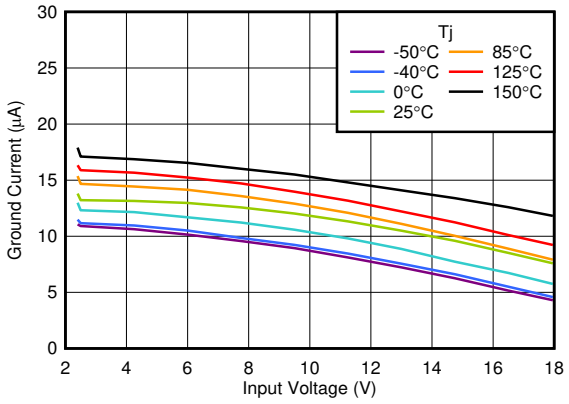
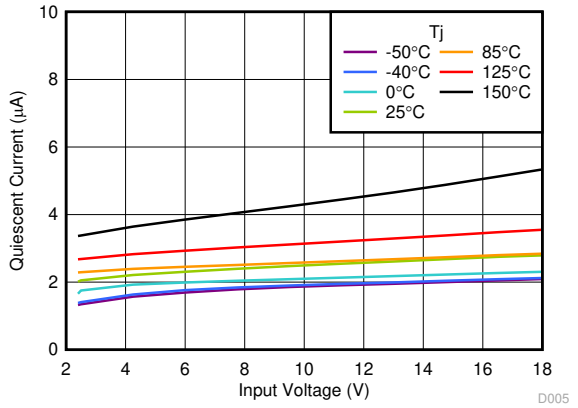


図 7-8. Current Limit vs V_{IN}



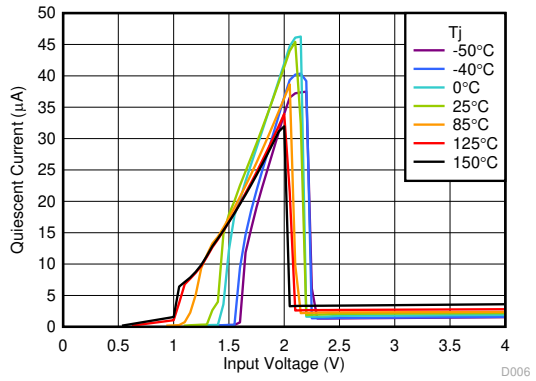
V_{OUT} = 1.24 V, I_{OUT} = 1 mA

図 7-9. I_{GND} vs V_{IN}



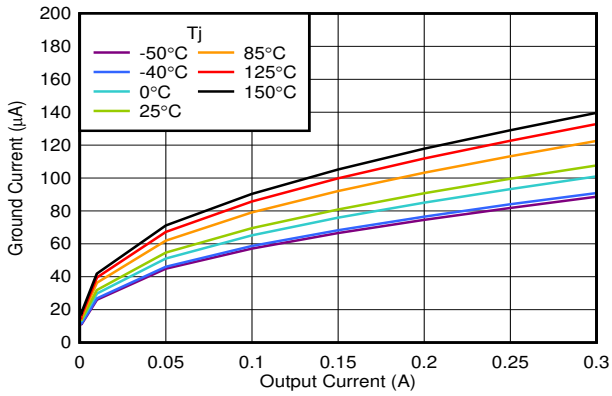
V_{OUT} = 1.24 V, I_{OUT} = 0 A

図 7-10. I_Q vs V_{IN}



V_{OUT} = 1.24 V, I_{OUT} = 0 A

図 7-11. I_Q vs V_{IN}

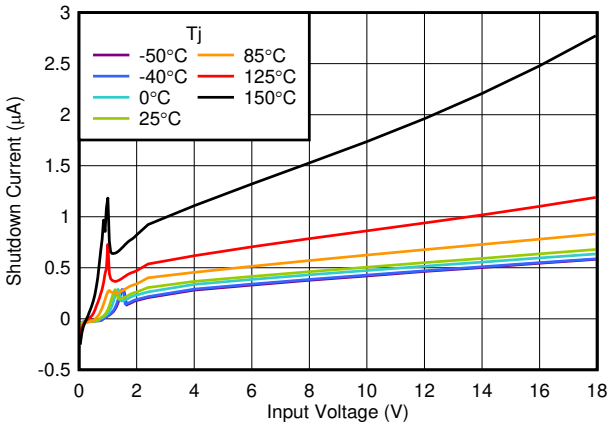


V_{OUT} = 1.24 V

図 7-12. I_{GND} vs I_{OUT}

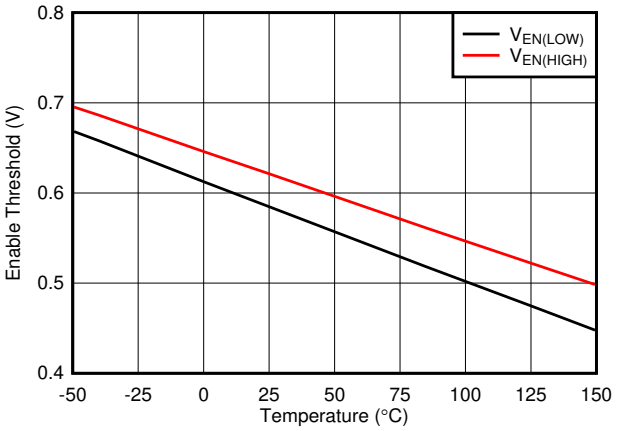
7 Typical Characteristics (continued)

at operating temperature T_J = 25°C, I_{OUT} = 1 mA, V_{EN} = 0.9 V, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, and V_{IN} = $V_{OUT(typ)}$ + 0.5 V or 2.4 V (whichever is greater), unless otherwise noted; typical values are at T_J = 25°C



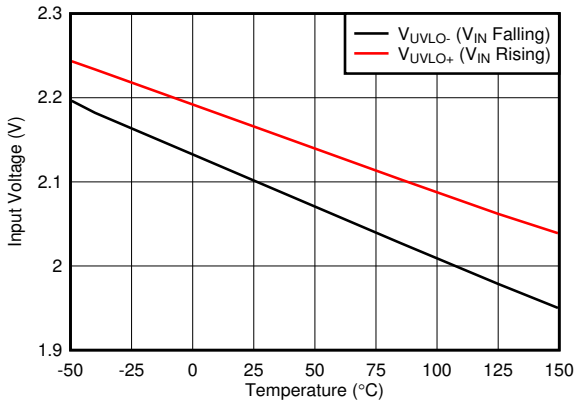
V_{OUT} = 1.24 V

図 7-13. Shutdown Current vs V_{IN}



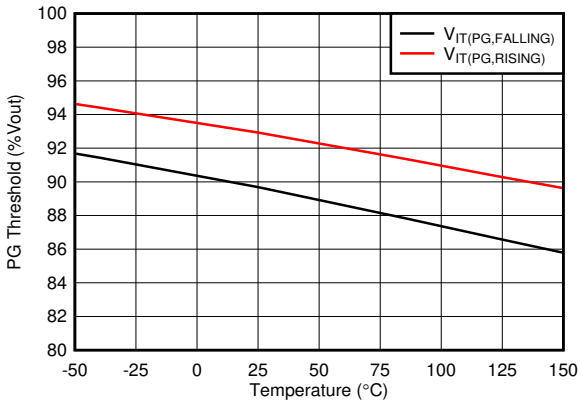
V_{OUT} = 1.24 V, 2.4 V ≤ V_{IN} ≤ 18 V

図 7-14. V_{EN} Thresholds vs Temperature



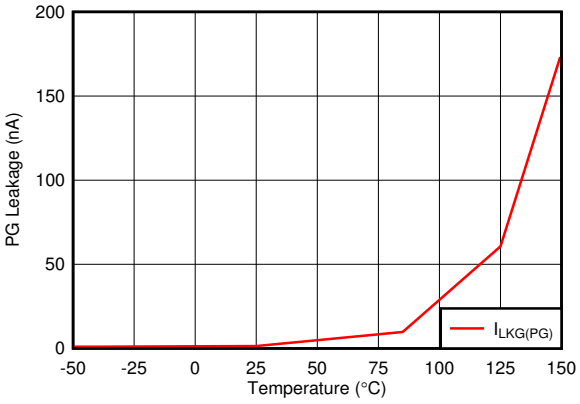
V_{OUT} = 1.24 V, I_{OUT} = 1 mA

図 7-15. UVLO Thresholds vs Temperature



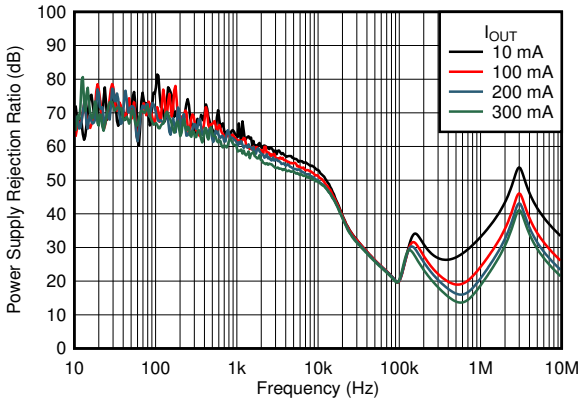
V_{OUT} = 1.24 V

図 7-16. PG Thresholds vs Temperature



V_{OUT} = 1.24 V

図 7-17. PG Leakage Current vs Temperature

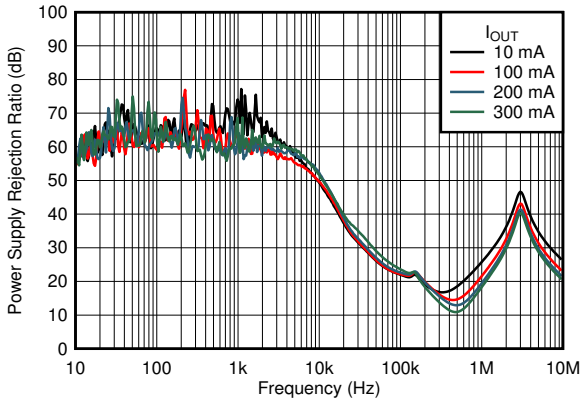


V_{OUT} = 1.24 V, C_{IN} = 0 µF, C_{OUT} = 1 µF, C_{FF} = 10 nF

図 7-18. PSRR vs Frequency and I_{OUT}

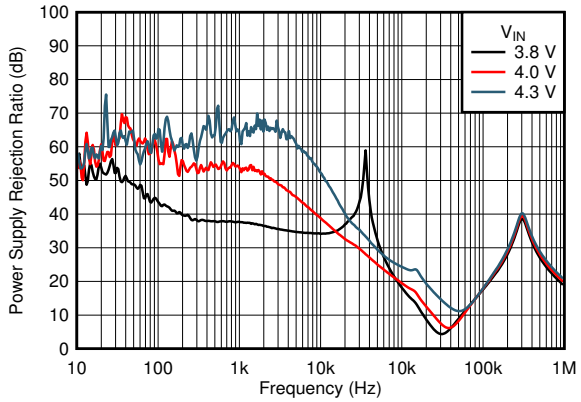
7 Typical Characteristics (continued)

at operating temperature T_J = 25°C, I_{OUT} = 1 mA, V_{EN} = 0.9 V, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, and V_{IN} = $V_{OUT(typ)}$ + 0.5 V or 2.4 V (whichever is greater), unless otherwise noted; typical values are at T_J = 25°C



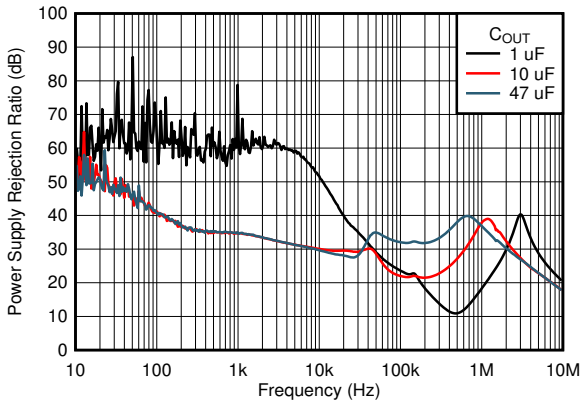
V_{OUT} = 3.3 V, V_{IN} = 4.3 V, C_{IN} = 0 µF, C_{OUT} = 1 µF, C_{FF} = 10 nF

図 7-19. PSRR vs Frequency and I_{OUT}



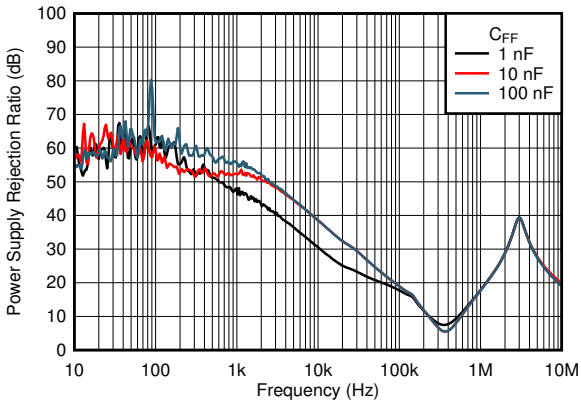
V_{OUT} = 3.3 V, I_{OUT} = 0.3 A, C_{IN} = 0 µF, C_{OUT} = 1 µF, C_{FF} = 10 nF

図 7-20. PSRR vs Frequency and V_{IN}



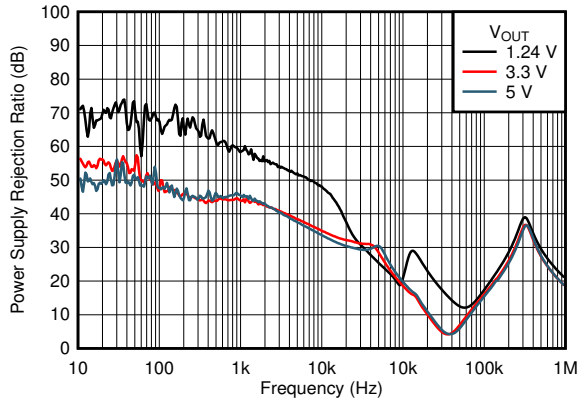
V_{OUT} = 3.3 V, V_{IN} = 4.3 V, I_{OUT} = 0.3 A, C_{IN} = 0 µF, C_{FF} = 10 nF

図 7-21. PSRR vs Frequency and C_{OUT}



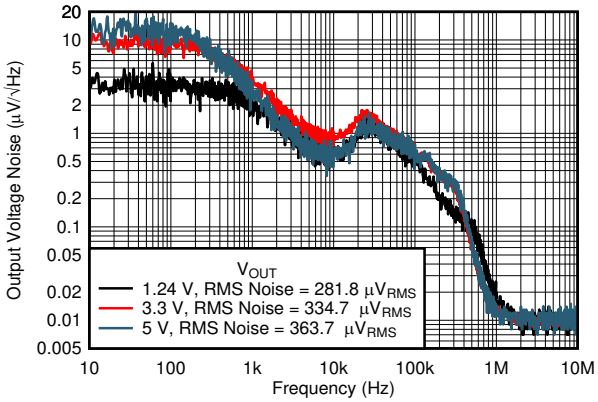
V_{OUT} = 3.3 V, V_{IN} = 4.3 V, I_{OUT} = 0.3 A, C_{IN} = 0 µF, C_{OUT} = 1 µF

図 7-22. PSRR vs Frequency and C_{FF}



V_{IN} = V_{OUT} + 1 V or 2.4 V (whichever is greater), I_{OUT} = 0.3 A, C_{IN} = 0 µF, C_{OUT} = 1 µF, C_{FF} = 10 nF

図 7-23. PSRR vs Frequency and V_{OUT}

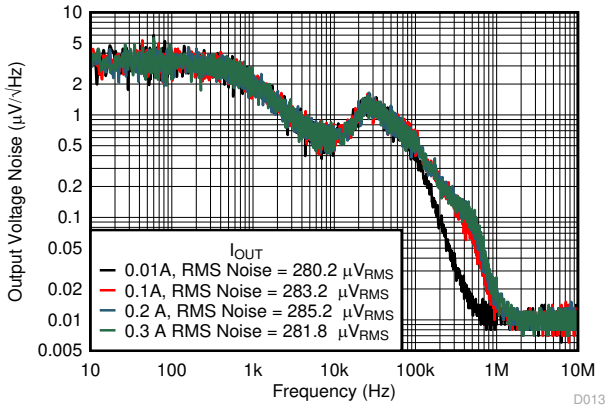


V_{IN} = V_{OUT} + 1 V or 2.4 V (whichever is greater), I_{OUT} = 0.3 A, C_{IN} = 1 µF, C_{OUT} = 1 µF, C_{FF} = 10 nF, V_{RMS} BW = 10 Hz to 100 kHz

図 7-24. Output Noise (V_n) vs Frequency and V_{OUT}

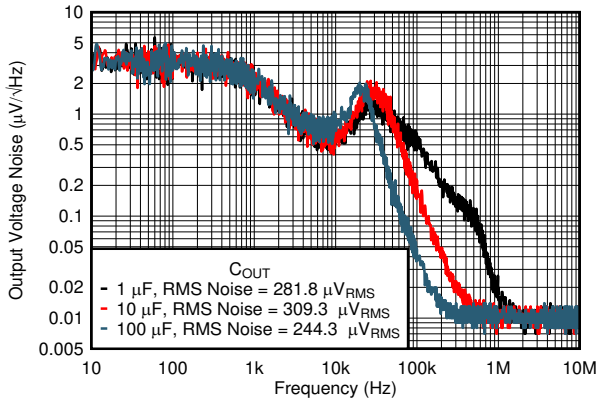
7 Typical Characteristics (continued)

at operating temperature T_J = 25°C, I_{OUT} = 1 mA, V_{EN} = 0.9 V, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, and V_{IN} = $V_{OUT(typ)}$ + 0.5 V or 2.4 V (whichever is greater), unless otherwise noted; typical values are at T_J = 25°C



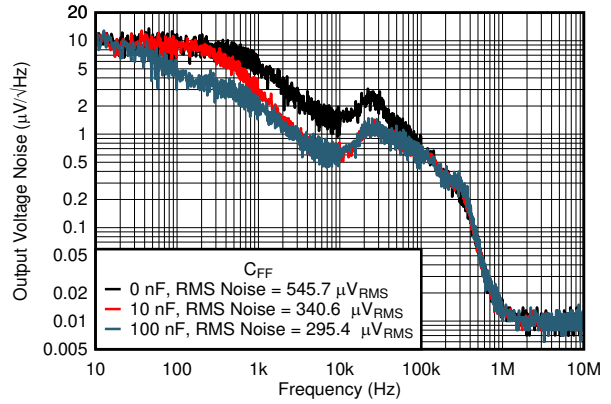
V_{OUT} = 1.24 V, C_{IN} = 1 µF, C_{OUT} = 1 µF, C_{FF} = 10 nF, V_{RMS} BW = 10 Hz to 100 kHz

図 7-25. Output Noise (V_n) vs Frequency and I_{OUT}



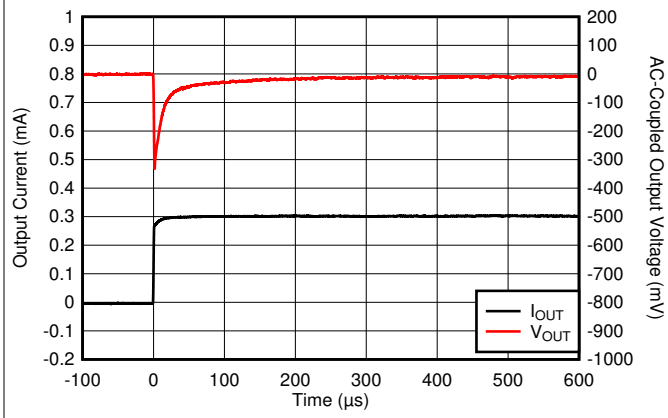
V_{OUT} = 1.24 V, V_{IN} = 2.4 V, I_{OUT} = 0.3 A, C_{IN} = 1 µF, C_{FF} = 10 nF, V_{RMS} BW = 10 Hz to 100 kHz

図 7-26. Output Noise (V_n) vs Frequency and C_{OUT}



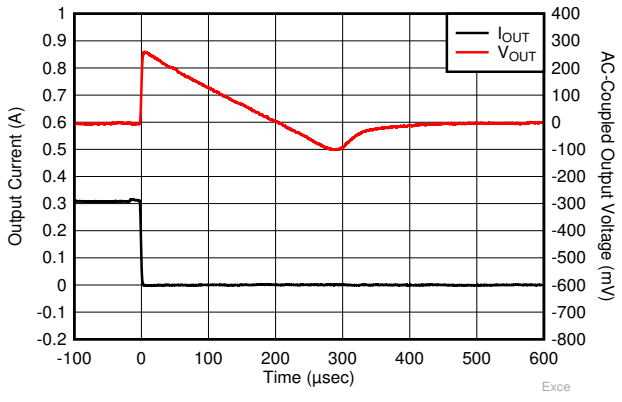
V_{OUT} = 3.3 V, V_{IN} = 4.3 V, I_{OUT} = 0.3 A, C_{IN} = 1 µF, C_{OUT} = 1 µF, V_{RMS} BW = 10 Hz to 100 kHz

図 7-27. Output Noise (V_n) vs Frequency and C_{FF}



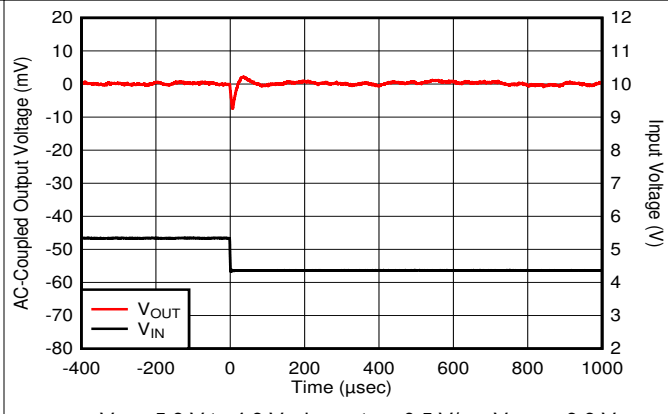
I_{OUT} = 0.001 A to 0.3 A, slew rate = 0.5 A/µs, V_{OUT} = 3.3 V, V_{IN} = 4.3 V, C_{IN} = 1 µF, C_{OUT} = 1 µF

図 7-28. Load Transient



I_{OUT} = 0.3 A to 0.001 mA, slew rate = 0.5 A/µs, V_{OUT} = 3.3 V, V_{IN} = 4.3 V, C_{IN} = 1 µF, C_{OUT} = 1 µF

図 7-29. Load Transient

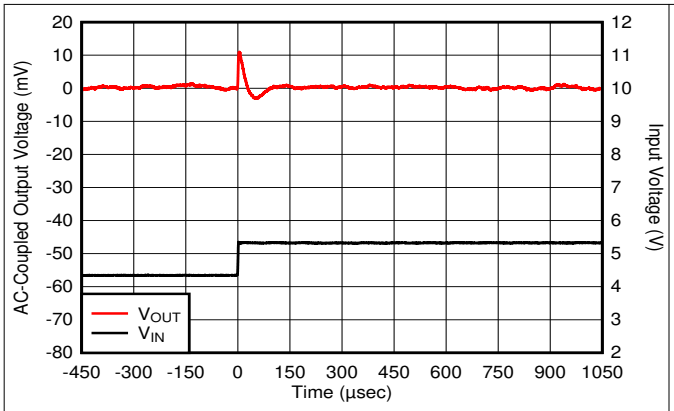


V_{IN} = 5.3 V to 4.3 V, slew rate = 0.5 V/µs, V_{OUT} = 3.3 V, I_{OUT} = 0.5 A, C_{IN} = 1 µF, C_{OUT} = 1 µF

図 7-30. Line Transient

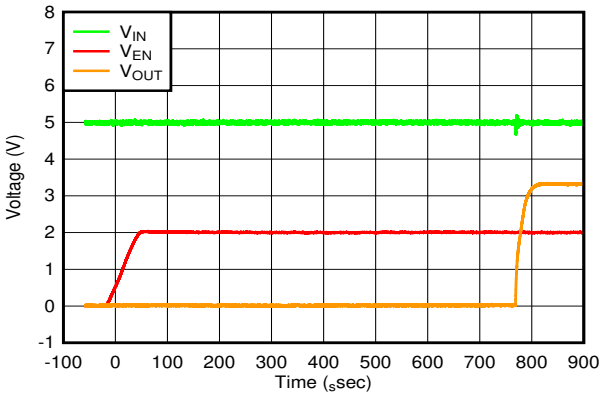
7 Typical Characteristics (continued)

at operating temperature T_J = 25°C, I_{OUT} = 1 mA, V_{EN} = 0.9 V, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, and V_{IN} = $V_{OUT(typ)}$ + 0.5 V or 2.4 V (whichever is greater), unless otherwise noted; typical values are at T_J = 25°C



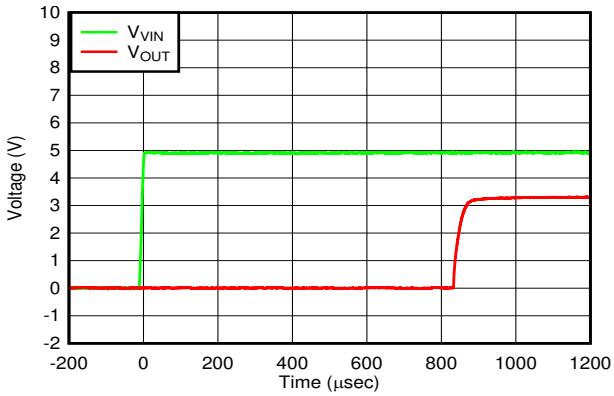
V_{IN} = 4.3 V to 5.3 V, slew rate = 0.5 V/µs, V_{OUT} = 3.3 V, I_{OUT} = 0.5 A, C_{IN} = 1 µF, C_{OUT} = 1 µF

図 7-31. Line Transient



V_{IN} = 5 V, V_{EN} = 0 V to 2 V, V_{OUT} = 3.3 V, I_{OUT} = 0.3 A, C_{IN} = 1 µF, C_{OUT} = 1 µF

図 7-32. Start-Up With Enable



V_{IN} = 0 V to 5 V, V_{EN} = V_{IN}, V_{OUT} = 3.3 V, I_{OUT} = 0.3 A, C_{IN} = 1 µF, C_{OUT} = 1 µF

図 7-33. Start-Up With Enable Pin Tied to Input

8 Detailed Description

8.1 Overview

The TPS7A25 is an 18-V, low quiescent current, low-dropout (LDO) linear regulator. The low I_Q performance makes the TPS7A25 an excellent choice for battery-powered or line-power applications that are expected to meet increasingly stringent standby-power standards.

The 1% accuracy over temperature and power-good indication make this device an excellent choice for meeting a wide range of microcontroller power requirements. Additionally, the TPS7A25 has an internal soft-start to minimize inrush current into the output capacitance.

For increased reliability, the TPS7A25 also incorporates overcurrent, overshoot pulldown, and thermal shutdown protection. The operating junction temperature is –40°C to +125°C, and adds margin for applications concerned with higher working ambient temperatures.

The TPS7A25 is available in a thermally enhanced WSON package.

8.2 Functional Block Diagrams

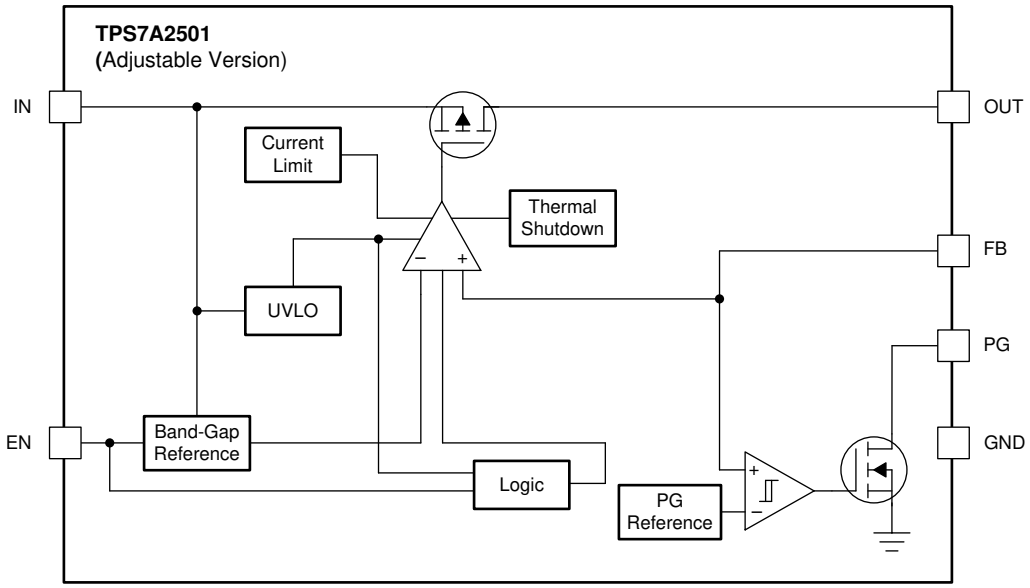


図 8-1. Adjustable Version

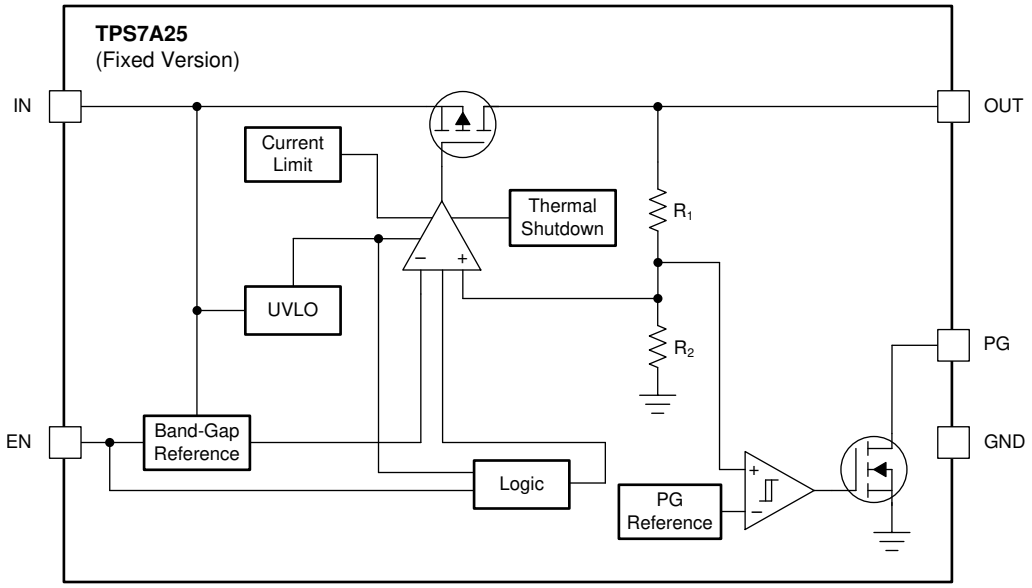


図 8-2. Fixed Version

8.3 Feature Description

8.3.1 Output Enable

The enable pin for the device is an active-high pin. The output voltage is enabled when the voltage of the enable pin is greater than the high-level input voltage of the EN pin and disabled with the enable pin voltage is less than the low-level input voltage of the EN pin. If independent control of the output voltage is not needed, connect the enable pin to the input of the device.

8.3.2 Dropout Voltage

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage ($V_{IN} – V_{OUT}$) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. Use 式 1 to calculate the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

8.3.3 Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a brick-wall scheme. In a high-load current fault, the brick-wall scheme limits the output current to the current limit (I_{CL}). I_{CL} is listed in the *Electrical Characteristics* table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power [($V_{IN} – V_{OUT}$) × I_{CL}]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application note.

図 8-3 depicts a diagram of the current limit.

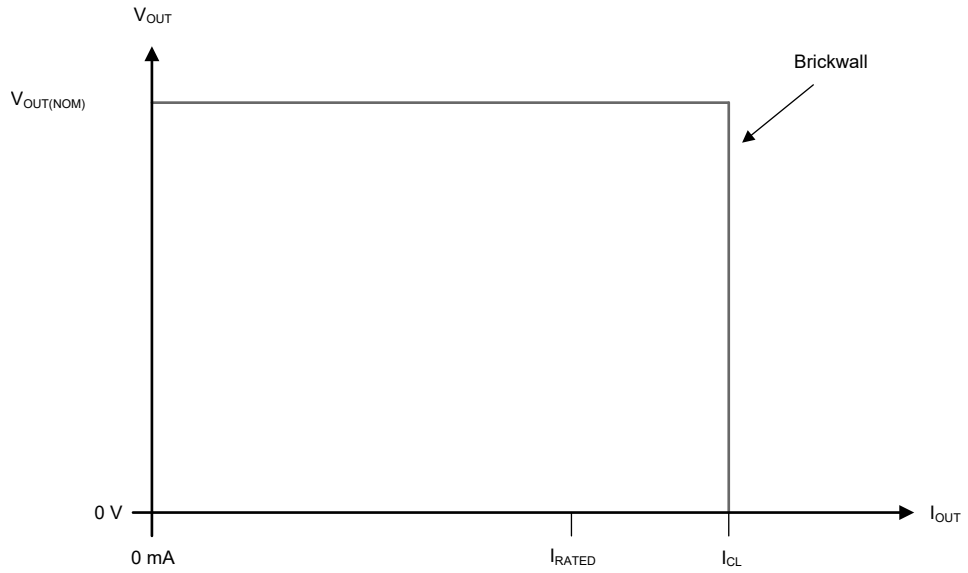


図 8-3. Current Limit

8.3.4 Undervoltage Lockout (UVLO)

The device has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage, allowing a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has hysteresis as specified in the *Electrical Characteristics* table.

8.3.5 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis assures that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short, thus the device may cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start-up can be high from large V_{IN} – V_{OUT} voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start-up completes.

When the thermal limit is triggered with the load current near the value of the current limit, the output may oscillate prior to the output switching off.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed its operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

8.3.6 Power Good

The power-good (PG) pin is an open-drain output and can be connected to a regulated supply through an external pullup resistor. The maximum pullup voltage is listed as V_{PG} in the *Recommended Operating Conditions* table. For the PG pin to have a valid output, the voltage on the IN pin must be greater than $V_{UVLO(RISING)}$, as listed in the *Electrical Characteristics* table. When the V_{OUT} exceeds $V_{IT(PG,RISING)}$, the PG output is high impedance and the PG pin voltage pulls up to the connected regulated supply. When the regulated output falls below $V_{IT(PG,FALLING)}$, the open-drain output turns on and pulls the PG output low after a short deglitch time. If output voltage monitoring is not needed, the PG pin can be left floating or connected to ground.

The recommended maximum PG pin sink current ($I_{PG-SINK}$) and the leakage current into the PG pin ($I_{LKG(PG)}$) are listed in the *Electrical Characteristics* table.

The PG pullup voltage (V_{PG_PULLUP}), the desired minimum power-good output voltage ($V_{PG(MIN)}$), and $I_{LKG(PG)}$ limit the maximum PG pin pullup resistor value (R_{PG_PULLUP}). V_{PG_PULLUP}, the PG pin low-level output voltage ($V_{OL(PG)}$), and $I_{PG-SINK}$ limit the minimum R_{PG_PULLUP}. Maximum and minimum values for R_{PG_PULLUP} can be calculated from the following equations:

$$R_{PG\_PULLUP(MAX)} = (V_{PG\_PULLUP} - V_{PG(MIN)}) / I_{LKG(PG)\_MAX} \quad (2)$$

$$R_{PG\_PULLUP(MIN)} = (V_{PG\_PULLUP} - V_{OL(PG)}) / I_{PG-SINK} \quad (3)$$

For example, if the PG pin is connected to a pullup resistor with a 3.3-V external supply, from 式 2, $R_{PG\_PULLUP(MAX)}$ is 11 MΩ. From 式 3, $R_{PG\_PULLUP(MIN)}$ is 5.8 kΩ.

8.3.7 Active Overshoot Pulldown Circuitry

This device has pulldown circuitry connected to V_{OUT}. This circuitry is a 100-µA current sink, in series with a 5.5-kΩ resistor, controlled by V_{EN}. When V_{EN} is below $V_{EN(LOW)}$, the pulldown circuitry is disabled and the LDO output is in high-impedance mode.

If the output voltage is more than 60 mV above nominal voltage when $V_{EN} \geq V_{EN(LOW)}$, the pulldown circuitry turns on and the output is pulled down until the output voltage is within 60 mV from the nominal voltage. This feature helps reduce overshoot during the transient response.

8.4 Device Functional Modes

8.4.1 Device Functional Mode Comparison

表 8-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

表 8-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{EN(LOW)}$	Not applicable	$T_J > T_{SD(shutdown)}$

8.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

8.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during start-up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

8.4.4 Disabled

The output of the device can be shutdown by forcing the voltage of the enable pin to less than the maximum EN pin low-level input voltage (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off and internal circuits are shutdown.

Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Adjustable Device Feedback Resistors

The adjustable-version device requires external feedback divider resistors to set the output voltage. V_{OUT} is set using the feedback divider resistors, R_1 and R_2, according to the following equation:

$$V_{OUT} = V_{FB} \times (1 + R_1 / R_2) \quad (4)$$

To ignore the FB pin current error term in the V_{OUT} equation, set the feedback divider current to 100 times the FB pin current listed in the *Electrical Characteristics* table. This setting provides the maximum feedback divider series resistance, as shown in the following equation:

$$R_1 + R_2 \leq V_{OUT} / (I_{FB} \times 100) \quad (5)$$

9.1.2 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. As a rule of thumb, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors recommended in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

9.1.3 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. An input capacitor is recommended if the source impedance is more than 0.5 Ω. A higher value capacitor may be necessary if large, fast transient load or line transients are anticipated or if the device is located several inches from the input power source.

Dynamic performance of the device is improved with the use of an output capacitor. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table for stability.

The effective output capacitance is recommended to not exceed 50 µF.

9.1.4 Reverse Current

Excessive reverse current can damage this device. Reverse current flows through the intrinsic body diode of the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} \leq V_{IN} + 0.3$ V.

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, external protection is recommended to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated.

図 9-1 shows one approach for protecting the device.

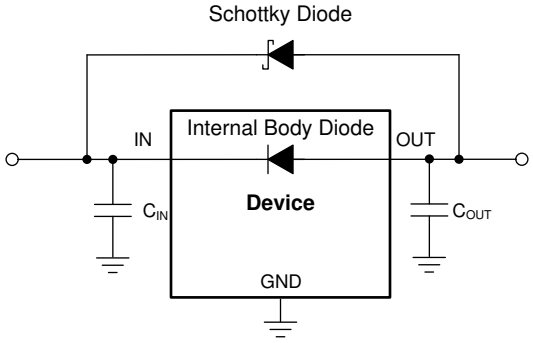


図 9-1. Example Circuit for Reverse Current Protection Using a Schottky Diode

図 9-2 shows another, more commonly used, approach in high input voltage applications.

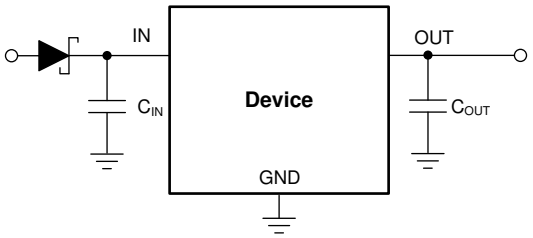


図 9-2. Reverse Current Prevention Using A Diode Before the LDO

9.1.5 Feed-Forward Capacitor (C_{FF})

For the adjustable-voltage version device, a feed-forward capacitor (C_{FF}) can be connected from the OUT pin to the FB pin. C_{FF} improves transient, noise, and PSRR performance, but is not required for regulator stability. Common C_{FF} value choices range between 10 nF and 100 nF. A higher capacitance C_{FF} can be used; however, the start-up time increases. For a detailed description of C_{FF} tradeoffs, see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application note.

9.1.6 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation (P_D).

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (6)$$

注

Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to the following equation, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (7)$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance.

9.1.7 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the linear regulator when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter (ψ_{JT}) and junction-to-board characterization parameter (ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J), as described in the following equations. Use the junction-to-top characterization parameter (ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter (ψ_{JB}) with the PCB surface temperature 1 mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \psi_{JT} \times P_D \quad (8)$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + \psi_{JB} \times P_D \quad (9)$$

where:

- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the *Semiconductor and IC Package Thermal Metrics* application note.

9.1.8 Special Consideration for Line Transients

During a line transient, the response of this LDO to a very large or fast input voltage change can cause a brief shutdown lasting up to a few hundred microseconds from the voltage transition. This shutdown can be avoided by reducing the voltage step size, increasing the transition time, or a combination of both. 図 9-3 provides a boundary to follow to avoid this behavior. If necessary, reduce slew rate and the voltage step size to stay below the curve.

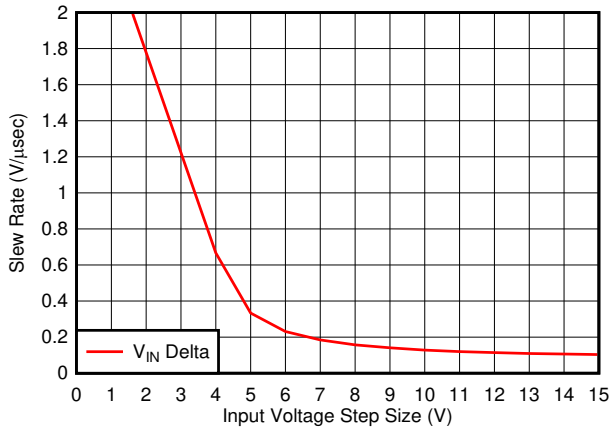


図 9-3. Recommended Input Voltage Step and Slew Rate in a Line transient

9.2 Typical Application

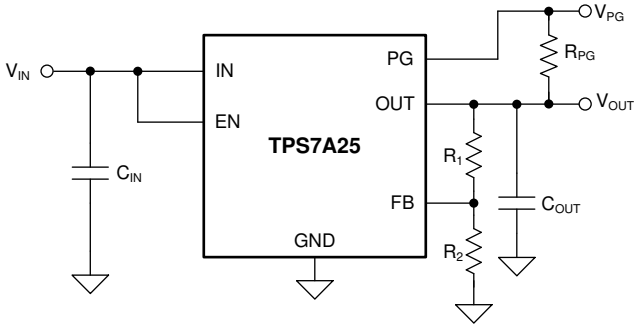


図 9-4. Generating a 5-V Rail From a Multicell Power Bank

9.2.1 Design Requirements

表 9-1 summarizes the design requirements for 図 9-4.

表 9-1. Design Parameters

PARAMETER	DESIGN VALUES
V_{IN}	8.4 V
V_{OUT}	5 V ±1%
$I_{(IN)}$ (no load)	< 5 µA
I_{OUT} (max)	220 mA
T_A	70°C (max)

9.2.2 Detailed Design Procedure

Select a 5-V output, fixed or adjustable device to generate the 5-V rail. The fixed-version LDO has internal feedback divider resistors and thus has lower effective quiescent current. The adjustable-version LDO requires external feedback divider resistors, and resistor selection is described in the *Selecting Feedback Divider Resistors* section.

9.2.2.1 Transient Response

As with any regulator, increasing the output capacitor value reduces over- and undershoot magnitude, but increases transient response duration.

9.2.2.2 Selecting Feedback Divider Resistors

For this design example, V_{OUT} is set to 5 V. The following equations set the feedback divider resistors for the desired output voltage:

$$V_{OUT} = V_{FB} \times (1 + R_1 / R_2) \quad (10)$$

$$R_1 + R_2 \leq V_{OUT} / (I_{FB} \times 100) \quad (11)$$

For improved output accuracy, use 式 11 and $I_{FB(TYP)}$ = 10 nA as listed in the *Electrical Characteristics* table to calculate the upper limit for series feedback resistance, $R_1 + R_2 \leq 5$ MΩ.

The control-loop error amplifier drives the FB pin to the same voltage as the internal reference (V_{FB} = 1.24 V as listed in the *Electrical Characteristics* table). Use 式 10 to determine the ratio of $R_1 / R_2 = 3.03$. Use this ratio and solve 式 11 for R_2. Now calculate the upper limit for $R_2 \leq 1.24$ MΩ. Select a standard resistor value for R_2 = 1.18 MΩ.

Reference 式 10 and solve for R_1:

$$R_1 = (V_{OUT} / V_{FB} – 1) \times R_2 \quad (12)$$

From 式 12, R_1 = 3.64 MΩ can be determined. Select a standard resistor value for R_1 = 3.6 MΩ. From 式 10, V_{OUT} = 5.023 V.

9.2.2.3 Thermal Dissipation

Junction temperature can be determined using the junction-to-ambient thermal resistance ($R_{\theta JA}$) and the total power dissipation (P_D). Use 式 13 to calculate the power dissipation. Multiply P_D by $R_{\theta JA}$ and add the ambient temperature (T_A), as 式 14 shows, to calculate the junction temperature (T_J).

$$P_D = (I_{GND} + I_{OUT}) \times (V_{IN} – V_{OUT}) \quad (13)$$

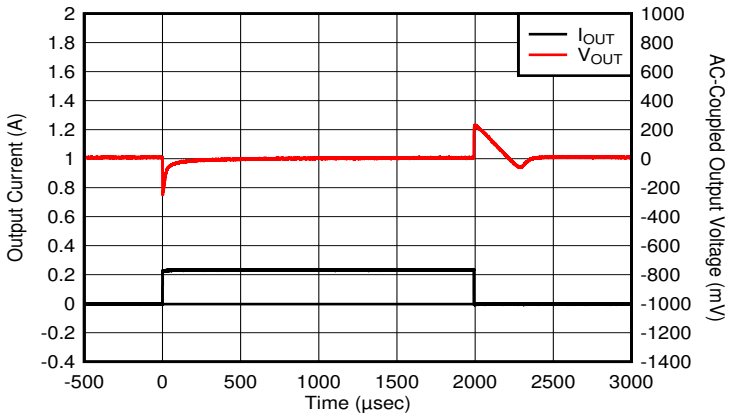
$$T_J = R_{\theta JA} \times P_D + T_A \quad (14)$$

式 15 calculates the maximum ambient temperature. 式 16 calculates the maximum ambient temperature for this application.

$$T_{A(MAX)} = T_{J(MAX)} – (R_{\theta JA} \times P_D) \quad (15)$$

$$T_{A(MAX)} = 125°C – [73.3°C/W \times (8.4\ V – 5\ V) \times 0.22\ A] = 70.2°C \quad (16)$$

9.2.3 Application Curve



I_{OUT} = 1 mA to 0.22 A, slew rate = 0.5 A/µs, V_{OUT} = 5 V, V_{IN} = 8.4 V, C_{IN} = 1 µF, C_{OUT} = 1 µF, C_{FF} = 0 µF

図 9-5. TPS7A25 Load Transient (1 mA to 220 mA)

9.3 Power Supply Recommendations

The device is designed to operate from an input supply voltage range of 2.4 V to 18 V. To ensure that the output voltage is well regulated and dynamic performance is optimum, the input supply must be at least $V_{OUT(nom)}$ + 0.5 V. Connect a low output impedance power supply directly to the input pin of the TPS7A25.

9.4 Layout

9.4.1 Layout Guidelines

- Place input and output capacitors as close to the device pins as possible
- Use copper planes for device connections to optimize thermal performance
- Place thermal vias around the device and under the DRV thermal pad to distribute heat

9.4.2 Layout Examples

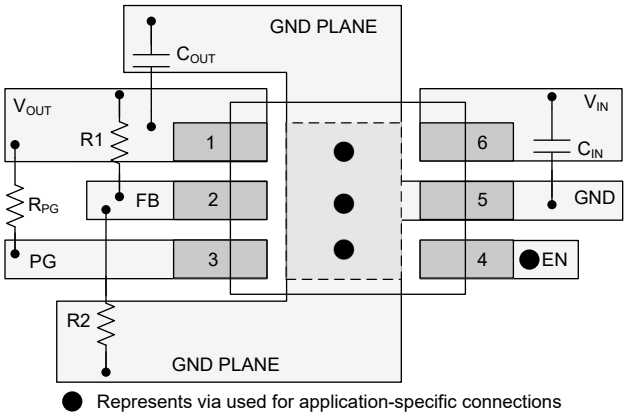


図 9-6. Adjustable Version Layout Example

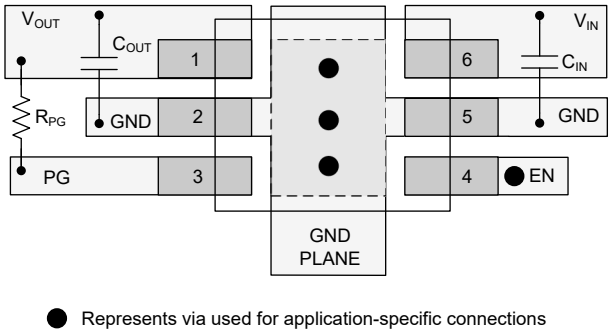


図 9-7. Fixed Version Layout Example

9 Device and Documentation Support

9.1 Device Support

9.1.1 Device Nomenclature

表 9-1. Device Nomenclature(1)

PRODUCT	V_{OUT}
TPS7A25**xx(x)yyyz**	**xx(x)** is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; for output voltages with a resolution of 50 mV, three digits are used (for example, 28 = 2.8 V; 125 = 1.25 V). 01 indicates adjustable output version. **yyy** is the package designator. **z** is the package quantity. R is for large quantity reel, T is for small quantity reel.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

Texas Instruments, *TPS7A26 500-mA, 18-V, Ultra-Low I_Q, Low Dropout Linear Voltage Regulator With Power-Good* data sheet

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

9.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

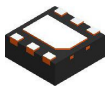
9.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

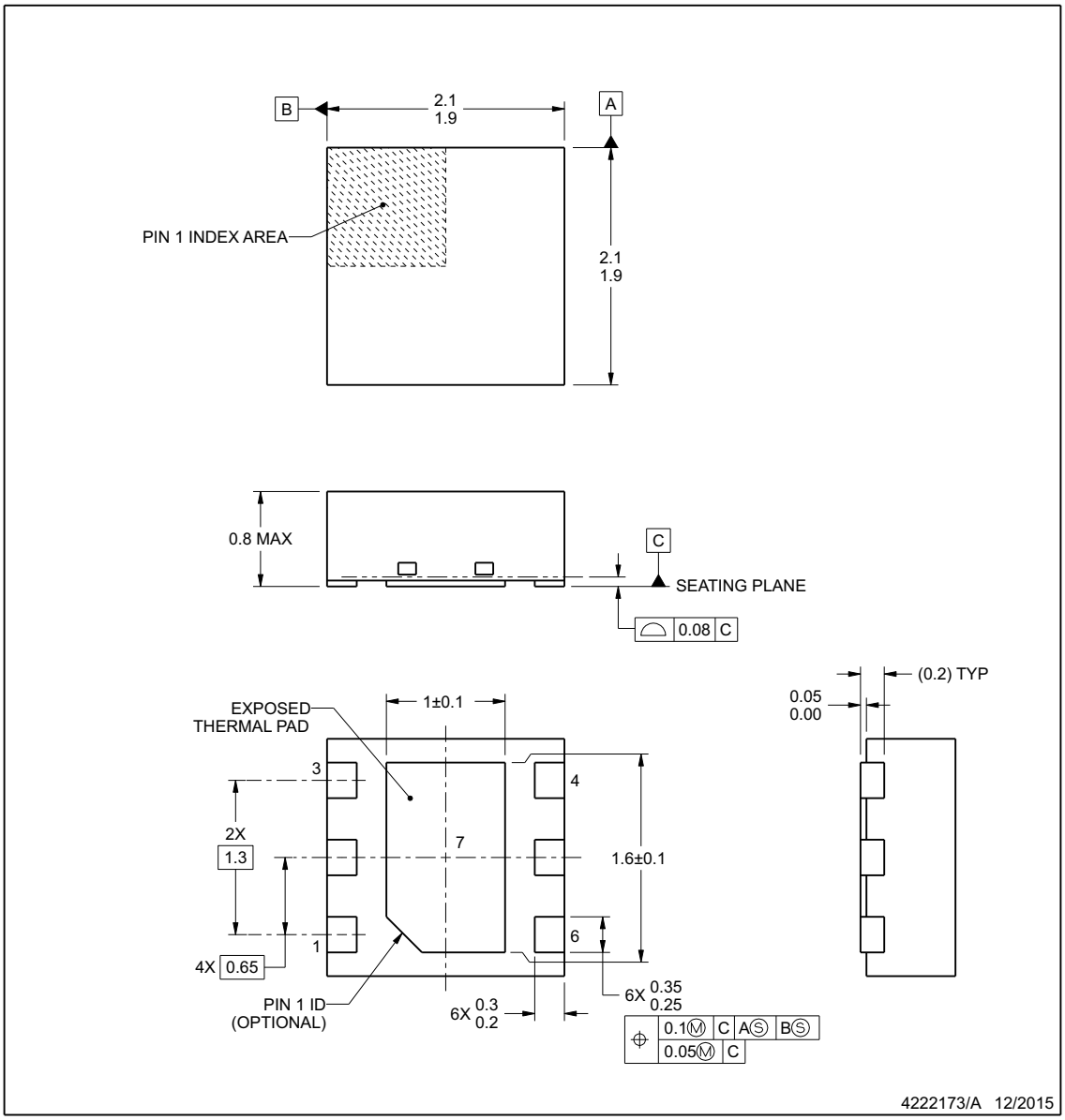
10.1 Mechanical Data



PACKAGE OUTLINE

DRV0006A — **WSON - 0.8 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

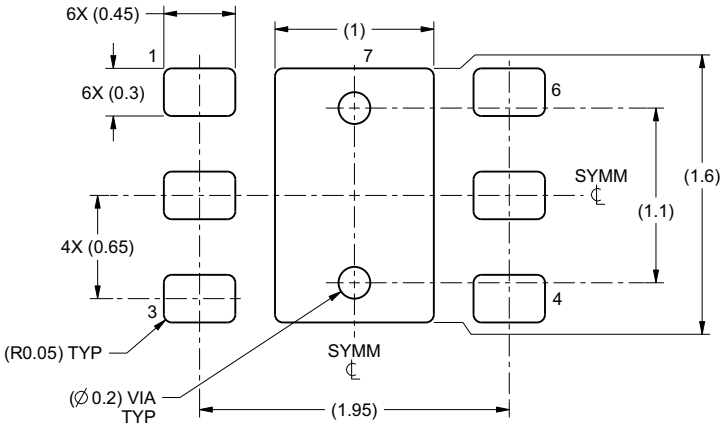
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

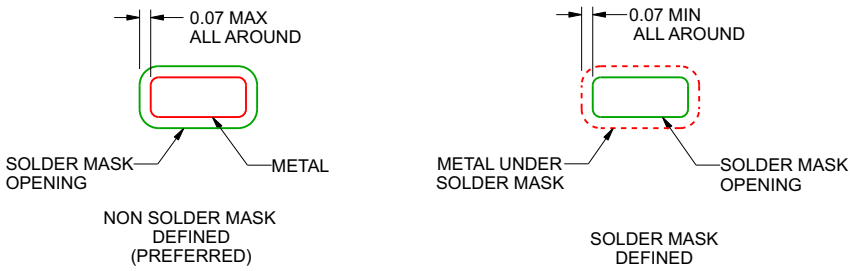
DRV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS

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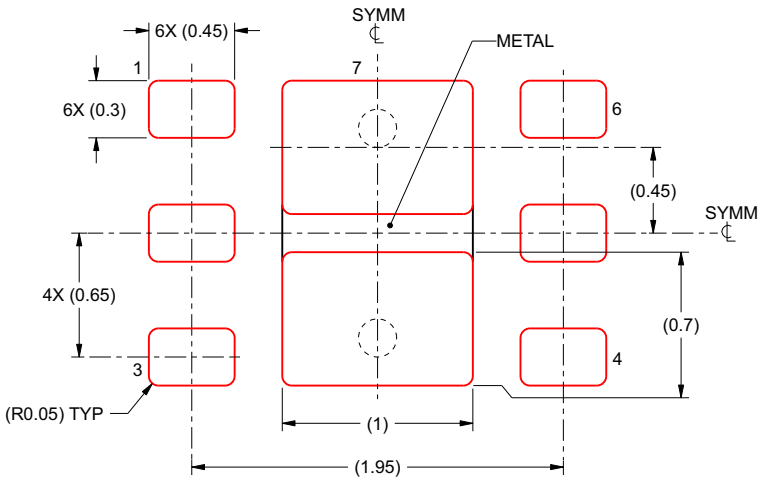
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DRV0006A — **WSON - 0.8 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/A 12/2015

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7A2501DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7A25
TPS7A2501DRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7A25
TPS7A2501DRVRG4	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7A25
TPS7A2501DRVRG4.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7A25
TPS7A2501DRVT	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7A25
TPS7A2501DRVT.A	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7A25
TPS7A25125DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1XCP
TPS7A25125DRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1XCP
TPS7A25125DRVRG4	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1XCP
TPS7A25125DRVRG4.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1XCP
TPS7A2518DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1XBP
TPS7A2518DRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1XBP
TPS7A2525DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1XAP
TPS7A2525DRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1XAP
TPS7A2533DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1WSP
TPS7A2533DRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1WSP
TPS7A2533DRVRG4	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1WSP
TPS7A2533DRVRG4.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1WSP
TPS7A2550DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1WQP
TPS7A2550DRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1WQP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

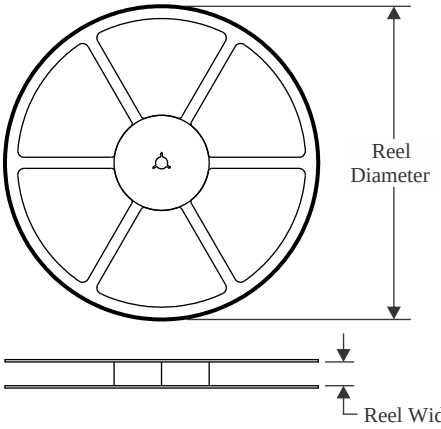
(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

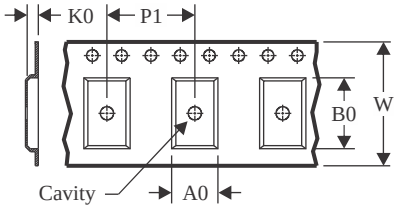
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

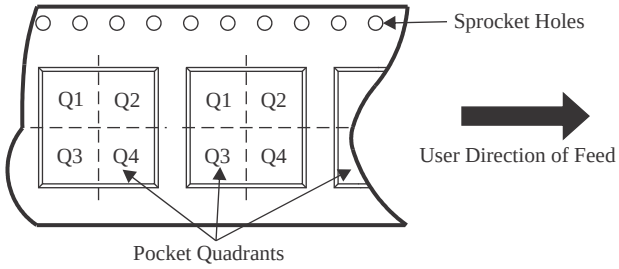


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

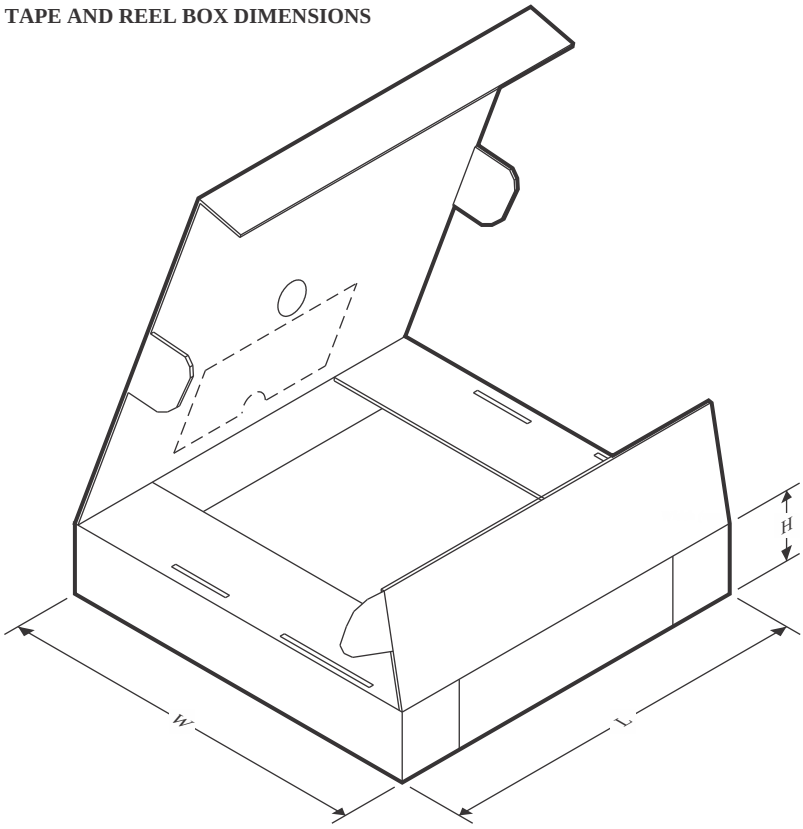
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A2501DRVR	WSON	DRV	6	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS7A2501DRVRG4	WSON	DRV	6	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS7A2501DRVT	WSON	DRV	6	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS7A25125DRVR	WSON	DRV	6	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS7A25125DRVRG4	WSON	DRV	6	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS7A2518DRVR	WSON	DRV	6	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS7A2525DRVR	WSON	DRV	6	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS7A2533DRVR	WSON	DRV	6	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS7A2533DRVRG4	WSON	DRV	6	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS7A2550DRVR	WSON	DRV	6	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

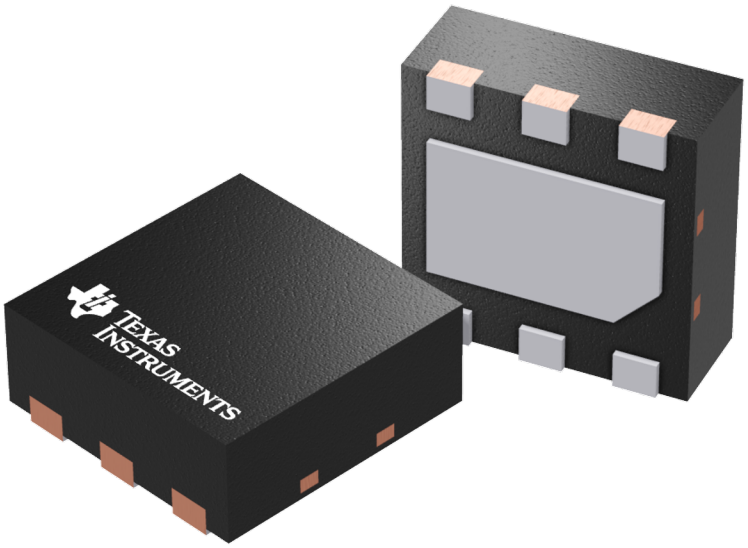


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A2501DRVR	WSON	DRV	6	3000	205.0	200.0	33.0
TPS7A2501DRVRG4	WSON	DRV	6	3000	205.0	200.0	33.0
TPS7A2501DRVT	WSON	DRV	6	250	205.0	200.0	33.0
TPS7A25125DRVR	WSON	DRV	6	3000	205.0	200.0	33.0
TPS7A25125DRVRG4	WSON	DRV	6	3000	205.0	200.0	33.0
TPS7A2518DRVR	WSON	DRV	6	3000	205.0	200.0	33.0
TPS7A2525DRVR	WSON	DRV	6	3000	205.0	200.0	33.0
TPS7A2533DRVR	WSON	DRV	6	3000	205.0	200.0	33.0
TPS7A2533DRVRG4	WSON	DRV	6	3000	205.0	200.0	33.0
TPS7A2550DRVR	WSON	DRV	6	3000	205.0	200.0	33.0

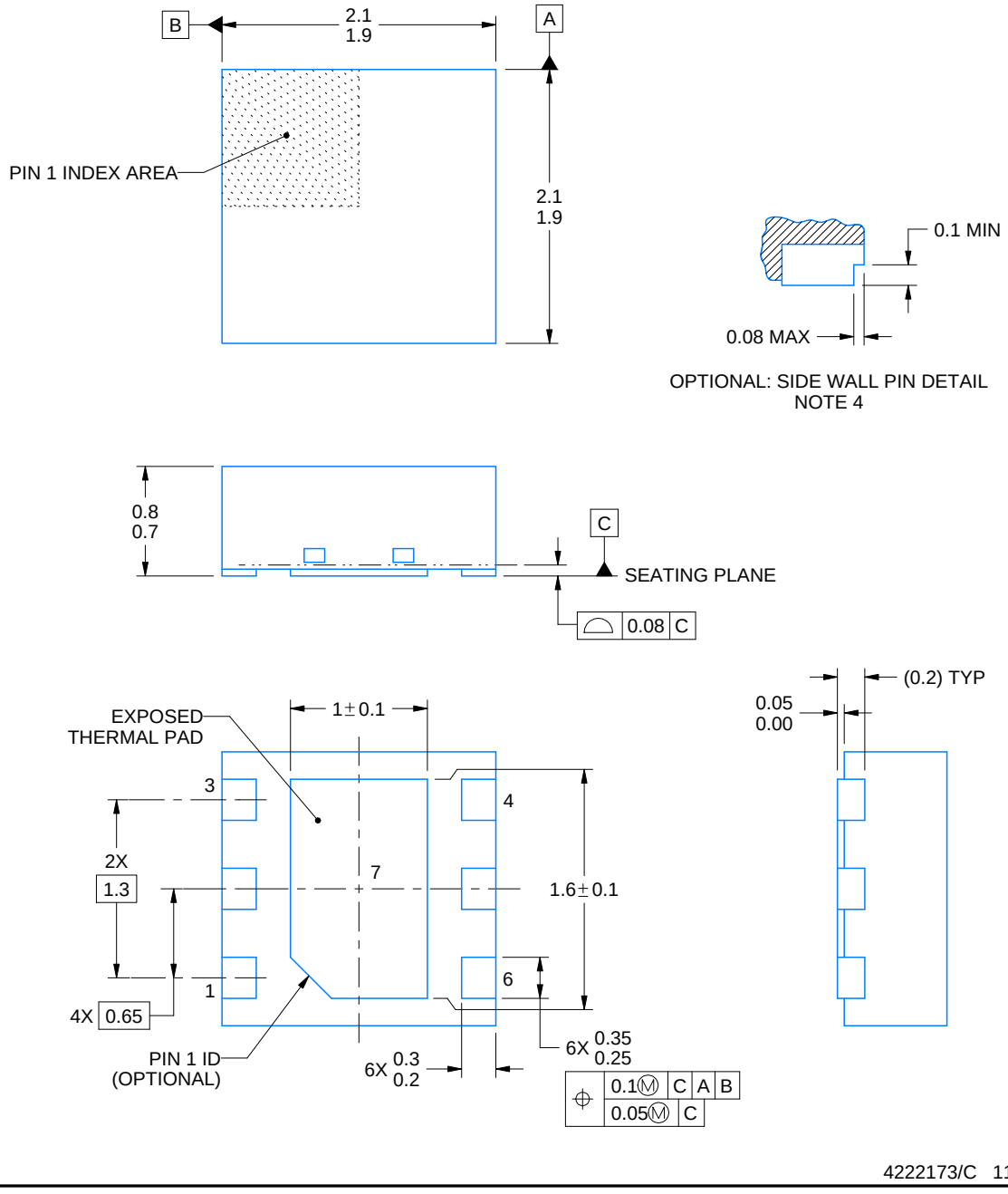
DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



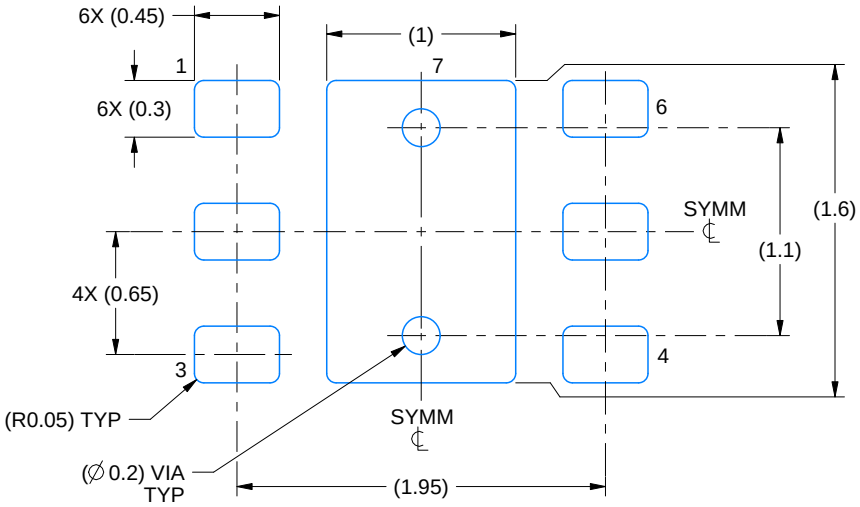
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PLASTIC SMALL OUTLINE - NO LEAD

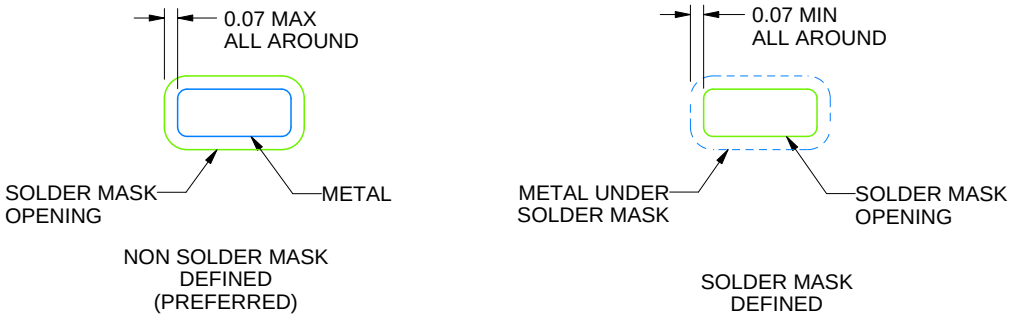


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS

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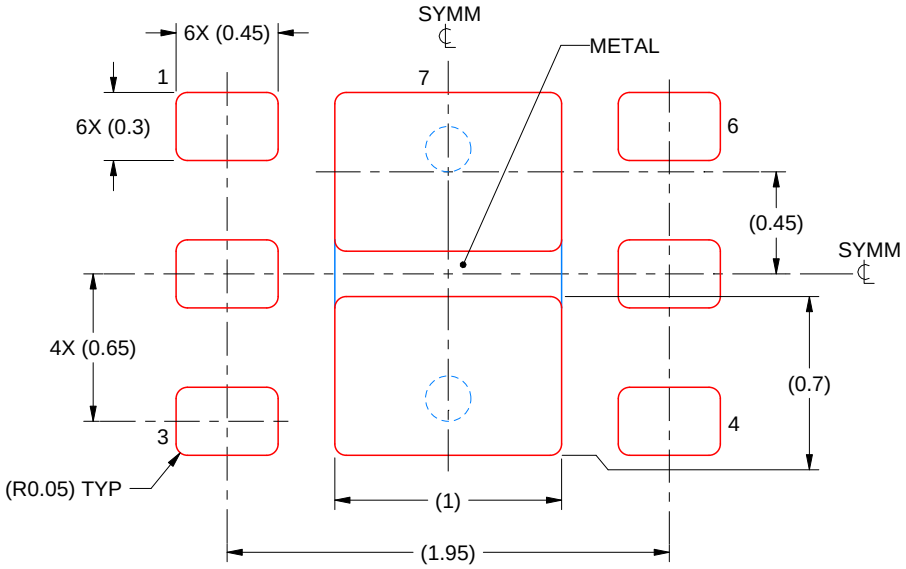
NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月