TPS7A63-Q1、TPS7A6401-Q1
超低I_Q、300mA、40V、低ドロップアウト・レギュレータ

1 特長

- 車載アプリケーション用に AEC-Q100 認定取得済み
  - 温度グレード 1: -40°C～125°C、T_A
  - 接合部温度:–40℃～150℃、T_J
- 低いドロップアウト電圧：
  - I_{OUT} = 150mA で 300mV
- 7V～40V の広い入力電圧範囲、最大 45V の過渡電圧に対応
- 最大出力電流：300mA
- 非常に低い静止電流
  - 軽負荷時に $I_{QUIESCENT}$ = 35µA (標準値)
  - EN = LOW のとき I_{SLEEP} < 2µA
- 固定 (3.3V および 5V) および可変 (2.5V～7V) の出力電圧
- フォルト / フラグ付きのウォッチドッグを内蔵
- 低 ESR のセラミック出力コンデンサで安定動作
- パワーオン・リセット機能を搭載
  - 遅延をプログラム可能
  - オープン・ドレイン・リセット出力
- フォルト保護機能を搭載
  - 短絡保護と過電流保護
  - サーマル・シャットダウン
- 低入力電圧トラッキング
- 熱的に強化された 14 ピンの HTSSOP-PWP パッケージと 10 ピンの VSON-DRK パッケージ

2 アプリケーション

- 車載用ヘッド・ユニット
- ヘッドライト
- DC/DC コンバータ
- 車載センター情報ディスプレイ

3 概要

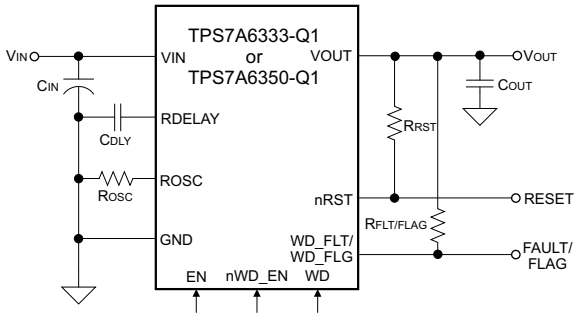
TPS7A63-Q1およびTPS7A6401-Q1は、低ドロップアウトのリニア電圧レギュレータのファミリで、消費電力が低く、軽負荷アプリケーションで静止電流が35µA未満に設計されています。これらのデバイスは、低ESRのセラミック出力コンデンサでも安定して動作するよう設計されており、プログラム可能なウィンドウ・ウォッチドッグと過電流保護機能が搭載されています。設計者は、外付け抵抗を使用して出力電圧をプログラムできます。低電圧トラッキング機能により、小型の入力コンデンサを使用でき、コールド・クランク状況では多くの場合に昇圧コンバータが不要になります。パワー・オン・リセット遅延は固定(標準値250µs)で、外付けコンデンサにより遅延をプログラムできます。これらの特長から、これらのデバイスは各種の車載アプリケーション用の電源に最適です。

製品情報(1)

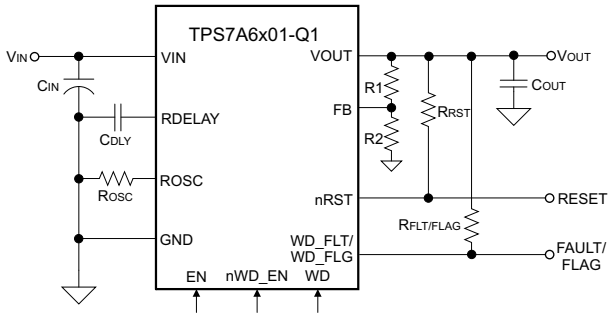
型番	パッケージ	本体サイズ(公称)
TPS7A63-Q1、TPS7A6401-Q1	HTSSOP (14)	5.00mm×4.40mm
TPS7A63-Q1	VSON (10)	4.00mm×3.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

固定出力電圧オプション



可変出力電圧オプション



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision F (June 2018) から **Revision G** に変更 **Page**

- AEC-Q100 の「*特長*」項目を新標準に合わせて 変更 ... 1
- ドキュメント全体で入力電圧範囲を 11V から 7V に 変更 ... 1
- 「*アプリケーション*」セクションを 変更 ... 1
- Added footnote to V_{IN} row in *Recommended Operating Conditions* table ... 5
- Added footnote to V_{IN} row in *Electrical Characteristics* table ... 6

Revision E (September 2015) から **Revision F** に変更 **Page**

- デバイス名を TPS7A63-Q1 TPS7A6401-Q1 に 変更 ... 1
- 4 番目の「*特長*」項目で 4V を 11V に 変更 ... 1
- Changed V_{IN}, V_{EN} parameter row in *Recommended Operating Conditions* table: separated V_{IN} and V_{EN} into different rows, changed V_{IN} minimum specification from 4 V to 11 V ... 5
- Changed V_{IN} minimum specification from V_{OUT} + *0.3 V* to *11 V* in *Electrical Characteristics* table ... 6
- Changed 4 V to 11 V in *Example values* column of *Input voltage range* row of *Design Parameters* table ... 22
- Changed 4 V to 11 V in *Example values* column of *Input voltage range* row of *Design Parameters* table ... 23
- Changed 4 V to 11 V in first sentence of *Power Supply Recommendations* section ... 24

Revision D (July 2012) から **Revision E** に変更 **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 5

Revision C (April 2012) から **Revision D** に変更 **Page**

- データシート全体で複数個所の型番を訂正 ... 1
- 「特長」一覧の最初に新項目を追加 ... 1
- Deleted the NO. column from the electrical tables ... 5

- Deleted two Typical Characteristics graphs 8

Revision B (December 2011) から **Revision C** に変更 **Page**

- Changed regulated output voltage (6.1), added text to the test conditions (10mA to 200mA, V_{IN} = V_{OUT} + 1V to 16V) 6

Revision A (August 2011) から **Revision B** に変更 **Page**

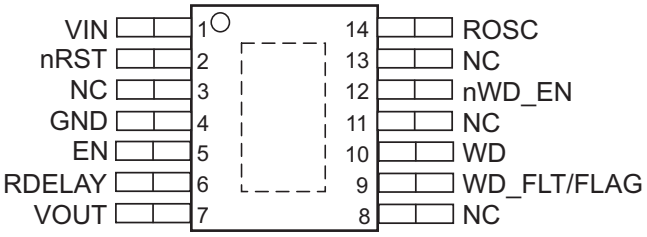
- TPS7A64333-Q1 および TPSA6450-Q1 を削除..... 1

2011年**6**月発行のものから更新 **Page**

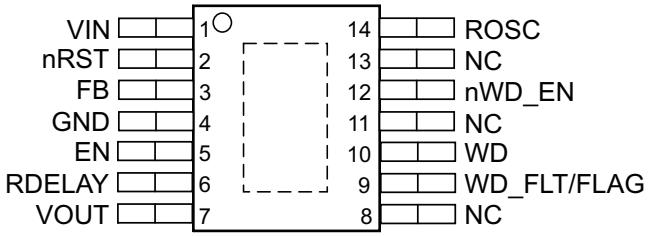
- Deleted the Ordering Information Table 4
- Changed values for V_{IL} and V_{IH} in the Watchdog Enable Input (nWD_EN pin) section..... 7
- Changed values for V_{IL} and V_{IH} in the Watchdog Input Pulse (WD pin) section..... 7

5 Pin Configuration and Functions

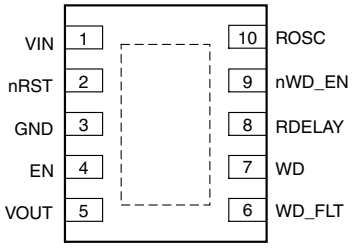
PWP Package
14-Pin HTSSOP With PowerPAD IC Package
Top View (Fixed Output Voltage Option)



PWP Package
14-Pin HTSSOP With PowerPAD IC Package
Top View (Adjustable Output Voltage Option)



DRK Package
10-Pin VSON With Exposed Thermal Pad
Top View (Fixed Output Voltage Option)



Pin Functions

PIN			I/O	DESCRIPTION
NAME	PWP	DRK		
EN	5	4	I	Chip enable pin: This is a high-voltage-tolerant input pin with an internal pulldown. A high input to this pin activates the device and turns the regulator ON. Connect this input to the VIN terminal for self-bias applications. If this pin remains unconnected, the device stays disabled.
FB	3	—	I	Feedback pin (only applicable for TPS7A6x01-Q1): Sense voltage for error amplifier
GND	4	3	I/O	Ground pin: This is signal ground pin of the device.
NC	3	—	—	Not connected (only applicable for TPS7A6333-Q1 and TPS7A6350-Q1)
NC	8	—	—	Not connected
NC	11	—	—	Not connected
NC	13	—	—	Not connected
nRST	2	2	O	Reset pin: This is an open-drain reset output pin with an external pullup resistor connected to the VOUT pin.
nWD_EN	12	9	I	Watchdog enable pin: A high input to this pin disables the watchdog, and vice versa. This is an active-low input pin with an internal pulldown. Leaving this pin is unconnected and floating keeps the watchdog enabled. An external microcontroller can pull this pin high momentarily to disable and reinitialize the watchdog.
RDELAY	6	8	O	Reset delay timer pin: This pin programs the reset delay timer using an external capacitor (C_{DLY}) to ground.
ROSC	14	10	O	ROscillator pin: This pin programs the internal oscillator frequency (and hence the duration of the watchdog window) by connecting an external resistor to ground.
WD	10	7	I	Watchdog service pin: This is an input pin to provide a service signal to the watchdog.
WD_FLAG	9	6	O	Watchdog flag pin (for TPS7A6401-Q1 only): This is an active-high latched fault (that is, flag) output pin with an external pullup resistor connected to VOUT pin.
WD_FLT	9	6	O	Watchdog fault pin (for TPS7A63-Q1 only): This is an active-low fault output pin with an external pullup resistor connected to the VOUT pin.
VIN	1	1	I	Input voltage pin: The unregulated input voltage is supplied to this pin. A bypass capacitor connected between the VIN pin and GND pin dampens line transients on the input.
VOUT	7	5	O	Regulated output voltage pin: This is a regulated voltage output (V_{OUT} = 3.3 V or 5 V or a programmed value) pin with a limitation on maximum output current. For devices with adjustable output voltage (TPS7A6x01-Q1), connecting an external resistor network programs the output voltage. In order to achieve stable operation and prevent oscillation, connect an external output capacitor (C_{OUT}) with low ESR between this pin and GND pin.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

DESCRIPTION		MIN	MAX	UNIT
V_{IN}, V_{EN}	Unregulated inputs(2)(3)		45	V
V_{OUT}	Regulated output		7	V
FB	Sense voltage for error amplifier(2)		7	V
ROSC	Constant-voltage reference(2)		7	V
nWD_EN, WD, WD_FLAG, WD_FLT	Watchdog inputs and outputs(2)		7	V
nRST	Open-drain reset output(2)		7	V
RDELAY	Reset delay timer output(2)		7	V
T_A	Operating ambient temperature		125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to GND.
(2) Absolute negative voltage on these pins not to go below –0.3 V.
(3) Absolute maximum voltage for duration less than 480 ms.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±4000	V
		Charged device model (CDM), per AEC Q100-011	±1500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{IN}	Unregulated input voltage	7(1)	40	V
V_{EN}	Enable pin voltage	4	40	V
nRST, RDELAY, nWD_EN, WD_FLT(2), WD_FLAG(3), WD, FB(4)	Low voltage input or output	0	5.25	V
T_J	Operating junction temperature range	–40	150	°C

(1) V_{IN} can go down to 4 V for 130 ms or less and remain functional. If V_{IN} is less than 7 V for longer than 130 ms, then some devices can turn off until the input voltage rises above 7 V.
(2) Applicable for TPS7A63-Q1 only
(3) Applicable for TPS7A6401-Q1 only
(4) Applicable for TPS7A6301-Q1 and TPS7A6401-Q1 only

6.4 Thermal Information

THERMAL METRIC[1]		TPS7A6401-Q1 TPS7A63-Q1		UNIT
		PWP (HTTSOP)	DRK (VSON)	
		14 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	46	36.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.6	36.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	27.4	11.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.2	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	27.2	11.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.5	3.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

V_{IN} = 14 V, T_J = –40ºC to 150ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE (VIN PIN)						
V_{IN}	Input voltage	V_{OUT} = 2.5 V to 7 V, I_{OUT} = 1 mA	7[1]		40	V
$I_{QUIESCENT}$	Quiescent current	V_{IN} = 8.2 V to 18 V, V_{EN} = 5 V, I_{OUT} = 0.01 mA to 0.75 mA		35		µA
I_{SLEEP}	Sleep or shutdown current	V_{IN} = 8.2 V to 18 V, V_{EN} < 0.8 V, I_{OUT} = 0 mA (no load), T_A = 125°C			3	µA
$V_{IN-UVLO}$	Undervoltage lockout voltage	Ramp V_{IN} down until output is turned OFF		3.16		V
$V_{IN(POWERUP)}$	Power-up voltage	Ramp V_{IN} up until output is turned ON		3.45		V
DEVICE ENABLE INPUT (EN PIN)						
V_{IL}	Logic-input low level		0		0.8	V
V_{IH}	Logic-input high level		2.5		40	V
REGULATED OUTPUT VOLTAGE (VOUT PIN)						
V_{OUT}	Regulated output voltage	Fixed V_{OUT} value (3.3 V, 5 V or a programmed value), I_{OUT} = 10 mA to 200 mA, V_{IN} = V_{OUT} + 1 V to 16 V	–2%		2%	
$\Delta V_{LINE-REG}$	Line regulation	V_{IN} = 6 V to 28 V, I_{OUT} = 10 mA, V_{OUT} = 5 V			15	mV
		V_{IN} = 6 V to 28 V, I_{OUT} = 10 mA, V_{OUT} = 3.3 V			20	
$\Delta V_{LOAD-REG}$	Load regulation	I_{OUT} = 10 mA to 200 mA, V_{IN} = 14 V, V_{OUT} = 5 V			25	mV
		I_{OUT} = 10 mA to 200 mA, V_{IN} = 14 V, V_{OUT} = 3.3 V			35	
$V_{DROPOUT}$	Dropout voltage (V_{IN} – V_{OUT})	I_{OUT} = 200 mA			500	mV
		I_{OUT} = 150 mA			300	
R_{SW}[2]	Switch resistance	VIN to VOUT resistance			2	Ω
I_{OUT}	Output current	V_{OUT} in regulation	0		200	mA
		[V_{OUT} in regulation, V_{OUT} = 3.3 V, V_{IN} = 6 V][3]	0		300	
I_{CL}	Output current limit	V_{OUT} = 0 V (VOUT pin is shorted to ground)	350		1000	mA
PSRR[4]	Power-supply ripple rejection	$V_{IN-RIPPLE}$ = 0.5 Vpp, I_{OUT} = 200 mA, frequency = 100 Hz, V_{OUT} = 5 V and V_{OUT} = 3.3 V		60		dB
		$V_{IN-RIPPLE}$ = 0.5 Vpp, I_{OUT} = 200 mA, frequency = 150 kHz, V_{OUT} = 5 V and V_{OUT} = 3.3 V		30		

(1) V_{IN} can go down to 4 V for 130 ms or less and remain functional. If V_{IN} is less than 7 V for longer than 130 ms, then some devices can turn off until the input voltage rises above 7 V.
(2) This test is done with V_{OUT} in regulation, measuring the V_{IN} – V_{OUT} parameter when V_{OUT} drops by 100 mV from the programmed value (of V_{OUT}) at specified loads.
(3) Design Information - not tested; specified by characterization.
(4) Specified by design - not tested.

Electrical Characteristics (continued)

V_{IN} = 14 V, T_J = –40ºC to 150ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RESET (nRST PIN)						
V_{OL}	Reset pulled low	I_{OL} = 5 mA			0.4	V
I_{OH}	Leakage current	Reset pulled to VOUT through a 5-kΩ resistor			1	µA
$V_{TH(POR)}$	Power-on-reset threshold	V_{OUT} powered up above internally set tolerance, V_{OUT} = 5 V	4.5	4.65	4.77	V
		V_{OUT} powered up above internally set tolerance, V_{OUT} = 3.3 V		3.07		
UV_{THRES}	Reset threshold	V_{OUT} falling below internally set tolerance, V_{OUT} = 5 V	4.5	4.65	4.77	V
		V_{OUT} falling below internally set tolerance, V_{OUT} = 3.3 V		3.07		
t_{POR} (3)	Power-on-reset delay	C_{DLY} = 100 pF		300		µs
		C_{DLY} = 100 nF		300		ms
$t_{POR-PRESET}$	Internally preset Power-on-reset delay	C_{DLY} not connected, V_{OUT} = 5 V and V_{OUT} = 3.3 V		250		µs
$t_{DEGLITCH}$	Reset deglitch time			5.5		µs
RESET DELAY (RDELAY PIN)						
$V_{TH(RDELAY)}$	Threshold to release nRST high	Voltage at RDELAY pin is ramped up		3	3.3	V
I_{DLY}	Delay capacitor charging current		0.75	1	1.25	µA
I_{OL}	Delay capacitor discharging current	Voltage at RDELAY pin = 1 V	5			mA
CURRENT VOLTAGE REFERENCE (ROSC PIN)						
V_{ROSC}	Voltage reference		0.95	1	1.05	V
WATCHDOG FAULT / FLAG OUTPUT (WD_FLT / WD_FLAG Pin)						
V_{OL}	Logic output low level	I_{OL}= 5 mA			0.4	V
I_{OH}	Leakage current	WD_FLT/WD_FLG pulled to V_{OUT} through 5-kΩ resistor			1	µA
WATCHDOG ENABLE INPUT (nWD_EN PIN)						
V_{IL}	Logic input low level				0.8	V
V_{IH}	Logic input high level	3 V < V_{DD} < 5.25 V	2.5			V
WATCHDOG INPUT PULSE (WD PIN)						
V_{IL}	Logic input low level				0.8	V
V_{IH}	Logic input high level	3 V < V_{DD} < 5.25 V	2.5			V
t_{WD}	Watchdog window duration	R_{OSC} = 10 kΩ ± 1%		10		ms
		R_{OSC} = 20kΩ ± 1%		20		
t_{WD-tol}	Tolerance of watchdog period using external resistor	Excludes tolerance of R_{OSC} (external resistor connected to ROSC pin)	–10%		10%	
$t_{WD-DEFAULT}$	Default watchdog period	External resistor not connected, ROSC pin is floating or open	108	164	254	ms
$t_{WD-HOLD}$	Minimum pulse width for resetting watch dog timer			1.65		µs
OPERATING TEMPERATURE RANGE						
T_J	Operating junction temperature		–40		150	ºC
$T_{SHUTDOWN}$	Thermal shutdown trip point			165		ºC
T_{HYST}	Thermal shutdown hysteresis			10		ºC

6.6 Typical Characteristics

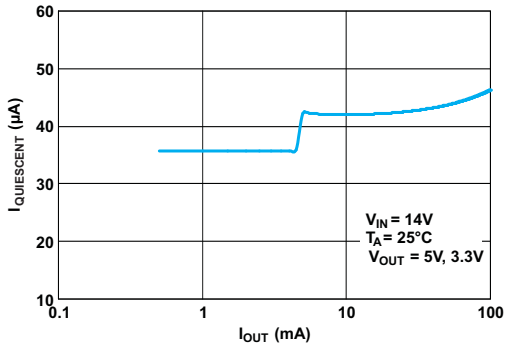


Figure 1. Quiescent Current vs Load Current

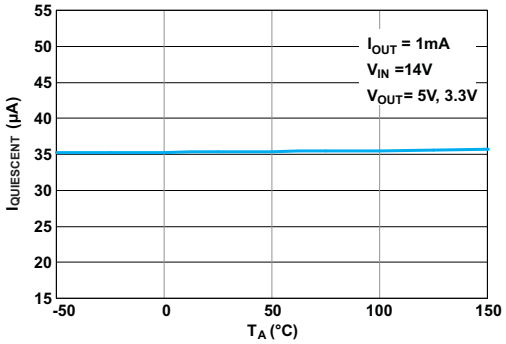


Figure 2. Quiescent Current vs Ambient Air Temperature

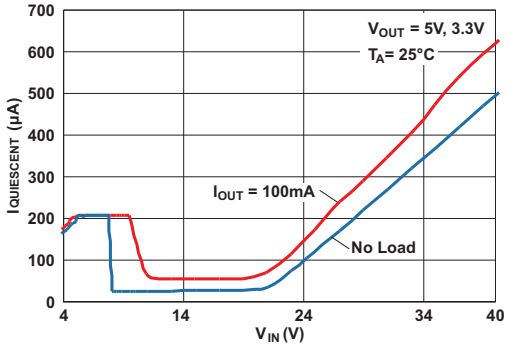
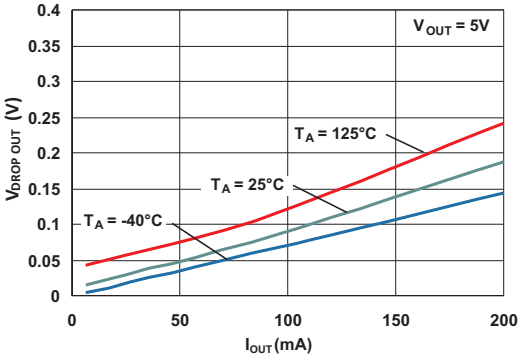


Figure 3. Quiescent Current vs Input Voltage



Measure dropout voltage when the output voltage drops by 100 mV from the regulated output-voltage level. (For example, for an output voltage programmed to be 5 V, measure the dropout voltage when the output voltage drops down to 4.9 V from 5 V.)

Figure 4. Dropout Voltage vs Load Current

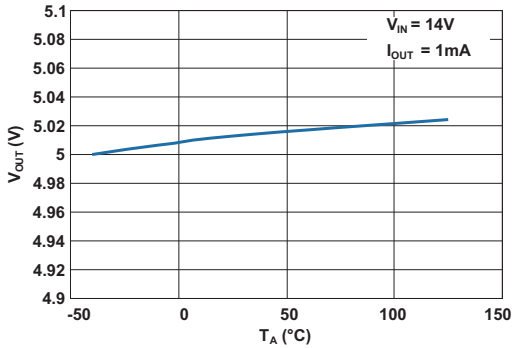


Figure 5. Output Voltage vs Ambient Air Temperature (V_{OUT} Set To 5 V)

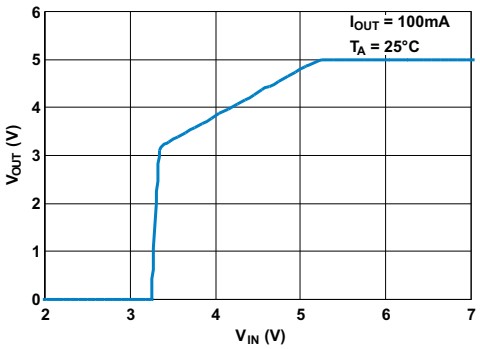


Figure 6. Output Voltage vs Input Voltage (V_{OUT} Set To 5 V)

Typical Characteristics (continued)

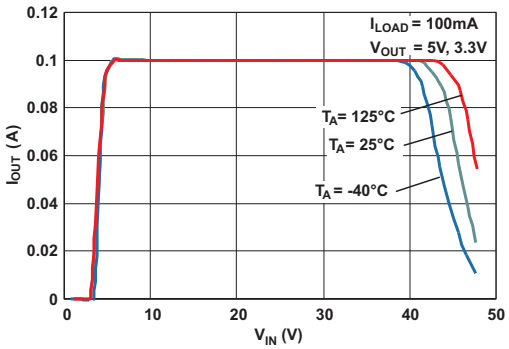


Figure 7. Output Voltage vs Input Voltage

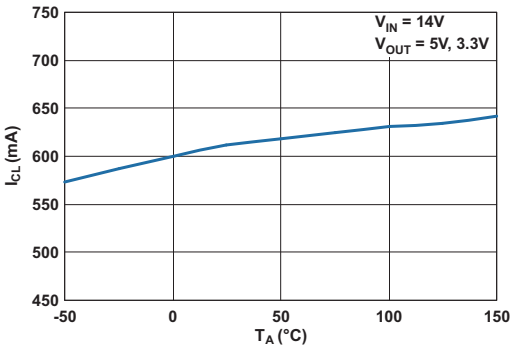


Figure 8. Output Current Limit vs Ambient Air Temperature

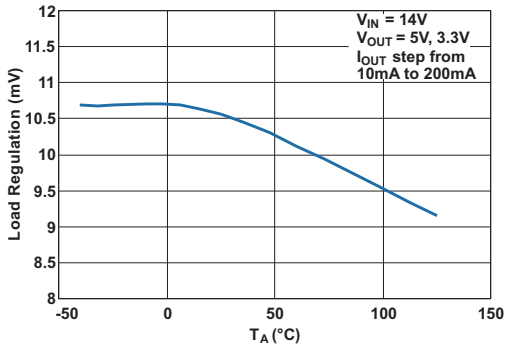


Figure 9. Load Regulation vs Ambient Air Temperature

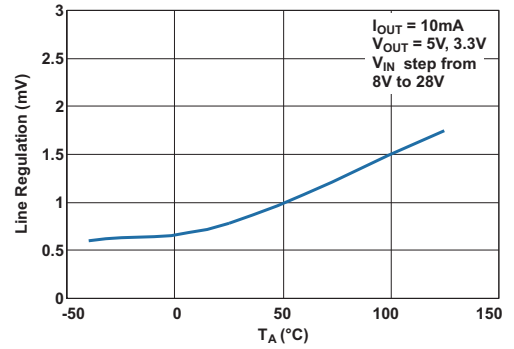


Figure 10. Line Regulation vs Ambient Air Temperature

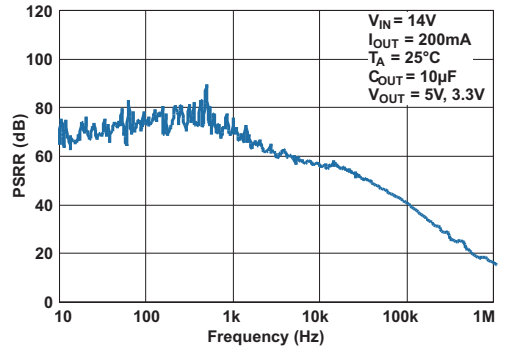


Figure 11. PSRR at Heavy Load Current

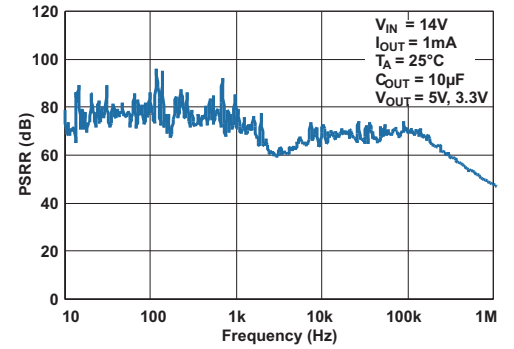


Figure 12. PSRR at Light Load Current

7 Detailed Description

7.1 Overview

The TPS7A63-Q1 and TPS7A6401-Q1 are a family of monolithic low-dropout linear voltage regulators with integrated watchdog and reset functionality. These voltage regulators are designed for low power consumption and quiescent current less than 25 µA in light-load applications. Because of a programmable reset delay (also called power-on-reset delay), these devices are well-suited in power supplies for microprocessors and microcontrollers.

These devices are available in two fixed and adjustable output-voltage versions as follows:

- Fault (WD_FLT) output version: TPS7A63-Q1
- Flag (WD_FLAG) output version: TPS7A6401-Q1

Feature Description describes the features of the TPS7A63-Q1 and TPS7A6401-Q1 voltage regulators in detail.

7.2 Functional Block Diagrams

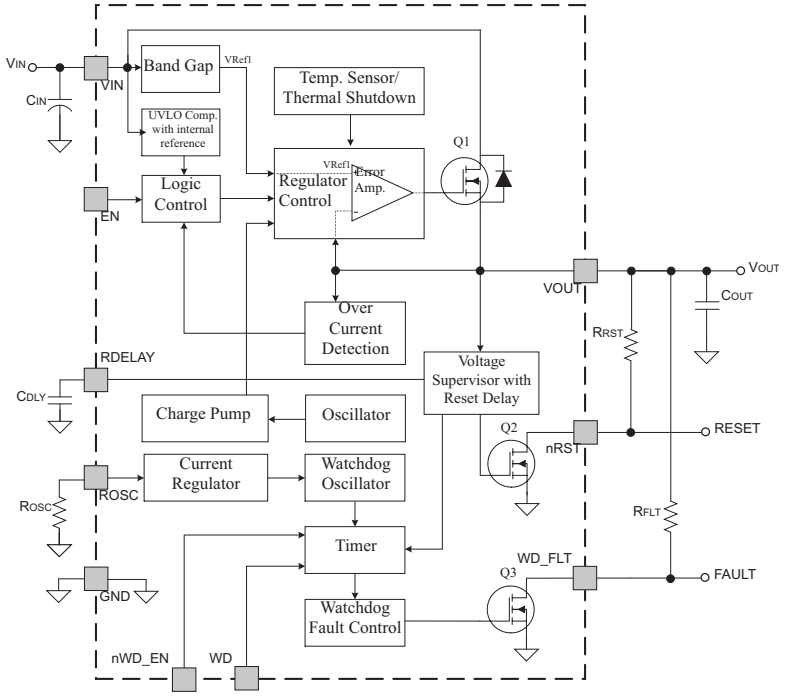


Figure 13. TPS7A6333-Q1 and TPS7A6350-Q1 (Fixed Output Voltage With Fault Output)

Functional Block Diagrams (continued)

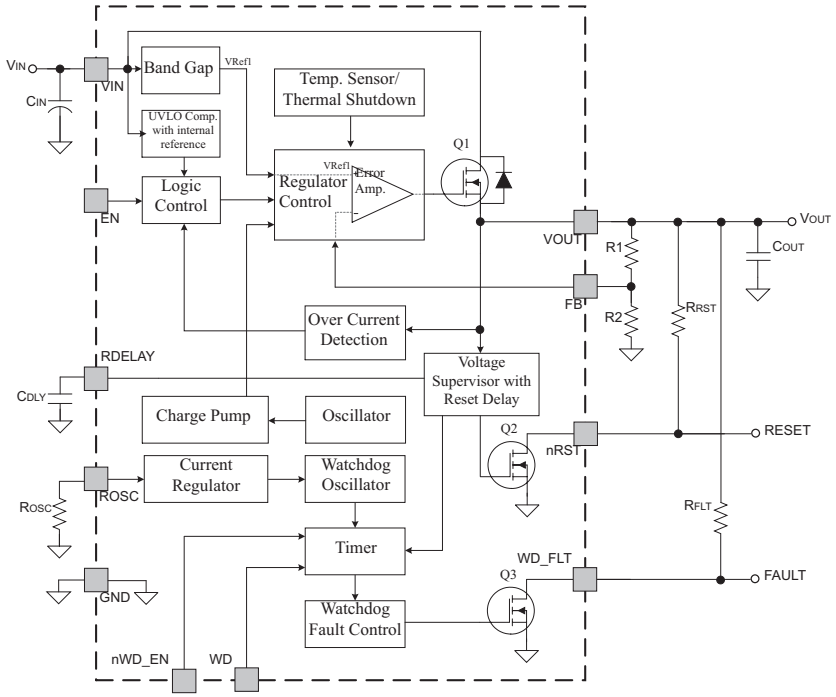


Figure 14. TPS7A6301 (Adjustable Output Voltage With Fault Output)

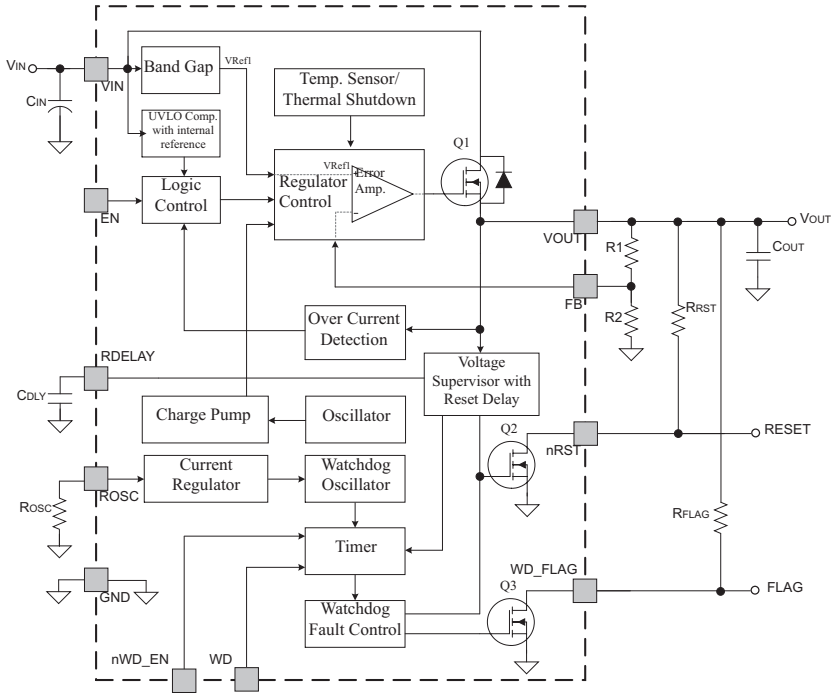


Figure 15. TPS7A6401-Q1 (Adjustable Output Voltage With Flag Output)

7.3 Feature Description

7.3.1 Power Up, Reset Delay, and Reset Output

During power up, the regulator incorporates a protection scheme to limit the current through the pass element and output capacitor. When the input voltage exceeds a certain threshold ($VIN_{(POWERUP)}$) level, the output voltage begins to ramp up as shown in Figure 16.

When starting up, and also when the output recovers from a negative voltage spike due to a load step or a dip in the input voltage for a specified duration, the device implements reset delay to indicate that output voltage is stable and in regulation.

When the output voltage reaches the power-on-reset threshold ($V_{TH(POR)}$) level, that is, 93% of regulated output voltage (3.3 V or 5 V, or a programmed value), a constant output current charges an external capacitor (C_{DLY}) to an internal threshold ($V_{TH(RDELAY)}$) voltage level. Then, nRST asserts high and C_{DLY} discharges through an internal load. This allows C_{DLY} to charge from approximately 0 V during the next power cycle.

Program the reset delay time by connecting an external capacitor (C_{DLY} ,100 pF to 100 nF) to the RDELAY pin. Equation 1 gives the delay time:

$$t_{POR} = \frac{CDLY \times 3}{1 \times 10^{-6}} \quad (1)$$

where

- t_{POR} = reset delay time in seconds
- C_{DLY} = reset delay capacitor value in farads

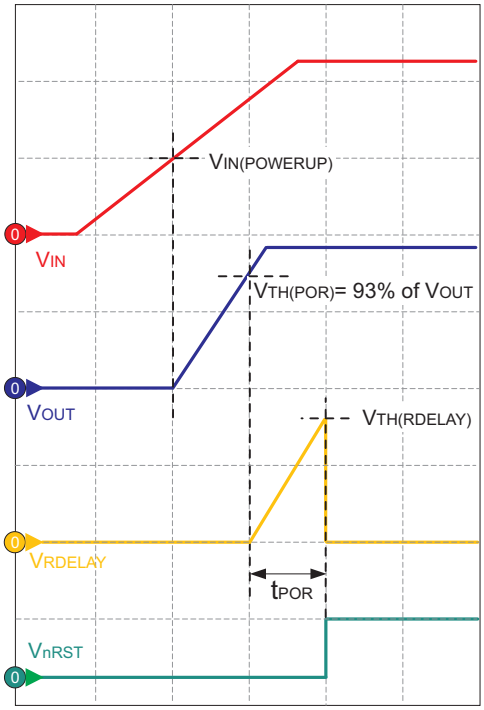


Figure 16. Power Up and Conditions for Activation of Reset

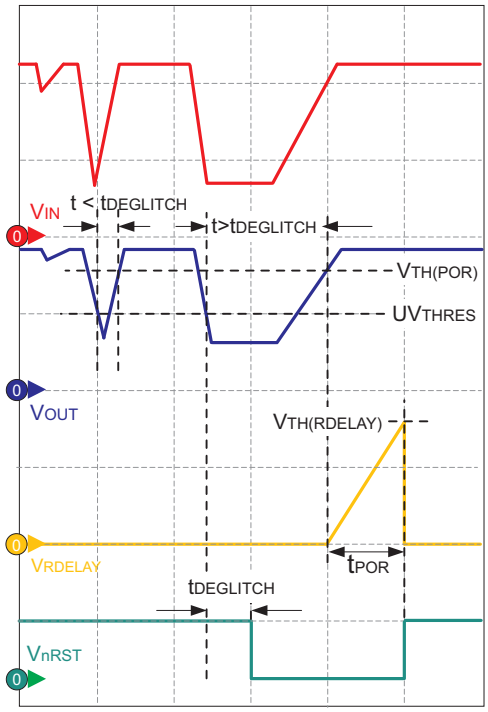


Figure 17. Reset Delay and Deglitch Filter

As Figure 17 shows, if the regulated output voltage falls below 93% of the set level, nRST asserts low after a short de-glitch time of approximately 5.5 µs (typical). In case of negative transients in the input voltage (V_{IN}), the reset signal asserts low only if the output (V_{OUT}) drops and stays below the reset threshold level ($V_{TH(POR)}$) for more than the deglitch time ($t_{DEGLITCH}$), as Figure 17 and Figure 20 illustrate. While nRST is low, if the input voltage returns to the nominal operating voltage, the normal power-up sequence ensues. nRST asserts high only if the output voltage exceeds the reset threshold voltage ($V_{TH(POR)}$) and the reset delay time (t_{POR}) has elapsed.

Feature Description (continued)

7.3.2 Adjustable Output Voltage

Program the regulated output voltage (V_{OUT}) by connecting external resistors to FB pin. Calculate the feedback resistor values using Equation 2.

$$V_{OUT} = V_{REF}\left[1 + \frac{R1}{R2}\right] \quad (2)$$

where

- V_{OUT}= desired output voltage
- V_{REF} = reference voltage (V_{REF}= 1.23 V, typically)
- R1, R2 = feedback resistors (see Figure 15)

Equation 3 gives the overall tolerance of the regulated output.

$$tol_{V_{OUT}} = tol_{V_{REF}} + \left[\frac{R1}{R1 + R2}\right]\left[tol_{R1} + tol_{R2}\right] \quad (3)$$

where

- tol_{VOUT} = tolerance of the output voltage
- tol_{VREF} = tolerance of the internal reference voltage (tol_{VREF} = ± 1.5% typically)
- tol_{R1},tol_{R2} = tolerance of feedback resistors R1, R2

For a tighter tolerance on V_{OUT}, select lower-value feedback resistors. TI recommends to select feedback resistors such that the sum of R1 and R2 is from 20 kΩ to 200 kΩ.

7.3.3 Chip Enable

These devices have a high-voltage-tolerant EN pin that an external microcontroller or a digital control circuit can use to enable and disable them. A high input to this pin activates the device and turns the regulator on. For self bias applications, connect this input to the VIN terminal. An internal pulldown resistor is connected to this pin, and therefore if this pin remains unconnected, the device stays disabled.

7.3.4 Charge Pump Operation

These devices have an internal charge pump which turns on or off depending on the input voltage and the output current. The charge pump switching circuitry must not cause conducted emissions to exceed required thresholds on the input voltage line. For a given output current, the charge pump stays on at lower input voltages and turns off at higher input voltages. The charge pump switching thresholds are hysteretic. Figure 18 and Figure 19 show typical switching thresholds for the charge pump at light (I_{OUT} < approximately 2 mA) and heavy (I_{OUT} > approximately 2 mA) loads, respectively.

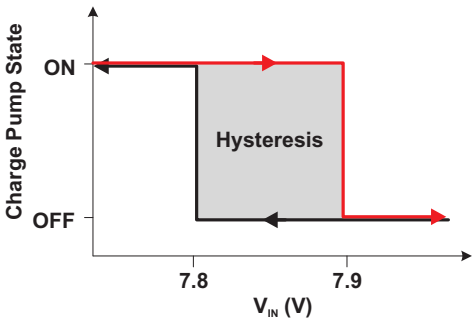


Figure 18. Charge Pump Operation at Light Loads

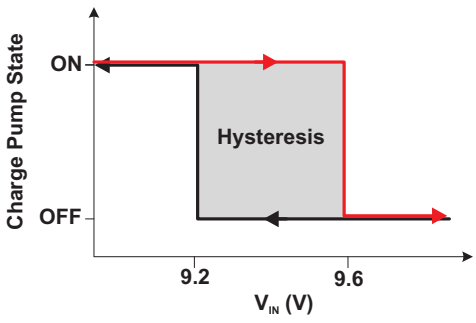


Figure 19. Charge Pump Operation at Heavy Loads

7.3.5 Low-Power Mode

At light loads and high input voltages (V_{IN} > approximately 8 V, such that the charge pump is off), the device operates in low-power mode and the quiescent current consumption is reduced to 25 µA (typical) as shown in Table 1.

Table 1. Typical Quiescent Current Consumption

I_{OUT}	Charge Pump ON	Charge Pump OFF
I_{OUT} < approximately 2 mA (Light load)	250 µA	35 µA (Low-power mode)
I_{OUT} > approximately 2 mA (Heavy load)	280 µA	70 µA

7.3.6 Undervoltage Shutdown

These devices have an integrated undervoltage lockout (UVLO) circuit to shut down the output if the input voltage (V_{IN}) falls below an internally fixed UVLO threshold level ($V_{IN-UVLO}$). This ensures that the regulator does not latch into an unknown state during low input voltage conditions. The regulator powers up when the input voltage exceeds the $V_{IN(POWERUP)}$ level, as Figure 20 shows.

7.3.7 Low-Voltage Tracking

At low input voltages, the regulator drops out of regulation, and the output voltage tracks the input minus a voltage based on the load current (I_{OUT}) and switch resistance (R_{SW}), as Figure 20 shows. This feature allows for a smaller input capacitor and can possibly eliminate the need of using a boost convertor during cold crank conditions, as Figure 20 shows.

7.3.8 Integrated Fault Protection

These devices feature integrated fault protection to make them ideal for use in automotive applications. In order to remain in a safe area of operation during certain fault conditions, the devices use internal current-limit protection and current-limit foldback to limit the maximum output current. This protects them from excessive power dissipation. For example, during a short-circuit condition on the output, fault protection limits the current through the pass element to I_{CL} to protect the device from excessive power dissipation.

7.3.9 Thermal Shutdown

These devices incorporate a thermal shutdown (TSD) circuit as a protection from overheating. For continuous normal operation, the junction temperature should not exceed the TSD trip point. The junction temperature exceeding the TSD trip point causes the output to turn off. When the junction temperature falls below TSD trip point, the output turns on again, as Figure 21 shows.

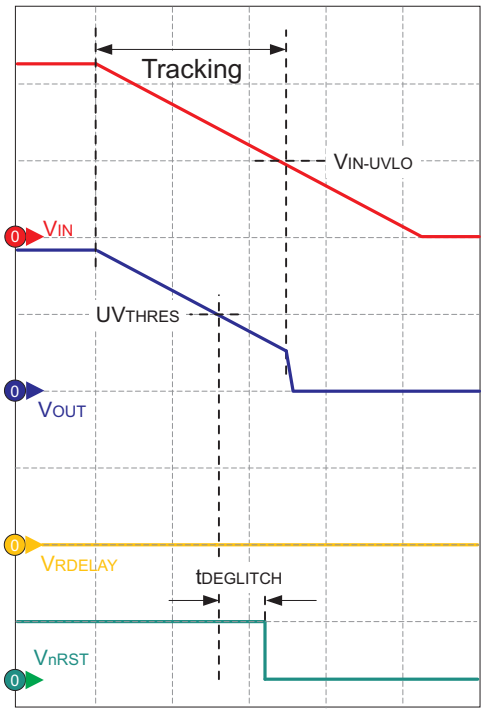


Figure 20. Low-Voltage Tracking and Undervoltage Lockout

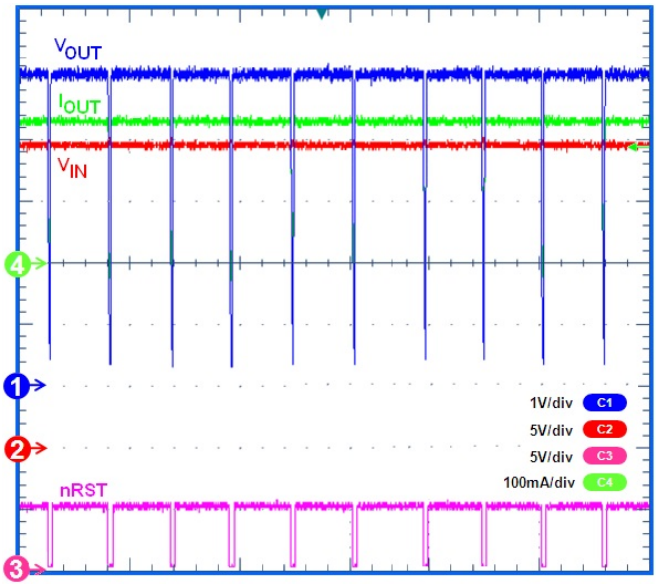


Figure 21. Thermal Cycling Waveform for TPS7A6350-Q1 (V_{IN}= 24 V, I_{OUT}= 200 mA, V_{OUT}= 5 V)

7.3.10 Integrated Window Watchdog

These devices have an integrated watchdog with fault (WD_FLT) and flag (WD_FLAG) output options. Both device options are available in fixed- and adjustable-output versions. The watchdog operation, service fault conditions, and difference between fault (TPS7A63-Q1) and flag (TPS7A6401-Q1) output versions are described as follows.

7.3.10.1 Programmable-Window Watchdog

Program the duration of the watchdog window by connecting an external resistor (R_{OSC}) to ground at the ROSC pin. The current through the resistor sets the clock frequency of the internal oscillator. The user can adjust the duration of the watchdog window (that is, the watchdog timer period) by changing the resistor value. The duration of the watchdog window and the duration of the fault output are multiples of the internal oscillator frequency and are given by the following equations:

$$t_{WD} = 10^{-6} \times R_{OSC} = 5000 \times 1 / f_{OSC} \quad (4)$$

$$t_{WD\_OUT} = 1 / f_{OSC} \quad (5)$$

$$t_{CW} = t_{OW} = 1 / 2\ t_{WD}$$

where

- t_{WD} = width of watchdog window
- R_{OSC} = resistor connected at ROSC pin
- t_{WD_OUT} = duration of fault output
- f_{OSC} = frequency of internal oscillator
- t_{CW} = duration of closed window
- t_{OW} = duration of open window (6)

As shown in Figure 22, each watchdog window consists of an open window and a closed window, each having a width approximately 50% of the watchdog window. However, there is an exception to this; the first open window after watchdog initialization is eight times the duration of the watchdog window. All open windows except the one after watchdog initialization are one-half the width of the watchdog window. On initialization, the watchdog must receive service (by software, external microcontroller, and so forth) only during an open window. A watchdog serviced during a closed window, or not serviced during a open window, creates a watchdog fault condition.

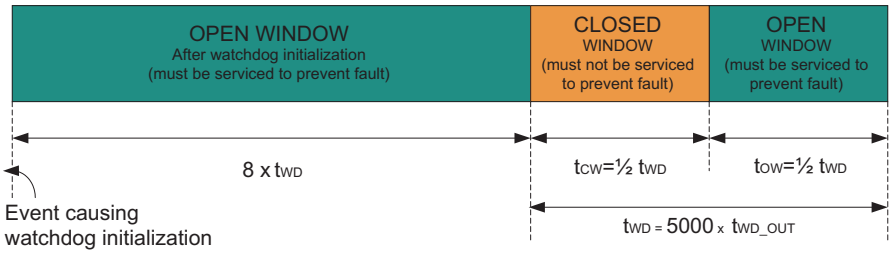


Figure 22. Watchdog Window Duration

7.3.10.2 Watchdog Enable

An external microcontroller or a digital circuit can apply an appropriate signal to the nWD_EN pin to enable or disable the watchdog. A low input to this pin turns the watchdog on. Because of an internal pulldown resistor connected to this pin, leaving the pin unconnected keeps the watchdog enabled.

7.3.10.3 Watchdog Service Signal

In order for the watchdog service signal (WD) to service an open window correctly, the service signal must stay high for a duration of at least t_{WD_HOLD}. The recommended value of t_{WD_HOLD} is given by Equation 7:

$$t_{WD\_HOLD} = 3 \times t_{WD\_OUT} \quad (7)$$

7.3.10.4 Watchdog Fault Outputs

The WD_FLT pin and WD_FLAG pin are fault output terminals for the TPS7A63-Q1 and TPS7A6401-Q1 devices, respectively. Typically, one pulls these fault outputs high to a regulated output supply. In the case of a watchdog fault condition, the TPS7A63-Q1 momentarily pulls WD_FLT low for a duration of t_{WD_OUT}, whereas the TPS7A6401-Q1 latches the WD_FLAG high and momentarily pulls nRST low for a duration of t_{WD_OUT}.

7.3.10.5 Watchdog Initialization

On power up and during normal operation, the watchdog initializes under the conditions shown in Table 2. The normal operation of the watchdog for the WD_FLT and WD_FLAG output device options is shown in Figure 23 and Figure 24, respectively.

Table 2. Conditions For Watchdog Initialization

Edge	What causes watchdog to initialize?	TPS7A63-Q1 (FAULT Option)	TPS7A6401-Q1 (FLAG Option)
	Rising edge of nRST (when V_{OUT} exceeds $V_{TH(POR)}$) while the watchdog is in the enabled state, for example, during soft power up	✓	✓
	Falling edge of nWD_EN while the nRST is already high, for example, when the microprocessor enables the watchdog after the device is powered up	✓	✓
	Rising edge of WD_FLT while the nRST is already high and the watchdog is in the enabled state, for example, right after a closed window is serviced	✓	X

7.3.10.6 Watchdog Operation

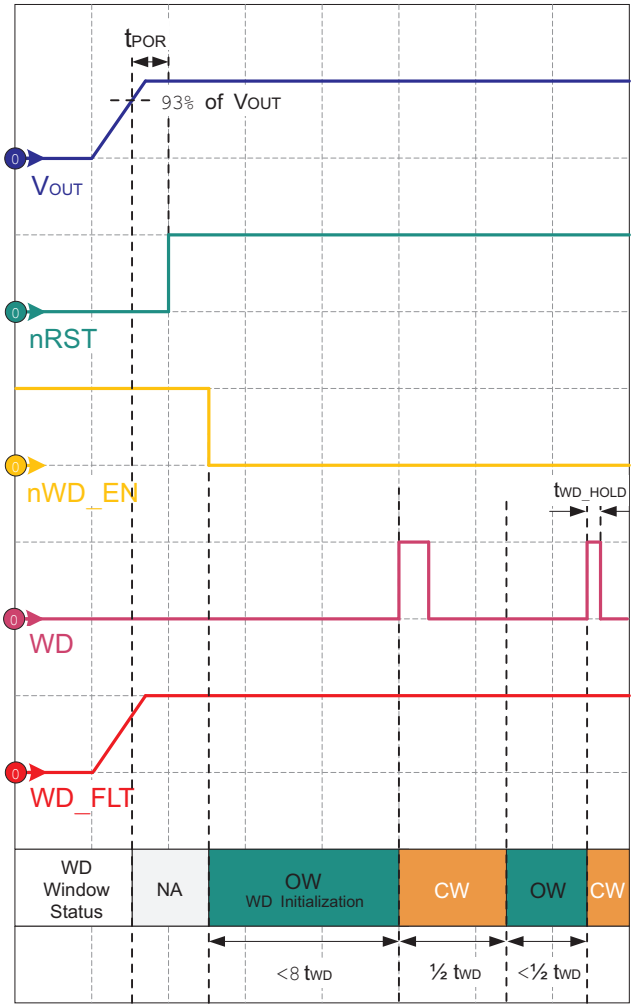


Figure 23. Power Up, Initialization, and Normal Operation for TPS7A63-Q1

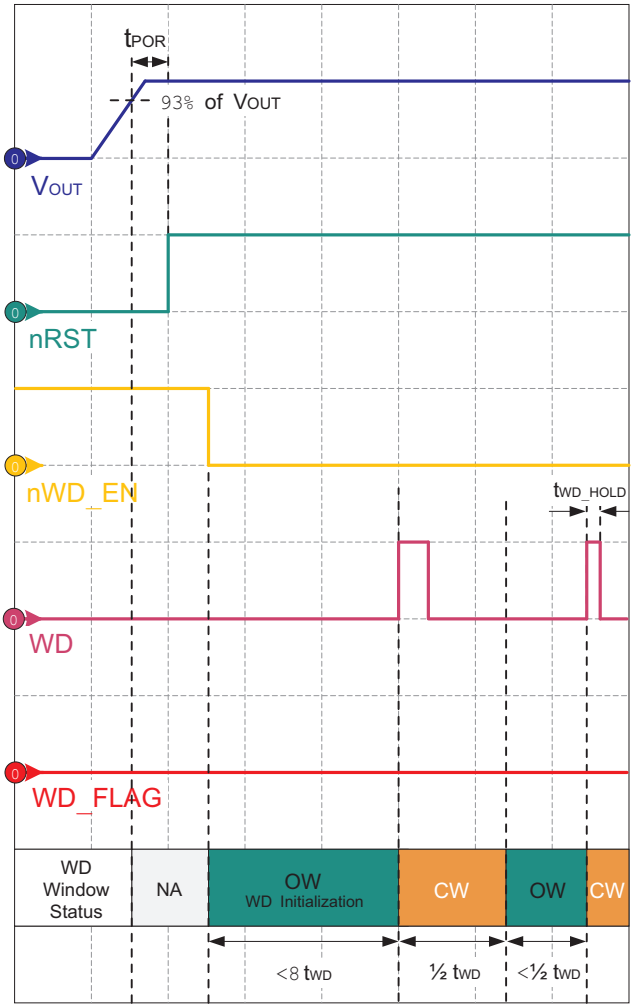


Figure 24. Power Up, Initialization, and Normal Operation for TPS7A6401-Q1

Figure 23 shows watchdog initialization and operation for the TPS7A63-Q1. After output voltage is in regulation and reset asserts high (clearly the chip-enable pin is high), the watchdog becomes enabled when an external signal pulls nWD_EN (the watchdog enable pin) low. This causes the watchdog to initialize and wait for a service signal during the first open window for 8× the duration of t_{WD}. A service signal applied to the WD pin during the first open window resets the watchdog counter and a closed window starts. To prevent a fault condition from occurring, watchdog service must not occur during the closed window. Watchdog service must occur during the following open window to prevent fault condition from occurring. The fault output (WD_FLT), externally pulled up to VOUT (typically), stays high as long as the watchdog receives proper serviced and there is no fault condition.

Figure 24 shows watchdog initialization and operation for FLAG output version (TPS7A6401-Q1). The fault output (WD_FLAG), externally pulled up to VOUT (typically), stays low as long as the watchdog receives proper service and there is no fault condition.

Likewise, enabling the watchdog before powering the device on (that is, pulling the nWD_EN pin low before power up), the watchdog initializes as soon as the output voltage is in regulation and reset asserts high (see Table 2 for Conditions for Watchdog Initialization).

7.3.10.7 Watchdog Fault Conditions

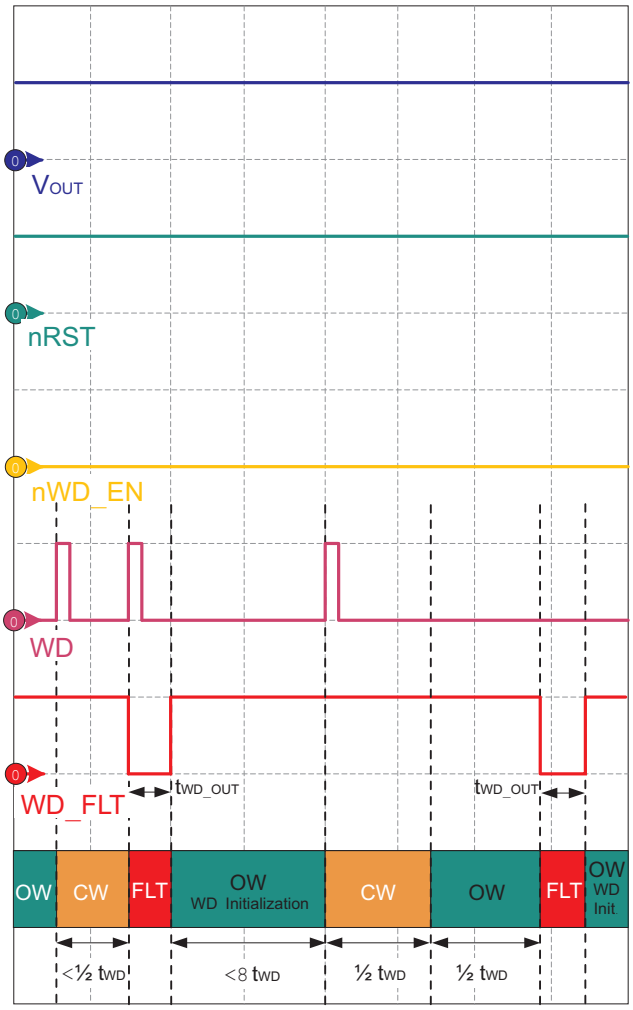


Figure 25. Watchdog Service Fault Conditions for TPS7A63-Q1

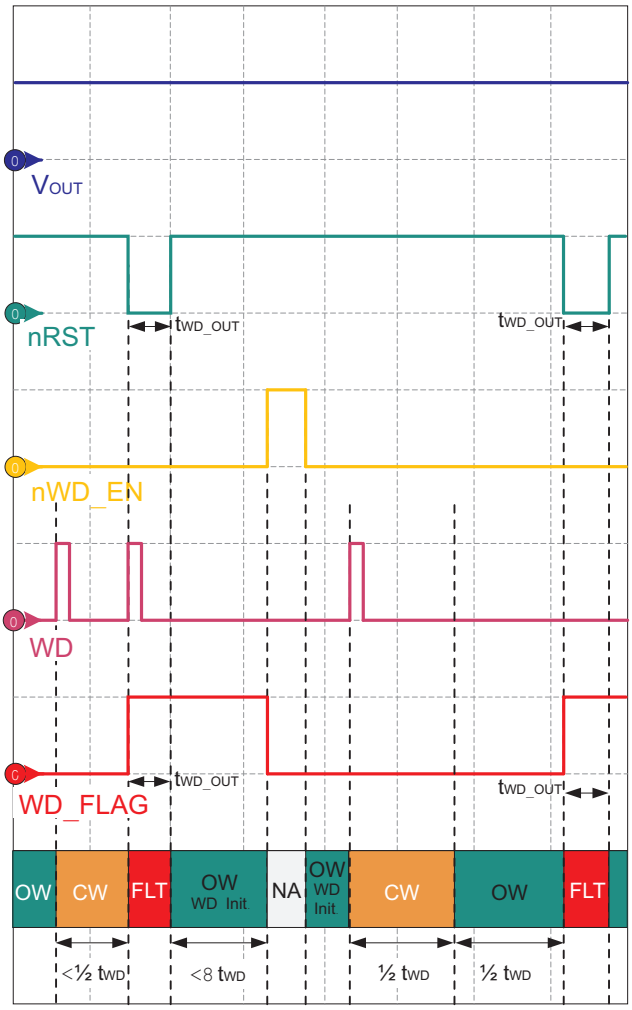


Figure 26. Watchdog Service Fault Conditions for TPS7A6401-Q1

For both device options, a watchdog fault condition occurs in following (non-exhaustive) cases:

- When the watchdog receives service during a closed window.
- When watchdog does not receive service during an open window (this open window could be the one after watchdog initialization, or the one following a closed window).

As shown in Figure 25, for TPS7A63-Q1 the first watchdog fault registers when the watchdog receives service during a closed window. This causes the watchdog fault pin (WD_FLT) to go low temporarily for a duration of t_{WD_OUT}. Following the fault, the watchdog reinitializes. Likewise, the second fault registers when the watchdog does not receive service during an open window (following a closed window). Again, the fault pin (WD_FLT) is asserts low for a duration of t_{WD_OUT}.

As shown in Figure 26, for TPS7A6401-Q1 the first watchdog fault registers when watchdog receives service during a closes window. This causes the watchdog flag pin (WD_FLAG) to become high and stay latched. At the same time, nRST pin goes low temporarily for the duration of t_{WD_OUT}. WD_FLAG remains high until toggling the nWD_EN pin disables and re-enables the watchdog or the watchdog receives service properly (while nWD_EN is low and nRST is high). The second fault registers when the watchdog does not receive service during an open window (following a closed window). While WD_FLAG is high (that is, during a fault condition), if the watchdog stays enabled, and reset is high; a watchdog service signal can also bring WD_FLAG low (about 5 µs after the watchdog receives service).

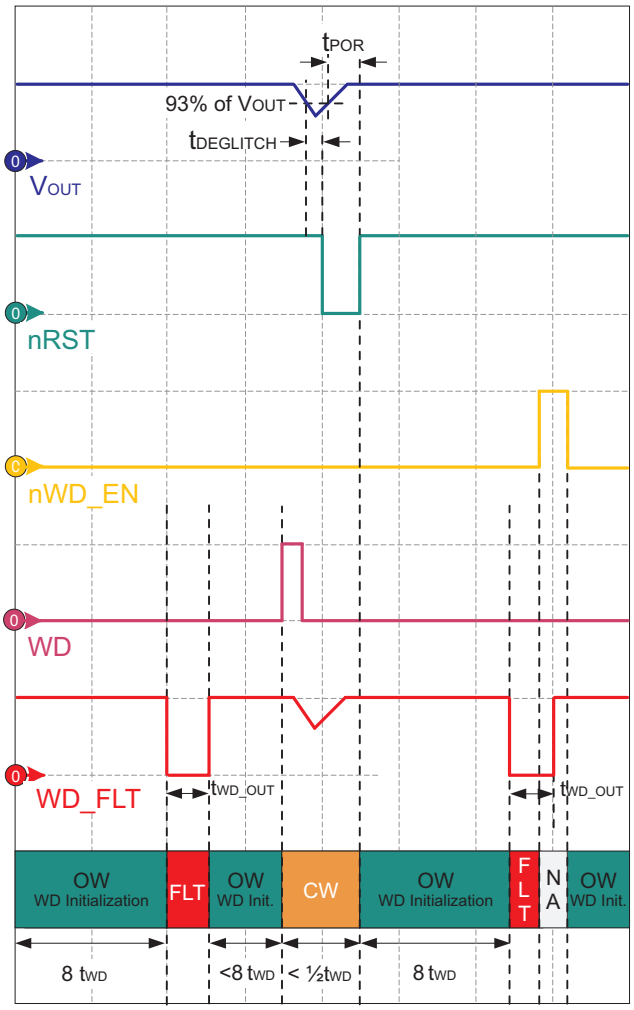


Figure 27. Watchdog Fault During Initialization, and Reinitialization During Reset for TPS7A63-Q1

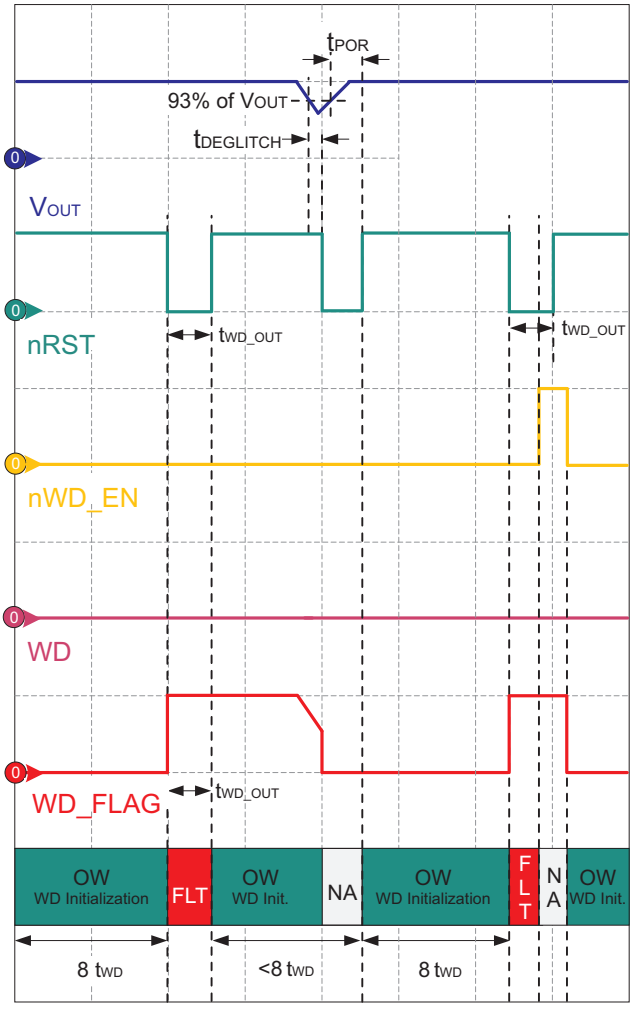


Figure 28. Watchdog Fault During Initialization, and Reinitialization During Reset for TPS7A6401-Q1

As shown in Figure 27 for the TPS7A6401-Q1, the watchdog fault condition also occurs if the watchdog does not receive service during the open window after watchdog initialization. That is, if the watchdog does not receive service during the first 8× t_{WD_OUT} period after initialization, a fault condition occurs. This causes the watchdog fault pin (WD_FLT) to go low temporarily for a duration of t_{WD_OUT}. In case of a load transient, if the regulated output voltage drops down causing reset (nRST) to go low, the rising edge on nRST causes the watchdog to reinitialize (that is, when reset becomes high with the watchdog still enabled). During a fault condition (that is, WD_FLT is low) with the watchdog disabled, the fault output continues to stay low until t_{WD_OUT} is elapsed. A falling edge on nWD_EN pin causes the watchdog to reinitialize while nRST is still high.

As shown in Figure 28 for the TPS7A6401-Q1, the watchdog fault condition also occurs if the watchdog does not receive service during the open window after watchdog initialization. That is, if the watchdog does not receive service in first 8× t_{WD_OUT} period after initialization, a fault condition occurs. This causes the watchdog flag pin (WD_FLAG) to become high and stay latched. At the same time, the nRST pin goes low temporarily for a duration of t_{WD_OUT}. In the case of a load transient, if the regulated output voltage drops down causing the reset output to go low, the WD_FLAG asserts low, and the rising edge on nRST causes the watchdog to reinitialize (while the watchdog remains enabled). During a fault condition (that is, WD_FLAG is high), and with a disabled watchdog, the flag output continues to stay high as long as the watchdog remains enabled or receives proper service. However, nRST stays low until t_{WD_OUT} elapses. Re-enabling the watchdog causes watchdog to reinitialize (while nRST is still high).

7.4 Device Functional Modes

7.4.1 Operation With V_{IN} Lower Than 4 V

The TPS7A63-Q1 and TPS7A6401-Q1 family devices operate with input voltage above 4 V. The typical UVLO voltage is 3.16 V. The device can operate at input voltage lower than 4 V, but at input voltage below the actual UVLO, the device will shut down.

7.4.2 Operation With V_{IN} Larger Than 4 V

When V_{IN} is greater than 4 V, if the input voltage is higher than V_{OUT} plus the dropout voltage, the output voltage is equal to the set value. Otherwise, the output voltage is equal to VIN minus the dropout voltage.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Typical application circuits for TPS76333-Q1/TPS76350-Q1 and TPS7A6401-Q1 are shown in Figure 29 and Figure 32. Depending on the end application, one may use different values of external components. Carefully select feedback resistors (R1 and R2), used to program the output voltage. Using smaller resistors results in higher current consumption, whereas using very large resistors impacts the sensitivity of the regulator. Therefore, TI recommends selecting feedback resistors such that the sum of R1 and R2 is from 20 kΩ to 200 kΩ.

8.1.1 Example

If the desired regulated output voltage is 5 V, after selecting R2 then one can calculate R1 using (or vice versa) Equation 2. Knowing V_{REF} = 1.23 V (typical), V_{OUT} = 5 V, selecting R2 = 20 kΩ, the calculated value of R1 is 61.3 kΩ.

During fast load steps, an application may require a larger output capacitor to prevent the output from temporarily dropping down. TI recommends a low-ESR ceramic capacitor with dielectric of type X5R or X7R. One can also connect a bypass capacitor at the output to decouple high-frequency noise as per the end application.

8.2 Typical Applications

8.2.1 Typical Application Using the TPS7A6333-Q1 or TPS7A6350-Q1

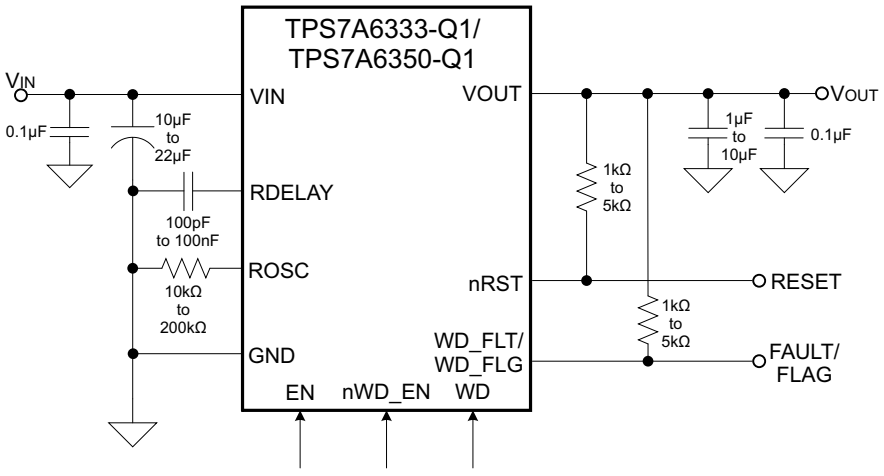


Figure 29. Typical Application Schematic, TPS7A6333-Q1/6350-Q1

Typical Applications (continued)

8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 3.

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUES
Input voltage range	7 V - 40 V
Input capacitor range	10 µF - 22 µF
Output voltage	3.3 V, 5 V
Output current rating	300 mA maximum
Output capacitor range	1 µF-10 µF

8.2.1.2 Detailed Design Procedure

When using the TPS7A6333-Q1, TPS7A6350-Q1, TI recommends adding a 10-µF to 22-µF capacitor to the input to keep the input voltage stable. TI also recommends adding a 1-µF to 10-µF low ESR ceramic capacitor to get a stable output.

The reset delay time is set by an external capacitor (CDLY) to ground, capacitor value typical from 100 pF to 100 nF. Equation 1 provides the method for the calculation.

Connecting an external resistor to ground at the ROSC pin can set the duration of the watchdog window. Equation 4 provides the method for the calculation. Usually a 10-kΩ to 200-kΩ resistor can be used to set the time.

8.2.1.3 Application Curves

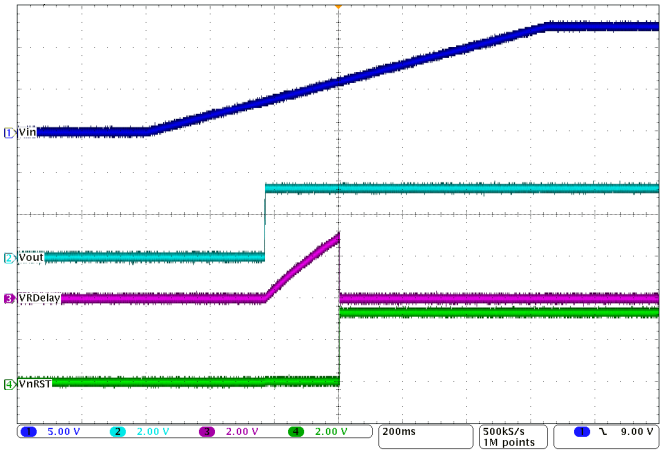


Figure 30. TPS7A6333-Q1 Power Up Waveform

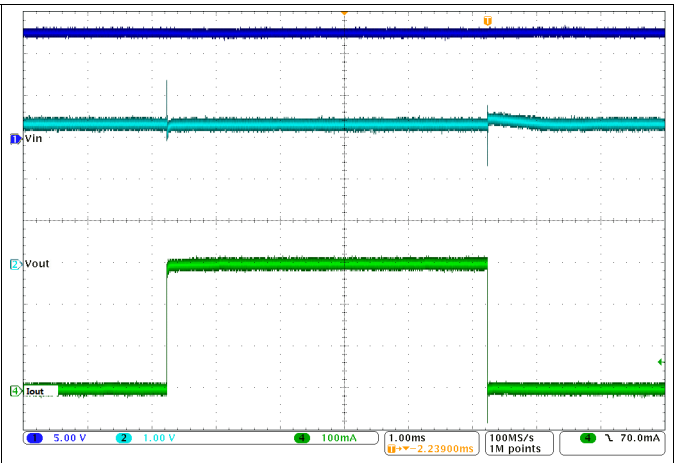


Figure 31. TPS7A6333-Q1 Load Transient Waveform

8.2.2 Typical Application Using the TPS7A6401-Q1

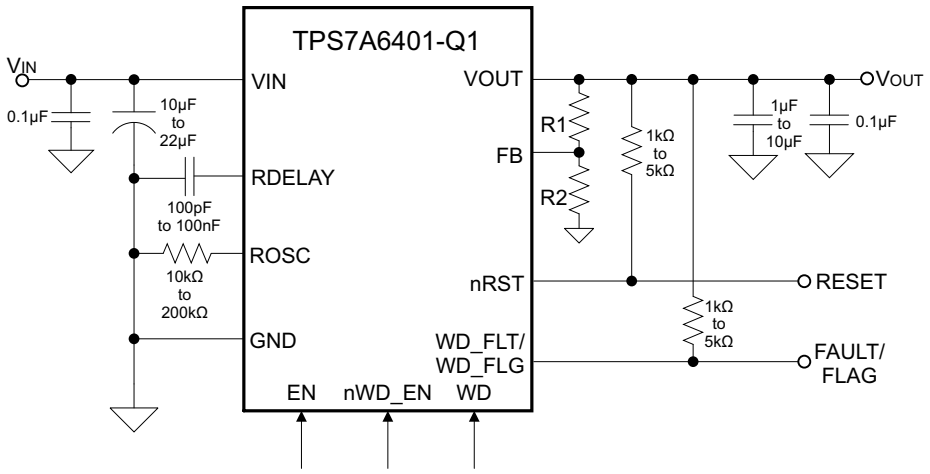


Figure 32. Typical Application Schematic TPS7A6401-Q1

8.2.2.1 Design Requirements

For this design example, use the parameters listed in Table 4.

Table 4. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUES
Input voltage range	7 V - 40 V
Input capacitor range	10 µF-22 µF
Output voltage	2.5 V - 7 V
Output current rating	300 mA maximum
Output capacitor range	1 µF-10 µF

8.2.2.2 Detailed Design Procedure

When using TPS7A6401-Q1, TI recommends adding a 10-µF to 22-µF capacitor to the input to keep the input voltage stable. TI also recommends adding a 1-µF to 10-µF low ESR ceramic capacitor to get a stable output.

The output voltage is set by the R1 and R2 resistor network. Output voltage can be calculated by Equation 2.

The reset delay time is set by an external capacitor (CDLY) to ground, capacitor value typical from 100 pF to 100 nF. Equation 1 provides the method for the calculation. Connecting an external resistor to ground at the ROSC pin can set the duration of the watchdog window. Equation 4 provides the method for the calculation. Usually a 10-kΩ to 200-kΩ resistor can be used to set the time.

8.2.2.3 Application Curves

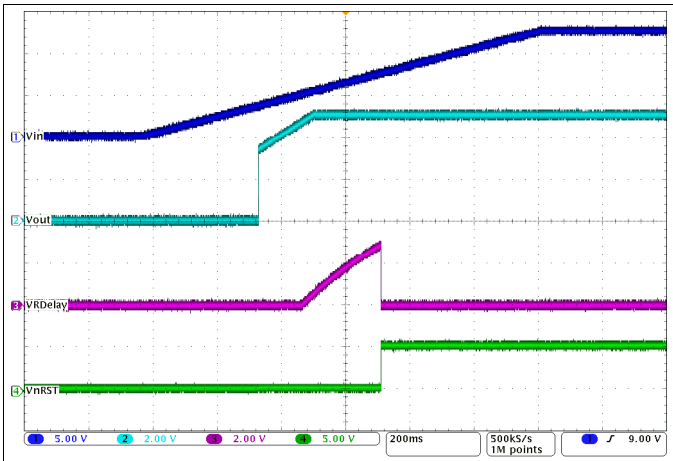


Figure 33. TPS7A6401-Q1 Power Up Waveform

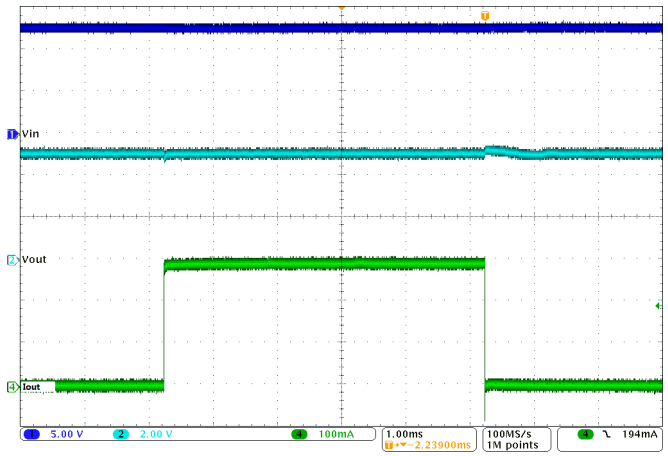


Figure 34. TPS7A6401-Q1 Load Transient Waveform

9 Power Supply Recommendations

The device is designed to operate from an input-voltage supply range from 7 V to 40 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS7A63XX-Q1 or TPS7A64XX-Q1 device, TI recommends adding an electrolytic capacitor with a value of 10 µF and a ceramic bypass capacitor at the input.

10 Layout

10.1 Layout Guidelines

For the LDO power supply, especially these high voltage and large current ones, layout is an important step. If layout is not carefully designed, the regulator could not deliver enough output current because of the thermal limitation. To improve the thermal performance of the device, and maximize the current output at high ambient temperature, it is recommended to spread the thermal pad as large as possible and put enough thermal vias on the thermal pad. Figure 37 shows an example layout.

10.1.1 Power Dissipation and Thermal Considerations

Calculated the power dissipated in the device using Equation 8.

$$P_D = I_{OUT} \times (V_{IN} - V_{OUT}) + I_{QUIESCENT} \times V_{IN}$$

where

- P_D = continuous power dissipation
- I_{OUT} = output current
- V_{IN} = input voltage
- V_{OUT} = output voltage
- $I_{QUIESCENT}$ = quiescent current

(8)

As $I_{QUIESCENT} << I_{OUT}$, therefore, ignore the term $I_{QUIESCENT} \times V_{IN}$ in Equation 8.

For a device in operation at a given ambient air temperature (T_A), calculate the junction temperature (T_J) using Equation 9.

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where

- $R_{\theta JA}$ = junction-to-ambient-air thermal impedance

(9)

Calculate the rise in junction temperature due to power dissipation using Equation 10.

Layout Guidelines (continued)

$$\Delta T = T_J - T_A = (R_{\theta JA} \times P_D) \quad (10)$$

For a given maximum junction temperature ($T_{J\text{-}Max}$), calculate the maximum ambient air temperature ($T_{A\text{-}Max}$) at which the device can operate using Equation 11.

$$T_{A\text{-}Max} = T_{J\text{-}Max} - (R_{\theta JA} \times P_D) \quad (11)$$

10.1.1.1 Example

If I_{OUT} = 100 mA, V_{OUT} = 5 V, V_{IN} = 14 V, $I_{QUIESCENT}$ = 250 µA, and $R_{\theta JA}$= 50°C/W, the continuous power dissipated in the device is 0.9 W. The rise in junction temperature due to power dissipation is 45°C. For a maximum junction temperature of 150°C, the maximum ambient air temperature at which the device can operate is 105°C.

For adequate heat dissipation, TI recommends soldering the thermal pad (exposed heat sink) to the thermal land pad on the PCB. Doing this provides a heat conduction path from the die to the PCB and reduces overall package thermal resistance. Power derating curves for the TPS7A63-Q1 and TPS7A6401-Q1 PWP package and TPS7A6333-Q1 DRK are comparable; see Figure 35.

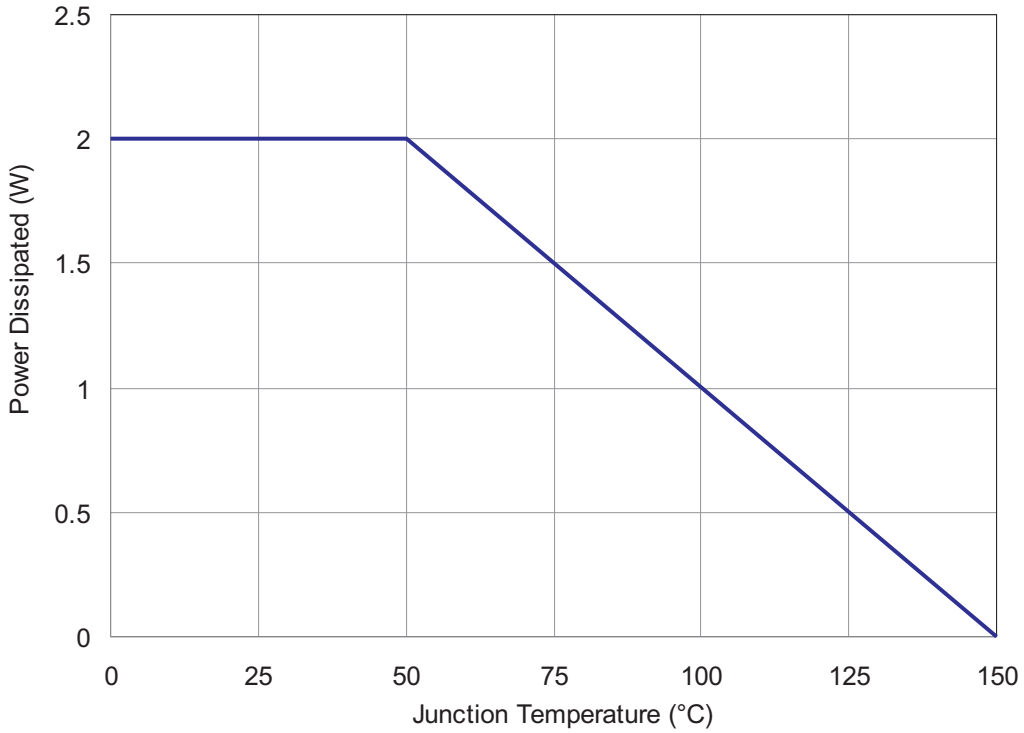


Figure 35. Power Derating Curve

For optimum thermal performance, TI recommends using a high-K PCB with thermal vias between the ground plane and solder pad or thermal land pad; see Figure 36 (a) and (b). Further, use a thicker ground plane and a thermal land pad with a larger surface area to inprove considerably the heat-spreading capabilities of a PCB. For a two-layer PCB, a bat wing layout can enhance the heat-spreading capabilities.

Layout Guidelines (continued)

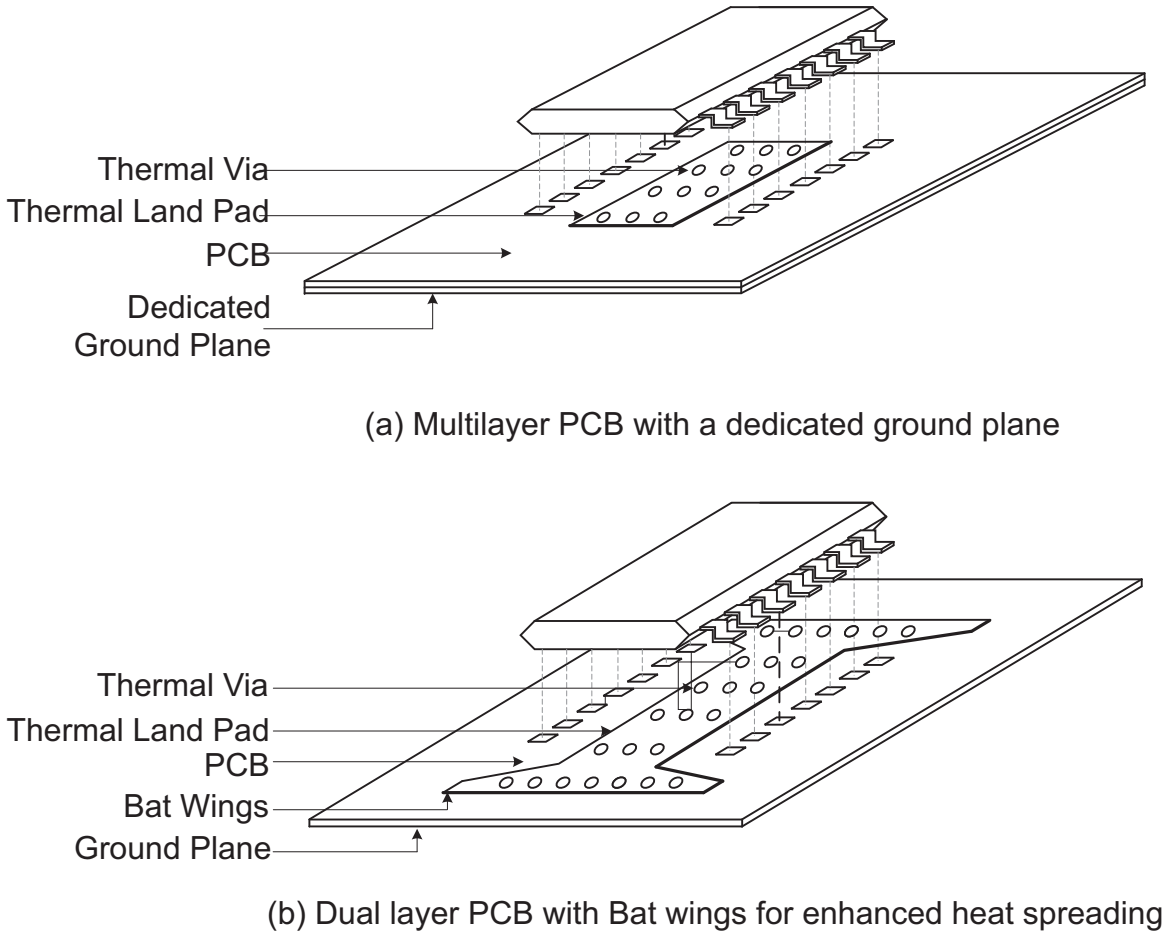


Figure 36. Using Multilayer PCB and Thermal Vias for Adequate Heat Dissipation

Keeping other factors constant, surface area of the thermal land pad contributes to heat dissipation only to a certain extent.

10.2 Layout Example

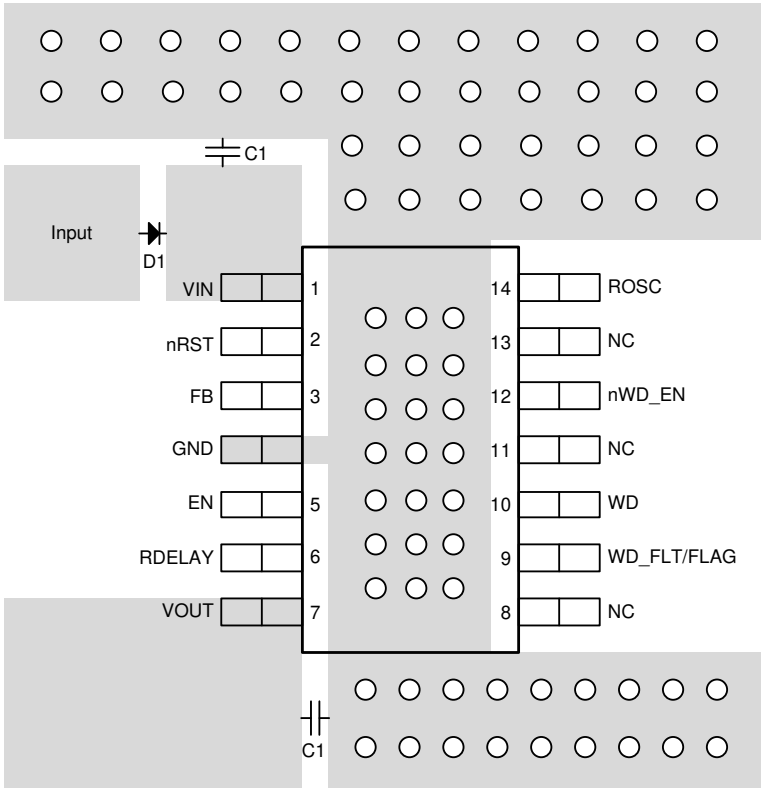


Figure 37. Layout Recommendation

11 デバイスおよびドキュメントのサポート

11.1 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびご注文へのクイック・アクセスが含まれます。

表 5. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
TPS7A63-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TPS7A6401-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 コミュニティ・リソース

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.4 商標

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11.5 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7A6301QPWPRQ1	Active	Production	HTSSOP (PWP) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	7A6301
TPS7A6301QPWPRQ1.A	Active	Production	HTSSOP (PWP) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	7A6301
TPS7A6333QDRKRQ1	Active	Production	VSON (DRK) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	PRGQ
TPS7A6333QDRKRQ1.A	Active	Production	VSON (DRK) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	PRGQ
TPS7A6333QPWPRQ1	Active	Production	HTSSOP (PWP) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	7A6333
TPS7A6333QPWPRQ1.A	Active	Production	HTSSOP (PWP) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	7A6333
TPS7A6350QPWPRQ1	Active	Production	HTSSOP (PWP) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	7A6350
TPS7A6350QPWPRQ1.A	Active	Production	HTSSOP (PWP) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	7A6350
TPS7A6401QPWPRQ1	Active	Production	HTSSOP (PWP) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	7A6401
TPS7A6401QPWPRQ1.A	Active	Production	HTSSOP (PWP) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	7A6401

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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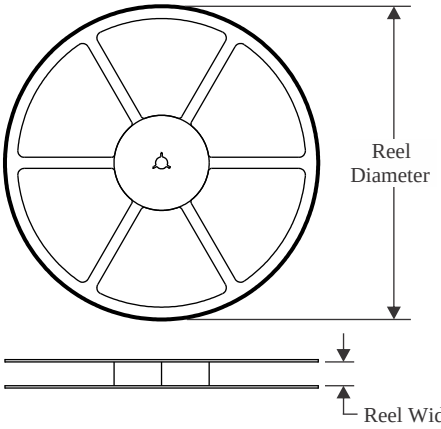
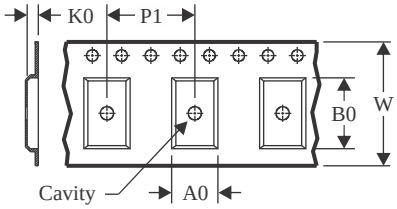
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

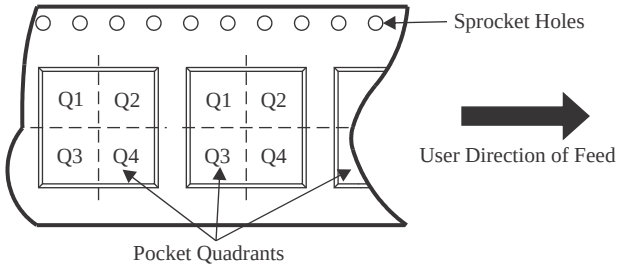


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

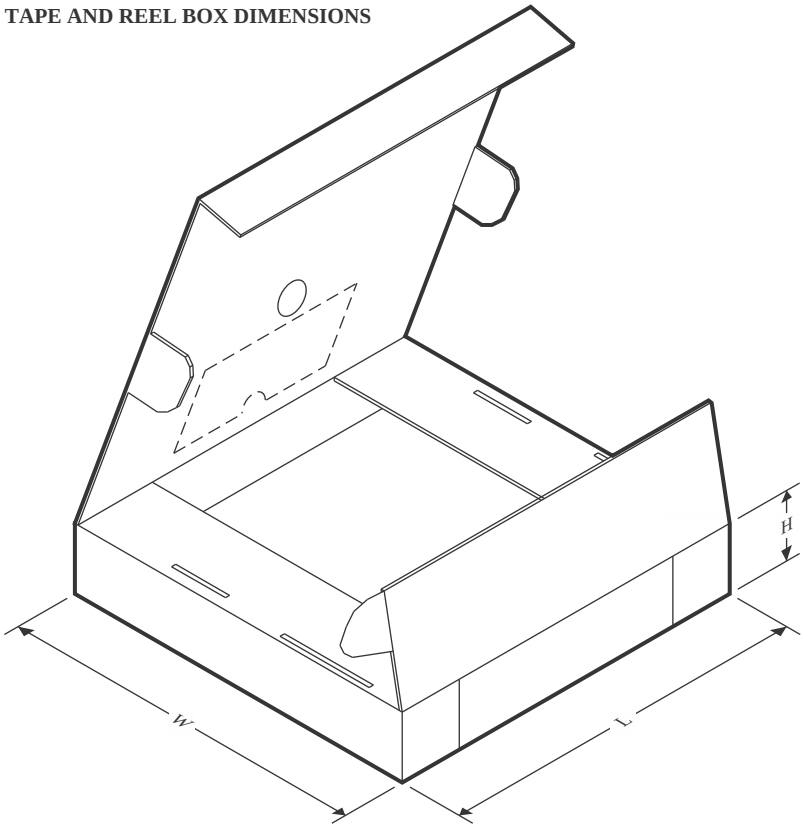
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A6301QPWPRQ1	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS7A6333QDRKRQ1	VSON	DRK	10	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
TPS7A6333QPWPRQ1	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS7A6350QPWPRQ1	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS7A6401QPWPRQ1	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

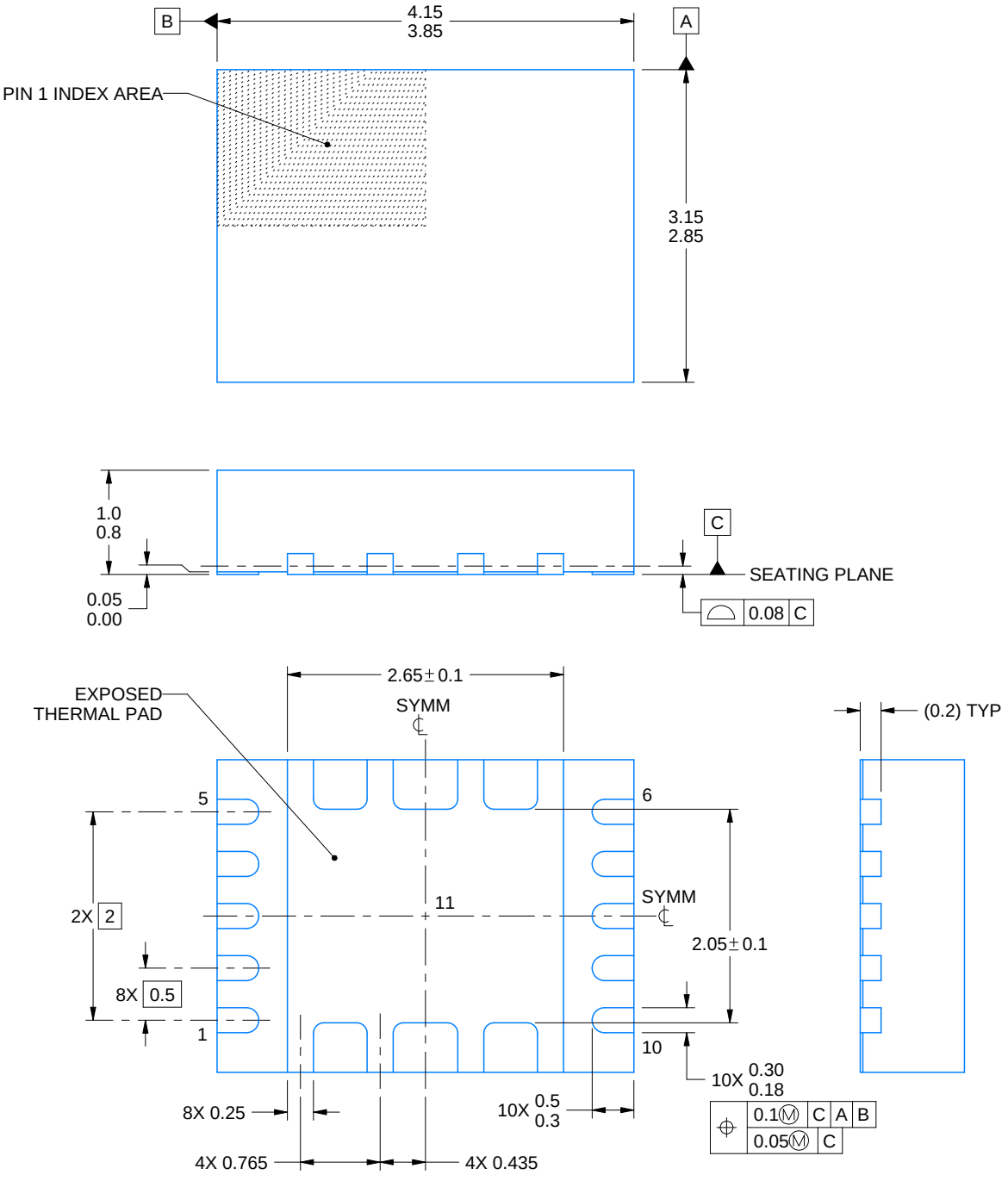
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A6301QPWPRQ1	HTSSOP	PWP	14	2000	350.0	350.0	43.0
TPS7A6333QDRKRQ1	VSON	DRK	10	3000	353.0	353.0	32.0
TPS7A6333QPWPRQ1	HTSSOP	PWP	14	2000	350.0	350.0	43.0
TPS7A6350QPWPRQ1	HTSSOP	PWP	14	2000	350.0	350.0	43.0
TPS7A6401QPWPRQ1	HTSSOP	PWP	14	2000	350.0	350.0	43.0

PACKAGE OUTLINE

DRK0010A

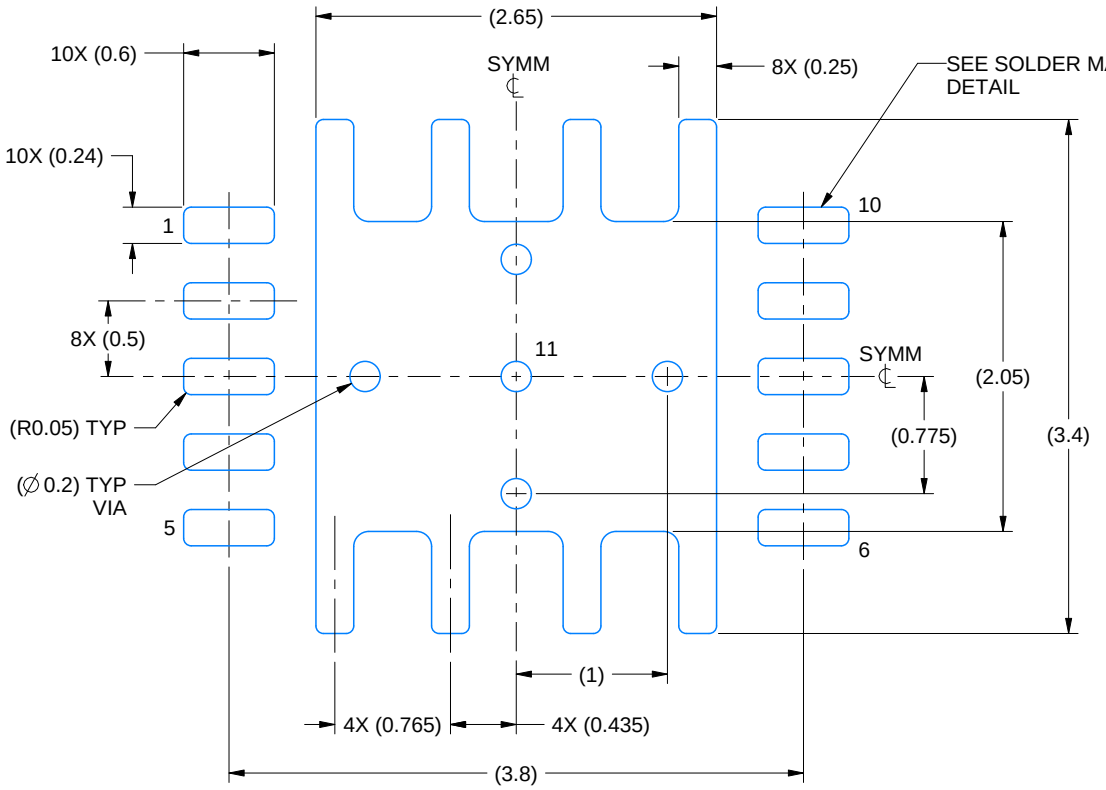
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

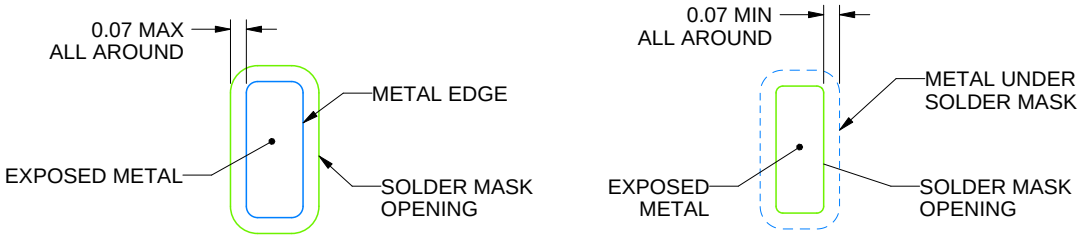


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON SOLDER MASK DEFINED (PREFERRED)

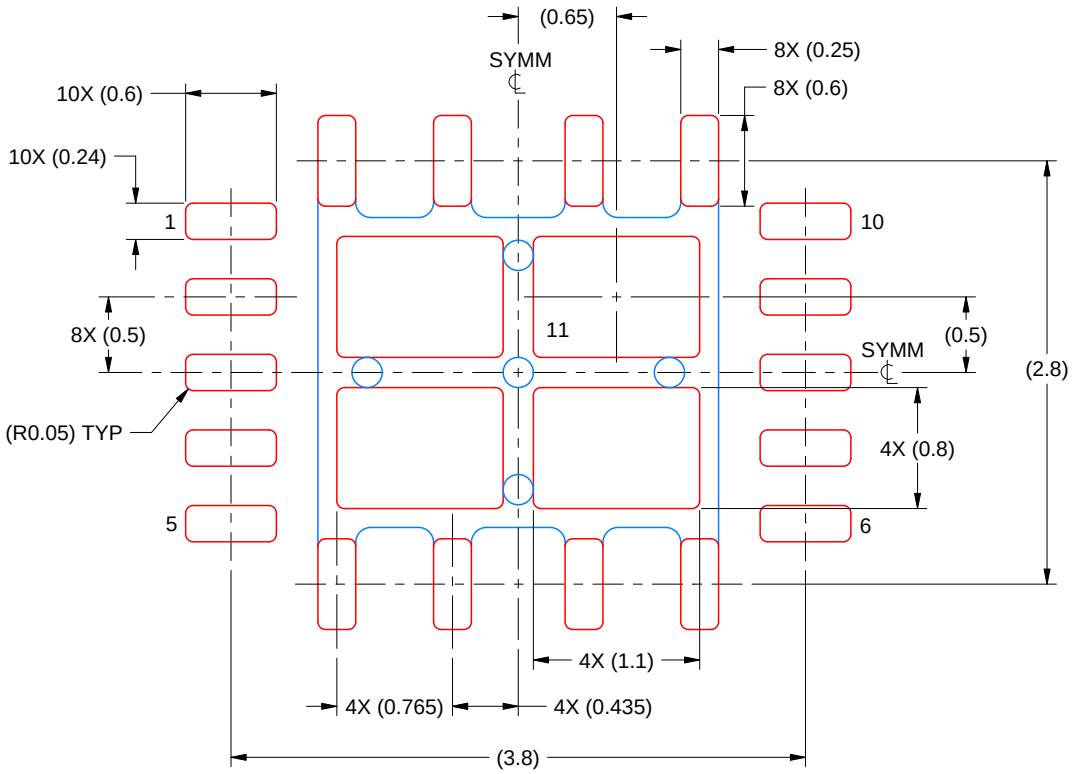
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4218888/A 02/2025

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 11
70% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4218888/A 02/2025

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

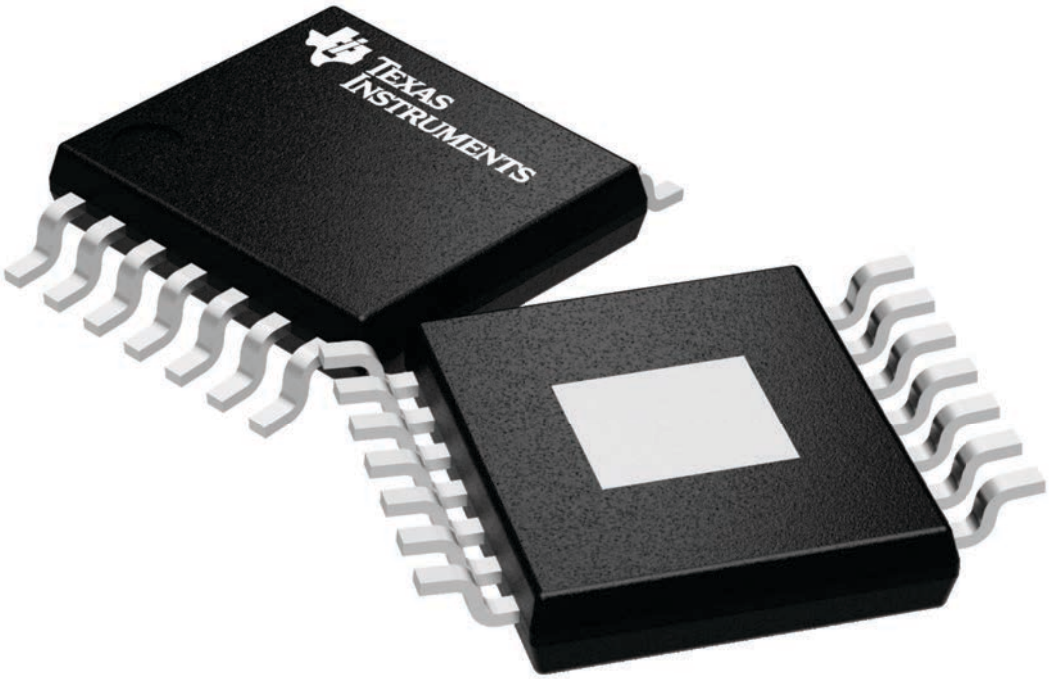
PWP 14

PowerPAD TSSOP - 1.2 mm max height

4.4 x 5.0, 0.65 mm pitch

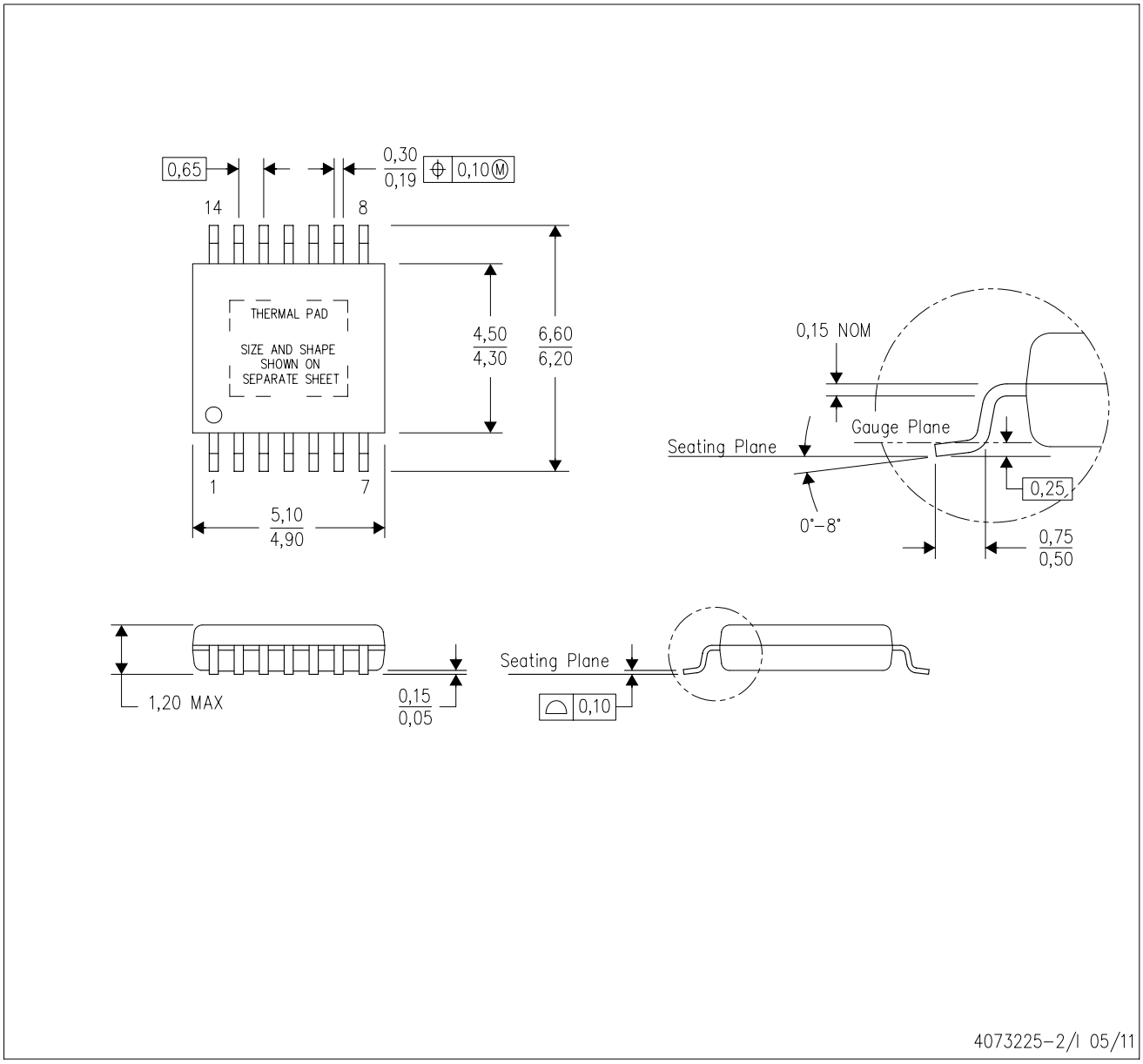
PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224995/A

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

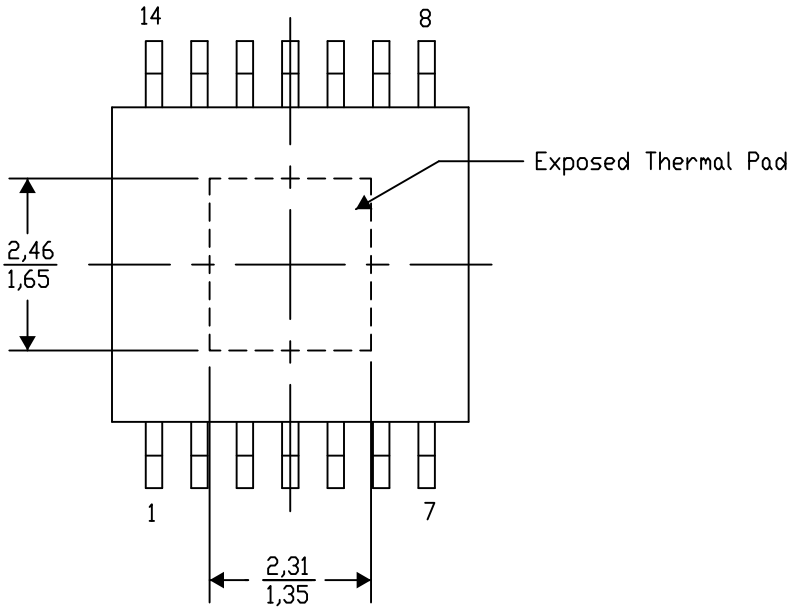
PWP (R–PDSO–G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

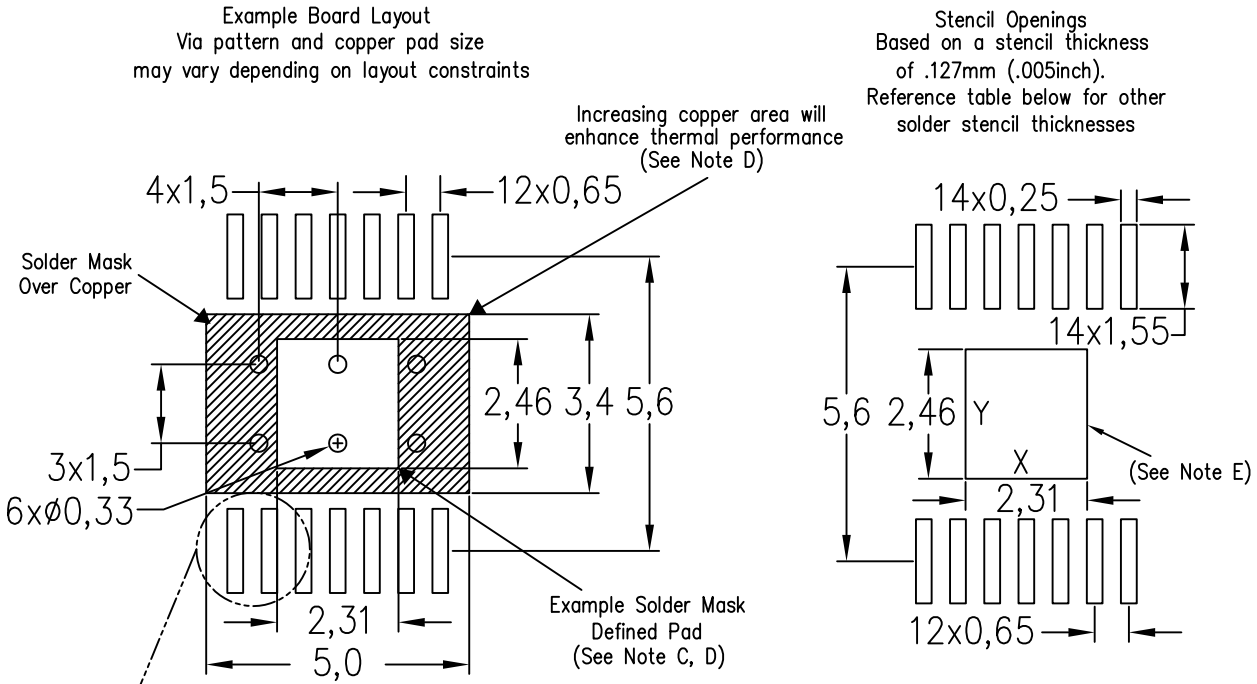
Exposed Thermal Pad Dimensions

4206332–2/AO 01/16

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE

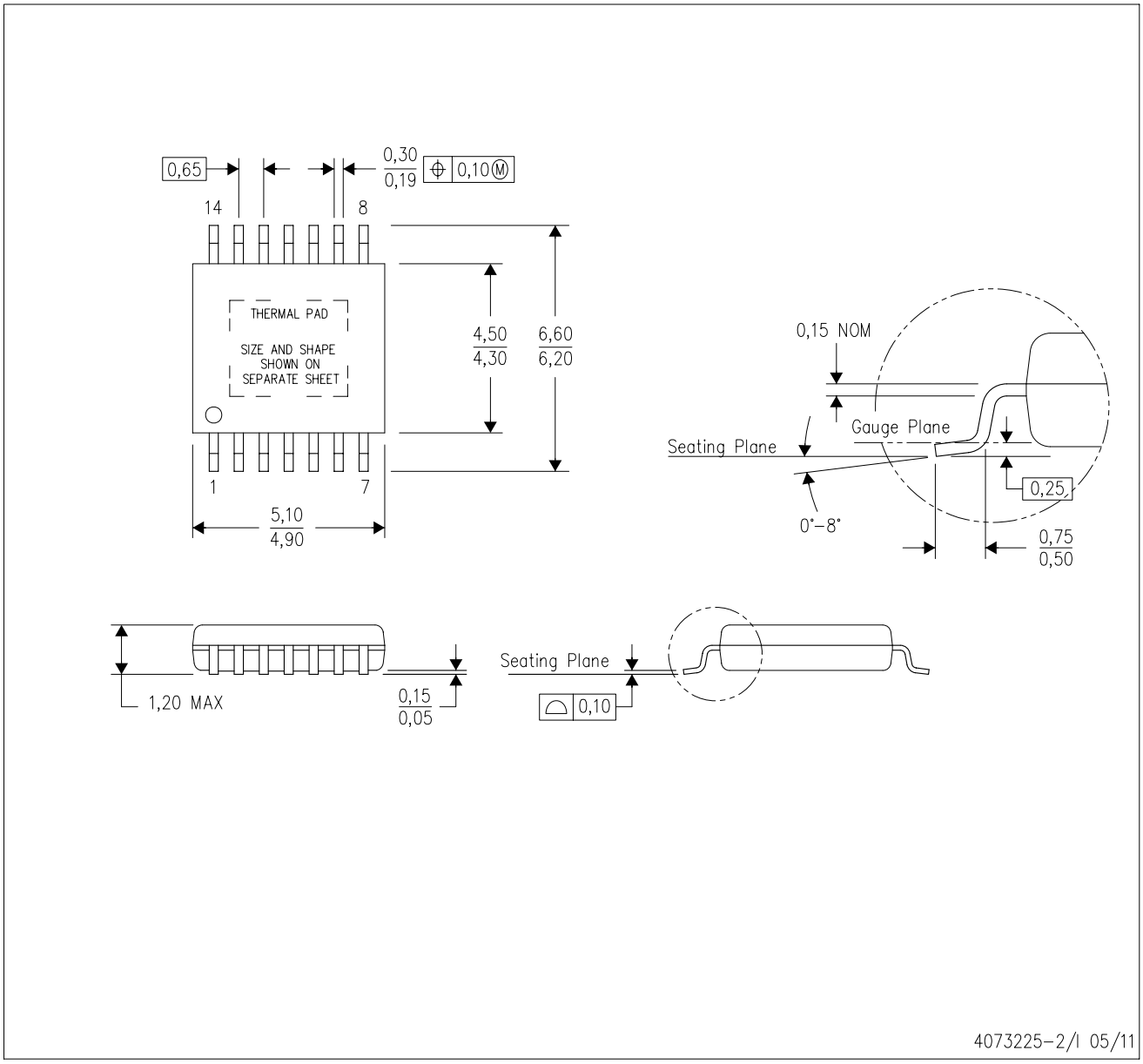


Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

4207609–2/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

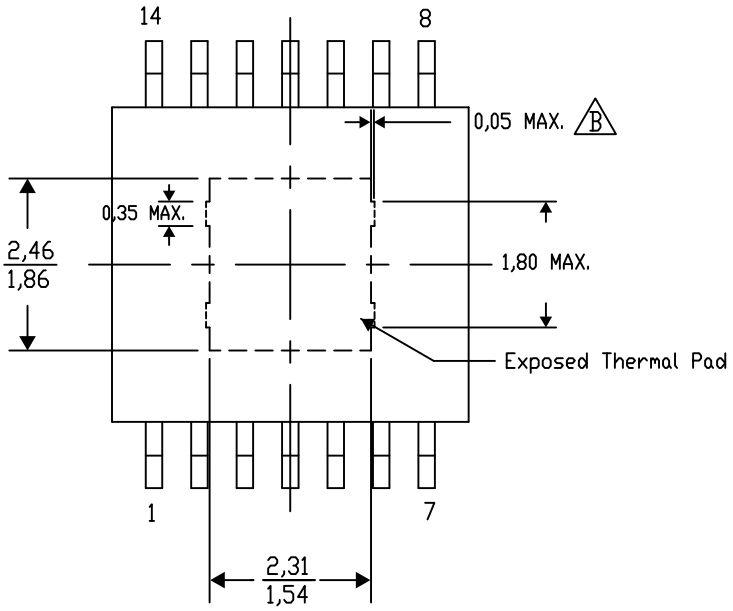
PWP (R–PDSO–G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332–44/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

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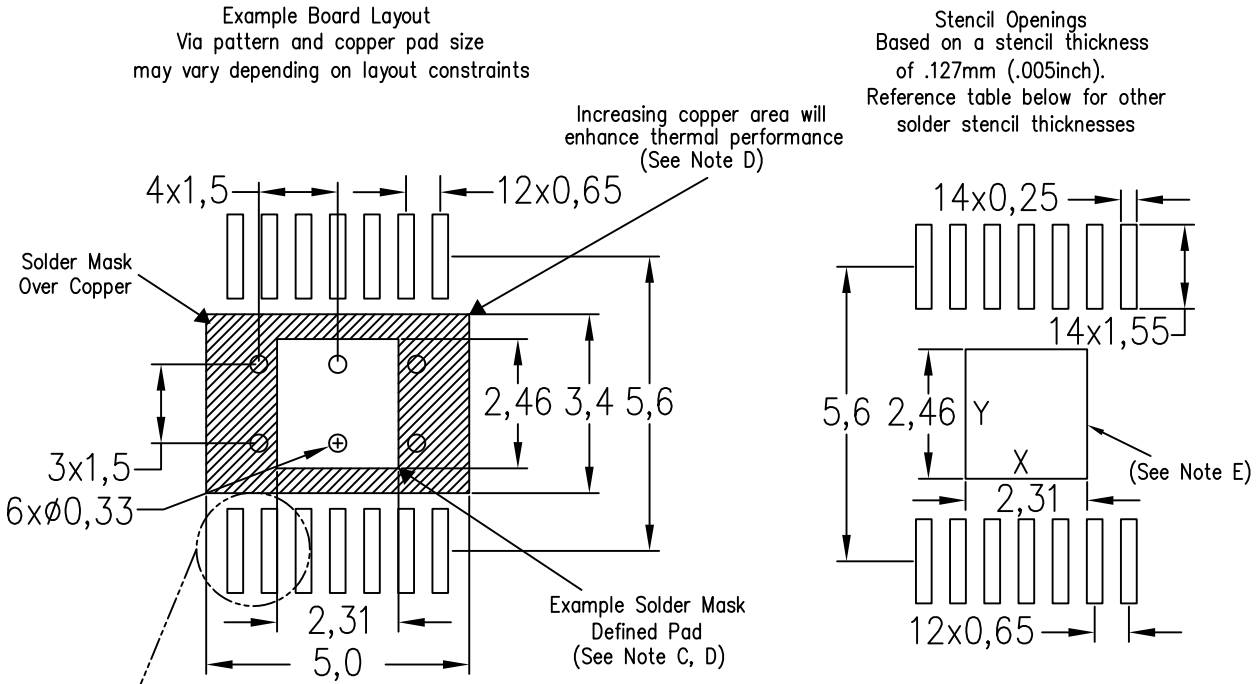
PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

4207609–2/W 09/15

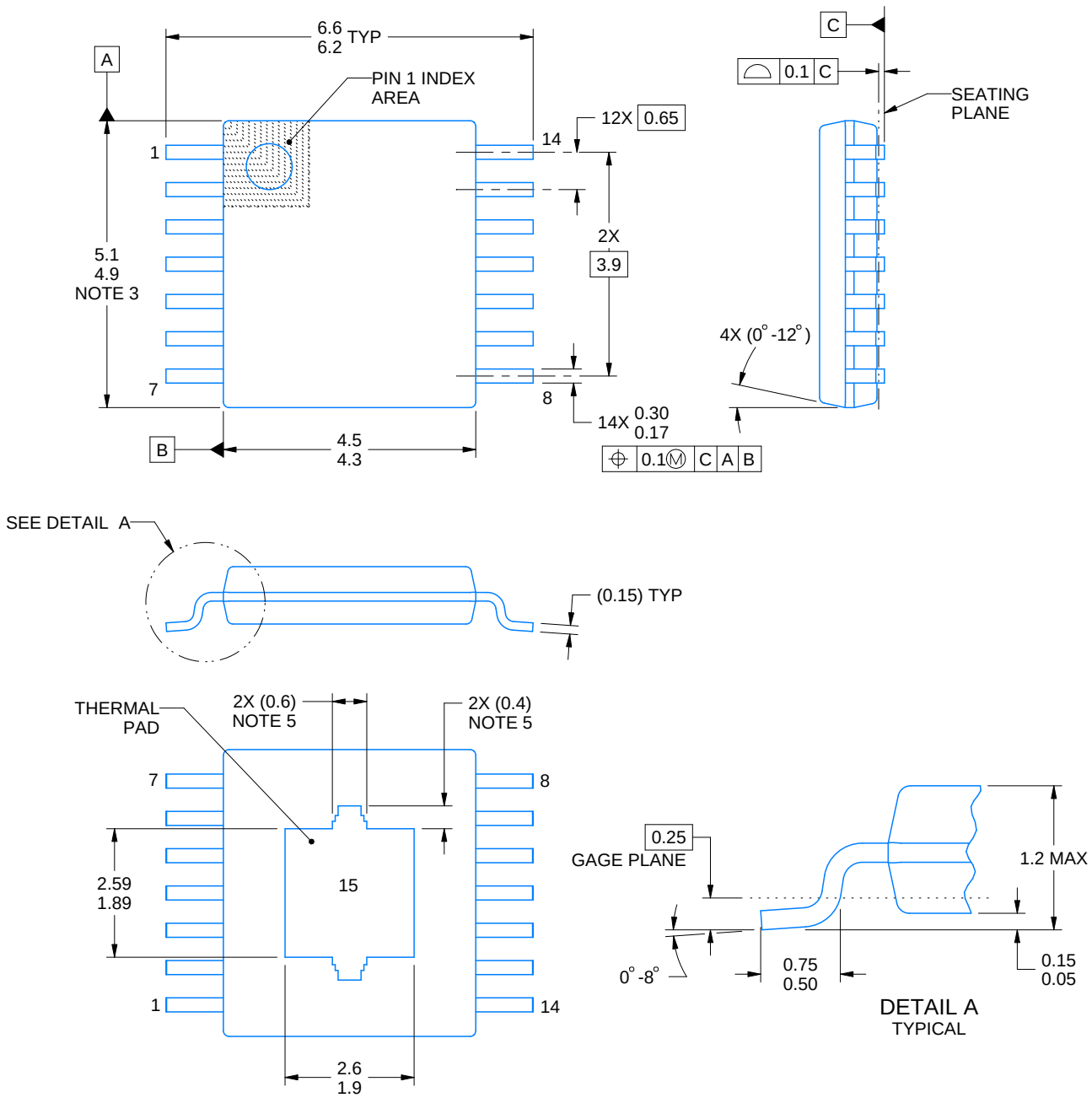
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PWP0014K

PowerPAD™ TSSOP - 1.2 mm max height

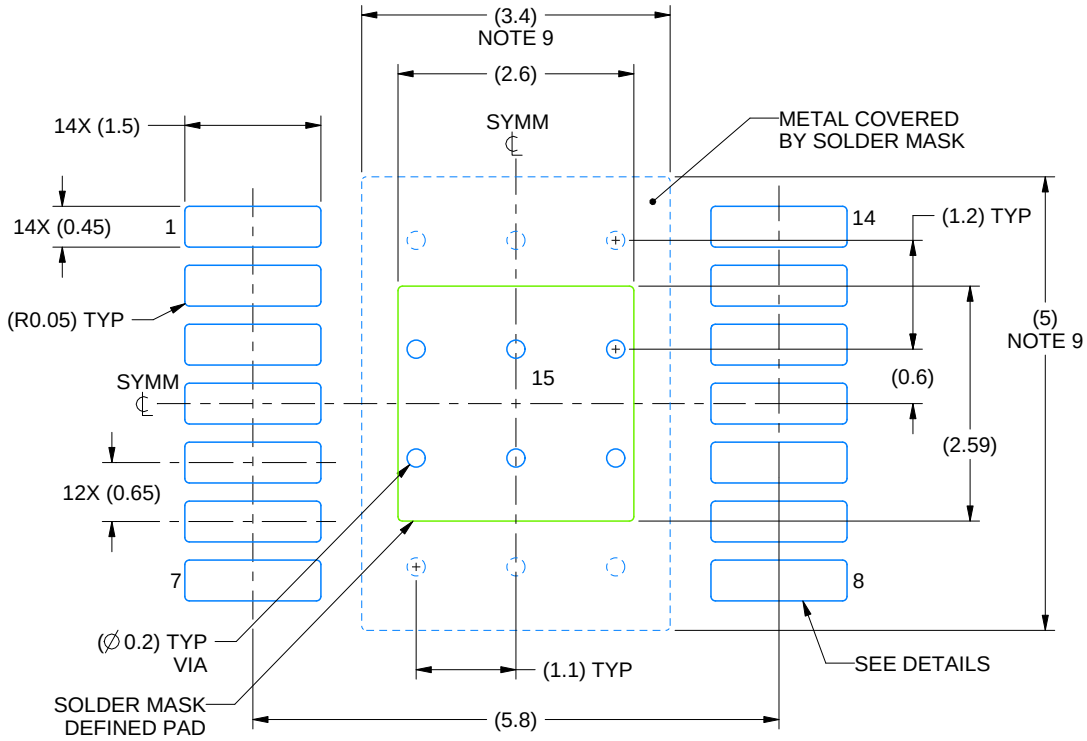
SMALL OUTLINE PACKAGE



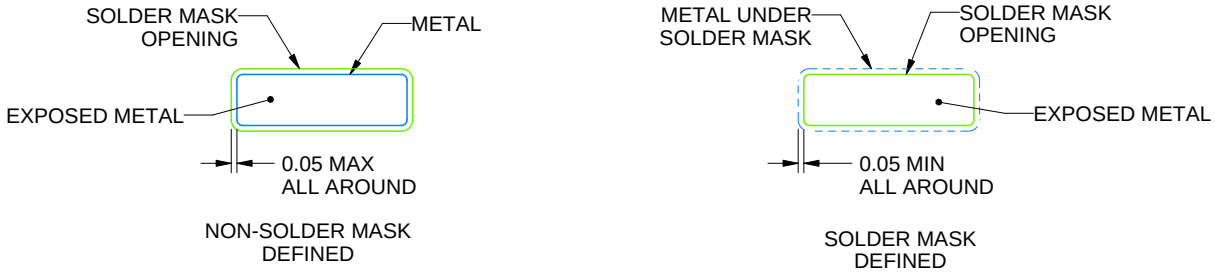
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X

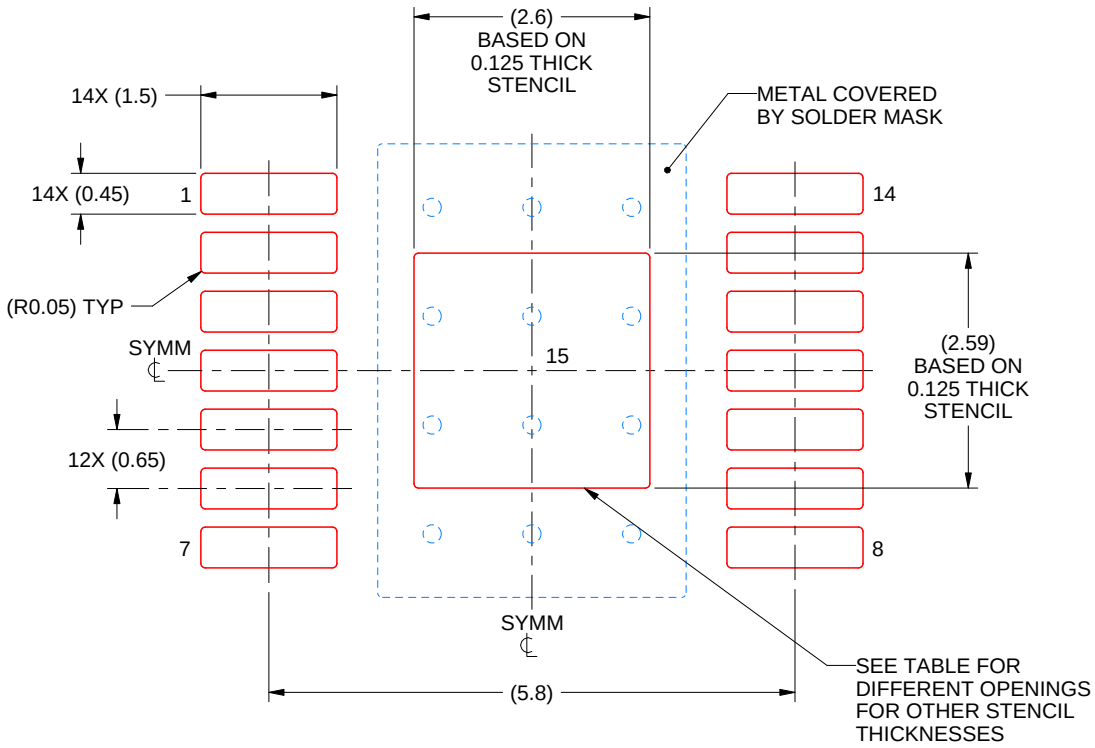


SOLDER MASK DETAILS

4229706/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 2.90
0.125	2.60 X 2.59 (SHOWN)
0.15	2.37 X 2.36
0.175	2.20 X 2.19

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月