TPS7N53 3A、低入力電圧、低ノイズ、高精度、低ドロップアウト (LDO) 電圧レギュレータ

1 特長

- 入力電圧範囲:
  - 1.1V～2.2V
- 出力電圧ノイズ:2.2μV_{RMS}
- ライン、負荷、温度の全範囲にわたって 1.5% (最大値) の精度
- 低いドロップアウト:95mV (標準値)、3A 時
- 電源電圧変動除去比 (3A):
  - 1kHz 時に 80dB
  - 10kHz 時に 63dB
  - 100kHz 時に 51dB
  - 1MHz 時に 25dB
- 可変出力電圧範囲:0.5V～1.5V
- 調整可能なソフトスタート突入電流制御
- オープン ドレインのパワー グッド (PG) 出力
- パッケージ:3mm × 3mm、16 ピン WQFN

2 アプリケーション

- マクロ リモート無線ユニット (RRU)
- 屋外バックホール ユニット
- アクティブ アンテナ システム (AAS) の mMIMO
- 超音波スキャナ
- 実験室およびフィールド向け計測機器
- センサ、画像処理、レーダー

3 概要

TPS7N53 は低ノイズ (2.2μV_{RMS})、超低ドロップアウトのリニア レギュレータ (LDO) で、3A を供給でき、ドロップアウトは出力電圧に関係なく最大でわずか 95mV (標準値) です。デバイスの出力電圧は、1 個の外付け抵抗を使って 0.5V～1.5V の範囲で調整可能です。低ノイズ、高 PSRR、大出力電流能力を組み合わせた TPS7N53 は、レーダーの電源、通信、画像処理の各アプリケーションで使用される、ノイズに敏感な部品 (RF アンプ、レーダー センサ、SERDES、アナログ チップセットなど) への電力供給に最適です。

ASIC (Application-Specific Integrated Circuit)、FPGA (Field-Programmable Gate Array)、DSP (Digital Signal Processor) など、低入力電圧、低出力電圧 (LILO) での動作を必要とするデジタル負荷には、非常に優れた精度 (負荷、ライン、および温度の全範囲で 1.5%)、リモート センシング、優れた過渡性能、ソフトスタート機能により、最適なシステム性能を提供します。汎用性、高性能、小型フットプリントを特長とするこの LDO は、A/D コンバータ (ADC)、D/A コンバータ (DAC)、イメージング センサなどの大電流アナログ負荷や、シリアライザ / デシリアライザ (SerDes)、FPGA、DSP などのデジタル負荷用の優れた選択肢です。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
TPS7N53	RTE (WQFN、16)	3.00mm × 3.00mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値で、該当する場合はピンも含まれます。

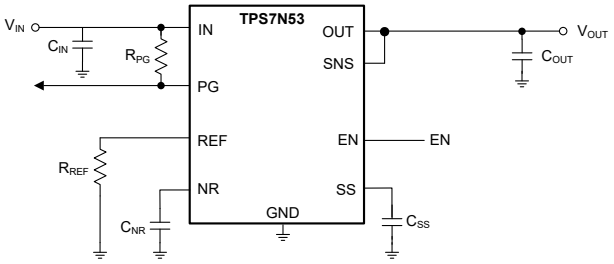


図 3-1. 代表的なアプリケーション回路

Table of Contents

1 特長.....1
2 アプリケーション.....1
3 概要.....1
4 Pin Configuration and Functions.....3
5 Specifications.....4
5.1 Absolute Maximum Ratings.....4
5.2 ESD Ratings.....4
5.3 Recommended Operating Conditions.....5
5.4 Thermal Information.....5
5.5 Electrical Characteristics.....6
5.6 Typical Characteristics.....8
6 Detailed Description.....12
6.1 Overview.....12
6.2 Functional Block Diagram.....13
6.3 Feature Description.....14
6.4 Device Functional Modes.....18
7 Application and Implementation.....19
7.1 Application Information.....19
7.2 Typical Application.....28
7.3 Power Supply Recommendations.....29
7.4 Layout.....29
8 Device and Documentation Support.....31
8.1 Documentation Support.....31
8.2 ドキュメントの更新通知を受け取る方法.....31
8.3 サポート・リソース.....31
8.4 Trademarks.....31
8.5 静電気放電に関する注意事項.....31
8.6 用語集.....31
9 Revision History.....31
10 Mechanical, Packaging, and Orderable Information.....31
10.1 Package Option Addendum.....35

4 Pin Configuration and Functions

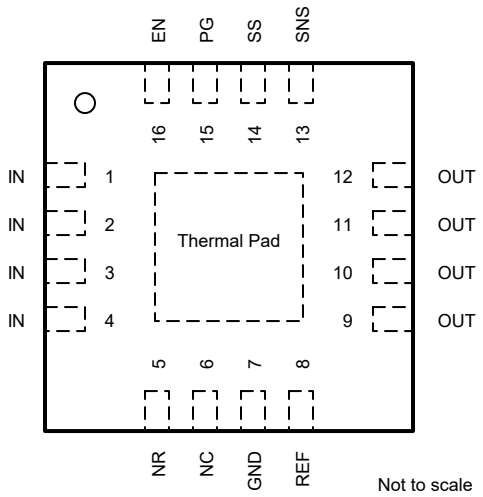


図 4-1. RTE Package, 16-Pin WQFN (Top View)

Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
EN	16	I	Enable pin. See the *Precision Enable and UVLO* section for additional information.
GND	7	GND	Ground pin. See the *Layout Guidelines* section for additional information.
IN	1, 2, 3, 4	I	Input supply voltage pin. See the *Input and Output Capacitor Requirements (C_{IN} and C_{OUT})* section for more details.
NC	6	—	Not connected. This pin can be left floating or tied to GND for improved thermal performance.
NR	5	I/O	Noise-reduction pin. See the *Input and Output Capacitor Requirements (C_{IN} and C_{OUT})* and *Soft-Start (SS Pin) and Noise Reduction (NR Pin)* sections for additional information.
SS	14	I/O	Soft-start pin. Connect a capacitor (C_{SS}) to adjust the start-up time. See the *セクション 7.1.4* section for additional information.
OUT	9, 10, 11, 12	O	Regulated output pin. See the *Output Voltage Setting and Regulation* and *Input and Output Capacitor Requirements (C_{IN} and C_{OUT})* sections for more details.
PG	15	O	Open-drain, power-good indicator pin for the low-dropout regulator (LDO) output voltage. See the *Power-Good Pin (PG Pin)* section for additional information.
REF	8	I/O	Reference pin. See the *Output Voltage Setting and Regulation* section for additional information.
SNS	13	I	Output sense pin. See the *Output Voltage Setting and Regulation* section for additional information.
Thermal Pad	—	GND	Connect the pad to GND for best possible thermal performance. See the *Layout* section for more information.

(1) I = input, O = output, I/O = input or output, GND = ground.

5 Specifications

5.1 Absolute Maximum Ratings

over operating junction temperature range and all voltages with respect to GND (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	IN, PG, EN	–0.3	6.5	V
	REF, SS, SNS	–0.3	6	
	OUT, NR	–0.3	V_{IN} + 0.3 (2)	
Current	OUT	Internally limited		A
	PG (sink current into the device)		5	mA
Temperature	Operating junction, T_J	–40	150	°C
	Storage, T_{stg}	–55	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The absolute maximum rating is V_{IN} + 0.3V or 6.0V, whichever is smaller.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{IN}	Input supply voltage range	1.1		2.2	V
V_{REF}	Reference voltage range	0.5		1.5	V
V_{OUT}	Output voltage range	0.5		1.5	V
I_{OUT}	Output current	0		3	A
C_{IN}	Input capacitor	10			µF
C_{OUT}	Output capacitor (1)	10		470	µF
C_{OUT_ESR}	Output capacitor ESR	1		20	mΩ
C_{OUT_ESL}	Output capacitor ESL	0.15		1.6	nH
C_{NR}	Noise-reduction capacitor		1	10	µF
C_{SS}	Soft-Start capacitor		10		nF
R_{PG}	Power-good pull-up resistance	10		100	kΩ
T_J	Junction temperature	–40		125	°C

(1) Effective output capacitance of 7 µF minimum required for stability

5.4 Thermal Information

THERMAL METRIC (1)		TPS7N53 RTE (WQFN) (2) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	42.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	17.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.5	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics* the application note.
(2) Evaluated using JEDEC standard (2s2p).

5.5 Electrical Characteristics

over operating temperature range (T_J = –40 °C to +125 °C), $V_{IN(NOM)}$ = $V_{OUT(NOM)}$ + 0.4V, I_{OUT} = 0A, V_{EN} = 1.8V, C_{IN} = 10 µF, C_{OUT} =10µF, C_{NR} = open, C_{SS} = 10nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{UVLO(IN)}$	Input supply UVLO	V_{IN} rising		1.07	1.1	V
$V_{HYS(UVLO\_IN)}$	Input supply UVLO hysteresis			60		mV
I_{SS}	SS fast start-up charging current	V_{SS} = GND, V_{IN} = 1.1 V	27	30	35	µA
t_{SS}	Soft-Start Time	C_{SS} = 10nF, V_{OUT} = 0.75V		0.7		ms
V_{OUT}	Output voltage accuracy (1)	0.5V ≤ V_{OUT} ≤ 1.5V, 0A ≤ I_{OUT} ≤ 3A, 1.1V ≤ V_{IN} ≤ 2.2V	–1.5	±0.5	1.5	%
I_{REF}	REF current pin	V_{IN} = 1.1 V, V_{OUT} = 0.5 V, I_{LOAD} = 0 A		150		µA
		1.1V ≤ V_{IN} ≤ 2.2V (1), 0.5V ≤ V_{OUT} ≤ 1.5V, 0A ≤ I_{OUT} ≤ 3A	–1.5	±1	1.5	%
V_{OS}	Output offset voltage (V_{NR} - V_{OUT})	1.1V ≤ V_{IN} ≤ 2.2V (1), 0.5 V ≤ V_{OUT} ≤ 1.5V, 0A ≤ I_{OUT} ≤ 3A	–2		2	mV
$\Delta V_{OUT(\Delta VIN)}$	Line regulation	1.1V ≤ V_{IN} ≤ 2.2V, V_{OUT} = 0.5V, I_{OUT} = 0A		-200		µV/V
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	V_{OUT} = 1.5V, 0A ≤ I_{OUT} ≤ 3A		-100		µV/A
V_{DO}	Dropout voltage (2)	V_{OUT} ≥ 1.2V, I_{OUT} = 3A		95	140	mV
		V_{OUT} ≥ 1.2V, I_{OUT} = 3A, –40°C ≤ T_J ≤ +85°C			125	
I_{LIM}	Output current limit	V_{OUT} forced at 0.9 × $V_{OUT(NOM)}$, $V_{OUT(NOM)}$ = 1.5V, V_{IN} = $V_{OUT(NOM)}$ + 400 mV	3.3	3.6	3.9	A
I_{SC}	Short circuit current limit	R_{LOAD} = 10 mΩ, under foldback operation		1.1		A
I_{GND}	GND pin current	I_{OUT} = 3 A, V_{OUT} = 1.5V		15		mA
		V_{IN} = 1.1 V, I_{OUT} = 3 A, V_{OUT} = 0.5 V	13	15	19	
I_{SDN}	Shutdown GND pin current	PG = (open), V_{IN} = 2.2 V, V_{EN} = 0.4 V		100	300	µA
I_{EN}	EN pin current	V_{IN} = 2.2V, 0 V ≤ V_{EN} ≤ 6 V	-5		5	µA
$V_{IH(EN)}$	EN trip point rising (turn-on)	V_{IN} = 1.1 V	0.62	0.65	0.68	V
$V_{IL(EN)}$	EN trip point falling (turn-off)	V_{IN} = 1.1 V	0.58	0.61	0.64	V
$V_{HYS(EN)}$	EN trip point hysteresis	V_{IN} = 1.1 V		40		mV
$V_{IT(PG)}$	PG pin threshold	For PG transitioning low with falling V_{OUT}, V_{IN} = 1.1 V, V_{OUT} < $V_{IT(PG)}$, I_{PG} = –1 mA (current into device)	87	90	93	%
$V_{HYS(PG)}$	PG pin hysteresis	V_{IN} = 1.1 V, V_{OUT} < $V_{IT(PG)}$, I_{PG} = –1 mA (current into device)		2		%
$V_{OL(PG)}$	PG pin low-level output voltage	V_{IN} = 1.1 V, V_{OUT} < $V_{IT(PG)}$, I_{PG} = –1 mA (current into device)			0.4	V
$I_{LKG(PG)}$	PG pin leakage current	V_{PG} = 6 V, V_{OUT} > $V_{IT(PG)}$, V_{IN} = 1.1 V			1	µA
PSRR	Power-supply ripple rejection	f = 1 MHz, V_{IN} = 1.8V, $V_{OUT(NOM)}$ = 1.5 V, I_{OUT} = 3 A, C_{NR} = 1 µF		23		dB
		f = 1 MHz, V_{IN} =1.1 V, $V_{OUT(NOM)}$ = 0.5 V, I_{OUT} = 3 A, C_{NR} = 1 µF		25		
V_n	Output noise voltage	BW = 10Hz to 100kHz, 1.1V ≤ V_{IN} ≤ 2.2 V, 0.5V ≤ V_{OUT} ≤ 1.5V, I_{OUT} = 3A, C_{NR} = 1 µF		8		μV_{RMS}
V_n	Output noise voltage	BW = 100Hz to 100kHz, 1.1V ≤ V_{IN} ≤ 2.2V, 0.5V ≤ V_{OUT} ≤1.5V, I_{OUT} = 3A, C_{NR} = 1µF		2.2		μV_{RMS}
R_{DIS}	Output pin active discharge resistance	V_{IN} = 1.1V, V_{EN} = 0V V_{OUT} = 0.2V		110		Ω
R_{NR_DIS}	NR pin active discharge resistance	V_{IN} = 1.1 V, V_{EN} = 0 V, V_{NR} = 0.2V		250		Ω
R_{SS_DIS}	SS pin active discharge resistance	V_{IN} = 1.1V, V_{EN} = 0V, V_{SS} = 0.2V		5.6		kΩ
$T_{SD(shutdown)}$	Thermal shutdown temperature	Shutdown, temperature increasing		165		°C

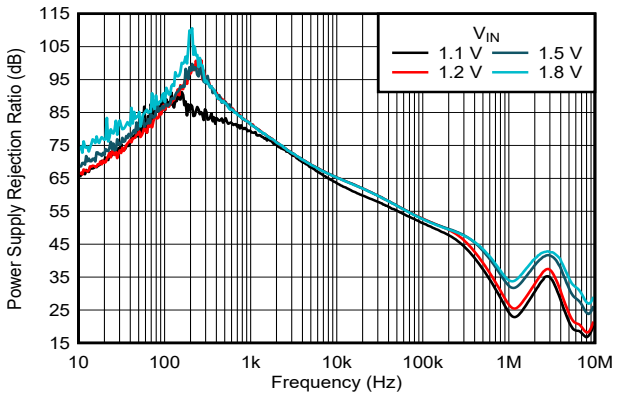
over operating temperature range (T_J = –40 °C to +125 °C), $V_{IN(NOM)}$ = $V_{OUT(NOM)}$ + 0.4V, I_{OUT} = 0A, V_{EN} = 1.8V, C_{IN} = 10 µF, C_{OUT} =10µF, C_{NR} = open, C_{SS} = 10nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{SD(reset)}$	Thermal shutdown reset temperature	Reset, temperature decreasing		150		°C

(1) Limited by max power dissipation of 2 W.
(2) V_{REF} = V_{IN}, V_{SNS} = 95% × V_{REF}.

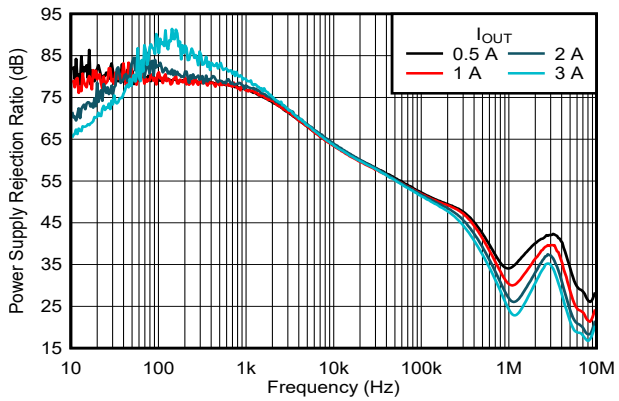
5.6 Typical Characteristics

V_{IN} = 1.1V,V_{EN} = 1.8V, C_{IN} = 10 µF, C_{NR} = 1µF, C_{OUT} = 10 µF, C_{SS} = 10 nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at T_J = 25°C



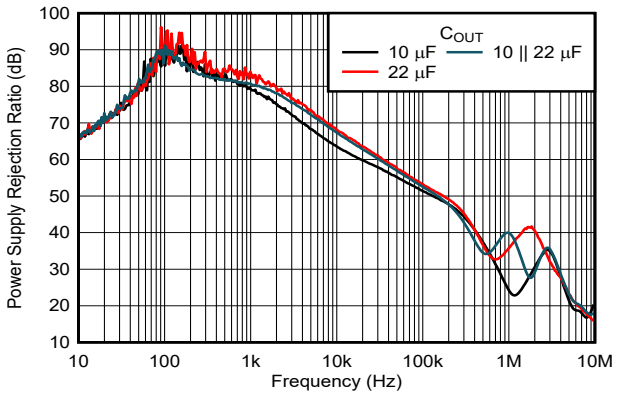
V_{OUT}= 0.5V, C_{NR} = 1µF, C_{IN} = 4µF, I_{OUT} = 3A

図 5-1. PSRR vs Frequency and V_{IN}



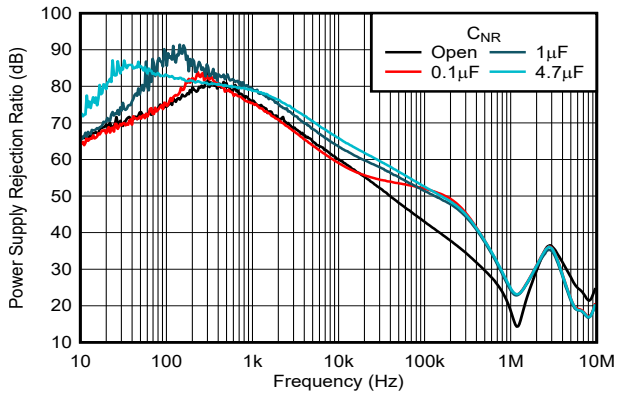
V_{OUT} = 0.5V, V_{IN}=1.1V, C_{NR} =1µF, C_{IN} = 4µF

図 5-2. PSRR vs Frequency and I_{OUT}



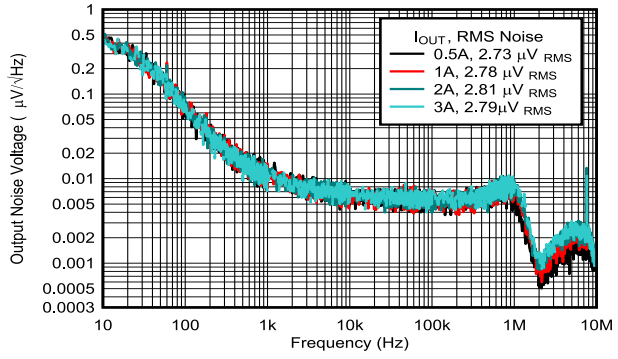
V_{OUT} = 0.5V, V_{IN}=1.1V, C_{NR} =1µF, C_{IN} = 4µF, I_{OUT} = 3A

図 5-3. PSRR vs Frequency and C_{OUT}



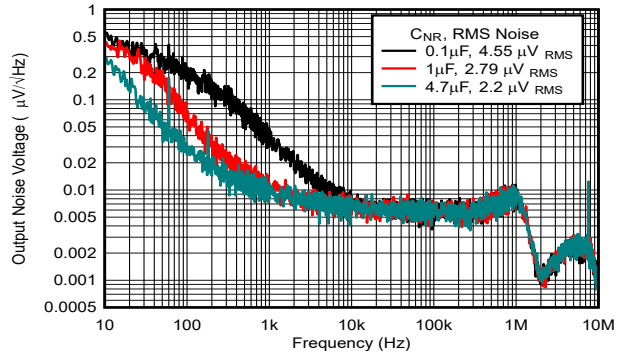
V_{OUT} = 0.5V, V_{IN}=1.1V, C_{IN} = 4µF, I_{OUT} = 3A

図 5-4. PSRR vs Frequency and C_{NR}



V_{OUT} = 0.5V, V_{IN}=1.1V, C_{NR} =1µF

図 5-5. Output Voltage Noise Density vs Frequency and I_{OUT}

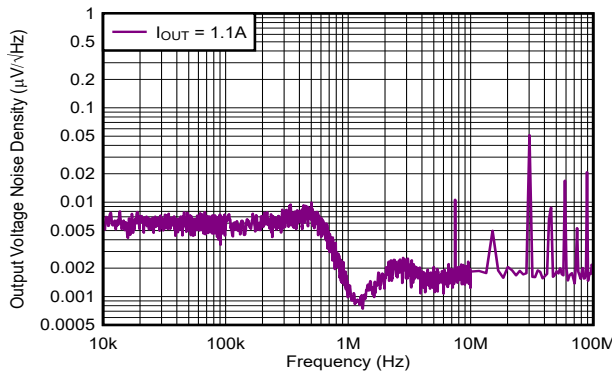


V_{OUT} = 0.5V, V_{IN}=1.1V, I_{OUT} =3A

図 5-6. Output Voltage Noise Density vs Frequency and C_{NR}

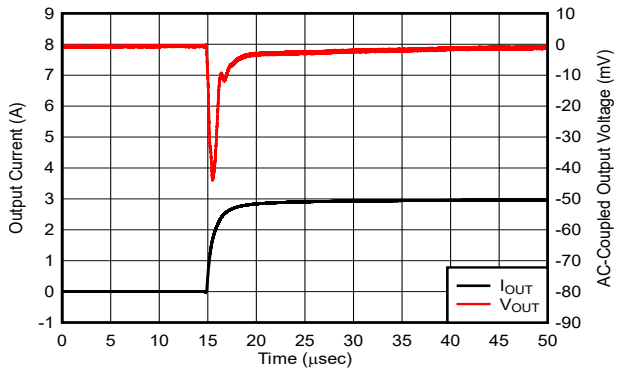
5.6 Typical Characteristics (continued)

V_{IN} = 1.1V,V_{EN} = 1.8V, C_{IN} = 10 µF, C_{NR} = 1µF, C_{OUT} = 10 µF, C_{SS} = 10 nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at T_J = 25°C



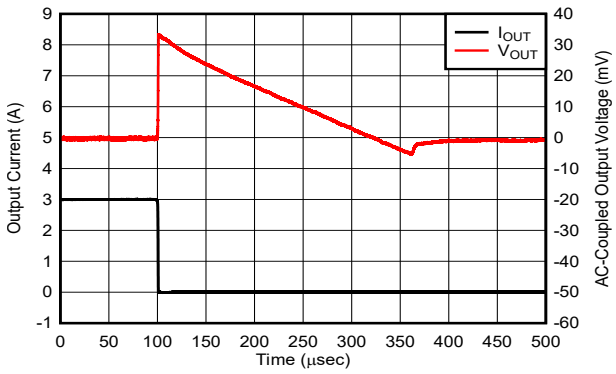
V_{OUT} = 0.75V, V_{IN}=1.5V, C_{IN} = 22µF, C_{OUT} =22µF||2.2µF|| 22nF

図 5-7. Charge Pump Output Voltage Noise Density vs Frequency and I_{OUT}



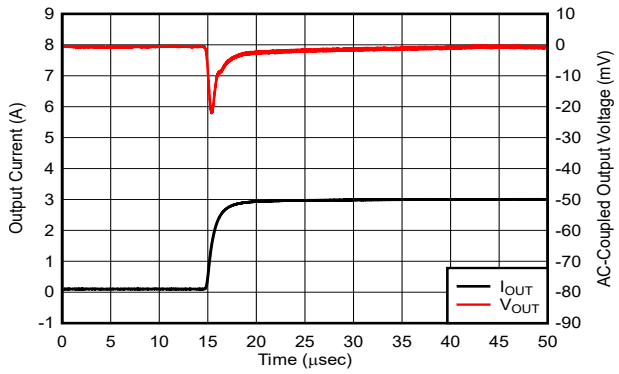
V_{OUT} = 0.5V, C_{NR} = 1µF, V_{IN}=1.1V, Slew Rate = 1A/µs

図 5-8. Load Transient for I_{OUT} = 0A to 3A



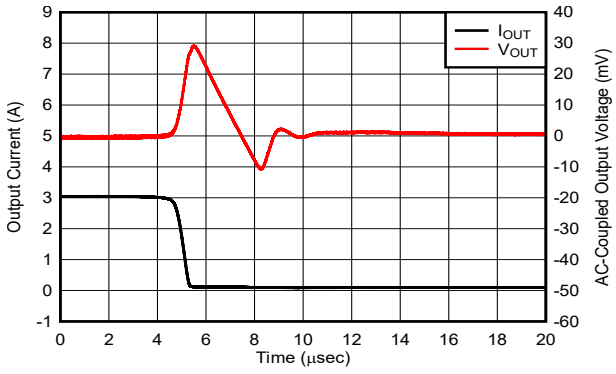
V_{OUT} = 0.5V, C_{NR} = 1µF, V_{IN}=1.1V, Slew Rate = 1A/µs

図 5-9. Load Transient for I_{OUT} = 3A to 0A



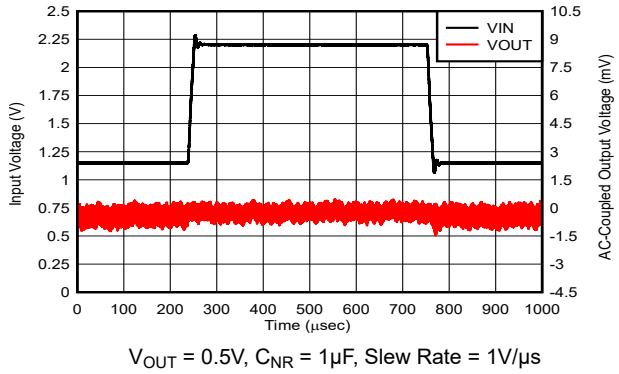
V_{OUT} = 0.5V, C_{NR} = 1µF, V_{IN}=1.1V, Slew Rate = 1A/µs

図 5-10. Load Transient for I_{OUT} = 100 mA to 3A



V_{OUT} = 0.5V, C_{NR} = 1µF, V_{IN}=1.1V, Slew Rate = 1A/µs

図 5-11. Load Transient for I_{OUT} = 3A to 100mA

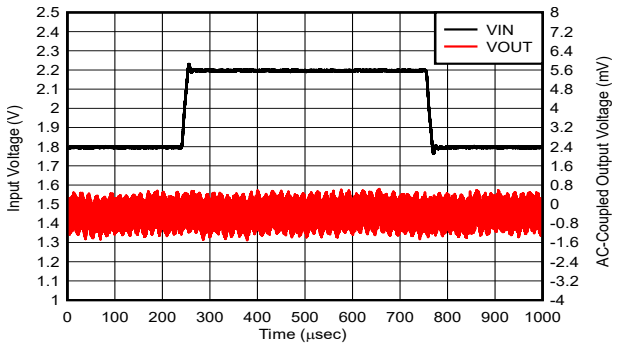


V_{OUT} = 0.5V, C_{NR} = 1µF, Slew Rate = 1V/µs

図 5-12. IN Line Transient for V_{IN} = 1.1V to 2.2V

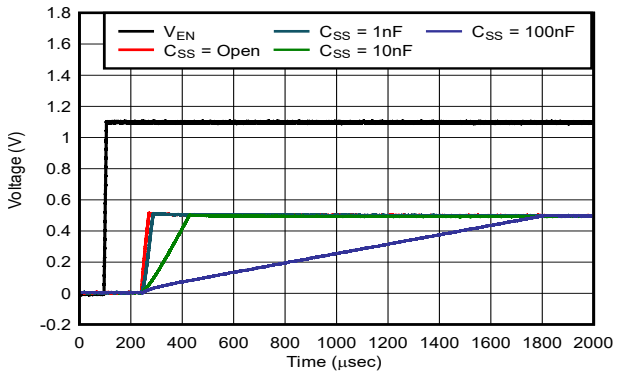
5.6 Typical Characteristics (continued)

V_{IN} = 1.1V,V_{EN} = 1.8V, C_{IN} = 10 µF, C_{NR} = 1µF, C_{OUT} = 10 µF, C_{SS} = 10 nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at T_J = 25°C



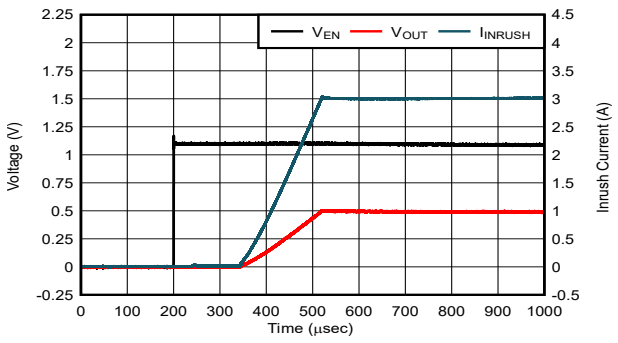
V_{OUT} = 1.5V, C_{NR} = 1µF, Slew Rate = 1V/µs

図 5-13. IN Line Transient for V_{IN} = 1.8 V to 2.2V



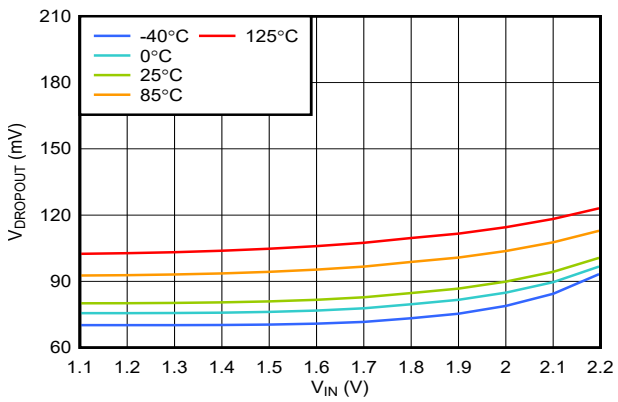
V_{OUT} = 0.5V, C_{NR} = 1µF, I_{OUT} = 3A

図 5-14. Start-Up for C_{SS}



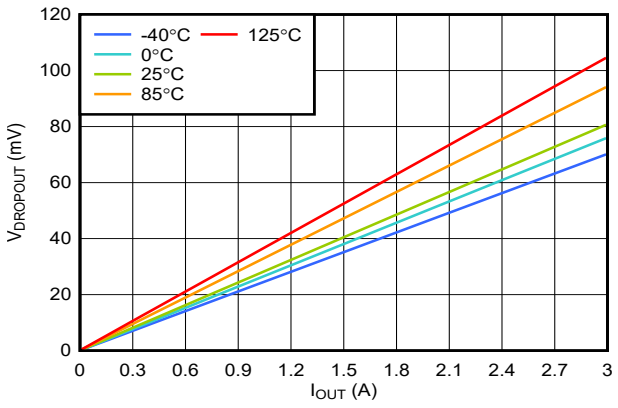
C_{NR} = 1µF, I_{OUT} = 3A

図 5-15. Inrush Current for V_{OUT} = 0.5V



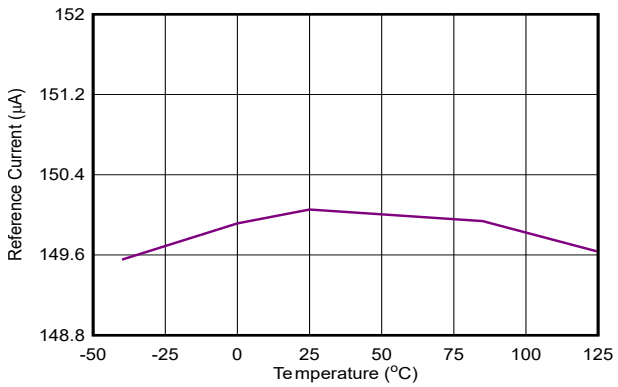
V_{OUT} = 0.5V, I_{OUT} = 3A, V_{EN} = 0.7V

図 5-16. Dropout Voltage vs V_{IN}



V_{IN} = 1.1V, V_{EN} = 0.7V

図 5-17. Dropout Voltage vs I_{OUT}

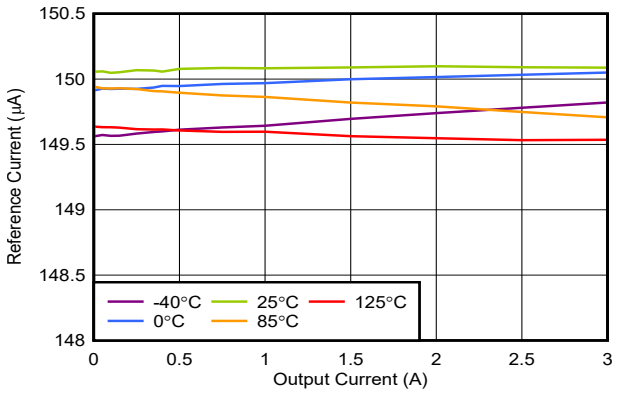


V_{OUT} = 0.5V, V_{IN} = 1.1V, V_{EN} = 0.7V, I_{OUT} = 0A

図 5-18. Reference Current vs Temperature

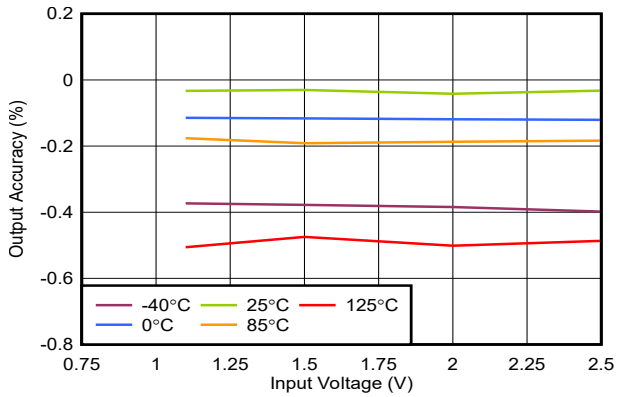
5.6 Typical Characteristics (continued)

V_{IN} = 1.1V,V_{EN} = 1.8V, C_{IN} = 10 µF, C_{NR} = 1µF, C_{OUT} = 10 µF, C_{SS} = 10 nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at T_J = 25°C



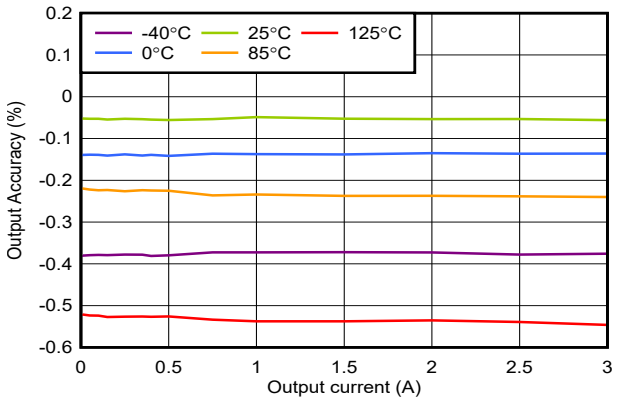
V_{OUT} = 0.5V, V_{IN} = 1.1V, V_{EN} = 0.7V

図 5-19. Reference Current Accuracy vs I_{OUT}



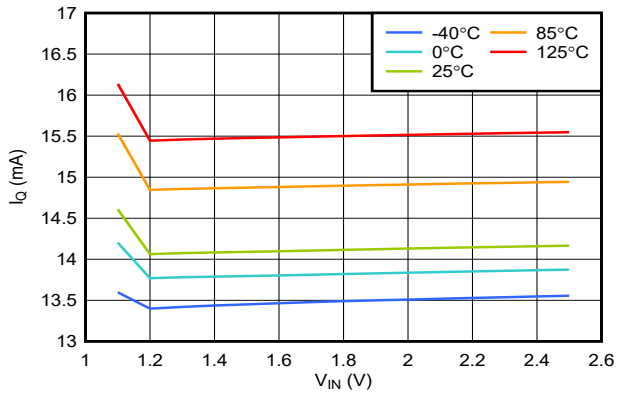
V_{OUT} = 0.5V, I_{OUT} = 3A, V_{EN} = 0.7V

図 5-20. Output Voltage Accuracy vs V_{IN}



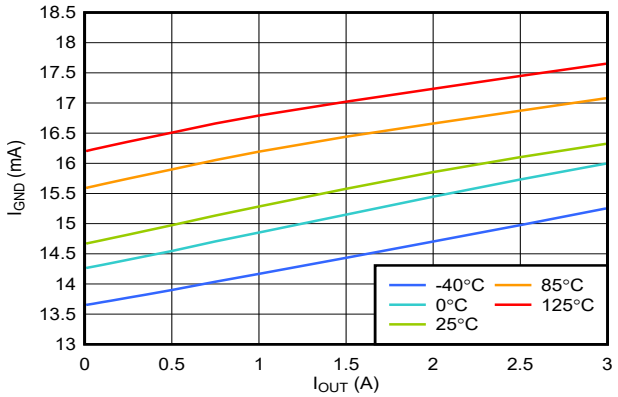
V_{OUT} = 0.5V, V_{IN} = 1.1V, V_{EN} = 0.7V

図 5-21. Output Voltage Accuracy vs I_{OUT}



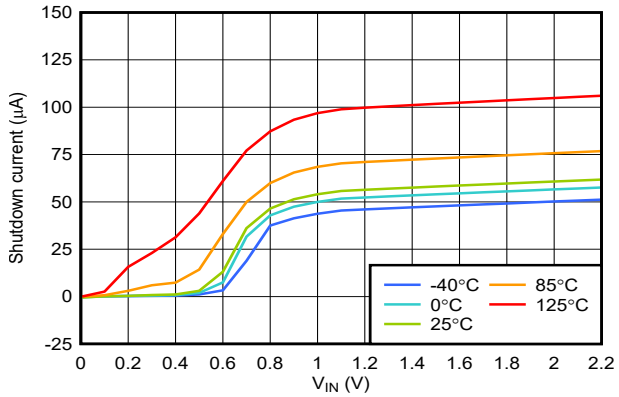
V_{OUT} = 0.5V, V_{IN} = 1.1V, V_{EN} = 0.7V

図 5-22. Quiescent Current vs V_{IN}



V_{OUT} = 0.5V, C_{NR} = 1µF, V_{EN} = 0.7V

図 5-23. Quiescent Current vs I_{OUT}



V_{OUT} = 0.5V, C_{NR} = 1µF, V_{EN} = 0.4V

図 5-24. Shutdown Current vs V_{IN} for V_{OUT} = 0.5V

6 Detailed Description

6.1 Overview

The TPS7N53 is a low-noise (2.2μV_{RMS} over 100Hz to 100kHz bandwidth), ultra-high PSRR (> 33dB to 1MHz), high-accuracy (1.5%), ultra-low-dropout (LDO) linear voltage regulator with an input range of 1.1V to 2V and an output voltage range from 0.5V to 1.5V. This device uses innovative circuitry to achieve wide bandwidth and high loop gain, resulting in ultra-high PSRR even with very low operational headroom [V_{OpHr} = (V_{IN} – V_{OUT})]. The TPS7N53 has an integrated charge-pump for ease of use to allow low dropout. At a high level, the device has two main primary features (the current reference and the unity-gain LDO buffer) and a few secondary features (such as the adjustable soft-start inrush control, precision enable, and PG pin).

The current reference is controlled by the REF pin. This pin sets the output voltage with a single resistor.

The SS pin sets the start-up time, and the NR filters the noise generated by the reference and external set resistor.

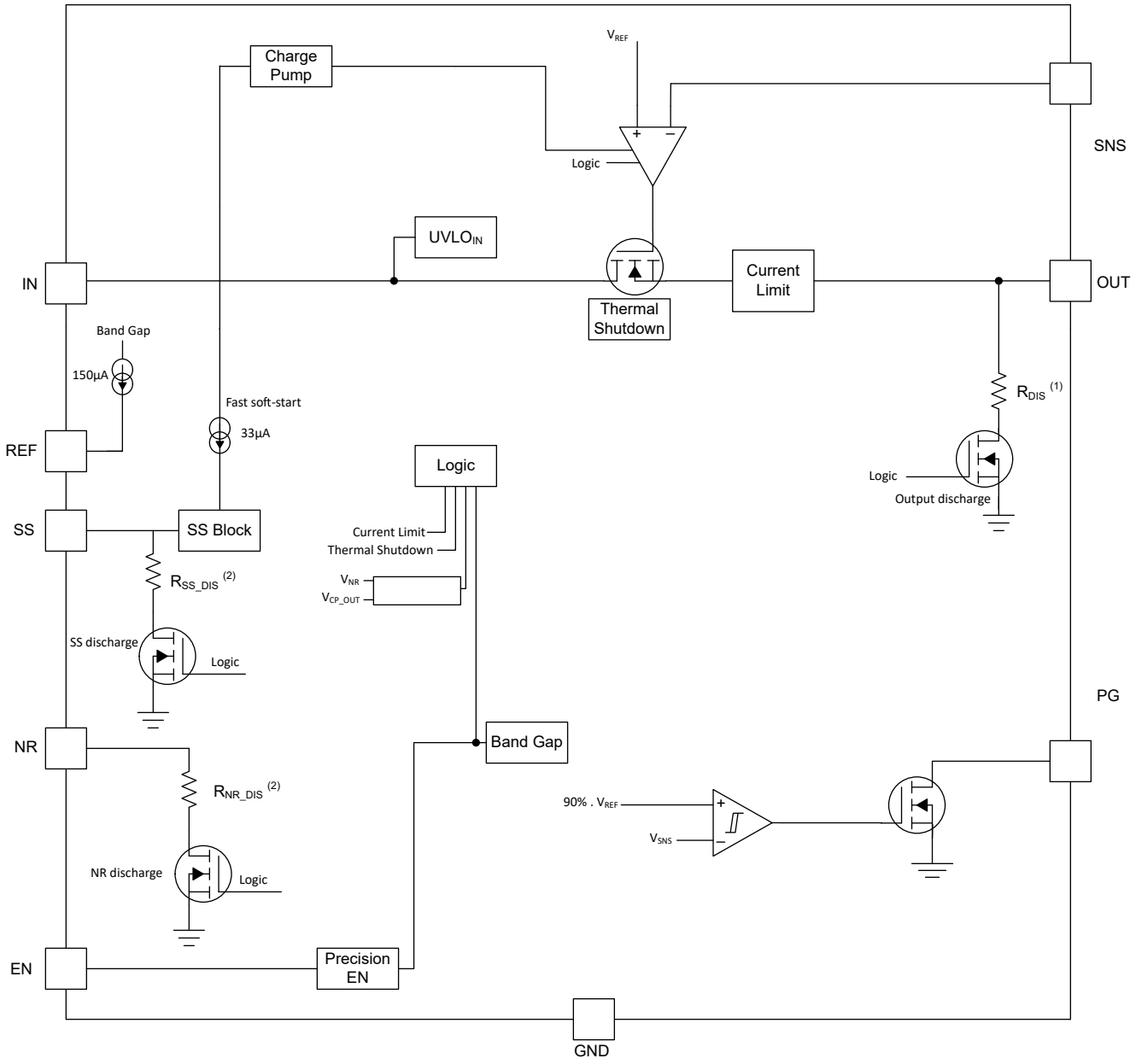
The unity-gain LDO buffer controls the output voltage. The low noise does not increase with output voltage and provides wideband PSRR. As such, the SNS pin is only used for remote sensing of the load.

The low-noise current reference, 150μA typical, is used in conjunction with an external resistor (R_{REF}) to set the output voltage. This process allows the output voltage range to be set from 0.5V to 1.5V. To achieve low noise and allow for a soft-start inrush, external capacitors, C_{NR} and C_{SS}(typically 1μF and 10nF), are placed on the NR and SS pins. When start-up is completed and the switch between REF and NR is closed, the C_{NR} capacitor is in parallel with the R_{REF} resistor attenuating the band-gap noise. The R_{REF} resistor sets the output voltage. This unity-gain LDO provides ultra-high PSRR over a wide frequency range without compromising load and line transients.

The EN pin sets the precision enable feature; a resistor divider on this pin selects the optimal input voltage at which the device starts. There are two independent undervoltage lockout (UVLO) voltages in this device: the internal fixed UVLO thresholds for the IN, and the externally adjustable UVLO threshold using the EN pin.

This regulator offers current limit, thermal protection, is fully specified from –40°C to +125°C, and is offered in a 16-pin WQFN, 3-mm × 3-mm thermally efficient package.

6.2 Functional Block Diagram



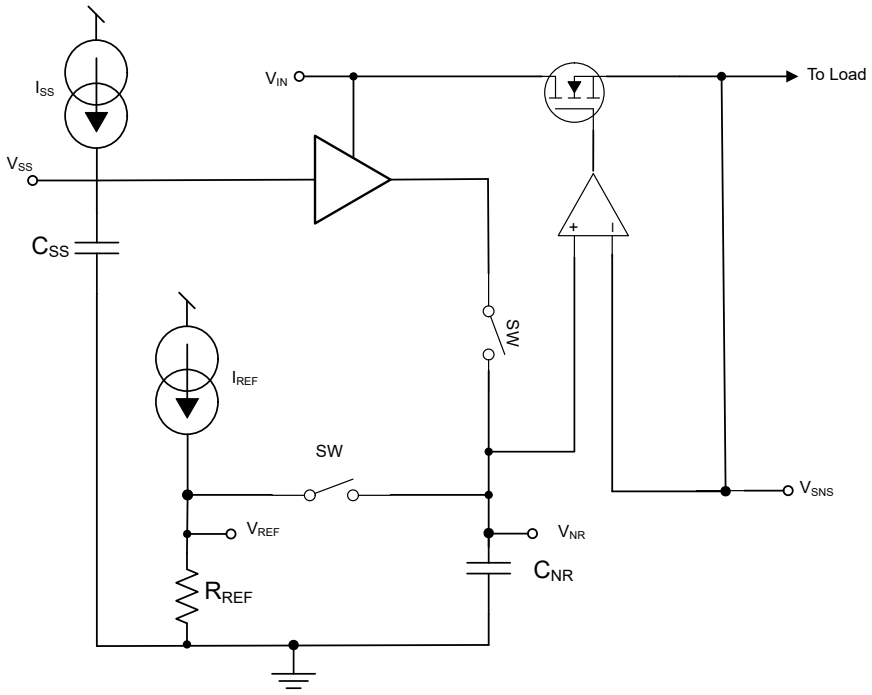
A. See the R_{DIS} (the output pin active discharge resistance) value in the *セクション 5.5* table.
B. See the R_{NR_DIS} (the NR pin active discharge resistance) value in the *セクション 5.5* table.
C. See the R_{SS_DIS} (the SS pin active discharge resistance) value in the *セクション 5.5* table.

6.3 Feature Description

6.3.1 Output Voltage Setting and Regulation

The simplified regulation circuit is shown in 図 6-1, in which the input signal (V_{REF}) is generated by the internal current source (I_{REF}) and the external resistor (R_{REF}). The LDO output voltage is programmed by the V_{REF} voltage because the error amplifier is always operating in unity-gain configuration. The V_{REF} reference voltage is generated by an internal low-noise current source driving the R_{REF} resistor and is designed to have very low bandwidth at the input to the error amplifier through the use of a low-pass filter (C_{NR} || R_{REF}).

The unity-gain configuration is achieved by connecting SNS to OUT. Minimize trace inductance on the output and connect C_{OUT} as close to the output as possible.



$V_{OUT} = I_{REF} \times R_{REF}$.

図 6-1. Simplified Regulation Circuit

This unity-gain configuration, along with the highly accurate I_{REF} reference current, enables the device to achieve excellent output voltage accuracy. The low dropout voltage (V_{DO}) enables reduced thermal dissipation and achieves robust performance. This combination of features make this device an excellent voltage source for powering sensitive analog low-voltage (≤ 1.5V) devices.

6.3.2 Low-Noise, Ultra-High Power-Supply Rejection Ratio (PSRR)

The device architecture features a highly accurate, high-precision, low-noise current reference followed by a state-of-the-art, complementary metal oxide semiconductor (CMOS) error amplifier (6 nV/$\sqrt{\text{Hz}}$ at 10-kHz noise for V_{OUT} ≥ 0.5 V). Unlike previous-generation LDOs, the unity-gain configuration of this device provides low noise over the entire output voltage range. Additional noise reduction and higher output current can be achieved by placing multiple TPS7N53 LDOs in parallel.

6.3.3 Programmable Soft-Start (SS Pin)

The device features a programmable, monotonic, current-controlled, soft-start circuit that uses the C_{SS} capacitor to minimize inrush current into the output capacitor and load during start-up. This circuitry can also reduce the start-up time for some applications that require the output voltage to reach at least 90% of the set value for fast system start up. The soft-start feature can be used to eliminate power-up initialization problems. The controlled output voltage ramp also reduces peak inrush current during start up, minimizing start-up transients to the input power bus.

Use 式 1 to estimate the ramp-up time for V_{OUT}

$$t_{SS}=\left(\frac{V_{REF}\times C_{SS}}{I_{SS}}\right) \quad (1)$$

Where I_{SS} = 30µA, V_{REF} = I_{REF} x R_{REF}, in which I_{REF} = 150µA and R_{REF} is the resistor installed at the REF pin to set the output voltage.

See the *Soft-Start (SS Pin) and Noise Reduction (NR Pin)* section for more details.

6.3.4 Precision Enable and UVLO

Depending on the circuit implementation, up to two independent undervoltage lockout (UVLO) voltage circuits can be active. An internally set UVLO on the input supply (IN pin) automatically disables the LDO when the input voltage reaches the minimum threshold. A precision EN function (EN pin) can also be used as a user-programmable UVLO.

1. The internal input supply voltage UVLO circuit prevents the regulator from turning on when the input voltage is not high enough, see the *Electrical Characteristics* table for more details.
2. The precision enable circuit allows a simple sequencing of multiple power supplies with a resistor divider from another supply. This enable circuit can be used to set an external UVLO voltage at which the device is enabled using a resistor divider on the EN pin; see the *Precision Enable (External UVLO)* section for more details.

6.3.5 Power-Good Pin (PG Pin)

The PG pin is an output indicating if the LDO is ready to provide power. This pin is implemented using an open-drain architecture. During the start-up phase, the PG voltage threshold is set by the REF voltage when the fast soft-start is ongoing and is set by the NR voltage when the fast soft-start is completed and the switch between REF and NR is closed.

As shown in the *Functional Block Diagram*, the PG pin is implemented by comparing the SNS pin voltage to an internal reference voltage and, as such, is considered a voltage indicator reflecting the output voltage status.

For PG pin implementation, see the *Power-Good Functionality* section.

6.3.6 Active Discharge

To quickly discharge internal nodes, the device incorporates three internal pulldown metal-oxide semiconductor field effect transistors (MOSFETs). The first pulldown MOSFET connects a resistor (R_{DIS}) from OUT to ground when the device is disabled to actively discharge the output capacitor. The second pulldown MOSFET connects a resistor from NR (R_{NR_DIS}) to ground when the device is disabled and discharges the NR capacitor. The third pulldown MOSFET connects a resistor from SS (R_{SS_DIS}) to ground when the device is disabled and discharges the SS capacitor. All pulldown MOSFETs are activated by any of the following events:

- Driving the EN pin below the $V_{EN(LOW)}$ threshold
- The IN pin voltage falling below the undervoltage lockout $V_{UVLO(IN)}$ threshold

注

A brownout event on V_{IN}during a low-input, low-output (LILO) operation (V_{IN} = $V_{IN(min)}$) can result in incomplete C_{NR} discharge. Consider the time constant on both the NR and OUT pins for a proper system shutdown procedure.

6.3.7 Thermal Shutdown Protection (T_{SD})

A thermal shutdown protection circuit disables the LDO when the pass transistor junction temperature (T_J) rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis verifies that the device resets (turns on) when the temperature falls to $T_{SD(shutdown)}$ (typical). The thermal time constant of the semiconductor die is fairly short, thus the device can cycle off and on when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start up can be high from large V_{IN} – V_{OUT} voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start up completes. For reliable operation, limit the junction temperature to the maximum listed in the *Electrical Characteristics* table. Operation above this maximum temperature causes the device to exceed the operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overload conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

6.4 Device Functional Modes

表 6-1 provides a quick comparison between the normal, dropout, and disabled modes of operation.

表 6-1. Device Functional Modes Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	EN	I_{OUT}	T_J
Normal(1)	$V_{IN} > V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{IH(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{sd}$
Dropout(1)	$V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{IH(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{sd}$
Disabled(2)	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{IL(EN)}$	—	$T_J > T_{sd}$

(1) All table conditions must be met.
(2) The device is disabled when any condition is met.

6.4.1 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{LIM}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD(shutdown)}$)
- The voltage on the EN pin has previously exceeded the $V_{IH(EN)}$ threshold voltage and has not yet decreased to less than the enable falling threshold

6.4.2 Disabled

The output can be shutdown by forcing the voltage of the EN pin to less than the $V_{IH(EN)}$ threshold (see the *セクション 5.5* table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the NR pin, SS pin and OUT pin voltages are actively discharged to ground by internal discharge circuits to ground when the IN pin voltage is higher than or equal to a diode-drop voltage.

6.4.3 Current-Limit Operation

If the output current is greater than or equal to the minimum current limit ($I_{LIM(Min)}$), then the device operates in current-limit mode. Current limit is a foldback implementation.

7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Precision Enable (External UVLO)

The precision enable circuit (EN pin) turns the device on and off. This circuit can be used to set an external undervoltage lockout (UVLO) voltage, as shown in 図 7-1, to turn on and off the device using a resistor divider between IN, EN, and GND.

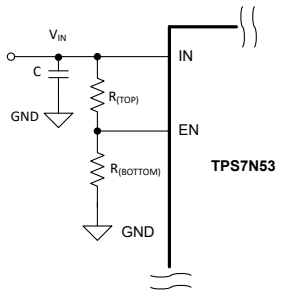


図 7-1. Precision EN Used as an External UVLO

This external UVLO solution is used to prevent the device from turning on when the input supply voltage is not high enough and can place the device in dropout operation. This solution also allows simple sequencing of multiple power supplies with a resistor divider from another supply. Another benefit from using a resistor divider to enable or disable the device is that the EN pin is never left floating because this pin does not have an internal pulldown resistor. However, a Zener diode can be needed between the EN pin and ground to comply with the absolute maximum ratings on this pin.

Use 式 2 and 式 3 to determine the correct resistor values.

$$V_{ON} = V_{OFF} \times [(V_{IH(EN)} + V_{HYS(EN)}) / V_{EN}] \quad (2)$$

$$R_{(TOP)} = R_{(BOTTOM)} \times (V_{OFF} / V_{IH(EN)} - 1) \quad (3)$$

where:

- V_{OFF} is the input voltage where the regulator turns off
- V_{ON} is the input voltage where the regulator turns on

注

For the EN pin input current, I_{EN}, effects are ignored.

7.1.2 Input and Output Capacitor Requirements (C_{IN} and C_{OUT})

The TPS7N53 is designed and characterized for operation with ceramic capacitors of 10 µF or greater at the output and 10µF or greater at the input. Use at least a 10µF capacitor at the input to minimize input impedance. Place the input and output capacitors as near as practical to the respective input and output pins to minimize trace parasitics. If the trace inductance from the input supply to the TPS7N53 is high, a fast current transient can cause V_{IN} to ring above the absolute maximum voltage rating and damage the device. This situation can be

mitigated by adding additional input capacitors to dampen the ringing, thereby keeping any voltage spike below the device absolute maximum ratings.

注

Because of the wide bandwidth, the LDO error amplifier can react faster than the output capacitor. In such a case, the load behavior appears directly on the LDO supply, potentially dragging the supply down. To avoid such behaviors, minimize both ESR and ESL present on the output; see the *Recommended Operating Conditions* table.

7.1.3 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) and low equivalent series inductance (ESL) ceramic capacitors at the input, output, and noise-reduction pin. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and COG-rated dielectric materials provide relatively good capacitive stability across temperature. The use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, ceramic capacitance varies with operating voltage and temperature. Make sure to take derating into consideration. The input and output capacitors recommended herein account for a capacitance derating of approximately 30%, but at high temperature, the derating can be greater than 50%, and must be taken into consideration.

The device requires input, output, and noise-reduction capacitors for proper operation of the LDO. Use the nominal or larger than nominal input and output capacitors as specified in the *Recommended Operating Conditions* table. Place input and output capacitors as close as possible to the corresponding pin and make the capacitor GND connections are as close as possible to the device GND pin to shorten transient currents on the return path. Using a larger input capacitor or a bank of capacitors with various values is always good design practice to counteract input trace inductance, improve transient response, and reduce input ripple and noise. Similarly, multiple capacitors on the output reduce charge pump ripple and optimize PSRR; see the *Optimizing Noise and PSRR* section.

Use the nominal soft-start C_{SS} capacitor because using a larger C_{SS} capacitor can lengthen the start-up time.

7.1.4 Soft-Start (SS Pin) and Noise Reduction (NR Pin)

The TPS7N53 has an SS pin and an NR pin to independently control the soft-start time and reducing the noise generated by the internal band-gap reference and the external resistor R_{REF}.

The device features a programmable, monotonic, voltage-controlled, soft-start circuit that is set to work with an external capacitor (C_{SS}). In addition to the soft-start feature, the C_{NR} capacitor lowers the output voltage noise of the LDO. The soft-start feature can be used to eliminate power-up initialization problems. The controlled output voltage ramp also reduces peak inrush current during start up, minimizing start-up transients to the input power bus.

To achieve a monotonic start up, the device output voltage tracks the V_{NR} reference voltage until this reference reaches the set value (the set output voltage). The V_{NR} reference voltage is set by the R_{REF} resistor and, during start up, the device uses a fast charging current (I_{SS}), as shown in 図 7-2, to charge the C_{SS} capacitor.

注

Any leakage on the NR and REF pins directly impacts the accuracy of the reference voltage.

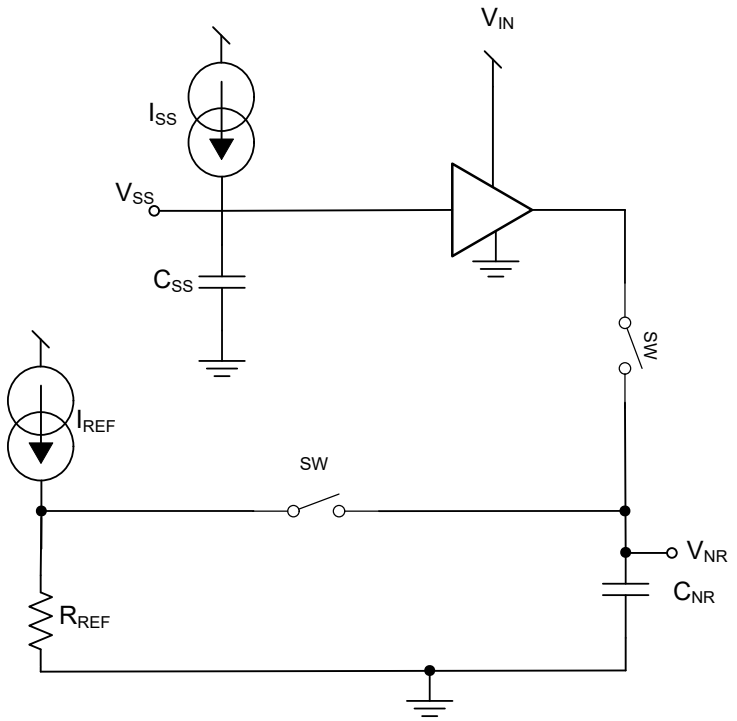


図 7-2. Simplified Soft-Start Circuit

The 30µA (typical) I_{SS} current quickly charges C_{SS} until the voltage reaches approximately 90% of the set output voltage, then the I_{SS} current turns off, the switch between NR and SS closes, as well as the switch between NR and REF.

注

The discharge pulldown resistor on NR and SS (see the *Functional Block Diagram*) is engaged when any of the GND referenced UVLOs have been tripped, or when any faults occur (overtemp, PORs, IREF bad, or OTP error) and the NR, SS pin voltages are above 50 mV.

The soft-start ramp time depends on the fast start-up (I_{SS}) charging current, the reference current (I_{REF}), C_{SS} capacitor value, and the targeted output voltage ($V_{OUT(target)}$). *式 4* calculates the soft-start ramp time.

$$\text{Soft-start time } (t_{SS}) = (V_{OUT(target)} \times C_{SS}) / (I_{SS}) \quad (4)$$

The I_{SS} current is provided in the *セクション 5.5* and has a value of 30µA (typical). The I_{REF} current has a value of 150µA (typical). The remaining 10% of the start-up time is determined by the $R_{REF} \times C_{NR}$ time constant.

The output voltage noise can be lowered significantly by increasing the C_{NR} capacitor. The C_{NR} capacitor and R_{REF} resistor form a low-pass filter (LPF) that filters out noise from the V_{REF} voltage reference, thereby reducing the device noise floor. The LPF is a single-pole filter and 式 5 calculates the LPF cutoff frequency. Increasing the C_{NR} capacitor can significantly lower output voltage noise. For low-noise applications, use a 1µF or larger C_{NR} for optimal noise.

$$\text{Cutoff Frequency } (f_{cutoff}) = 1 / (2 \times \pi \times R_{REF} \times C_{NR}) \quad (5)$$

注

Current limit can be entered during start up with a small C_{NR} and large C_{OUT} because V_{OUT} no longer tracks the soft-start ramp.

図 7-3 shows the impact of the C_{NR} capacitor on the LDO output voltage noise.

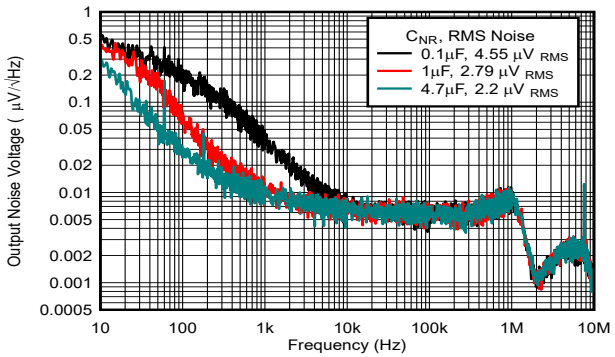


図 7-3. Output Voltage Noise Density vs C_{NR}

7.1.5 Charge Pump Noise

The device internal charge pump that has a switching frequency around 15MHz.

The high-frequency components of the output voltage noise density curve are filtered out in most applications by properly selecting C_{OUT}that have low impedance close to the chargepump frequency. Multiple capacitors in parallel can also help filter (typically within 10nF to 100nF range) the harmonics from the chargepump. In addition, using a ferrite bead between the LDO output and the load input capacitors forms a pi-filter, further reducing the high-frequency noise contribution. Please note that proper attention must be made when selecting a ferrite bead. The noise generated by the charge pump is shown in Charge Pump Noise.

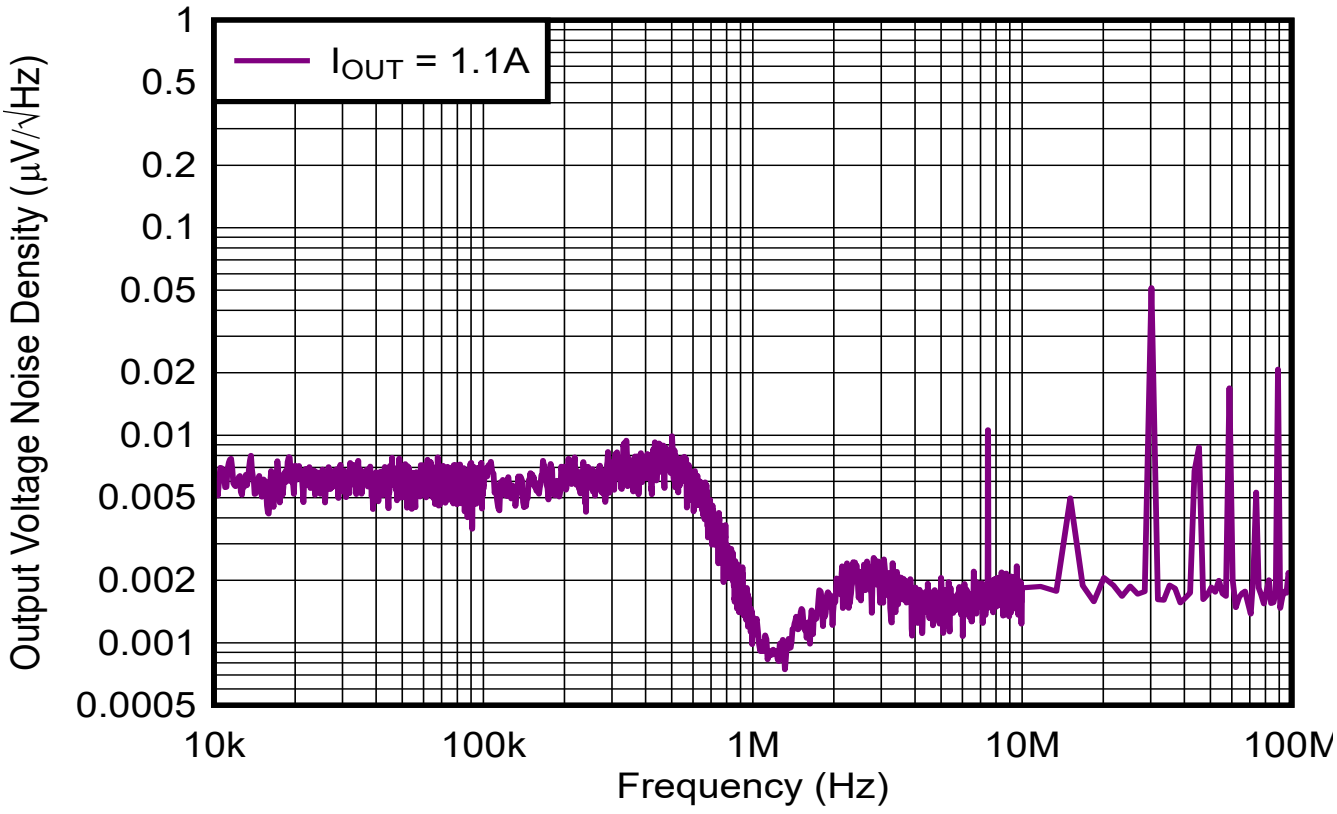


図 7-4. Charge Pump Noise

7.1.6 Optimizing Noise and PSRR

Noise can be generally defined as any unwanted signal combining with the desired signal (such as the regulated LDO output) that results in degraded power-supply source quality. Noise can be easily noticed in audio as a hissing or popping sound. Extrinsic and intrinsic are the two basic groups that noise can be categorized into. Noise produced from an external circuit or natural phenomena such as 50 to 60 hertz power-line noise (spikes), along with the harmonics, is an excellent representative of extrinsic noise. Intrinsic noise is produced by components within the device circuitry such as resistors and transistors. For this device, the two dominating sources of intrinsic noise are the error amplifier and the internal reference voltage (V_{REF}). Another term that sometimes combines with extrinsic noise is PSRR, which refers to the ability of the circuit or device to reject or filter out input supply noise and is expressed as a ratio of output voltage noise ripple to input voltage noise ripple.

Optimize the device intrinsic noise and PSRR by carefully selecting:

- C_{NR} for the low-frequency range up to the device bandwidth
- C_{OUT} for the high-frequency range close to and higher than the device bandwidth
- Operating headroom, $V_{IN} – V_{OUT}$ (V_{OpHr}), mainly for the low-frequency range up to the device bandwidth, but also for higher frequencies to a less effect

The device noise performance can be significantly improved by using a larger C_{NR} capacitor to filter out noise coupling from the input into the device V_{REF} reference. This coupling is especially apparent from low frequencies up to the device bandwidth. The low-pass filter formed by C_{NR} and R_{REF} can be designed to target low-frequency noise originating in the input supply. One downside of a larger $C_{NR/SS}$ capacitor is a longer start-up time. The device unity-gain configuration eliminates the noise performance degradation that other LDOs suffer from because of the feedback network. Furthermore, increasing the device load current has little to no effect on the device noise performance.

Further improvement to the device noise at a higher frequency range than the device bandwidth can be achieved by using a larger C_{OUT} capacitor. However, a larger C_{OUT} increases inrush current and slows down the device transient response.

Increasing the operational headroom between V_{IN} and V_{OUT} has little to no effect on improving noise performance. However, this increase does improve PSRR significantly for frequency ranges up to the device bandwidth. Higher headroom can also improve transient performance of the device as well. Although C_{OUT} has little to no affect on improving PSRR at low frequency, C_{OUT} can improve PSRR for higher frequencies beyond the device bandwidth. A combination of capacitors, such as 10 µF || 22µF provide and effective combination by lowering ESR and ESL. This behavior is illustrated in 図 5-3 .

表 7-1. Output Noise for 0.5-V_{OUT} vs C_{NR} and C_{OUT}

V_n (µV_{RMS}), 10-Hz to 100-kHz BW	C_{NR} (µF)	C_{OUT} (µF)
3.03	1	22
2.2	4.7	10

7.1.7 Adjustable Operation

As shown in 図 7-5, the output voltage of the device can be set using a single external resistor (R_{REF}).

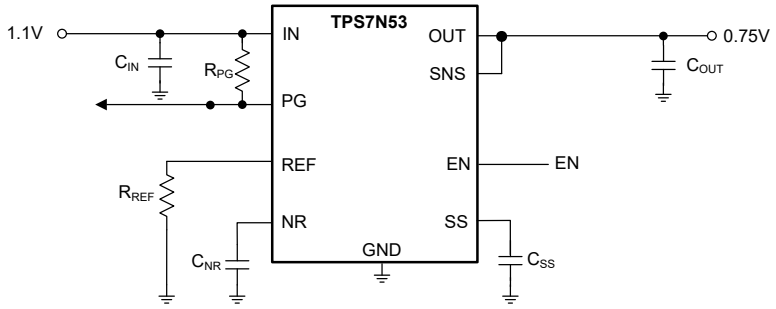


図 7-5. Typical Circuit

Use 式 6 to calculate the R_{REF} value needed for the desirable output voltage.

$$V_{OUT} = I_{REF(NOM)} \times R_{REF} \quad (6)$$

表 7-2 shows the recommended R_{REF} resistor values to achieve several common rails using a standard 1%-tolerance resistor.

表 7-2. Recommended R_{REF} Values

TARGETED OUTPUT VOLTAGE (V)	R_{REF} (kΩ)(1)	CALCULATED OUTPUT VOLTAGE (V)
0.5	3.3	0.495
0.6	4	0.600
0.7	4.7	0.705
0.8	5.36	0.804
0.9	6	0.900
1.0	6.68	1.002
1.2	8.06	1.209
1.5	10	1.500

(1) 1% resistors.

7.1.8 Load Transient Response

The load-step transient response is the LDO output voltage response to load current, whereby output voltage regulation is maintained. There are two key transitions during a load transient response: the transition from a light to a heavy load, and the transition from a heavy to a light load. The regions shown in 図 7-6 are broken down in this section. Regions A, E, and H are where the output voltage is in steady-state regulation.

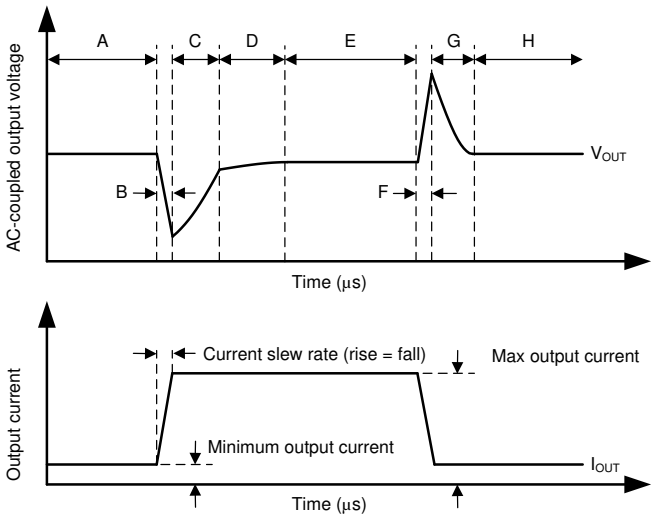


図 7-6. Load Transient Waveform

During transitions from a light load to a heavy load:

- The initial voltage dip is a result of the depletion of the output capacitor charge and parasitic impedance to the output capacitor (region B)
- Recovery from the dip results from the LDO increasing the sourcing current, and leads to output voltage regulation (region C)

During transitions from a heavy load to a light load:

- The initial voltage rise results from the LDO sourcing a large current, and leads to the output capacitor charge to increase (region F)
- Recovery from the rise results from the LDO decreasing the sourcing current in combination with the load discharging the output capacitor (region G)

Transitions between current levels changes the internal power dissipation because the device is a high-current device (region D). The change in power dissipation changes the die temperature during these transitions, and leads to a slightly different voltage level. This temperature-dependent output voltage level shows up in the various load transient responses.

A larger output capacitance reduces the peaks during a load transient but slows down the response time of the device. A larger dc load also reduces the peaks because the amplitude of the transition is lowered and a higher current discharge path is provided for the output capacitor.

注

The TPS7N53, with the high bandwidth, can react faster than the output capacitors. Verify that there is sufficient capacitance at the input of the LDO.

7.1.9 Power-Good Functionality

As described in the *Functional Block Diagram*, the PG pin is a open-drain MOSFET driven by a Schmitt trigger. The Schmitt trigger compares the SNS pin voltage to a preselected voltage equal to 90% that of the reference voltage.

As mentioned in the セクション 5.3 table, the pullup resistance must be between 10kΩ and 100kΩ for optimal performance. If the PG functionality is not desired, the PG pin can either be left floating or connected to GND.

7.1.10 Paralleling for Higher Output Current and Lower Noise

Achieving higher output current and lower noise is achievable by paralleling two or more LDOs. Implementation must be carefully planned out to optimize performance and minimize output current imbalance.

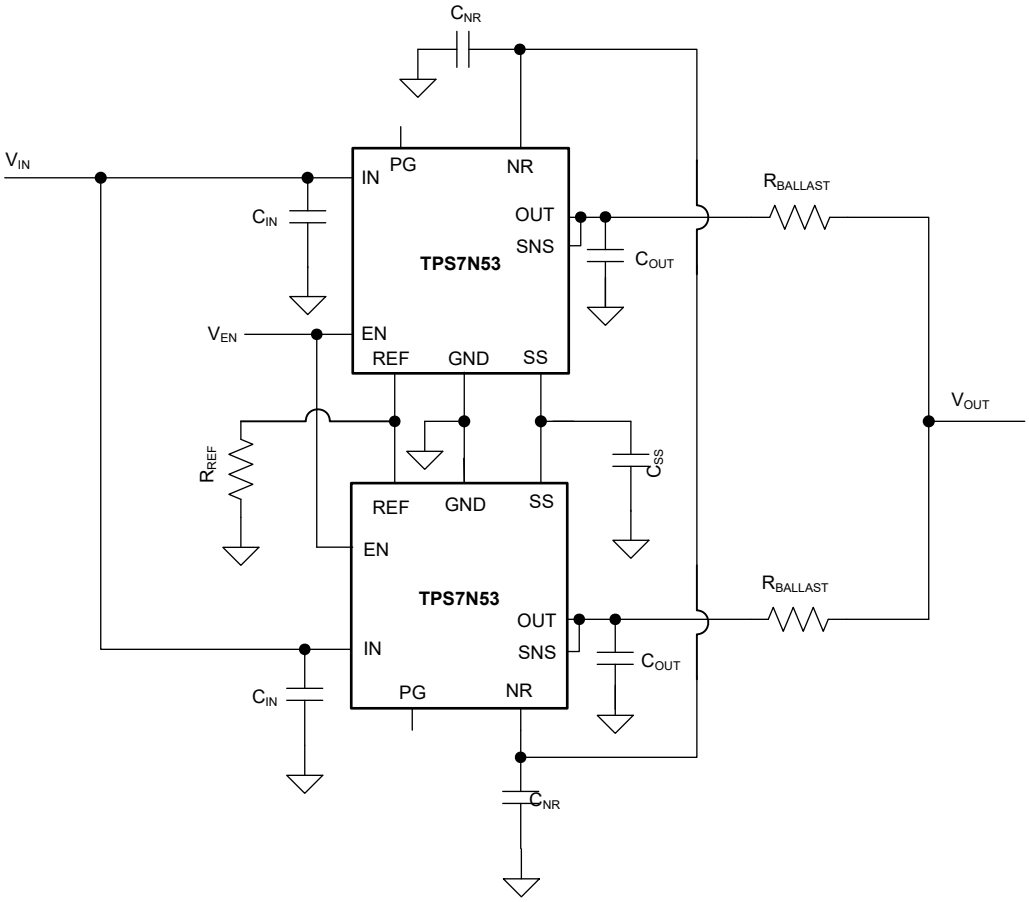


図 7-7. Paralleling Multiple TPS7N53 Devices

Please refer to the following documents for further information for paralleling LDOs:

- *Scalable, High-Current, Low-Noise Parallel LDO Reference Design* design guide
- *Parallel LDO Architecture Design Using Ballast Resistors* white paper
- *Comprehensive Analysis and Universal Equations for Parallel LDO's Using Ballast Resistors* white paper

7.1.11 Power Dissipation (P_D)

Circuit reliability demands that proper consideration be given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

As a first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. 式 7 calculates P_D:

$$P_D = (V_{OUT} - V_{IN}) \times I_{OUT} \quad (7)$$

注

Power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the device allows for maximum efficiency across a wide range of output voltages.

The primary heat conduction path for the package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane.

The power dissipation through the device determines the junction temperature (T_J) for the device. Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A), according to 式 8. The equation is rearranged for output current in 式 9.

$$T_J = T_A = (R_{\theta JA} \times P_D) \tag{8}$$

$$I_{OUT} = (T_J - T_A) / [R_{\theta JA} \times (V_{IN} - V_{OUT})] \tag{9}$$

Unfortunately, this thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Thermal Information* table is determined by the JEDEC standard, PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the RTE package junction-to-case (bottom) thermal resistance ($R_{\theta JCbot}$) plus the thermal resistance contribution by the PCB copper.

7.1.12 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are used in accordance with 式 10 and are given in the *セクション 5.5* table.

$$\Psi_{JT}: T_J = T_T + \Psi_{JT} \times P_D$$
$$\Psi_{JB}: T_J = T_B + \Psi_{JB} \times P_D \tag{10}$$

where:

- P_D is the power dissipated as explained in 式 7
- T_T is the temperature at the center-top of the device package
- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

7.2 Typical Application

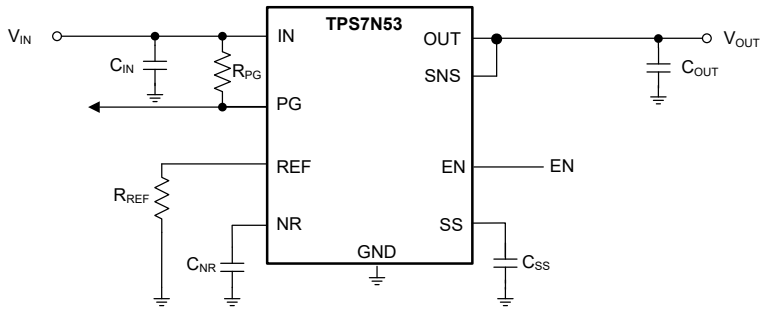


図 7-8. Typical Application Schematic

7.2.1 Design Requirements

The table below lists the required application parameters for this design example.

表 7-3. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	1.1V, ±2%, provided by the DC/DC converter switching at 1MHz
Output voltage	0.5V, 2%
Output current	3A (maximum), 1.1A (minimum)
Noise	Less than 5μV_{RMS}
PSRR at 10kHz	60dB at max load current
PSRR at 1MHz	> 30dB at max load current

7.2.2 Detailed Design Procedure

In this design example, the device is powered by a dc/dc convertor switching at 1 MHz. The load requires a 0.5V clean rail with less than 5μV_{RMS}. A 10μF input capacitor , 22μF output capacitor, 1μF NR capacitor, and 10nF SS capacitor are used to achieve a good balance between fast start-up time and excellent noise, and PSRR performance and load transient.

The output voltage is set using a 3.3kΩ, thin-film resistor value calculated as described in the *Output Voltage Setting and Regulation* section. The PG can be pulled up to V_{IN} pin using a 10kΩ to provide a Power-Good signal. The enable voltage is provided by a external I/O. 図 7-10 illustrates that the device meets all design noise requirements. 図 7-9 depicts adequate PSRR performance..

図 7-8 depicts the implementation of these components.

7.2.3 Application Curves

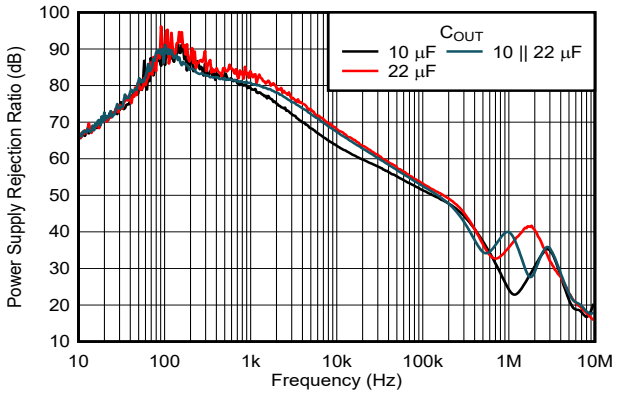


図 7-9. PSRR vs Frequency

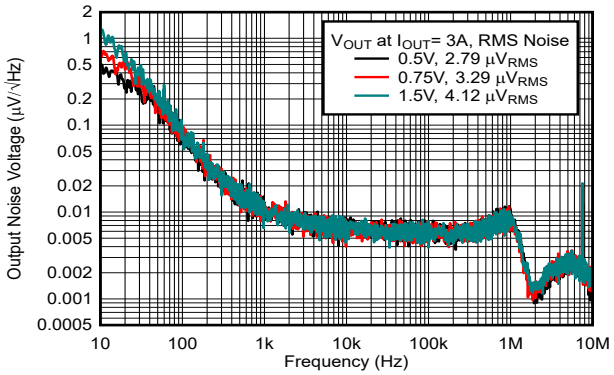


図 7-10. Noise vs Frequency

7.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply ranging from 1.1 V to 2.2 V. Ensure that the input voltage range provides adequate operational headroom for the device to have a regulated output. This input supply must be well regulated and low impedance. If the input supply is noisy, use additional input capacitors with low ESR and increase the operating headroom to achieve the desired output noise, PSRR, and load transient performance. There is no sequencing requirement between IN and EN.

7.4 Layout

7.4.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. To avoid negative system performance, do not use vias and long traces to the input and output capacitors. The grounding and layout scheme illustrated in 図 7-11 minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability.

Because of the wide bandwidth and high output current capability, inductance present on the output negatively impacts load transient response. For best performance, minimize trace inductance between the output and load. A low ESL capacitor combined with low trace inductance limits the total inductance present on the output and optimizes the high-frequency PSRR.

To improve thermal and overall performance, use a ground reference plane, either embedded in the PCB or placed on the bottom side of the PCB opposite the components. This reference plane serves to verify accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device when connected to the thermal pad. In most applications, this ground plane is necessary to meet thermal requirements. Use as many vias as possible under the thermal pad to help spread (or sink) the heat from the LDO to the GND planes underneath.

7.4.2 Layout Example

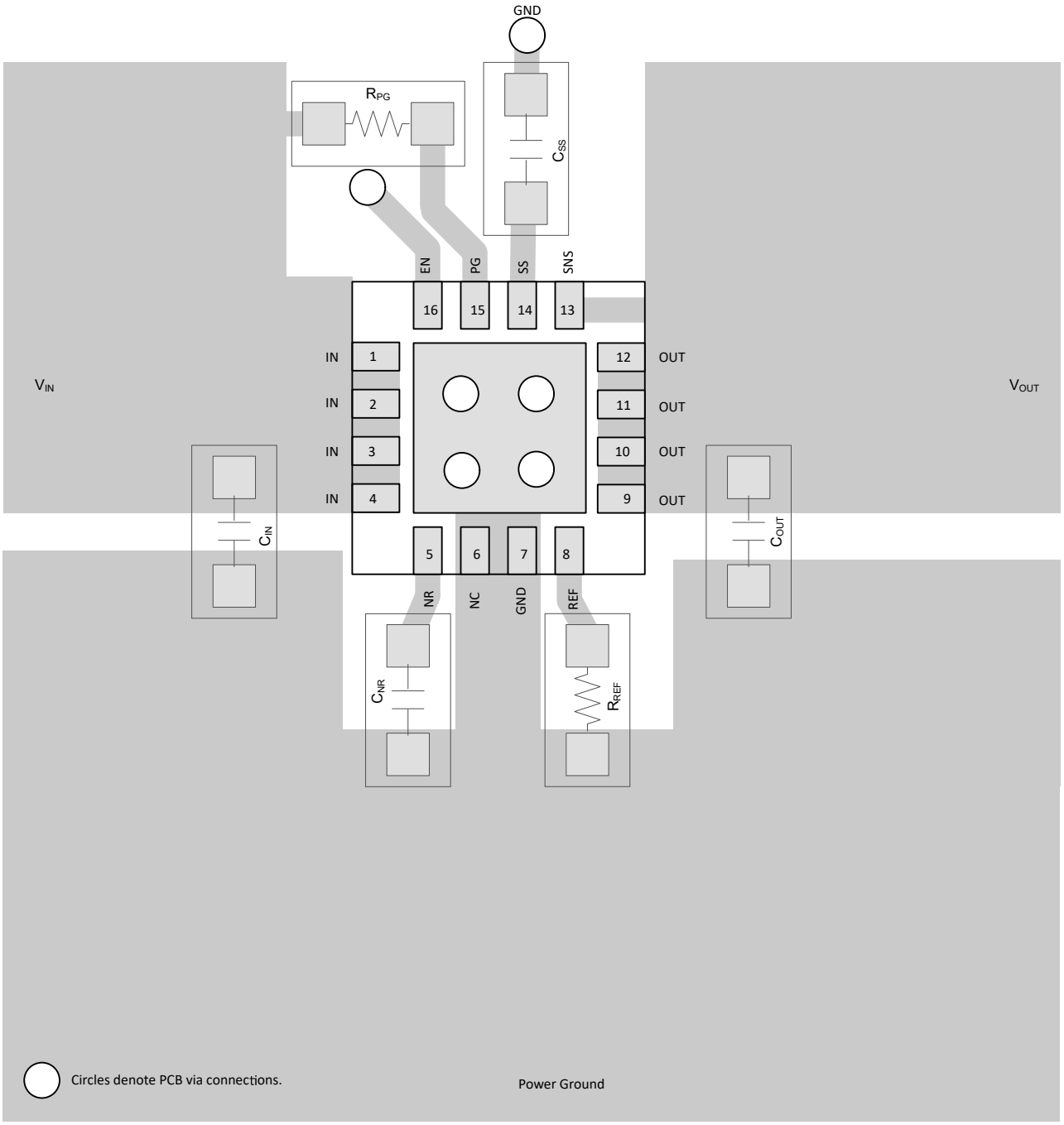


図 7-11. Recommended Layout

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *High-Current, Low-Noise Parallel LDO Reference Design* design guide

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

8.4 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

8.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (October 2024) to Revision A (December 2024)	Page
• 特長を追加	1
• ドキュメントのステータスを「事前情報」から初回リリースに更新。	1

10 Mechanical, Packaging, and Orderable Information

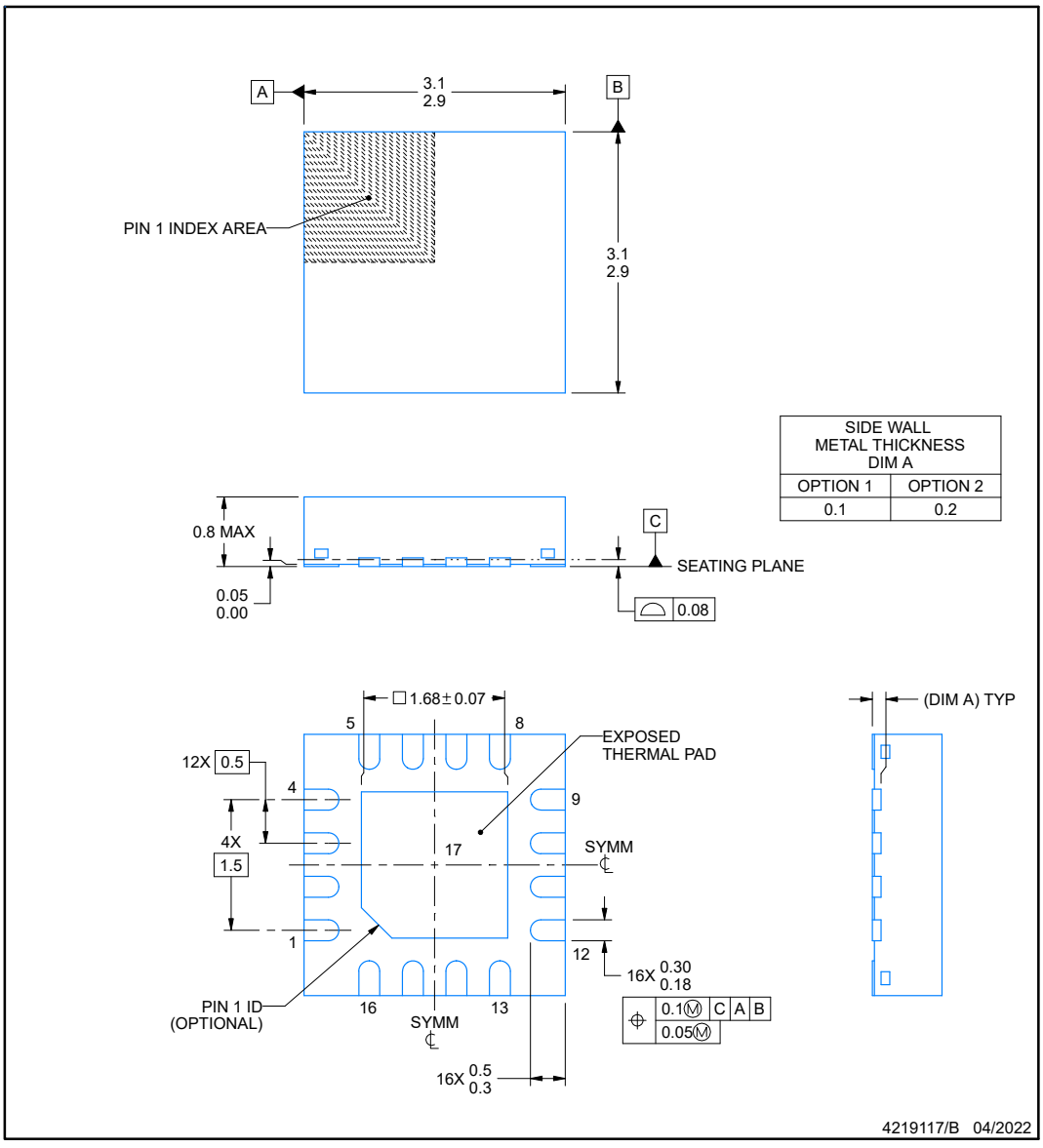
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

RTE0016C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

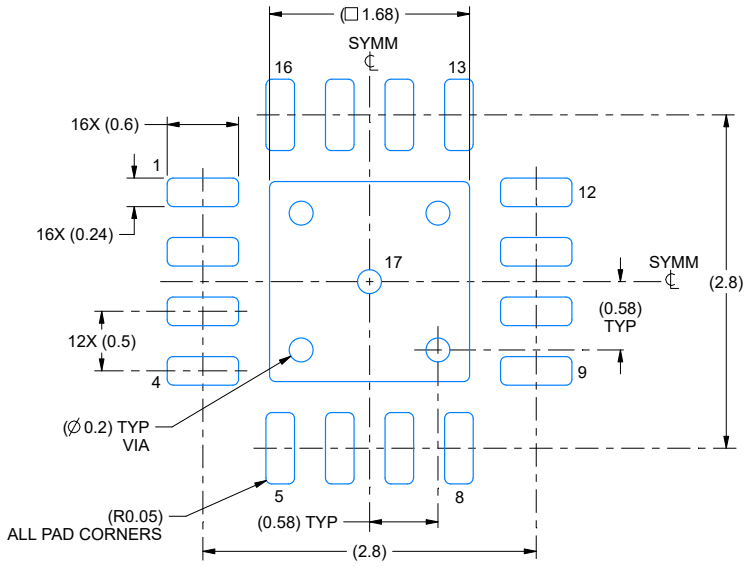
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

TEXAS INSTRUMENTS
www.ti.com

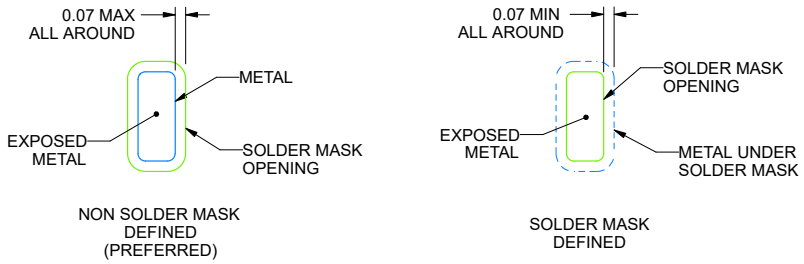
EXAMPLE BOARD LAYOUT

RTE0016C — **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4219117/B 04/2022

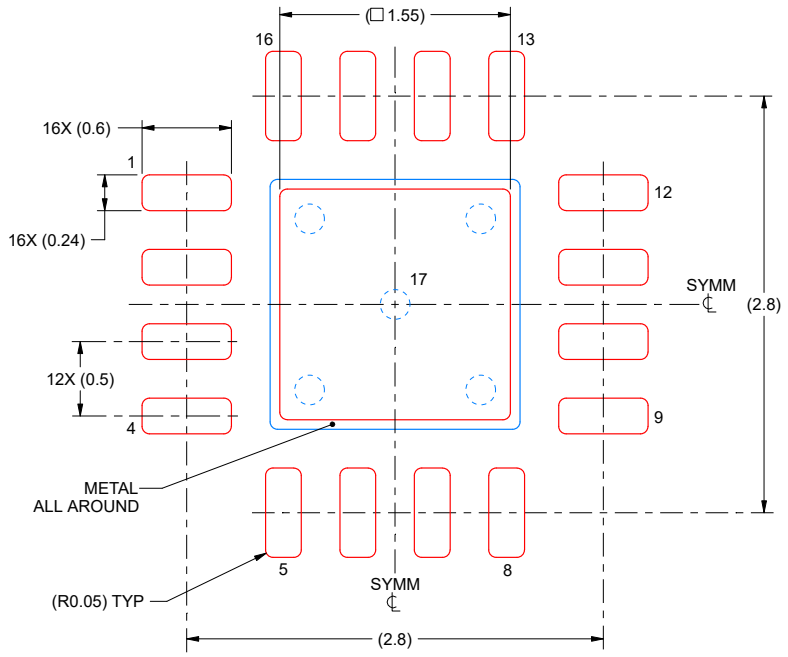
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RTE0016C — **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219117/B 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

10.1 Package Option Addendum

Packaging Information

Orderable Device	Status(1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead/Ball Finish(6)	MSL Peak Temp(3)	Op Temp (°C)	Device Marking(4) (5)
PTPS7N5301RTER	ACTIVE	WQFN	RTE	16	5000	RoHS & Green	NIPDAU	Level-1-260CG-2 Years	-40 to 125	P7N53

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7N5301RTER	Active	Production	WQFN (RTE) | 16	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7N5301
TPS7N5301RTER.A	Active	Production	WQFN (RTE) | 16	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7N5301

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

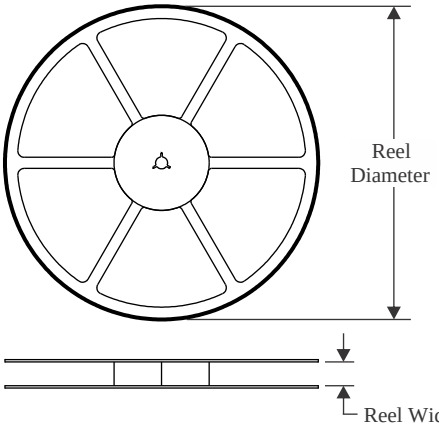
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

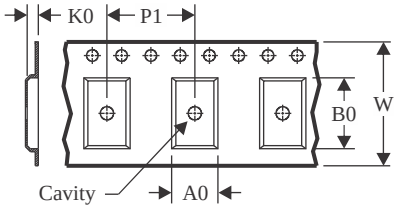
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

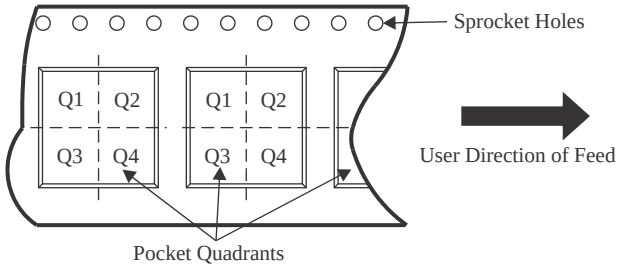


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

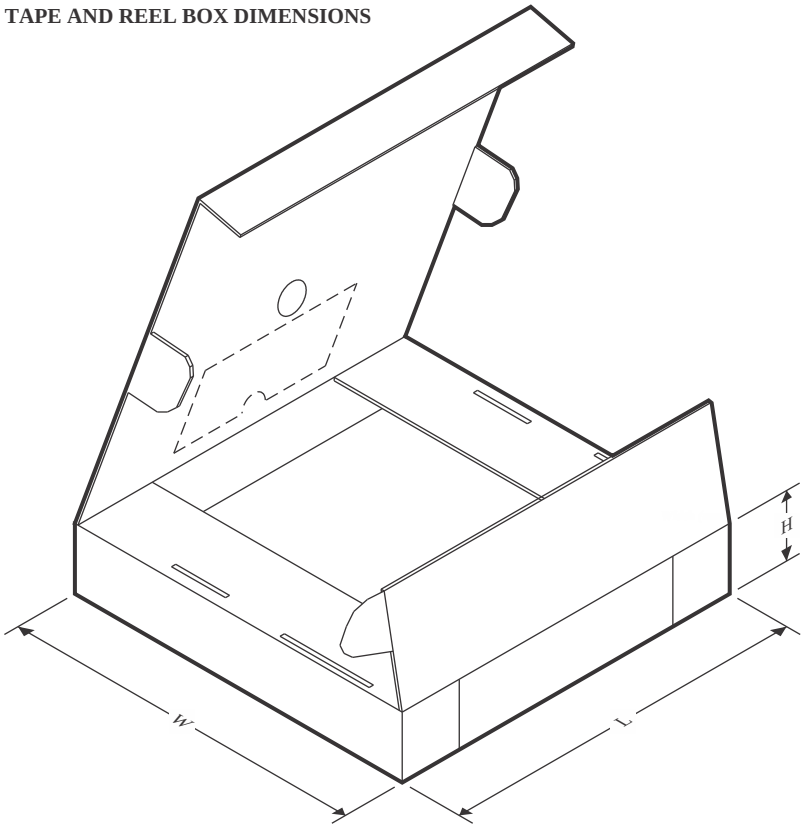
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7N5301RTER	WQFN	RTE	16	5000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7N5301RTER	WQFN	RTE	16	5000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

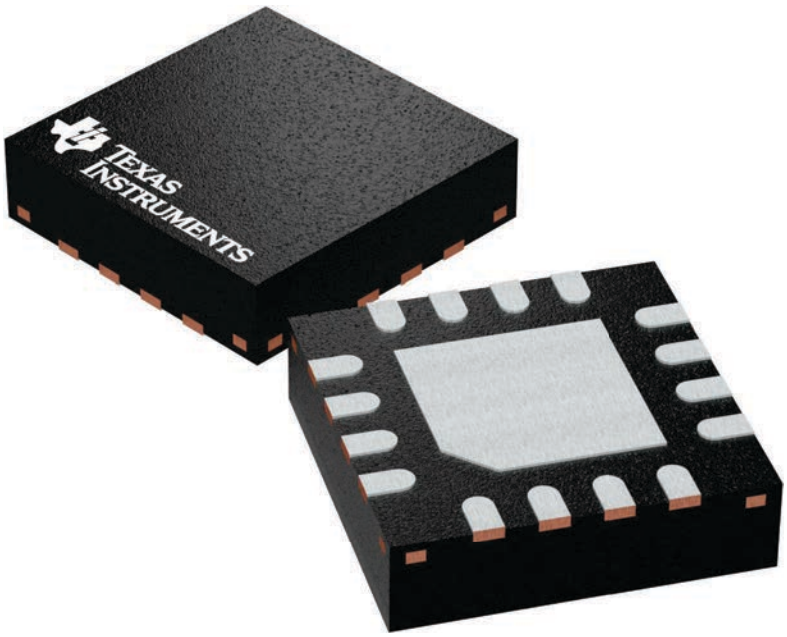
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

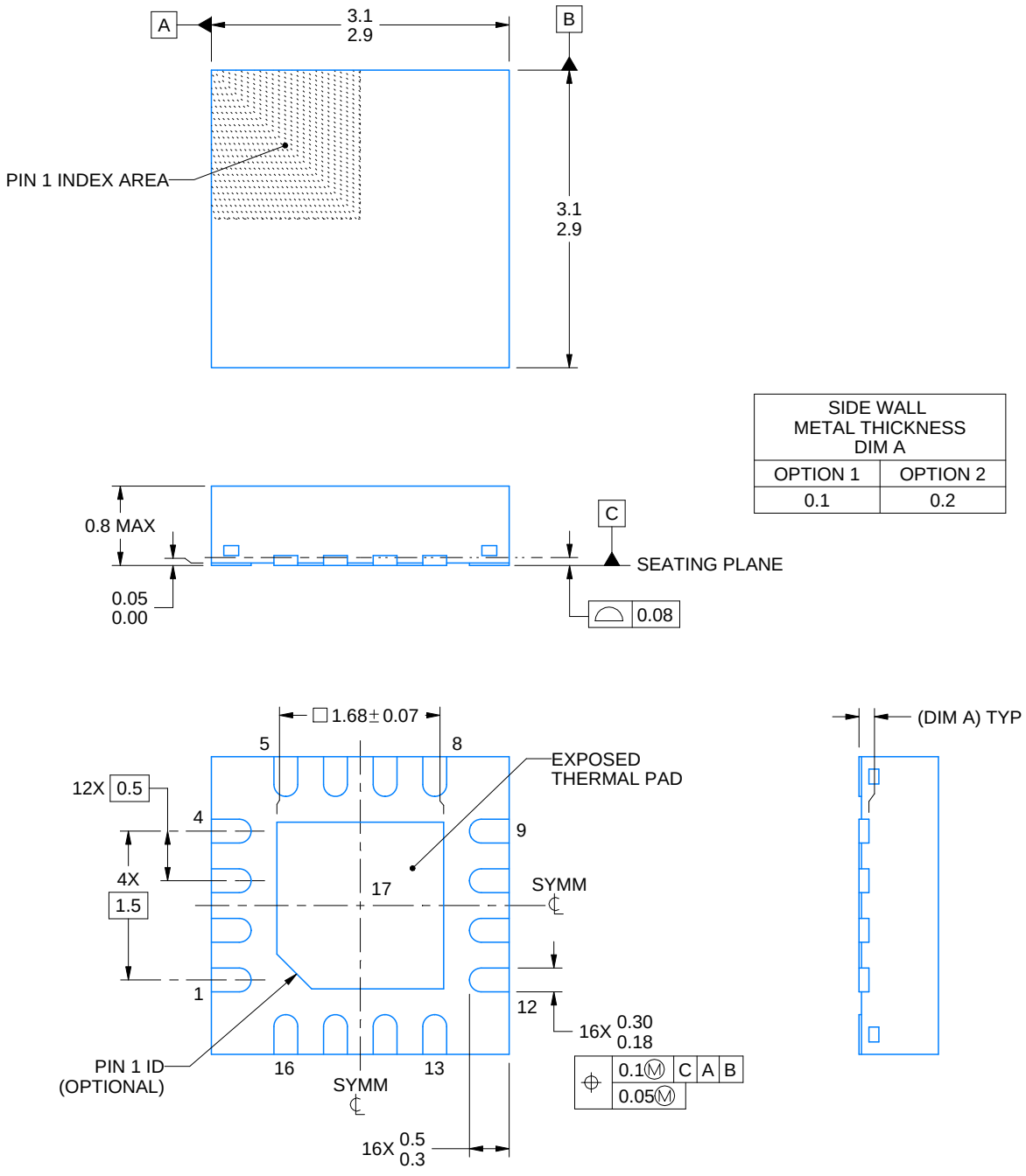


RTE0016C

PACKAGE OUTLINE

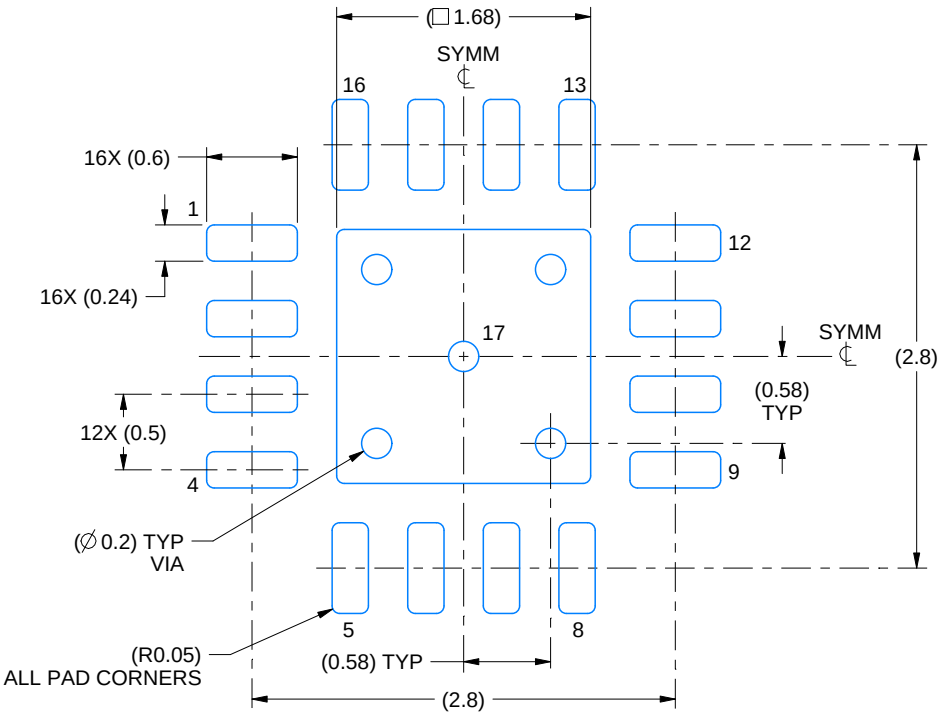
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

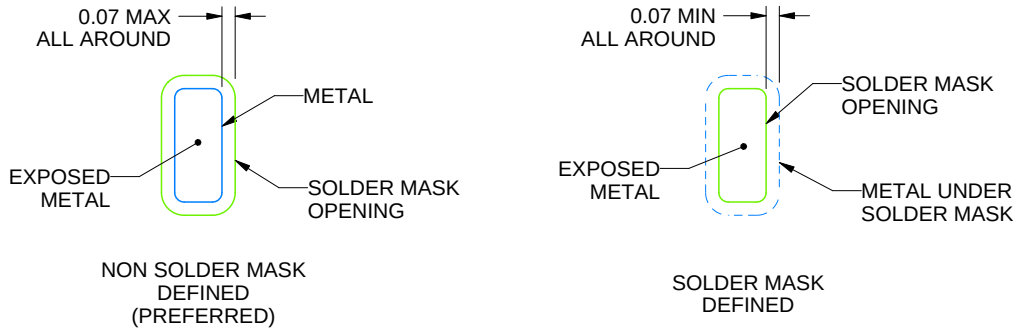


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

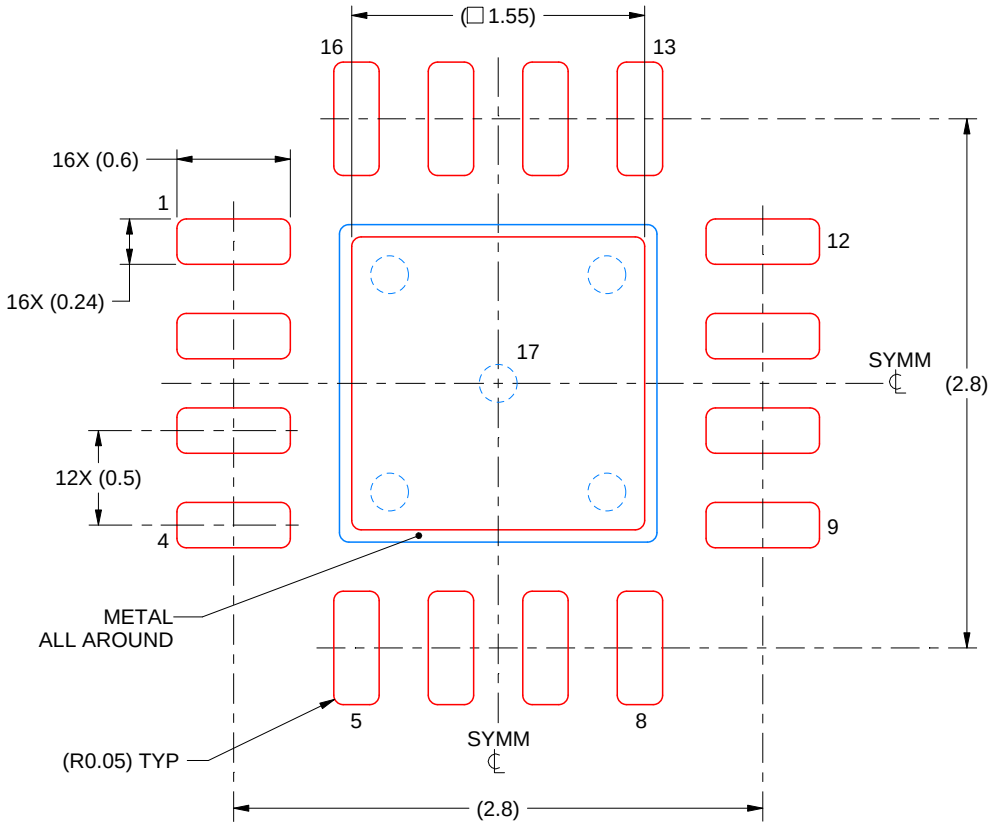


SOLDER MASK DETAILS

4219117/B 04/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219117/B 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、 TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

最終更新日：2025 年 10 月